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REVIEW OPEN ACCESS

A Comprehensive Review of Fault-Current Limiter Technologies for Smart and Resilient Power Systems

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ABSTRACT

The transition toward inverter-dominated, renewable-rich power systems has significantly increased short-circuit levels, often exceeding the interrupting capability of conventional protection. Fault-current limiters (FCLs) have emerged as important technologies for mitigating these currents and supporting grid reliability. This article provides a comprehensive, system-oriented review that bridges device-level FCL characteristics with grid-level requirements across alternating current, direct current (DC), and hybrid networks. It systematically categorizes and evaluates superconducting FCL, solid-state FCL, and hybrid FCL technologies, detailing their operating principles, dynamic fault responses, and control strategies. A structured comparison framework is established to assess the trade-offs among current-limiting capability, response speed, steady-state losses, cost, and technical maturity. In addition to device-level classification, the review examines fault-current behavior in modern grids by considering inverter-limited fault currents (inverter-based resource saturation), DC offset decay dynamics, and asymmetrical fault conditions using symmetrical components. The review also examines the coordination of FCLs with adaptive protection schemes and considers optimization approaches for FCL placement and sizing in converter-dominated networks. The findings indicate that no single FCL technology is universally superior; optimal selection depends on specific operating constraints, fault characteristics, and voltage levels. Finally, the review highlights several areas that warrant further investigation, including standardized benchmarking, long-term field validation, and improved integration with modern control architectures.

1 | Introduction

Historically, distribution networks were small and simple to install, and their generation capacities were limited [1]. Therefore, fault currents did not pose a significant risk when faults occurred; consequently, conventional protection devices, such as circuit breakers (CBs), fuses, and overcurrent relays, were used to detect and interrupt fault currents, thereby disconnecting and isolating the faulted section from the rest of the network [2]. These protection devices were not designed to

handle the enormous fault currents that would arise from the expansion of larger interconnected grids; however, they were adequate for the smaller grids that existed at the time.

Currently, the integration of renewable energy sources (RESs) and distributed generation (DG) has increased grid complexity and introduced bidirectional flows [3, 4]. The impact of this integration on fault characteristics is highly nuanced. At the device level, grid-connected inverters typically restrict their

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short-circuit contribution to 1.0–1.5 times their rated current to prevent thermal damage to sensitive power-electronic switches. However, at the macro-system level, the sheer aggregation of these resources at main substation buses, combined with decreased equivalent grid impedance, can drive prospective fault levels beyond the interrupting ratings of existing CBs. At the other end of the spectrum, in highly distributed or islanded microgrids, the inherently limited fault currents of inverter-based resources (IBRs) often fail to trip standard overcurrent relays, thereby rendering conventional protection schemes blind. Such excessive currents cause severe mechanical stress, insulation failure, and the risk of fire. Furthermore, they risk CB failure and cause current transformer (CT) saturation, leading to maloperation of protection and system instability [5, 6]. The scale and urgency of this transition are no longer speculative: global renewable power capacity reached 4448 GW by the end of 2024, following a record single-year addition of 585 GW (15.1% growth), with variable renewable capacity-solar and wind-expanding by 23.3% to reach 31.2% of total installed renewable capacity [7]. This rapid displacement of synchronous generation by inverter-interfaced sources has already led to documented protection failures in operating bulk power systems. On August 16, 2016, transmission faults induced by the Blue Cut Fire in Southern California cleared normally within 2.5 cycles by conventional protection; nonetheless, they caused approximately 1200 MW of utility-scale solar photovoltaic (PV) generation to disconnect, entirely due to erroneous inverter control responses rather than any breaker or relay misoperation [8]. A comparable event on October 9, 2017 (Canyon 2 Fire) resulted in the loss of approximately 900 MW of solar PV generation from a single, normally cleared phase-to-phase fault [9]. These incidents illustrate that the interaction between fault-current behavior and protection performance in inverter-dominated grids, quantified further through the relay-sensitivity analysis in Section 4.1, is a demonstrated reliability concern rather than a theoretical refinement, directly motivating the system-oriented contributions of this review.

To address this problem, various measures have been implemented to reduce fault current in modern power system transmission and distribution networks. Figure 1 presents a standard categorization of fault-current strategies. The fundamental objective of fault-current-limiting methodologies is to limit fault current to predetermined thresholds by either reducing short-circuit current levels or inserting a high-impedance element into the fault path. As illustrated in Figure 1, these measures can be categorized as active or passive [10, 11].

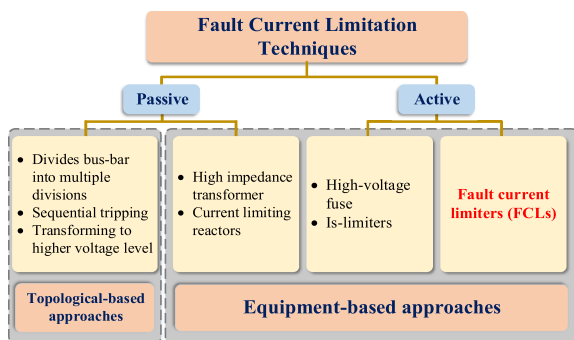


FIGURE 1 | Classification of fault-current-limiting measures.

The term “passivity” refers to measures that maintain a specific configuration regardless of network conditions. Bus splitting during a fault is a typical example. It raises the system impedance to prevent excessive increases in fault currents [12]. However, this permanent structural change complicates matters, making protection coordination more difficult and increasing recovery time [13]. In sequential tripping, protective devices operate sequentially to isolate faults rather than tripping simultaneously. Although this method can detect errors, it leads to slow error resolution, high equipment load, complex coordinate settings, and potential cascading errors [14]. Another topological strategy involves supplying a weak subsystem with power from a stronger upstream network, thereby increasing its short-circuiting capability [15]. These methods change the network configuration and are therefore classified as “topological-based approaches” as illustrated in Figure 1. In addition to passive techniques such as high-impedance transformers and current-limiting reactors, which reduce fault currents by increasing system impedance. However, they introduce voltage drops and additional power losses during regular operation [16, 17], thus they are classified as “Equipment-based approaches.”

The term “active” refers to methods that remain inactive during normal operation and are activated only upon failure. For example, fuses are a popular choice due to their low cost, reliability, and subcycle operating speed. However, disposables require manual replacement, resulting in long-term downtime [18, 19]. The Is-limiter is an ultrafast-acting device that fundamentally differs from ordinary mechanical switches. It primarily consists of a pyrotechnic commutating switch coupled in tandem with a high-rated current-limiting fuse. During normal operation, the continuous load current flows via the low-impedance main bridge. When a short circuit occurs, an electronic measuring device instantaneously detects the sharp current surge (di/dt) [20]. Within about 1 ms, a pyrotechnic charge is ignited, actively rupturing (blowing) the primary conductor. This explosive action drives the fault current to commute into the parallel fuse, which subsequently melts, restricting the fault current before it reaches its initial asymmetrical peak. It is vital to note that the Is-limiter is a sacrificial device, not a simple reusable contactor; once it functions, the pyrotechnic insert and the parallel fuse are entirely blown and must be manually replaced to restore the system.

Fault-current limiters (FCLs) have emerged to address these limitations by actively limiting the peak fault current [21, 22]. By mitigating electrical and thermal stress during faults, FCLs protect infrastructure, increase network reliability, and enable the use of lower-rated equipment [23–26].

In contemporary power systems, the necessity for fault-current limitation is increasingly influenced by inverter-dominated grids, microgrids, high-voltage direct current (HVDC) networks, and extensive integration of renewable energy, rather than solely by the expansion of classic synchronous-machine systems. Converter-rich systems exhibit distinct short-circuit characteristics, narrower protection margins, and more stringent ride-through and selectivity requirements, thereby making the coordination of FCL technologies, power-electronic interfaces, and protection schemes a pivotal challenge for smart and resilient grids. This review emphasizes both the device-level

characteristics of superconductor FCL (SFCL), solid-state FCL (SSFCL), and hybrid FCL (HFCL) technologies and their significance in ensuring the dependable operation of inverter-dominated distribution feeders, microgrids, and HVDC systems with substantial integration of RESs. Classified as active, device-based mitigation strategies, these limiters are detailed in Section 2.

Fault research in smart and resilient power systems increasingly extends beyond current-limiting hardware to encompass complementary detection and diagnostic layers operating at different stages of the fault lifecycle. At the pre-fault stage, gas-sensor-array techniques have been developed to identify thermal fault states in cable insulation sheaths from volatile gas signatures released during early-stage overheating, enabling detection before an electrical fault develops [27]. At the coordination layer, multiagent systems combined with artificial intelligence have been proposed to automate fault diagnosis, isolation, and recovery in specialized power infrastructures such as subway traction power systems, extending the self-healing and adaptive-coordination concepts discussed later in this review (Sections 3.5, 4.2, and 4.3) to adomains not otherwise addressed here [28]. At the post-fault diagnostic stage, intelligent approaches based on dissolved gas analysis, including neural networks, fuzzy theory, rough sets, and swarm intelligence, have matured substantially for oil-immersed power transformers, offering a methodologically instructive parallel to the optimization-based FCL allocation techniques surveyed in Section 4.1 [29]. These directions are complementary to, rather than a substitute for, the fault-current-limitation focus of this review: they address the detection and diagnosis of fault conditions, whereas FCLs act directly on the fault current itself once a fault occurs. Their inclusion here underscores that FCL technology forms one component of a broader, increasingly multimodal fault-management ecosystem in smart and resilient power systems.

1.1 | Contributions to This Review

The current FCL reviews have given useful coverage of device classifications, operating principles, structural configurations, and selected technical characteristics. This review extends this literature by using a system-oriented perspective to link FCL behavior to protection, converter-dominated networks, and emerging smart-grid requirements. The main areas considered in the review are summarized as follows:

- *Mathematical Formulation of Inverter-Dominated Grid Faults*: This review synthesizes and examines the mathematical representations of fault currents in converter-dominated networks, moving beyond standard linear models of synchronous-generator-dominated grids. Specifically, it systematically discusses the integration of piecewise nonlinear inverter current saturation boundaries, mixed-source short-circuit contributions, and dual-rate control-driven direct current (DC) offset dynamics. Furthermore, it incorporates the symmetrical components framework to analyze asymmetrical fault conditions, including zero-sequence impedance-netting behavior under single line-to-ground (SLG) scenarios.
- *Advanced Power Electronic and Control-Loop Interlocking (MMCs)*: This article presents a comprehensive synthesis of the relationship between FCL parameters and the modular

multilevel converter (MMC) architectures, the dominant topology for utility-scale VSC-HVDC and medium-voltage direct current (MVDC) systems. The review discusses, in particular, the current models of transient fault evolution in three-stage MMC (submodule [SM] capacitor discharge, freewheeling diode conduction, and steady-state rectification). In addition, it describes quantitative placement trade-offs (DC-side, arm, and alternating current [AC]-side) and the mathematical limits of arm energy deviations (ΔW_{arm}) reported in the literature to avoid SM capacitor voltage balancing disturbances and cascaded protection bypasses.

- *Quantitative Smart-Grid Communication Engineering*: The review systematically synthesizes stringent quantitative criteria required for communication-assisted adaptive protection coordination, going beyond qualitative discussions. More specifically, it collects and analyzes well-known normative limits on communication latency (e.g., IEC 61850-5 Classes P2/P3 and GOOSE multicast < 4 ms), bandwidth profiles for substations for sample value (SV) and wide-area measurement systems (WAMSs), and synchronized timing constraints ($\pm 1 \mu\text{s}$ via IEEE 1588 PTP). It also covers important cybersecurity threat vector mitigations (FDI, MitM, DoS, etc.) as they relate to IEC 62351/62443 compliance.
- *Analytical Uncertainty Modeling and Optimization Meta-Analysis*: This review provides a detailed mathematical synthesis and critical evaluation of modern optimization frameworks applied to the allocation (placement and sizing) of FCLs under high renewable stochasticity and load variations. Specifically, it examines the operational formulations of Two-Stage Stochastic programming (e.g., solved via sample average approximation (SAA)), robust Min-Max optimization (incorporating the budget-of-uncertainty parameter, Γ).
- *Multiscenario Grid Applications and the Weather Resilience Envelope*: To evaluate real-world utility-scale survivability, this review synthesizes a preliminary, illustrative “Weather Resilience Envelope” framework based on established thermal, structural, and electrical principles. This conceptual framework characterizes FCL performance under extreme atmospheric multihazard, examining parameters, such as adiabatic thermal ride-through limits (dT/dt) during cooling outages and Category 5 aerodynamic wind forces (F_{wind}) for enclosure hardening, serving as a concrete baseline for future experimental or numerical validation. Furthermore, the article integrates design-centric HVDC benchmarks derived from actual direct current circuit breaker (DCCB) standards and outlines a multidimensional, scenario-driven deployment matrix encompassing distributed energy resource (DER)-dense feeders, microgrids, and meshed networks.

Several literature reviews on FCL technologies have been published in recent years, most notably by Safaei et al. [5], Majeed et al. [16], and Chowdhury and Bhaumik [30]. These works offer valuable and comprehensive coverage of FCL device physics, structural variants, and comparative technical parameters, and are drawn upon throughout this review. Table 1 benchmarks the scope of the present work against these representative reviews across six specific dimensions. This comparison emphasizes topics that receive limited collective attention in existing literature, thereby highlighting the comprehensive, system-oriented synthesis adopted in our work.

It should be noted that this review is best understood, in the typology of Grant and Booth [31], as a *critical review*: a review form that, unlike a purely narrative or systematic review, explicitly synthesizes established theoretical relations into an integrated analytical framework and, where appropriate, derives new organizing models from that synthesis. Accordingly, the analytical formulations developed in Sections 2–5 draw on individually established and cited physical, control, and optimization relations from the reviewed literature; their role in this review is to consolidate and systematize these relations into a coherent, system-level picture of FCL behavior, rather than to report new experimentally or numerically validated findings. Quantitative illustrations computed from representative parameter values (Sections 5.1 and 5.2) are presented explicitly as order-of-magnitude design references for this purpose and are distinguished in the text from field- or simulation-validated results reported directly from the cited literature.

1.2 | Review Methodology

This review adopts a critical, synthesis-oriented methodology in the sense of Grant and Booth [31], rather than a formal systematic-review protocol. To improve transparency in literature identification, targeted searches were conducted using combinations of terms, such as “fault current limiter,” “fault current limiting,” “grid-forming inverter fault current,” “optimal location/allocation of FCL,” “FCL protection coordination,” and “FCL review.” Relevant literature was identified through commonly used scholarly search platforms, including Scopus, Google Scholar, IEEE Xplore, ScienceDirect, Wiley Online Library, and MDPI. The search initially focused on publications from approximately 2005 to 2024, while additional recent studies were incorporated during manuscript preparation and revision to capture developments in IBRs, adaptive protection, and HVDC systems. Studies were considered eligible when they directly addressed FCL technologies, fault-current behavior, control, protection coordination, placement or sizing, or applications in inverter-dominated, renewable-rich, micro-grid, or HVDC systems. Studies with limited relevance to these topics were excluded from the core synthesis. Peer-reviewed English-language journal articles constituted the primary literature base, while conference papers, standards, and technical reports were included selectively when they provided relevant technical benchmarks, standards, or operational context not otherwise available in the journal literature. The retained sources were then comparatively synthesized based on device characteristics, fault behavior, protection and control interactions, optimization approaches, and application context.

The remainder of this article organized as follows: Section 2 introduces the concept and role of FCLs. Section 3 reviews FCL properties under normal and fault conditions and examines various FCL types. Section 4 discusses coordinating conventional protection devices with FCLs, as well as optimal FCL parameters and placement in power systems. Section 5 addresses current challenges and future developments; Finally, Section 6 concludes the paper.

TABLE 1 | Positioning of this review relative to existing FCL literature reviews.

Dimension	Safaei et al. [5]	Majeed et al. [16]	Chowdhury and Bhaumik [30]	This review
SFCL/SSFCL/HFCL device classification	✓	✓	✓	✓
Analytical fault-current modeling (symmetrical components)	Qualitative only	Qualitative only	Qualitative only	✓
MMC/HVDC control-loop integration (submodule level)	Not a primary focus	Not a primary focus	Not a primary focus	✓
Quantitative communication and cybersecurity engineering (IEC 61850, PTP, FDI/MitM/DoS)	Not a primary focus	Not a primary focus	Not a primary focus	✓
Optimization meta-analysis (stochastic/robust/chance-constrained)	Brief mention	Not a primary focus	Not a primary focus	✓
Scenario-based climate-resilience deployment guidance	Not a primary focus	Not a primary focus	Not a primary focus	✓

Abbreviations: DoS, denial-of-service; FCL, fault-current limiter; FDI, false data injection; HFCL, hybrid FCL; HVDC, high-voltage direct current; MitM, man-in-the-middle; MMC, modular multilevel converter; PTP, precision time protocol; SFCL, superconductor FCL; SSFCL, solid-state FCL.

2 | FCL Concept

According to IEEE STD C37.02, an FCL is a protective device that minimizes the first-peak and RMS fault currents by inserting resistive or reactive impedance into the system during a fault [32]. Figure 2a illustrates that numerous new power plants and DG units are expected to be connected to power grids, primarily due to the expansion of the power system and advances in renewable energy production technologies.

A parallel impedance connection of sources certainly minimizes the equivalent impedance. It results in an increase in the current value during the faults. Equation (1) explains the fault-current magnitude.

$$I_{\text{fault}} = \frac{V_s}{Z_s + Z_{\text{fault}}} \quad (1)$$

The system can be adjusted by incorporating an FCL, thereby increasing the circuit's total impedance and avoiding fault-current issues, as shown in Figure 2b. The fault current can be explained in Equation (2).

$$I_{\text{fault}} = \frac{V_s}{Z_s + Z_{\text{FCL}} + Z_{\text{fault}}} \quad (2)$$

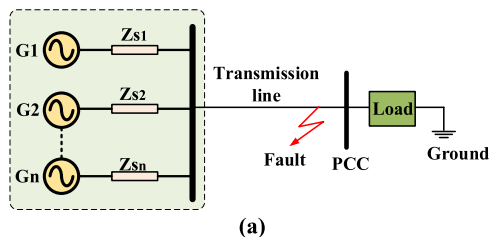
Fault-current properties in the presence of an FCL may also be determined through analysis. Figure 3 illustrates the equivalent circuit of a basic power system. During a short circuit in the system, the current starts to increase at a defined rate, which depends on various system elements, including source resistance (R), source inductance (L), the load angle (δ), and the voltage angle at the fault beginning (α). In addition, the specifications of the FCL should be included, which consists of two components: a resistive (R_{FCL}) and an inductive component (L_{FCL}).

The following equation illustrates the action of fault current, including the FCL impedance [33].

$$(L_s + L_{\text{FCL}}) \frac{di(t)}{dt} + (R_s + R_{\text{FCL}})i(t) = V_m \sin(\omega t + \delta + \alpha) \quad (3)$$

The instantaneous fault current may be computed after solving the previous equation as follows:

$$i(t) = i_{\text{AC}}(t) + i_{\text{DC}}(t) = \frac{V_m}{Z} \left[\sin(\omega t + \alpha + \delta - \varphi) - e^{-\frac{t}{\tau}} \sin(\alpha + \delta - \varphi) \right] \quad (4)$$



where

$$Z = \sqrt{(R_s + R_{\text{FCL}})^2 + \omega^2(L_s + L_{\text{FCL}})^2} \quad (5)$$

$$\varphi = \tan^{-1} \left(\frac{\omega(L_s + L_{\text{FCL}})}{R_s + R_{\text{FCL}}} \right) \quad (6)$$

$$\tau = \frac{L_s + L_{\text{FCL}}}{R_s + R_{\text{FCL}}} \quad (7)$$

While Equations (1)–(7) give a basic foundation, they do not completely describe the transitory intricacies of current, DER-dominated networks. In realistic smart-grid settings, the following dynamic aspects must be incorporated:

1. *Inverter-Limited Fault Currents:* The traditional model assumes that all fault-current sources behave as ideal voltage sources behind an impedance. However, grid-connected inverters actively restrict their output current to safeguard semiconductor devices. The inverter fault-current contribution is more effectively stated as in Equation (8) [34].

$$I_{\text{inv}}(t) = \begin{cases} I_{\text{cmd}}(t) & \text{if } |I_{\text{cmd}}(t)| \leq I_{\text{max}}, \\ I_{\text{max}} \cdot e^{j\angle I_{\text{cmd}}(t)} & \text{if } |I_{\text{cmd}}(t)| > I_{\text{max}}, \end{cases} \quad (8)$$

where $I_{\text{max}} = k_{\text{lim}} \cdot I_{\text{rated}}$ is the inverter current limit [35] (typically $k_{\text{lim}} = 1.0\text{--}1.5$ p.u.), and $I_{\text{cmd}}(t)$ is the current reference. Equation (8) describes a grid-following inverter, whose current reference is generated by an outer control loop and clamped once its magnitude exceeds I_{max} . Grid-forming (GFM) inverters regulate voltage behind an impedance rather than a current reference, and therefore do not abruptly saturate. Most GFM implementations instead rely on a virtual-impedance (VI) loop that increases the apparent output impedance as current approaches the limit:

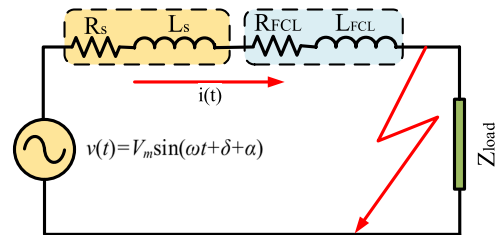


FIGURE 3 | Equivalent circuit of the simple power system with fault-current limiter (FCL).

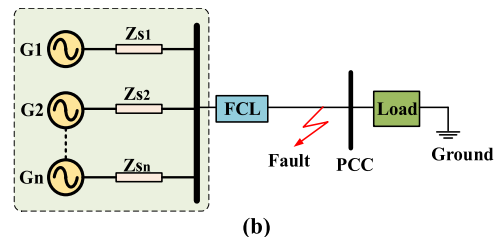


FIGURE 2 | FCL expression power system: (a) without FCL and (b) with FCL. FCL, fault-current limiter; PCC, point of common coupling.

$$Z_v(t) = Z_{v0} + k_v \cdot \max(0, |I(t)| - I_{th}),$$

where $I_{th} < I_{max}$ is the threshold at which the VI action begins. This produces a gradual, impedance-mediated response, and the hard clamp of Equation (8) is invoked only as a last-resort protective layer once the VI action itself saturates. Consequently, Equation (9) should be understood as applying whichever saturation model—the hard clamp of Equation (8) or the VI law—matches the specific control mode of each $I_{inv,k}(t)$ contributor. In a mixed grid with both synchronous generators (SGs) and IBRs, the total fault current at the FCL point becomes as depicted in the following equation [34]:

$$I_{\text{fault,total}}(t) = I_{SG}(t) + \sum_{k=1}^{N_{IBR}} I_{inv,k}(t), \quad (9)$$

where N_{IBR} refers to the number of IBRs, the FCL must be designed to restrict this combined current, allowing for the fact that IBR contributions saturate at I_{max} , but SG contributions may continue to climb. Undersizing the FCL impedance may fail to appropriately restrict the SG contribution even when IBRs are saturated.

2. *DC Offset Decay in Inverter-Dominated Grids:* The traditional DC offset term demands a single time constant $\tau = (L_S + L_{FCL})/(R_S + R_{FCL})$. In inverter-dominated grids, the SG and IBR contributions follow fundamentally different physical mechanisms rather than two variants of the same decay process. SGs exhibit a genuine subtransient DC offset because their fault current is governed by flux linkage that cannot change instantaneously. IBRs possess no such property, since their output is a controlled current reference rather than an electromotive force behind a physical inductance; no comparable DC offset ever develops in their contribution. Instead, the inner current control loop of IBRs (with bandwidth $\omega_{cc} = 500\text{--}2000$ rad/s) drives their output to its steady-state value with a first-order lag. The corrected total fault-current expression is stated in Equation (10).

$$i(t) = \frac{V_m}{Z_{SG}} \left[\sin(\omega t + \psi_{SG}) - e^{-\frac{t}{\tau_{SG}}} \sin(\psi_{SG}) \right] + I_{\text{max,IBR}} \left[1 - e^{-\omega_{cc} t} \right] \cos(\omega t + \phi_{IBR}), \quad (10)$$

where $I_{\text{max,IBR}} \equiv \sum_{k=1}^{N_{IBR}} I_{\text{max,k}}$ denotes the aggregate steady-state IBR fault-current contribution across all N_{IBR} inverter-based sources defined in Equation (9), and ϕ_{IBR} is the corresponding aggregate current angle. The disaggregated, per-inverter form is recovered by replacing the second term of Equation (10) with $\sum_{k=1}^{N_{IBR}} I_{\text{max,k}} [1 - e^{-\omega_{cc,k} t}] \cos(\omega t + \phi_{IBR,k})$, consistent with the summation structure already established in Equation (9). The FCL must minimize the first-peak fault current, which in such grids is governed largely by the SG contribution because the IBR transient is soon suppressed.

3. *Asymmetrical Fault Conditions Using Symmetrical Components:* Equations (1)–(7) implicitly assume balanced (three-phase symmetrical) fault circumstances, providing

a single-phase equivalent expression. In actual DER-rich distribution networks, the bulk of fault occurrences are asymmetrical—SLG, line-to-line (LL), and double line-to-ground (DLG) failures—which necessitate a symmetrical components structure. The FCL-modified fault current for an SLG fault on phase A is represented in Equation (11).

$$I_{F,SLG} = \frac{3V_a}{(Z_1 + Z_{FCL,1}) + (Z_2 + Z_{FCL,2}) + (Z_0 + Z_{FCL,0})}, \quad (11)$$

where Z_1, Z_2 , and Z_0 are the positive, negative, and zero-sequence system impedances, respectively, and $Z_{FCL,1}, Z_{FCL,2}$, and $Z_{FCL,0}$ are the corresponding FCL sequence impedances. For a resistive FCL, the sequence impedances are equal: $Z_{FCL,1} = Z_{FCL,2} = Z_{FCL,0} = R_{FCL}$, giving the following equation:

$$I_{F,SLG,FCL} = \frac{3V_a}{Z_1 + Z_2 + Z_0 + 3R_{FCL}}. \quad (12a)$$

This implies that, for an SLG fault, assuming symmetric FCL insertion across all three phases, the device adds R_{FCL} to each sequence network (positive, negative, and zero). Consequently, the cumulative impedance in the total fault loop is $3R_{FCL}$. It is worth noting that if the FCL operates asymmetrically (i.e., quenching only in the faulted phase), the sequence networks become coupled rather than remaining independently additive. This coupling can be formalized explicitly using the classical unbalanced-series-impedance formalism. For an FCL inserting a time-varying impedance $Z_{FCL}(t)$ in the faulted phase only (with the other two unaffected phases), transforming the resulting diagonal phase-domain impedance into the sequence domain via $Z_{012} = A^{-1} \text{diag}(Z_a, Z_b, Z_c) A$ yields

$$Z_{012,\text{total}}(t) = \begin{bmatrix} Z_0 & 0 & 0 \\ 0 & Z_1 & 0 \\ 0 & 0 & Z_2 \end{bmatrix} + \frac{Z_{FCL}(t)}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}, \quad (12b)$$

where the identical off-diagonal terms $Z_{FCL}(t)/3$ couple the zero-, positive-, and negative-sequence networks, requiring the full matrix relation $[V_0; V_1; V_2] = Z_{012,\text{total}}(t) \cdot [I_0; I_1; I_2]$ to be solved jointly rather than as three independent scalar equations. As a consistency check, when the FCL quenches symmetrically across all three phases ($Z_a = Z_b = Z_c = R_{FCL}$), the off-diagonal coupling terms vanish identically, and Equation (12b) reduces exactly to the additive result of Equation (12a), $Z_1 + Z_2 + Z_0 + 3R_{FCL}$, confirming that the symmetric quench case treated earlier in this section is recovered as the decoupled special case of this more general formulation.

Applying the general sequence-network matrix (Equation 12b) to the LL fault case, only the positive- and negative-sequence networks participate, since no path to ground exists:

$$I_{F,LL} = \frac{\sqrt{3} V_a}{(Z_1 + Z_{FCL,1}) + (Z_2 + Z_{FCL,2})}. \quad (12c)$$

Similarly, for the DLG fault, the general matrix formulation simplifies such that the positive-sequence network sees the parallel combination of the negative- and zero-sequence networks:

$$I_{a1} = \frac{V_a}{(Z_1 + Z_{FCL,1}) + \frac{(Z_2 + Z_{FCL,2})(Z_0 + Z_{FCL,0})}{(Z_2 + Z_{FCL,2}) + (Z_0 + Z_{FCL,0})}} \quad (12d)$$

with the total ground-fault current defined as $I_f = 3I_{a0}$, where $I_{a0} = -I_{a1}(Z_2 + Z_{FCL,2}) / (Z_2 + Z_{FCL,2}) + (Z_0 + Z_{FCL,0})$. Unlike the SLG case, the FCL's zero-sequence impedance interacts with the negative-sequence network multiplicatively rather than additively. Consequently, an FCL sized from the SLG condition alone may under- or overperform for DLG faults depending on the Z_2/Z_0 ratio, this distinction should therefore be considered when FCL sizing is evaluated for multiple fault types.

FCLs increase fault-loop impedance, thereby limiting both AC and DC components. The type of impedance determines the transient behavior: resistance reduces the FCL time constant (τ) and increases the power factor, thereby accelerating damping. In contrast, inductive FCLs increase (τ), but given the inherently high X/R ratio of the grid, their impact on the power factor is minimal [36]. After explaining the concept of FCL and the parameters that affect the current under fault conditions, it is crucial to demonstrate the characteristics of FCL under both normal and fault conditions.

Key Takeaways:

- Classical fault-current models (Equations 1–7) assume ideal voltage-source-behind-impedance behavior and do not capture inverter current saturation, reduced DC offset, or asymmetrical fault paths typical of DER-rich grids.
- IBR fault contribution saturates at $I_{\max} = k_{\text{lim}} \cdot I_{\text{rated}}$ (typically 1.0–1.5 p.u.), while SG contributions do not; undersized FCL impedance may therefore fail to restrict SG-dominated fault current even after IBR saturation.
- For SLG faults, a symmetric resistive FCL adds impedance additively across all three sequence networks ($3R_{\text{FCL}}$); for DLG faults, the interaction is multiplicative, sizing from the SLG case alone can under- or overperform for DLG conditions.
- Resistive FCL impedance shortens the fault time constant τ and improves damping; inductive FCL impedance lengthens τ with comparatively little power-factor effect.

3 | Characteristics and Classification of FCLS

Figure 4 shows the FCL duty cycle: It must maintain a negligible impedance during regular operation to minimize losses, inject a high impedance immediately to limit fault currents, and ensure rapid recovery after faults to restore service [38]. The impedance involved in the FCL arrangement may be fixed or vary with the magnitude of the fault current. An efficient FCL should present a negligible impedance during normal operation to avoid voltage drops and losses, yet switch to a high impedance during faults with a fast response [39, 40]. It must withstand transmission/distribution voltages and currents, limit AC and DC fault components, and recover automatically without manual intervention. Other

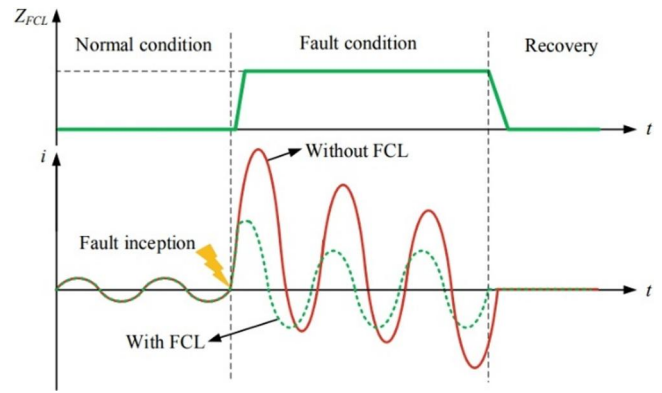


FIGURE 4 | Properties of FCL in power system [37]. FCL, fault-current limiter.

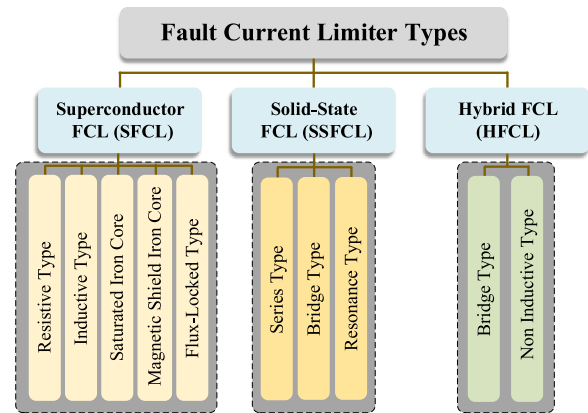


FIGURE 5 | Different types of fault-current limiters (FCLs).

requirements include reliability and a reasonable lifetime; scalability and manufacturability across all ranges; coordination with relays and CBs; immunity to disruptive tripping (motor start/start current); and optimal placement determined by system studies. Finally, FCLs should provide realistic economic benefits compared with alternative mitigation measures [41]. The following section classifies and reviews the principal types of FCLs, detailing their operating principles, performance characteristics, advantages, and limitations. The studies categorize FCLs into different categories based on technology: SFCLs, SSFCLs, and HFCLs [42], as shown in Figure 5.

3.1 | Superconducting Fault-Current Limiter

The operating principle of SFCLs depends on the superconducting state, which has zero electrical resistance when the temperature, current density, and magnetic field remain below their critical values (T_c , J_c , H_c) [43]. If any of these parameters exceeds its critical limit, the superconductor quenches and undergoes rapid Joule heating; the impedance increases rapidly, and the device enters a current-limited (resistive) state, thereby limiting the fault current [44].

3.1.1 | Resistive-Type SFCL (R-SFCL)

R-SFCL is the simplest type of SFCL in terms of structure. It can be executed using a high-temperature superconducting (HTS)

element integrated with a shunt impedance (R_{shunt} or L_{shunt}), as shown in Figure 6.

During normal operation, the resistance of HTS becomes very low. In this situation, the current flows typically to the load [45]. When the current exceeds the critical value during a fault, the superconductor undergoes a rapid transition (quench) and becomes resistive. While the quench time in faulty lines varies, it is often relatively quick. The shunt branch helps address specific requirements, such as minimizing hotspots and extreme overvoltage buildup at the R-SFCL connections [46].

To quantitatively characterize the quenching mechanism of an SFCL, the dynamic resistance $R_{\text{SFCL}}(t)$ during a fault is often approximated using an exponential transition. When the fault current surpasses the critical current at time t_0 , the resistance shifts from a superconducting state (zero resistance) to its maximum limiting value R_m according to Equation (13)

$$R_{\text{SFCL}}(t) = \begin{cases} 0, & t < t_0, \\ R_m \left(1 - e^{-\frac{t-t_0}{\tau_q}}\right), & t_0 < t < t_1, \\ R_m, & t \geq t_1, \end{cases} \quad (13)$$

where τ_q is the quench time constant representing the transition speed, and t_1 is the moment when the maximum resistance is fully formed. Furthermore, the energy-dissipation path is critical for the recovery phase. The total thermal energy wasted inside the superconductor during the limitation period t_c is evaluated as in Equation (14):

$$E_{\text{SFCL}} = \int_{t_0}^{t_c} i_{\text{SFCL}}^2(t) \cdot R_{\text{SFCL}}(t) dt. \quad (14)$$

This dissipated energy E_{SFCL} directly dictates the thermal stress on the HTS material and determines the required cryogenic cooling capacity and the following recovery time.

R-SFCL development is well documented: Early reviews consolidated operating principles, models, and materials through 2015 [47], while impedance analysis and YBCO tape tests under varying fault durations followed [48]. At utility scale, the European ECCOFLOW project validated a 24-kV, 1-kA R-SFCL for busbar and transformer-feeder protection using ~3 km of 12 mm YBCO tape [49]. For HVDC applications, comparative modeling

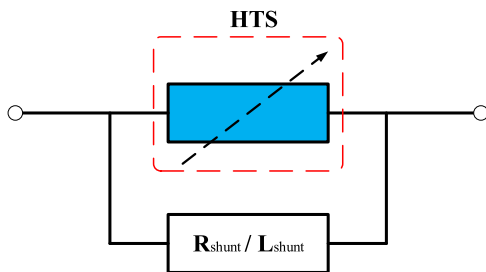


FIGURE 6 | R-SFCL configuration. HTS, high-temperature superconducting; R-SFCL, resistive-type superconductor fault-current limiter.

(step, exponential, rational quadratic [RQ], and magneto-thermal [MT]) identified the RQ model as the preferred balance of simplicity and accuracy, reducing both fault currents and mechanical-CB requirements in a multiterminal HVDC grid [50]. Designs up to 220 kV using long HTS tape with LN₂-gap-dependent dielectric strength have also been reported [51].

3.1.2 | Inductive-Type SFCLs (I-SFCLs)

Figure 7 shows the I-SFCL: A copper-wound primary coil connected in series with the main power line, an HTS secondary coil that limits the fault current, and a magnetic flux that flows between the primary and the HTS [52].

During normal operation, the HTS behaves as a short-circuited secondary winding. The current in the primary coil produces a magnetic field that produces a countercurrent in the superconducting loop due to strong inductive coupling. This opposite current cancels most of the flux in the core, resulting in a very low net magnetic flux. As a result, the I-SFCL presents minimal impedance to the main circuit, allowing current to flow with negligible losses. When a short circuit forms, the main current rises rapidly, leading to a fast-changing magnetic field inside the core. Consequently, a high current is generated in the HTS beyond its critical value, causing it to quench and transition from its superconducting state to its highly resistive state instantly. The secondary current is largely suppressed due to the sharp change in resistance, causing the magnetic field to collapse within the HTS. Consequently, all the magnetic flux associated with the primary fault current is allowed to establish itself inside the core [53].

I-SFCL development spans HVDC-oriented topology reviews [54], flexible simulation frameworks for transformer-type designs [55], and an autotransformer-based configuration validated for both technical efficiency and economic feasibility [56]. At the device level, an integrated bean-model/finite element method (FEM)/iterative prediction method for magnetic flux and supercurrent density was validated through prototype testing with high accuracy [57], while a self-adaptive DC I-SFCL incorporating energy dissipation was shown, through short-circuit and experimental testing, to reduce DC fault-current surge speed and amplitude while accelerating CB isolation [58].

3.1.3 | Saturated Iron-Core-Type SFCL (SI-SFCL)

Figure 8 shows the configuration of SI-SFCL, which consists of two cores, a superconducting coil (DC Coil), a DC power supply

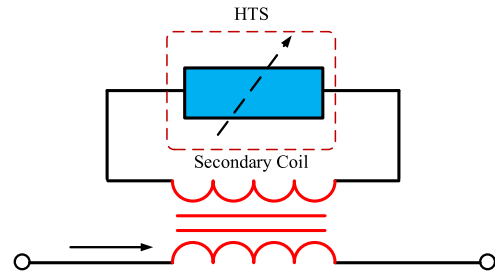


FIGURE 7 | I-SFCL configuration. HTS, high-temperature superconducting; I-SFCL, inductive-type superconductor fault-current limiter.

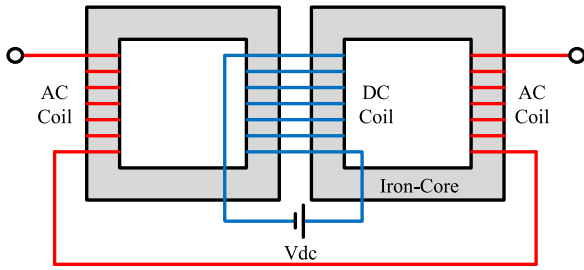


FIGURE 8 | Structure of SI-SFCL. AC, alternating current; DC, direct current; SI-SFCL, saturated iron-core-type superconductor fault-current limiter.

(V_{dc}), and a traditional coil (AC coil). In each SI-SFCL phase, two sets of conventional coils are utilized, both having the same number of turns and oriented in opposite directions [59]. A superconducting coil wound around each of the two iron cores creates a DC magnetic field that saturates the cores.

During normal operation, the DC coil is supplied with a fixed current, resulting in a robust and stable magnetic field (H_{DC}), and the iron core becomes magnetically saturated. In this saturated condition, the core's magnetic permeability (μ) is exceedingly low. Consequently, the inductance (L) of the AC coil is quite low. The inductive reactance ($X_L = 2\pi fL$) becomes very low. As a result, the AC load current passes through the AC coil with little voltage drop and loss. During the fault, a large AC current surges through the AC coil, generating a large opposing AC magnetic field (H_{AC}) in the core. The peak of the opposite H_{AC} field wipes out a large bias field from (H_{DC}). When $H_{DC} + H_{AC} \approx 0$ (or below saturation level), the iron core exits saturation and enters the linear region of its $B-H$ curve. In the linear region, the μ becomes very high, and the L of the AC coil increases dramatically. The X_L becomes very high, resulting in a high impedance that limits the magnitude of the fault current flowing through the AC coil.

SI-SFCLs can offer fast response, relatively short recovery times, and applicability across a wide range of voltage ratings. Field and prototype validation spans 15 kV/1.2 kA and 220 kV/300 megavolt-amperes (MVA) demonstrations, with a 500-kV design phase completed [60–62], though conventional SI-SFCLs remain bulky relative to alternative topologies. A compact, self-triggered, fast-recovery three-phase variant improved efficiency and cost on an IEEE 9-bus RES-integrated test network [63]. Comparing single-core dual- and single-AC-winding configurations, the single-winding model achieves adequate peak-current cutoff but incurs high normal-operation voltage drop, making bias design critical to its applicability [64].

3.1.4 | Magnetic Shield Iron-Core-Type SFCL (MI-SFCL)

Figure 9 shows the MI-SFCL, which consists of a series-connected primary winding, an HTS cylinder placed between the windings and the core, and an iron core. Its operation is analogous to a series transformer, which has a copper primary and a superconducting secondary [65].

During normal operation, the HTS shield is superconducting and screens out the alternating flux produced by the primary

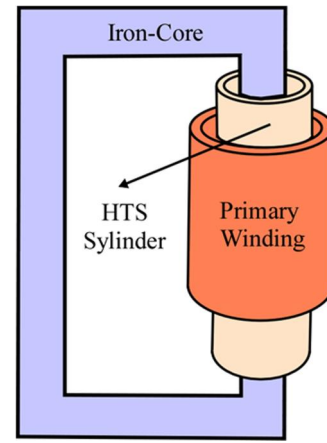


FIGURE 9 | Structure of magnetic shielded iron-core-type superconductor fault-current limiter. HTS, high-temperature superconducting.

winding, preventing flux coupling with the iron core. Therefore, the core remains effectively unmagnetized, and the primary inductance is low; hence, the load is supplied with minimum impedance. During a fault, the primary current and its associated field exceed the critical magnetic field of the HTS shield, causing the screen to switch into a resistive state. Flux then enters, and the core becomes highly magnetized, acting as a high-permeability flux sink. The primary thus behaves as a high-inductance element, and its large reactance limits the fault current.

An inductive-resistive variant (IR-SFCL) employing a superconducting multilayer solenoidal screen, more reliable than brittle conventional magnetic screens, has also been developed; the associated core-magnetization and shielding analysis attributes the improved shielding primarily to the diamagnetism of the HTS tape [66].

3.1.5 | Flux-Locked-Type SFCL (FL-SFCL)

Figure 10 depicts the main construction of the FL-SFCL. It has three traditional windings, an iron core, a superconducting element, a magnetic field coil, a resistor, and a capacitor. The HTS is connected in series with coil 2 and parallel with coil 1. In addition, the magnetic field coil (L_f), capacitor, and resistor are connected in series with the terminals of coil 3 [67].

The following equations can determine the voltage across each coil:

$$v_1 = n_1 \frac{d\varnothing}{dt}, \quad v_2 = n_2 \frac{d\varnothing}{dt}, \quad v_3 = n_3 \frac{d\varnothing}{dt}, \quad (15)$$

with $\varnothing$ representing the iron-core linkage flux. The number of turns of coils 1, 2, and 3 is also represented as n_1 , n_2 , and n_3 , respectively.

Under normal conditions, the electrical resistance of the HTS element is virtually zero; thus, v_1 equals v_2 . Therefore, the following equation may be recovered in this case:

$$(n_1 \pm n_2) \frac{d\varnothing}{dt} = 0, \quad (16)$$

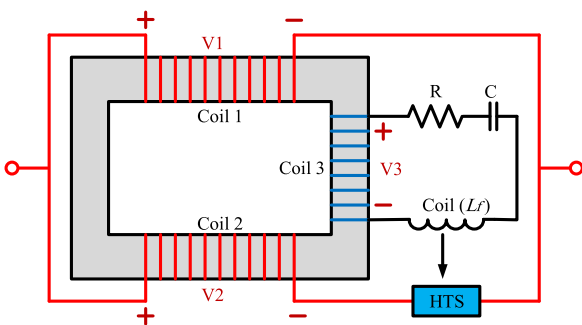


FIGURE 10 | Flux-lock-type superconductor fault-current limiter configuration. HTS, high-temperature superconducting.

where the $(\pm)$ sign denotes the additive or subtractive magnetic polarity depending on the relative winding direction of coils 1 and 2; the turns of coils 1 and 2 are not identical. The preceding equation requires $d\phi/dt$ to be zero. This indicates that the iron core experiences a constant linkage flux under normal circumstances, and the induced voltage in all coils is zero. As a result, only the resistance of traditional windings affects the voltage across SFCL terminals. Equation (16) becomes invalid as soon as the fault current causes the electric resistance of the superconductor to emerge, and the linkage flux changes over time. This occurrence results in the suppression of fault current and the induction of voltage in the coils [67]. In addition, current is drawn from the magnetic field coil due to the voltage present across the terminals of coil 3. These coils generate a magnetic field that helps the superconductor achieve enhanced current limitations by increasing its resistance. A capacitor enhances the stability of a superconductor in fault conditions. Still, it may negatively impact SFCL's limiting behavior by lowering iron-core linkage flux and raising the current from coil 3, creating a series resonant circuit protected by a resistor.

FL-SFCL technologies and applications have been comprehensively reviewed [68], and overcurrent-relay coordination with FL-SFCL has been investigated [69]. For DC applications, a dual-parallel-winding, two-series-module DC FL-SFCL has been analyzed [70], although its reported current-limiting and fault-recovery characteristics may not directly carry over to DC systems. Table 2 provides the advantages, disadvantages, uses, and other details of SFCL.

As summarized in Table 2, SFCL selection is governed by application-specific trade-offs rather than a single universal topology. R-SFCLs excel in subcycle response (< 5 ms) and compactness, but their long recovery times (220–310 ms) and thermal stress limit their viability for repetitive faults. Conversely, saturated iron-core designs offer mature, high-voltage (HV) scalability (12–500 kV) despite their large footprint and complex control systems, while inductive types provide instantaneous response but are restricted to medium voltages and incur DC losses. Furthermore, flux-lock types offer optimizable and adjustable operational modes, whereas magnetic-shield designs benefit from a simple, passive operation that requires no external control. Ultimately, optimal SFCL deployment requires balancing response/recovery dynamics, steady-state losses, physical footprint, and voltage ratings.

Building upon these deployment considerations, SFCLs have been investigated for applications beyond conventional AC

transmission substations, particularly in DC and hybrid AC/DC grids, where their fast impedance insertion can reduce stresses on HVDC breakers and improve fault ride-through (FRT) of converter stations. Demonstrations of saturated-core and R-SFCL prototypes at medium-voltage (MV) and HV levels indicate that these devices can facilitate the connection of additional generation and interties without exceeding short-circuit constraints, which is particularly relevant for renewable-rich and meshed transmission systems.

Key Takeaways:

- *R-SFCL*: Subcycle response (< 5 ms), compact, but recovery time 220–310 ms limits repetitive-fault viability.
- *Saturated iron-core SFCL*: Comparatively mature, with reported operation/designs up to 500 kV, but bulky, with complex control systems.
- *I-SFCL*: Very fast response, with reported applications concentrated at MV levels with DC losses.
- FL-SFCL offers adjustable, optimizable operation; magnetic-shield SFCL offers simple, passive operation with no external control.
- No single SFCL subtype dominates selection balances response/recovery dynamics, losses, footprint, and voltage rating (Table 2).

While SFCLs offer distinct advantages in fault limitation through their physical properties, SSFCLs provide active, ultrafast control. Following the analysis of SFCLs, the subsequent section details the general architecture of SSFCL technologies.

3.2 | Solid-State FCLs

Improvements in high-power semiconductor devices like emitter turn-off thyristor (ETO), insulated-gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT), silicon-controlled rectifier (SCR), gate turn-off thyristor (GTO), and super GTO (SGTO) have led to the development of solid-state current limiters (SSFCL). These additional impedances are stacked according to the fault current and need a fault detection system to operate properly [76].

3.2.1 | The Series-Type SSFCL (S-SSFCL)

Figure 11 depicts the topology of a series switch-type solid-state FCL (S-SSFCL). The S-SSFCL is designed with a parallel arrangement of multiple components, including bidirectional controlled semiconductors (S_{ss}), a bypass switch (S_{bp}), a current-limiting impedance ($Z_{limiter}$), overvoltage protection devices (Z_{no}), and a snubber circuit.

During normal operation, the current flows to the load through the S_{ss} switch. During the fault, the fault detector gives a signal to turn off the S_{ss} switch and $Z_{limiter}$ inserted in the path to limit the fault current. The Z_{no} helps manage the voltage across the switch by storing energy in the line inductance and providing an alternative current pathway. A snubber circuit is a crucial

TABLE 2 | Superconducting FCL comparison.

Comparison criteria/SFCL	Resistive [49, 51, 71, 72]	Inductive [54–56, 73, 74]	Saturated iron core [60–62, 75]	Magnetic shield [66]	Flux lock [67–70]
Advantages	– Fast response – Compact– Simple design– Low losses	– Instantaneous response – No delay – Self-triggered	– High-voltage capability – High reliability – Excellent coordination with breakers	– Simple passive design – No external control needed	– Multiple operating modes – Optimizable performance
Disadvantages	– Long recovery time – Thermal stress	– Large size – DC losses – Higher cost	– Very complex control system – Large and heavy	– Manufacturing challenges – Complex behavior	– Requires iron core – Limited field deployment
Response time	Very fast (< 5 ms)	Instantaneous (no delay)	Fast (≈ 20 ms)	Fast (≈ 5 ms)	Adjustable (≈ 10 ms)
Recovery time	220–310 ms	400 ms	600–800 ms	300 ms	350 ms
Normal-operation losses	Very low (hysteresis only)	Low (2–4 kW)	Low-medium	Very low	Very low
First-peak limiting	Excellent	Excellent	Good	Good	Good–excellent
Controllability	Limited	Limited	Good (adjustable)	Limited	Excellent (adjustable)
Size and weight	Compact and light	Large and heavy	Large and heavy	Medium	Medium
Complexity	Very simple	Medium	Complex	Medium	Medium–complex
Cost	Low–medium	Medium–high	Very high	Medium–high	Medium–high
Reliability	Good	Excellent	Good–excellent	Good	Good–excellent
Suitable voltage	6–220 kV [49, 51]	Medium voltage [54, 55]	12–500 kV [60–62, 75]	6–12 kV [66]	10 kV/ 500 A [67, 69]
Technical maturity	High (TRL 7–8) [48, 51]	Medium (TRL 4–5) [55, 56]	Very high (TRL 8–9) [60–62]	Medium (TRL 4–5) [66]	Medium (TRL 5–6) [67, 70]

Note: Quantitative values are approximate and highly dependent on specific design ratings and application contexts “Suitable Voltage” is reported per subtype; the Saturated Iron-Core subtype’s upper bound (500 kV) sets the SFCL family-level maximum reported in Table 4.

Abbreviations: FCL, fault-current limiter; SFCL, superconductor fault-current limiter; TRL, technology readiness level.

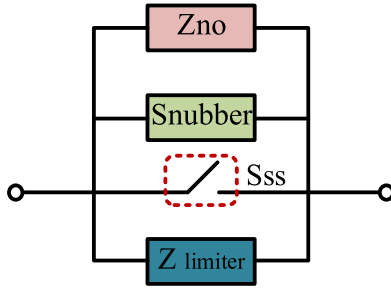


FIGURE 11 | Series switch-type solid-state fault-current limiter.

element of the semiconductor switch. It reduces the rate of voltage increase across the switch (dv/dt) during deactivation to prevent damage to the switch.

The switching dynamics of the SSFCL are governed by the semiconductor commutation process. When the bidirectional switch S_{ss} is forced off, the rate of voltage rise across the semiconductor must be strictly limited by the snubber capacitance C_s to avoid destruction, mathematically expressed as

$$\frac{dv_{ss}}{dt} = \frac{i_{\text{fault}}(t)}{C_s}. \quad (17)$$

Once the voltage across the switch approaches the clamping voltage of the overvoltage protection device (e.g., ZnO varistor), indicated as V_{clamp} , the fault current commutates into the ZnO and Z_{limiter} branches. The energy-dissipation path during this very transient switching phase is mostly regulated by the varistor. The total energy absorbed by the varistor to safely suppress the inductive energy of the grid is computed as in Equation (18).

$$E_{\text{ZnO}} = \int_{t_{\text{switch}}}^{t_{\text{clear}}} V_{\text{clamp}} \cdot i_{\text{ZnO}}(t) dt. \quad (18)$$

These dynamic equations highlight the fundamental design trade-off in SSFCLs: while faster switching speeds minimize the first peak of the fault current, they simultaneously impose severe dv/dt stress and demand significantly higher energy-dissipation capabilities from the snubber and varistor circuits.

Fast-acting SSFCL methods using power-electronic switches have been validated on a 400-kV power systems computer-aided design/electromagnetic transients including DC (PSCAD/EMTDC) model, demonstrating effective fault-level reduction over passive limiters [77]. At the distribution level, an SSFCL integrated with a 100-kW PV system through a 100-kVA transformer was shown to limit prospective fault current and mitigate point of common coupling (PCC) voltage sags under both symmetrical and unsymmetrical faults [78]. Extending this toward digital integration, an IoT-based SSFCL architecture enabling cloud-monitored fault detection and control has also been demonstrated on an IEEE 6-bus test system [79].

3.2.2 | Resonant-Type SSFCL (R-SSFCL)

The principle of operation of R-SSFCL is based on the resonance between series or parallel combinations of L and C components, as depicted in Figure 12.

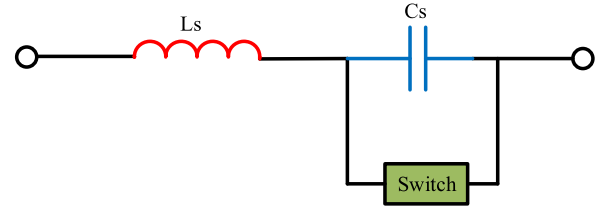


FIGURE 12 | Resonant-type solid-state fault-current limiter.

Under normal operation, semiconductor switches are normally opened, thereby making the current flow through the LC circuit. This is achieved by selecting values for L and C such that resonance at the system frequency (50 or 60 Hz) occurs, thereby causing no impedance or voltage drop. As soon as the fault is identified within the system, semiconductor switches are closed to shift away from resonance, thereby introducing higher impedance within the circuit.

The LC tank circuit is tuned to system frequency f_0 such that

$$f_0 = \frac{1}{2\pi\sqrt{L_s C_s}}.$$

Under normal circumstances, the resonant impedance is nominally zero. Upon fault detection, the switch opens and the circuit departs from resonance, inserting an effective impedance as shown in Equation (19):

$$Z_{\text{FCL}} = j\omega L_s + \frac{1}{j\omega C_s} = j\left(\omega L_s - \frac{1}{\omega C_s}\right), \quad (19)$$

which becomes significantly inductive at frequencies deviating from f_0 , thereby limiting the fault current.

Resonance-based prototypes have been experimentally validated across multiple configurations. A three-phase series-parallel resonance FCL constrained fault currents to 75%–85% of their unlimited value across three-phase, three-phase-to-ground, two-phase-to-ground, and phase-to-ground faults, with MATLAB/Simulink simulations confirmed against 380 V short-circuit tests [80]. Bench-scale comparison of series-switched-reactor and resonant-circuit SSFCLs, implemented with SCRs and IGBTs, reduced fault current from 600 to 75 A for both topologies; an accompanying microcontroller-based detection algorithm using instantaneous current and its derivative minimized false triggering from measurement noise [81]. For MVDC applications (e.g., marine power, subsea oil, and gas), two improved LC -resonant CBs suppressed fault currents within microseconds while integrating with existing solid-state or hybrid DCCBs, reducing energy stress and surge-arrester requirements; hardware-in-the-loop (HIL) testing at 1.2 MW and laboratory prototypes confirmed their efficiency in driving the main switch current to near zero with minimal components [82].

3.2.3 | Bridge-Type SSFCLs (B-SSFCLs)

B-SSFCL consists of two main parts, the bridge part and the shunt branch, as shown in Figure 13. The bridge part includes four diodes, a DC reactor (L_{dc}), a resistor R_{dc} , an IGBT switch,

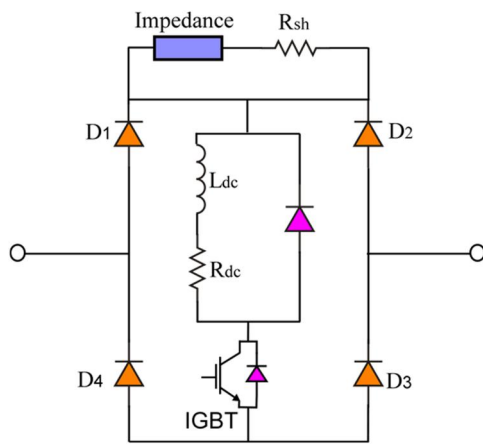


FIGURE 13 | Bridge-type solid-state fault-current limiter configuration. IGBT, insulated-gate bipolar transistor.

and a freewheeling diode. The shunt branch includes an impedance (inductor or capacitor) connected in series with a resistor (R_{sh}).

With the IGBT on, current flows through $D_1 - L_{dc} - R_{dc} - D_4$ and $D_2 - L_{dc} - R_{dc} - D_3$ in the positive and negative half-cycles, respectively. The unidirectional current charges L_{dc} to the peak value, making it behave nearly as a short circuit; thus, the BSSFCL introduces negligible voltage drop in normal operation. During the fault, the IGBT switch is turned off, and the bridge becomes an open circuit. The shunt track, therefore, limits the fault current. Meanwhile, the freewheeling diode aims the reactor (L_{dc}) to discharge.

Recent B-SSFCL configurations emphasize multifunctionality: an air-core reactor topology detects faults within 1 ms, reduces current by 42% across transient events, and maintains safe semiconductor dv/dt limits [83]; a dual-functional design switches instantly, without detection delay, between inductive-circuit fault limiting and capacitive-circuit dynamic voltage restoration (DVR) [84]; and a related BFCL-DVR integration actively controls fault intensity while accelerating post-fault voltage recovery [85]. The referenced applications indicate that SSFCL technologies can be well-suited to inverter-dominated settings. Their power-electronic characteristics enable seamless integration with grid-connected converters in PV plants, wind farms, and MVDC links, enabling rapid and adjustable limiting of fault currents and alleviating voltage sags at the PCC, while maintaining the functionality of sensitive converter controls. To synthesize the operational dynamics of these configurations, Table 3 provides a comparative overview of Series, Resonance, and B-SSFCLs, detailing their respective advantages, limitations, technical maturity, and typical applications.

As indicated in Table 3, SSFCL topologies offer complementary performance trade-offs. S-SSFCLs enable microsecond-level fault blocking and accurate control, but their constant conduction losses and thermal stress demand sophisticated thermal management. Conversely, R-SSFCLs exploit LC resonance to minimize steady-state losses and achieve substantial fault reduction (50%–70%); however, they remain subject to frequency deviations and transient resonance instabilities. Meanwhile, bridge-type topologies offer improved dynamic control

and bidirectional operation, albeit at the penalty of higher semiconductor device counts, complex gate-drive circuitry, and increased electromagnetic interference (EMI). Ultimately, SSFCL designs trade architectural complexity and continuous losses for ultrafast, highly controlled responses, making them particularly suitable for converter-dominated and HVDC applications.

Key Takeaways:

- *S-SSFCL*: Microsecond-level fault blocking, precise control, but continuous conduction losses require robust thermal management.
- *R-SSFCL*: Minimal steady-state losses, 50%–70% fault-current reduction, but sensitive to frequency deviation and transient resonance instability.
- *B-SSFCL*: Bidirectional operation, strong dynamic control, but the highest device count, complex gate-drive circuitry, and increased EMI.
- SSFCLs trade architectural complexity and continuous losses for ultrafast, controllable response, making them particularly suitable for converter-dominated and HVDC applications (Table 3).

Having detailed the operating principles and diverse topologies of SSFCLs, this section introduces the third and final major classification: HFCL technologies.

3.3 | Hybrid Fault-Current Limiter

The HFCLs integrate SFCLs and SSFCLs. The fundamental architecture of these FCLs relies on a superconductor, often connected to a semiconductor switch. Consequently, these FCLs combine the advantages of both SFCLs and SSFCLs.

3.3.1 | Bridge-Type HFCL

A two-stage HVDC FCL/breaker, combining inductive and resistive current limiting to reduce breaker energy consumption and improve hybrid DCCB fault-current magnitude and operating speed, has been theoretically evaluated, confirmed via PSCAD/MATLAB-Simulink, and validated through scaled-down laboratory testing [87]. A complementary H-bridge HFCL, whose bidirectional current-commutation branch limits the fault-current rate-of-rise during current transfer, was assessed for electrical stress and transient energy transfer through ± 500 kV bipolar HVDC simulations in PSCAD/EMTDC, showing reduced IGBT and metal-oxide varistor (MOV) requirements alongside fast fault isolation [88].

3.3.2 | Noninductive HFCL

The methodology focuses on limiting the fault current by utilizing the high impedance generated during the transient-state operation of the superconducting element, thereby transitioning the triggering coil to the normal state. In this HFCL, two superconducting coils are arranged antiparallel: a trigger coil and a limiting coil, both exhibiting magnetic coupling and identical self-inductance, thereby allowing them to share the same line current. When a fault occurs, the current in the trigger coil

TABLE 3 | Comparison between solid-state FCL types [86].

SSFCL type	Series-type SSFCL	Resonance-type SSFCL	Bridge-type SSFCL
Advantages	• Fast switching response • Precise control • Can block fault current within microseconds	• Utilizes natural <i>LC</i> resonance to cancel impedances during normal operation • Very low conduction losses • Limited fault-current reduction range • Sensitive to frequency variations and component tolerances • Resonance instability risk under transient conditions	• Allows bidirectional current flow • Excellent dynamic control • Integrates well with hybrid systems
Disadvantages	• Continuous conduction losses • Semiconductor stress under normal load • Requires robust thermal management • Higher losses than passive FCLs		• Complex control and gate-drive requirements • Highest device count and gate-drive complexity • Electromagnetic interference challenges • More failure points
Technical maturity	Medium (commercial at LV and select MV industrial feeders)	Low-to-medium (validated in labs and limited MV demonstrations)	Medium – Mature at LV (close to solid-state breakers) – MV solutions are emerging/pilot level with series-connected devices
Typical applications	MV grids, distribution systems	Transmission and distribution of sensitive equipment	Advanced grid applications, microgrids, smart grids
Cost	Moderate	Higher due to passive components and control	High due to complex power electronics and control
Current-limiting capability	30%–50% of the fault current	50%–70% of the fault current	30%–60% of the fault current

Abbreviation: LV, low voltage; MV, medium voltage.

reaches a specific threshold, prompting it to switch from superconducting to normal mode. This change alters the current ratio between the coils, ensuring the reactor's magnetic flux is nonzero. Consequently, the equivalent impedance of the coils increases, thereby restricting the fault current.

In [89], a noninductive HFCL was introduced. The core thesis of this HFCL is that the fault current is limited by a high-impedance pathway that forms during the transition from superconducting to normal conditions. The HFCL's hybrid bridge circuit incorporates two superconducting coils, a trigger coil, and a limiting coil, all configured in an antiparallel arrangement. Table 3 provides a technical comparison of all FCLs based on the technical topics covered in the preceding subsections.

In extensive multiterminal HVDC and hybrid AC/DC systems, HFCLs are especially appealing due to their ability to merge minimal losses during standard operation with rapid limiting and coordination with hybrid DCCBs. These capabilities directly address critical resilience concerns for future backbone grids, where the dense connectivity of renewable generation and converter-based transmission heightens the risk of widespread disturbances following DC faults. Having explored the distinct characteristics and applications of superconducting, solid-state, and hybrid topologies, Table 3 provides a comprehensive comparative analysis of these three primary FCL families across key technical, operational, and economic parameters.

As illustrated by the comparative parameters in Table 4, selecting among SFCL, SSFCL, and HFCL families necessarily requires balancing distinct operational and economic trade-offs. SFCLs generally offer high reliability and low steady-state losses, but their implementation is often constrained by physical footprint, cryogenic requirements, and capital cost. SSFCLs generally provide more compact and adaptable configurations, although their reliance on semiconductor components can lead to higher voltage drops, harmonic distortion, and other reliability issues. HFCLs can provide a compromise between low-loss superconducting operation and power-electronic control, but at the cost of greater integration and maintenance complexity.

Operating voltage figures are consolidated from [30]; the SFCL upper bound (500 kV) is independently corroborated by the Saturated Iron-Core field/design data reported in Section 3.1.3 [62] and Table 2.

Subfamily-level performance differentiation underlying this cross-family comparison is detailed further in Table 2 (SFCL) and Table 3 (SSFCL), application-specific operating trade-offs are summarized in Table 5, and the quantitative capital and operating expenditure basis for the capital expenditure (CAPEX) figures reported above is developed in full in Section 5.2 through the Net Present Value (NPV) framework of Equation (42).

Key Takeaways:

- SFCLs generally offer high reliability and low steady-state losses but incur the highest CAPEX and have the largest footprint, best reserved for critical HV nodes.

- SSFCLs generally offer more compact configurations and comparatively lower upfront cost, at the cost of lower reliability and higher harmonic generation.
- HFCLs can provide an intermediate trade-off, combining superconductor-level losses with power-electronic-level control speed, at the cost of dual (cryogenic + power-electronic) maintenance complexity.
- Family-level selection (Table 4) should be treated as a starting point, refined by the scenario-specific guidance developed in Section 3.4.

3.4 | Critical Comparative Insights and Selection Guidelines

Superconducting, solid-state, and hybrid FCLs all reduce short-circuit current by inserting impedance during faults, but their suitability depends on the specific application [90]. The preferred technology is determined by system voltage, prospective fault current, required response time, expected fault duty and recovery needs, and constraints, such as normal-operation losses, footprint, and maintenance capability.

SFCLs are particularly suitable for applications requiring minimal losses and effective current limitations, especially within HV substations. However, their widespread adoption is constrained by the necessity for cryogenic systems, extended quench recovery periods, and limited large-scale operational experience. SSFCLs offer rapid current limitations for HVDC applications, but they encounter challenges, such as continuous conduction losses and increased system complexity, which hinder scalability. HFCLs integrate superconductors with power electronics to optimize performance, yet they also present integration challenges that require precise coordination to ensure adequate protection of circuit components.

These findings suggest that selecting FCL technologies should be guided by specific application scenarios rather than by the technologies themselves. For instance, saturated-core SFCLs are well suited for HV transmission nodes where robustness and high current ratings are required, and installation space is sufficient. In contrast, compact solid-state and hybrid designs are more appropriate for distribution feeders with high DER penetration and for HVDC grids, where ultrafast current limitations and advanced control capabilities are necessary [91].

To be more specific, from a voltage-level perspective, SFCLs, particularly saturated iron-core designs, are technically validated for HV transmission applications (12–500 kV), offering the highest current ratings (up to 10 kA) at the cost of the most expensive capital investment and the largest physical footprint. This primarily limits their deployment to important transmission substations, where space and budget constraints are less stringent. Conversely, SSFCLs represent the most compact and cost-effective solution of the three families, making them highly suitable for MV distribution feeders (up to 20 kV) and converter-dominated grids, though their moderate reliability and high harmonic generation limit their scalability to higher voltage levels. Occupying an intermediate ground, HFCLs provide a balanced cost-performance profile appropriate for MV

TABLE 4 | Technical comparison of FCL families [30].

Parameters/FCL	SFCL	SSFCL	HFCL
Material technology	Superconductor	Semiconductor	Superconductor and semiconductor
Operating voltage	Up to 500 kV	Up to 20 kV	Up to 15 kV
Rated current	A few amperes to 10 kA	A few amperes to 3 kA	2 kA
Energy loss in normal operation	Very low	Moderate	Very low
Time response	2.5–10 ms	1 μ s to a few ms	Less than 1–2 ms
Percent of transient overvoltage	0.6%–2.3%	About 2%	About 10%
Weight	3–36 tones	A few kg–a few tones	From one to a few tones
Physical dimensions	The largest	The smallest	Fairly large
Cooling system	High-power ratings, voluminous, liquid nitrogen	Heatsink, air ballast	Heat sink, air ballast, liquid nitrogen
Cost	The most expensive	The cheapest	Fairly expensive
Manufacturing as a compact pack	No	Yes	No
Modular	No	Yes	No
Reliability	The most reliable	Has the lowest reliability	Reliable
Harmonic generation	Very low	Very high	High
Loss	Very low	Low	Low
Voltage drops	Very low	High	Low
No-load loss	Very high	Very low	Low
Needs maintenance	High	Low	Very high
Technology readiness level	4–9 (subtype-dependent; saturated-core designs field-demonstrated up to a 500-kV/300-MVA design stage, per Table 2)	4–8 (subtype-dependent; series-type commercial at LV/MV, resonance-type validated in labs with limited MV pilots, per Table 3)	3–5 (predominantly simulation-validated and scaled-down laboratory prototypes; no full-scale field deployment reported in the reviewed literature)
Indicative installed CAPEX	USD 1–5 million per phase (transmission-level units); HTS conductor cost USD 50–200/kA·m; see Section 5.2	USD 50,000–500,000 (MV applications); see Section 5.2	Not yet systematically reported in the published literature, identified as a cost-benchmarking research gap (Section 5.2)

Note: Values for response time, cost, dimensions, and losses are illustrative ranges that represent current state-of-the-art developments and vary with specific utility requirements.

Abbreviations: CAPEX, capital expenditure; FCL, fault-current limiter; HFCL, hybrid FCL; HTS, high-temperature superconducting; LV, low voltage; MV, medium voltage; SFCL, superconductor fault-current limiter; SSFCL, solid-state fault-current limiter.

networks and HVDC links (up to 15 kV) but introduce dual maintenance complexity for both cryogenic and power-electronic subsystems, thereby raising the overall lifespan cost. On the basis of the foregoing discussion, Table 5 highlights, for each FCL family, the operating parameters under which it works best, the key practical limits documented in the literature, and the associated trade-offs between performance, cost, and scalability.

To bring together the device-level and demonstration-level evidence discussed across the three FCL families, Table 6 consolidates the field- and laboratory-validated deployment projects referenced throughout Sections 3.1–3.3, summarizing their rated voltage/power, validation method, and reported outcome.

These demonstrations confirm technical feasibility across a range of voltage and power levels, yet remain predominantly at the prototype or pilot project stage rather than sustained commercial operation, a gap addressed from a control-strategy perspective in Section 3.5. To complement the deployment evidence summarized in Table 6 with a direct visual benchmark, Figure 14 consolidates the quantitative response time, recovery time, and current-limiting performance data already reported in Tables 2 and 3, allowing cross-family comparison at a glance.

As Figure 14a illustrates, I-SFCLs and solid-state/hybrid topologies offer sub-millisecond-to-few-millisecond response, whereas Figure 14b shows that this speed advantage for SFCLs

TABLE 5 | Comparative operating conditions and practical limitations of FCL families.

FCL family	Best operating conditions	Key real-world limitations	Performance–cost–scalability trade-off
SFCLs	Ideal for MV/HV substations with constrained breakers, requiring minimal operating losses and strong peak fault-current limitation.	High-cost, bulky solutions require cryogenic cooling and quench recovery time, with limited long-term field experience.	Delivers excellent limitation and negligible losses, but high costs (CAPEX/OPEX) and complexity restrict its deployment to critical nodes.
SSFCLs	Ideal for converter-dominated grids, HVDC/VSC systems, and high-DER MV feeders requiring ultrafast, controllable fault limitation.	Faces conduction/switching losses, EMI, and complex design challenges, with limited maturity at very high voltages.	Offers fast, flexible limiting but with higher losses and complexity; economic viability depends on the critical need for advanced protection.
HFCLs	Ideal for HVDC and meshed networks requiring both low losses and fast, controllable limitation to reduce stress on DC/hybrid breakers.	Inherits combined SFCL/SSFCL challenges, requiring complex overvoltage protection and dual maintenance for both cryogenic and power-electronic components.	Offers balanced performance (loss, speed, control) but requires high integration effort, making it suitable only for high-value, demanding nodes.

Abbreviations: CAPEX, capital expenditure; DER, distributed energy resource; EMI, electromagnetic interference; FCL, fault-current limiter; HFCL, hybrid FCL; HV, high voltage; HVDC, high-voltage direct current; MV, medium voltage; OPEX, operational expenditure; SFCL, superconductor fault-current limiter; SSFCL, solid-state fault-current limiter; VSC, voltage source converter.

is generally offset by recovery times an order-of-magnitude longer (220–800 ms); Figure 14c further shows that among SSFCL subtypes, resonance-type circuits achieve the highest current-limiting capability (50%–70%) at the cost of the frequency sensitivity discussed in Section 3.2.2.

3.5 | Advanced FCL Control in Modern Power Systems

Recent literature progresses from passive hardware solutions to adaptive, control-centric FCL techniques, notably addressing the vulnerabilities of converter-dominated grids. Within microgrids utilizing IBRs—particularly GFM architectures—VI strategies are increasingly integrated directly into the principal control loops [92]. This software-driven technique not only defends sensitive semiconductor switches from severe thermal overloads but also actively reshapes the fault-current profile. Furthermore, by dynamically co-optimizing these virtual parameters, these approaches lay the groundwork for resilient protection coordination during both grid-connected and islanded operation modes, seamlessly bridging device-level control with system-level protection.

Building upon this transition to system-level protection, from an adaptive standpoint, the deployment of FCLs fundamentally alters the time-current characteristics seen by upstream and downstream protective relays [93]. In systems with variable DER penetration, fault-current levels may fluctuate significantly between peak generation and low-generation operating states, making fixed relay settings inadequate. FCLs address this challenge by constraining the upper bound of fault-current excursions, effectively narrowing the range of fault-current variation that relay settings must accommodate [94]. This enables the implementation of adaptive overcurrent-relay schemes, wherein relay pickup currents and time-dial settings are dynamically recalculated via IEC 61850-based communication with a central protection controller based on real-time FCL status and network topology [95]. Furthermore, FCLs facilitate

the coordination of directional overcurrent relays (DOCRs) in meshed and multisource networks by ensuring that fault current directionality remains consistent regardless of DER dispatch levels, thereby helping preserve protection selectivity across varying operating conditions.

To further enhance RES-dominated microgrids, recent research prioritizes adaptive, control-oriented insertion tactics over conventional static methods. In AC applications, such as standalone wind microgrids, the selective faulty-phase insertion of FCLs greatly mitigates power and speed oscillations, thereby enhancing transient stability. Concurrently, in DC microgrids, hybrid fault-limiting devices combine superconducting and power-electronic components with advanced algorithms to actively minimize peak currents and interruption times [96]. Ultimately, these developments indicate an increasing shift from purely passive FCL applications toward more actively managed operation coordinated with modern AC and DC converter topologies.

In inverter-dominated microgrids, the incorporation of hardware FCLs must be meticulously aligned with the active management techniques of power-electronic converters to guarantee robust FRT and system stability.

1. *AC Microgrid Control Strategies:* In AC microgrids, FCL control must be synchronized with the hierarchical control framework (primary, secondary, and tertiary layers) that regulates IBRs. At the basic control level, GFMs inverters use droop control to manage voltage and frequency, as shown in Equations (20) and (21).

$$V = V^* - K_v \cdot (Q - Q^*), \quad (20)$$

$$f = f^* - K_f \cdot (P - P^*), \quad (21)$$

where k_v and k_f are the voltage and frequency droop coefficients [97], respectively, and V^* , f^* , P^* , and Q^* are the

TABLE 6 | Summary of reported FCL demonstration and deployment projects.

Project/prototype	FCL family and type	Rated voltage/power/current	Validation method	Reported outcome	Reference
ECCOFLOW project	R-SFCL	24 kV, 1 kA	Field tests on busbar and transformer feeder (~ 3 km, 12 mm YBCO tape)	Feasibility confirmed at the distribution level	[49]
Saturable-core prototype	SI-SFCL	15 kV/1.2 kA	Prototyping and bench testing	Adequate peak fault-current cutoff validated	[60]
Factory- and field-tested unit	SI-SFCL	220 kV/300 MVA	Factory + field tests	Confirmed field-deployable at HV transmission level	[61]
Winding/experimental study unit	SI-SFCL	500 kV	Winding technology + experimental study	Confirms technical feasibility of 500-kV-class design	[62]
Compact self-triggered SI-SFCL	SI-SFCL	IEEE 9-bus test network	Simulation on RES-integrated test system	Improved efficiency and cost savings reported	[63]
Air-core reactor B-SSFCL prototype	B-SSFCL	LV-scale laboratory unit	Laboratory prototype	Fault detected in < 1 ms; 42% current reduction across transient events	[83]
Series-parallel resonance FCL	R-SSFCL	380 V	Laboratory prototype + short-circuit tests	Fault current constrained to 75%–85% of the unlimited value	[80]
Series-switched reactor/resonant-circuit prototypes	SSFCL (series and resonant)	Bench scale	Bench prototype comparison	Fault current reduced from 600 to 75 A	[81]
Resonant MVDC circuit breaker	Resonant SSFCL/DCCB	MVDC, 1.2 MW	Hardware-in-the-loop simulation + laboratory prototype	Efficiency confirmed; main switch current reduced to near zero	[82]

Abbreviations: B-SSFCL, bridge-type SSFCL; DCCB, direct current circuit breaker; FCL, fault-current limiter; HV, high voltage; LV, low voltage; MVDC, medium-voltage direct current; RES, renewable energy source; R-SFCL, resistive type superconductor fault-current limiter; SI-SFCL, saturated iron-core type superconductor fault-current limiter; SSFCL, solid-state FCL; YBCO, yttrium barium copper oxide.

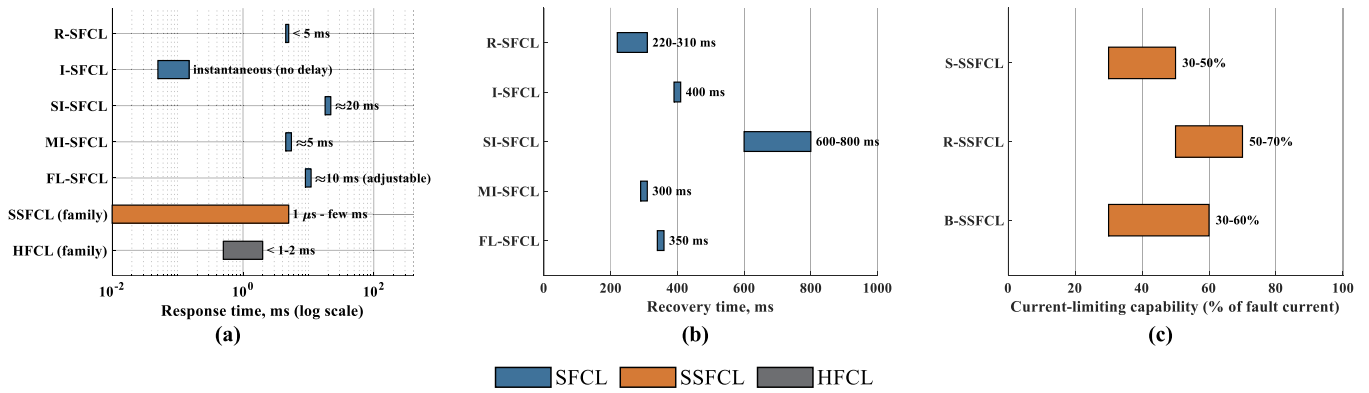


FIGURE 14 | Quantitative benchmark of (a) response time across SFCL subtypes and the SSFCL/HFCL family ranges (log scale), (b) recovery time across SFCL subtypes, and (c) current-limiting capability across SSFCL subtypes. Bar ranges reflect the values. B-SSFCL, bridge-type SSFCL; FCL, fault-current limiter; FL-SFCL, flux-locked-type SFCL; HFCL, hybrid FCL; I-SFCL, inductive-type SFCL; MI-SFCL, magnetic shield iron-core-type SFCL; R-SFCL, resistive-type superconductor fault-current limiter; R-SSFCL, resonant-type SSFCL; SFCL, superconductor fault-current limiter; SI-SFCL, saturated iron-core type superconductor fault-current limiter; SSFCL, solid-state FCL; S-SSFCL, series-Type SSFCL.

reference setpoints. In the event of a malfunction, the software control logic must swiftly restrict the current to safeguard the IGBTs, while maintaining synchronization. This is accomplished using adaptive impedance control and threshold virtual impedance (TVI), in which a dynamic impedance $Z_v(s)$ is included in the inverter output impedance as shown in Equation (22).

$$V_{\text{ref}}(s) = E(s) - Z_v(s) \cdot I_o(s). \quad (22)$$

During regular operation, Z_v is set to a minimum value. Upon detecting a fault-triggered when the output current $|I_o|$ exceeds a safety threshold I_{th} or via dv/dt detection—the TVI control loop quickly raises the impedance to actively restrict the fault-current contribution to a desirable level [98] (usually $1.2-1.5 I_{\text{rated}}$). At the secondary level, a centralized microgrid controller adjusts the reference setpoints to correct voltage and frequency deviations produced by FCL insertion, employing a gradual integral action (bandwidth < 1 Hz) to maintain stable hierarchical functioning.

Furthermore, for selective fault isolation, zone-selective interlocking via IEC 61850 GOOSE messaging (delay < 4 ms) prevents upstream FCLs from needlessly injecting impedance. In island modes, when fault currents are much smaller, the VI is adaptively decreased to avoid protection blinding, as illustrated in the following equation:

$$Z_{v,\text{island}} = Z_{v,\text{grid}} \cdot \left(\frac{I_{\text{sc,grid}}}{I_{\text{sc,island}}} \right). \quad (23)$$

2. DC Microgrid Control Strategies: DC microgrids have a fundamentally different issue owing to the lack of natural current zero-crossings and the very high rate of increase of fault currents, dictated by circuit inductance: $di/dt = (V_{\text{DC}} - V_{\text{fault}})/L_{\text{line}}$. The current spike is primarily due to the unrestrained discharge of the DC-link capacitors. To adjust the DC-bus voltage during fault situations, droop-controlled converters adopt a two-stage current-limiting law: Stage 1 (normal

operation), $V_{\text{DC}} = V_{\text{DC}}^* - R_{\text{droop}} \cdot I_{\text{DC}}$; Stage 2 (fault limiting), $I_{\text{DC,ref}} = \min(I_{\text{DC}}^*, I_{\text{FCL,max}})$.

The transition is triggered instantly when $dI_{\text{DC}}/dt > (di/dt)_{\text{threshold}}$. Because conventional linear controllers (like standard PI loops) are often too slow for this transient, advanced nonlinear strategies such as Finite Control Set Model Predictive Control are heavily utilized to evaluate switching states and suppress the current rise within microseconds (< 50 μs).

For hybrid DC FCLs, the coordinated sequence incorporates quench initiation upon di/dt detection, followed by current limiting to I_{peak} , and lastly solid-state interruption where the energy stored in the line inductance ($E = 0.5LI_{\text{peak}}^2$) is securely absorbed by MOV arresters.

In multiterminal DC microgrids, a distributed FCL control architecture is crucial. A central DC controller solves a real-time optimum current redistribution issue (updated at 10–100 ms intervals) to guarantee the overall fault current does not exceed the DC breaker rating while favoring healthy feeders:

$$\min \sum_i w_i \cdot (I_{\text{FCL},i} - I_{\text{FCL},i,\text{ref}})^2$$

subject to

$$\sum_i I_{\text{FCL},i} \leq I_{\text{CB, rated}},$$

$$I_{\text{FCL},i,\text{min}} \leq I_{\text{FCL},i} \leq I_{\text{FCL},i,\text{max}}.$$

To synthesize these distinct operational dynamics, Table 7 outlines the comparative control parameters for FCL integration in AC and DC microgrids.

Furthermore, the integration of FCLs plays a crucial role in ensuring transient stability and meeting severe FRT grid rules

TABLE 7 | Comparative FCL control strategies in AC and DC microgrids.

Parameter	AC microgrid FCL control	DC microgrid FCL control
Control timescale	10–100 ms (primary droop)	< 1 ms (current derivative)
Primary mechanism	Virtual-impedance injection	Current saturation + rate limiting
Fault detection method	Overcurrent threshold + dv/dt	di/dt threshold
Coordination protocol	IEC 61850 GOOSE (< 4 ms)	Low-latency DC-bus signaling (< 2 ms)
Operating mode adaptation	Grid-connected versus islanded VI adjustment	MT-DC optimal current redistribution
Key challenge	Selectivity under variable DER	Submillisecond response without zero-crossing
Preferred FCL type	SFCL + Virtual impedance	Hybrid DC FCL (SFCL + SSFCL)

Abbreviations: AC, alternating current; DC, direct current; DER, distributed energy resource; FCL, fault-current limiter; MT-DC, multiterminal DC; SFCL, superconductor fault-current limiter; SSFCL, solid-state FCL; VI, virtual impedance.

in current power systems [99]. During a short-circuit incident, the significant voltage sag at the PCC threatens the continuing functioning of inverter-based DERs, such as wind turbines (e.g., DFIGs) and solar PV plants [100]. By rapidly introducing high impedance into the fault line, FCLs dramatically minimize the voltage loss at the PCC. This dynamic voltage support is crucial for enabling renewable generating units to ride through the problem without tripping, thereby reducing cascading outages and ensuring compliance with contemporary grid rules. From the standpoint of SGs, the added impedance restricts the decline in electrical power production during the malfunction. This decrease in the generator's accelerating power immediately raises the critical clearing time (CCT) and broadens the overall transient stability margin [101]. Consequently, FCLs act not just as current-limiting safety devices, but as vital dynamic stability enhancers that protect the continuous and robust operation of renewable-rich grids.

3. *Impact of FCLs on System Transient Stability:* Transient stability, defined as the power system's ability to maintain synchronism during severe disturbances, is a critical operational constraint in modern grids. Strategic placement of FCLs significantly improves transient stability margins, with effects varying across generation technologies:

- *SGs and Large-Signal Stability (Equal-Area Criterion):* In conventional SGs, transient stability is determined by the swing equation and assessed using the equal-area criterion. During a severe short-circuit, electrical power output (P_e) drops sharply, resulting in significant accelerating power ($P_m - P_{e,\text{fault}}$) and a rapid increase in rotor angle (δ). The accelerating area (A_{acc}) is defined in the following equation:

$$A_{\text{acc}} = \int_{\delta_0}^{\delta_d} (P_m - P_{e,\text{fault}}) d\delta. \quad (24)$$

By inserting a resistive FCL, a substantial active impedance (R_{FCL}) is introduced into the fault loop. This actively consumes active power during the fault, thereby elevating the fault-state electrical power $P_{e,\text{fault}}^{\text{FCL}}$ as shown in Equation (25).

$$P_{e,\text{fault}}^{\text{FCL}} = \frac{E/V_s}{X'_d + X_{\text{FCL}} + X_{\text{line}}} \sin \delta + I_{\text{fault}}^2 R_{\text{FCL}}. \quad (25)$$

This dynamic intervention substantially reduces the accelerating area (A_{acc}) and increases the maximum available decelerating area ($A_{\text{dec,max}}$). As a result, FCLs suppress the first-swing rotor angle peak and significantly extend the CCT, often by 15%–40% as reported in standard IEEE test systems [102]. This extension prevents pole-slipping and maintains generator synchronism.

- *IBRs (Transient Synchronization Stability):* In converter-dominated grids, such as those incorporating DFIG wind farms and solar PV systems, transient instability primarily arises from phase-locked loop (PLL) synchronization failure rather than from mechanical rotor swings. During severe voltage sags, the PLL may lose its voltage-tracking capability, leading to control instability and cascaded inverter tripping [103]. FCLs address this issue by decoupling the PCC from the deep fault, thereby clamping the voltage sag and maintaining V_{PCC} above critical Low-Voltage Ride-Through (LVRT) thresholds. This approach prevents PLL desynchronization and limits transient rotor overcurrents, ensuring that converters remain within their safe operational limits.
- *MT-HVDC Transient Stability:* In multiterminal HVDC networks, transient stability depends on the DC-link voltage profile. The rapid insertion of solid-state and hybrid FCLs prevents catastrophic discharge of DC-link capacitors, thereby preserving the DC voltage stability margin [104]. This action avoids mandatory converter blocking and enables rapid restoration of transient active power transfer capability following fault clearance.

Alongside these technical advancements, the primary economic benefit of deploying FCLs is avoiding costly infrastructure upgrades for lower-rated equipment. By rapidly inserting series impedance to clamp fault magnitudes within the interrupting capabilities of existing breakers, FCLs significantly enhance overall system reliability and stability [105]. Furthermore, they facilitate the robust operation of parallel and highly meshed grids without violating short-circuit constraints, thereby accelerating post-fault recovery and enhancing transient stability. Building upon these critical device-level features, the successful grid integration of FCLs necessitates careful coordination with traditional protection schemes to maintain strict selectivity and ensure optimal fault isolation.

4 | Coordination of FCLs With Protection Devices

4.1 | Optimal Parameter Design and Placement Strategies

To support the efficient and secure operation of the electrical power system, it is necessary to properly coordinate FCL and traditional protection devices such as CBs, relays, and fuses [106, 107]. This is needed for several reasons:

- **Altered Fault-Current Profiles:** The primary role of FCL is to limit the fault-current value. This depends on its position, as different areas of the network have low current. It may affect distant areas if installed near the source or load, because only a few areas of the network will experience low currents.
- **Protection Sensitivity and Selectivity:** The setting of conventional devices is based on anticipated fault currents at the point of installation, assumed to remain constant throughout the system's operating life. When FCL is implemented, fault currents change throughout the network, and the settings of protection devices need to be re-appraised to avoid malfunctions. The addition of FCL impedance Z_{FCL} into the fault loop modifies the apparent impedance observed by distance relays [108]. Without FCL, the observed impedance is $Z_{app} = V_{relay}/I_{fault} = Z_{line}$. With FCL, the apparent impedance becomes $Z_{app} = Z_{line} + Z_{FCL}$, leading the relay to underreach—viewing the fault as more than its real position. This underreach effect may shift the fault beyond Zone 1 coverage, slowing fault clearance from ~100 ms to Zone 2 time (~300–500 ms). Relay settings must consequently be revised to account for Z_{FCL} , especially for resistive FCL types where the extra impedance has a considerable real component that changes the measured impedance vector away from the relay's characteristic circle.
- **Prevention of Protection Blind Spots:** A wrongly located FCL may result in currents below the level of detection being drawn during a fault, thereby making some faults undetected or unexplained. Coordination today involves ensuring even low currents are detectable and that effective fault isolation is achieved. A prominent example of this vulnerability occurs in distribution networks, where fuse-recloser coordination relies on maintaining a precise time-current grading margin between the fuse melting curve and the recloser fast-curve operation. FCL insertion reduces fault-current magnitudes, shifting both curves along the time-current plane. If the FCL-limited current falls below the fuse minimum melting current, the fuse loses its ability to interrupt the fault, a condition specifically known as protection blinding. Mathematically, the minimum FCL-limited fault current (I_{FCL}) must satisfy the following equation:

$$I_{FCL} > I_{fuse-min} = K \cdot I_{rated}, \quad (26)$$

where K is the fuse-coordination factor (typically 1.25–1.5). FCL sizing must therefore incorporate this constraint as a lower boundary condition alongside the upper boundary of the breaker interrupting rating.

- **Effect on Differential Protection:** Transformer and busbar differential protection methods rely on a current balance between primary and secondary measurements [109]. FCL insertion in series with the protected element creates a current-limiting impact that may produce a transient differential current mismatch during the FCL transition phase—notably for R-SFCLs where the quench transition takes 2–10 ms. During this time, the differential relay may detect a false differential current $\Delta I = I_{primary} - I_{secondary} \neq 0$, thereby triggering unintended tripping. This is reduced by either (i) adjusting the differential relay constraint slope k_{slope} to accommodate FCL transition current, or (ii) inserting a small-time delay (5–15 ms) in the differential element coordinated with the FCL quench time [110]. **System Stability and Reliability:** FCL placement also impacts fault currents and dynamic system performance. A coordinated approach helps avoid cascading, overload, or instability normally associated with failure events.

The appropriate distribution of FCLs in a power network provides several benefits. These benefits include enhancing system reliability and security, reducing fault current and voltage sags, improving FRT capability, and increasing the integration of RESs. Various approaches for determining the optimal location and parameters have been reported in the literature [111, 112]. The FCL's impact on a power network's performance, particularly during issues, necessitates careful optimization.

Several objectives are typically proposed for this optimization. The primary goals are to minimize the total cost of the FCLs and mitigate the network's fault current to ensure the safety of power system equipment. The number, parameters, and location of FCLs are all crucial factors that define the benefits of incorporating them into radial distribution or loop transmission systems [113, 114]. Optimization problems with multiple conflicting objectives often use specific techniques. For example, the weighted sum technique combines several objectives into a single function by assigning weight coefficients based on their relative importance. The Pareto technique is used to handle multiple conflicting aims, such as cost reduction and total fault-current mitigation, by identifying a set of optimal, non-dominated solutions known as the Pareto Front [115].

As shown in Table 8, the optimal location, size, and number of FCLs have been investigated across various test systems, from standard to practical applications. As demonstrated in Table 8, formulating the objective functions requires a careful balance of both technical and economic factors. From a technical perspective, the ideal distribution of FCLs enhances the system's overall stability, security, reliability, and fault-riding capability. In addition, optimizing the allocation of FCLs increases the power system's hosting capacity, allowing for greater integration of RESs. From an economic standpoint, this optimization reduces financial burdens, as the installation and maintenance of FCLs are typically more expensive than those of protective equipment. Various optimization techniques have been employed to identify the best distribution of FCLs for both single-objective and multiobjective functions [126].

Read jointly, the entries in Table 8 reveal a discernible pattern in problem-scale suitability that is not evident from any single

row in isolation. Across the population-based metaheuristic studies included in the table, OPSO, GA, NSGA-II/MOEA, the multiobjective bat algorithm, hybrid PSO-GSA, multiobjective coyote optimization algorithm (MOCOA), and discrete continuous PSO, the reported applications are limited to small- and medium-scale distribution test systems, with the largest reported distribution case involving 85 buses. Within these studies, the reported computational characteristics also reflect a trade-off between search behavior and computational burden: Multiobjective particle swarm optimization (MOPSO) is associated with fast convergence but a risk of local-optimum entrapment, while NSGA-II and MOCOA are reported to incur increased computational effort as problem complexity grows. By contrast, the only study in Table 8 evaluated at transmission scale is the iterative mixed-integer nonlinear programming formulation applied to a 395-bus network, which provides deterministic solutions but also reports dimensionality-related limitations for larger grids. Within the studies included in Table 8, no population-based metaheuristic FCL allocation formulation was evaluated on a transmission-scale test system. This observation suggests that the scalability of such approaches for larger transmission networks has not been sufficiently demonstrated in the reviewed studies. Accordingly, optimizer selection should be guided by the formulation of the FCL allocation problem, the number and types of decision variables, the network scale, and the computational requirements, rather than by generic assumptions about the superiority of any particular algorithm. To overcome the constraints of deterministic techniques, current advanced methodologies rely on robust frameworks:

- A. *Sources of Uncertainty in FCL Allocation:* The optimal allocation of FCLs in contemporary power networks is inherently subject to many sources of uncertainty that deterministic optimization techniques fail to capture. These include: (i) stochastic variability of renewable energy generation PV output follows a Beta distribution parameterized by solar irradiance statistics, while wind power follows a Weibull distribution governed by site-specific wind speed parameters; (ii) load demand uncertainty, modeled as a normal distribution $N(\mu L, \sigma^2 L)$ around the forecast mean load μL ; (iii) network topology uncertainty arising from random equipment outages and planned switching operations; and (iv) fault occurrence probability, typically represented as a Poisson process with rate parameter λ_f (faults/year/km) [127]. Ignoring these uncertainties leads to FCL placements that are optimum only under assumed nominal circumstances but may fail to sustain protection coordination or fault current limiting during off-nominal operating situations.
- B. *Stochastic Optimization Framework:* Stochastic programming provides a logical framework for FCL allocation under uncertainty by maximizing expected performance across a set of probabilistic scenarios. The two-stage random FCL allocation problem is defined by Equation (27).

$$\min_x c^T x + \mathbb{E}_\xi [Q(x, \xi)], \quad (27)$$

where x is the binary vector representing FCL placement choices, $c^T x$ represents the CAPEX cost of chosen sites, ξ is

the random vector encapsulating DER output and load uncertainty, and $Q(x, \xi)$ is the second-stage recourse cost assessed for each scenario realization. The expectation $\mathbb{E}_\xi [Q(x, \xi)]$ is estimated by SAA utilizing N_s Monte Carlo scenarios generated from the joint probability distribution of ξ [128]. Convergence of the SAA solution is assured as $N_s \rightarrow \infty$. FCL size optimization is embedded as a continuous second-stage variable: $Z_{FCL,i} \in [Z_{\min}, Z_{\max}]$, where $Z_{\max}$ is constrained by normal-operation voltage drop limits as illustrated in the following equation:

$$\Delta V_i = I_{\text{Load}} \cdot Z_{FCL,i} \leq 0.03 \cdot V_{\text{rated}}, \quad (28)$$

ensuring the FCL does not introduce unacceptable voltage regulation under peak load conditions.

- C. *Robust Optimization Approach:* As an alternative to stochastic programming, robust optimization seeks FCL placements that remain viable and near optimal for all realizations of uncertainty inside a particular uncertainty set U . The robust FCL allocation issue is phrased as

$$\min_x \max_{\xi \in U} F(x, \xi)$$

Subject to $g_j(x, \xi) \leq 0, \forall \xi \in U, j = 1, \dots, m$, where $F(x, \xi)$ is the worst-case objective (e.g., highest fault current), and $g_j(x, \xi)$ reflects protective coordination restrictions. The uncertainty set U is commonly specified as a box set or an ellipsoidal set calibrated to previous DER generation data. The conservativeness of the robust solution is adjusted by a budget-of-uncertainty parameter $\Gamma \in [0, n]$, enabling utilities to trade-off between solution robustness and cost efficiency—a significant practical factor given the high CAPEX of FCL installations.

- D. *Chance-Constrained Programming:* Chance-constrained programming provides a compromise between deterministic and completely robust formulations by demanding that protection coordination conditions be fulfilled with a defined minimum probability level α (confidence level):

$$\text{Prob}\{I_{\text{Fault},i}(x, \xi) \leq I_{\text{CB,rated},i}\} \geq \alpha, \quad \forall i \in N_{\text{buses}},$$

$$\text{Prob}\{I_{\text{relay},j}(x, \xi) \geq I_{\text{pickup},j}\} \geq \alpha, \quad \forall j \in N_{\text{relays}},$$

where α is commonly adjusted to 0.90–0.99 depending on the criticality of the protected element. The first restriction guarantees that FCL-limited fault currents stay within CB interrupting ratings with probability α , while the second assures that FCLs do not drop fault currents below relay pickup thresholds, addressing the protection blinding danger.

4.2 | Communication-Assisted and Adaptive Coordination in Smart Grids

In modern smart grids and microgrids, FCL deployment is increasingly combined with communication-assisted, adaptive protection designs. Centralized microgrid controllers continuously monitor grid topology and DG status to dynamically change relay

TABLE 8 | Various approaches for FCLs' optimum allocation.

Reference	Objective function	Optimization method	FCL type	Advantages of optimizer	Disadvantages of optimizer	Practical	Standard
[116]	Minimum coordination index and FCL size	Multiobjective particle swarm optimization (MOPSO)	SFCL/SSFCL	- Fast convergence speed - Excellent at mapping complex Pareto fronts	- High risk of trapping in local optima - Sensitive to initial parameter settings		IEEE 33-bus and part of IEEE 30-bus
[117]	Minimum protection cost	Genetic algorithm (GA)	Solid-state (SSFCL)	- Highly robust in discrete spaces - Search global space effectively	- High computational burden - Slower convergence near optimal solutions	13-Bus distribution system	
[118]	Reliability of power system, economic impact. Increase the power network reliability and reduce the fault-current and short-circuit current reduction	MOPSO, nondominated sorting GA (NSGA-II), and multiobjective evolutionary algorithm (MOEA)	Resistive SFCL	- NSGA-II provides superior elite preservation - Well-distributed nondominated solutions	- High computational time for multisource topologies - Complex parameter tuning		IEEE 39- and IEEE 57-bus systems
[119]	Minimum costs and fault currents to levels within the breakers' limits	Iterative mixed-integer nonlinear	Inductive/resistive FCL	- Provides exact analytical and deterministic solutions - No stochastic chattering	- Highly sensitive to initial initialization - Suffers from curse of dimensionality in large grids	North American 395-bus transmission	IEEE 9- and IEEE 30-bus systems
[120]	Minimum Cost, fault-current mitigation, and maximum load reliability index	Multiobjective bat algorithm with Monte Carlo simulation	SFCL/active FCL	- Exceptional exploration capability - Balances local and global search via echolocation mimicry	- Tends to converge prematurely in highly nonlinear constraints - Poor exploitation phase		IEEE 33- and IEEE 30-bus systems
[121]	Maximizing the mitigation effect of FCLs and minimizing the FCLs cost	Hybrid PSO-gravitational search algorithm	Resistive type	Combines the social thinking of PSO with the local search strength of GSA	Extremely high algorithmic complexity		IEEE 33 kV meshed distribution system

(Continues)

TABLE 8 | (Continued)

Reference	Objective function	Optimization method	FCL type	Advantages of optimizer	Disadvantages of optimizer	Practical	Standard
[122]	Minimizing power losses, fault currents, FCL size, voltage deviation, and voltage stability index	A multiobjective coyote optimization algorithm (MOCOA)	Resistive SFCL	- High acceleration profile - Outstanding performance in multiscenario settings - High adaptation to time-varying bounds	- Significant computational overhead per iteration - Complex social structure equations - Slower execution rate in large networks	85-Bus Egyptian system of the East Delta Network (EDN)	IEEE 33-, 69-, and 37-bus systems
[123]	Limiting the high current by a resistive type of superconducting FCL	Simulation by means of PSCAD/EMTDC software	Resistive SFCL	Captures nonlinear transient quenching with ultrahigh fidelity	- Lacks automated optimization searching loops - Trial-and-error dependent		Three-terminal HVDC system
[124]	Increase the reliability, minimize power loss, and economical use FCLs	A combination of discrete and continuous PSO	SFCL	Accurately handles mixed integer problems (binary location, continuous size)	Premature convergence in complex multimodal landscapes		Modified RBTS 2-bus test system
[125]	Minimizing fault current and power losses	Electrical transient analyzer program (ETAP) and a fuzzy-based multiobjective mechanism	Solid-state (SSFCL)	Converts heuristic operator experience into robust linguistic rules	Highly dependent on the subjectivity of membership function design		IEEE 21- and 28-bus distribution systems

Abbreviations: EMTDC, electromagnetic transients including DC; FCL, fault-current limiter; HVDC, high-voltage direct current; PSCAD, power systems computer-aided design; PSO, particle swarm optimization; RBTS, Roy Billinton Test System; SFCL, superconductor fault-current limiter; SSFCL, solid-state FCL.

settings, organically accounting for FCL operation [129]. This adaptive system enables main relays to respond immediately to local fault readings, while a supervisory controller ensures effective coordination in both radial and meshed topologies. For this degree of dynamic adaptability, FCLs should be considered as proactive protection elements within an integrated smart-grid framework. Within this tiered framework—spanning field devices, communication infrastructure, and control centers—FCLs interface with the energy management system and the distribution management system to offer real-time awareness of fault currents. The integration of FCLs with supervisory control and data acquisition (SCADA) systems and phasor measurement units (PMUs) provides a major enabler for this wide-area coordination [130]. SCADA systems provide supervisory control of FCL operating states (normal, limiting, and recovery), enabling remote monitoring and post-fault analysis. Concurrently, PMUs give subcycle visibility of voltage and current phasors at FCL installation locations. This high-resolution data are exploited to (i) detect the onset of fault conditions with greater sensitivity, particularly under the low-fault-current signatures of inverter-dominated networks; (ii) validate FCL triggering events; and (iii) provide feedback signals for adaptive FCL impedance control [131]. The communication delay required for PMU/FCL coordination should therefore be considered alongside the applicable IEC 61850 communication requirements.

To implement these communication-aware frameworks, several quantitative requirements should be considered in four key areas: latency, bandwidth, synchronization accuracy, and cybersecurity. To distinguish documented requirements from illustrative or forward-looking content, this subsection explicitly labels each quantitative threshold as either directly specified by a named standard, calculated from a named standard via an explicit derivation, or an authorial estimate/recommendation offered for illustrative or research-direction purposes.

1. *Communication Latency Requirements:* IEC 61850-5 specifies five performance classes for maximum end-to-end message transfer times in protection applications [132]. For FCL-relay coordination in smart grids, the relevant classes are: Class P2 (less than 20 ms) for adaptive overcurrent-relay setting updates sent from the supervisory controller to field relays after FCL state changes; Class P3 (less than 10 ms) for busbar protection and fast differential schemes, where FCL quench transitions must be communicated to prevent spurious tripping; and GOOSE multicast (less than 4 ms) for interlocking signals between FCL controllers and adjacent CBs during zone-selective isolation. The 4/10/20 ms thresholds themselves are specified directly by IEC 61850-5 [132]; their assignment here to specific FCL-coordination use cases is the authors' interpretive application of these general performance classes, since IEC 61850-5 does not itself address FCL-specific communication. During rapid network reconfiguration, such as tie-switch closure after a feeder fault, updated FCL impedance setpoints should reach all coordinated protection devices within approximately one protection operating cycle; we adopt 100 ms as a representative engineering approximation for this purpose, consistent with the reconfiguration timescales discussed in [133], rather than as a value explicitly specified by a

single standard. If these latency requirements are not met, there is a period of uncoordinated protection operation, which may lead to unnecessary load interruptions or failure to isolate faults.

2. *Bandwidth Requirements:* The communication infrastructure for FCL-integrated adaptive protection must meet specific minimum bandwidth requirements. IEC 61850 GOOSE messages require about 100 kbps per intelligent electronic device for binary state exchanges, including FCL status, relay trip signals, and interlocking commands [134]. IEC 61850-9-2 SV for high-resolution current and voltage measurements at FCL monitoring points requires 100 Mbps per substation bay, based on an 80 samples-per-cycle rate at 50 Hz. IEEE C37.118 PMU data streams require 10–100 kbps per PMU, depending on the reporting rate, typically 25–120 frames per second [135]. A representative WAMS backbone capacity of around 1 Gbps per substation may be appropriate for supporting simultaneous GOOSE, SV, and PMU traffic, depending on the communication architecture and traffic load. Operating below these bandwidth thresholds increases the risk of packet collisions and retransmission delays, which can compromise protection selectivity during critical post-reconfiguration periods.
3. *Synchronization Accuracy Requirements:* Accurate time synchronization is essential for PMU-based FCL coordination, differential protection, and sequence-of-events recording across distributed FCL installations [136, 137]. The following accuracy standards apply: GPS-based synchronization offers $\pm 1 \mu\text{s}$ absolute accuracy and serves as the reference for WAMS. IEEE 1588 precision time protocol also provides $\pm 1 \mu\text{s}$ accuracy over dedicated LANs and is recommended for substation-level FCL coordination when GPS signals are unreliable. IEEE C37.118-2 requires a maximum Total Vector Error (TVE) of 1% for PMU measurements in protection applications [136]. This standard-specified TVE limit equates, via the standard small-angle phase-to-time relationship at 50 Hz, to a maximum phase angle error of ± 0.01 radians and a corresponding timing error of $\pm 31.8 \mu\text{s}$, a value we calculate from the standard's TVE requirement rather than one stated explicitly in the standard itself. For FCL-assisted differential protection, we estimate that timing errors greater than ± 1 ms could produce apparent differential currents on the order of 0.3% of rated current, an illustrative approximation rather than a value drawn from a specific field or test report, potentially leading to false trips in sensitive high-impedance schemes. During network reconfiguration, synchronized timestamps on FCL state transitions and relay operations allow the centralized protection controller to update relay settings in the correct sequence, ensuring coordination margins are restored in the proper order across all affected zones.
4. *Cybersecurity Requirements:* Integrating FCLs into communication-assisted protection frameworks introduces cybersecurity risks that must be addressed to ensure system integrity. Three main threats are relevant. First, false data injection attacks on PMU data streams can alter fault-current measurements, leading to premature FCL activation or failure to

respond during actual faults [138]. Second, man-in-the-middle attacks on GOOSE interlocking messages can falsify FCL state signals, disrupting coordination and causing either missed trips or unnecessary tripping [139]. Third, denial-of-service attacks on the communication backbone can introduce artificial latency, violating performance requirements and leading to periods of uncoordinated protection [140].

The applicable security standards for FCL communication infrastructure are: IEC 62351 (Parts 1–8), which specifies authentication, encryption, and access control for IEC 61850 GOOSE and Sampled Value messages using transport layer security and role-based access control; IEC 62443, which defines security levels for industrial automation and control systems, with FCL controllers classified as Security Level 2 (protection against intentional violation using simple means) at minimum; and NERC CIP-007 (systems security management), applicable to FCL installations in bulk electric systems, which mandates port and service management, patch management, and security event monitoring.

A key research gap identified in the reviewed literature is the limited availability of standardized cybersecurity testing frameworks for FCL-integrated protection systems. The strict latency requirements of protection-class communication (the standard-specified sub-4-ms GOOSE threshold [132]) often conflict with the computational demands of cryptographic authentication. We propose, as an open research direction rather than a demonstrated result, that lightweight authentication schemes, such as hardware-accelerated message authentication codes (HMAC-SHA256) implemented in dedicated security co-processors, merit dedicated investigation as a candidate approach to meeting this latency constraint.

Together, these quantitative requirements define the communication infrastructure envelope within which FCL parameters, relay characteristics, and microgrid controllers can be co-optimized to form a cohesive, resilient system.

4.3 | Synthesis of Literature and Emerging Optimization Trends

The reviewed literature shows several recurring themes in FCL coordination and allocation. A number of studies suggest that FCLs can be particularly effective when strategically deployed at nodes, where they may concurrently reduce fault levels at many important buses, so deferring equipment upgrades and permitting higher DER penetration, while avoiding protection “blind spots” and loss of relay sensitivity. Coordination with overcurrent and distance relays may require reassessment of pickup currents and time–current characteristics after the introduction of FCLs, particularly in meshed and inverter-dominated networks, where short-circuit levels are close to protection thresholds.

From an optimization standpoint, key themes include the creation of multiobjective placement and sizing problems and the employment of metaheuristic algorithms to solve them. Representative works employ GAs, MOPSO, NSGA-II, Jaya, and improved coyote optimization to discover optimal FCL placements

and settings, frequently in combination with DG siting [141]. Typical objectives are to limit short-circuit currents, investment cost, and active-power losses, while maximizing reliability indices or voltage stability margins under contingency situations [142]. More recent contributions expand this approach to multi-type FCLs and microgrids, demonstrating that multiple FCL technologies may be optimal at different buses within the same system.

Key Takeaways:

Overall, the reviewed studies suggest that (i) FCL placement should be considered a system-level optimization problem rather than a purely local design choice; (ii) relay coordination and, if applicable, converter protection settings must be co-designed with FCL parameters; and (iii) multiobjective optimization tools offer utilities a useful way to quantify the trade-offs between fault-level mitigation, cost, losses, and reliability when planning FCL deployment.

5 | Current Challenges and Outlook of FCLs in Smart and Resilient Power Systems

The transition toward smart and resilient power systems, characterized by high DER penetration, inverter-dominated generation, and frequent network reconfiguration, reshapes short-circuit behaviors and challenges conventional protection philosophies. In future grids, fault levels and fault signatures may vary widely with operating mode (grid-connected or islanded), topology (reconfiguration and restoration switching), and control states of converters. Consequently, utilities increasingly require solutions that keep fault currents within breaker interrupting capabilities while preserving selectivity and enabling higher DER hosting capacity. FCLs, across superconducting and nonsuperconducting families, provide a promising pathway; however, their value in emerging grid scenarios depends on systematic, scenario-driven deployment and coordination with protection and control layers.

5.1 | Scenario-Driven Application Possibilities

1. *DER-Dense Distribution Networks:* High penetration of PV, wind, and storage might increase prospective fault levels at specific buses (at substations or feeder interties) while concurrently producing converter-shaped, and sometimes limited, fault currents in downstream portions. Properly placed FCLs can reduce equipment upgrade requirements, expand hosting capacity, and restore coordination margins at crucial nodes (substations, tie lines, and sectionalizing points). The significant difficulty is ensuring protection, security, and selectivity under switching and DER variability, necessitating the collaborative design of FCL sizing/ placement with relay, recloser, and fuse coordination.
2. *Microgrids and Island Operation:* Microgrids encounter dramatic variations in fault-current amplitude and waveform between grid-connected and island modes. FCLs can reduce the need for mode-dependent protection retuning and support robust reconnection by minimizing excessive currents during resynchronization. Beyond FRT, an additional aspect of FCL

value in microgrids is their potential contribution to smooth and uninterrupted operation, the capacity to sustain continuous, stable service without load disconnection throughout all operational states and RES generation levels. Smooth and continuous operation is a critical pillar of power system resilience, especially in freestanding DC microgrids, where the lack of grid support puts the system totally reliant on local production and storage resources. Under high-RES penetration, rapid fluctuations in PV and wind output introduce frequent transient overcurrent events as the DC-bus voltage controller attempts to balance generation and load—events that, without current limiting, may trigger false protection operations and cause unnecessary load shedding. Under low-RES penetration, the lower system inertia and fault-current contribution pose the opposite challenge: fault currents may fall below relay pickup levels, producing protection blind spots and delayed fault isolation that needlessly disrupt service. FCLs handle both extremities of this operating spectrum. At high-RES penetration levels, FCLs clamp transient overcurrents within the interrupting capabilities of DCCBs, reducing nuisance tripping and ensuring power continuity to important loads. The FCL successfully decouples the fault-current magnitude from source impedance fluctuations caused by variable RES output, ensuring that the protection system operates at stable, predictable current levels independent of instantaneous generation dispatch. At low RES penetration levels, the FCL's small normal-operation impedance preserves relay sensitivity by avoiding the voltage drop that would otherwise diminish fault-current detectability, thereby maintaining protection selectivity without compromising continuity. Resilient grids (restoration and reconfiguration): Resilience solutions increasingly rely on quick sectionalizing and reconfiguration to restore key loads after contingencies. Such topological changes can abruptly affect short-circuit levels and disrupt coordination. Strategically located FCLs, particularly at interties and important corridors, can “decouple” fault levels over reconfiguration areas, enabling rapid restoration without violating interruption ratings. An important research direction is co-optimizing restoration switching and FCL operational states/parameters, employing resilience-oriented objectives (e.g., load restored, restoration time) in addition to typical fault-level limitations.

3. **HVDC and Multiterminal HVDC (MT-HVDC) Grids:** Although most deployments are in AC systems, the rise of VSC-HVDC and MT-HVDC makes DC-side fault mitigation increasingly essential due to quick fault propagation and converter sensitivity. Solid-state and hybrid FCL methods may be particularly interesting for ultrafast limitation. To provide actionable design references for FCL integration in these systems, the following illustrative benchmarks, computed from representative parameter ranges reported in the cited literature rather than from dedicated simulations or field measurements in this review, characterize typical DC fault behavior and FCL performance requirements in VSC-HVDC and MT-HVDC networks.
4. **DC Fault-Current Rise Rate and Peak-Current Benchmarks:** In VSC-HVDC systems, the DC-side fault current increases at a rate determined by the cable or overhead

line inductance and the DC-bus capacitance [143]. For underground HVDC cables, which are prevalent in offshore wind and interconnector applications, the fault-current rate of increase is represented in Equation (29).

$$\frac{di_{DC}}{dt} = \frac{V_{DC}}{L_{cable}} \approx 1 - 10 \text{ kA/ms}, \quad (29)$$

where L_{cable} is typically 0.2–2 mH/km for HVDC cables, and VDC ranges from ± 200 to ± 525 kV in current commercial deployments. For a ± 320 -kV link with a 50-km cable, the fault current can reach 10–15 times the rated converter current within 5–10 ms if current limiting is not applied. This far exceeds the 2–3 times rated current withstand capability of press-pack IGBT devices commonly used in voltage source converter (VSC) converters [144, 145]. Therefore, the FCL must insert enough impedance to limit the first-peak fault current below the IGBT withstand level before the converter blocking threshold is reached, typically within 1–3 ms of fault inception.

For overhead HVDC lines used for long-distance bulk power transmission, higher inductance (1–5 mH/km) reduces the initial di/dt but increases fault energy due to a longer fault duration before detection. In these cases, the peak fault-current benchmark is 8–12 kA for a ± 500 -kV, 3000-MW link. To keep currents within the DC breaker's interrupting capability, an FCL impedance insertion of $Z_{FCL} \geq 5\text{--}15 \Omega$ is required.

- **FCL Response-Time Requirements:** The SSFCL response time in VSC-HVDC systems depends on the converter IGBT's thermal withstand capability. The maximum allowable fault energy dissipated in the IGBT during the fault interval is defined in the following equation:

$$E_{IGBT,max} = \int_0^{t_{block}} V_{CE} \cdot i_{fault}(t) dt \leq E_{SC, rated}, \quad (30)$$

where V_{CE} is the collector-emitter voltage during a short circuit, and $E_{SC, rated}$ is the device-rated short-circuit energy, typically 1–5 J for 4.5 kV/2000 A press-pack IGBTs. Using typical fault-current profiles, the maximum permissible fault duration is $t_{block} = 2\text{--}10$ ms before converter blocking is required [146]. Therefore, the FCL must reach its full current-limiting impedance within

$$t_{FCL} \leq t_{block} - t_{detection} \leq 2.5 \text{ ms},$$

where $t_{detection} = 0.5\text{--}1$ ms accounts for fault detection algorithms (di/dt threshold or undervoltage detection). Under these benchmark response-time requirements, SSFCLs (typically 1 μ s–1 ms) and HFCLs ($< 1\text{--}2$ ms) are more likely to satisfy the strict limitation window. In contrast, R-SFCLs (often exhibiting response times of 2.5–10 ms) may be borderline for HVDC converter protection and could require supplementary crowbar arrangements, depending on the specific converter and fault characteristics.

- **DCCB Coordination Benchmarks:** The FCL must reduce fault current to a level within the DCCB interrupting capability before interruption occurs. Mechanical DCCBs

interrupt in 30–50 ms at 8–16 kA, which limits offshore use [147]. Hybrid DCCBs, such as those from asea brown boveri (ABB) and general electric (GE), interrupt in 2–5 ms at 9–16 kA, making them suitable for MT-HVDC backbones. Solid-State DCCBs interrupt in less than 1 ms but are limited to 4–8 kA, primarily serving DC distribution and MVDC applications.

The FCL must limit the fault current to below the DCCB maximum interrupting current ($I_{CB,interrupt}$) within the DCCB interruption time. For a Hybrid DCCB with a 5-ms interruption time and a 9-kA interrupting capability on a ± 320 -kV link with a rated current of 1.8 kA, the needed FCL current limitation ratio is as given in Equation (31). This operating point is drawn from the seminal industry publication introducing the hybrid HVDC breaker concept [148], which reports a 9.0-kA breaking capability for a 320-kV HVDC grid with 2 kA rated transmission current, the same order of magnitude adopted in this illustrative example.

$$\eta_{FCL} = \frac{I_{fault,no-FCL}(t_{CB})}{I_{CB,interrupt}} = \frac{15 \text{ kA}}{9 \text{ kA}} \approx 1.67. \quad (31)$$

Assuming a single pole-to-ground fault (the most prevalent fault type, applying $V_{DC,pole} = 320$ kV), the corresponding minimum FCL impedance is shown in Equation (32):

$$Z_{FCL,min} = \frac{V_{DC,pole}}{I_{CB,interrupt}} - R_{line} \approx \frac{320 \text{ kV}}{9 \text{ kA}} - 0.5 \Omega \approx 35 \Omega. \quad (32)$$

$R_{line} \approx 0.5 \Omega$ represents the pure DC resistance of the 50-km cable (inductive reactance is neglected as it does not limit the steady-state peak fault current). This impedance benchmark, derived from the DCCB operating point of [148], provides a concrete design target for FCL sizing in ± 320 kV MT-HVDC applications that is not widely reported in the FCL literature reviewed here.

- **Energy Absorption and Converter Blocking Benchmarks:** During fault-current limitation, the FCL must absorb the energy stored in the DC network inductance without thermal damage. The total energy to be dissipated by the FCL during the fault interval is shown in Equation (33).

$$E_{FCL} = \frac{1}{2} L_{DC} I_{Peak}^2 - \frac{1}{2} L_{DC} I_{CB,interrupt}^2 = \frac{1}{2} 50 \text{ mH} \times [(15 \text{ kA})^2 - (9 \text{ kA})^2] \approx 3.6 \text{ MJ}. \quad (33)$$

For a representative MT-HVDC pole with $L_{DC} = 50$ mH (including the smoothing reactor), consistent with reported MMC-HVDC fault-current-limiting circuit designs [149], the energy absorption requirement is 3.6 MJ per single fault event. This value provides a benchmark for the thermal design of the FCL energy-dissipation element, such as the MOV arrester for SSFCLs or the HTS conductor for SFCLs, and is about 200 times higher than the requirement for MV distribution FCL applications. For SFCLs, this benchmark determines the minimum HTS tape volume and cryogenic cooling capacity needed per

HVDC pole. For SSFCLs, it defines the MOV energy class and the number of parallel arrester columns. These quantitative benchmarks are not widely reported in the HVDC-FCL literature reviewed here and may help connect device-level FCL specifications with system-level HVDC protection requirements [150].

Equations (29)–(33) are expressed in general parametric form; the ± 320 -kV/9-kA operating point is one illustrative substitution rather than a restriction of the underlying relations. The same closed-form expressions apply directly to other deployed hybrid-DCCB ratings, for example, the 200 kV/3 ms/15 kA unit deployed in China's Zhoushan five-terminal DC project (2016) or the upgraded 320-kV/3-ms/20-kA ABB design reported in 2020, by substituting the corresponding $V_{DC,pole}$ and $I_{CB,interrupt}$ values.

Despite well-defined quantitative requirements, system-level studies of the coordinated operation of FCLs with DC breakers, converter-blocking schemes, and AC/DC compatibility in meshed MT-HVDC networks remain limited. A particularly important and comparatively underexplored aspect of FCL deployment in VSC-HVDC systems concerns the MMC, the dominant topology for modern HVDC and MVDC applications, whose distinctive fault dynamics impose fundamentally different requirements on FCL design and coordination compared with the two-level VSC assumed in earlier analyses.

- **MMC Fault-Current Dynamics:** Unlike two-level VSC converters, the MMC consists of series-connected half-bridge or full-bridge submodules (FBSMs) arranged in upper and lower arms per phase, with arm inductors L_{arm} providing inherent current limiting [151]. Under a DC pole-to-pole fault, the MMC fault current evolves through three distinct stages, each imposing different requirements on the FCL:

Stage 1—SM Capacitor Discharge ($t = 0$ to approximately 5 ms): The dispersed SM capacitors discharge via the low-impedance fault pathway. The fault current increases in the following equation:

$$L_{eq} \frac{di_{arm}(t)}{dt} + R_{eq} i_{arm}(t) + v_{C,eq}(t) = 0, \quad (34)$$

where $v_{C,eq}(t) = V_{DC0} - \frac{1}{C_{eq}} \int i_{arm}(t) dt$.

For a standard ± 320 -kV MMC with L_{arm} ranging from 50 to 100 mH and SM capacitance (C_{SM}) between 4 and 10 mF, the initial peak arm current can attain 8–15 kA within 3–8 ms. This is comparable to the fault currents of two-level VSC, despite the greater arm inductance, as the energy source is the distributed capacitor bank rather than solely the DC link.

Stage 2—Freewheeling Diode Conduction ($t \approx 5$ –30 ms): After all SM IGBTs are rendered nonconductive (either by overcurrent protection or intentional blocking instruction), the antiparallel diodes in each SM create an uncontrolled rectifier bridge. AC networks short-circuit current travels over this bridge, adding extra fault current as shown in the next equation:

$$I_{AC,fault} = \frac{V_{AC,LL}}{\sqrt{Z_{AC}^2 + (\omega L_{arm})^2}}. \quad (35)$$

The AC-side contribution, which is not included in basic DC fault calculations, may maintain fault current at two to four times the rated value for many tens of milliseconds after converter blockage, and cannot be restricted only by the DC-side FCL.

Stage 3—Steady-State Diode Rectification ($t > 30$ ms): The MMC functions as an uncontrolled diode rectifier until the AC CB is disengaged. The FCL must stay functional throughout this phase to restrict the prolonged AC-to-DC fault-current contribution [152].

- **FCL Placement Options in MMC-Based Systems:** The three-stage MMC fault development indicates that a single FCL placement technique cannot handle all fault-current contributions. Three placement alternatives have been examined in the literature, each offering different benefits:

(a) **DC-Side FCL:** Positioned in series with the DC pole conductor between the MMC terminals and the DC bus. This configuration successfully restricts the discharge current of the Stage 1 capacitor, using the necessary FCL impedance as shown in Equation (36):

$$Z_{\text{FCL,DC}} \geq \frac{0.5V_{\text{DC}}}{I_{\text{CB,rate}}} - R_{\text{DC,link}} \approx 30 - 50 \Omega \quad (36)$$

for ± 320 kV systems. However, DC-side FCLs cannot restrict the Stage 2 AC-side diode rectifier contribution, which bypasses the DC-side FCL totally via the freewheeling channel. SSFCLs and HFCLs are recommended for DC-side implantation owing to their submillisecond response requirement.

(b) **Arm FCL:** Placed in series with each MMC arm inductor. This arrangement reduces arm currents throughout all three fault phases, including the freewheeling diode conduction period. The arm FCL substantially raises the overall arm impedance as shown in Equation (37):

$$Z_{\text{arm,total}} = j\omega L_{\text{arm}} + Z_{\text{FCL,arm}} \quad (37)$$

Arm FCL placement allows a vital capability: nonblocking MMC functioning during DC failures. By restricting arm currents below the IGBT threshold (usually $2-3 \times I_{\text{rated}}$), the FCL permits the MMC to stay in active control mode—sustaining reactive power injection at the AC terminals throughout the fault rather than blocking and losing controllability. This non-blocking feature is critical for grid-code compliance in offshore wind applications, where reactive power supply during AC faults is necessary [153].

(c) **AC-Side FCL:** Placed between the transformer and the MMC AC terminals. This location restricts the contributions of Stages 2 and 3 AC-side diode rectifiers but has no influence on Stage 1 capacitor discharge. AC-side FCLs are compatible with all FCL technologies (SFCL, SSFCL, and HFCL) and benefit from the AC voltage zero-crossing, which permits natural current interruption.

- **Full-Bridge MMC and FCL Interaction:** FBSM MMCs provide an alternative to FCL deployment: by applying

negative SM voltages during a DC fault, the FBSM-MMC may actively oppose the fault current using its own stored energy, thereby interrupting the DC fault current without an external FCL or DCCB. The fault-current suppression time is shown in Equation (38).

$$t_{\text{suppress}} = \frac{2L_{\text{arm}}I_{\text{rated}}}{n_{\text{SM}}V_{\text{C,SM}} - 0.5V_{\text{DC}}}, \quad (38)$$

where n_{SM} is the number of SMs per arm and $V_{\text{C,SM}}$ is the SM capacitor voltage. However, this self-blocking capacity comes at a cost: about 100% increase in semiconductor losses during normal operation and 50%–100% higher converter cost compared with half-bridge MMCs (HBSMs) [154]. FCLs provide a cost-effective solution that enables HBSM-MMCs, with their reduced cost and losses, to meet DC fault protection standards without the exorbitant expense of FBSM conversion. The techno-economic trade-off between FBSM-MMC (no FCL required) and HBSM-MMC with FCL depends on system voltage level, fault frequency, and FCL lifespan costs—a comparative study that is presently lacking in the FCL literature.

- **FCL Coordination with MMC SM Balancing:** An important yet comparatively underexplored relationship concerns the interaction between FCL operation and MMC SM capacitor-voltage balancing. During normal MMC operation, the modulation algorithm continually balances SM capacitor voltages within a restricted band (usually $\pm 5\%$ of $V_{\text{C,nom}}$) [155]. When an FCL introduces series impedance during a failure, the resulting arm-current distortion upsets the energy balance between the upper and lower arms. The arm energy divergence is shown in Equation (39).

$$\Delta W_{\text{arm}} = \int_0^{t_{\text{FCL}}} (v_{\text{arm,upper}} \cdot i_{\text{arm,upper}} - v_{\text{arm,lower}} \cdot i_{\text{arm,lower}}) dt \quad (39)$$

If this energy imbalance exceeds the SM capacitor energy buffer ($0.5C_{\text{SM}}V_{\text{C,nom}}^2$ per SM), individual capacitors may overcharge or undercharge, triggering overvoltage protection and potentially causing cascaded SM bypass, effectively disabling the FCL's current-limiting function at the worst possible moment. FCL sizing and control must consequently integrate an SM capacitor energy-balancing limitation, ensuring that FCL activation does not cause arm energy deviations beyond the capacitor buffer capacity [156].

4. **Renewable Energy Integration Challenges and FCL Mitigation Strategies:** The large-scale integration of RES, predominantly inverter-interfaced PV and wind generation, introduces a distinct set of fault-current challenges that FCLs can help address. Unlike SG, which contributes sustained and predictable short-circuit currents, grid-connected inverters typically limit their fault-current contribution to 1.0–1.5 times the rated current due to semiconductor current limits, producing low-magnitude, converter-shaped fault signatures that challenge conventional overcurrent protection sensitivity [157]. Conversely, at grid interconnection points—such as PCC busbars and substation tie-lines—the aggregation of many RES units

and the lowering of grid impedance might concurrently boost probable fault levels above CB interrupting ratings [158]. FCLs mitigate these conflicting challenges through a dual mechanism: (i) at high-fault-current nodes, they insert series impedance to clamp fault magnitudes within breaker ratings, deferring costly equipment upgrades; (ii) at low-fault-current locations, their negligible normal-operation impedance preserves relay sensitivity without introducing voltage drops that would otherwise penalize RES power quality. Additionally, FCLs improve the LVRT and High-Voltage Ride-Through (HVRT) performance of RES inverters by reducing the severity of voltage disruptions during fault events, thereby avoiding unnecessary inverter disconnection and enabling grid code compliance [159]. The coordination of FCL sizing and placement with RES hosting capacity optimization as addressed through the multiobjective frameworks in Section 3.1 ensures that protection integrity is maintained as renewable penetration levels continue to increase toward national and regional decarbonization targets.

5.2 | Cross-Cutting Research Gaps

Across these scenarios, several areas remain important for further investigation and wider power-system-scale adoption:

- *Protection Coordination and Selectivity:* Quantify how FCLs affect relay sensitivity, time-current coordination (fuses/reclosers/relays), reclosing behavior, and selectivity under reconfiguration and varying DER penetration levels. For HVDC systems, coordinated studies involving DC breakers and converter protection are essential.
- *Modeling and Stability Assessment Under Uncertainty:* Develop tractable EMT and linearized/small-signal models that capture FCL transient behavior and its interactions with inverter controls and weak-grid dynamics. Robust parameter tuning and uncertainty-aware analysis are needed to avoid adverse oscillations or delayed fault recognition.
- *Placement and Sizing Optimization:* Move beyond minimizing peak fault current to a multiobjective planning approach that also accounts for hosting capacity, breaker upgrade deferral, reliability/resilience metrics, and operational flexibility.
- *Coordinated Control With Grid Devices:* Investigate coordinated strategies between FCLs and FACTS devices, adaptive protection, and converter control functions, especially in cyber-physical smart grids, where communication-enabled adaptation can improve both security and dependability.
- *Installation Constraints:* The physical deployment of FCLs in existing power infrastructure presents constraints that extend well beyond electrical ratings. For SFCLs, the combined weight of the HTS assembly and cryogenic vessel ranges from 3 to 36 tones, necessitating structural reinforcement of substation bays and careful civil engineering assessment prior to installation. Retrofitting SFCLs into existing substations is particularly challenging in urban environments, where space is limited, and dedicated buildings or underground vaults are often required. SSFCLs, being significantly lighter (a few kg to a few tones) and compact, offer greater installation flexibility and can be mounted in standard switchgear enclosures; however, their EMI emissions require adequate shielding and separation distances from sensitive measurement equipment. HFCLs present intermediate installation complexity, requiring both power-electronic rack space and a compact cryogenic unit. For all FCL types, IEEE STD C37.302 mandates compatibility with existing busbar arrangements, CT ratios, and relay panel constraints, which often necessitate site-specific adaptation studies before deployment approval.
- *Cooling Systems for SFCL:* Cryogenic cooling represents the most operationally demanding aspect of SFCL deployment. Commercial SFCL installations require continuous liquid nitrogen (LN_2) cooling at 77 K, consuming between 2 and 15 L of LN_2 per hour depending on the device rating and thermal insulation quality. The total cryogenic system—comprising vacuum-insulated vessels, LN_2 recirculation pumps, heat exchangers, and boil-off management systems—can account for 30%–45% of total SFCL installation cost and represents the primary source of ongoing operational expenditure (OPEX) [160]. Cooling system reliability is critical: a loss-of-coolant event causes the HTS material to warm above its critical temperature T_c , transitioning to the normal resistive state and potentially damaging the HTS tape if sustained fault current flows through the warmed conductor. Redundant cooling circuits and thermal alarms with automatic bypass switching are therefore mandatory for utility-grade SFCL deployments. Recent advances in conduction-cooled SFCL designs—utilizing closed-cycle cryocoolers (Gifford–McMahon or pulse-tube refrigerators) instead of open-bath LN_2 systems—offer improved reliability and reduced maintenance frequency, with demonstrated mean-time-between-maintenance intervals exceeding 10,000 h [161]. SSFCLs and HFCLs, by contrast, rely on conventional heatsink and forced-air cooling for their semiconductor components, with thermal management requirements governed by the junction-to-ambient thermal resistance and the maximum allowable junction temperature $T_j(\text{max})$ of the power devices (typically 125°C–175°C for IGBTs and IGCTs).
- *Electrothermal Quench Model Integration in System-Level Simulations:* Beyond the operating needs of cryogenic systems, the precise portrayal of SFCL quench dynamics in system-level simulations presents a distinct and equally crucial modeling challenge. The electrothermal behavior of SFCLs during quench is inherently nonlinear: as the fault current surpasses the critical current density J_c , the HTS material transitions from the superconducting to the resistive state through a strongly coupled electrothermal process in which the local temperature rise increases resistivity, which in turn increases Joule heating, further elevating temperature. This positive feedback makes the quench dynamics extremely nonlinear and time-dependent, with typical timeframes ranging from submillisecond (initial flux-flow regime) to hundreds of milliseconds (complete normal-zone propagation). Several modeling techniques for increasing fidelity have been developed for system-level simulation integration:
 - a. *Step Model:* The SFCL resistance shifts quickly from zero to a fixed value upon fault detection. While computationally easy, this model overestimates the initial rate of current restriction and includes false discontinuities that may cause

convergence difficulties in electromagnetic transient (EMT) simulation tools.

- b. *Exponential Transition Model*: The resistance grows according to Equation (13). This offers a smooth transition compatible with PSCAD/EMTDC and MATLAB/Simulink solvers and is suitable for protection coordination investigations when subcycle precision is required.
- c. *RQ Model (Resistance-Heat Capacity)*: The nonlinear coupling between resistance and temperature is captured through a lumped electrothermal model as shown in Equations (40) and (41).

$$C_{th} \frac{dT}{dt} = \rho(T, J) \cdot J^2 \cdot V_{HTS} - h_{cool}(T - T_{bath}), \quad (40)$$

$$\rho(T, J) = \begin{cases} \rho_n \left(\frac{J}{J_c(T)} \right)^{n-1}, & J \leq J_c(T), \\ \rho_n, & J > J_c(T), \end{cases} \quad (41)$$

where C_{th} is the lumped thermal capacitance of the HTS assembly, h_{cool} is the effective heat transfer coefficient to the LN_2 bath, and $J_c(T)$ is the temperature-dependent critical current density. The RQ model incorporates the thermal runaway process responsible for irreversible quench propagation and is appropriate for research requiring recurrent fault duty and thermal lifespan evaluation.

- d. *MT Model*: The most complete technique solves the coupled electromagnetic-thermal partial differential equations across the HTS conductor cross-section using FEMs. While too computationally demanding for direct incorporation into system-level EMT simulations, MT models are used to build lookup tables or reduced-order models (ROMs) that contain the nonlinear $R(T, J, B)$ characteristic as a state-dependent impedance element suitable for use with PSCAD or Simulink.

The selection among these models for system-level simulation depends on the study objective: the exponential model suffices for relay coordination and fault-level studies; the RQ model is required for thermal stress and recovery time assessment; and the MT-derived ROM is necessary for high-accuracy transient stability studies in inverter-dominated grids, where the interaction between SFCL dynamics and converter current control loops must be resolved at submillisecond timescales. One limitation evident in the reviewed literature is the limited availability of validated, publicly available PSCAD and Simulink component libraries for SFCL electrothermal models that incorporate DER-specific fault-current signatures, including inverter current saturation, reduced DC offset, and asymmetrical fault contributions [162]. Developing and testing such libraries on HIL test platforms constitutes a major research path to enable accurate system-level evaluation of FCL-integrated protection methods in future DER-rich grids. These modeling issues are reinforced by the economic limits discussed below, which, combined, define the practical hurdles to large-scale SFCL implementation.

- *Economic Feasibility CAPEX Versus OPEX*: A rigorous techno-economic evaluation of FCL deployment must distinguish between CAPEX and OPEX, as the balance between these two cost components varies substantially across FCL families and

application contexts. For SFCLs, CAPEX is dominated by HTS conductor costs (typically USD 50–200/kAm for second-generation YBCO tape), cryogenic vessel fabrication, and civil works, with total installed costs for utility-scale units ranging from USD 1–5 million per phase at transmission voltage levels. OPEX is driven primarily by cryogenic system energy consumption (0.5–2 kW/kA of protected current) and LN_2 replenishment. For SSFCLs, CAPEX is significantly lower (USD 50,000–500,000 for MV applications), but OPEX is higher due to continuous semiconductor conduction losses (rather than switching losses), which result in an ongoing energy dissipation of 0.1%–0.5% of rated power during normal operation. The economic justification for FCL investment is typically expressed through the NPV framework, as shown in Equation (42).

$$NPV = \sum_{t=1}^T \frac{B_t - C_t}{(1+r)^t} - CAPEX, \quad (42)$$

where B_t represents annual avoided costs (e.g., deferred equipment upgrades, reduced outage costs, and extended equipment lifetime), C_t represents annual OPEX, and r is the discount rate. Key benefit drivers include: (i) deferral of CB replacement or busbar splitting, with avoided costs of USD 200,000–2,000,000 per substation; (ii) reduced fault-induced equipment damage costs; and (iii) increased renewable hosting capacity revenue. Published techno-economic studies on IEEE 33- and 39-bus test systems demonstrate a positive NPV for strategically placed FCLs within a 5–8-year payback period, contingent on fault frequency and avoided upgrade costs. The absence of standardized utility-grade cost–benefit frameworks remains a primary barrier to widespread FCL adoption and represents a priority research direction for the field.

- *Climate Resilience and Physical-Hardening Against Extreme Weather Events*: While the electrical dimension of resilience (protection coordination and fault recovery) is extensively researched, the physical resilience and environmental survivability of FCL installations under extreme weather events—such as typhoons, hurricanes, and catastrophic floods—remain comparatively less developed areas of FCL research. FCLs, particularly cryogenic SFCLs and power-electronic SSFCLs, may be exposed to localized climate-induced stresses that warrant consideration of physical hardening, operational redundancy, and adaptive control:

Cryogenic Operational Integrity During Extended Power Outages: SFCL systems rely on continuous cryogenic cooling maintained by grid-powered cryocoolers. During extreme weather, primary substation power outages or physical damage to the cooling system might precipitate a significant loss-of-coolant incident. To improve operational resilience, future SFCL designs may benefit from incorporating a passive thermal ride-through window. Equations (43)–(45) combine established, individually cited thermal, structural, and electrical relations—a lumped heat balance [163], the standard wind-drag equation used in structural design codes [164], and the same I^2R thermal-energy integral already validated in Equation (14)—into a single illustrative envelope specific to FCL enclosures under extreme weather. No experimental or simulation evidence validates this

combination as an integrated framework; it is presented explicitly as a preliminary, order-of-magnitude synthesis intended to characterize an underexplored gap in the FCL literature, and dedicated experimental or simulation-based validation is identified below (Section 5.2, cross-cutting gaps) as a necessary direction for future work before these relations could inform actual design practice.

$$\frac{dT}{dt} = \frac{\dot{Q}_{\text{ingress}}}{mC_p}, \quad (43)$$

where $\dot{Q}_{\text{ingress}}$ is the parasitic heat ingress through the cryostat walls (usually restricted to < 1 W/m), m is the mass of the cryogenic fluid, and C_p is the specific heat capacity. This thermal buffer can keep temperatures below the crucial threshold ($T_c \approx 90$ K for 2G YBCO tapes) for 24–72 h without active refrigeration [165]. Active redundancy requires dedicated Uninterruptible Power Supplies in conjunction with localized battery energy storage devices. As an ultimate failsafe, if the thermal buffer is exhausted and $T \rightarrow T_c$, a fast-acting mechanical bypass switch must isolate the HTS modules within subcycles, preventing catastrophic thermal runaway caused by frequent load currents traveling through a quenched, highly resistive conductor.

- a. *Environmental Hardening and Redundancy in Typhoon-Prone Coastal Grids:* FCL systems deployed in coastal substations face a multihazard environment that combines strong wind loads, torrential downpours, and highly corrosive, moisture-laden salt-spray atmospheres. Physical hardening includes putting the auxiliary electronics and compressor components within certified marine-grade 316 L stainless steel structural enclosures. The aerodynamic wind force (F_{wind}) exerted on the FCL enclosure during a Category 5 typhoon (wind speeds $v \geq 250$ km/h) is quantified by Equation (44).

$$F_{\text{wind}} = \frac{1}{2} \rho_{\text{air}} v_{\text{wind}}^2 C_d A_{\text{enclosure}}, \quad (44)$$

where ρ_{air} is the air density, C_d is the aerodynamic drag coefficient, and $A_{\text{enclosure}}$ is the projected surface area. Enclosures must be structurally certified to sustain these severe mechanical stresses without deformation [166]. This detailed examination of physical susceptibility to airborne threats underscores the need for improved component protection. To stop wind-induced overhead line oscillations (conductor galloping) from imparting severe mechanical loads to the delicate HTS tape matrices, heavy-duty shock absorbers must disconnect the cryostat base from the substation structural frame. To defend against storm surges, key control electronics must be raised on structural concrete pylons high above the 500-year flood plain level.

- b. *Impact of Weather-Induced Fault Characteristics on FCL Response:* Weather-driven disturbances display different fault signatures that significantly affect FCL triggering and coordination dynamics. Lightning surges exhibit high-frequency, ultrafast transient overvoltage (1.2/50 μ s waveforms) with severe dv/dt and di/dt features. In SFCLs, these transients may produce local current densities above the critical current J_c , producing a partial, false quench even

during nonfault surges. Consequently, MOVs must be carefully synchronized in parallel with the FCL to skip lightning impulses without producing an undesired quench [167]. Conversely, wind-blown debris, fallen tree limbs, and conductor galloping frequently trigger intermittent, high-impedance evolving faults (HIFs) [168]. The ensuing borderline fault currents may lie dangerously near the FCL's triggering threshold, leading to chattering or partial quenching that produces severe, localized thermal hot spots. FCL control algorithms must consequently replace static overcurrent thresholds with adaptive time-frequency and wavelet transform algorithms to successfully discern between solid grid short-circuits and transient, weather-induced high-impedance anomalies. Finally, flood-induced ground faults result in solid, low-impedance SLG faults that frequently persist for lengthy periods owing to flood-damaged downstream CBs [169]. Under these protracted backup clearing circumstances, the FCL undergoes huge cumulative thermal-energy dissipation, stated as the following equation:

$$E_{\text{thermal}} = \int_0^{t_{\text{backup}}} i_{\text{fault}}^2(t) \cdot R_{\text{FCL}}(t) dt. \quad (45)$$

This necessitates an expanded thermal-capacity design—such as increasing the thickness of the copper/silver stabilizing layer on HTS tapes—to avoid irreversible device deterioration during delayed protection backup operations ($t_{\text{backup}} > 500$ ms).

These weather-induced fault types, lightning surge follow-through, wind-blown debris HIFs, and flood-related ground faults, illustrate several environmental conditions that may influence FCL performance and coordination. Incorporating such conditions into dedicated testing protocols and physical-hardening criteria could therefore provide a useful direction for future FCL deployment in climate-exposed grid environments.

5.3 | Technology Roadmap Across FCL Families

Superconducting FCLs (SFCLs). Future development should focus on improving 2G HTS conductor performance and reducing costs, while complementing cryogenic systems that are small, dependable, and low-maintenance. Long-term pilot demonstrations are necessary to measure reliability, failure modes, and operational processes. Solid-state and hybrid FCLs. Leveraging wide-bandgap devices (SiC and GaN) can reduce losses and footprint while enabling very fast response, making these alternatives suitable for converter-dominated networks and HVDC applications. Key issues include thermal robustness, fault energy handling, and synchronization with converter protection.

Saturated-core and other nonsuperconducting inductive designs. These remain intriguing due to their robustness and ease of operation. Research should focus on improving size/weight, magnetic materials, and performance assessment under inverter-shaped fault currents and weak grid circumstances.

Digital integration and adaptive operation. Across all families, integrating sensing, communication, and adaptive control can transform FCLs into smart-grid assets (dynamic setpoints,

coordinated restoration logic, and enhanced support for renewable FRT) without reducing protection assurance.

5.4 | Scenario-Technology Mapping

To provide a systematic outlook for smart and resilient power systems, Table 9 links representative emerging grid scenarios to the dominant requirements and candidate FCL technologies, together with the main open research issues. This scenario-driven mapping highlights that FCL selection is application-dependent and must be coordinated with protection and operational objectives.

From a resilience standpoint, FCLs are critical enablers of higher DER penetration and meshed grid operations without violating existing equipment short-circuit ratings. Consequently, they facilitate rapid restoration and minimize the impacts of outages following system disruptions. However, to fully exploit this potential in smart grids, future research must explicitly address the dynamic interactions among FCL devices, inverter control modes, microgrid islanding and resynchronization strategies, and HVDC protection philosophies. Achieving this synergy is paramount to maintaining both transient stability and protection selectivity across a wide spectrum of fault conditions and network reconfigurations.

As illustrated in Figure 15, the research trajectory concerning FCLs has evolved significantly over the past two decades. This historical bibliometric trend is presented exactly as reported by the authors of [30]. According to this data set, following an initial surge in interest (with a notable peak in 2005), publication volumes declined

noticeably around 2010 and 2012. This temporary plateau is likely attributable to technological bottlenecks, high implementation costs, and a lack of large-scale commercial deployments during that period. However, post-2012, the literature exhibits a robust resurgence that directly correlates with the aggressive global expansion of renewable energy, DG, and smart-grid infrastructure. The integration of these technologies introduced new fault dynamics and protection challenges, thereby catalyzing renewed academic and industrial interest in advanced FCL topologies. Specifically, the data set highlights renewed peaks in 2017 and 2019, contrasting with a temporary drop in 2018. Despite these year-over-year fluctuations, the overarching momentum of the past decade underscores that FCLs have transitioned from niche theoretical devices to essential components for enhancing grid reliability, managing dynamic fault currents, and enabling adaptive protection coordination in contemporary power networks.

5.5 | Practical Decision Framework and Recommendations for Practitioners and Policymakers

The technical, economic, and deployment evidence developed throughout this review can be consolidated into a single decision-support reference. Table 10 synthesizes the voltage-class guidance of Section 3.4, the scenario-technology mapping of Table 9, the sizing and coordination constraints of Sections 4.1 and 5.1, and the deployment maturity evidence of Table 6 into a quick reference guide for technology selection. Building on this synthesis, the following subsections separate the review's practical implications for two distinct audiences:

TABLE 9 | Scenario-driven mapping of FCL application potential in smart and resilient power systems.

Emerging scenario	Dominant system requirements (context)	Candidate FCL technologies (best-fit traits)	Main open research issues
DER-dense distribution feeders	Variable fault contributions, possible rise of prospective fault levels at substations/tie points; need low loss and preserved selectivity	Inductive/saturated-core at substations and tie-lines; selective SFCL at critical buses; hybrid for constrained nodes	Protection coordination (fuse-recloser-relay); placement/sizing under topology and DER uncertainty; impact on reclosing and selectivity
Microgrids (grid-connected/islanded)	Large mode-dependent changes in fault level and waveform; inverter-dominated faults in islanded mode; stability-sensitive	SFCL (fast limitation) where justified; inductive/saturated core for rugged operation; hybrid to balance speed and losses	Low-fault detection and adaptive protection; interaction with GFM controls; stability versus protection trade-offs
Resilient restoration and reconfiguration	Rapid sectionalizing and tie switching changes short-circuit levels; need “fault-level decoupling” during restoration with high availability	Inductive/saturated core at interties/corridors; configurable hybrid concepts	Co-optimization of restoration switching with FCL states/parameters; reliability, failure modes, and operational procedures
VSC-HVDC/MT-HVDC networks	Fast DC fault propagation and converter vulnerability; ultrafast limitation coordinated with DC protection	Solid-state and hybrid DC FCL concepts; selective non-SC solutions where cryogenics are impractical	Coordination with DC breakers and converter blocking; AC/DC interoperability; EMT-level validation; placement in meshed MT-HVDC grids

Abbreviations: AC, alternating current; DC, direct current; DER, distributed energy resource; EMT, electromagnetic transient; FCL, fault-current limiter; GFM, grid forming; HVDC, high-voltage direct current; MT-HVDC, multiterminal HVDC; SC, superconducting; SFCL, superconductor fault-current limiter; VSC, voltage source converter.

engineers directly responsible for FCL specification and coordination, and policymakers or standards bodies responsible for the regulatory and funding environment in which FCL technologies mature.

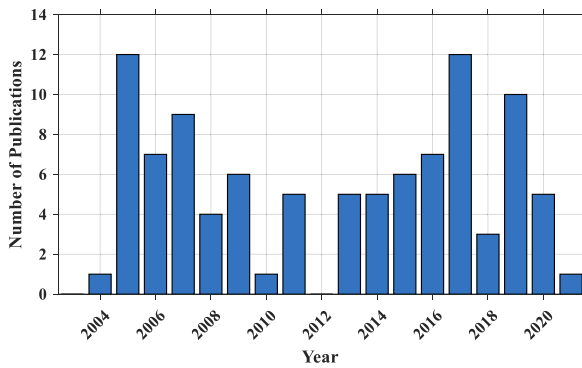


FIGURE 15 | Research publication trend on fault-current limiters. Data reproduced from [30].

TABLE 10 | Quick-reference technology selection guide, consolidating the voltage-class, speed, coordination, maturity, and scenario-based selection criteria developed throughout Sections 3–5.

Selection criterion	Grid condition	Recommended FCL family	Supporting evidence
System voltage class	HV transmission (12–500 kV), critical substation nodes	SFCL (saturated iron core preferred)	Highest current rating (up to 10 kA), lowest steady-state losses (Table 4 and Section 3.4)
System voltage class	MV distribution feeders (≤ 20 kV), converter-dominated	SSFCL	Generally, more compact and comparatively lower in upfront cost (USD 50k–500k); accepts moderate reliability/harmonics trade-off (Sections 3.4 and 5.2)
System voltage class	MV networks and HVDC links requiring balanced loss/speed	HFCL	Combines SC low losses with PE fast response; dual maintenance cost (Section 3.4)
Response-speed requirement	Submillisecond suppression (VSC-HVDC/MMC arm protection)	SSFCL or HFCL are more likely to satisfy this requirement under the stated benchmark assumptions.	SFCL response (2.5–10 ms) exceeds IGBT thermal-withstand window $t_{\text{block}} \leq 2.5$ ms (Section 5.1)
Fault-current headroom	Risk of fuse-recloser protection blinding	Any family, sized per Equation (26)	Requires $I_{\text{FCL}} > I_{\text{fuse-min}} = K \cdot I_{\text{rated}}$ (Section 4.1)
Deployment maturity	Long-duration field reliability required	Saturated iron-core SFCL (TRL 8–9)	Among the subtypes reviewed, the saturated iron-core SFCL has the most established long-duration field-demonstration record.(Table 2, Table 6)
Grid scenario	DER-dense distribution feeders	Inductive/saturated-core at substations and tie-lines; selective SFCL at critical buses	Table 9
	Microgrids (grid-connected/islanded)	SFCL where justified; hybrid for balanced speed/loss	
	Resilient restoration/reconfiguration	Inductive/saturated-core at interties and corridors	
	VSC-HVDC/MT-HVDC networks	Solid-state and hybrid DC FCL concepts	

Abbreviations: DC, direct current; DER, distributed energy resource; FCL, fault-current limiter; HFCL, hybrid FCL; HV, high voltage; HVDC, high-voltage direct current; MMC, modular multilevel converter; MT-HVDC, multiterminal HVDC; MV, medium voltage; SC, superconducting; SFCL, superconductor fault-current limiter; SSFCL, solid-state FCL; VSC, voltage source converter.

5.5.1 | Recommendations for Practitioners

Building on Table 10, the following actions are recommended for protection and utility engineers specifying, sizing, or coordinating FCL installations:

1. Use system voltage class and available fault-current headroom as the first screening criterion, applying the family-level guidance of Table 10 and the detailed voltage-level discussion of Section 3.4.
2. Re-run relay coordination studies after any FCL insertion, accounting for the apparent-impedance shift $Z_{\text{app}} = Z_{\text{line}} + Z_{\text{FCL}}$ derived in Section 4.1, to avoid distance-relay underreach.
3. Verify FCL sizing against the fuse-coordination lower bound of Equation (26) to prevent protection blinding in fuse-recloser schemes.
4. For MMC-based HVDC applications, select FCL placement (DC-side, arm, or AC-side) according to the fault-stage

requirements identified in Section 5.1, using Equation (36) as the DC-side sizing benchmark.

5. Apply the NPV framework of Equation (42), together with the CAPEX/OPEX figures compiled in Section 5.2, as the standard basis for economic justification rather than qualitative cost comparison alone.

5.5.2 | Recommendations for Policymakers and Standards Bodies

The following priorities are recommended for regulators, standards organizations, and funding agencies:

1. Develop standardized, weather- and DER-aware FCL benchmarking and testing protocols, addressing the “weather resilience envelope” gap identified in Section 5.1.
2. Mandate standardized techno-economic (CAPEX/OPEX) reporting for FCL installations, addressing the absence of comparable cost data identified in Section 5.2.
3. Update grid interconnection codes to formally incorporate FCL-aware adaptive relay coordination under IEC 61850, consistent with the communication-latency and cybersecurity requirements detailed in Section 4.2.
4. Prioritize funding for demonstration-to-commercial deployment pathways: the project inventory in Table 6 shows that most reported FCL installations remain at prototype or pilot scale, indicating that suggesting that limited deployment experience remains a major barrier to wider adoption, alongside device-level and system-integration considerations.

6 | Conclusion

With an emphasis on their function in allowing resilient and converter-dominated grids, this article provided a thorough and system-oriented assessment of FCL technologies for contemporary power systems. The operating principles, performance characteristics, and integration issues of superconducting, solid-state, and hybrid FCLs were critically examined from both device-level and system-level viewpoints.

FCL selection is intrinsically application-dependent, as the comparative study demonstrates. Although there are issues with cost, footprint, and cryogenic requirements, SFCLs have excellent current-limiting capability with low steady-state losses, making them appropriate for HV critical nodes. For HVDC and converter-dominated systems, SSFCLs offer ultrafast and adjustable fault-current restriction, but at the cost of increased losses and system complexity. Although their integration introduces new design and coordination challenges, HFCLs offer a balanced approach by combining the benefits of both technologies.

Large-scale deployment is hampered by several issues despite notable advancements, such as the limited availability of standardized benchmarking techniques, a lack of long-term field validation, as reflected in the predominantly prototype- and pilot-scale nature of the demonstration projects summarized in Table 6, and inadequate interaction with adaptive protection and control frameworks. Furthermore, rather than focusing on

whole-system-level effects under dynamic operating conditions, most current research focuses on isolated device performance.

Building on the decision framework and stakeholder-specific recommendations synthesized in Section 5.5 (Table 10), three priorities are especially critical for translating device-level FCL innovation into deployed grid assets: standardized, weather- and DER-aware benchmarking protocols; techno-economic reporting standards that make the CAPEX/OPEX figures compiled in Section 5.2 directly comparable across vendors and projects; and grid-code updates that formally incorporate FCL-aware adaptive relay coordination (Sections 4.1 and 4.2) into interconnection standards.

All things considered, FCL technologies are a major facilitator of improving protection coordination, boosting system resilience, and expanding the use of renewable energy. Coordinated, multidisciplinary research and extensive demonstration efforts will be necessary to close the gap between device innovation and system-level implementation to ensure the successful integration of these devices into future power systems.

Author Contributions

Abdelrahman Farghly: writing – original draft, methodology. **Eslam Essam:** methodology, visualization. **Hilmy Awad:** investigation. **Samia Abdelfatah:** validation. **Walid Issa:** funding acquisition, resources. **Abdallah M. Hamada:** resources, project administration.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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