Journey towards CdTe-based Graded Band Gap Electrodeposited Solar Cells on P-type Window

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Declaration

I hereby declare that:

1. I have not been enrolled for another award of the University, or other academic or professional organisation, whilst undertaking my research degree.

2. None of the material contained in the thesis has been used in any other submission for an academic award.

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Dedication

Abdul Hamid Howlader, a peasant whose forefathers inhabited the largest mangrove forest on earth; and

Fazlar Rahman Miya, a victim of forceful migration during the Bengal-partition.

To the lives of the two grandfathers of mine; the giants, standing on whose shoulders I see further.

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This thesis is an outcome of a long and determined personal journey. But this journey was encouraged, supported, cheered, and sometimes even pushed forward by an army of friends, colleagues, family members, and mentors. Whoever I have become today as a human being, I owe it to my parents, especially my mother, the person who shaped every bit of my thoughts and morale. Hence, let this manuscript be the opportunity for me to say out loud for the first time in my life that- “I love you, Ammu”. I would also love to thank all my other family members in Bangladesh for their supports and well-wishes from five thousand miles away. Thanks to my high school teachers, specially Shahidullah Sir and Sabur Sir for instilling goodwill for people in me.

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List of publications

Journal Articles

1. **A. E. Alam**, O. I. Olusola, D. A. Loch, K. Shukla, W. M. Cranton, I. M. Dharmadasa, "Electrodeposited ternary compounds for novel PV application: Optimisation of electrodeposited CdMnTe thin-films as p-type window layer", Nature Scientific Reports, DOI: 10.1038/s41598-020-78066-y

2. I. M. Dharmadasa, **A. E. Alam,** A. A. Ojo and O. K. Echendu**,** "Scientific complications and controversies noted in the field of CdS/CdTe thin film solar cells and the way forward for further development", JMSE, DOI: 0.1007/s10854-019-02422-6

3. I. M. Dharmadasa, Y. Rahaq, and **A. E. Alam,** "Perovskite solar cells: short lifetime and hysteresis behaviour of current–voltage characteristics", JMSE, DOI: 10.1007/s10854-019-01759-2

4. **A. E. Alam**, W. M. Cranton, and I. M. Dharmadasa, ''Electrodeposition of CdS thin-films grown from Cadmium acetate and Ammonium thiosulfate precursor", JMSE, DOI: 10.1007/s10854-019-00750-1

5. **A. E. Alam**, A. A. Ojo, J. B. Jasinski and I. M. Dharmadasa, "*Magnesium incorporation in n-CdTe to produce wide bandgap p-type CdTe:Mg window layers*", ChemEngineering, DOI: 10.3390/chemengineering2040059

Conferences

1. **A. E. Alam**, A. A. Ojo, J. B. Jasinski and I. M. Dharmadasa, "Development of next-generation electrodeposited solar cells with p -type window layer", ICESF 2019

2. **A. E. Alam**, A. A. Ojo and I. M. Dharmadasa, "Development of next-generation electrodeposited solar cells with p -type window layer", PVSAT-15, DOI: 10.13140/RG.2.2.17820.74881

3. **A. E. Alam**, A. A. Ojo and I. M. Dharmadasa, “Magnesium incorporation in n-CdTe to produce wide bandgap p-type CdTe:Mg window layers”, UK Semiconductor 2018

Manuscripts awaiting submission

1. I. M. Dharmadasa and **A. E. Alam, “**Critical analysis of the recently reported 19% efficient CdSe/CdTe solar cell fabricated using thermal evaporation.”
2. I. M. Dharmadasa, **A. E. Alam** and Xu Xu, “Transforming Lives of Needy Communities Using Solar Village Projects: A Sri-Lankan Experience”

Abstract

Photovoltaic (PV) technology being the world's most utilised renewable source of energy copes with many challenges technically and socially. Cadmium Telluride (CdTe)-based thin-film PVs are the most commercially successful solar cells that hold potential to develop further. This work proposes a novel device structure for CdTe-based solar cells which is implementable using electrodeposition, an easy and affordable fabrication technique for the developing world. Inclusion of a wide band gap p-type semiconductor as a window layer of a graded band gap device and use of suitable back diffusion barrier layers to mitigate thermionic back diffusion, have been proposed to potentially improve the open circuit voltage (V_{oc}) of the cells. This concept has been tested and verified with GaAs and Perovskite based solar cells, but this work aims to investigate the concept for CdTe-based devices grown with inexpensive electrodeposition technique for the first time. In the material selection phase of this work, firstly, CdTe:Mg, CdMnTe and ZnTe layers are electrodeposited on glass/FTO surface, characterised, optimised and compared to be the p-type wide band gap window layer. ZnTe layers have been grown both in n-type and p-type with reasonably good crystallinity and selected as the window material for the device. Secondly, CdTe layers have been electrodeposited from cheap, low purity cadmium precursors, characterised and growth conditions were optimised to be used as the absorber layer of the cell. Thirdly, CdS thin films have been electrochemically grown, characterised, optimised and compared with n-ZnTe layers to be used as the hole back-diffusion barrier (hbdb) layer at the back of the device. Considering the ease of production, n-ZnTe has been selected as the n-type hbdb layer for the device. Following the selection of materials and finding their optimal growth parameters, firstly, ZnTe/CdTe based devices are fabricated employing the conventional n-window approach having an architecture of glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au. Growth parameters of the materials used in individual layers have been optimised in the material selection phase. These devices exhibited 3.63% of highest efficiency with V_{oc}, J_{sc} and Fill-factor of 430 mV, 30.2 $mAcm^{-2}$ and 0.28 respectively. Finally, according to the conceptualised novel device design, p-window based glass/FTO/p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe/In architecture has been fabricated producing highest efficiency of 5.41% with V_{oc}, J_{sc} and fill-factor of 560 mV, 33.3 $mAcm^{-2}$ and 0.28 respectively. Despite having concerns about the material quality of the layers, experiments have shown that p-window based graded band gap CdTe solar cells exhibit greater Voc, hence better performance compared to their n-window counterpart.

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Chapter 1

Introduction

1.1 Personal motivation

It is repetitive to say that over-dependence on fossil fuels to meet the energy needs of the global civilisation will almost certainly end up in a catastrophe [1], [2]. This upheaval is not even a far-fetched reality, this devastation has already started coming into being since a long time now. In fact, way before the recently popularised catch phrases like climate emergency, extinction rebellion, etc. have been introduced, fossil-fuel dependency had hurt the social, economic, and political fabric of many human societies. It is widely believed by many historians that the infamous Pearl Harbour attack which officially brought the US into the second world war, was partly carried out as a desperate measure of Japan due to their declining oil reserves [3], [4]. Around the globe, conflicts and violence have noticeably been sparked relating to the presence, absence or distribution of fossil fuels and their transportation routes [5]. Even for post-conflict regions, political stability has been greatly affected due to the energy situation of the region [6]. The author, as a Bengali national, belonging to a nation that has sustained an immense post-genocide energy predicament [7], [8], has always personally felt that the ever-growing threat of energy deficit should be dealt not as a mere infrastructural mission, but with a much greater social-political goodwill and vision too.

Bangladesh has long been one of the countries with the world's lowest per capita energy consumption [9]. Research suggests that up to 2010, the energy crisis in Bangladesh was largely due to the country's over-dependence (~80%) on limited natural Gas (projected to finish by 2030 if burnt at current rate) as a fuel, and because of the geo-social restraints of the over-populated fertile agricultural land area remaining an obstacle to large-scale coal mining for energy generation [8], [10]–[13]. This has hurt the country with a loss of 0.5% in annual GDP even a few years back [14]. From then onward, the country had taken a firm effort to fight back by rapid electrification projects, and has managed to maintain one of the highest annual GDP growth rates globally [15], [16]. But like most other quick successes, this also came at a cost. In order to swiftly bring together the energy sector, the country relied on short-term, imported-petroleum based, grid connected, private-public ventures called quick rental power plant (QRPP) companies, producing up to 50% of the national generation [17]. This, on one hand, created some ethical issues such as corruption, but more worryingly created certain environmental issues. As research

suggested, oil-based power plants have higher global warming emissions than that of natural gas [18], [19]. Moreover, despite the fact that QRPP is a temporary solution, it has also been observed that the overall air pollution of the country has already become unprecedentedly high during this period, landing the country in the top 5 countries having the highest air pollution in the world according to the WHO [20], [21].

Therefore, it is extremely necessary that the country comes up with more sustainable plans of energy generation to sustain the environment as well as the current economic growth. Hence, alongside initiating nuclear power generation, back in 2008 the government has taken steps to implement a National Renewable Energy road map to break this trend [13]. According to that policy, by the end of 2021 the country aimed to gain the capacity of generating at least 2400 MW of power from renewable sources, growing from just 55 MW generation in 2011 [22]–[24]. The prospect of wind power (present total installed capacity is 2 MW), bio-energy (present installed capacity 1 MW) or new hydro-power, have been limited in Bangladesh and therefore, growth of renewable energy in a tropical sun-belt country like Bangladesh has naturally relied primarily on solar power [22]. But to date, the current installed capacity that Bangladesh has for solar power is only 488 MW, with a maximum probable capacity of 1681 MW approved for installation [25], [26]. Under this circumstance, it seems impractical to assume that the projected capacity is achievable by the anticipated timeline.

Despite having a huge necessity, natural potential and government initiatives, the reasons why the solar sector of the country is struggling to implement the plans have been discussed over time. The government has recently drafted a National Solar Energy Action Plan 2021-2041 to utilise solar energy better in contributing to the national energy need. It is anticipated that a major reason has been the lack of technical capacity building opportunities for solar energy [12] [26]. Hence there have been agendas taken to attract initiatives from both public and private sectors for the local capacity development in terms of R&D, infrastructure building, project preparations and for testing, labelling and standardisation of equipment [24] [26]. Moreover, another major issue affecting the solar sector of Bangladesh is the import-based model of business. Though some local initiatives are taken to assemble a little amount of PV modules within the country, but 100% of the PV cells are imported from various counties, majorly from China and India [27]. It is also argued that the module quality has impacted the solar output in a large scale, compared to the high price it claimed [12], [28]. This problem itself has hampered a durable

financial model for the photovoltaic sector of the country. Researchers from Bangladesh Atomic Energy Commission (BAEC) have claimed that, given the adequate technical capacity is there, fabrication of large scale solar cells in the country can reduce the cost of modules by more than 30% [27]. This assumption has been made for commercial multi-crystalline Silicon solar cell production and can vary based on the material and fabrication technique involved.

The author of this thesis feels strongly to comply with both the findings that technical capacity building is key and that the development of low-cost solar cell fabrication technique for commercial production in lower-middle income countries like Bangladesh, hold immense importance to sustain the renewable energy sector with a sustainable outlook.

1.2 Technical Motivation

When it comes to industrial production of Photovoltaic (PV) cells, the most conventional and industrially matured PV material is crystalline Silicon (c-Si). The latest updates (2020) by the National Renewable Energy Lab (NREL), as depicted in figure 1.1, shows that the Power conversion efficiency (PCE) of standard to large commercial modules of c-Si increased to 24.4% for modules from Kaneka Corporation, Japan. However, the other materials that have successfully achieved regular to large commercial modules are thin-film based materials, namely copper indium gallium selenide (CIGS), amorphous silicon (a-Si) and cadmium telluride (CdTe). Amongst these, CdTe is the only material that has demonstrated a steady growth in module efficiency, reaching 19% by First Solar, USA in 2020 [29].

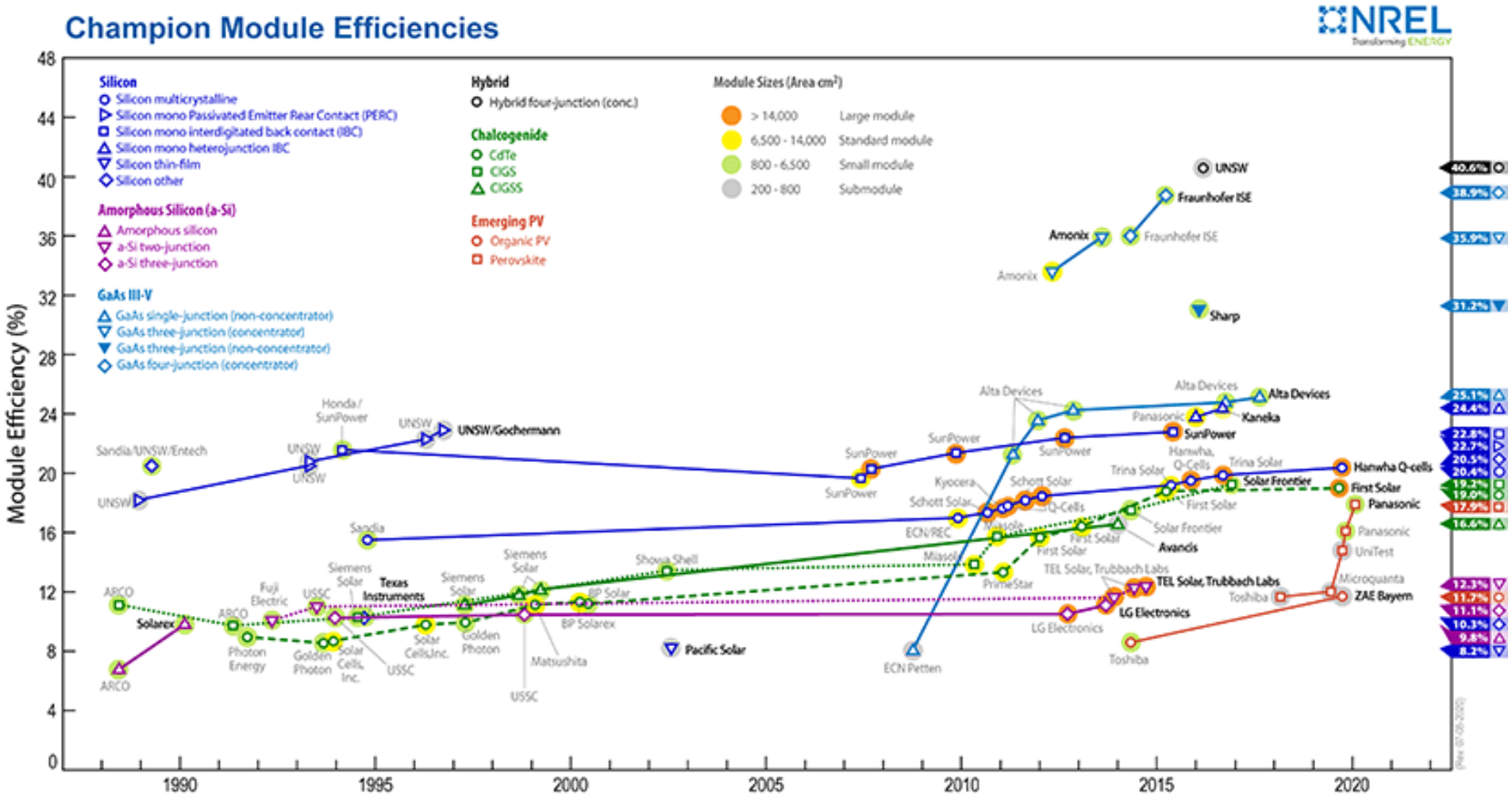

Fig 1.1 Champion Photovoltaic Module Efficiency Chart from 1984 to 2020 [29]

Nevertheless, module efficiency is not the only point of concern here. Commercial success of the material and method should be evaluated by the price of the module per watt. Figure 1.2 presents a price comparison amongst the major players in the standard PV module market. This illustrates that according to the latest update, CdTe-based standard solar modules are the cheapest per wattage ($0.255/Watt) of power generation. The price of the modules has been standardised according to the currency rate of USD in 2019. The closest competitor in this regard is c-Si based solar modules with module price of $0.280/Watt. It has been anticipated that between 2030 to 2040 the cost of c-Si based solar modules may come down to $0.240/Watt, whereas CdTe-based solar modules anticipate an even more dramatic price drop to $0.144/Watt by just 2024 [31-32]. Hence, it can be stated that despite having slightly lower module efficiency record, CdTe-based PV modules offer the greater financial success for mass production.

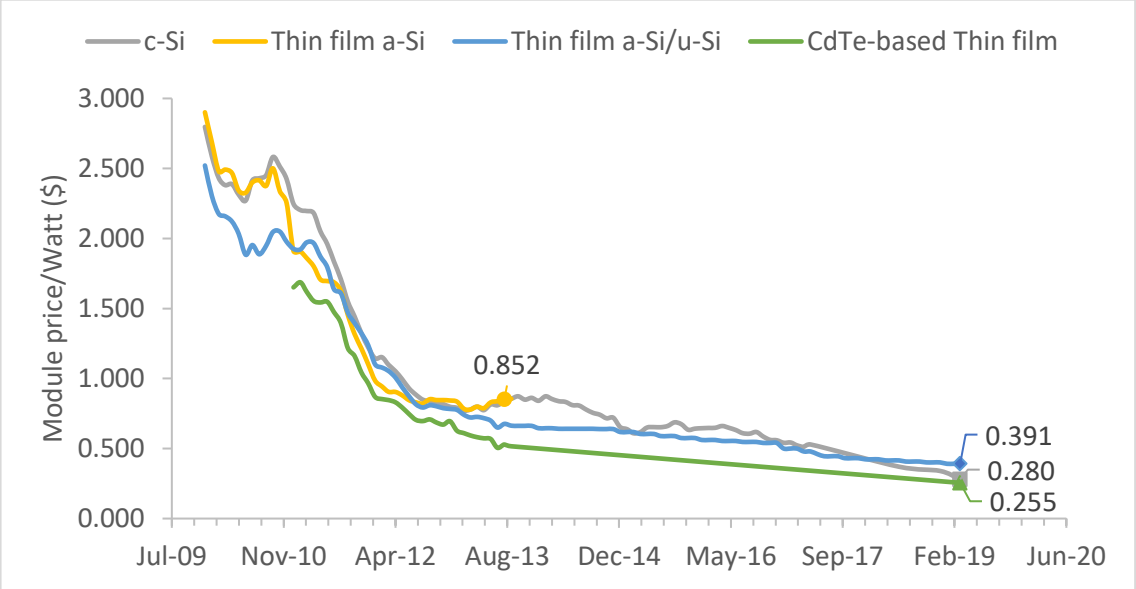

Fig. 1.2 Decade-long global average selling price trend of various PV modules [30], [31], [32]

Moreover, in 2017 Louwen et al. also argued that in comparison to all other established PV modules, CdTe-based modules have the lowest Energy Payback Time (EPBT). EPBT is a parameter affected by the solar irradiance on the geographic location, the existing energy mix of the locality and the maturity of the technology, but CdTe-based modules showed lowest EPBT regardless. A similar scenario has been observed also for Green House Gas (GHG) emission per kWh by different types of PV modules. The model showed lowest GHG emission (gCO_2-eq/kWh) during manufacturing by the CdTe-based modules [33]. These observations are very much in agreement with the previous life cycle

studies conducted by Leccisi et al., Peng et al. and Fthenakis et al. in 2016, 2013 and 2012 respectively [34]–[36]. Therefore, it is quite clear that in terms of environmental impacts CdTe-based solar modules are evidently safer than the other materials and technologies.

However, with regard to selecting the correct material for PV manufacturing, along with the price, efficiency and environmental aspects, health & safety (H&S) concerns are of paramount importance too. This is especially the case when a heavy metal such as Cadmium (Cd) is involved. Cd is produced as a biproduct of Zinc (Zn) mining [37]. Incorporation of Cd into any compound can be and should rightfully be a point of concern, because elemental Cd is a lung carcinogen and has long-term detrimental effects on kidney and bone due to high aquatic toxicity [38]. Although most recent toxicological data shows that the CdTe compound unlike elemental Cd is not water soluble and possesses less toxicity, it may still stay as a point of H&S concern because even if the encapsulated CdTe-modules themselves do not become the source of Cd toxicity, the industrial process of CdTe solar module manufacturing can release Cd waste into the environment [37], [39]. It is worth mentioning that the Bangladeshi population are already exposed to excessively high levels of Cd in their diet due to the elevated Cd concentrations in rice caused by Cd toxicity of agricultural land. Moreover, aquatic life is also getting jeopardised since studies found Cd presence higher than the national limit in rivers surrounding the capital and port cities. The main sources of Cd pollution in Bangladesh are industrial wastes from fabric pigments, pharmaceuticals and battery industries [40]. Lack of any viable recycling policy for Cd waste and absence of awareness regarding feasible utilisation of Cd wastes is hurting the greater public health. Therefore, for lower middle income or developing countries like Bangladesh, a trade-off between whether to allow the ongoing Cd pollution without intervention or to allow the probable and containable risk of Cd toxicity by PV manufacturing, can be a viable way to deal with the undesirable Cd waste. In fact, historical evidence shows health effects from Cd exposure such as “itai-itai disease” in Japan was caused by Cd in Zn mining waste that was discharged into the environment as opposed to being used in products [37].

Hence, it can be said that, to comply with Bangladesh government’s solar energy action plan 2020-2040, the most suitable solar energy material in terms of financial, environmental, and public health aspects that can be considered for commercial manufacturing and studied for further development is CdTe.

1.3 State of the art

CdTe based thin-film photovoltaic (PV) cells are currently leading the thin-film PV market. Though First Solar-USA is in the commercial forefront with 18.7% module efficiency at present, the first ever commercial manufacturing of CdTe-based solar cells was successfully executed by British Petroleum (BP) in 2001 with their 10.6% efficient ~1 m^2 solar modules [41], [42]. Since, for the manufacturing of their solar cells, First Solar-USA uses Vapour Transport Deposition (VTD) which evolved from the Close Space Sublimation (CSS) technique, CSS has become the leading fabrication method worldwide and a vast amount of research emphasis has been given on cells based on this technique [43]. Apart from CSS, other growth techniques used for CdTe-based solar cell fabrication such as Chemical vapour deposition (CVD), Sputtering, Molecular beam epitaxy (MBE) etc have also been experimentally explored, however, the only other technique that could be commercially implemented for large scale CdTe-based solar cells was BP's Electrochemical deposition (ED) [43]–[46]. The untimely exit of BP from their CdTe-based solar project around 2002 and later their complete termination of the solar venture in 2011 slowed down the development of this excellent technique. Yet, electrodeposition is still one of the only two commercially successful fabrication techniques for thin-film solar panels and requires very economical manufacturing set-up compared to the others [47]. As a matter of fact, considering the simplicity of the set-up, deposition process continuity, doping simplicity, self-purification capability, scalability, manufacturability, economic viability, likelihood of Cd-containing waste reduction and necessity of comparatively less number of production lines, electrodeposition is the most suitable fabrication technique that can be feasibly executed in the developing world [48]–[53].

Currently, the Solar energy research group, at Sheffield Hallam University (SHU) holds the record of highest cell efficiency for CdTe-based electrodeposited PV, where a graded bandgap structure has been implemented to fabricate the devices [54]. Graded bandgap (GBG) multi-layered solar cells are highly promising in designing the next generation solar devices. It has been conceptualised that GBG devices can be constructed on the basis of two approaches in terms of the electronic conduction type of the window material: (i) fabricated on n-type window and (ii) fabricated on p-type window. Though the current highest efficiency for electrodeposited CdTe-based GBG solar cells are

achieved from n-window devices, cells fabricated on p-type windows have a potential to achieve higher performance due to the possibility of producing higher open circuit voltage (V_{oc}) resulted from a higher potential barrier [55], [56]. This has been experimentally demonstrated by achieving $V_{oc} \approx 1.17$ V with GaAs/AlGaAs and $V_{oc} \approx 1.00$ V with Perovskite based solar cells [57], [58].

1.4 Project aims and objectives

A major challenge in the field of CdTe thin-film solar devices is the low open circuit voltage (V_{oc}) of these devices. In fact, low V_{oc} is considered a common issue for almost all types of solar devices. It is considered a challenge to achieve a V_{oc} nearing 1V for poly-crystalline CdTe based thin-film solar devices. Hence, this work has proposed a novel device model that can potentially exceed this 1V barrier. This model can also be implemented for organic-inorganic hybrid or inorganic-perovskite hybrid solar devices too. The proposed device architecture and work presented in this thesis has now been published, suitable materials have been explored, synthesised, and characterised and devices have been fabricated to materialise the concept. The work in this project aims to achieve a device structure for CdTe-based low-cost ED solar cells that is based on the p-window approach. A prospective device has been presented in Figure 1.3 below.

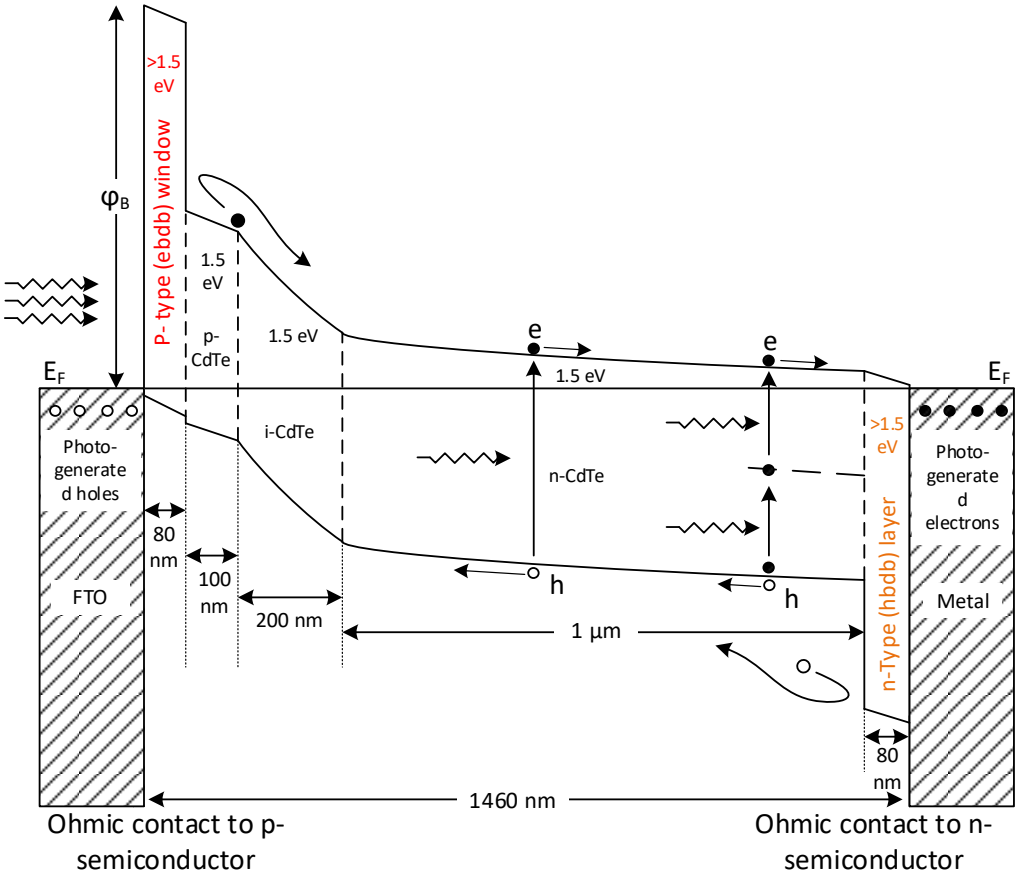

Fig 1.3 Energy band diagram drawn to scale for a short-circuited multi-layer solar cell based on p-type window material (p^+-p-i-n-n^+ structure). p^+ and n^+ layers act as electron back diffusion barrier (ebdb) layer (or Hole Transport Layer- HTL), and hole back diffusion barrier (hbdb) layer (or Electron Transport Layer- ETL) respectively.

In order to implement this conceptual solar device, the primary task is to search for a suitable p-type semiconductor material that can be electrodeposited having a bandgap higher than that of the absorber material, which in this case is >1.45 eV of CdTe. Moreover, for the best outcome of the device it is also vital that the material has a reasonable crystallinity along with low or no intermediate defect levels present within the bandgap range for better carrier transport and accurate Fermi level positioning, respectively. Hence for the search and identification of the suitable materials to be used as the material layers and for the fabrication of the devices according to the concept above, this research work has majorly worked on the following four objectives:

1. Growth and characterisation of potential wide bandgap p-type window layer that will also perform as the electron back diffusion barrier (ebdb) layer. In search of the suitable material, carrying out growth and characterisation of ternary compounds such

as CdTe:Mg and CdMnTe, as well as a binary compound like ZnTe. Optimising the growth parameters such as material composition, growth voltage (Vg), bath temperature, pH, stirring rate etc of the chosen window layer for device fabrication.

2. Growing and characterising the main absorber material, cadmium telluride (CdTe) and optimising the growth parameters for the bath. Using cadmium nitrate, $Cd(NO_3)_2$ as the Cd precursor, since that has been proved to be showing the best material quality from the previous works within the group.
3. Growth and characterisation of potential wide bandgap n-type back layer that will also perform as the hole back diffusion barrier (hbdb) layer. In search of the suitable material, carrying out growth and characterisation of CdS, CdSe and ZnTe. Optimising the growth parameters such as material composition, growth voltage (V_g), bath temperature, pH, stirring rate etc of the chosen hbdb layer for device fabrication.
4. Fabrication of PV devices by combining the chosen materials and available fabrication techniques within the group, and their assessment using current-voltage (I-V) and capacitance-voltage (C-V) techniques to evaluate device properties.

1.5 Thesis outline

As per the aims discussed and objectives set above there had been a detailed Gantt chart maintained and updated throughout the whole project lifetime. The thesis outline is as follows:

Chapter 1 This chapter briefly describes the author's motivation to take up this research, is focused on related state of the art research activities, the author's aims and objectives and, how the project has been planned to achieve those aims.

Chapter 2 This chapter presents the related literature review describing all the theoretical backgrounds and technical bases of the research. This includes an explanation of the physics behind graded band gap (GBG) solar cells and what are the issues that need careful attention to avoid the typical complications and controversies exist in the field of CdTe-based PV research.

Chapter 3 In this chapter, all the relevant methodologies employed in this research are discussed and described. Beginning from the different thin-film fabrication techniques used in this work, all the analytical techniques, measurement methodologies and instruments are presented along with their working principles. The range of material

characterisation techniques as well as device characterisation techniques used are discussed with interactive graphical representation. This chapter aims to present the contents in a way so that it helps readers from different knowledge levels to relate to it.

Chapter 4 From this chapter onward, the experimental details along with the achieved results are discussed and analysed. This chapter presents the experiments and findings attained for the objective 01 of the section 1.4 above. In this chapter the author discusses the material properties of the possible p-type wide bandgap window layers and presents arguments for deciding the most suitable layer to be used for the expected device architecture. For ease of the readers, this chapter has been divided into 3 major portions namely 4.2, 4.3 and 4.4 focusing on different materials.

Chapter 5 In this chapter, the experimental details, results and relevant discussions are presented for the CdTe absorber layer material. This chapter presents the experiments and findings attained for the objective 02 of the section 1.4 above.

Chapter 6 This chapter presents the experiments and findings attained for the objective 03 of the section 1.4 above. A description of the electrodeposition process for the possible candidates for hole back diffusion barrier (hbdb) layers is provided. This chapter describes the characterisation details of the different material layers selected and nominated for the final layer that was used for the final device fabrication.

Chapter 7 This chapter presents the fabricated device parameters along with the discussions about the possible working principle of the devices. A description of the device performances is provided in this chapter with an aim to clarify the pros and cons of different approaches taken in this research project. This chapter corresponds to the final objective mentioned in section 1.4

Chapter 8 This is the concluding chapter of this thesis. It presents a summary of the overall project workflow, the major findings, along with a description of and the challenges encountered by the author in order to help the readers to draw their individual decisions about the whole project. This chapter is also of enormous importance because it discusses the possibilities for future research on this topic as well as further possible developments in the application front of solar energy to society.

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Chapter 2

Concept of Photovoltaics

2.1 Band structure of solids

In an effort to explain the behaviour of molecules in ideal gases, back in the 1860's the physicist James Clark Maxwell came up with the idea of a distribution statistics, that being further improved by Ludwig Boltzmann was termed as the Maxwell-Boltzmann (M-B) statistics around 1870's [1], [2]. The distribution mechanism implied that, with the gradual decrement of the temperature, at absolute zero all the molecules of a gaseous medium will settle to a single kinetic state. More than half a decade later, when the idea of electron already had been postulated, the Austrian physicist Wolfgang Pauli, while explaining the behaviour of electrons, came up with his famous 'exclusion principle' in 1925, which formulated that no two electrons can stay in the same physical-quantum state [3]. Hence due to this newly discovered limitation, the Maxwell-Boltzmann distribution could no longer explain the behaviour of electron gases and was unable to explain solid state materials.

In 1926, the physicists Enrico Fermi and Paul Dirac independently proposed that, instead of settling to a common state as per M-B statistics, electrons will occupy separate quantum states below a certain energy level called Fermi level at absolute zero temperature to abide by the Pauli's exclusion principle [4], [5]. The Fermi level suggested the idea that- above this level, the probability of finding an electron increases with temperature increment; below this level, the probability of finding an electron decreases with temperature increment and at this level, the probability of finding an electron is always half (1/2) regardless of the temperature. This distribution statistics proposed by the duo is termed as the Fermi-Dirac (F-D) distribution statistics.

F-D distribution can very well explain the electron distribution for solid state materials because temperature decrement implies low inter-atomic distance, which is a key characteristic for all solid-state materials. For solid materials at low temperature, while the atomic distance is very low, the interatomic energy-levels are supposed to overlap on each other as per M-B statistics. But to abide by Pauli's exclusion principle, they do not overlap, rather create bands of different energies to accommodate all the proximate energy-levels with slight separations.

Therefore, the outermost band created in a solid material by the outermost interatomic shells, is defined as the 'valence band (VB)' where the probability of finding an electron is the highest (1). In order to have conduction of electric current flow, the electrons bound to this valence band need to be elevated from the highest band edge (E_v) to a virtual upper energy band-edge separated by an energy distance, called the bandgap (E_g). This upper band which allows the electric conduction is called the 'conduction band (CB)', where the probability of finding an electron is the lowest (0) at low temperature, since no electrons will be there until they are energised to break free from the valence band and reach the lowest edge of conduction band (E_c). Now, in semiconductors, the virtual energy level where the probability of finding an electron will be half (1/2), resides exactly between the E_v and E_c levels and is termed as the Fermi level (E_F) as per the F-D statistics mentioned above.

In terms of electrical conduction, solid-state materials can be of mainly three types- conductors, insulators and semiconductors. Conductors are the materials which conduct electricity under any circumstances, provided a potential difference exists. Solid state conductors are majorly metals. Though some non-metals can also be showing conductive properties, conductivity can also be due to ions. As per band theory, in the band structure of conductors, valence band edge (E_v) and the conduction band edge (E_c) overlap each other leaving no bandgap. Insulators are the materials which do not conduct any electricity regardless of the provided potential difference across them. According to band theory, insulators have such a high bandgap that can never be overcome irrespective of the provided energy to the valence electrons, except through a process of breakdown.

The most interesting and investigated solid-state materials are semi-conductors. Intrinsic (pure) semi-conductors behave like insulators at low temperature, whereas at higher temperature or in the presence of light they may behave like conductors. Therefore, band formation in the semiconductors is in a manner that the bandgap is higher than zero and lower than that of insulators. Quantification of the bandgap energy has revealed that typical bandgap of semiconductors ranges between ~0.3-4.0 eV, where conductors have no bandgap and insulators have bandgap of >4.0 eV typically [6–8]. Solids with bandgap ≤0.3 eV are classified as narrow-bandgap semiconductors.

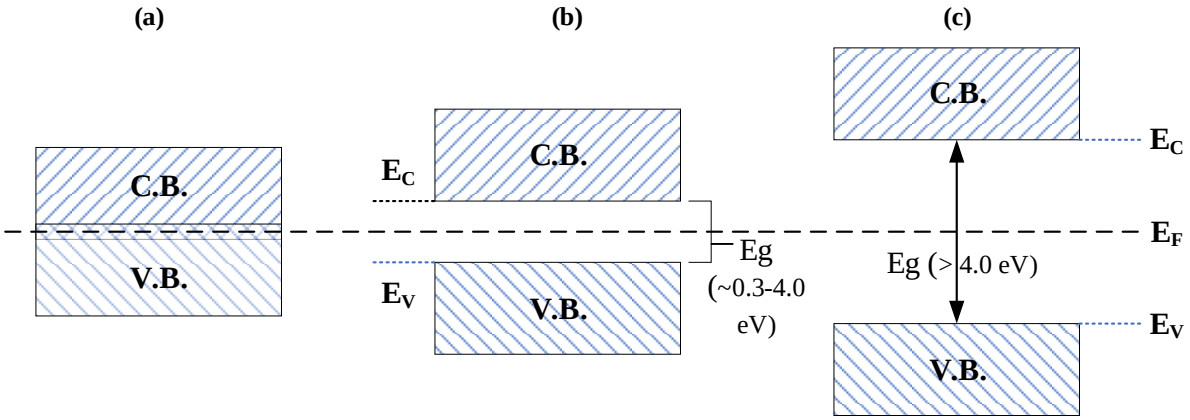


Fig 2.1 Energy band-diagram of **(a)** conductors, **(b)** semiconductors and **(c)** insulators

2.1.1 Idea of semiconductor doping

Semiconductor materials utilised in electronic applications are mostly crystalline or polycrystalline solids [9]. The elemental composition within the crystal structure can be changed by incorporating impurities or dopants. This process is called doping. Doped semiconductor materials are called extrinsic semiconductors where, undoped semiconductors are known as intrinsic (i-type) semiconductors. As per the figure 2.2, a typical i-type semiconductor structure consisting of four valence electrons (fig 2.2a) can either be doped p-type by incorporating impurities/dopants having lesser number of valence electrons to the crystal structure (fig 2.2b) or can be doped n-type by incorporating impurities/dopants having more valence electrons to the crystal structure (fig 2.2c). Therefore, p-type doping creates a 'vacancy of electron' (hole) in the crystal structure and n-type doping creates an excess of electron in the crystal structure. Both n-type and p-type materials only have elemental compositions with electron rich and hole rich crystal lattice respectively, hence none of them are negatively or positively charged individually.

Since p-doped crystals lack electrons in the valence band, the probability of finding an electron in the valence band reduces. Therefore, to keep the Fermi level at the point where electron-finding probability is half (1/2), the fermi level moves nearer to the valence band (fig 2.2e). Accordingly, n-doped crystals have excess electrons in the conduction band which increases the electron-finding probability at this band and thus the Fermi level moves nearer to the conduction band (fig 2.2f). However, the position of the Fermi level in extrinsic semiconductors (either n or p) depends on the concentration of dopants added

to the intrinsic crystal, which is termed as the doping concentration [10]. This means, if the semiconductor is heavily dopped (n+ or p+), the position of the Fermi level will be nearer to the corresponding band edge (fig 2.2e and fig 2.2f).

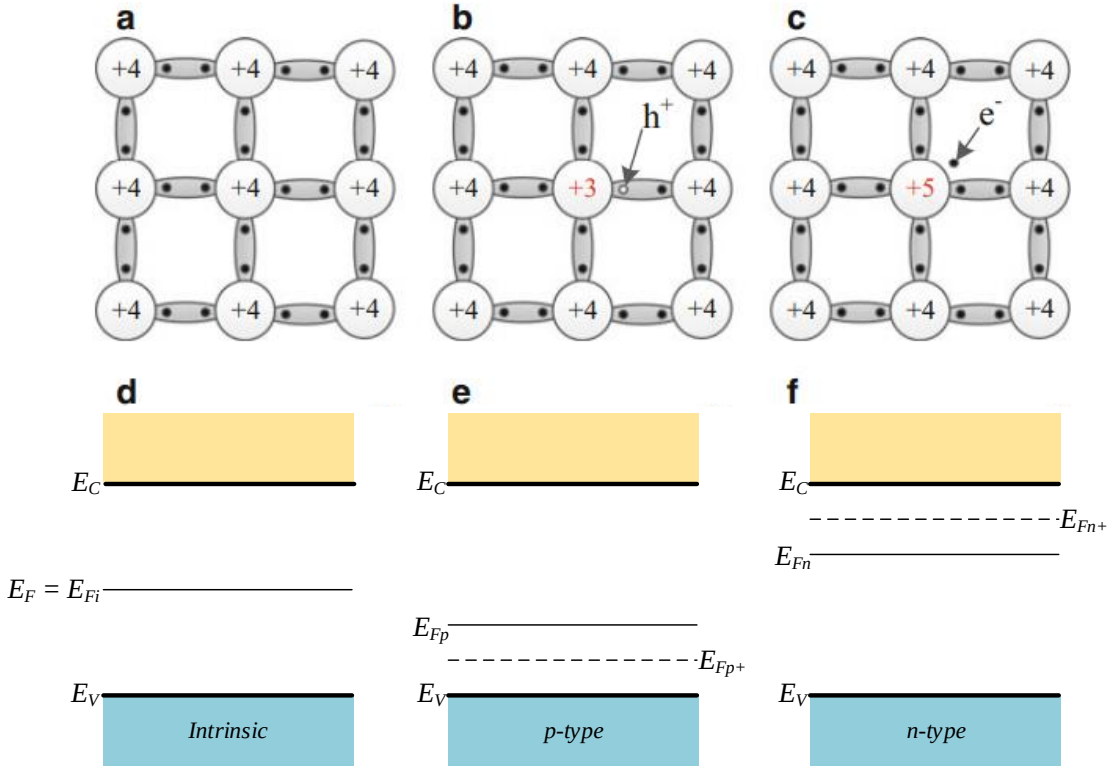


Fig. 2.2 Schematic diagram of a typical **(a)** intrinsic, **(b)** p-doped and **(c)** n-doped semiconductor materials bonds. The band diagram of **(d)** intrinsic, **(e)** p-doped and **(f)** n-doped semiconductor materials are also shown in terms of different Fermi level positions caused by different doping concentration (modified from [8]).

2.2 Device structures of Photovoltaic (PV) cells

2.2.1 Single junction devices

Photovoltaic (PV) device fabrication process mainly comprises of creating junctions of different materials having different solid-state characteristics or band structures. There are possibilities of creating semiconductor-semiconductor junctions, metal-semiconductor junctions, metal-insulator-semiconductor junctions etc depending on the device requirements. The major junction arrangements and their probable band alignments are described as follows:

2.2.1.1 Semiconductor-Semiconductor junction

The most basic type of PV cell is based on semiconductor p-n junction [7], [11]. Due to the excess of holes and electrons present in p-type and n-type semiconductor materials, respectively, when the semiconductors are in intimate contact, holes from the p-type material diffuse into the n-type material leaving behind negatively charged acceptor atoms, while electrons from the n-type material diffuse into the p-type material leaving behind positively charged donor atoms assisted by the density gradient [7]. Due to this exchange of charge carriers between the two portions, the p-type layer near the junction becomes negatively charged and the n-type layer near the junction becomes positively charged and an opposing electric field is generated restricting further diffusion of carriers by creating an equilibrium. This creates a depletion region at the semiconductor junction. Alongside, for the band-structure, the Fermi level is adjusted, and CB and VB move accordingly to create a band-bending which is analogous to the depletion region. The depletion width depends on the doping density [8].

Now when solar radiation falls on the junction and provides enough energy to the valence band electrons to be elevated to the conduction band, free electrons and corresponding electron-vacancies are created which are also called electron-hole pairs. These pairs are separated by the help of the internal electric field, and electrons flow towards the downward slope and holes flow towards the upward band-bending. Figure 2.3 depicts the whole process of creation of internal electric field and electron-hole pairs as well as their separation mechanism and transport mechanism.

It is to be noted that, **creation** of electron-hole pairs by the absorption of photon-energy take place throughout the semiconductor material, but the **separation** of charge carriers only takes place in the depletion region. Hence, a narrow depletion region means the active area of the cell is also narrow. Slight improvisation to the p-n junction of basic PV device structure is often done by incorporating an intrinsic (i-type) layer of semiconductor sandwiched in the middle to form a p-i-n junction structure. This helps the depletion region to be spread over the whole intrinsic region, hence maximizing the active volume of the device, thus forcing better output [12].

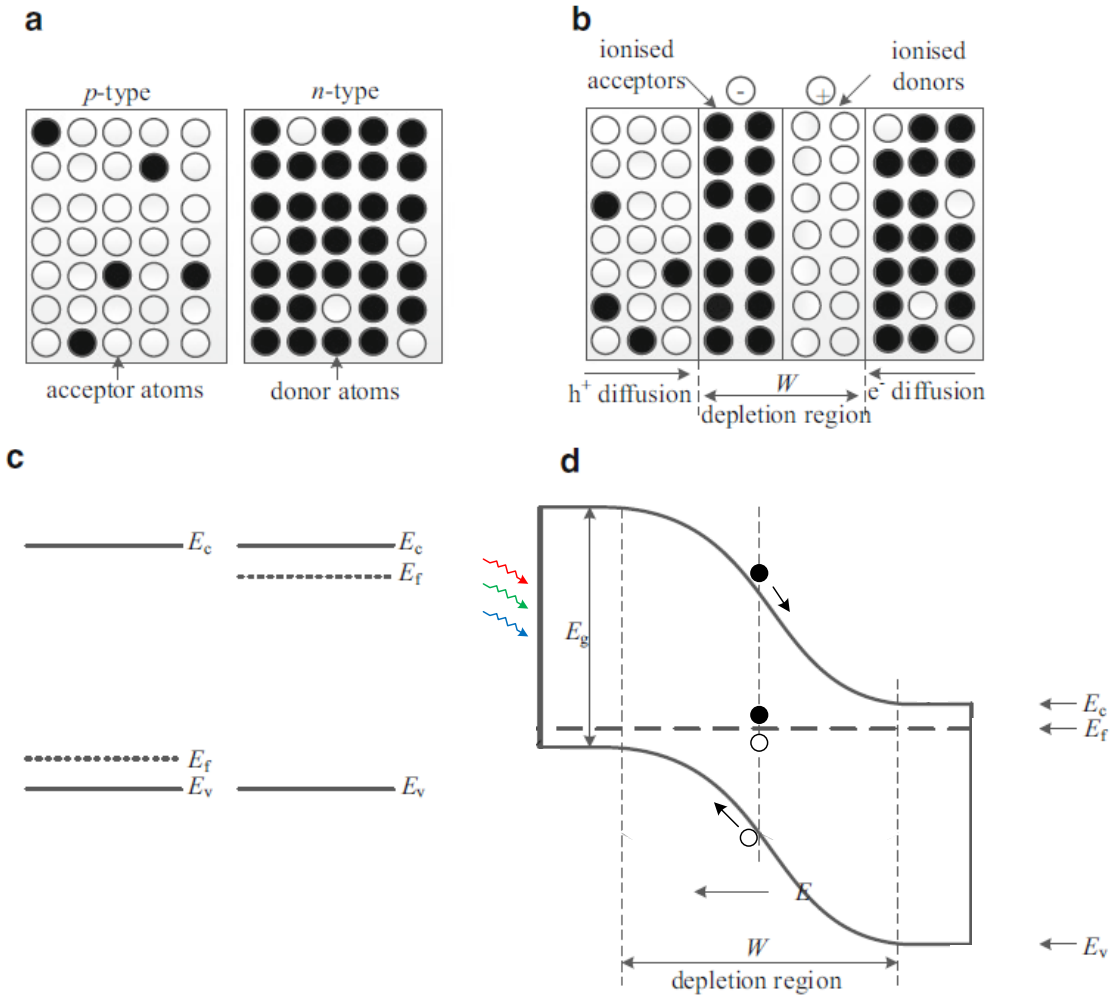


Fig. 2.3 Schematic illustration of (a) p- and n-type material prior to junction formation, (b) after p-n junction formation and energy band diagram of (c) p- and n-type semiconductor materials prior to the formation of p-n junction and (d) after junction formation and exposed under solar radiation.

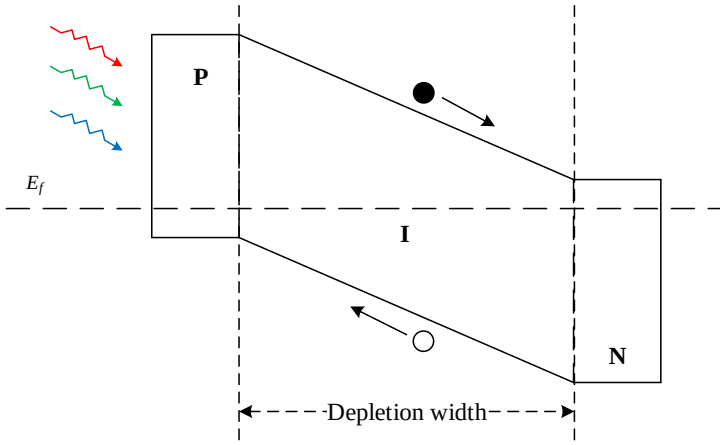


Fig 2.4 Band structure of p-i-n junction under illumination

Band-bending at semiconductor-semiconductor junction can also take place when alteration in doping concentration causes junction between n-n+ or p-p+ regions, having different Fermi level positioning. One recognisable attribute of these junctions is the low potential step (figure 2.5) they create. However, n-n+ or p-p+ junctions may positively contribute to a PV device performance when working in auxiliary to other junctions, by helping higher photon to electron conversion [13].

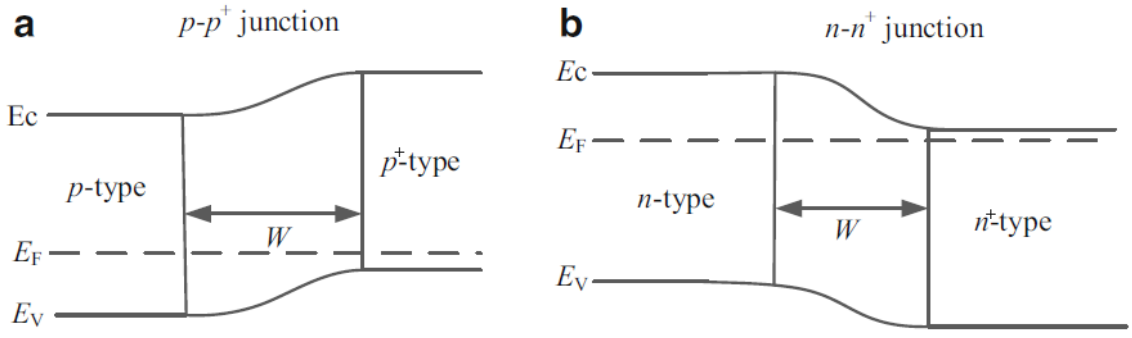


Fig 2.5 Band structure of (a) p-p$^+$ and (b) n-n$^+$ semiconductor-semiconductor junctions

2.2.1.2 Metal-Semiconductor (M/S) junction

In the process of semiconductor device fabrication, especially in case of PV device fabrication, metal contacts created on the semiconductor surfaces are of paramount importance. In a PV cell, for a semiconductor-semiconductor junction to be able to contribute current to an external circuit, metal contacts on the two ends of the device are essential. These metal contacts create unique interfaces between the different metals and semiconductors, the characteristics of which need understanding for effective device design, material identification and analysis. Depending on the metal and semiconductor (S/C) type, M/S junctions can mainly be of two types: (i) non-rectifying Ohmic contact that allows flow of current in both directions with lowest resistance, and (ii) rectifying Schottky contact that allows current flow in only one direction [14], [15].

As per the Table 2.1, at a metal-semiconductor junction, ohmic contact will be formed under either of these two conditions: (i) when an n-type semiconductor having a work function $\varphi_{ns,}$ makes contact with a metal having a smaller work function φ_m ($\varphi_m < \varphi_{ns}$); and (ii) when a p-type semiconductor having a work function $\varphi_{ps,}$ makes contact with a metal having a higher work function φ_m ($\varphi_m > \varphi_{ps}$). Contrarily, an M/S contact will show rectifying characteristics under either of these two conditions: (i) when an n-type semiconductor having a work function $\varphi_{ns,}$ makes contact with a metal having a higher work function φ_m; and (ii) when a p-type semiconductor having a work function $\varphi_{ps,}$ makes contact with a metal having a smaller work function φ_m. To be noted that, an Ohmic contact also comprises of a negligible (<0.40 eV) barrier height (φ_b), hence allows flow of current in both directions under a biased condition. Rectifying Schottky contacts form a large barrier height (φ_b) of >0.40 eV [9]. In ideal condition, for any M/S junction,

$$\varphi_b = \varphi_m - \chi_s \qquad \text{(Equation 2.1)}$$

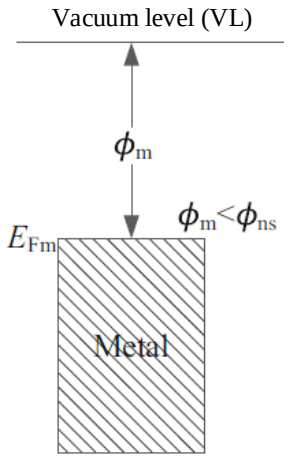
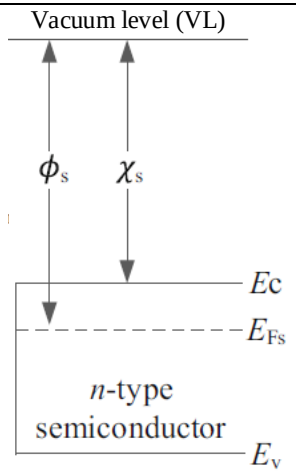
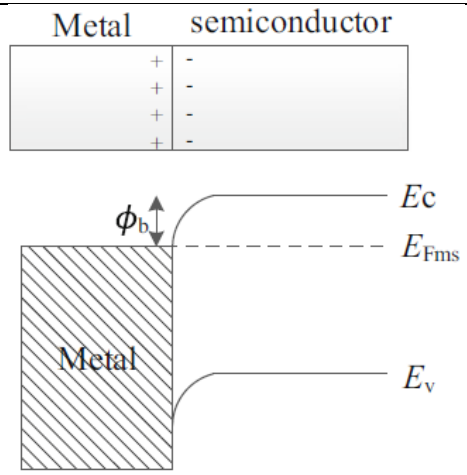
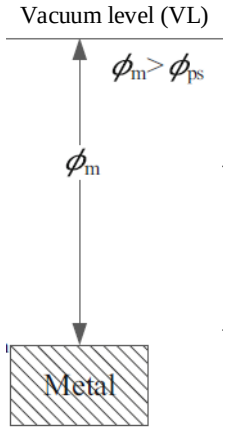
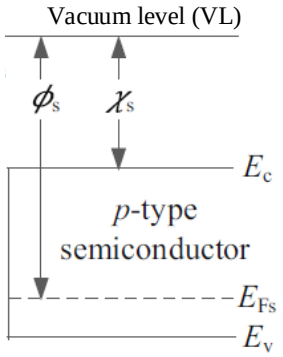
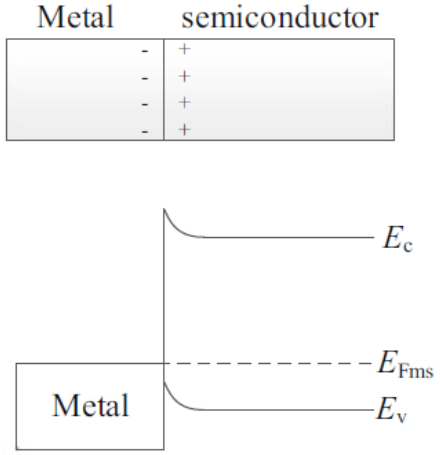
The metallic work function (φ_m) is the amount of energy necessary to take an electron to the vacuum energy level from the metal's surface or Fermi level (illustrated in Table 2.1). φ_m values of metals are typically found within a constant range, given the surface of the material is reasonably clean. The semiconductor work function (φ_s) on the other hand can be determined from the equation 2.2:

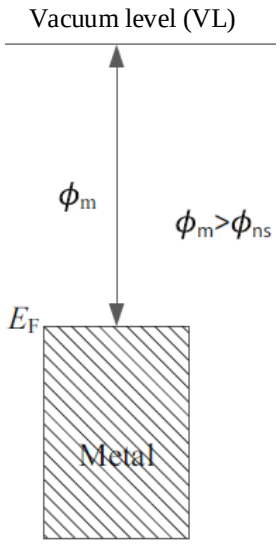
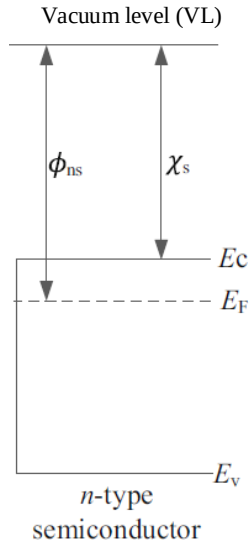
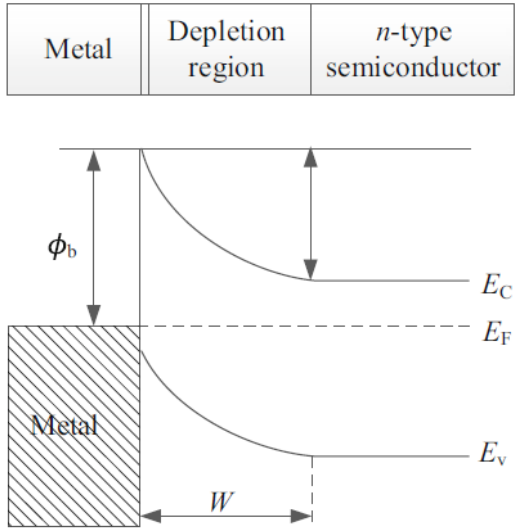
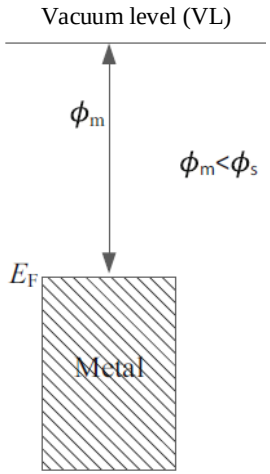
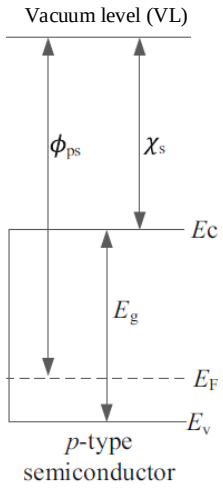
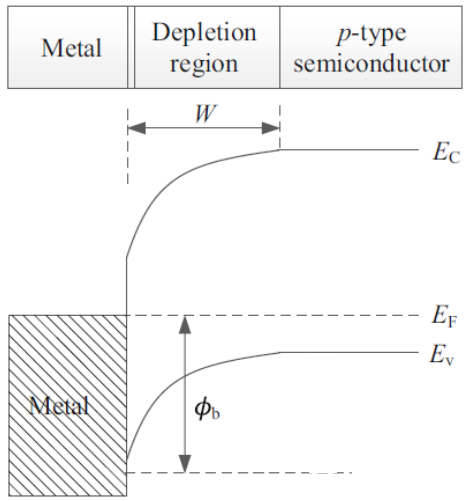
$$\varphi_s = \chi_s + (E_c - E_F) \qquad \text{(Equation 2.2)}$$

Where, χ_s = Electron affinity of the semiconductor, E_c = Energy of the conduction band minimum and E_F = Fermi level energy of the semiconductor.

However, the above discussion is only true in case of ideal situations. In reality, no surface is defect free and it is often impossible to precisely forecast the Fermi level positioning because M/S surfaces are prone to defects and Fermi level pinning [16]–[18]. Yet, considering the uncertainty of M/S junction while choosing a metal contact on a semiconductor, one should begin searching considering the equation 2.1 above.

Table 2.1 Summary of conditions behind different M/S junction formations along with band alignment

Contact type	S/C type	Metal	Semiconductor	M/S junction
Ohmic contact	n-type			
	p-type			

Rectifying contact	n-type			
	p-type			

2.2.1.3 Metal-Insulator-Semiconductor (MIS) junction

At the M/S interface of a PV device, the open circuit voltage (V_{oc}) of the corresponding device is proportional to the barrier height (φ_b) formed due to rectifying metal-semiconductor junction [9], [15]. However, M/S junction Schottky devices generally exhibit lower barrier height (φ_b), hence lower V_{oc} than that of the p-n junction [11]. Therefore, depending on the device design, it may be necessary to increase the barrier height of Schottky contacts and a great way to do that is to incorporate a thin insulating layer sandwiched between the metal and semiconductor layers, forming a Metal-Insulator-Semiconductor (MIS) junction. The insulating layer, as illustrated in figure 2.6, detaches the semiconductor from the metal layer and elevates the Fermi level positioning near to the conduction band, hence increases the barrier height. Moreover, inclusion of the insulating layer also reduces the possibility of the potential degradation of the M/S contacts. Sometimes for PV devices, unintentionally grown oxide layers between metal-semiconductor junction may also work as an intermediate insulating layer and form an MIS structure [19], [20]. However, the thickness (δ) of the insulating layer, if not optimised can negatively contribute to the series resistance (R_s) of the device, degrading the device performance in turn.

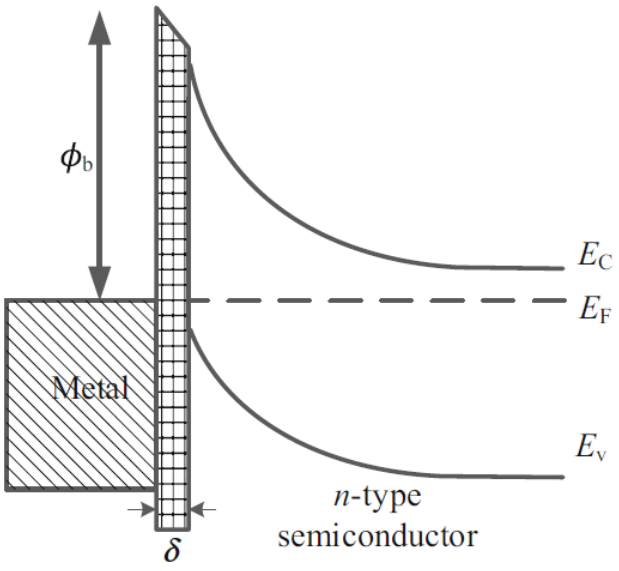


Fig 2.6 Energy band diagram of an MIS interface showing enhancement in potential barrier height due to incorporation of thin insulating layer of thickness, δ, at the interface.

2.2.2 Multi-junction PV devices

In 1954, when Bell Laboratory announced its success with the first ever practically usable photovoltaic device that directly converts sunlight into electrical power, though not

readily available for day-to-day household use, this had created a great excitement in the scientific community considering the abundance of sunlight as a source of energy [21]. There started an impressive race amongst scientists to analyse, optimise and predict the potential of this new device [22]. In the late 50's extra-terrestrial applications started to show notable use of PV cells and several predictions based on empirical values had surfaced in determining the maximum possible efficiency limit for these kinds of devices [23]. In 1961, the physicists William Shockley and Hans Queisser came up with the most widely accepted calculation of upper theoretical limit for the efficiency of Si-base single p-n junction solar cells [22]. This limit later became famous by the name of Shockley-Queisser limit, which predicted the upper theoretical limit to be ~30% given the cell performance being limited by-

i. Single junction of one bandgap material, hence absorbing just a certain portion of electromagnetic spectrum.

ii. Radiative recombination, being the only loss mechanism that cannot be reduced to zero.

Shockley and Queisser, in their prediction, took the semiconductor band gap as 1.1 eV, considering Silicon as the most widely used material, and illuminated the cell by a black body with a surface temperature of 6000 K. However, today the AM 1.5G (1000 Wm^{-2}) spectrum is the standard spectrum for non-concentrated photovoltaic conversion, taking light absorption and scattering in the atmosphere into account. Moreover, new photovoltaic materials having different bandgap energies and different loss mechanisms involved are investigated every day expanding the possibility of different theoretical upper limits for single junction cells. To date the highest possible theoretical upper limit of a single junction PV cell is ~33.7% for semiconductor material having 1.34 eV bandgap energy [24].

Now, surpassing this basic limit set by Shockley-Queisser analysis is a major challenge taken by the scientific community. The largest limitation presented by Shockley-Queisser is the spectral limitation set by the single-junction approach. Hence in terms of this spectral constraint, several approaches have been explored to significantly surpass the basic limit by engaging multiple junctions formed with different semiconductor materials having different bandgap energies. The two major approaches of multijunction solar cell constructions are discussed below.

2.2.2.1 Tandem based multijunction

The word 'tandem' is often used for bicycles having two separate pedals for two riders to bike in conjunction [25]. Since the performance of conventional single junction PV devices are limited by the Shockley–Queisser limit due to the band-gap limitation as well as in terms of absorption limitation of solar spectrum, the Tandem structure of solar cells came into being to facilitate absorption of most parts of the solar spectrum, as per figure 2.7 [22], [26]–[28].

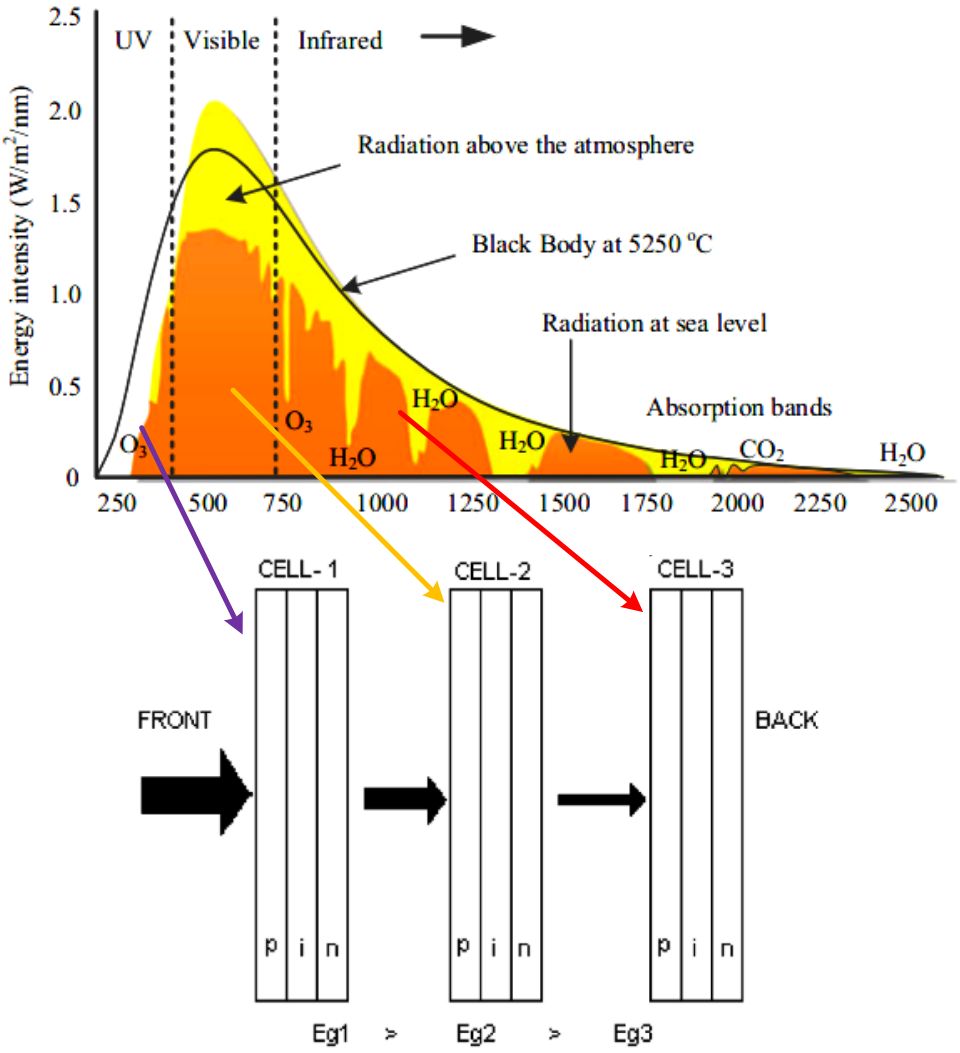


Fig 2.7 Approximate arrangement of three different p–i–n diodes to utilise photons from three spectral regions. The bandgaps of individual sub-cell materials have gradually decreased from cell-1 to cell-3 to absorb the UV, Visible and Infrared portion of the EM spectrum respectively (Adapted from [8], [26])

In tandem multi-junction solar cells, instead of a single p-n junction, multiple number of p-n, p-i-n, p-n-n^+ or n-p-p^+ structures are connected in series with a tunnel junction in

between. Each material's p-n junction produces electric current in response to different wavelengths of light. Due to the series connection, according to Kirchhoff's current law (KCL), the individual voltages of the sub-cells add up giving a rise to the overall V_{oc} of the device [29]. However, as per KCL the circuit's current reading is matched for all the individual devices and hence drops lower than the lowest current produced by any sub-cell. Therefore, for Tandem solar cells a high V_{oc} and comparatively lower J_{sc} is often observed. In order for two or more cells to be connected in series an ohmic connection between two individual cells need to be formed. Consequently, for two p-n or p-i-n junctions to be connected in series the interim ohmic connection must also be made without collapsing the device's band structure. Therefore, in a Tandem device, in order to allow the collected carriers by an individual sub-cell to contribute current to the circuit without causing major losses, tunnel recombination junction (TRJ) diodes are typically used between the solar cells. The TRJ should be a low bandgap, optically transparent p-n junction with no rectifying behaviour due to heavy degenerative doping greatly shrinking the depletion width, to allow the electrons from the top cell and holes from the bottom cell to tunnel through and recombine to maintain a continuous current flow (figure 2.8) [30]–[33].

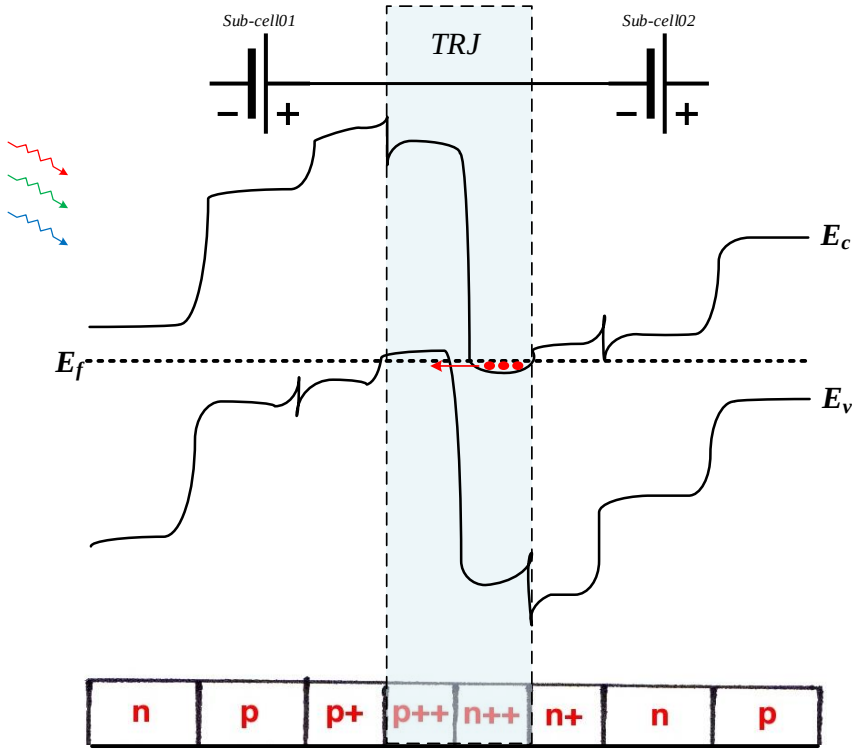


Fig 2.8 Tunnel recombination Junction (TRJ) between two PV cells namely sub-cell01 and sub-cell02 allowing direct flow of electron through the TRJ.

It is important for a tandem solar cell that its individual sub-cells produce current comparable to all the other sub-cells to maintain a reasonable overall current. That is why direct tunnelling of produced charge carriers is important hence it is the fastest process of recombination hence enables best current flow comparable to an ohmic contact. The major drawback of Tandem solar devices is that, though the tunnel junctions employed in between the individual cells are theorised to be ohmic contacts to both the connecting cells [34], the recombination process is mainly dominated by radiative or non-radiative recombination respectively in reality. Whereas radiative recombination at the TRJ is the slowest process and immediately hampers the cell performance, non-radiative recombination caused by mid-gap defects is comparatively faster and may contribute positively [32][35]. Figure 2.9 depicts this probable phenomenon of local recombination with band diagram. Therefore, for tandem based multijunction solar devices, careful material selection, doping, thickness optimisation and incorporation of appropriate TRJs remains a key challenge. Moreover, the procedure inherently requires more processing steps during production which possesses certain economic challenges too [36].

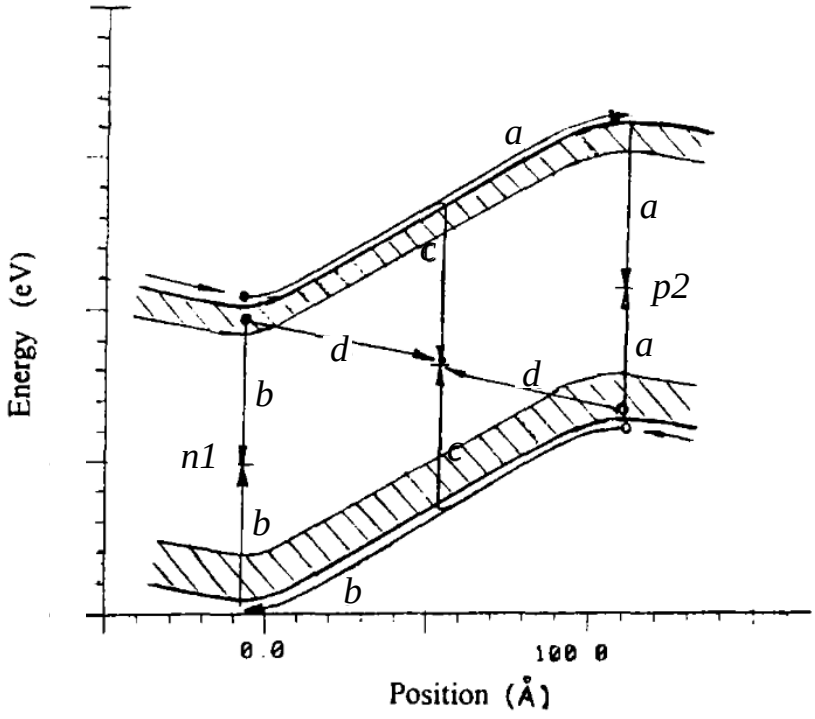


Fig 2.9 The processes of localized recombination and non-localized recombination. In localized recombination charge carriers have to overcome the big potential energy barrier. In the process (a) electrons overcome the big energy barrier to the p2 region; in the process(b) holes overcome

the big energy barrier to the n1 region, and in the process(c) electrons and holes each overcome about half of the energy barrier to a middle point. The process (d) is the non-local recombination. Electrons and holes tunnel to a defect states at the middle of the "tunnel junction" and recombine [adopted and modified from [32]].

2.2.2.2 Graded bandgap multijunction

Another approach to overcome the Shockley–Queisser limit for PV devices is the development of graded bandgap (GBG) devices. This device structure was first conceptualised by Konagai et al. [37], and was later improved and next-generation multilayer graded bandgap solar cells were proposed and implemented by the Solar energy research group, Sheffield Hallam University [9], [26], [38], [39]. As shown in figures 2.10 and 2.11, GBG devices are developed by sequentially growing semiconductor layers with materials having gradually decreasing bandgaps where the conduction type of the semiconductor layers beginning from a certain type (n or p) changes to the other (p or n) at the end. This continuous and descending full gradation of bandgaps allows the device to absorb greater portions of the solar spectrum and therefore causes separation of more electron-hole pairs creating a greater flow of short circuit current (I_{sc}) [8]. Greater I_{sc} is also caused by phenomenon called impact ionisation and impurity PV effect (as described in section 2.3.4.3) in GBG devices. Since short circuit currents add up for these kinds of devices, according to Kirchhoff's current law it can be deemed as a parallel connection of cells [9], [29]. Due to not having any tunnel junctions within the device unlike the tandem multi-junction devices, GBG devices do not suffer from any major possibility of inter-device recombination. However, GBG devices may suffer from a constraint in terms of open circuit voltage (V_{oc}), because barrier height (φ_b) can be limited by the lowest bandgap absorber layer used in the device(figure 2.10). It is noteworthy that, limitation of V_{oc} is another feature of parallelly connected cells [29]. V_{oc} of the graded bandgap solar devices can be maximised by using a wide bandgap p-type window approach that is further discussed in section 2.3.2. Moreover, this kind of device can be fabricated using low-cost fabrication technique like electrodeposition (ED) and is suitable to be studied and even manufactured in developing countries [40], [41]. In this thesis, the author focused on fabricating next generation graded bandgap solar cells based on Cadmium Telluride (CdTe) absorber material and with a p-type wide bandgap window approach.

2.3 CdTe based Graded Bandgap Devices

Acceleration of photovoltaic (PV) research started from the early 1970s with the first oil crisis, and Cadmium Telluride (CdTe) based CdS/CdTe hetero-junction solar cells became one of the major thin film solar cells put under intense research [42]. Out of the two materials from the II-VI family, undoped Cadmium Sulphide (CdS) having a typical bandgap of ~2.4.2 eV is inherently an n-type semiconductor and CdTe with a typical ~1.45 eV bandgap can exist in both n- and p-type electrical conduction intrinsically [8]. Therefore, the CdTe/CdS heterostructure immediately presents a potential to form a bandgap gradation while carefully put into a device structure.

By the end of the 1980s, the conversion efficiency of this device gradually entered into double digits and Britt *et al* [43] in 1993 reported 15.8% for a lab-scale device. The development progress became slow and it took nearly another decade to increase the efficiency only by 0.7% to 16.5% by Wu et al in 2001 [44]. In parallel to this scientific research, BP Solar initiated a scaling up process in the mid-1980s using electro-plated CdTe and successfully manufactured 0.96 m^2 solar panels with an efficiency of 10.6% [45]. Although BP Solar was in the forefront of this technology, termination of this manufacturing work together with other solar energy activities around 2011 was a real set-back for the development of CdS/CdTe solar cells. Although scientific research continued in academic and research institutes, the highest solar energy conversion efficiency stagnated at 16.5% for another decade until ~2013.

Around 2013, the First Solar Company in the United States started to report rapid progress in the development of this device. The lab-scale efficiencies rapidly rose from reported 16.5% to ~22% in ~2017 [46]–[48] within a short period of four years. First Solar is now producing ~19% efficient solar panels, becoming the largest thin-film solar panel manufacturer in this field and reported that they are fabricating their latest devices based on a Graded Band Gap (GBG) approach [49].

The main features of GBG devices are (i) presence of wide bandgap window material in the front, (ii) gradual reduction of the bandgap towards the back absorber material, (iii) slow change of electrical conductivity from p- to n- or n- to p-, and by keeping the smallest bandgap used at ~1.40 eV (typical bandgap of CdTe absorber layer) to achieve V_{oc} values above 1.00 V, when optimised.

2.3.1 Graded bandgap devices with n-type window

According to figure 2.10a, the device has an n-type window layer with a possibility of harnessing photons across UV, Vis and IR region of electromagnetic spectra gradually absorbed by the different materials with different bandgaps. Moreover, carriers elevated by thermal energy and trapped within possible defect states can also contribute to the net current by the help of two phenomena called impurity PV effect and impact ionisation [50], [51]. These phenomena are further discussed in later sections.

2.3.2 Graded bandgap devices with p-type window

GBG devices can also be grown on p-type window layers for achieving a good spectral response over the wide solar irradiance. Like the n-type window approach, the performance of these devices are also affected by impurity PV effect and impact ionisation [50], [51]. But this approach also has some advantages over its n-window counterpart due to having a possibility of achieving a higher potential barrier height ($ø_b$), which will increase the slope for carrier transport thus increase the open circuit voltage (V_{OC}) [39], [51]. Figure 2.10(b) shows the schematic of a typical GBG device grown on p-type window layer.

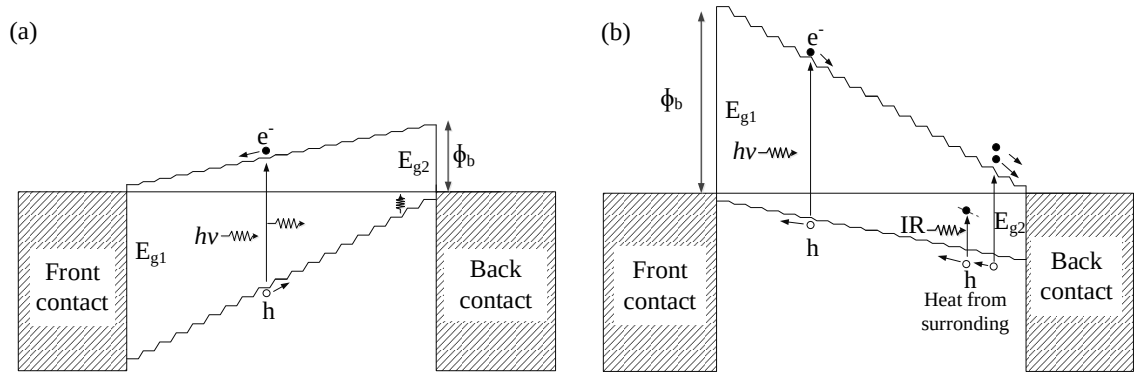


Fig 2.10 Graded bandgap device structures (a) on n-type window material and (b) on p-type window material.

Moreover, for the p-type window approach, since the flow of electrons is from the higher bandgap material towards the lower bandgap material, the electrons have a better possibility of gaining higher kinetic energy and therefore break more bonds on their way by impact ionisation and also contribute to the process of impurity PV effect. These mechanisms are further discussed in section 2.3.4.3.

The above model has been experimentally tested at least in two instances as per the literature. The experimented devices based on GaAs/AlGaAs and perovskite material have achieved high V_{oc} and PCE (η). Both devices have p-type window materials in the front, and bandgap grading is achieved using several material layers. Both devices produce high V_{oc} and conversion efficiencies; V_{oc}~1.175 and η~20% for GaAs/AlGaAs and V_{oc}>1.00 V and η>20% for perovskite solar cells [39], [52], [53].

2.3.3 Back diffusion barrier layers

For multilayer GBG solar cells, along with the regular window layer and absorber layer, more improvements may be incorporated in the form of an electron back-diffusion barrier (ebdb) layer and a hole back-diffusion barrier (hbdb) layer [54], by minimizing the recombination of photo-generated and separated charge carriers by thermionic emission over the potential barrier [9], [54], [55]. In figure 2.11, graded bandgap devices fabricated on p-window material, in both short-circuit and open circuit modes, are presented. Photo-generated e-h pairs should be readily created by the absorption of photons, separated and transported to the electrical contacts at both ends of the device by the slope or the internal electric field resultant from the potential barrier height. When in short circuit, the collected carriers are supposed to be flowing through the external circuit in form of an electrical current. However, when the device is in open circuit, electrons and holes tend to recombine by moving through thermionic emissions. A p^+-layer allows holes to transport easily to the front contact but prevent electrons moving to the front contact. Therefore, the layer is accurately labelled as an electron back diffusion barrier (ebdb) layer. Similarly, an n^+-layer allows electrons to transport easily to the back contact, but prevents holes moving in that direction. Therefore, the layer is labelled as a hole back diffusion barrier (hbdb) layer. Instead of p^+ and n^+ layers for (ebdb) and (hbdb), highly resistive insulating layers can also be used, only if their thicknesses are low enough for charge carriers to tunnel through. These layers then act as pinhole plugging layers, improving especially the thin film solar cell performance. Although this description, given in figure 2.11, is for a graded bandgap device based on p-window material, the use of ebdb and hbdb layers are identical for p-n, p-i-n or any other hetero-junction solar cell. However, for a p-window device, a wide bandgap p-type ebdb layer can also help by increasing the barrier height (φ_b), hence V_{oc}.

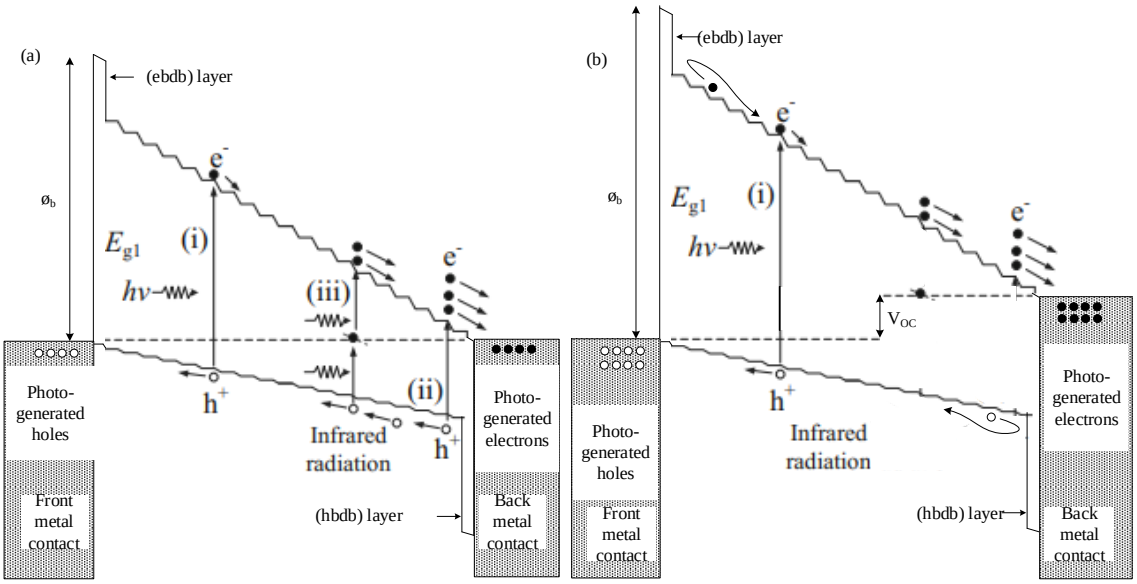


Fig 2.11 Energy band diagram of a graded bandgap solar cell fabricated on a p-type window material in both (a) short-circuit and (b) open-circuit modes. Note the addition of (ebdb) layer and (hbdb) layers to enhance charge separation in the device.

The Electron back diffusion barrier (ebdb) layer and hole back diffusion barrier (hbdb) layers are often termed as Hole Transport Layer (HTL) and Electron Transport Layer (ETL) respectively, but in reality rather than transporting holes or electrons, the way these layers improve device performance is by restricting the carriers to back-diffuse and recombine during device operation. Therefore, considering the prospects of thin-film solar cells based on p-type window layer and inclusion of ebdb and hbdb layers, the scientific community should further develop by focusing on implementing these ideas for CdTe-based devices. This research project has conceptualised CdTe-based novel devices incorporating both of these ideas and aimed for further developments [41], [56].

2.3.4 Complications and controversies around CdTe-based PV devices

2.3.4.1 Fermi level pinning at M/S interfaces

As discussed previously in the section 2.2.1.2 above, semiconductor surfaces are not ideal and there are always chances of finding one or more defect states on these surfaces. Therefore, at the M/S interface this phenomenon may cause the Fermi level to get pinned at a defect level. This phenomenon is widely known as Fermi Level pinning [8], [42]. The presence of high concentrations of defects has been experimentally observed at n-

CdTe/metal contacts and it has been found that there are at least 5 possible defect levels within the forbidden region of n-CdTe surface (see Figure 2.12) [18]. A large number of metal contacts fabricated on these surfaces have shown that the Fermi level pins at one of these defect levels. Pinning position depends on the history of materials and the nature of the surface. Te-rich n-CdTe surfaces tend to pin the FL at E_1, E_2 or E_3 producing Schottky Barriers (SB) with low potential barrier heights (E_c-E_1)~0.40, (E_c-E_2)~0.65 or (E_c-E_3)~0.73 eV. Cd-rich n-CdTe surfaces show FL pinning at E_4 or E_5 yielding large potential barrier heights (E_c-E_4)~0.96 or (E_c-E_5)~1.18 eV. When one of the defects has high concentrations, the SB formed is independent of the metal or the electrical contact material used. In order to produce excellent rectifying contacts on n-CdTe surfaces, Cd-rich CdTe surfaces should be used with un-reactive metals or electrical contact materials [57]. In summary, if large SBs with excellent rectifying contacts are desired, the n-CdTe surface should be prepared with Cd-richness and a non-reactive material like Sb or any other conducting material should be used [58].

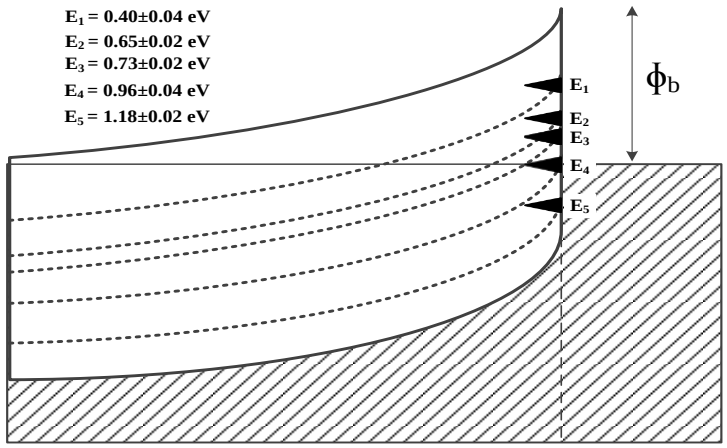


Fig 2.12 Experimentally observed possible Fermi level pinning positions (E_1 to E_5) at n-CdTe/metal interface. E_1, E_2 and E_3 are dominant when the surface is Te-rich and E_4 and E_5 are dominant when the surface is Cd-rich.

This FL pinning possibility may introduce reproducibility issues for n-CdTe/metal interfaces and can be tried to be controlled by different etching techniques [18]. Details about the etching process of CdTe surfaces are discussed in later sections.

2.3.4.2 Possible Device architectures

As mentioned earlier, CdS is inherently an n-type material whereas, CdTe can exist in both n- and p- conduction types very easily. However, it is often observed that CdTe has been presumed to be of p-type electrical conduction without carrying out appropriate

experimental studies [59], hence CdS/CdTe heterostructures are often presumed to be n-p junctions whereas this heterostructure can also exist as n-n+Schottky barriers.

As depicted in figure 2.13(a), the formation of p-n junction takes place when the CdTe layer is grown with p-type electrical conduction. On the other hand, if the CdTe layer is grown as n-type in electrical conduction due to variation of growth conditions, then the CdS/CdTe hetero-junction is an n-n type weak rectifying contact. During the fabrication of metal contacts to n-CdTe, the FL pinning effects described as in Figure 2.12 applies. To form a device with the highest slope or an intense internal electric field, the FL should be pinned at E_5 or forced to a place close to the VB maximum. In this situation the device is an n-n+large SB at the back as shown in Figure 2.13(b). Now there are two rectifying interfaces: a weak rectifying junction at the n-n interface and a strong SB of ~1.18 eV at the back contact. These two junctions support each other adding currents and therefore, the two junctions are connected in parallel. Since the SB is extremely large, even exceeding the potential barrier of CdTe p-n junction, and the whole device has a two-junction architecture, this device can perform better than the simple p-n junction [42].

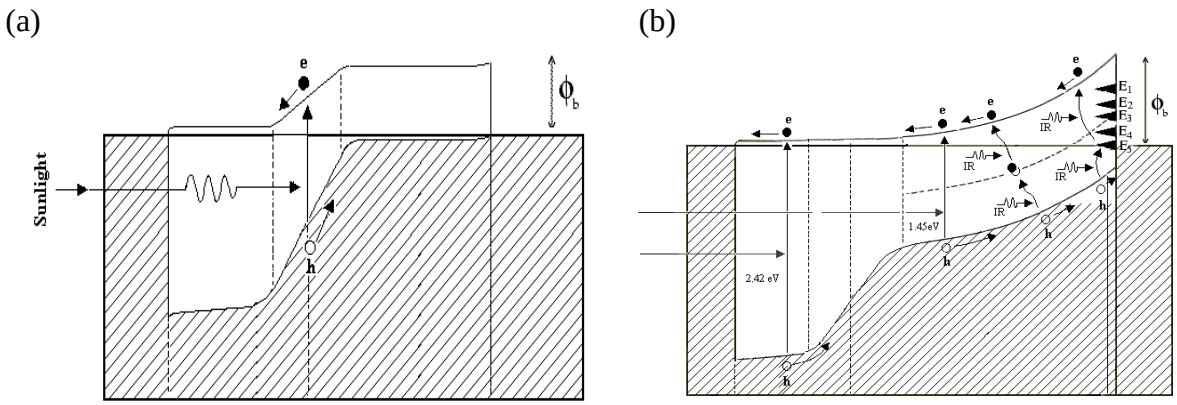


Fig 2.13 Two possible device architectures for CdS/CdTe based solar cell since intrinsic CdS is always n-type and CdTe can exist in both (a) p-type and (b) n-type electrical conduction.

2.3.4.3 High short circuit current density (J_{sc})

If a PV device is designed and fabricated to absorb all photons in the solar spectrum, J_{sc} can be increased to achieve ~54 $mAcm^{-2}$ [60]. However, this cannot be achieved simply by adding consecutive material layers with smaller bandgaps, since the V_{oc} depends on the smallest bandgap material used in the device as discussed above in section 2.3. Considering the standard test conditions and ideal loss mechanism, Geisthardt et al. have

recently calculated the highest possible values of single-junction CdTe based solar cells, where the possible J_{sc} is ~30 $mAcm^{-2}$ [61]. However, some batches of CdTe solar cells have regularly demonstrated higher J_{sc} than the above value, which indicates that other mechanisms must have been activated to harvest low energy photons and create more photo-generated charge carriers [8].

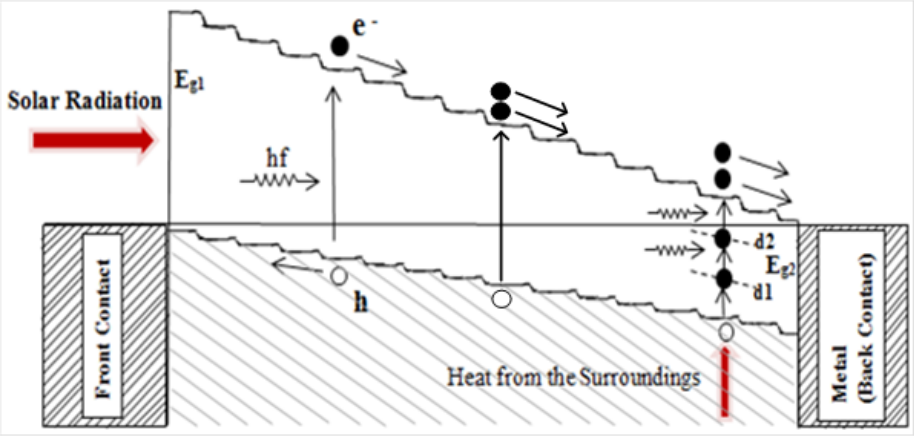


Fig 2.14 A graded bandgap solar cell device which can benefit from band-to-band impact ionisation and the combination of impurity PV effect and impact ionisation to create more photo-generated charge carriers. Note that there are two photon-inputs to such devices.

One possible mechanism active in a CdTe-based GBG device (as shown in Fig. 2.13b) is Impurity PV effect. This mechanism can be used by devices as shown in Figure 2.14. These have large bandgap in the front, and bandgap value gradually reduces towards the rear of the device. In order to keep large V_{oc} values above 1.00 V, the smallest bandgap should be limited to ~1.40 eV. Then the photons with energy less than the smallest bandgap used can be absorbed utilising native defects via multi-step absorption process or impurity PV effect. This is shown in Figure 2.14, and this process can be used to absorb almost all photons available in the solar spectrum. In addition, the surrounding heat can also contribute to the multi-step absorption process providing another input of photons to these kind of devices. All these processes contribute to the increase in J_{sc}, when the right conditions exist in this type of devices. When the multi-step absorption process is dominant, in a strong internal electric field, the recombination process is suppressed in such devices. It has been reported that GaAs/AlGaAs based graded bandgap devices fabricated with a p-window approach have demonstrated open circuit voltages (V_{oc}) of ~750 mV under complete darkness [50]. This indisputably demonstrates that impurity

PV effect is capable of becoming the dominating mechanism of charge creation in a GBG device.

Impact-ionisation is another possible mechanism that also increases the photo generated carriers. The photo-generated electrons in the front of the device accelerate towards the back-contact and travel through smaller bandgap materials. When the electron achieves kinetic energy greater than the bandgap of the absorbing material, an additional e-h pairs are created by band-to-band transitions (see Figure 2.14). This effect will be dominant in graded bandgap solar cells fabricated on p-type window materials.

The second type of impact-ionisation is more attractive and highly possible. Towards the rear of the devices, native defects are filled by infra-red (I-R) photons coming from both the solar spectrum and the surroundings. The accelerating photo-generated electrons from the front will have enough energy to transfer trapped electrons from defect levels to the conduction band. This combined process of impurity PV effect and impact-ionisation has a high probability of creating more charge carriers, and this will be an avalanche effect. Since both impurity PV effect and impact ionisation are built into this device, and with an additional input from the surrounding I-R radiation, the J_{sc} can achieve very high values beyond ~30 $mAcm^{-2}$ for CdTe solar cells. There are many publications with high J_{sc} values and First Solar has also reported 31.69 $mAcm^{-2}$ for CdS/CdTe solar cells [62] which is certainly exceeding reported theoretical values of ~26 and ~30 $mAcm^{-2}$.

2.4 Conclusion

The primary aim of this chapter was to cover the theoretical knowledge necessary to understand the physics of solid-state materials, especially that of semiconductors. Moreover, different interfaces between semiconductors and/or metals have also been discussed which are necessary for device formation. Modern approaches of PV device design and their corresponding advantages, limitations, and related challenges as well as controversies have also been discussed.

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Chapter 3

Methodology

3.1 Introduction

In this chapter the fabrication and characterisation techniques employed in this research are described. Cell fabrication techniques consist of the explanation of semiconductor layer deposition as well as metallisation techniques. Furthermore, electrochemical, structural, compositional, optical, electrical and morphological characterisation techniques for the semiconductor layers are also explained. Hence after the completion of device fabrication, the techniques to measure device parameters such as electrical and optical/spectral properties are also briefly explained.

3.2 Fabrication Techniques

CdTe based thin-film solar cells have been fabricated using a range of different techniques. For the fabrication of the semiconductor layers to form complete solar cells, the commonly used large-scale techniques are, vapour transfer deposition (VTD), close spaced sublimation (CSS) [1], sputtering [2], electrochemical deposition (ED) [3] etc. However, with respect to deposition process continuity, doping simplicity, self-purification, scalability, economic viability and Cd-containing waste reduction, electrodeposition (ED) is considered one of the most manufacturable techniques with proven track record [4]–[9]. In the work presented, considering these advantages, the electrodeposition (ED) technique is used for the semiconductor deposition.

Furthermore, for the complete fabrication of the device, metallisation is an inseparable step that must be done. Normally for electrodeposited CdTe-based solar cells, semiconductor layers are deposited on a glass/transparent conductive oxide (TCO) surface in a superstrate approach. Hence the metallisation is only necessary for the back electrical contact. This is done with either sputtering or vacuum evaporation technique.

3.2.1 Electrodeposition

Electrodeposition is a widely known scientific and industrial process where decomposition or deposition of certain material is achieved by the help of creating a potential difference between electrodes submerged into an electrolytic solution containing ions of the decomposed or deposited materials. Though this been used for a

long time to reduce various materials from their salts or for coating appliances such as utensils and jewelleries to ensure longevity, the working terms ‘electrolysis’, ‘electrode’, ‘anode’, ‘cathode’ ‘electrolyte’, ‘ion’ etc were first termed as Michael Faraday published his widely celebrated work in 1834 [10], [11]. In this work he stated the two laws that govern the phenomenon. The laws are known as ‘Faraday’s laws of electrolysis’.

The first law states, “The amount of any substance deposited at an electrode is directly proportional to the quantity of electric charge passed through the electrolyte.” The second law states, “The masses of different substances, liberated in electrolysis by the same quantity of electric charge are proportional to the ratio of the relative atomic mass to the chemical equivalent” [9].

Unification of the two laws have been worked out previously in the literature, which helps quantifying the amount of material deposited or liberated within a duration of time in reference to the measured current [9], [12]. Hence can also theoretically calculate the thickness of the electrodeposited layer according to the equation 3.1.

$$T = \frac{JtM}{zFd} \qquad (3.1)$$

Where, J = Average current density over the duration of electrolysis (A/cm^{-2}), t = Duration of electrolysis (s), M = Molar mass of the substance (gm/mol), F = Faraday's constant; 96,500 C/mol, d = Density of the substance deposited and z = Valency number of ions of substance (no. of electrons transferred) which can be calculated from the relevant chemical reaction equations, such as equation 3.2 in the case of typical CdTe electrodeposition.

$$Cd^{2+} + HTeO_2^{+} + 3H^{+} + 6e^{-} = CdTe + 2H_2O \qquad (3.2)$$

Here, equation 3.2 indicates that 6 electrons are transferred while CdTe gets deposited from any electrolyte containing Cd^{2+} and $HTeO_2^{+}$ ions. Hence, in this case the value of z is 6. So, it is extremely important to understand the chemical reaction occurring during the electrodeposition for having the estimation of electrodeposited thin-film thickness. Similarly, for the deposition of all other semiconductor materials, suitable precursors need to be selected.

In this work, electrodeposition has been carried out at a 2-electrode configuration using a potentiostatic (constant DC voltage) power supply and a cathodic working electrode, as per figure 3.1. In a polypropylene beaker, the required precursors (i.e. mix of cadmium

salt solution and TeO_2 solution for CdTe deposition) which were prepared using di-ionised water and stirred at a constant rpm with a magnetic stirrer at a constant temperature maintained by the hot-plate underneath. To ensure uniformity of the heat distribution, the deposition container is placed into another glass beaker filled with de-ionized water. The electrolytic solution releases anions (-ve) and cations (+ve) into the bath, which are attracted and neutralised by anode (graphite rod) through reduction (electron gaining) process and cathodic substrate (TCO coated glass) through oxidation (electron losing) process respectively. The current measurement is done in series as the deposition takes place, which then can be divided by the substrate area to find the current density at a given moment.

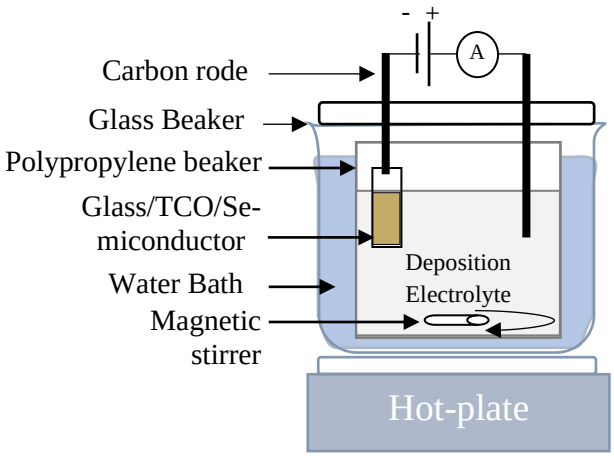


Fig 3.1 Electrodeposition of semiconductor material thin-films on glass/FTO substrate

A two-electrode configuration suffers from fluctuation in measured potential at working electrode caused by deposition of material on the electrode [12]. Electrodeposition can also be done with galvanostatic (constant DC current) power supply, anodic working electrode and three-electrode configuration. But, a three-electrode configuration had been avoided in CdTe work due to possible inclusion of unwanted dopants into the bath contributed from the additional reference electrode as was described previously [13], [14]. These impurities lead to drastic reduction of CdS/CdTe solar cell performance.

3.2.2 Metallisation

3.2.2.1 Thermal evaporation

Metallisation of the back contacts for the solar cell devices are often done with a widely used Physical Vapour Deposition technique called Vacuum thermal evaporation. This technique evaporates or sublimes target material (Au or In in this case) by the help of a resistive heater at very low vacuum pressure. The sample is placed in the path of vapour atoms with or without appropriate mask on as shown in figure 3.2.

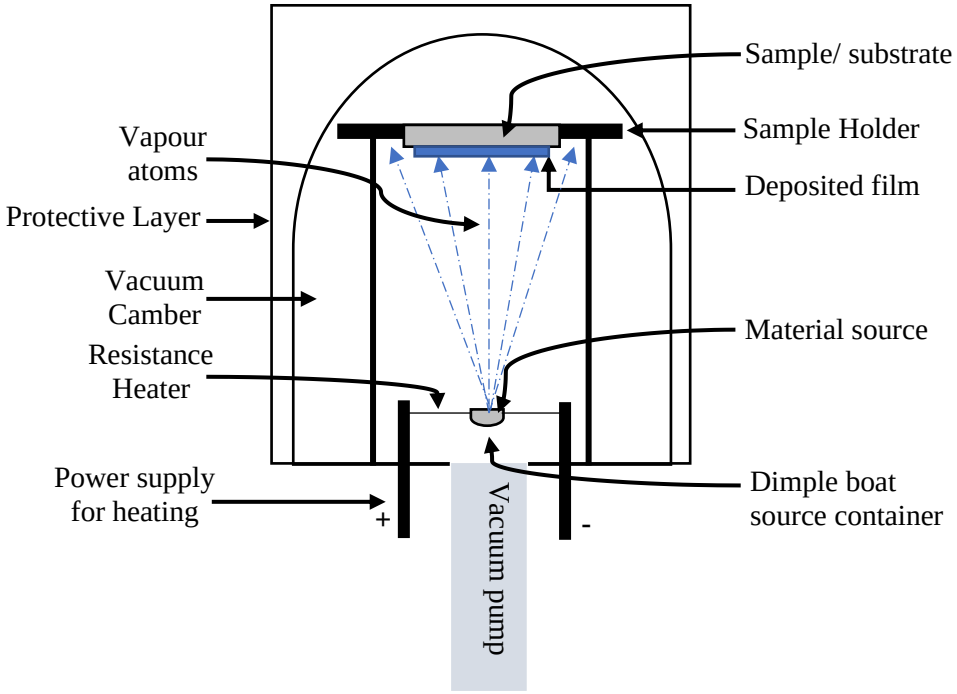


Fig 3.2 Generic working diagram of a vacuum evaporation system

The deposition thickness is a function of the evaporation rate, the geometry of the source and substrate, and the time of evaporation. The film thickness was measured with Quartz Crystal Microbalance (QCM) sensor, which is based on modified Saurbrey equation for high (>5%) frequency variation, linking the changes in the deposited mass with the oscillation frequency of a quartz crystal.

Modified Saurbrey equation: $\frac{\Delta m}{A} = \frac{N_q \rho_q}{\pi Z f_L} \tan^{-1}[Z \tan^{-1}(\pi \frac{f_U - f_L}{f_U})]$

Where, f_L is the frequency (Hz) of crystal after deposition, f_U is the frequency (Hz) of crystal before deposition, N_q is frequency constant for quartz crystal (1.668×10^{13} HzÅ),

Δm is the change of mass in g, A is the active crystal area in cm^2, ρ_q is the density of quartz crystal (2.468 gcm^{-3}) and the acoustic impedance of the film material, $Z = \sqrt{\frac{\rho_q \mu_q}{\rho_f \mu_f}}$

where, ρ_f is the density of the film material, μ_q is the shear modulus of the quarts crystal (2.947×10^{11} $gcm^{-1}s^{-2}$) and μ_f is the shear modulus ($gcm^{-1}s^{-2}$) of the film.

Since, all the other parameters are constants, the parameters of Z-factor and ρ_f are to be tuned in order to enabling in-situ measurements of the evaporated film thickness [15]. An Edwards Auto 306 has been used in this work for metallisation of back contacts at 10^{-7} mbar of vacuum pressure having a dimple boat type source container.

3.2.2.2 Sputtering

Apart from the vapour deposition technique, there had been another metallisation technique often used in solar cell fabrication, called sputtering. Sputtering is the process where thin-film coatings are deposited on a substrate with atoms or molecules of a material which are ejected from a target by the bombardment of high-energy ions [16]. Amongst the variety of sputtering systems used, the one that has been used in this work is a Magnetron sputter coater. Figure 3.3 depicts a typical magnetron sputtering chamber. The process starts by placing the glass/TCO/semiconductors substrate on the anodic sample holder of the vacuum chamber. The target material (metal) to be deposited is placed as the cathode. The permanent magnet creates a magnetic field around the cathodic target material. The vacuum chamber is then supplied with argon gas. When high voltage is applied, the argon gas gets ionised and forms a plasma around the magnetic field. Inside the plasma, the argon atoms are hit by free electrons and create secondary electrons. The atoms become positive ions therefore and gain kinetic energy due to the attraction by the negative cathode. The speeding argon ions then bombard the target surface and eject atoms of the target material, which again gain kinetic energy from the argon ion and speed towards the sample placed on the anodic holder, and a layer of target material gets deposited on the substrate. To ensure uniformity of the deposited layer, the sample holder is rotated at a constant rate.

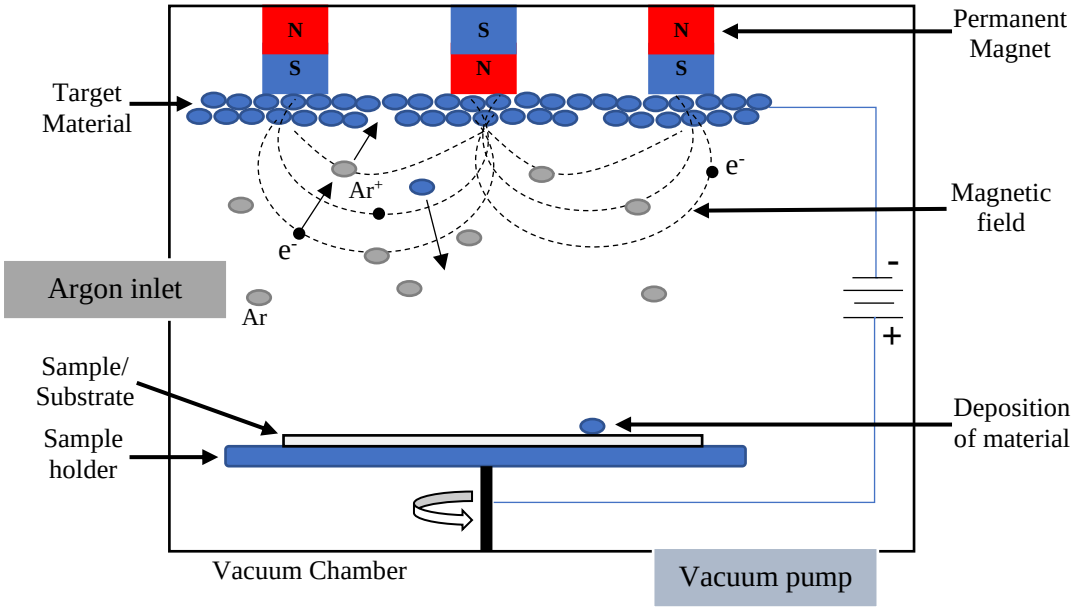


Fig 3.3 Schematic of a typical magnetron sputtering chamber

In this work, a Quorum Q300 TT Triple target sputtering system has been used. This sputter coater is fitted with a film thickness monitor (FTM), which measures the coating thickness within the chamber on a corresponding screen, in order to control the coating thickness of material deposited on the sample [17].

3.3 Material characterisation

3.3.1 Electrochemical characterisation

The research work carried out here is concerned with the study of electroactive materials. Electroactivity of these materials can be very effectively investigated with the technique called Cyclic Voltammetry (CV). In the course of solar cell fabrication from the electrodeposition (ED) technique, cyclic voltammogram (CV) is normally considered as the first experiment performed for the electrochemical study of the prepared electrolytes.

As per figure 3.4, the cyclic voltammogram is performed by measuring the varying current through the electrolytic solution while performing a potential sweep across the two electrodes [12]. In a two-electrode electrodeposition system the potential sweep can be carried out by ramping and receding the applied voltage between the electrodes within a range. In reference to a cathodic working electrode, while ramping there will be deposition of electrolyte-corresponding materials at different voltages due to reduction (gaining electrons) creating a sharp increment in current density (forward cycle in figure

3.4). On the contrary, while receding, deposited materials will get dissolved off from the working electrode at different voltages due to oxidation (losing electrons) and create sharp decrements in current density (reverse cycle in figure 3.4). The derived 'current density vs voltage' plot therefore helps to identify the cathodic voltage range suitable for the electrodeposition of target materials from an electrolyte.

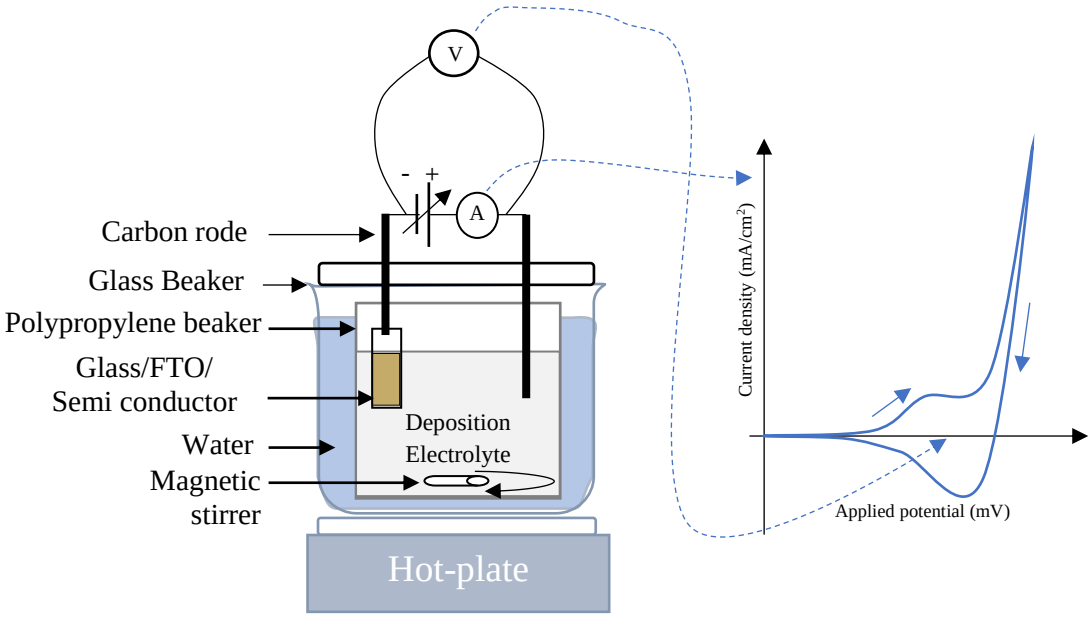


Fig 3.4 Typical formation of a cyclic voltammetric plot from a 2-electrode configuration

In this work, a Gill AC potentiostat from ACM instruments has been used to carry out the cyclic voltammogram within a range of 0-2000 mV. Voltage and current readings have been taken every 3 seconds.

3.3.2 Structural characterisation

3.3.2.1 X-ray diffraction (XRD) analysis

Being a trained physician, polymath Thomas Young came up with the first irrefutable experimental evidence in support of the wave theory of light with his famous double-slit experiment back in 1801 [18], [19]. The famous experiment showed the diffraction pattern created by the light wave while going through two slits separated by a distance, where amplitude of the light intensity demonstrated higher peaks at the point of constructive interference (bright fringes) and vice versa for the destructive interference (dark fringes). This same phenomenon later was observed for single slit also [20].

Governed by Bragg's law, this could quantify the size of the slit (d) according to equation 3.3

$$n\lambda = 2dsin\ \theta \qquad (3.3)$$

Where, λ = wavelength of the incident wave, n = integer order number and θ = incident angle of the wave (Bragg's angle).

Now, this was only possible because the size of the slit opening was of the same order as the wavelength of visible light (~10^{-6} m). For electromagnetic waves having much smaller wavelength, like x-rays, features much smaller (~10^{-9} m) are required for creating an interference pattern. In 1912, the physicist Max Von Laue suggested that a crystal lattice composed of atoms at specific distance may have a spacing small enough to create diffraction pattern using x-rays [21]. Therefore, the idea of x-ray diffraction (XRD) came to offer the possibility of detecting the crystal structure of any compound. Shown in figure 3.5, the identification of 2Θ values at peaks corresponding to constructive interference due to highly structured crystalline phases of material can be a way of confirming presence of a certain compound as well as its crystallinity.

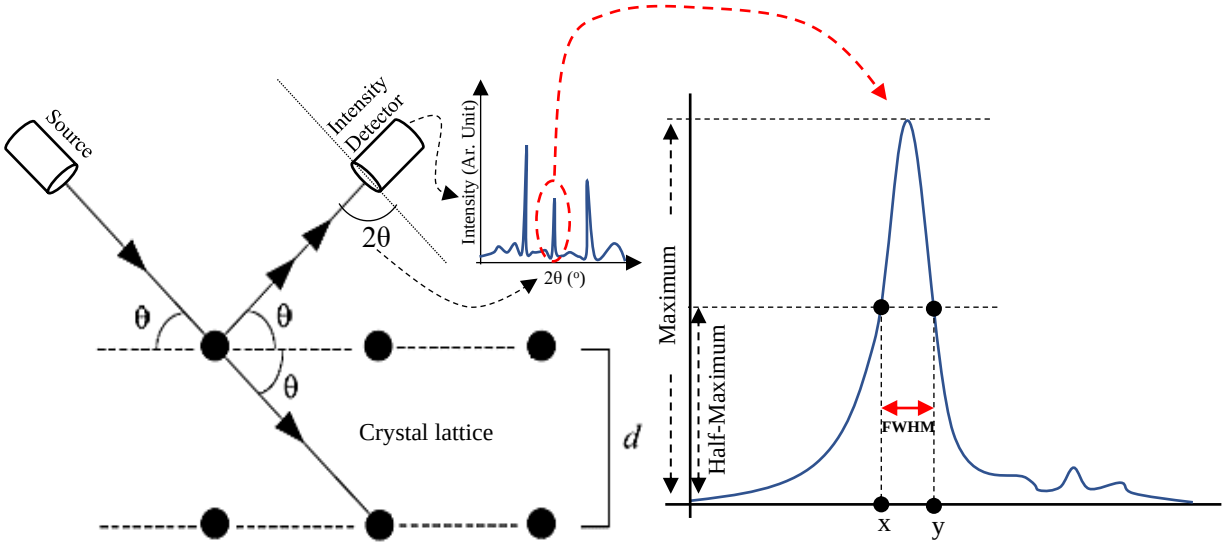


Fig 3.5 Formation of a typical XRD pattern upon X-ray interaction with material crystallite, and inset is the analysis of a typical XRD peak to calculate FWHM

Further information such as crystallite size (D) can also be calculated by analysing the peaks, using Scherrer's equation (eq. 3.4). Where K is a constant (0.94), λ is the X-ray wavelength (Å), β is the full width at half maximum (FWHM) of the diffraction peak in radians (calculated as per the example in figure 3.5 (inset) and θ is the Bragg's angle of incidence.

$$D = \frac{0.94\lambda}{\beta cos\theta} \qquad (3.4)$$

In this work, a Philips PW X'Pert diffractometer has been used with Cu-Kα monochromator having a wavelength of 1.54 Å, where the source tension and current were kept as 40 kV and 40 mA respectively. XRD scans were carried out within a range of 2θ varied from 20º to 70º.

3.3.3 Compositional and chemical analysis

3.3.3.1 Energy Dispersive X-ray (EDX) analysis

EDX spectroscopy is a non-destructive technique of qualitatively identifying the consisting elements present in a material layer and quantitatively measuring the compositional percentages of elements present in it. The technique first took off by the discovery of the phenomenon called 'Characteristic X-ray' by the mathematician turned physicist and later Nobel laureate Professor Charles Glover Barkla. In 1909 he made the discovery that each chemical element can radiate Rontgen rays (X-rays) having properties characteristic of that element [22][23]. If external radiation causes electron vacancies in a shell proximate to the nucleus, electrons from distant shells fill the vacancies by releasing specific packages of energy in form of x-rays, depending on the shell energy difference. This way each element produces a specific spectral pattern of characteristic x-rays while put under external radiation.

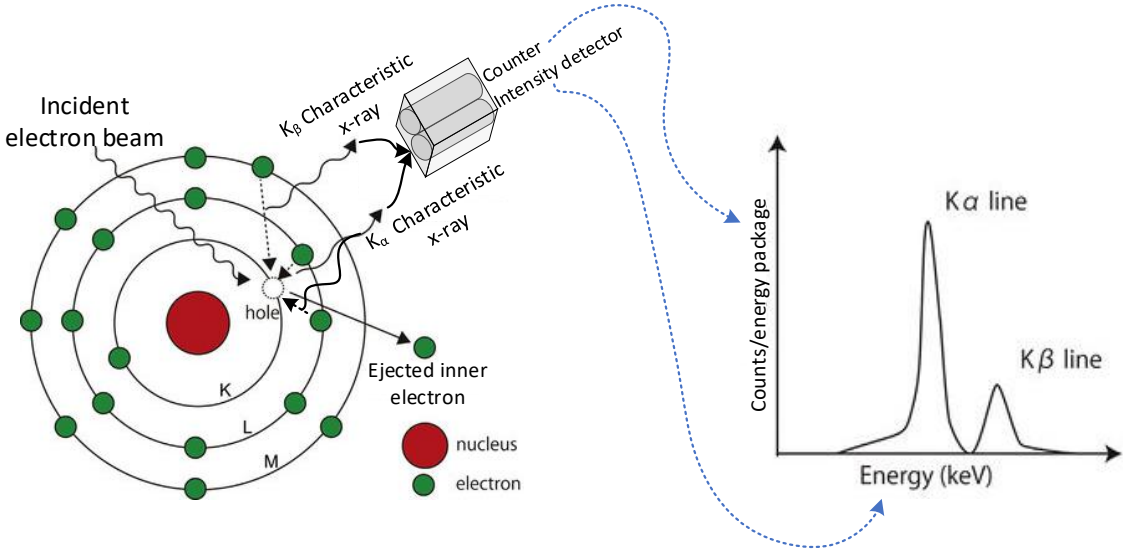


Fig 3.6 Schematic diagram of energy dispersive X-ray spectroscopy (EDX) and formation of a typical EDX spectra

In EDX, an electron gun is focused on the surface of the material layer investigated. The beam of electron knocks off electrons from different inner shells (K, L, M etc) to create vacancies which then accepts electrons from upper energy levels and in that process, the higher energy electrons lose some energy to accommodate themselves in the lower shell vacancy by releasing some energy in the form of characteristic X-ray. Normally the X-rays are emitted from the electrons of inner atomic orbits, therefore the original chemical structure of the material do not break due to the unchanged outer orbits [24]. Now, as shown in the figure 3.6, based on the number of counts per second per energy amount, quantified by the X-ray intensity detector against the energy emission from different atomic energy levels, gives the qualitative idea about the identification of an element being present on a surface. Quantitative analysis which determines the concentrations of the elements present, involves measuring the line intensities for each element in the sample and for the same elements in calibration standards of known composition [25]. EDX is an analysis technique that studies the average bulk composition of the material down to few microns. The overall analytical accuracy is ±2% [24]. Moreover, EDX is incapable of detecting elements lighter than Boron and is subject to overlapping elemental peaks [26].

The EDX spectroscopic analysis carried out in this work has been done using the compositional analysis software associated with the Quanta 650 SEM equipment with a 15.0 kV electron beam voltage.

3.3.3.2 X-ray Photoelectron Spectroscopy (XPS)

XPS is carried out for compositional analysis as well as chemical analysis of a material surface having a possibility of quantitative depth profiling of the sample layer. This technique can often be used for compositional analysis of materials considering the accuracy concerns of EDX technique. First discovered by Heinreich Hartz in 1887, and explained by Albert Einstein in 1905, the Nobel prize winning phenomenon 'Photo-electric effect' lies in the centre of this technique [27], [28].

In case of XPS, the excitation mechanism used is an X-ray beam having known energy (E_P), that breaks photoelectrons away from the nuclear attraction force (E_B) of the element and moves them to the vacuum level (φ) with a certain kinetic energy (E_K). According to the principle of photoelectric effect, equation (3.5) can be written as:

$$E_P = (E_B + \varphi) + E_K \qquad (3.5)$$

Where, E_B is the binding energy of the solid or, the energy necessary to bring an electron from the inner energy states to the surface and φ is the work function of the solid or, the energy necessary to move an electron from the surface to the vacuum level. As depicted in figure 3.7, once these photo-ejected electrons are in the vacuum, they are collected by an electron analyser that measures their kinetic energy (E_K). Hence, from equation 3.5, the energy value of (E_B + φ) can be worked out. Auger electrons produced by the photons emitted due to inner orbital recombination, can also be detected (figure 3.7). Since the work function (φ) of the material surface stays constant, for analytical convenience, an electron energy analyser produces an energy spectrum of photoelectron count (number of photo-ejected electrons/energy package) versus binding energy (E_B). In this spectra, each prominent energy peak corresponds to a specific elemental subshell [29].

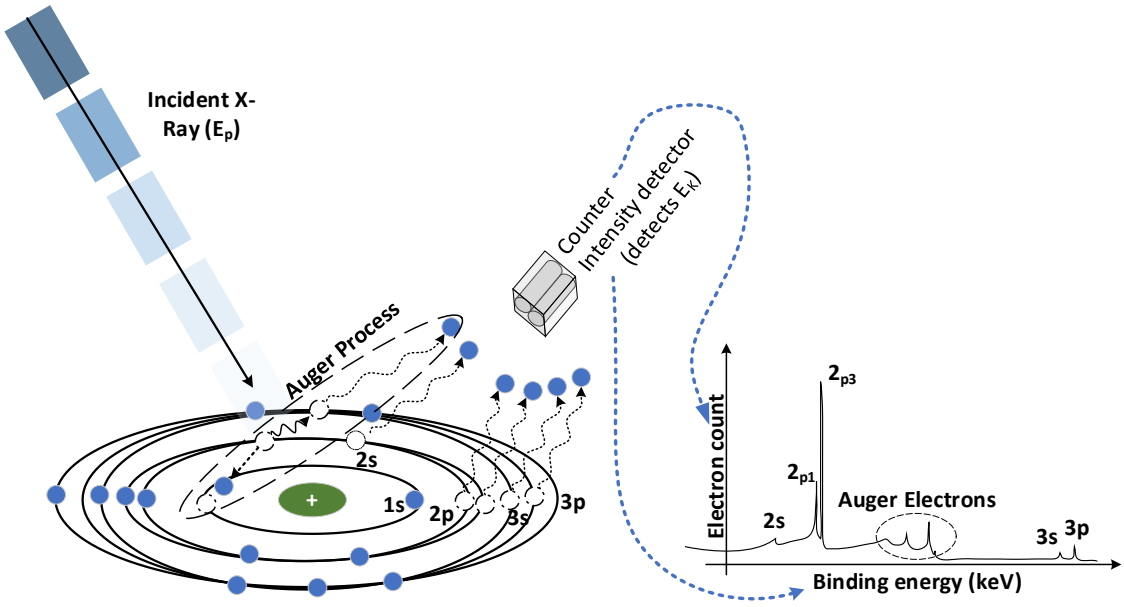


Fig 3.7 Schematic diagram of X-ray photoelectron spectroscopy (XPS) and formation of a typical XPS spectra

XPS spectra can accurately detect surface characteristics by providing following information:

- Elemental identification: The element from which the photoelectrons are emitted

- Chemical characterisation: from which orbital the photoelectrons are emitted
- Chemical shift: Change in binding energy of a core electron of an element due to a change in the chemical bonding of that element. This indicates, from which environment of the atom the photoelectrons are emitted (eg. Qualitative detection of altering oxidised states etc)

XPS analysis of the material surface is highly quantitative unless the bulk composition varies sharply in the outer ~10 nm of the surface. It is a more accurate quantitative technique than EDX if the surface chemistry is the same as the bulk chemistry. Moreover, molecular composition of elements can also be detected by tracking the electrostatic shielding of nuclear charge as a result of changes in bonding at the valence shell. Hydrogen and Helium cannot be detected by XPS technique due to having very small cross-section for photoemission [30]. In this work, a VG Scientific MultiLab 3000 ultra-high vacuum (UHV) surface analysis system equipped with CLAM4 hemispherical analyser and a dual-anode Mg/Al x-ray source has been used for XPS measurements. The equipment is situated at the Conn Centre for Renewable Energy Research, University of Louisville, USA and measurements have been conducted in a collaborative manner while data analysis has been carried out by the author.

3.3.3.3 Sputtered Neutral Mass Spectroscopy (SNMS)

Mass spectrometry is a destructive, high vacuum and very accurate material characterisation technique that is used to identify and investigate the elemental composition of the synthesised thin films. The main job of this instrument is to calculate the mass of a molecule. The most widely used type of mass spectrometer is called Secondary Ion Mass Spectrometer (SIMS) which works generally by bombarding ions of a noble gas on the target film and ejecting secondary ions from the material for investigation [31]. However, while bombarding the primary ions, almost all the time a considerable number of neutral atoms or molecules are also sputtered. In SIMS, these neutral particles remain widely unused. In the late 70s German physicists Oechsner and Stumpe decided to use an additional electron beam to post-ionise these sputtered neutral molecules to carry out mass spectrometry with [32]. This therefore introduced the idea of Sputtered Neutral Mass Spectroscopy (SNMS).

As depicted in figure 3.8, after the post-ionisation of sputtered neutral particles, positive ions are put through an acceleration chamber, where an electric filed (E) and an accelerating magnetic field (B_1) are applied across one another and hence a forward acceleration force gets applied on the positive ions as per the left-hand rule.

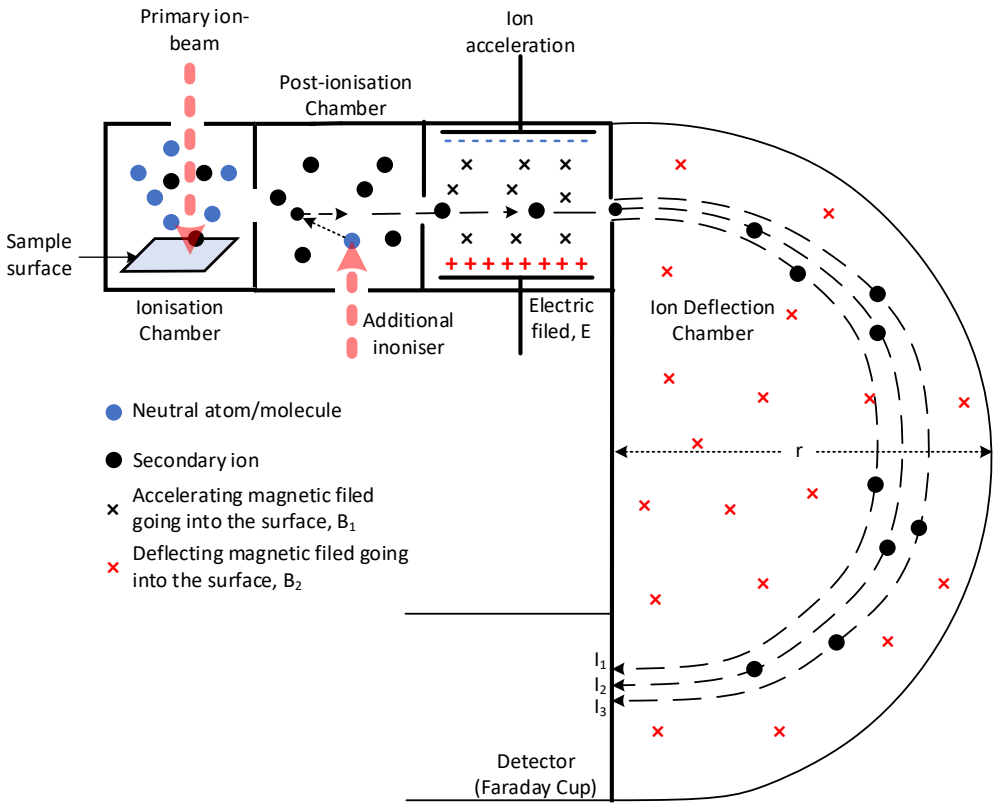


Fig 3.8 Top view of an SNMS instrument along with denoted fields, parameters and basic working principle

These accelerated ions travel in a straight line and enter a semi-circular deflection chamber having a radius of *r*, where there is another magnetic field (B_2) applied. This magnetic field therefore deflects the travelling ions, and their rate of deflection is inversely proportional to their individual masses. After deflection, the ions are then collected by a detector where a Faraday cup is conventionally used to generate a corresponding current (I_1, I_2, I_3 etc) which in turn quantifies the charge (q) of the particle. Using equation 3.6 below, mass (m) of the molecule can then be calculated with great accuracy.

$$m = \frac{\mathrm{qr}B_1B_2}{\mathrm{E}} \qquad (3.6)$$

Mass spectroscopy is a very sensitive technique being able to identify elemental composition down to a ppm level. Therefore, in case the other compositional techniques

fail to identify the presence of any material in the thin film, SNMS can be used [33]. Moreover, SNMS can also conduct depth profiling for material layers quite accurately. In this work, SNMS has been carried out using a HIDEN Secondary Ion Mass Spectroscopy (SIMS) workstation with a beam current of 100 µA and an acceleration voltage of 5 keV.

3.3.4 Optical characterisation

3.3.4.1 UV-Visible Spectrophotometry

Originally invented for estimating vitamin content in US military rations, the Spectrophotometer later became one of the most widely used analytical instruments of all time in various fields of experimental science [34]. In the case of device physics and solar energy research, the spectrophotometer is an essential analytical instrument that is majorly used to investigate the optical properties such as absorbance, transmittance, absorption coefficient, band gap etc. of a thin film. Moreover, absorption data from spectrophotometric study is also helpful for qualitative determination of the material crystallinity.

Spectrophotometry works based on the phenomenon of a certain substance's absorbing capacity of different wavelengths of electromagnetic spectra. As depicted in the figure 3.9, the basic construction outline consists of a monochromator focusing a mono-wavelength light beam having certain intensity (I_o) on the sample held in a sample holder and a detector of the transmitted light that converts the transmitted light into an electrical signal (I_T). As shown in figure 3.9, the ratio between the transmitted intensity of the studied material and that of the base material gives the reciprocal to transmittance (1/T), the logarithm of which gives the value of absorbance (α). From the absorbance data obtained at wavelengths ranging from the beginning of ultra-violet to the end of visible spectra, a Tauc plot of $(\alpha h\nu)^n$ *vs* $h\nu$ can be plotted, where n = 2 for direct bandgap semiconductors and n = ½ for indirect bandgap semiconductors. In this work, all the studied semiconductors are direct bandgap materials and hence n = 2 has been used throughout. An alternative Tauc plot can also be plotted where the square of absorbance (a^2) is plotted against photon energy ($h\nu$). This alternative plotting technique has been tested and verified as accurately comparable to the conventional $(\alpha h\nu)^2$ *vs* $h\nu$ plot [12], [35]. From the resultant curve of the Tauc plot, the intersection of the extrapolated tangent line on the linear part gives the direct band gap (E_g) of the studied semiconductor material. Though this study mainly focused on direct band gap materials, for indirect

semiconductors however, the Tauc plot is plotted as $(\alpha hv)^{1/2}$ *vs hv*. Here, *h* = Planck's constant and *v* = frequency of the incident photon = speed of light in vacuum/ wavelength of incident beam (λ). For direct band gap semiconductors, the slope of the Tauc plot is indicative of the density of the defect states, hence a steeper slope indirectly indicates greater crystallinity and shallower slope indicates lower crystallinity or high structural disorder.

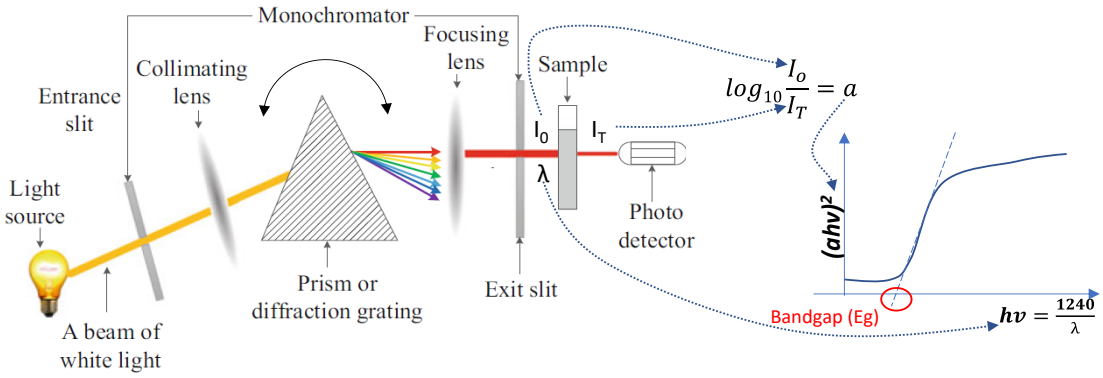


Fig 3.9 Basic instrumentation for UV-Vis spectrophotometer and formation of a typical Tauc Plot for a direct band gap material

In this work a Carry 50 scan UV-Vis spectrophotometer has been used to measure the absorbance data, hence the direct bandgap of the thin-films.

3.3.4.2 Photo-luminescence (PL) study

In PL study, the studied material is excited by an incident photon beam having energy greater than the expected bandgap. The excited electrons therefore get elevated from the valence band to a higher energy levels above the conduction band minimum and then emit energy while returning back to the lower energy levels. Given there are defect states within the forbidden energy region, there can be energy emissions taking place at lower intensity, before the electrons get recombined to the valence band emitting an energy equal to the bandgap energy (E_g). Figure 3.10 depicts the formation of a PL spectra for a typical direct bandgap semiconductor material.

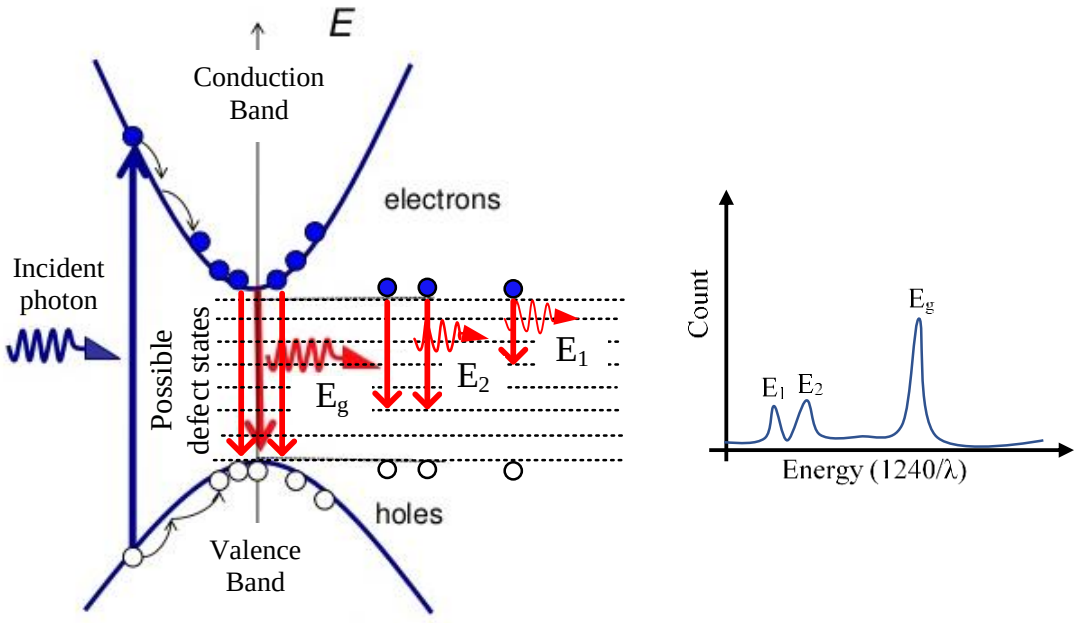


Fig 3.10 Formation of the PL spectra for a typical direct bandgap semiconductor

In this work, PL studies have often been carried out in order to re-confirm the bandgap measured from the optical absorption study as well as to identify possible defect states present in the material. A Renishaw inVia microRaman/PL system (Renishaw, New Mills, UK) has been used in this study and measurements were performed using a HeNe (632 nm) laser, optics with a 1800 diffraction grating, and a charge-coupled device (CCD) camera as a detector. The equipment used is situated at the Conn Centre for Renewable Energy Research, University of Louisville, USA and measurements have been conducted in a collaborative manner while data analysis has been carried out by the author.

3.3.5 Electrical characterisation

3.3.5.1 Photoelectrochemical (PEC) cell measurement

Semiconductor thin films grown by electrodeposition come with some unique sets of challenges when it comes to electrical characterisation. One basic understanding is that, for cathodic electrodeposition, the substrate for semiconductor growth must be conductive to be used as a cathode. The conventional methods of determining the electrical conduction type, or doping type, are the Hall measurement technique and hot-point probe measurement technique [36], [37]. But, due to having a conductive substrate, thin films grown with electrodeposition are not suitable for either of the techniques,

because the underlying conducting layer acts as an alternative low-resistance path for electrons or helps accumulate electrons under heat.

Therefore, Photoelectrochemical (PEC) measurements are carried out to determine the electrical conduction type of electrodeposited layers. This is essentially a qualitative and surface technique of finding the electrical conduction type of semiconductor thin films of conductive substrate. The measurements take the band bending occurred due to the creation of a semiconductor/liquid junction into account, for finding out the direction of charge carriers' flow under illuminated condition. As shown in figure 3.11, Semiconductor/liquid junctions work similarly to Schottky junctions where, E_F is the Fermi level of the semiconductor and E^o_{Redox} is the energy level of the liquid electrolyte [38].

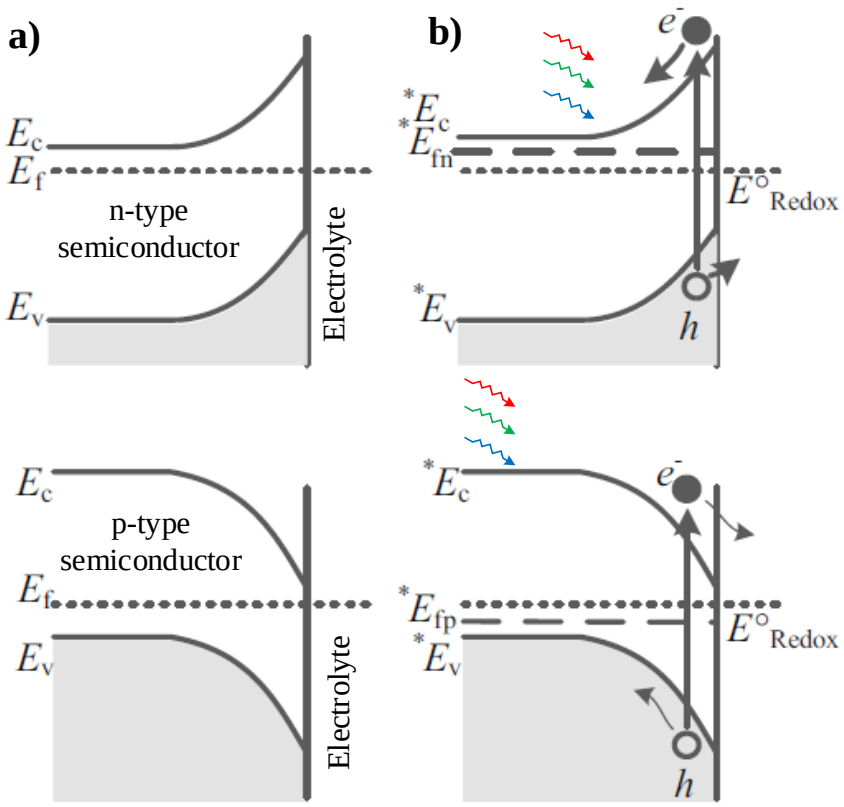


Fig 3.11 Band structure of different semiconductor/electrolyte junctions under **a)** dark and **b)** illuminated condition

By dipping a glass/TCO/semiconductor layer along with another carbon electrode into an electrolyte prepared from 0.1M $Na_2S_2O_3$ (sodium thiosulphate) aqueous solution and measuring the voltage difference between the electrodes under dark (V_D) and illuminated (V_L) condition, the conduction type of the semiconductor layer is determined (figure

3.12). This difference in voltages provides the open circuit voltage of the solid/liquid junction or the PEC signal. For n-type semiconductors the downward band bending at the junction under dark condition enables the photo-generated electrons to flow from the liquid towards the solid and vice-versa for the p-type semiconductors. Therefore, this direction of carrier flow found from the open circuit voltage differences under two conditions ($V_L - V_D$), differentiates the conduction types of the semiconductors. This voltage difference is commonly referred as the PEC signal. The set-up in this work is calibrated using a glass/FTO/CdS sample beforehand, since the conduction type of CdS is always known to be n-type [39]. For n-type layers the PEC signal is negative and for p-type it is positive for the setup used in this work, whereas for metals, insulators and intrinsic semiconductors PEC signal is ideally zero. Moreover, the strength of the PEC signal qualitatively indicates to the doping density and depletion width strength.

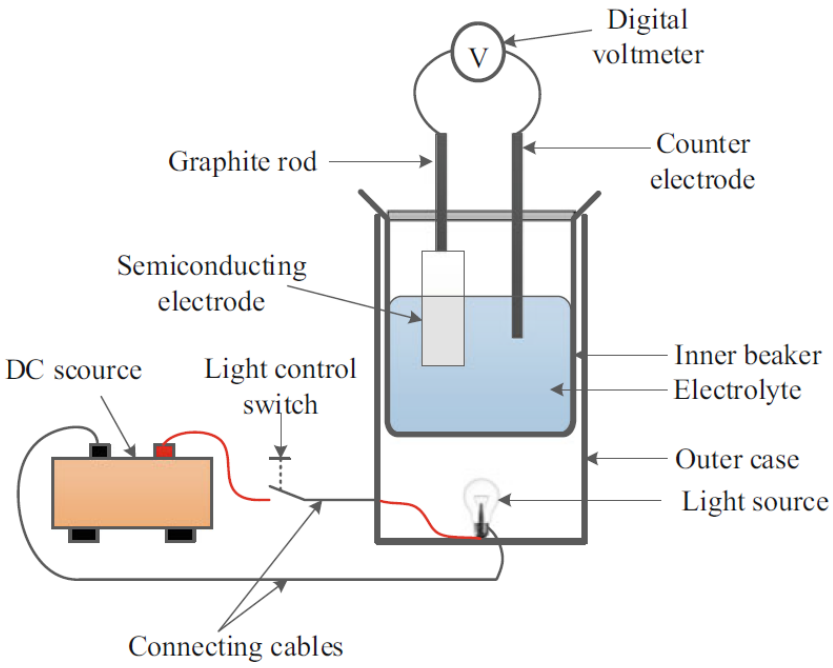


Fig 3.12 Schematic diagram of a typical Photoelectrochemical (PEC) cell measurement instrument setup.

3.3.5.2 Direct Current (DC) conductivity measurement

Electrical conductivity (σ) of the deposited semiconductor layers has been measured by forming a metallic ohmic contact on the semiconductor surface and carrying out DC current-voltage (I-V) measurement within an applied voltage range of -1.00 to 1.00 V. As per figure 3.13 below, the slope of the derived ohmic I-V curve designates the resistance

(R= $\frac{\Delta V}{\Delta I}$) of the path according to Ohm's law, which assists to calculate the conductivity of the semiconductor layer as per equation (3.7):

$$\sigma = \frac{RA}{l} \qquad (3.7)$$

where, l = thickness of the semiconductor film and A = cross-sectional area of the semiconductor = $\pi\ (d/2)^2$, which in this case is the area of ohmic contact formed on the semiconductor.

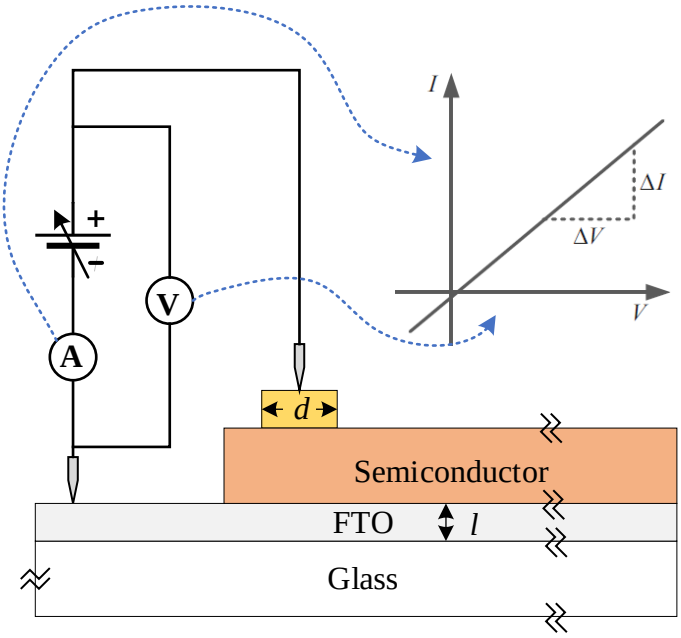


Fig 3.13 DC conductivity measurement set-up and formation of a typical I-V plot under this setup

While forming the ohmic contact for DC conductivity measurement, the metal should be carefully chosen. Hence, the difference between the metal work function and semiconductor electron affinity should not exceed 0.40 eV [9]. In this work the DC conductivity measurements have been carried out using a Keithley 2401 SourceMeter.

3.3.6 Morphological characterisation

For nanomaterials, morphological studies comprise of the study on shape, size and structure of a material surface which may give out important information because, for nanomaterials, morphology often dictates physical properties [40], [41]. Investigation of the morphological properties of the deposited films can be carried out using different microscopy techniques. The major reason behind electron microscopy often being used

for morphological studies is that, compared to light microscopy, electron microscopy offers a much better resolution and magnification factor due to energetic electron beams having small de-Broglie wavelengths.

3.3.6.1 scanning electron microscopy (SEM)

Using scanning electron microscopy (SEM), an electron generated image of the material surface can be derived, as well as estimating the size of the crystallites for crystalline materials. A basic schematic diagram of SEM process, along with possible sample-electron interaction scenarios are presented in figure 3.14 below. A primary electron beam is focused on the sample surface utilising standard magnetic and electronic condenser lenses. This electron beam interacts with the material sample in majorly three ways, creating- a) secondary electrons (SE) from the direct ejection by the primary beam, b) backscattered electrons (BSE) from the rebounding of high energy incident electrons by the atomic nuclei and c) characteristic x-ray as per the mechanism described in section 3.3.3.1. These different interactions take place at different penetration depths. Secondary electrons (SE) are created close to the surface of the sample, therefore, provide most information regarding the morphology of the investigated sample [42], [43].

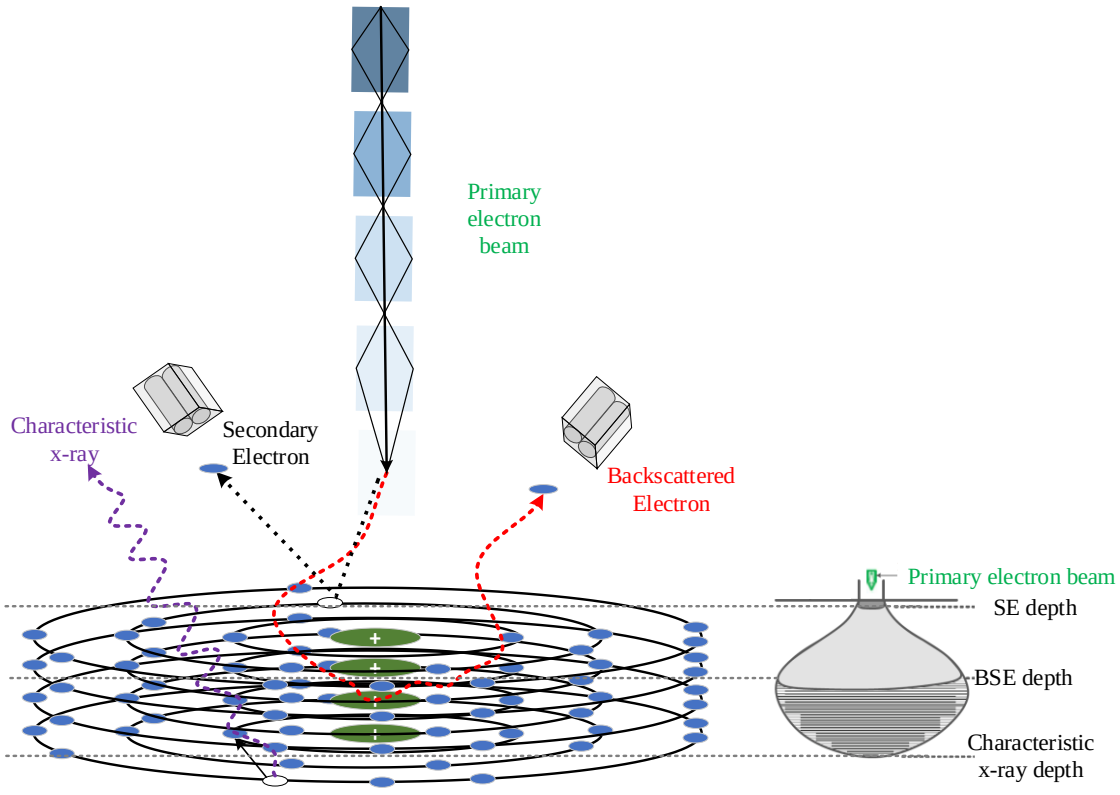


Fig 3.14 A basic schematic diagram of SEM process, along with possible sample-electron interaction scenarios at different penetration depths

In this work, SEM micrographs have been taken using Quanta 650 nano SEM instrument employing 15.0 kV electron beam voltage and 32,000X of magnification. The sample grown on glass/FTO substrates have been thoroughly cleaned and placed on the SEM stub using conducting carbon adhesive. To ensure further conductivity to avoid charging of the sample surface, corners of the samples have been also painted with silver paint.

3.4 Device Characterisation techniques

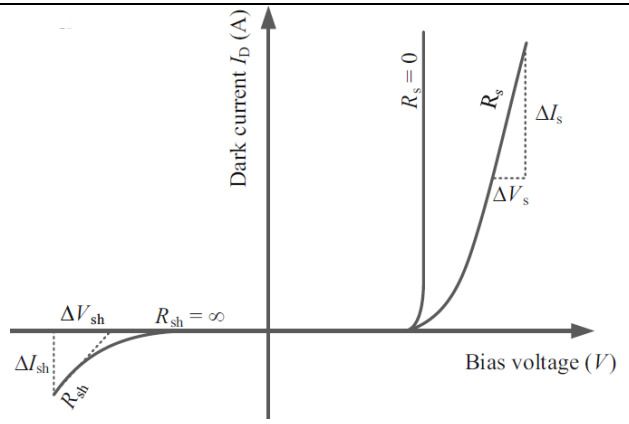
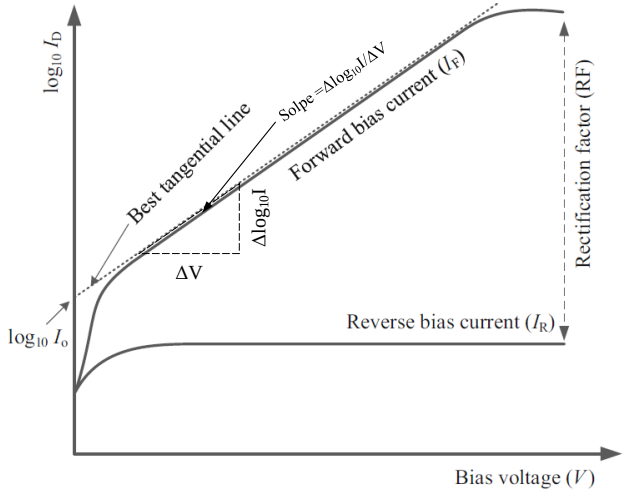
After the structural, compositional, optical, electrical and morphological characterisations are carried out for the electrodeposited semiconductor layers based on the cyclic voltametric assessment, and the optimum growth condition along with necessary post-growth treatment conditions (chloride treatment, annealing temperature, duration, etching conditions etc) are estimated, all the layers are sequentially grown on glass/FTO as per the required device structure. Metallisation of suitable contact material to complete the fabrication process is then carried out. After the device fabrication is complete, the devices are characterised to assess different performance parameters. The main device characterisation techniques executed are, current-voltage (I-V) characterisation and capacitance-voltage (C-V) characterisation.

3.4.1 Current-Voltage (I-V) characterisation

Some important electronic properties of the fabricated solar cells are measured by the help of current-voltage (I-V) characterisation. A bias voltage ranging from -1.00 to 1.00 V is applied and resulting current is measured under dark or illuminated condition. Plotting the retrieved data in different manners, a number of electrical parameters namely, ideality factor (n), saturation current (Io) and potential barrier height (ϕ_b), shunt (Rsh) and series (Rs) resistances, open-circuit voltage (Voc), short-circuit current density (Jsc), fill factor (FF) and conversion efficiency (η) are determined for the device as mentioned by the table 3.1.

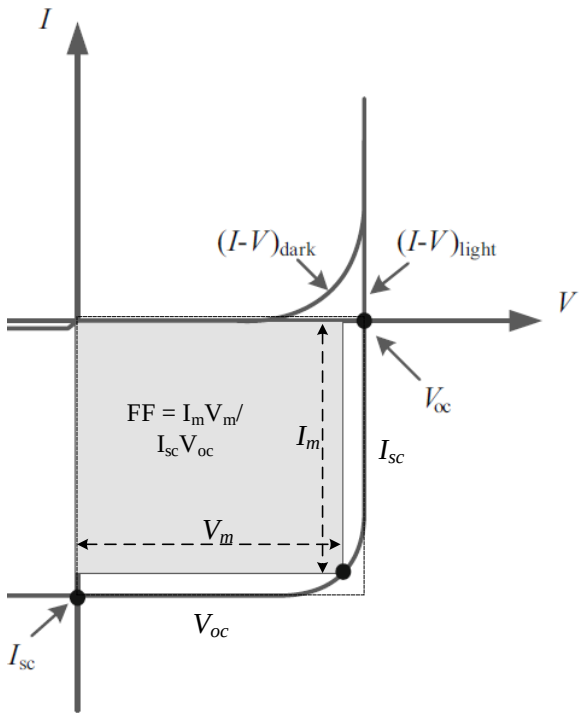
A Rera Solution I-V measurement system has been used in this work to perform I-V characterisation, supported by Keithley 2401 sourcemeter, LOT quantum design GmbH lamp and Rera tracer I-V software. The system is calibrated with a standard monocrystalline silicon solar cell.

Table 3.1 List of electrical properties measured using I-V measurement

Illumination condition	**Plotting condition**	**Measured properties and significance**	**Measurement procedure**
Dark	Linear-Linear	• *Series resistance (R_S)* • *Shunt resistance (R_{SH})*	
	Log-Linear	• *Reverse Saturation current (I_o)* • *Reification factor (RF):* RF $\geq 10^3$ is sufficient for high performance PV devices [9].	

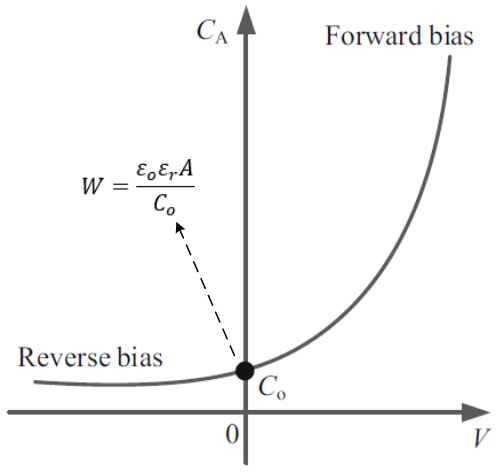
Dark	Log-Linear	• *Ideality factor (n)*	$n \cong \frac{16.78}{slope}$ [12] n = 1.00 means, thermionic emission is the only transport mechanism [44]. n = 2.00 means, recombination and generation (R&G) is the only transport mechanism [44]. 1.00 < n < 2.00 means, both thermionic emission and R&G is taking place [44]. n > 2.00 means, thermionic emission, R&G, tunnelling through barrier height and high series resistance, all are contributing the transport mechanism [45]. n ≤ 2.00 is better for high PV performance [12].
		• Potential barrier height (ϕ_b)	$\phi_b = \frac{kT}{e} \ln \frac{AA^*T^2}{I_0}$ Where, I_0 = Reverse saturation current (A) A = Area of the contact (cm^2) T = Temperature (in Kelvin)

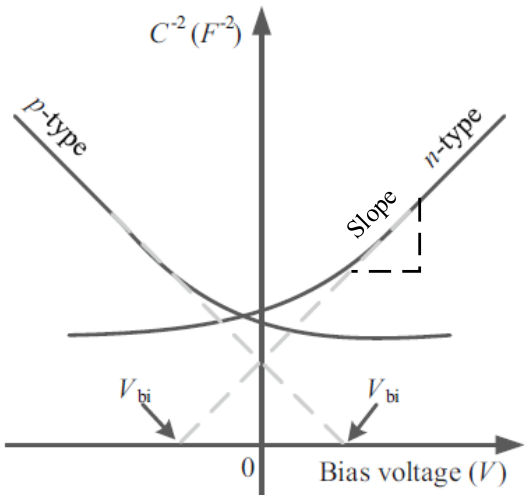
			e = Electronic charge (1.60×10^{-19} C) k = Boltzmann constant (1.38×10^{-23} JK^{-1}) and A^*= Effective Richardson Constant ($Acm^{-2}K^{-2}$) $= \frac{4\pi m^* k^2 q}{h^3}$ where, h = Planck's constant (6.626×10^{-30} cm^2kgs^{-1}) and m*= effective carrier mass **Note:** Effective carrier masses of n-CdTe and p-CdTe are $0.10m_o$ and $0.63m_o$ respectively; where, m_o = Free electron mass (9.1×10^{-31} kg) [46], [47]

1.5 AM illumination	Linear-Linear	• Open-circuit voltage (V_{OC}) • Short-circuit current density ($J_{SC}=I_{SC}/A$) • Fill-factor (FF)	
		Conversion efficiency (η)	$$\eta = \frac{V_{oc} J_{sc} FF}{Power\ Input}$$ where, $J_{sc} = I_{sc}/A$ of the cell Power input (at 1.5 AM) = 1000 Wm^{-2}

3.4.2 Capacitance-Voltage (C-V) characterisation

Since solar cells are combination of semiconductor or Schottky junctions, the junctions can be considered as parallel plate capacitors having the semiconductor material junctions or metal-semiconductor material junctions electrically separated by resistive depletion region [12]. Therefore, capacitance-voltage (C-V) characterisation under dark condition is used to extract several electrical parameters of the device, where capacitance of the device is measured against the applied bias voltage ranging from -1.00 to 1.00 V. Using the data extracted from the C-V setup, and in assistance with the DC conductivity (σ) measured from equation 3.7 above, parameters such as electrical conduction type of the semiconductor (n or p-type), depletion width at zero bias (W), value of Doping concentration (n) of donors (N_D), or acceptors (N_A) and perpendicular carrier mobility ($\mu_\perp$) can be calculated using different plotting conditions. There are mainly two different plotting conditions those are employed. They are- a) capacitance vs voltage (C-V) plot and b) Mott-Schottky plot, which is the reciprocal of the square of capacitance vs bias voltage ($1/C^2$ vs V) plot.

Plotting condition	**Measured parameters**	**Measurement procedure**
C vs V plot	Depletion width (W)	 Here, ε_o = permittivity of free space = 8.85 × 10^{14} Fcm^{-1} ε_r = relative permittivity of semiconductor [eg. CdTe has a ε_r of 11.0, ZnTe has a ε_r of 7.26] [48], [49]

<table>
<tr><td rowspan="3">Mott-Schottky ($1/C^2$ vs V) plot</td><td>Electrical conduction type (n or p-type)</td><td> 
</td></tr>
<tr><td>Doping concentration of n-type (N_D) and p-type (N_A) materials</td><td>$$n = \frac{2}{\varepsilon_0 \varepsilon_r A^2 . slope}$$
Where, A = junction contact area
$n \approx N_A$ when, material is p-type
$n \approx N_D$ when, material is n-type

$n = \sim 1.0 \times 10^{14}$ to 5×10^{15} cm^{-3} has been found to be producing high performance CdTe-based PV cells [50], [51].</td></tr>
<tr><td>Carrier mobility ($\mu_\perp$)</td><td>$$\mu_\perp = \frac{\sigma}{ne}$$
Where, σ = DC conductivity measured by eq. 3.7
e = Electronic charge (1.60×10^{-19} C)</td></tr>
</table>

In this work, C-V measurements and data acquisition have been carried out using a Keithley model 4200-SCS Semiconductor Characterization System at a signal frequency of 1 .0 MHz.

3.4 Conclusion

This chapter has discussed the technical details of the procedures employed in this study, beginning from the fabrication techniques utilised, to the material and device characterisation techniques used to analyse and optimise the individual layer parameters as well as investigating the cell performance. The approach of this chapter was such that, the reader will get an executable working knowledge to be able to follow the descriptions and will have necessary basic ideas to be able to deal with the synthesizing techniques, measurement instruments and analytical procedures. However, this chapter needs to be read in conjunction with chapter 7 to be able to understand the complete device fabrication steps along with procedural details of essential post-growth treatments.

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Chapter 4

Growth and characterisation of potential wide bandgap p-type window layers

4.1 Introduction

Graded bandgap (GBG) multi-layered solar cells are highly promising in designing the next generation solar devices. As discussed in the chapter 3, It has been conceptualised by the Solar energy research group of Sheffield Hallam University (SHU) that, GBG devices can be constructed based on two approaches in terms of the electronic conduction type of the window material; (i) fabricated on n-type window and (ii) fabricated on p-type window. Though the current highest efficiency for CdTe-based GBG solar cells are achieved from n-window devices, cells fabricated on p-type windows have not been tried despite having a theoretical probability to achieve higher performance due to the possibility of producing higher open circuit voltage (V_{oc}) resulted from a higher potential barrier [1], [2]. Therefore, the author now aims to achieve this device structure for CdTe-based low-cost ED solar cells. A prospective device design has been presented in chapter 1.

In order to implement this conceptual solar device, the primary task is to search for a suitable p-type semiconductor material that can be electrodeposited having a bandgap higher than that of the absorber material, which in this case is 1.45 eV of CdTe. Moreover, for the best outcome of the device it is also vital that the material has a reasonable crystallinity along with low or no intermediate defect levels present within the bandgap range for better carrier transport and accurate Fermi level positioning respectively. This chapter discusses about the author's journey in search of the suitable p-type wide bandgap window material. The materials discussed and compared in this chapter are CdTe:Mg, CdMnTe and ZnTe. Therefore, this chapter has been divided into three major sub-chapters namely 4.2, 4.3 and 4.4. Cited reference have been listed at the end of the overall chapter. The rationales behind investigating these materials have also been presented in the latter sections.

Chapter 4.2

Growth and Characterisation of ternary compound: CdTe:Mg

In search of a suitable p-type window layer, Magnesium (Mg) incorporated CdTe (CdTe:Mg), a ternary compound has been grown by Electrodeposition which has a potential to demonstrate a p-type electrical conductivity along with a bandgap higher than that of CdTe [3]. The reason to choose Mg to incorporate to the CdTe layer was mainly that Magnesium Telluride (MgTe) has shown a very small (0.7%) lattice mismatch with CdTe [4], [5]. Moreover, it is a wide bandgap (~3.00 eV) p-type material. Previous works were carried out regarding Mg inclusion to CdTe, mainly using epitaxial growth techniques, where bandgap tuning with the increment of Mg composition has been demonstrated [5]–[7]. This is the first attempt to incorporate Mg to CdTe layers using any electrochemical technique. The aim of this work is to produce a p-type and wide bandgap window material to develop CdTe-based graded bandgap devices as conceptualised.

4.2.1 Experimental procedure

Magnesium (Mg) inclusion to CdTe has been carried out to grow CdTe:Mg layers by gradually increasing the concentration of Mg^{2+} obtained from $MgSO_4$ precursor of 99.5% purity, into a 400 ml aqueous electrolytic solution containing Cd^{2+} obtained from 98% pure cadmium nitrate tetrahydrate ($Cd(NO_3)_2.4H_2O$) precursor and tellurium (Te) precursor prepared from acidic solution of 2 g tellurium dioxide (TeO_2) of 99.99% purity. First, the aqueous electrolyte was prepared from 1.5 M $Cd(NO_3)_2.4H_2O$ and 0.0002 M TeO_2. Then $MgSO_4$ precursor was added gradually at concentration of 10, 20, 30, 50, and 100 ppm, up to very high (50%) Mg incorporation in the bath. Both Mg^{2+} and Cd^{2+} ion precursor solutions were electro-purified before use. All these chemical precursors have been purchased from Sigma-Aldrich Ltd. (UK). The pH and temperature of the solution has been kept constant at 4.00 ± 0.02 and ~ 85^o C, respectively. The pH has been adjusted using either nitric acid or ammonium hydroxide (NH_4OH). Two electrode electrodeposition technique was used for depositing the semiconductor materials on Glass/ TEC-7 fluorine doped tin oxide (glass/FTO) substrates having sheet resistance of ~7 Ω/square. A high purity carbon rod was used as the anode, whereas the cathode (working electrode) was prepared by attaching glass/FTO substrates to carbon rod using insulating polytetrafluoroethylene (PTFE) tape. Prior to electrodeposition, the substrates were cut into 3 cm × 3 cm dimension and rinsed thoroughly with deionized water after

washing with soap solutions using cotton buds. The samples were later dried with nitrogen gas stream. GillAC potentiostat from ACM Instruments is used as the power source for the two-electrode ED system. The electrolytic solution was heated and stirred using a hot plate and magnetic stirrer. Moderate stirring rate has been applied to the bath throughout the electrodeposition process.

Cyclic voltammogram has been carried out to determine an estimated range of deposition potential where association of all the relevant ions (Cd, Te and Mg) take place. The deposited layers were investigated using X-ray diffraction (XRD), scanning electron microscopy (SEM), energy dispersive X-ray (EDX) spectroscopy, and X-ray photoelectron spectroscopy (XPS) for compositional, morphological, and material identification analyses. For characterising and optimising electrical and optical properties of the ED samples, photoelectrochemical (PEC) cell measurements, optical absorption using UV–Vis spectrophotometry and photoluminescence (PL) spectroscopy have been carried out.

4.2.2 Cyclic Voltammetric Study

Cyclic voltammograms were recorded for a 400 ml electrolyte containing Cd^{2+}, Mg^{2+}, and 1 ml of TeO_2 solution. The pH and temperature of the solution is adjusted to 4.00 ± 0.02 and ~85 °C, respectively. The pH value is decided to keep at 4.00 ± 0.02 in order to reduce acidity of the electrolyte to maintain adhesion of the layer. The cyclic voltammogram was recorded with a Gill AC potentiostat from ACM instruments with a sweep rate of 3 mVs^{-1} within the cathodic potential range of 0 mV to 2000 mV. Figure 4.1 depicts a typical voltammogram data plotted with explanatory symbols and legends.

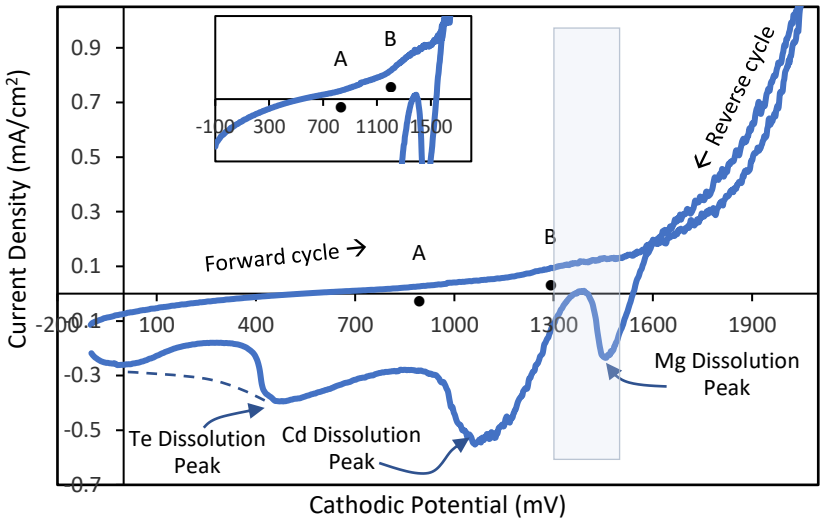


Fig 4.1 Typical cyclic voltammogram of an aqueous solution containing $Cd(NO_3)_2.H_2O$, $MgSO_4$, and TeO_2 as precursors. pH and temperature of the solution was kept at 4.00 ± 0.02 and ~85 °C, respectively.

Due to the difference of redox potentials amongst the consisting ions, in the forward cycle of voltammogram Te having a redox potential (E^o) of +0.593 V (with reference to standard H_2 electrode), starts depositing at the very beginning according to the electrochemical reaction equation 4.1:

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \qquad (4.1)$$

Later, Cd having an E^o of -0.403 V (w.r.t. standard H_2 electrode) starts depositing at ~900 mV (point A in Figure 4.1) according to the electrochemical reaction equation 4.2:

$$Cd^{2+} + 2e^- \rightarrow Cd \qquad (4.2)$$

Hence, the co-deposition of cadmium and tellurium begins hereafter and Te-rich CdTe starts to deposit from ~900 mV onward. As higher cathodic voltage is applied, Cd starts increasingly incorporating to the layer and eventually Cd-rich CdTe deposits [8]. Then, a rise of current density at ~1250 mV (point B in *Figure 4.1*) indicates the inclusion of Mg having an E^o of -2.372 V (w.r.t. standard H_2 electrode), to the deposited CdTe layer according to the electrochemical reaction equation 4.3:

$$Mg^{2+} + 2e^- \rightarrow Mg \qquad (4.3)$$

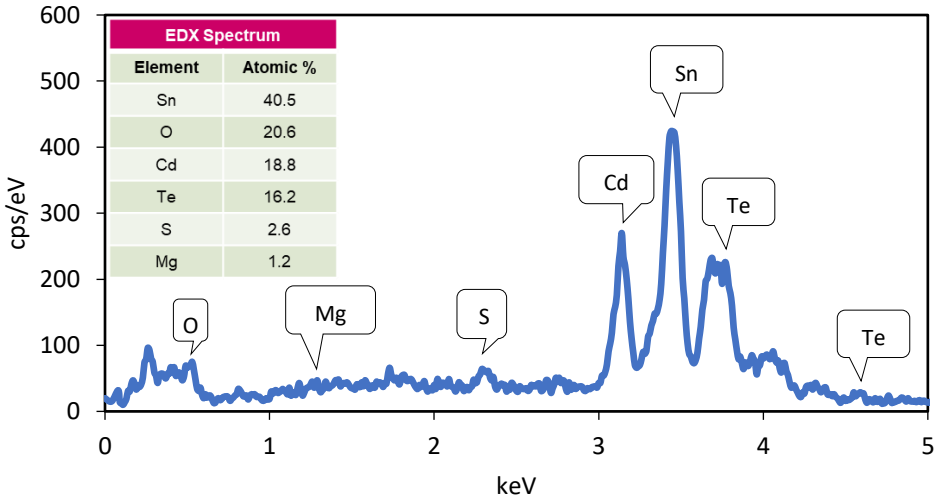
Therefore, from ~1250 mV to ~1500 mV CdTe:Mg growth takes place till the sharp increment of current density after 1500 mV, which indicates a rapid deposition of ions

and possible dissociation of water. Hydrogen creation at lower level can be helpful in reduction of defects using hydrogen passivation; but rapid water splitting can be harmful for good adhesion of the layer due to hydrogen gas bubbles, thus should be avoided.

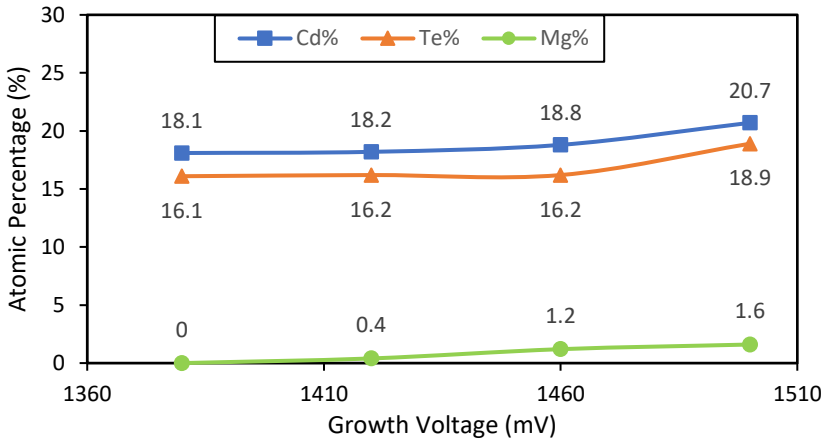
In the reverse cycle of the voltammogram, the dissolution peaks indicate a similar tendency of Mg dissolving first within a range of ~1550 mV to ~1360 mV, Cd dissolving second in the range of ~1350 mV to ~900 mV, and Te dissolving at the very end of the cycle from ~900 mV downwards.

4.2.3 Energy Dispersive X-ray (EDX) Spectroscopy

In order to obtain the chemical composition of the samples, EDX was carried out to the as-deposited CdTe:Mg samples, using the compositional analysis software associated with the Quanta 650 SEM equipment. An EDX spectrum of the layer grown at 1460 mV is presented in the figure 4.2(a). Figure 4.2(b) presents the gradual change of atomic percentage of Cd, Te, and Mg in the as-deposited CdTe:Mg layers grown with high Mg presence in the bath at different cathodic voltages. Despite keeping the accuracy concerns of the EDX technique in mind, this analysis gives a qualitative idea about the gradual increase of Mg inclusion into the Cd-rich CdTe layer with the increment of growth voltage. The phenomenon has been further verified with XPS analysis.



(**a**)



(b)

Fig 4.2 (**a**) EDX spectrum of an as-deposited CdTe:Mg grown at 1460 mV with high Mg presence in the bath and (**b**) gradual inclusion of Mg in the Cd-rich CdTe with increasing growth voltage.

4.2.4 X-Ray Photoelectron Spectroscopy (XPS) Analysis

X-ray photoelectron spectroscopy (XPS) measurements were performed to analyse the surface chemistry of as-deposited and heat-treated films. A VG Scientific MultiLab 3000 ultrahigh vacuum (UHV) surface analysis system, equipped with CLAM4 hemispherical electron energy analyser and a dual-anode Mg/Al X-ray source was used for XPS measurements. All spectra were collected under the base chamber pressure in the low 10^{-8} Torr range using a monochromatic Al K_{α} ($h\nu$ = 1486.6 eV) X-ray radiation. A survey spectrum from 1400 to 0 eV was collected to identify all elements. Additionally, high-resolution spectra of Mg_{1s}, Cd_{3d}, Te_{3d}, and O_{1s} were collected for elemental quantification and a high-resolution spectrum of C_{1s} for binding energy (BE) calibration. All spectra were calibrated using adventitious C_{1s}; C–C peak at 284.5 eV.

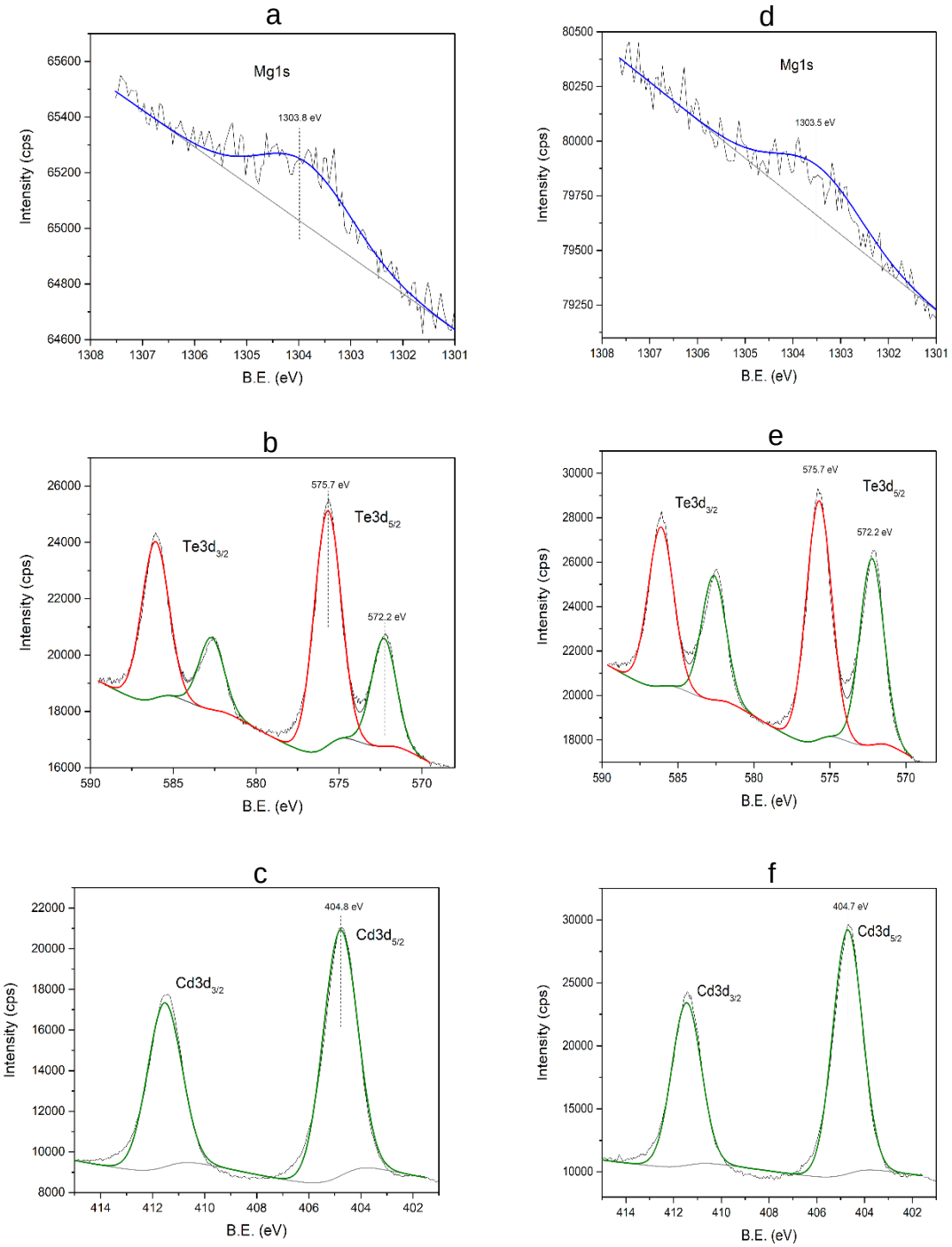


Fig 4.3 High-resolution XPS spectra of Mg1s, Te3d, and Cd3d for as-deposited (**a**–**c**) and heat-treated (**d**–**f**) layers grown at 1400 mV with high Mg presence in the bath.

XPS spectroscopy of CdTe:Mg samples was carried out for as-deposited and heat-treated (HT) layers grown at 1400 mV with high Mg presence in the bath. Figure 3a depicts an XPS peak at a binding energy of ~1303 eV, which corresponds to a typical Mg_{1s} orbital [9]. This peak loses intensity after the sample is heat treated in air for 20 minutes at 400

°C (Fig 4.3d). From Table 4.1 it is further confirmed that the atomic percentage of Mg reduces due to the heat treatment, whereas the Cd and Te percentage increases in the Cd-rich sample after heat treatment.

Figure 4.3b and 4.3e shows the high resolution Te3d peaks for as-deposited and heat-treated CdTe:Mg surface. High binding energy peak component ~3.5 eV away in the doublet clearly shows the oxidised Te on the surface. That can be due to formation of TeO_2 or Cd_xTeO_y on the surface. XRD studies on electroplated CdTe shows peaks related to Cd_xTeO_y [10] and these peaks can be the combination of the two components TeO_2 and/or Cd_xTeO_y. Heat treatment clearly reduces the surface oxygen, indicating the evaporation or sublimation of Te-oxide components from the surface.

The strongest $Cd3d_{5/2}$ peak at 404.8 eV does not show components related to CdO similar to Te. This is mainly because the binding energy of CdO is at 404.6 eV. This does not mean that Cd is not oxidised on the surface but cannot conclude from the XPS results because of the possible overlap of the peaks.

Table 4. 1 Peak intensity and atomic percentages (%) of corresponding elements of CdTe:Mg as-deposited and heat-treated (HT) layers.

Element	**Intensity (A. U.)**		**Atomic Percentage (%)**	
	As-dep	**HT**	**As-dep**	**HT**
Mg	1049	152	1.0	0.1
Cd	41877	64002	22.8	31.6
Te	45281	70033	16.0	22.4
O	12530	10508	60.3	45.9

It should be noted that the atomic percentage of elements, as detected by EDX and XPS, are different. While the EDX is detecting average values for the whole CdTe:Mg layer, the probing depth of XPS is only approximately 2–3 nm on the surface. The bulk compositions can be clearly different to the composition of the elements on the surface due to various reasons, such as evaporation and in-diffusion and out-diffusion of elements near the surface. Reduction of oxygen after heat-treatment indicates the evaporation of

oxides during heating. This also explains the increase in Cd and Te atomic percentage on the surface after heat treatment.

4.2.5 X-Ray Diffraction (XRD) Spectroscopic Analysis

Aim of this analysis is to observe the change of crystallinity in the as-deposited layers of CdTe:Mg with the change of Mg inclusion in the electrolytic bath. XRD spectroscopy has been carried out on five AD samples grown with electrolyte containing 0, 10, 20, and 50 ppm Mg and very high Mg inclusion in the electrolyte. A Philips PW X'Pert diffractometer was used with a Cu-Kα monochromator of wavelength of 1.54 Å, where the source tension and current were kept as 40 kV and 40 mA, respectively. XRD scans were carried out within a range of $2\theta = 20°$ to 70°. All the samples were grown at 1400 mV constant growth potential. Figure 4 shows a clear gradual decrement of the CdTe (111) cubic phase in terms of XRD peak intensity at $2\Theta \approx 23.8°$. Also, another two peaks of cubic CdTe were observed at $2\Theta \approx 38.9°$ and $2\Theta \approx 46.1°$ corresponding to the diffraction from (220) and (311) planes. Moreover, for the samples grown with 10, 20, and 50 ppm Mg in the bath, demonstrate a MgTe phase at $2\Theta \approx 43.1°$ from the (103) hexagonal plane. All these peaks also fade away with the increment of Mg inclusion in the bath.

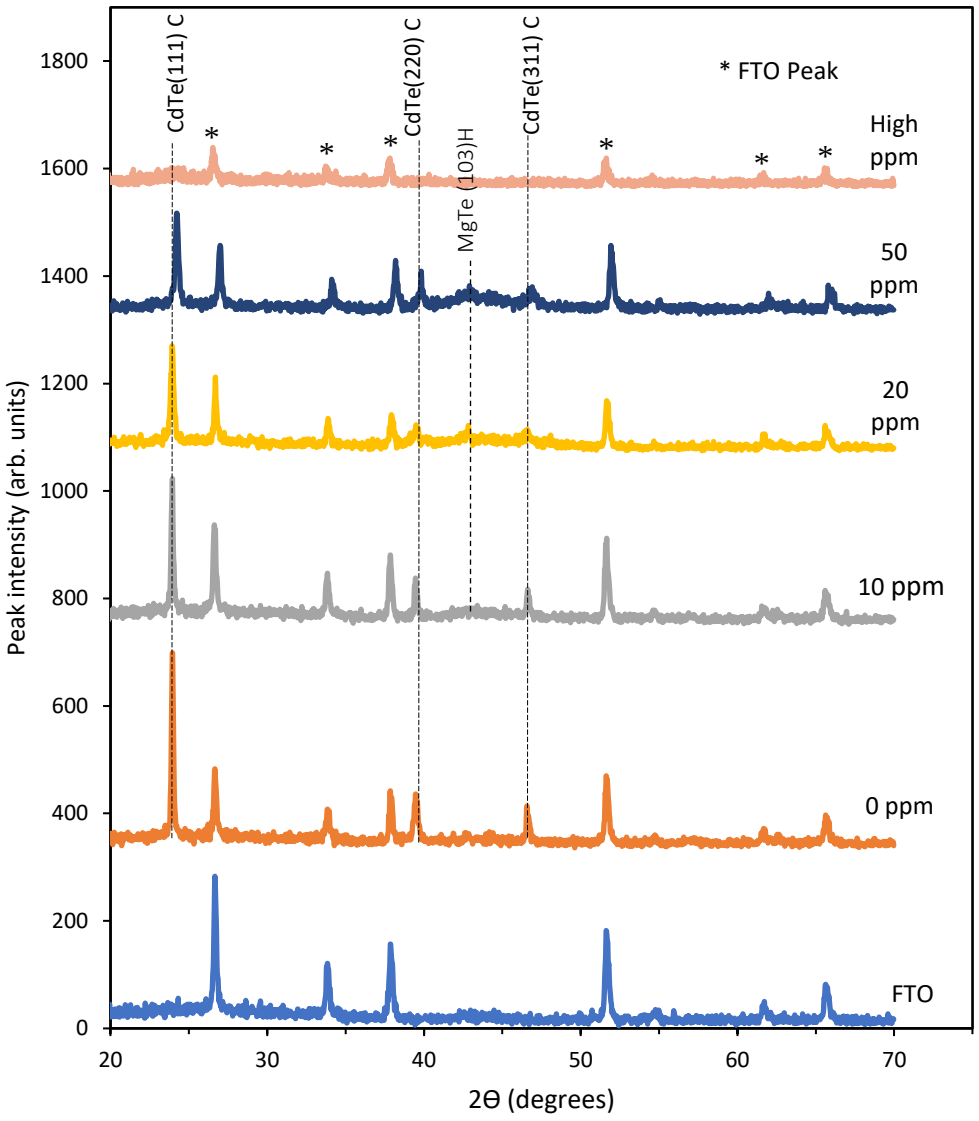


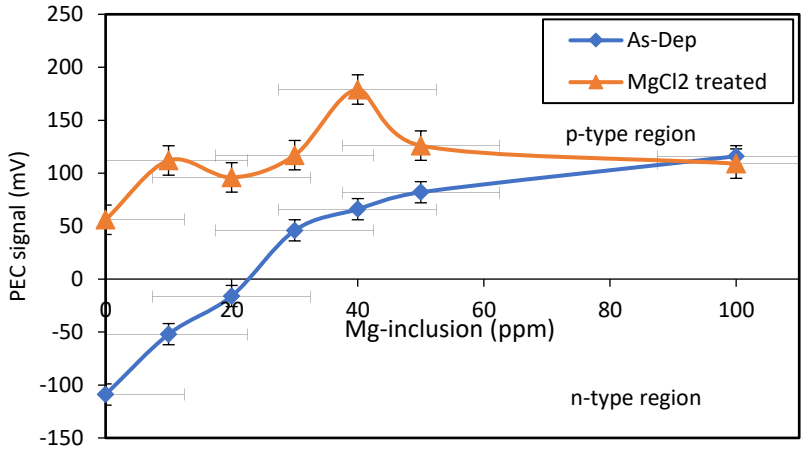
Fig 4.4 Decrement in XRD peak intensity with the increasing amount of Mg inclusion into the n-CdTe bath at ppm level.

Hence it can be assumed that the inclusion of Mg into the CdTe bath contributes not only to the formation of CdTe:Mg but also to some additional MgTe which creates possible defects in the lattice structure. Moreover, this disappearance of crystallinity of the CdTe phases can also be attributed to the competing phases of CdTe and MgTe structures. Since the reported heat of formation for MgTe (−1.08 eV/atom) is more negative than that of CdTe (−0.48 eV/atom), as soon as Mg is added to the CdTe bath, MgTe initiates to form and attempts to break the bonds between Cd and Te [11]. As a result, CdTe:Mg layers become amorphous.

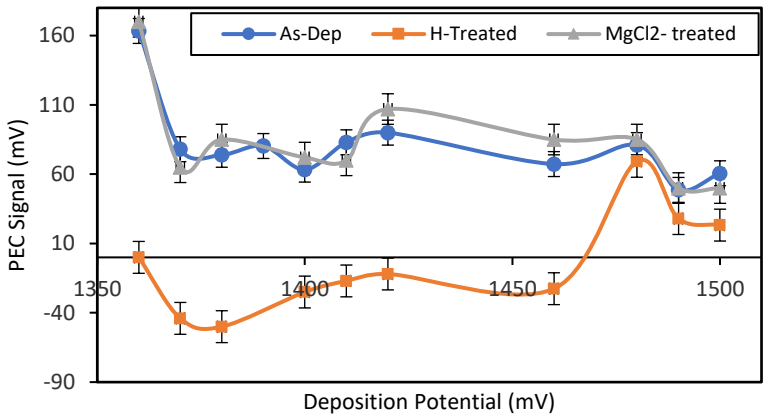
4.2.6 Photoelectrochemical Cell (PEC) Measurement

PEC measurements were carried out to determine the conduction type of ED layers. The measurements take the band bending that occurred due to the creation of a solid/liquid junction into account for finding out the direction of charge carriers' flow under illuminated condition. By dipping a glass/FTO/CdTe:Mg layer along with another carbon electrode into an electrolyte prepared from 0.1M $Na_2S_2O_3$ (sodium thiosulphate) aqueous solution and measuring the voltage difference between the electrodes under dark (V_D) and illuminated (V_L) condition, the conduction type of the semiconductor layer is determined. The above difference in voltages provides the open circuit voltage of the solid/liquid junction or the PEC signal. For n-type semiconductors the downward band bending at the junction under dark condition enables the photogenerated electrons to flow from the liquid towards the solid and vice-versa for the p-type semiconductors. Therefore, this direction of carrier flow found from the open circuit voltage differences under two conditions (V_L–V_D) and differentiates the conduction types of the semiconductors. This voltage difference is commonly referred as the PEC signal. The setup in this work is calibrated using a glass/FTO/CdS sample beforehand, since the conduction type of CdS is always known to be n-type [8]. For n-type layers the PEC signal is negative and for p-type it is positive for the setup used in this work, whereas for metals, insulators and intrinsic semiconductors PEC signal is ideally zero. Moreover, strength of the PEC signal qualitatively indicates to the doping density and depletion layer strength.

In this work, PEC measurements have been taken for as-deposited and $MgCl_2$ treated samples grown with different Mg concentrations in the CdTe bath. Mg inclusion into the bath was executed in parts per million (ppm) level. Voltammetric studies have indicated the possibility of Mg inclusion in the Cd-rich CdTe layer at 1400 mV. Cd richness in the CdTe layer produces a n-type material that is likely to ensure lesser defects than that of its Te-rich p-type counterpart due to less Te precipitation [8], [12], [13]. Therefore, the growth voltage has been kept constant at 1400 mV. All the samples were deposited on glass/FTO for two hours and were cut into two parts where one was kept as-deposited and the other was treated with $MgCl_2$ followed by annealing for 20 minutes at 400^o C in air. In Figure 5a, the PEC signals indicate a transition of conduction type from n to p for as-deposited samples at ~25 ppm of Mg inclusion. $MgCl_2$ treatment (MCT) on the other hand transits the conduction type to p-type for all samples regardless of the Mg incorporation.



(**a**)



(**b**)

Fig 4.5 (**a**) The PEC signal of as-deposited and $MgCl_2$- treated samples grown at 1400 mV with different levels (ppm) of Mg inclusion. (**b**) The PEC signal of as-deposited $MgCl_2$-treated and HT samples grown in a high concentration (~50%) Mg bath at varying cathodic potentials.

Higher Mg inclusion in the bath ensures the conduction type of the as-deposited layers to be p-type. Therefore, to investigate the effect of growth voltage on the layer properties, at a high stationary Mg concentration (~50%) samples were deposited within a range of 1350 mV to 1500 mV for two hours. Each deposited sample was divided into three parts for keeping one as-deposited, one $MgCl_2$ treated and the other heat treated in air at 400 °C for 20 minutes. Figure 5(b) shows the p-type conductivity of all the AD samples, where the heat-treated (in air) samples depict an n-type conduction up to ~1460 mV. Samples deposited at ≥ 1480 mV maintain a p-type conductivity with slightly lower PEC signal

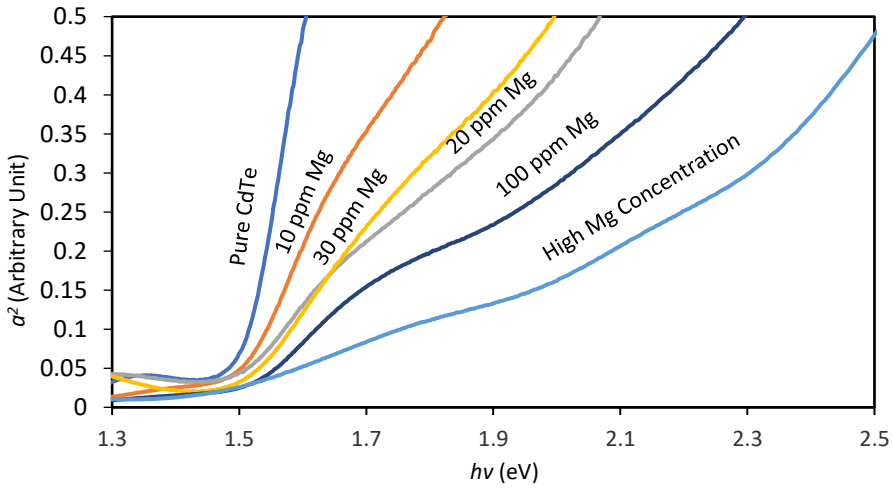
than that of the AD samples. All the points in Figure 5 are the average of three individual measurements.

Though, Mg has a high melting point of 923 °C, but it has been seen to be evaporated at much lower temperature than that of CdTe at approximately 400 °C due to the oxidation of the layer [14]–[16]. The presence of oxygen in the CdTe:Mg layers is clear from both the EDX and XPS outcomes above. Therefore, it can be assumed that sublimation of unreacted Mg due to heat treatment, leaves the CdTe:Mg layers n-type. At higher growth voltage, greater Mg inclusion enables the layers to remain p-type even after some Mg sublimation due to annealing. EDX and XPS analysis has shown a tendency consistent to it. This assumption holds true since all the $MgCl_2$ treated samples stay p-type even after the heat treatment at 400 °C for 20 minutes. This denotes that the treatment not only contributes more Mg to the layer, but also binds the Mg chemically within the structure.

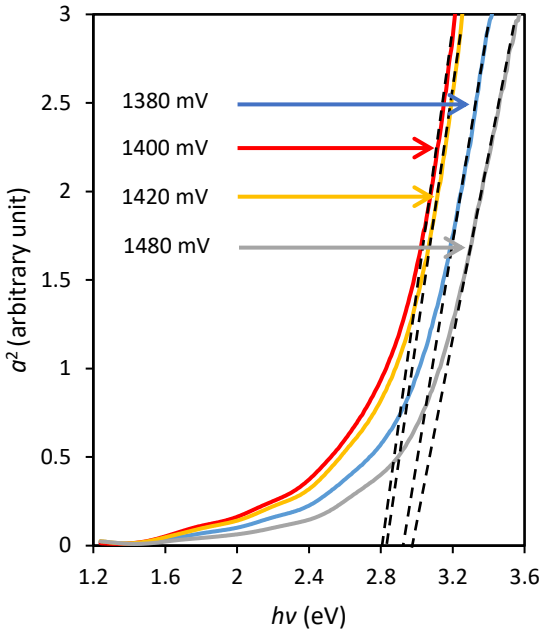
4.2.7 Bandgap Analysis

4.2.7.1 Optical Absorption Analysis

The as-deposited CdTe:Mg layers grown with varying Mg presence in the bath at a constant cathodic voltage of 1400 mV for 2 hours, were investigated for optical absorption studies using Carry 50 scan UV–Vis Spectrophotometer. The optical absorption data collected within the wavelength range of 300 nm to 1000 nm have been used to plot-square of absorbance (a^2) vs photon energy (hv) graph that is frequently used as an alternative to Tauc plot [10], [17]. The curve retrieved from the graph has been used to find the direct band-gap of the deposited material by fitting tangent line to it, extrapolation of which intersects the photon energy at band-gap point.



(a)



(**b**)

Fig 4.6 (**a**) Optical absorption (a^2 vs hv) plot for samples grown at 1400 mV with different amounts of Mg inclusion in the bath. (**b**) a^2 vs hv plot for samples grown at different growth voltages at high constant Mg concentration in the bath.

According to Figure 6a, with the increase of Mg inclusion to the ED bath there appears a gradual disappearance of typical absorption point of CdTe (~1.45 eV) when the growth voltage has been kept constant at 1400 mV. The steepness of the slope at the absorption edge weakens gradually which may indicate a presence of high defect state [17], [18]. The graph also depicts that at a high (~50%) Mg concentration in the bath, the grown layer does not demonstrate any absorption around the typical CdTe absorption point, therefore indicates a change in the band gap energy. Therefore, the absorption spectra of the layers grown at variable cathodic potentials (Vg) from the bath containing high Mg presence were investigated. Figure 6(b) illustrates a higher bandgap of grown layers ranging from ~2.80 to ~2.95 eV. Layers grown at approximately 1400 mV show steeper slopes compared to that of the higher or lower growth voltages.

4.2.7.2 Photoluminescence (PL) Spectroscopic Study

PL spectra were measured using a Renishaw inVia microRaman/PL system. The measurements were performed using a HeNe (632 nm) laser, optics with 1800 diffraction grating, and a CCD camera as a detector.

Figure 4.7 shows the PL spectra obtained for as-deposited and air-annealed CdTe:Mg samples grown with the bath having very high concentration of Mg. Main features of the PL spectra are similar to the PL spectra obtained using the same system and reported in reference [19]. The defect levels available for CdTe layer at T_1 (~0.66 eV), T_2 (~0.76 eV), T_3 (~0.98 eV), and T_4 (~1.39 eV) are observed for the CdTe:Mg samples, together with E_g at ~1.50 eV. The E_g value observed here corresponds to the CdTe phase. The bandgap for MgTe phase could not be observed because of instrumental limitations restricting higher range (2 to 3 eV) measurements. However, the intensity of T1 and T3 peaks have considerably increased for CdTe:Mg samples when compared to CdTe. Despite considering some instrument induced points at these levels, this shows that Mg in CdTe has introduced large number of defects in the layer. The previously reported PL work [16] above showed that $CdCl_2$ treatment reduce these defects. Therefore, when devices are processed with $CdCl_2$ treatment, superior devices will be produced; any inclusion of Mg at this stage will produce lower efficient devices.

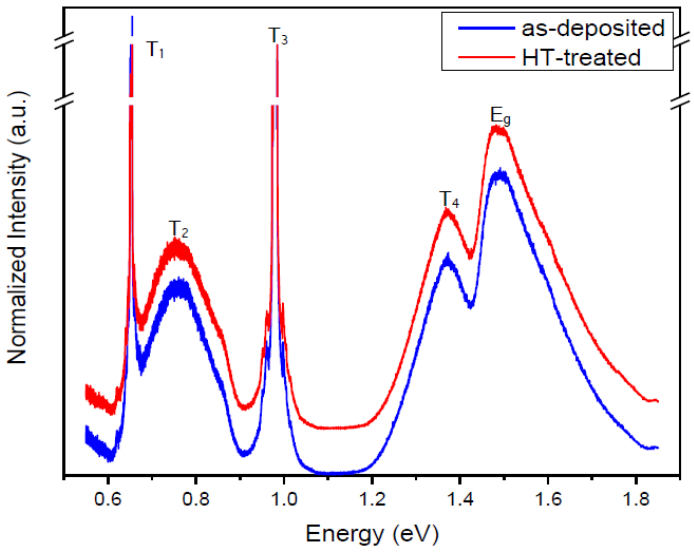
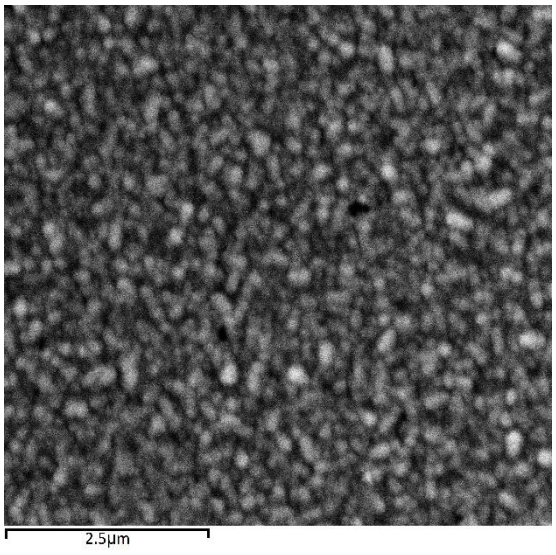


Fig 4.7 PL spectra obtained for as-deposited and heat-treated CdTe:Mg samples within the range of 0.5 eV to 1.9 eV.

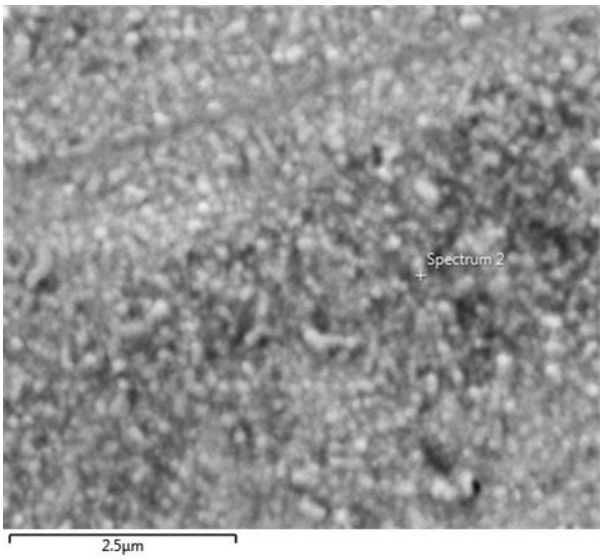
4.2.8 Scanning Electron Microscopy (SEM) Analysis

SEM micrographs of the CdTe:Mg films were analysed with a Quanta 650 nano SEM instrument using 15.0 kV electron beam voltage with magnification of 32,000× for layers grown at different growth potentials. The SEM was carried out to study the morphology and the effects of different Mg inclusion due to the change of cathodic potential for CdTe:Mg films. Figure 8a–c shows SEM images of glass/FTO/CdTe:Mg samples grown at very high Mg presence in the bath at 1360, 1460 and 1420 mV respectively. Figure 4.8 (a) and (b) shows a fairly uniform coverage of glass/FTO that further confirms the amorphous nature of the CdTe:Mg films alongside the XRD outcomes. Though not a clear crystallisation, Figure 8c shows a slight agglomeration of small crystallites clustering together when the film is grown at 1420 mV. The layer was then treated with $MgCl_2$ and annealed for 20 minutes at 400°C, which, as per Figure 8d, contributed to marginally enlarge the clusters but created some pinholes too. This observation is consistent to the previous remarks made in Section 3.6.1 about layers grown at ~1400 mV having steeper absorption edge slope.

(a) 1360 mV



(b) 1460 mV



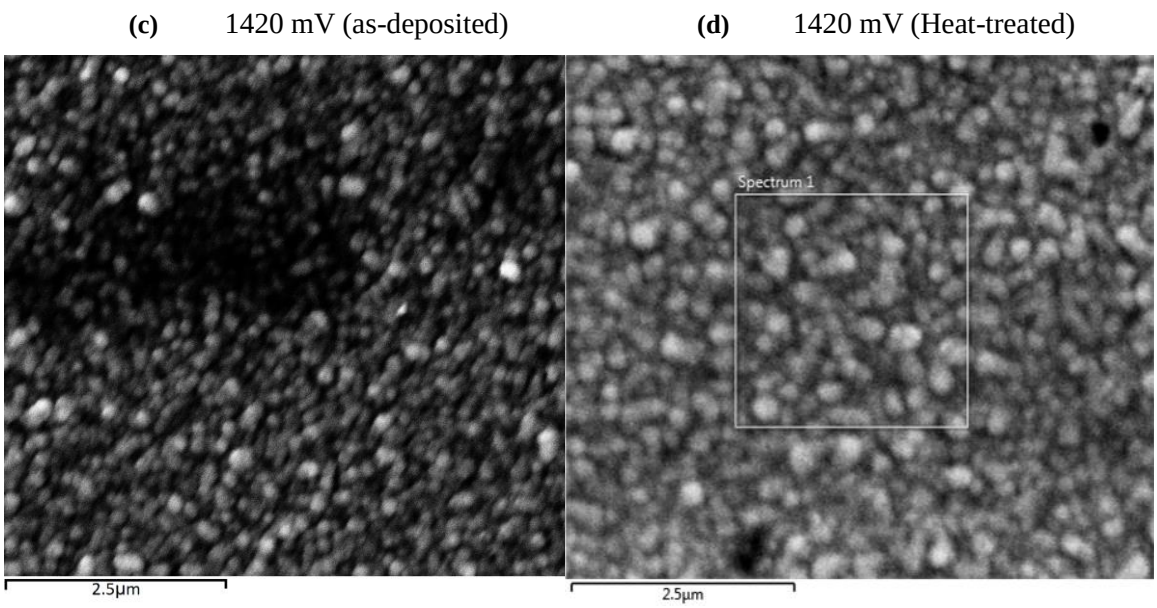


Fig 4.8 Typical SEM images of (**a**–**c**) as-deposited CdTe:Mg thin films grown at (**a**) 1360 mV, (**b**) 1460 mV, (**c**) 1420 mV, and (**d**) $MgCl_2$-treated CdTe:Mg film grown at 1420 mV with high Mg presence in the bath.

4.2.9 Summary of the CdTe:Mg characteristics

The work reported in this chapter leads to draw several conclusions. The main conclusions are the conversion of n-type CdTe layers into p-type CdTe:Mg layers as the Mg is incorporated. Also, bandgap widening has taken place from ~1.50 eV (CdTe) to ~2.85 eV (CdTe:Mg) as expected. However, the structural properties have deteriorated causing the change of polycrystalline CdTe layer into amorphous CdTe:Mg. PL studies show enhancement of defects within the sub-bandgap level after inclusion of Mg into CdTe. The low crystallinity and high defect levels in CdTe:Mg layers certainly reduce the solar cell performance.

Chapter 4.3

Growth and Characterisation of ternary compound: CdMnTe

The CdTe:Mg layers deposited in the previous section, exhibited a dramatic collapse of crystallinity with the incorporation of Mg and have been seen to give rise to an intermediate absorption point at ~1.45 eV which may potentially hamper the barrier height of the device. Hence, the layer lacked all the required properties to be used as the p-window layer of the designed device. This section focuses on incorporating Manganese (Mn) in the CdTe in order to form an electrodeposited ternary compound CdMnTe (CMT) to be used as the p-type window layer for CdTe-based PV cells. Once again, Mn has been chosen to incorporate due to the high lattice matching of MnTe with CdTe [20]. Moreover, CdMnTe is increasingly being used as a suitable material for different electronic applications [21], [22]. This project is however the first effort to electrochemically deposit CdMnTe layers aiming for CdTe-based solar devices.

4.3.1 Experimental Details of CdMnTe electrodeposition

Using GillAC ACM potentiostat, in 2-electrode potentiostatic configuration, CdMnTe ternary compound semiconductor was cathodically electrodeposited on conducting glass substrates. The conducting substrate used in this work is TEC 7 with a sheet resistance of 7 Ω/square. One vital factor which is essential in growing a uniform semiconductor material with proper adherence to the substrate is that the substrate surface must be thoroughly cleaned. To accomplish this, they were washed with soap solutions using cotton buds followed by a further rinsing action using de-ionised water. The surfaces were finally dried under a nitrogen gas flow, before being applied as the working electrode in the electrodeposition (ED) set-up.

The CdMnTe thin films were deposited from electrolyte containing 1.00 M $CdSO_4$ (99.999% purity), 5 ml of dissolved TeO_2 (99.995% purity) and 0.12 M of $MnSO_4$ (99.996% purity) solution in 400 ml of de-ionised water. The dissolved TeO_2 solution was prepared by adding 2 g of TeO_2 powder to 200 ml of de-ionised water. Since TeO_2 cannot dissolve completely in water, 30 ml of concentrated H_2SO_4 was added to the TeO_2 solution to aid its solubility. The prepared TeO_2 solution was subjected to continuous stirring and heating for ~45 minutes so as to obtain a very clear TeO_2 solution devoid of

powder [10]. After preparing 1.00 M of $CdSO_4$ in 400 ml of de-ionised water, it was continuously stirred to ensure dissolution of the chemical. After the dissolution of $CdSO_4$, 5 ml of TeO_2 and 0.12 M of $MnSO_4$ was finally added to the solution to prepare the electrolytic bath. The pH value of the deposition electrolyte was maintained at 2.00±0.02 by using either NH_4OH or H_2SO_4. The growth temperature of the electrolytic bath was ~85^oC and the solution was moderately stirred using a magnetic stirrer.

Before the commencement of CdMnTe layer growth, cyclic voltammetry study was carried out to determine the approximate deposition potential for CdMnTe thin films. The ED- CdMnTe thin films were characterised for their structural properties using X-ray diffraction (XRD) technique. In order to confirm Mn inclusion to the deposited layers, sputtered neutral mass spectrometry (SNMS) measurement has been carried out on a HIDEN Analytical SIMS Workstation utilising a quadrupole mass spectrometer. The electrical conductivity type of the ED-CdMnTe thin films was determined by using photo-electro-chemical (PEC) cell measurements. Scanning electron microscopy (SEM) was used in studying the surface morphology of the electrodeposited CdMnTe thin films. The SEM measurements were carried out by using Quanta 3D FEG NanoSEM equipment. The optical properties of the CdMnTe films were studied using Carry 50 Scan UV-Visible spectrophotometer. In order to confirm the p-type electronic conduction type of the $CdCl_2$ treated CdMnTe layers, both ohmic and rectifying behaviours were explored using Au and Al electrical contacts respectively. Required structures were fabricated using glass/FTO/p-CdMnTe/Au and glass/FTO/p-CdMnTe/Al and measured by using a computerised 619 Electrometer/Multimeter current-voltage (I-V) measurement system (Keithley Instruments Inc., OH, USA).

4.3.2 Cyclic voltammetry

Cyclic voltammetry studies were performed in an aqueous solution that contains 1.00 M $CdSO_4$, 0.12 M $MnSO_4$ and 5.0 ml of dissolved TeO_2 solution at a pH of 2.00±0.02 in 400 ml of de-ionised water. An FTO coated glass substrate was used as the working electrode to study the mechanism of deposition of CdMnTe thin films. A computerised GillAC potentiostat was used to carry out this voltammetric study at a sweep rate of 180 $mVmin^{-1}$. In this technique, a range of cathodic potentials from 0 to 2000 mV was applied across the electrolyte through the electrodes in a two-electrode system. In other words, the FTO working electrode is negative with respect to the carbon electrode. The potentiostat was used in monitoring the current through the electrolyte as the magnitude

of the voltages between electrodes are varied. In the forward cycle, positive ions in the electrolyte receives electrons from the cathode at appropriate voltages to neutralise and deposit on the cathode. During the reverse cycle, at appropriate voltages the deposited layer on the cathode dissolves into the electrolyte donating electrons to the cathode and moving positive ions into the electrolyte. Therefore, the electric current during the reverse cycle is opposite to that of the forward cycle.

The redox potential (E_o) of Te, Cd and Mn are ~+0.59, -0.40 and -1.19 V respectively (with reference to standard H_2 electrode). Since Te shows a more positive redox potential than Cd and Mn, it is therefore expected to deposit first. A typical cyclic voltammogram for FTO-coated glass substrate as cathode in the prepared electrolyte is shown in figure 4.9. The forward curve illustrated at the inset of figure 4.9 shows that Tellurium (Te) begins to deposit at ~300 mV. It has been shown that Te being a more noble element deposits first according to Eqn. (4.4). Cathodic deposition of Te at this voltage range is consistent with our previous works where same precursor for Te has been used at similar concentration [10].

$$HTeO_2^+ + 4e^- + 3H^+ = Te + 2H_2O \qquad (4.4)$$

As shown in figure 4.9 a rise was observed in the forward current density at ~1100 mV (point A), this signifies the initial deposition of Cd on the cathode according to the chemical reaction shown in Eqn. (4.5). At this point the deposition of binary CdTe initiates to take place which is consistent to our previous works on CdTe electrodeposition with sulphate precursor [17].

$$Cd^{2+} + 2e^- = Cd \qquad (4.5)$$

Since the E_o of Cd is more positive than Mn, Cd starts to deposit after Te and before the deposition of Mn. The rise in current density at ~1100 mV reaches its first peak around point B which is at ~1300 mV. At this point, there is the deposition of Mn on the cathode according to Eqn. (4.6).

$$Mn^{2+} + 2e^- = Mn \qquad (4.6)$$

At a cathodic potential above ~1300 mV, there seems to be stability in the forward current density from ~1320 mV to 1450 mV. Within this voltage range, co-deposition of Te, Cd and Mn takes place and hence the CdMnTe semiconductor compound starts to deposit on

the cathode according to the chemical reaction shown in Eqn. (4.7), which is a summation of equation (4.4), (4.5) and (4.6).

$$HTeO_2^+ + 3H^+ + Cd^{2+} + Mn^{2+} + 8e^- = CdMnTe + 2H_2O \qquad (4.7)$$

The rectangular box labelled '**P**' represents the selected voltage range (between ~1300 to ~1560 mV) to grow CdMnTe layers according to this experimental result. Cd-rich CdMnTe materials should grow near the end of this potential range. From the reverse cycle of the I-V curve shown in figure 4.9, the point of transition from the positive current density axis to the negative is ~1450 mV and the negative current reaches its first broad peak at point C. This broad peak indicates the dissolution of both elemental and reacted Mn and Cd from the layer formed on the cathode. The dissolution of Te from the surface of the cathode occurs at the broad peaks labelled D and E. Two broad peaks must be representing two phases of Te, presumably oxidised Te and elemental Te respectively. Thus, cyclic voltammetry technique is a vital tool which helps to determine the approximate growth voltage (V_g) range to deposit CdMnTe thin films. The deposition mechanism of the thin-film layers depending on the varied cathodic voltage and the resultant changes in the layer properties are further explained in section 4.3.6.1.

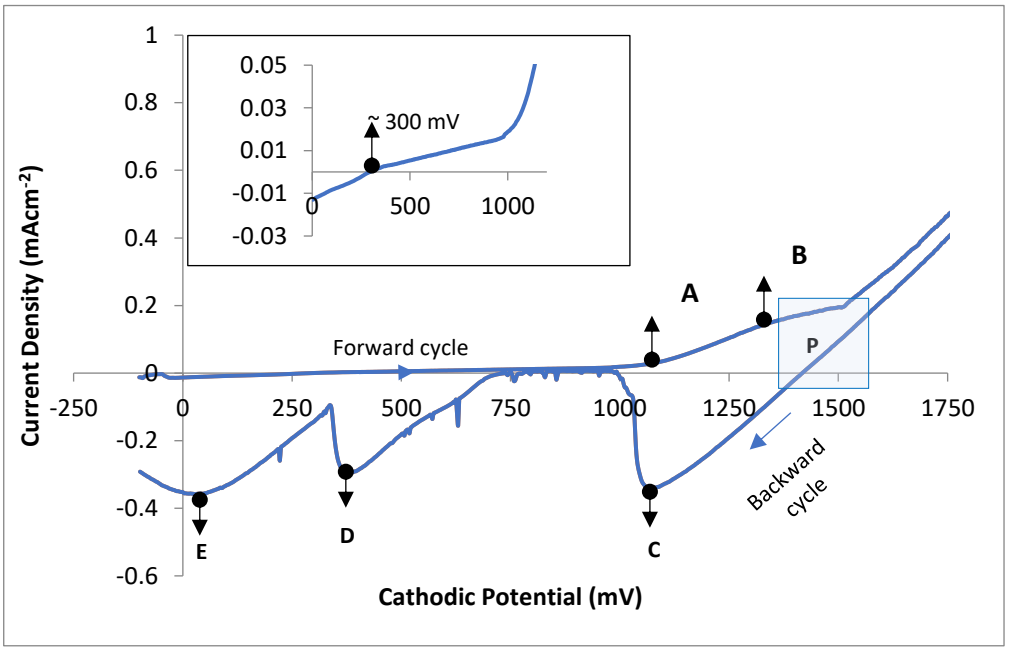
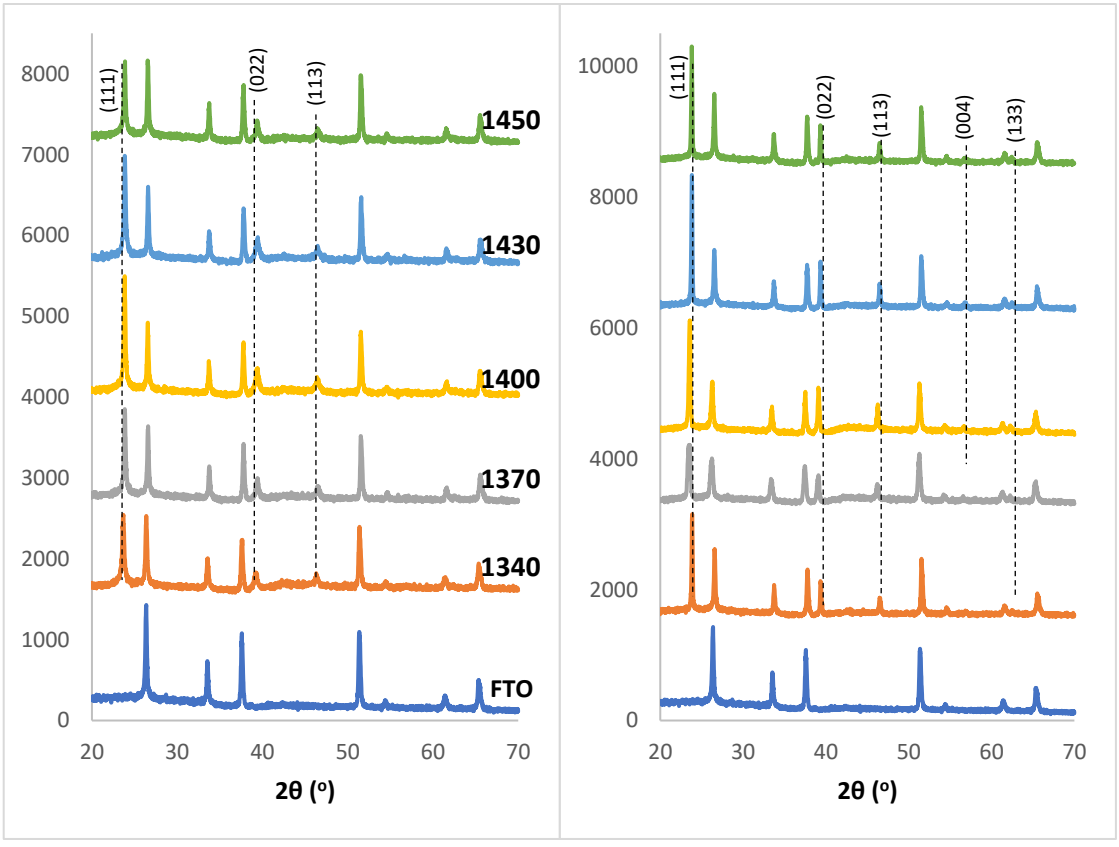


Fig 4.9 Cyclic voltammogram of electrolyte containing 1.00 M $CdSO_4$, 0.12 M $MnSO_4$ and 5.0 ml of dissolved TeO_2 solution (pH = 2.00±0.02, T ~ 85°C). (Inset shows the transition voltage at which Te begins to deposit).

4.3.3 Structural Study using X-Ray Diffraction (XRD) Technique

Structural analysis of the as-deposited (AD) and $CdCl_2$-treated (CCT) CdMnTe layers at different growth voltages were carried out using Philips PW X'Pert Pro diffractometer with a Cu-Kα monochromator having a wavelength of 1.54 Å, where the source tension and current have been kept as 40 kV and 40 mA respectively. XRD spectroscopy has been carried out on AD and CCT samples grown at 1340, 1370, 1400, 1430 and 1450 mV cathodic potentials. Figure 4.10 shows the XRD spectra for both AD and CCT CdMnTe layers grown at different growth voltages. It also shows the XRD pattern of the FTO substrate to aid identification of CdMnTe peaks arising from the layers. Three clear peaks (111), (022) and (113) can be observed for AD-CdMnTe layers showing its polycrystalline nature. In this work, XRD peak identification has been carried out indexing with the ICDD reference file 98-017-4576 for cubic phase.



(a) **(b)**

Fig 4.10 XRD patterns of **(a)** as-deposited and **(b)** $CdCl_2$ treated CdMnTe thin film layers grown at V_g range from 1340 to 1450 mV.

After the heat treatment with $CdCl_2$ at 400°C for 20 minutes in air, peak intensities have increased and two more peaks, (004) and (133) emerged indicating improvement of crystallinity. It is clear that the highest crystallinity is observed when CdMnTe layers are

grown at 1430 mV. This voltage (1430 mV) has been taken as the optimised growth voltage for CdMnTe under the experimental conditions used in this work, and the other characterisations were carried out only on the materials grown at that voltage. Here, it is to be noted that, CdMnTe is a ternary compound having a very similar crystal structure to CdTe; hence the differentiation of the XRD spectra can be impossible at times. Since, the electrodeposition bath has an excess of Cd precursor, and Mn is the most electro-negative element to deposit, CdTe can well be formed alongside CdMnTe. Inclusion of Mn can therefore be considered as a dopant replacing Cd sites, and the deposited layer could consist of a mixture of CdTe and CdMnTe phases. Due to the similarities in their XRD spectra, there can be overlaps of peak intensities too. Compositional and optical studies carried out in later sections have discussed this issue for further clarification.

The layers grown at optimum growth voltage of 1430 mV were tested for two different post-growth treatments, namely $CdCl_2$ treatment (CCT) and $GaCl_3$ treatment (GCT) based on the notion of previous boost of solar-cell performance observed in literature due to these treatments [10]. In both the cases, the treated layers were heated in air for 20 minutes at 400^{o}C. As shown in figure 4.11, the best crystallinity is found for layers treated under CCT conditions.

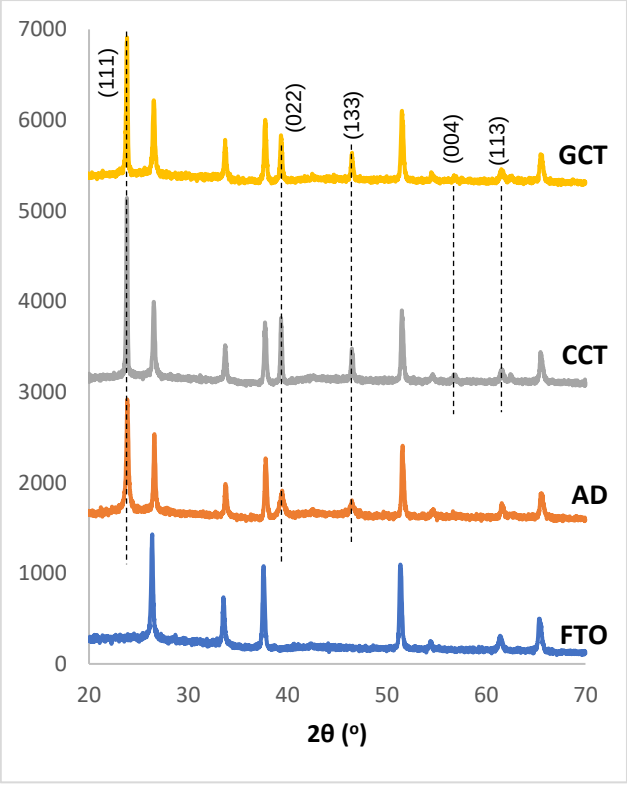


Figure 4.11 XRD spectra of as-deposited (AD), $CdCl_2$-heat treated (CCT) and $GaCl_3$ heat-treated (GCT) CdMnTe layers grown at a cathodic potential of 1430 mV.

4.3.4 Compositional study with sputtered neutral mass spectroscopy (SNMS)

In order to determine the inclusion of Mn in the electroplated layers, standard XPS measurements were carried out. However, these measurements failed to detect any Mn signal, most probably due to the inadequate sensitivity of the measurement instrument in detecting low level of Mn in the layers.

Therefore, to qualitatively demonstrate the inclusion of Mn in the deposited layer, sputtered neutral mass spectroscopy was utilised. Similar to secondary ion mass spectroscopy (SIMS); an Ar ion beam was used to sputter the material layer. An additional ioniser behind the orifice of the mass spectrometer ionises the neutral flux to make it detectable by a mass spectrometer. As the incident angle of the beam is 45° to the sample surface, data was only collected from within a gate area of 100×100 μm^2, to reduce the noise from the sputter trench sidewalls with increasing depth. The total raster area was 800×800 μm^2. The beam parameters were a beam current of 100 μA and an acceleration voltage of 5 keV. In addition to the layer material isotopes (^{55}Mn, ^{114}Cd, ^{130}Te), the tin isotope ^{120}Sn was also measured to identify the beginning of the underlying FTO substrate. The sample that has been used for this study is the CCT-CdMnTe layer grown at 1430 mV cathodic potential. In figure 4.12, it can be seen that in the first minute of the measurement the Ar ion beam remained switched off. The ioniser was in operation to measure the background signal. Once the beam is turned on, all observed isotopes show enhanced signal. After 3 minutes, the Mn signal reaches its maximum, before slowly reducing to the background level upon reaching the substrate. This indicates that Mn is not evenly distributed throughout the layer but concentrated predominantly to the upper levels. Te exhibits an even distribution over the whole layer, while Cd reaches the maximum intensity close to the substrate surface. The tin signal observed during the sputtering of the layer, can be related to holes in the layer exposing the substrate. However, once the substrate surface is reached, the Sn signal intensifies greatly while the layer material signals drop significantly. Due to the thinness of the layer, the sputter trench thickness could not be measured with enough confidence to report the depth. However, the composition of the layer is qualitatively found to be a Cd-rich CdTe layer with some inclusion of Mn into it. This qualitative composition is pertinent to the cyclic voltametric study carried out in section 4.3.2 where co-deposition of Cd, Mn and Te is presumably about to take place in a Cd-rich manner at ~1430 mV cathodic voltage.

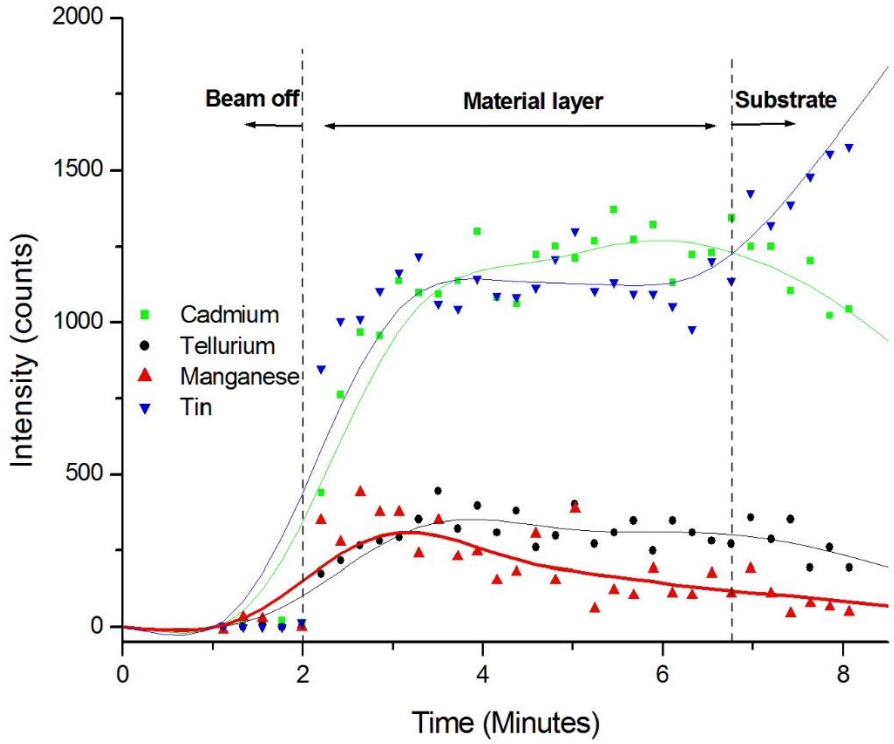
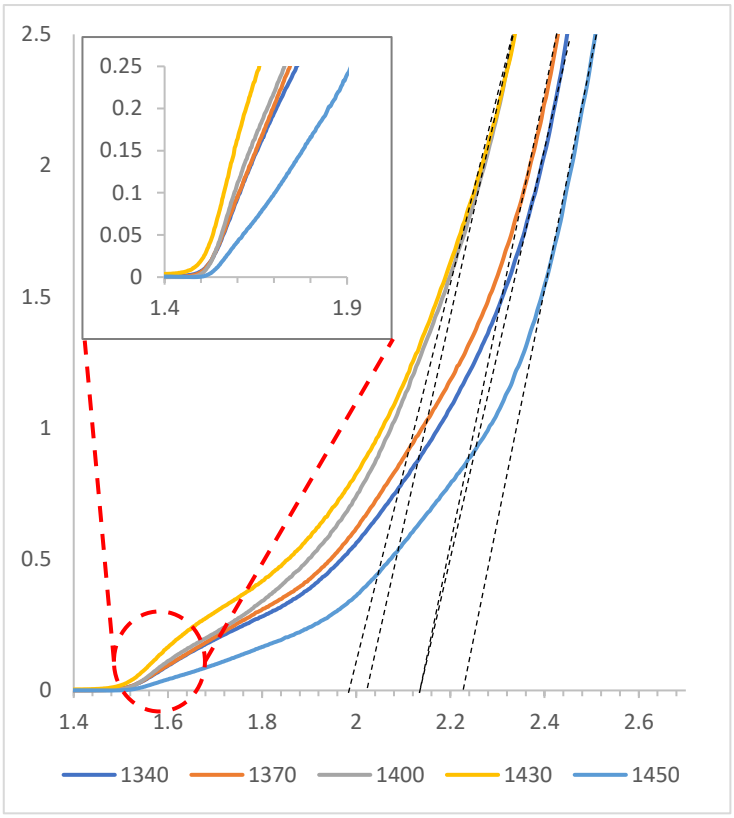


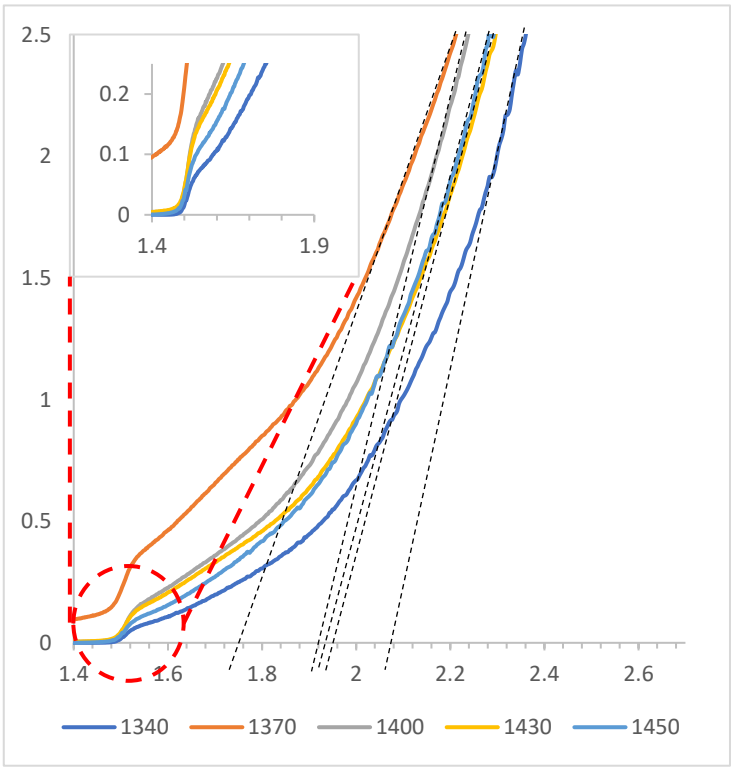
Figure 4.12. Sputtered neutral mass spectra for the $CdCl_2$-treated CdMnTe sample grown at 1430 mV with corresponding 5-points Fast Fourier Transform (FFT) smoothing.

4.3.5 Optical Absorption Study

One key reason of exploring CdMnTe in this work is due to the fact that the energy bandgap of the material is tuneable and wider bandgap than CdTe thin films can be obtained [23]. With the wide bandgap, it can serve the purpose of a p-type CdMnTe layer, to be used as a p-type window material in novel graded bandgap solar cells. Here, the bandgap of the material has been determined using an alternative Tauc plot, where square of absorbance (a^2) is plotted against photon energy (hv) [10]. The intersection of extrapolated tangent line derived from the curve with the hv-axis, gives the direct bandgap (E_g) of the studied semiconductor material. The absorbance data is collected using a Carry 50 scan UV-Vis spectrophotometer within the wavelength of 300 nm to 1000 nm. Figure 4.13 shows the a^2 vs hv plots of CdMnTe layers grown at different cathodic potentials, where bandgap (E_g) values vary between 1.72 eV and 2.22 eV. However, both the AD and CCT samples illustrate a sub-bandgap point (E_{g2}) of absorption for the material at ~930 nm, which matches the typical absorption wavelength of CdTe ($Eg \approx 1.45$ eV). It is also noticeable that post-growth treatments make the intra-bandgap absorption edge sharper. Hence, it can be confirmed that, the XRD spectra found in section 3.2 is contributed by both CdTe and CdMnTe crystals.



(a)



(b)

Figure 4.13 Optical absorption graphs for **(a)** as-deposited (AD) and **(b)** $CdCl_2$-treated CdMnTe layers grown within the range of 1340 to 1450 mV. Inset is the intra-bandgap point of absorption at ~930 nm.

Figure 4.14 shows the a^2 vs hv plot for AD, CCT and GCT layers grown at 1430 mV and the bandgap values produced for these layers are all ~1.95 eV, whereas samples grown at other voltages have shown quite a significant deviation in bandgaps upon post-growth treatment.

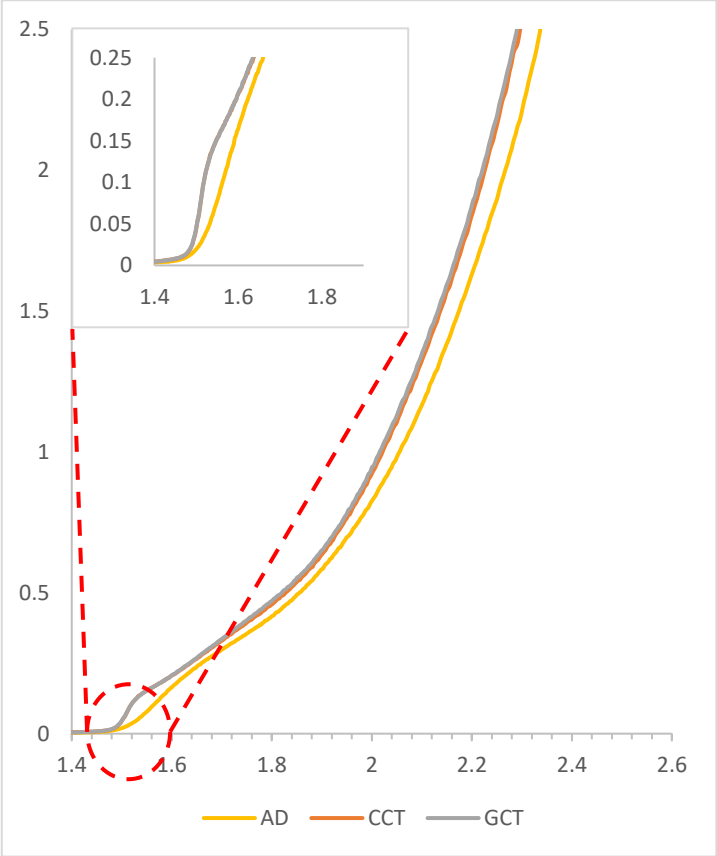


Figure 4.14 Optical absorption graphs for as-deposited (AD), heat-treated (HT) and $CdCl_2$-heat treated CdMnTe layers grown at 1430 mV.

This is further shown in Table 4.2, where it is evident that an overall decrease in the bandgap is observed after post-growth treatment, though bandgap of the materials grown at 1430 mV stayed almost the same regardless of the treatment. This gives an additional confirmation about the optimum quality of the layers grown at 1430 mV.

Table 4.2 Bandgap of the CdMnTe layers electrodeposited at different growth voltage (Vg) and post-growth treatments.

Vg (mV)	AD-CdMnTe	CCT-CdMnTe	GCT-CdMnTe
1340	2.12 ± 0.02 eV	2.05 ± 0.02 eV	-
1370	2.12 ± 0.02 eV	1.72 ± 0.02 eV	-
1400	2.02 ± 0.02 eV	1.92 ± 0.02 eV	1.92 ± 0.02 eV
1430	1.94 ± 0.02 eV	1.96 ± 0.02 eV	1.96 ± 0.02 eV
1450	2.22 ± 0.02 eV	1.94 ± 0.02 eV	2.20 ± 0.02 eV

4.3.6 Electrical properties of CdMnTe Layers

4.3.6.1 PEC Cell Measurement for electrical conductivity type

CdTe on its own shows p-type electrical conductivity when grown with Te-richness [2]. Hence, during electrodeposition, CdTe changes its conduction type from p to n, due to the greater incorporation of cadmium at larger cathodic voltages surpassing Te. Here in figure 4.15 (a), the AD layers change their conductivity type from p to n at ~1330 mV. All the points are the average of three individual measurements. At ~1330 mV the incorporation of Mn is low, consistent to the observation from the cyclic voltammogram in section 4.3.2. The effect of alloying CdTe with Mn on electrical conduction type is visible at ~1370 mV of cathodic potential, as the AD layers show an interesting trend of turning p-type from n-type again. This shows the effect of Mn incorporation in turning the conductivity type of the material to p-type. Comparing the change of conductivity type with the (111) peak intensity in figure 4.15 (b) and bandgap values in figure 4.15 (c) it is observed that, the best crystallinity and most stable bandgap value that indicates the quality of the material is found in the cathodic potential range of 1400 mV to 1430 mV. After the $CdCl_2$ (CCT) and $GaCl_3$ treatment (GCT) all the layers become p-type again and at ~1430 mV the treated layers exhibit the highest preferential peak intensity for (111) plane and a very stable bandgap of ~1.95 eV. The reason layers grown below ~1370 mV before significant Mn inclusion become p-type after CCT can be that, during the chloride treatment, acceptor like defects created near the top of the valence band cause p-type doping on the skin of the polycrystals, and the surface-sensitive nature of PEC picks that up [26, 28, 29]. For the same reason it is commonly observed in literature that p-type PEC signal is obtained even for Cd-rich electrodeposited CCT-CdTe layers [24], [25]. Therefore, to further confirm the conductivity type of the grain interior both ohmic and rectifying behaviours were explored forming Au and Al electrical contacts respectively. However, the acidic nature of $GaCl_3$ treatment leaves the layers grown at lower potentials (than 1370 mV) damaged and hence ineligible for characterisation. Since for the application on CdMnTe as the window layer to the proposed GBG solar cells, conduction type of the layers need to be p-type having reasonable optimised crystallinity with bandgap more than 1.50 eV, CCT-CdMnTe grown at ~1430 mV can be considered as the suitable layer for the purpose.

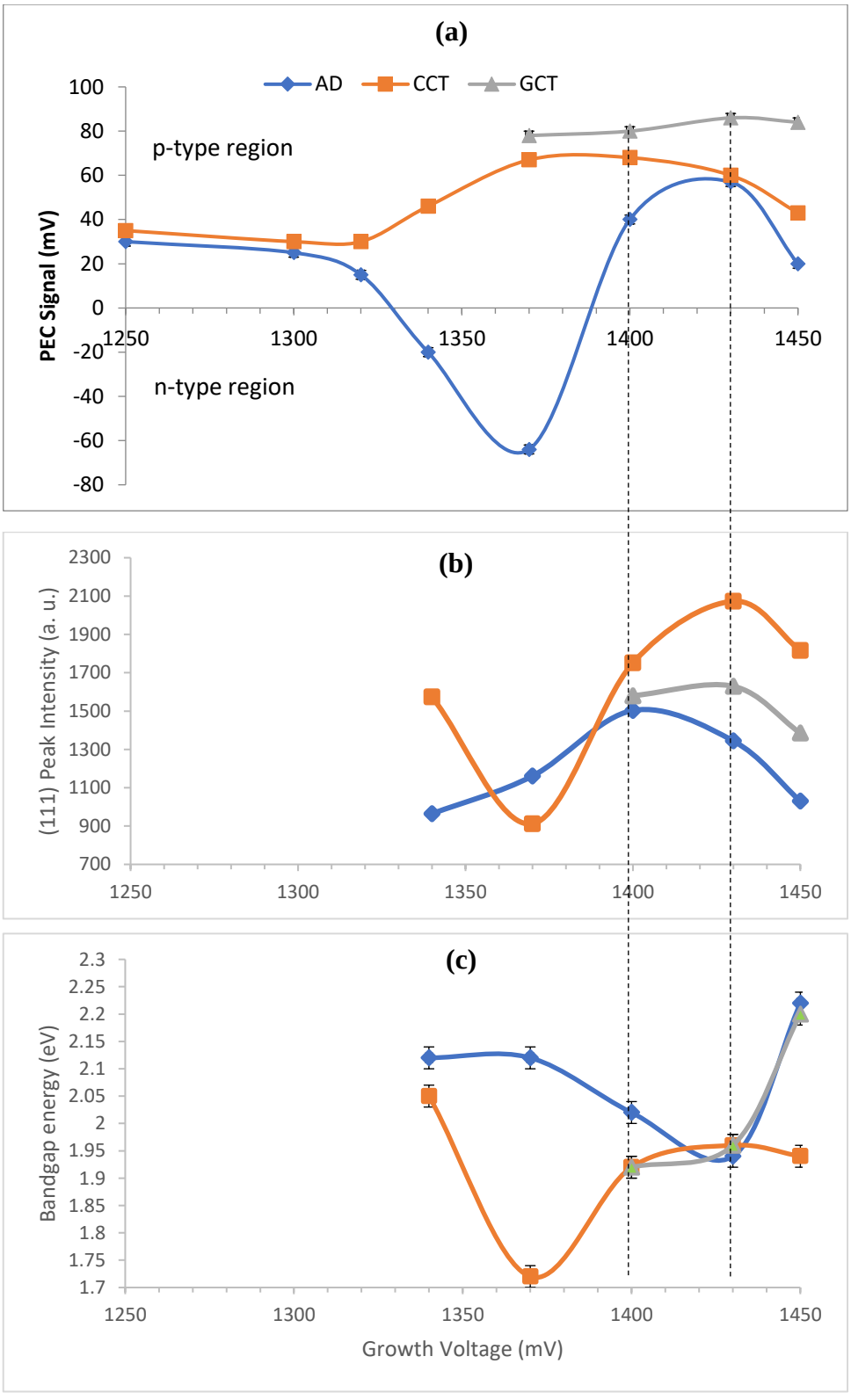


Fig 4.15 Variation of **(a)** PEC signal, **(b)** XRD intensity of (111) peak and **(c)** bandgap energy as a function of cathodic deposition potential for as-deposited (AD), $CdCl_2$-treated (CCT) and $GaCl_3$-treated (GCT) CdMnTe layers grown between 1250 – 1450 mV cathodic potentials.

4.3.6.2 DC conductivity measurement of CdMnTe layers

Since the p-type semiconductors form ohmic contacts with Au when Fermi level pinning is not existent, glass/FTO/p-CdMnTe/Au structures were used to explore their electrical behaviour and estimate DC electrical conductivity. 100 nm thick and 0.20 cm diameter circular Au contacts were sputtered on the optimised samples grown at 1430 mV and $CdCl_2$ treated at different temperatures. For the measurements, the layers were heat treated at 320, 350, 380 and 400^oC for 20 minutes in the presence of $CdCl_2$. All the contacts showed ohmic behaviour in their I-V characteristics. Moreover, in table 4.3 and figure 4.16, effect of temperature in post-growth $CdCl_2$ treatment on the resistivity of the optimised layer has been demonstrated, which shows that $CdCl_2$-annealed samples treated at 400^oC for 20 minutes shows lowest resistivity hence highest electrical conductivity.

Table 4.3 Resistivity and conductivity data of the CdMnTe layers $CdCl_2$-treated at different temperatures.

Sample	Resistivity, ρ (Ωcm)	Conductivity, σ $(\Omega cm)^{-1}$
AD	27.71×10^3	3.61×10^{-5}
CCT320	23.02×10^3	4.34×10^{-5}
CCT350	16.77×10^3	5.96×10^{-5}
CCT380	6.25×10^3	16.01×10^{-5}
CCT400	3.94×10^3	25.36×10^{-5}

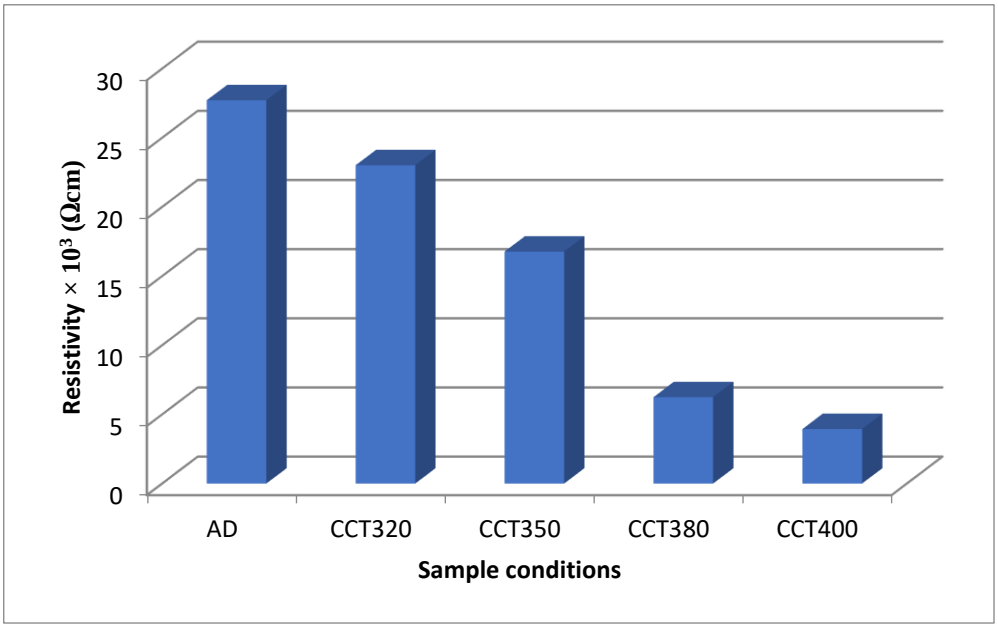
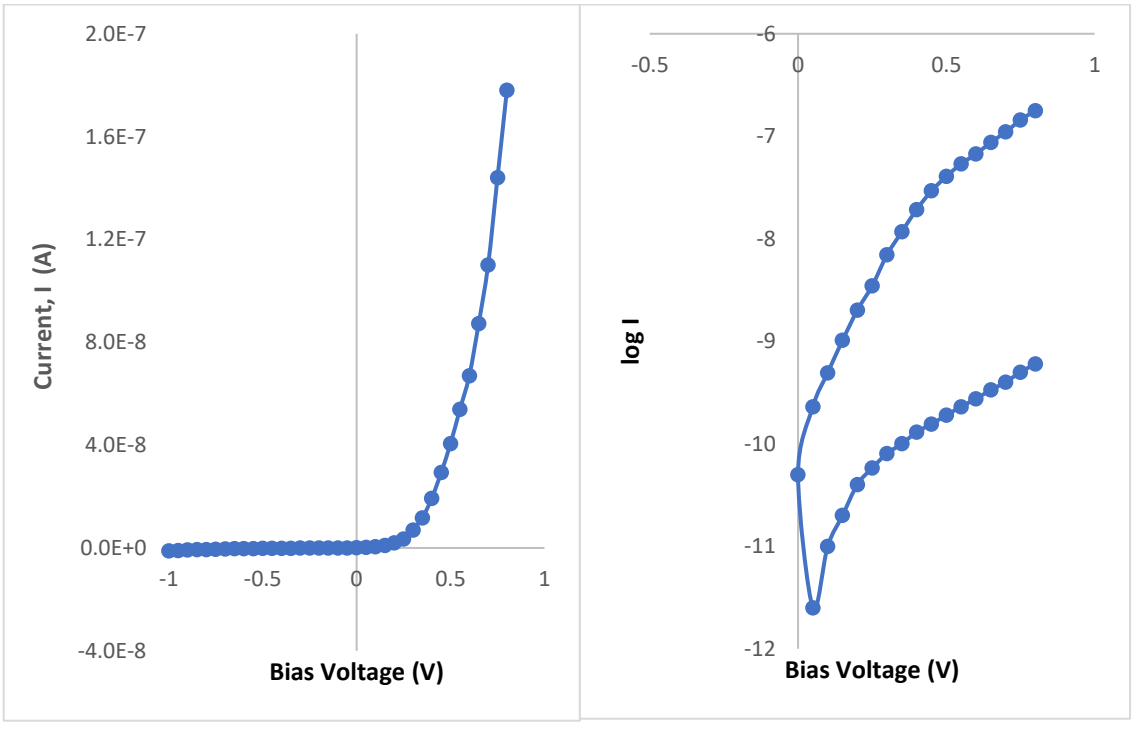


Fig 4.16 Effect of heat-treatment temperature on the resistance of CCT-CdMnTe layers.

4.3.6.3 Rectifying Behaviour of Schottky Diodes Fabricated with CdMnTe layers

In order to further confirm the p-type electrical conduction of CdMnTe layers and to verify their electronic device quality and expected rectifying quality, glass/FTO/p-CdMnTe/Al structures were fabricated and examined. The layer that exhibited highest conductivity in sec 4.3.6.2 has been taken and 2.0 mm diameter circular Al contacts have been made using vacuum evaporation. As expected, p-CdMnTe/Al interface showed rectifying properties and typical dark I-V curves are shown in figure 4.17. With a series resistance (R_s) 1.46 × 10^6 Ω and shunt resistance (R_{sh}) of 2.87 × 10^8 Ω, these Schottky diodes depicted a rectification factor (RF = I_F/I_R) of ~$10^{2.5}$ and an ideality factor (n) of ~1.19. The ideality factor indicates that the current transport mechanism is contributed by thermionic emission as well as recombination and generation (R&G) [26]. The calculated barrier height is ~0.88 eV which indicates to a reasonably good diode characteristic. The measurements demonstrate that, keeping aside the possible itnra-bandgap absorption points present in the layers, electroplated CdMnTe layers after $CdCl_2$ treatment forms rectifying Schottky barriers with Al and is suitable for electronic devices.



(a) **(b)**

Fig 4.17 (a) Linear-linear I-V and **(b)** log-linear I-V characteristics of glass/FTO/p-CdMnTe/Al Schottky diodes under dark condition.

4.3.7 Morphological Study of CdMnTe Layers

In order to carry out the morphological characterisation of the CdMnTe layers, SEM analysis has been done in the form of micrographs with Quanta 3D FEG SEM instrument using 20.0 kV electron beam voltage and 30,000× of magnification. Figure 4.18 (a) is the SEM image of as-deposited CdMnTe layer. The grains exhibit small cauliflower-like nature when compared to $CdCl_2$-heat-treated CdMnTe. Figure 4.18 (b) is the SEM image of $CdCl_2$-annealed CdMnTe layer. Very large grains upto ≈0.80 μm were observed in the layers after the CCT treatment. This shows that agglomeration of crystallites turns into large grains following the CCT treatment.

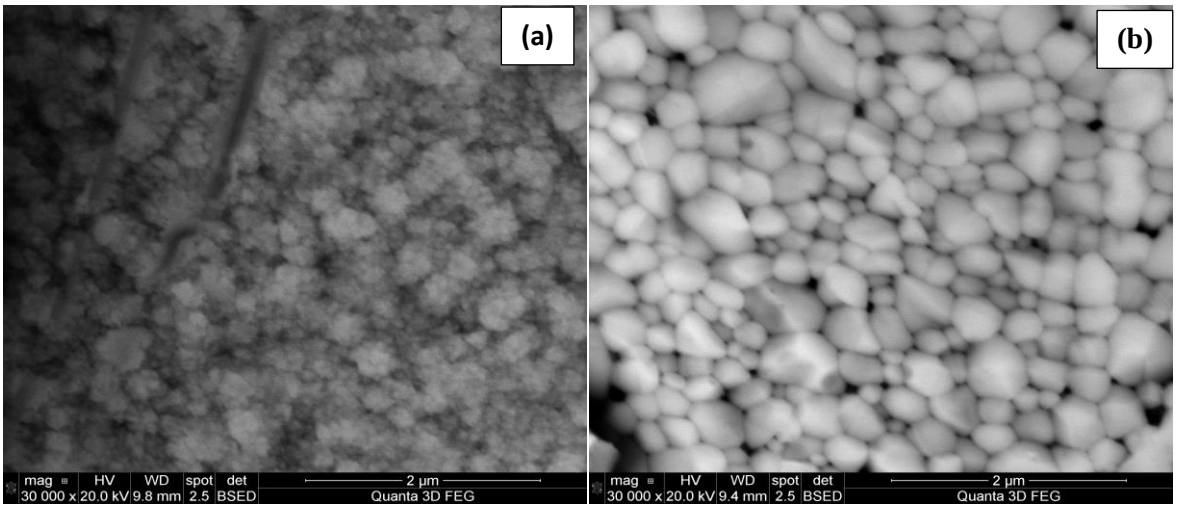


Fig 4.18 SEM micrographs of **(a)** AD-CdMnTe layers and **(b)** CCT-CdMnTe (at 400^{o}C for 20 minutes) layers grown at 1430 mV cathodic potential.

4.3.8 Comparison among the electrodeposited ternary compounds

When compared to the previous work on Mg incorporation in n-CdTe, Mn incorporation seems to have some added advantages. Both Mg and Mn converts n-CdTe layers into p-type layers as required. Bandgap widening also takes place with both Mg (up to ~2.80 eV) and Mn (up to ~2.20 eV) incorporation. However, Mg incorporation tended to reduce the crystallinity and form completely amorphous material layers. On the contrary, Mn kept the required poly-crystalline nature of the layers formed, hence possesses to be more suitable for PV application.

Nevertheless, Photoluminescence (PL) study carried out on the ED CdTe:Mg layers previously showed that, Mg incorporation gives rise to intermediate defect levels though the optical absorption studies showed disappearance of typical CdTe absorption point

(~1.45 eV) and widening of the material bandgap (~2.80 eV) [27]. On the other hand, electrodeposited CdMnTe layers clearly show mixed phases in the optical absorption study (sec 4.3.5), hence this intermediate absorption point at ~1.45 eV has a strong possibility to act as a defect state.

The formation of ohmic contacts with high work function Au, and rectifying contacts with low work function Al, confirms the p-type electrical conduction of CdMnTe layers, and absence of Fermi level pinning at p-CdMnTe/Metal interface.

However, it should be noted that, unlike the other electrodeposited binary semiconductors, both CdTe:Mg and CdMnTe are electrodeposited ternary compounds and hence have a possibility to form mixed phased material which itself may come with additional pros and cons.

4.3.9 Conclusion

The work carried out in this project focused on exploring electrodeposited CdMnTe thin films to use in novel graded bandgap multilayer solar cells based on p-type window materials. The work presented demonstrated for the first time that, Mn can be electrochemically incorporated into poly-crystalline CdTe successfully at a very low level. This Mn incorporation converts the n-CdTe layers into p-type CdMnTe layers with a wide bandgap of ~1.95 eV. Schottky barrier study carried out on the layers exhibits expected electrical properties and confirms the change in electrical conduction. However, the material shows mixed phased characteristic in optical absorption study, which is commonly exhibited in ternary compound previously electrodeposited for the same purpose, hence possesses a specific risk of detrimental Fermi level pinning.

Chapter 4.4

Growth and Characterisation of binary compound: ZnTe

While electrochemically growing wide bandgap p-type ternary compounds having possible lattice matching with CdTe, several issues those can be deemed detrimental for the device performance have been observed. One major issue is the possibility of developing a multiphase material with with two bandgaps presents, hence has the possibility of intra-bandgap absorption that may lower the barrier height, where the major reason to aim for p-window-based approach is increasing it. Therefore, to find a better candidate for this purpose a binary compound is explored based on the idea that, unlike ternary compounds it has negligible chance of adding any intra-bandgap absorption point by developing any additional material phase.

Although having a lower lattice matching with CdTe, compared to the previously explored electrodeposited ternary compounds, Zinc Telluride (ZnTe) has become a promising material in recent times [28]. First Solar uses ZnTe as a high bandgap p-type back layer for their commercial cells [29]. Not just as back layers, ZnTe has also shown promise as a p-type window material in hetero-junction solar cells fabricated with chalcogenide semiconductors such as CdS and CdSe [30], [31]. Moreover, elemental Zn is an earth abundant material, therefore very affordable and ZnTe compound is a non-toxic material, hence it holds probability to reduce the use of Cd amount from the cells.

ZnTe has been synthesized using many different techniques such as, Sputtering, Close Spaced Sublimation (CSS), Chemical Vapour Deposition (CVD), electrodeposition etc [32]–[36]. ZnTe mostly appears in p-type electrical conductivity, therefore efforts have been made to extrinsically dope ZnTe for n-type conversion [37], [38]. However, Electrodeposition being one of the few techniques that allows a fair control over the composition of the deposited layers, Olusola et al. have demonstrated growth of both p-type and n-type ZnTe from the same electrodeposition bath using $ZnSO_4.7H_2O$ as Zn precursor whereas and TeO_2 solution as Tellurium precursor [35]. In this work, ZnTe thin-films have been cathodically electrodeposited using slightly different precursors and layers have been characterised to find the optimum growth potential suitable for the decided device design in Chapter 01.

4.4.1 Experimental procedure for ZnTe growth and characterisation

Zinc Telluride (ZnTe) thin-film layers were grown by mixing 2 ml of 99.995% pure TeO_2 solution into a 400 ml aqueous solution of 99.95% pure 0.015M Zinc Sulphate Monohydrate [$ZnSO_4.H_2O$]. Due to the low water-solubility issue of TeO_2, a solution was prepared by dissolving 2 gm of TeO_2 powder into 30 ml concentrated Sulfuric Acid [H_2SO_4], then mixing the dissolved solution with de-ionized water to make a 200 ml solution. Type 1 ultra-purified de-ionised water has been used in this work for all the solutions. All the chemicals have been purchased from Sigma-Aldrich Ltd (UK). The pH and temperature of the solution has been kept constant at 3.50 ± 0.02 and ~ 85° C respectively. The pH has been adjusted using either diluted sulfuric acid or ammonium hydroxide (NH_4OH). Two-electrode electrodeposition technique has been used for depositing the semiconductor materials on Glass/TEC-7 Fluorine doped tin oxide (glass/FTO) substrates having sheet resistance of ~7 Ω/square. High purity carbon rod has been used as the anode whereas, cathode (working electrode) has been prepared by attaching a glass/FTO substrate to a carbon rod using insulating Polytetrafluoroethylene (PTFE) tape. Prior to electrodeposition, the substrates were cut into 3 cm × 2 cm dimension and rinsed thoroughly with de-ionized water after washing with soap solutions using cotton buds. The substrates were later dried with a high-pressure stream of nitrogen gas. GillAC potentiostat from ACM Instruments have been used as the power source for the 2-electrode ED system. The electrolytic solution was heated and stirred using a hot plate and magnetic stirrer. Moderate stirring rate has been applied to the bath throughout the electrodeposition process.

Cyclic voltammetry has been carried out to determine an estimated range of deposition potential where Zn and Te co-deposition takes place. Physical properties such are thickness and deposition rate for the layers have been measured using Chronoamperometry. The deposited layers were investigated using Sputtered neutral mass spectroscopy (SNMS) for compositional and material identification analysis, X-ray diffraction (XRD) for structural analysis and Scanning electron microscopy (SEM) for morphological analysis. For characterising and optimising electrical and optical properties of the ED samples, photoelectrochemical (PEC) cell measurements and optical absorption using UV-Vis spectrophotometry have been carried out.

4.4.2 Electrochemical analysis with Cyclic voltammetry

Cyclic voltammogram has been recorded for electro-purified aqueous electrolyte containing 0.015 M $ZnSO_4.H_2O$ and 2 ml of TeO_2 solution. The pH and temperature of the solutions were adjusted to 3.50 ± 0.02 and ~85° C respectively. The cyclic sweep is recorded with a sweep rate of 3 mVs^{-1} within a cathodic potential range of 0.0 mV to 2000 mV. Fig. 4.19 depicts a typical voltammogram data plotted with instructive symbols and legends.

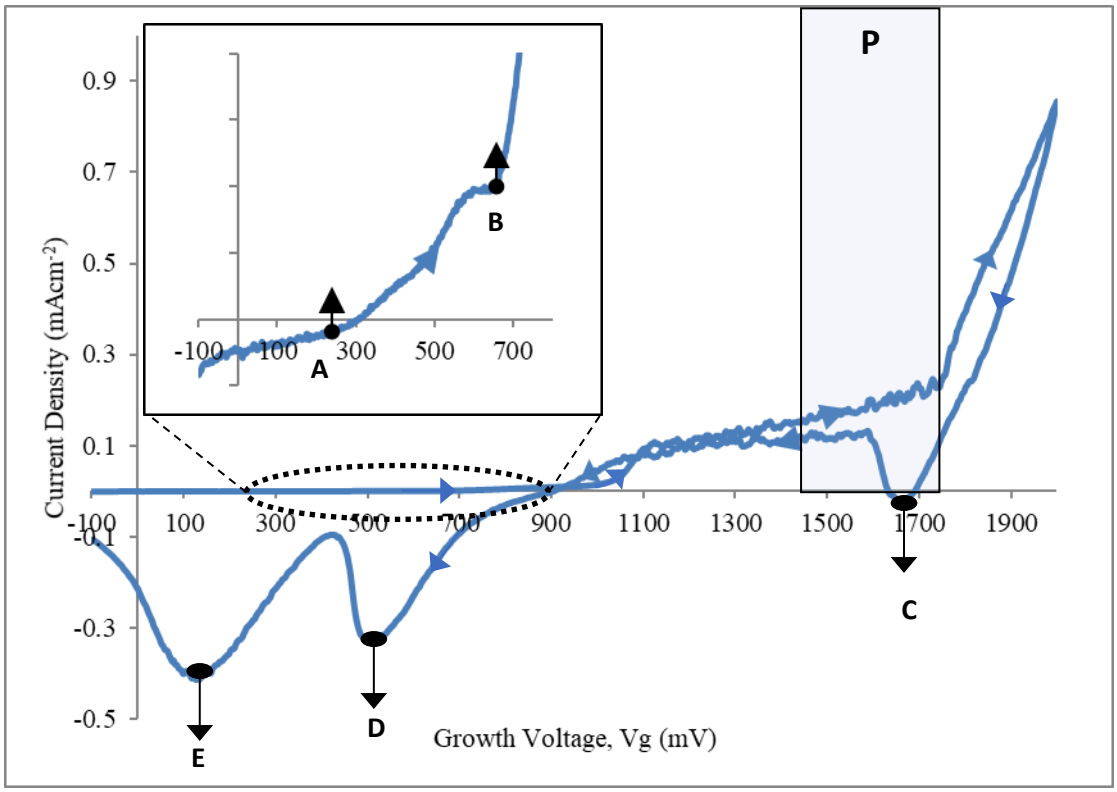


Fig 4.19. Typical cyclic voltammogram of aqueous solution containing 0.015 M $ZnSO_4.H_2O$ and 2 ml TeO_2 solution in de-ionised water. pH and temperature of the solution were kept at 3.50 ± 0.02 and ~85° C

Figure 4.19 depicts, due to the difference of redox potentials amongst the consisting ions, in the forward cycle of voltammogram, Tellurium (Te) having a redox potential (E^o) of ~+0.59 V (with reference to standard H_2 electrode), starts depositing at the beginning at ~300 mV, as per point A depicted in the inset of figure 4.19. The deposition takes place from the Te precursor, according to the electro-chemical reaction equation 4.8:

$$HTeO_2^+ + 4e^- + 3H^+ = Te + 2H_2O \qquad (4.8)$$

Later, Zn having an E^o of -0.762 V (w.r.t. standard H_2 electrode) starts depositing at ~700 mV (Point B of the inset of Fig 4.19) and therefor co-deposition of Zn and Te takes place with slow deposition of ZnTe compound according to the electro-chemical reaction equation 4.9:

$$Zn^{2+} + Te + 2e^- = ZnTe \qquad (4.9)$$

Since, at the beginning of the ZnTe deposition the compound shall be having a lot more Te compared to its Zn counterpart. But with the increment of growth voltage, Zn deposition shall start dominating. Figure 4.19 shows that at ~950 mV there is a visible peak in current density indicating a rise in the Zn deposition. Therefore, it is estimated that near-stoichiometric ZnTe layer can be found within a range of ~1500 mV to ~1700 mV of growth potential (within the P region). From ~1700 mV onward, there is a relatively higher increment in current density, which indicates the possible dissociation of water, hence it is better to avoid growth of thin films beyond this point due to the risk of poor adhesion caused by Hydrogen bubbles underneath the material layer.

In the revers cycle of figure 4.19, the broad negative peak at ~1700 mV (point C) reconfirms the beginning of the dissolving of elemental Zn back into the electrolyte. Further in the reverse cycle, negative peaks at ~500 mV and ~150 mV (point D and E respectively) corresponds to the dissolution of oxidised Te and elemental Te respective, which is consistent with the previous observations made for Te [39]. Observing the voltammogram outcomes, it is decided that the layers are to be deposited within a range of 1500 mV to 1650 mV. The grown layers are then to be heat-treated at 300^{o}C for 10 minutes in air. The heat-treatment parameters have been decided based on previous literatures [35], [36].

4.4.3 Conduction type determination with PEC measurement

Since the main aim of this work is to find a semiconductor material that can be used for p-type window material, therefore determination of the conduction type of the grown layers is carried out at the beginning using Photoelectrochemical Cell (PEC) measurement. The measurements are taken by dipping a glass/FTO/Material layer along with another carbon electrode into an electrolyte prepared from 0.1M $Na_2S_2O_3$ (sodium thiosulphate) aqueous solution. The voltage difference between the electrodes under dark (V_D) and illuminated (V_L) condition is measured to determine the conduction type of the

semiconductor layer. This difference ($V_L - V_D$) represents the open circuit voltage of the solid/liquid junction and is commonly referred as the PEC signal. Polarity of the PEC signal indicates the conduction type. In this work, negative polarity of the PEC signal directs to n-type semiconductor and positive polarity directs to p-type semiconductor, whereas for metals, insulators and intrinsic semiconductors PEC signal is ideally zero. It is also observed that, highly doped layers (p^+ and n^+) too demonstrate a conductor-like behaviour, hence showing near-zero PEC signal [40], [41]. Figure 4.20 shows the material layers deposited at different cathodic potentials within the range of 1500 mV to 1650 mV for 30 minutes. As expected, the layers grown at the beginning of the range show a weak positive PEC signal indicating a p^+ electrical conduction whereas from 1550 mV onward p-type electrical conduction appears implied by a higher positive PEC signal. Below 1550 mV, the layer is dominated by Te, which is a narrow band gap (~0.38 eV) p-type semiconductor/semi metal. Therefore the PEC signal is a small positive value.

In the range 1550-1575 mV, the layer is Te-rich ZnTe, which is a p+ doped ZnTe semiconductor. At 1600 mV, the ZnTe shows best p-type semiconductor properties. As the Vg increases, Zn composition gradually increase and at 1625 mV the material is stoichiometric, and is an intrinsic semiconductor. More Zn addition make it to a best n-ZnTe at ~1640 mV, and then becomes a n+-ZnTe layer. At ~1625 mV the layer grown shows near-zero PEC signal indicating an i-type electrical conduction hence a probable compositional stoichiometry (V_i). This changes gradually towards a negative PEC signal which depicts the change of electrical conduction to n-type. Both as-deposited (AD) and heat-treated (HT) samples show a similar trend in PEC signal, with slight tendency of moving towards p-type for the HT samples. Strength of the PEC signal qualitatively indicates to the doping density and depletion region strength. Each point in the figure 4.20 is the average of three independent measurements.

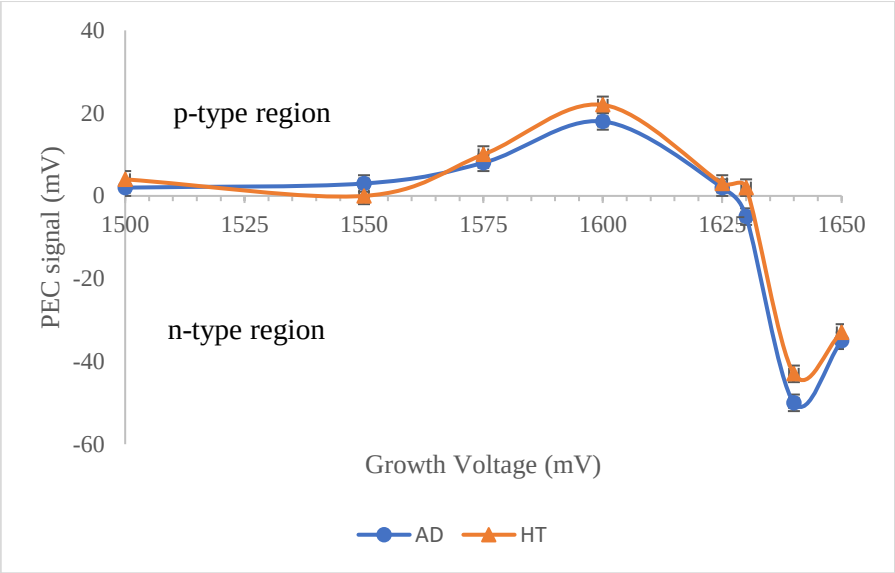


Fig 4.20. PEC signal for AD ZnTe samples along with Heat-treated (HT) samples at 300 °C for 10 minutes

The PEC measurements of the grown layers are very much consistent with the cyclic voltametric analysis of section 4.4.2 above which predicts a deposition of Te-rich layers at lower growth voltage as opposed to Zn-rich layers grown at higher voltage leaving a possible stoichiometric point in the middle. It is to be noted that, Te-richness and Zn-richness causes p-type and n-type electrical conductivity respectively for ZnTe thin films [42].

4.4.4 Compositional analysis with Sputtered Neutral Mass Spectroscopy (SNMS)

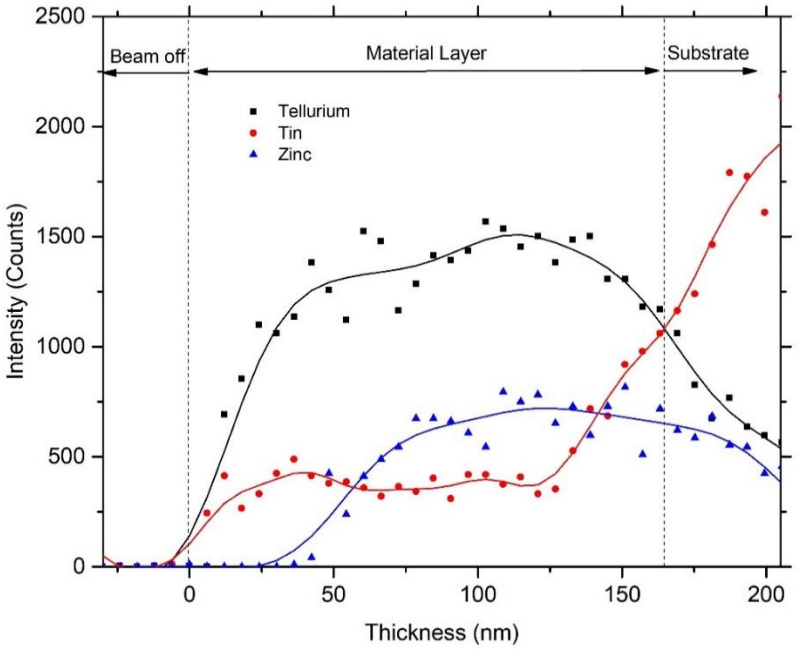
Compositional analysis has been qualitatively carried out using SNMS due to the unavailability of EDX facility during this time. Similar to secondary ion mass spectroscopy (SIMS); an Ar ion beam was used to sputter the material layer. An additional ioniser behind the orifice of the mass spectrometer ionises the neutral flux to make it detectable by a mass spectrometer. As the incident angle of the beam is 45° to the sample surface, data was only collected from within a gate area of 100×100 μm^2, to reduce the noise from the sputter trench sidewalls with increasing depth. The total raster area was 800×800 μm^2. The beam parameters were a beam current of 100 µA and an acceleration voltage of 5 keV. In addition to the layer material isotopes (^{64}Zn and ^{130}Te), the tin isotope ^{120}Sn was also measured to identify the beginning of the underlying FTO substrate. The samples those have been used for this study are the AD-ZnTe layers grown at 1600 mV (figure 4.21a) and 1625 mV (figure 4.21b) cathodic potential. Depth profiling has been

carried out as per the film thickness measured in the later section 4.4.7. In the first minute of the measurement the Ar ion beam remained switched off. The ioniser was in operation to measure the background signal. Once the beam is turned on, all observed isotopes show enhanced signals those gradually reach maximum before slowly reducing to the background level upon reaching the substrate.

From the figure 4.21 it is qualitatively observed that the layer grown at 1600 mV is a Te-rich layer, whereas the layer grown at 1625 mV shows a decreased level of Zn incorporation into the film which indicates to a possible stoichiometry. Quantitative composition of the films could not be measured due to the unavailability of a standard ZnTe reference, but these qualitative results clearly explain what happens as we expect. For both the samples, it is also observed that Zn is not evenly distributed throughout the layer and incorporation of it has taken place from ~20 nm onward into the film.

The tin signal observed during the sputtering of the layer, can be related to holes in the layer exposing the substrate. However, once the substrate surface is reached, the Sn signal intensifies greatly while the layer material signals drop significantly. This qualitative compositional analysis is pertinent to the cyclic voltammetry and PEC studies carried out in section 4.4.2 and 4.4.3 where co-deposition of Zn and Te is presumably about to take place in a Te-rich and stoichiometric manner at ~1600 mV and ~1625 mV cathodic potential respectively.

(a)



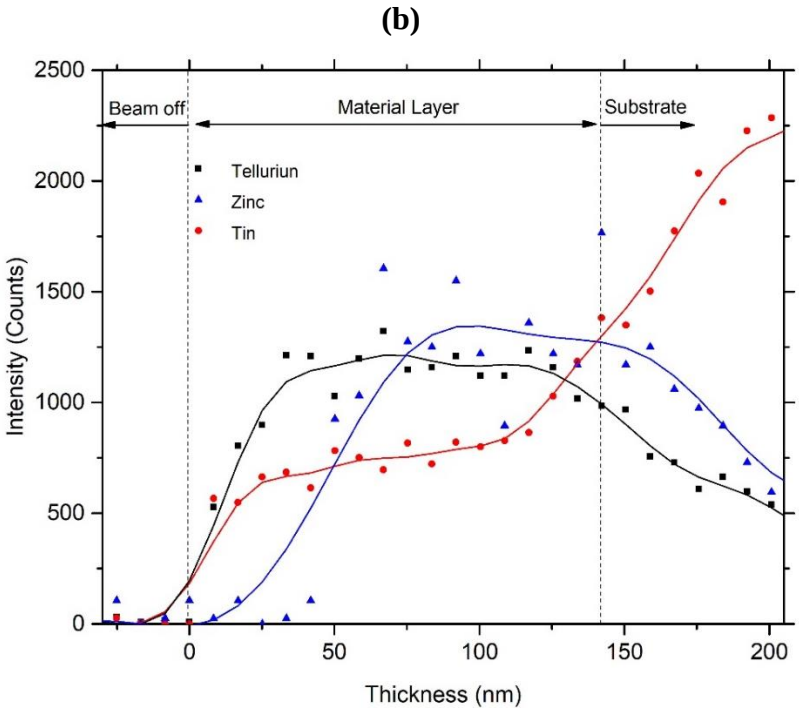


Figure 4.21 Sputtered neutral mass spectra for the ZnTe as deposited sample grown at **(a)** 1600 mV and **(b)** 1625 mV with corresponding 2-points Fast Fourier Transform (FFT) smoothing.

4.4.5 Structural analysis with X-ray diffraction (XRD)

Aim of this analysis is to identify the compound and carry out the structural analysis of the deposited layers at different growth voltages. Philips PW X'Pert Pro diffractometer has been used with Cu-Kα monochromator having a wavelength of 1.54 Å, where the source tension and current were kept as 40 kV and 40 mA respectively. XRD spectroscopy have been carried out on 4 as-deposited (AD) and 4 heat-treated (HT) samples grown at 1575, 1600, 1625 and 1650 mV cathodic potential. From the measured XRD spectra, crystallite size was estimated using the peak with highest intensity. Scherrer's formula given by equation (4.10) was used for this estimation.

$$D = \frac{0.9\lambda}{\beta cos\theta} \qquad (4.10)$$

where wavelength, λ = 1.54 Å, β = full width at half maximum (FWHM) of the diffraction peak in radian and θ = Bragg's angle of incidence. Along with the peak intensity, change of the ZnTe crystallite size due to growth voltage is shown in table 4.4 for both the AD and HT samples.

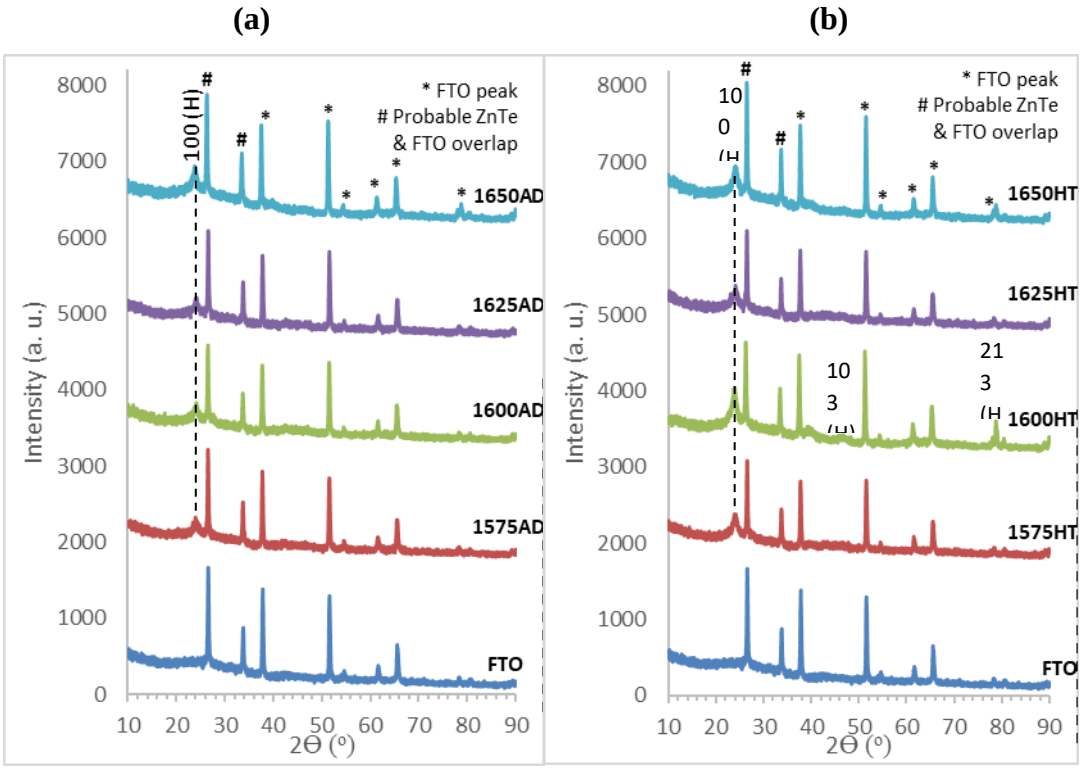


Fig 4.22 XRD patterns of ZnTe thin films grown at Vg range from 1575-1650 mV **(a)** for as-deposited and **(b)** after heat treatment for 10 minutes under 300° C in air

Though, the XRD spectra shown in figure 4.22 for the deposited layers show a low level of crystallinity of the films, the spectral pattern can be decisively identified as hexagonal ZnTe compound as per the JCPDS reference code 00-019-1482. In figure 4.22(a), at $2\Theta \approx 23.9^{o}$ the as-deposited samples show XRD peak corresponding to the diffraction from ZnTe (100) hexagonal plane. Though, peak intensity of the (100) plane is seen to be higher in the AD samples grown at 1600 mV (p-type) and 1650 mV (n-type) compared to the one grown at V_i (1625 mV), point to be noted that XRD intensity can vary due to sample mounting, orientation etc, hence comparison between low intensity peaks are not a reliable indicator of crystallinity. Rather, looking at the crystallite size (D) and atomic spacing (d-spacing), at the V_i, D is large. Therefore, crystallinity is high. Also, at V_i, d-spacing is the smallest. Therefore, atoms are closely packed, which means better crystallinity.

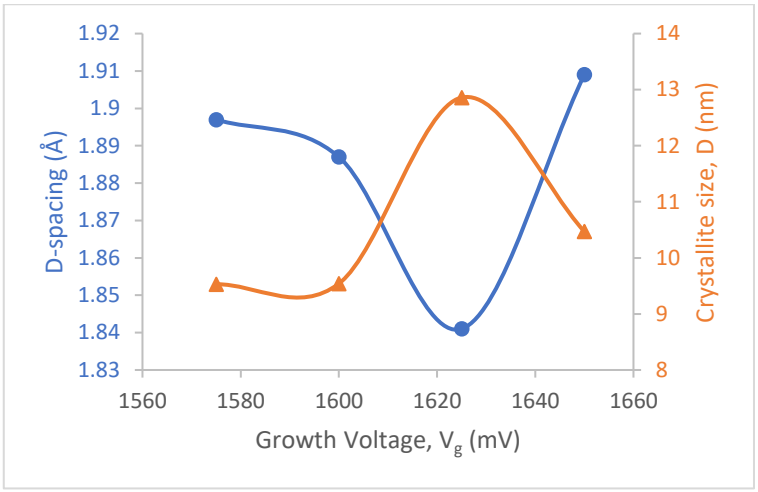
Table. 4.4 XRD analysis of *as-deposited* and *heat treated* ZnTe layers with the increasing V_g from 1575-1650 mV

Sample	**Growth Voltage, Vg (mV)**	**Peak Position, 2Θ (º)**	**Peak intensity, (A. U.)**	**d-spacing (Å)**	**Crystallite size, D (nm)**	**Plane of orientation (h k l)**	**Assignments**
As-deposited	1575	23.94	242	1.897	9.53	(100)	Hexagonal ZnTe
	1600	24.07	259	1.887	9.54		
	1625	24.71	247	1.841	12.86		
	1650	23.79	333	1.909	10.47		
Heat-treated	1575	23.87	295	1.902	8.93	(100)	Hexagonal ZnTe
	1600	23.99	461	1.893	10.61		
	1625	24.09	308	1.886	11.17		
	1650	24.05	359	1.889	9.22		

After heat-treatment it is observed from figure 4.22(b) that the peak intensity increases keeping the similar trend as the AD samples. Moreover, the HT samples grown at 1600 and 1650 mV also show a rise of (213) hexagonal peak at $\sim 2\Theta \approx 78.9^{o}$

Moreover, it is interesting that unlike most materials the crystallite size of the grown ZnTe layers decreased after heat treatment whereas, peak intensity of preferred (100) plane increased, as depicted in figure 4.23 and 4.24. However, this does not necessarily mean that upon heat treatment the periodicity of the atoms is increasing but the size of the crystallites is decreasing, rather the probable cause of this visible decline of crystallite size is that rise of other planes of hexagonal ZnTe such as (213) is occurring, and upon heat treatment the crystallite size is increasing along that orientation.

(a)



(b)

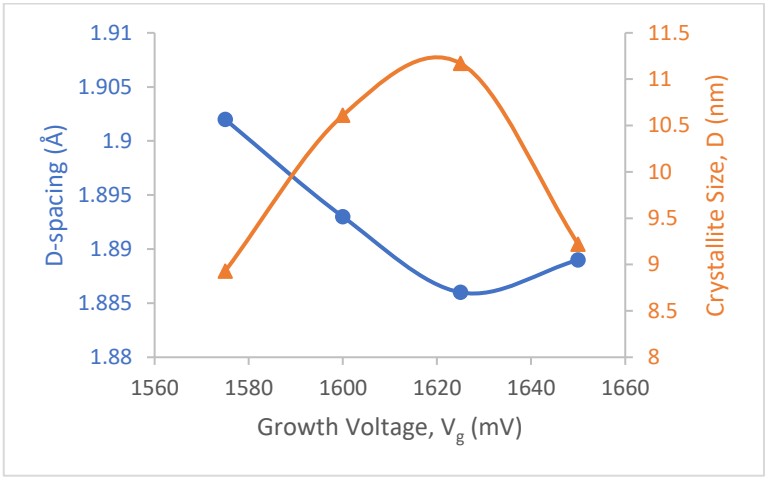


Fig 4.23 Comparative representation of dominant peak intensities, crystallite size and D-spacing for **(a)** AD and **(b)** HT layers grown at different cathodic voltages

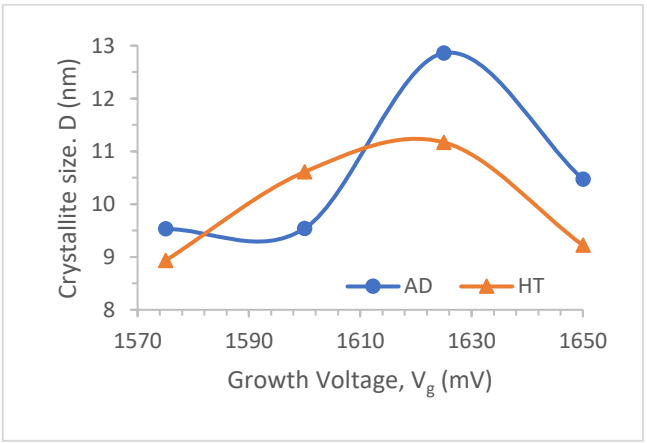


Fig 4.24 Change of the crystallite size along (100) plane of the grown ZnTe layers upon heat treatment

4.4.6 Optical absorption analysis

4.4.6.1 Bandgap studies with Tauc analysis

Optical absorption study has been carried out using Carry 50 scan UV-Vis spectrophotometer, for AD and HT ZnTe layers deposited at different growth voltages. The obtained absorption data within the wavelength of 300 nm to 900 nm, have been used to plot an alternative Tauc plot, where square of absorbance (a^2) is plotted against photon energy (hv). The intersection of extrapolated tangent line derived from the curve, gives the direct band-gap (E_g) of the studied semiconductor material.

According to figure 4.25(a) and figure 4.26, as-deposited ZnTe layers show direct band-gaps ranging between ~1.80 eV to ~2.68 eV. This broad range of band-gaps is far from the typical bandgap of bulk ZnTe (~2.20 to 2.30 eV) [43], [44], but in agreement with the thinfilm bandgap [45]. However, as depicted in figure 4.25(b) and figure 4.26, after heat-treatment of all the layers, bandgap of the layers come within a range of ~2.10 eV to ~2.30 eV which is more proximate to the bulk band-gap. This happens due to the recrystallisation of the nanocrystalline material layer upon heat treatment as noticed in section 4.4.5 [46], [47]. The only exception is the layer grown at stoichiometric voltage 1625 mV, where little change is observed upon heat-treatment. It is accepted widely that large bandgap (>2 eV) binary semiconductors have a tendency to naturally have anion vacancies [48]. These vacancies act as acceptors within the lattice and a phenomenon called self-compensation often takes place for large bandgap II-VI semiconductors, where the effect of extrinsic dopants/impurities are compensated by these native vacancies and hence keeping the conduction type unchanged while affecting the conductivty [37], [49], [50]. That is one reason why ZnTe has been obsereved to have Zn vacancies in its crystal structure and hence seen to be self-compensating if doped with extrinsic impurities, maintaining the material's natural tendency to stay p-type [37], [48]–[50]. However, since in case of electrodeposition there is no extrinsic dopant involved, the composition of the layer changes due to intrinsic doping and thus the conductvity type, but at V_i the self-compenation mechanism may still work for any impurities present in the electrolyte including oxygen. Therefore it is likely that, the layer grown at V_i is more oxydised than others due to the self-compensation mechanism and the high bandgap of this layer is consistent with that [51].

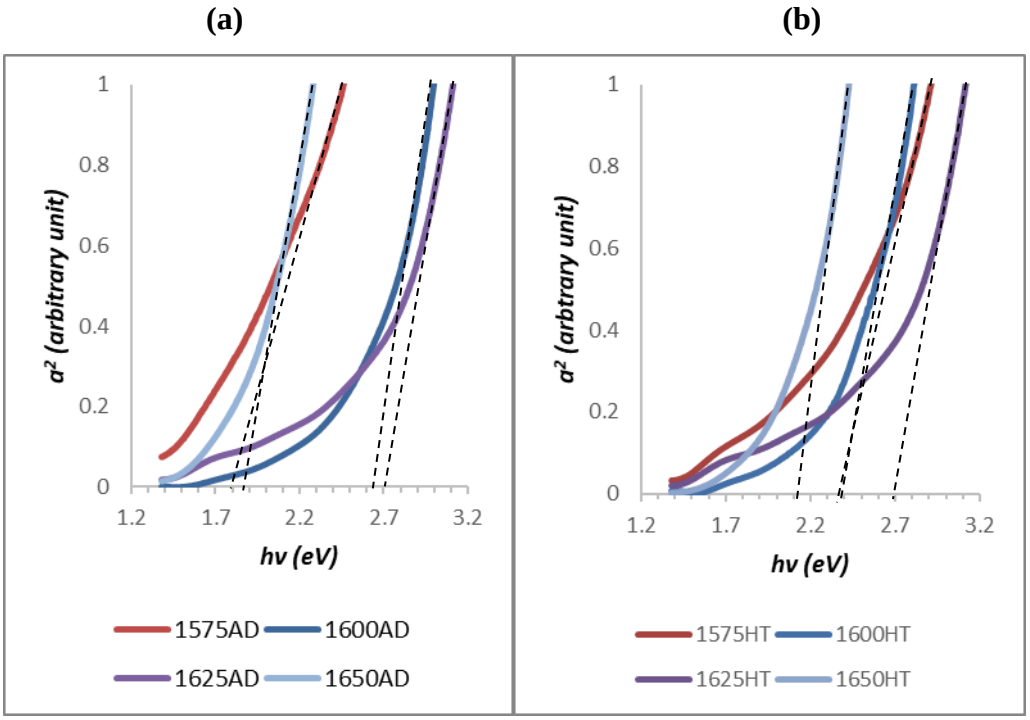


Fig 4.25 a^2 vs hv plot for **(a)** As-deposited and **(b)** Heat-treated (at 300° C for 10 minutes in air) ZnTe samples.

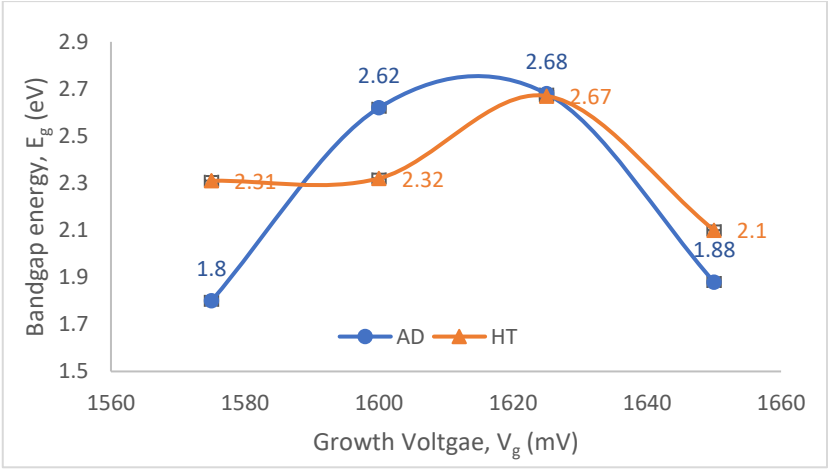


Fig 4.26. Change of bandgap for ZnTe samples due to the change of growth potential

4.4.6.2 Urbach energy analysis

From the optical absorption data, it is also possible to qualitatively have an idea about the probable presence of band tail induced defect levels within the bandgap of the material. Though Urbach analysis more suitably predicts defect positions at the absorption edges of amorphous materials, it is also widely used for nano-crystalline materials [52]–[54].

By plotting a graph between the natural logarithm of absorption (ln*a*) and the photon energy (*hv*), it is possible to find the slope from the linear portion of the exponential curve, which is the reciprocal of Urbach energy [55]. The calculated Urbach energy (E_U) is indicative of the temperature dependent width of the band tail or in other words possible absorption points near the band edge of the thin film at a particular temperature. Figure 4.27 below show the ln*a* vs *hv* plot for all the Heat-treated ZnTe layers. The graph shows linear portions of the exponential curves those are nearly vertical, therefore a sharpness of the slope. This indicates to the absence of any additional localised electronic state or intra-bandgap defect level which means a good crystalline structure for all the layers.

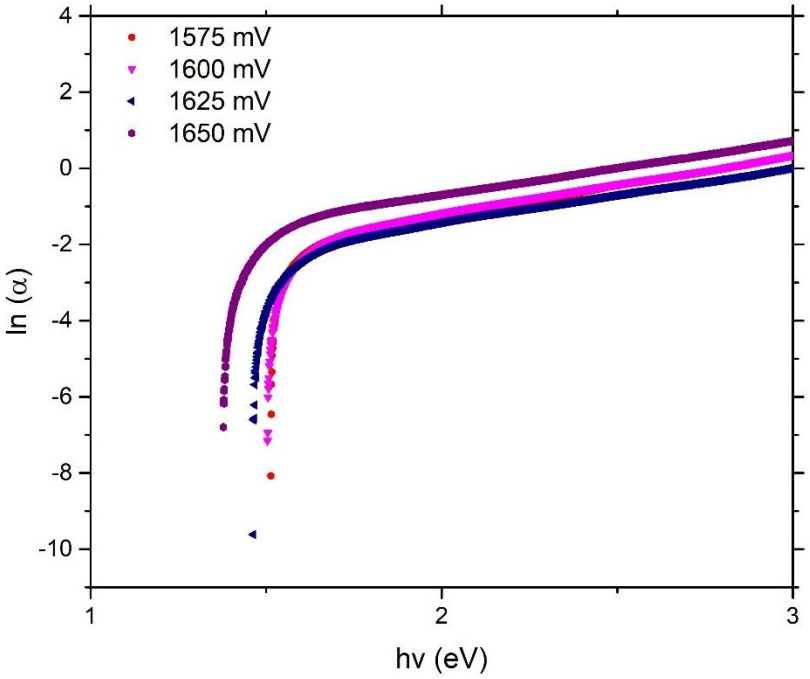


Fig 4.27 ln*a* vs *hv* plot for the HT ZnTe layers indicative of slopes that inversely signify Urbach tail.

Figure 4.28 presents a comparison amongst all the potential p-type layers electrodeposited in this work. It is visible that both only CdTe:Mg shows a spreading of band tail ~0.3 eV above the valence band edge, which is expected as the layers show amorphous characteristics. CdMnTe and ZnTe on the other hand shows negligible width of band tail in the range of ~0.04 eV.

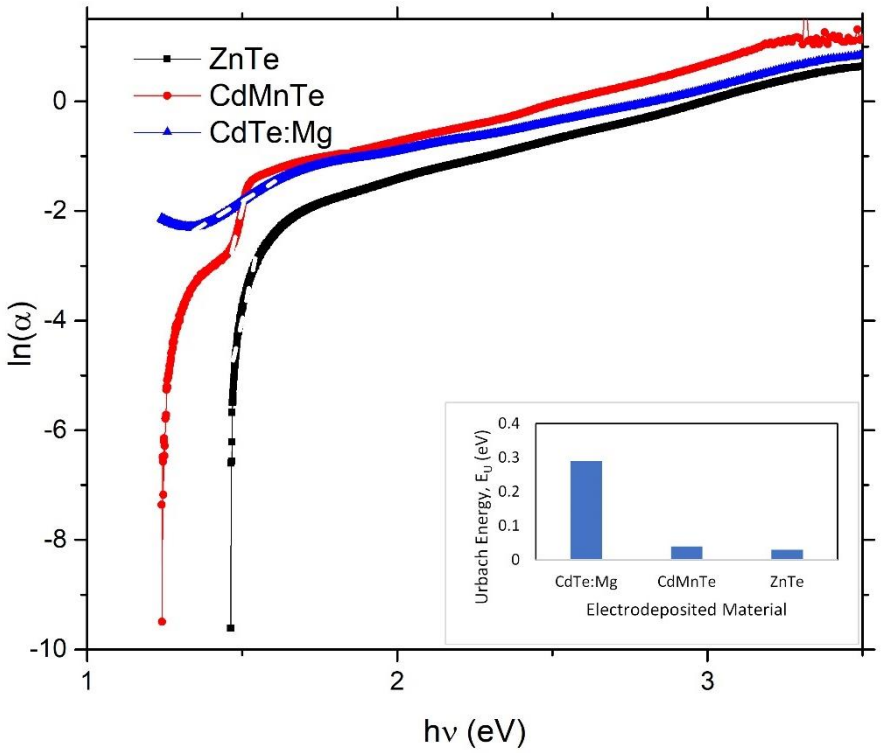


Fig 4.28 Comparison of Urbach tails amongst the best material layers grown for CdTe:Mg, CdMnTe and ZnTe. Inset shows the lowest Urbach energy calculated for the ZnTe layers.

Point to be noted that, Urbach analysis does not account for all the possible defect levels in ta material and often very dependant on temperature. Therefore a wide range Photoluminescence (PL) analysis is often used for the verification of the Urbach calculation, which could not be carried out for this work [56].

4.4.7 Chronoamperometric analysis for thickness and deposition rate

Chronoamperometry is an analytical technique used for electrochemical characterisation of materials where change of current density over time is traced at a static applied voltage. A Gill AC potentiostat has been used to carry out Chronoamperometric studies in this work where one current density reading has been taken every 3 seconds. Figure 4.29 below shows a typical chronoamperometric (current density vs time) plot where the applied voltage is 1600 mV. Area under the chronoamperometric curve gives the theoretical amount of charge transferred which, using the Faraday's law of electrolysis according to equation (3.1), helps the theoretical calculation of the thickness of the thin films. This calculation assumes that no electric charge is used for water splitting and hence provide the upper limit of the thickness of the layers.

The minimum voltage required to break the water molecule is ~1.20 V, and with system losses, water splitting starts around ~1500 mV. Therefore, some of the water splitting is expected when 1600 mV is applied, and this production of atomic hydrogen at the cathode will be important for passivating defects in the growing material. This is one advantage in electroplating of semiconductors from aqueous solutions. Since this process consumes some electric charge, the exact thickness of the layer will be slightly less than the theoretically estimated value.

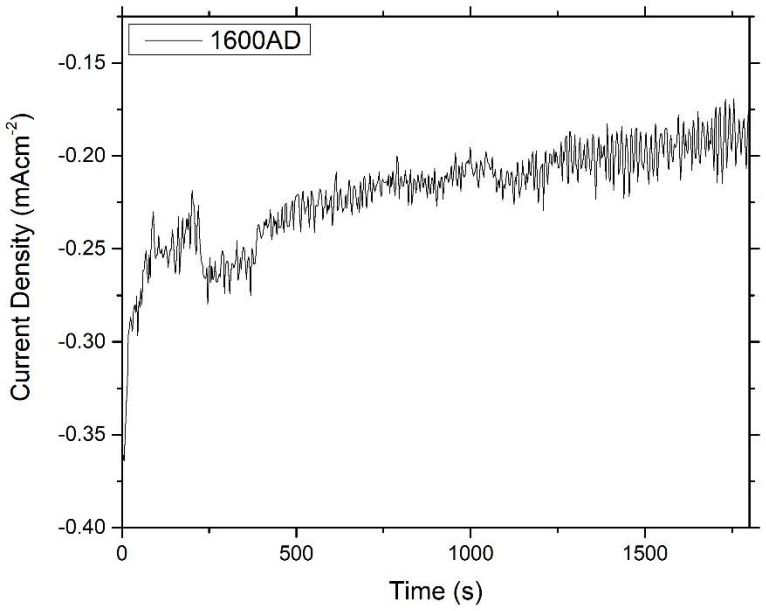


Fig 4.29 Current density (J) vs Time (T) plot for the ZnTe sample growth at 1600 mV for 30 minutes

Furthermore, in the figure 4.30, the thickness vs time curve is presented for the layers grown at 1600 mV, 1625 mV and 1650 mV which shows a nearly linear trend of progression. From the slope of the linear fit, it is possible to calculate the rate of deposition at different deposition voltage. Figure 4.31 shows that at the applied cathodic potential of V_i (1625 mV) deposition rate is the slowest amongst all the other applied voltages. This observation is consistent for other electrodeposited i-type layers too where lower deposition rate was observed at V_i [8].

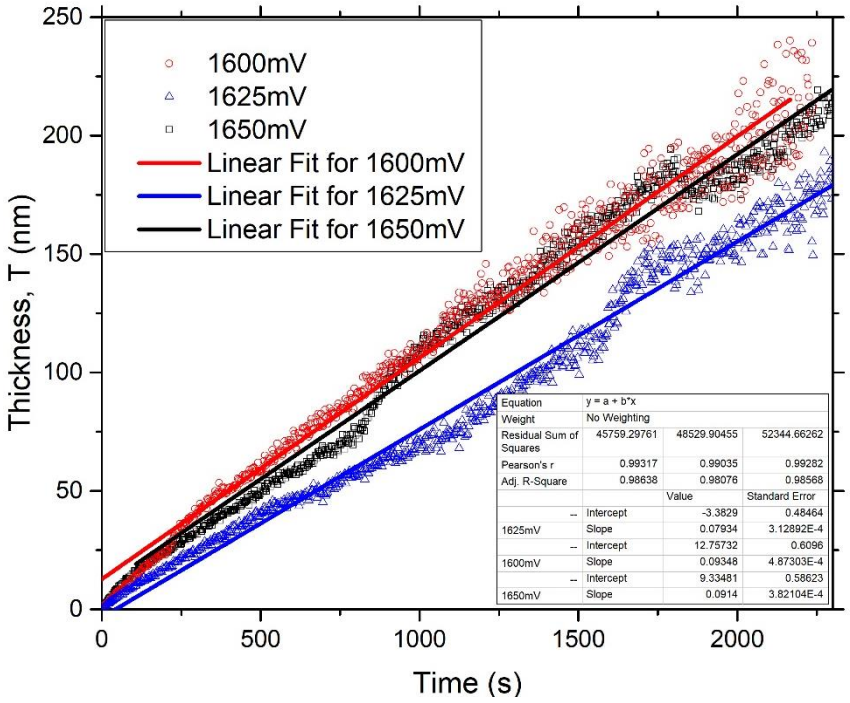


Fig 4.30 Change of ZnTe layer thickness over time for different cathodic voltages applied

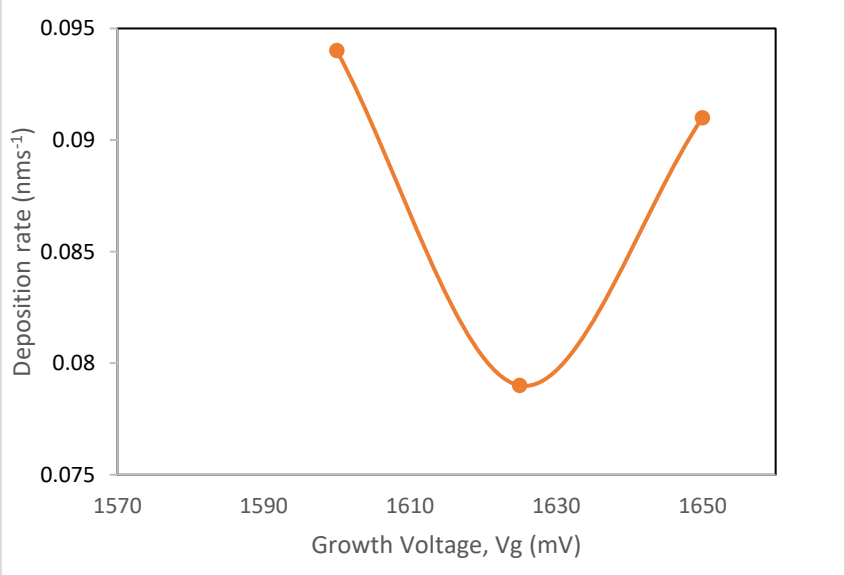


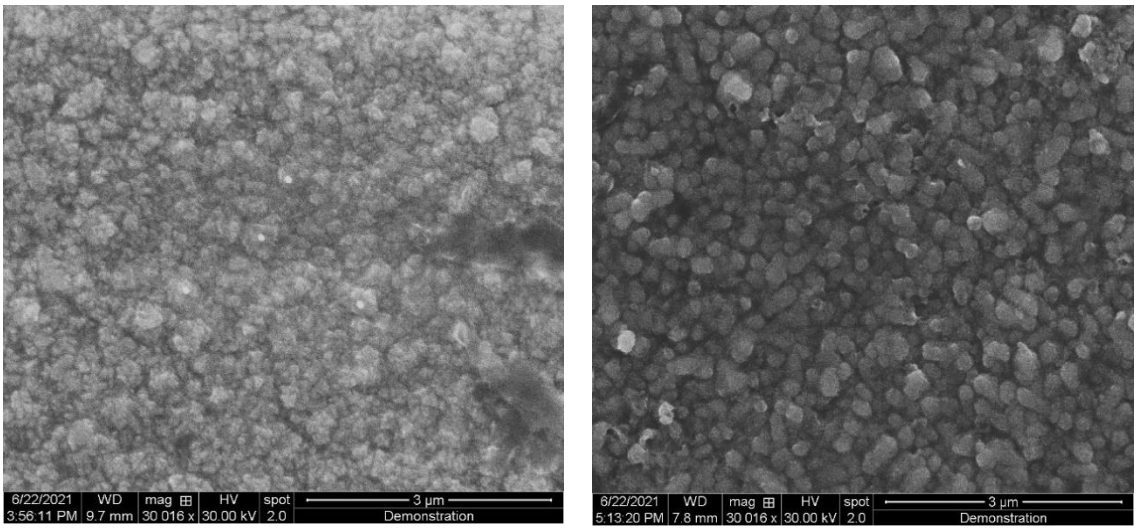
Fig 4.31 Transition of Deposition rate of ZnTe layers as a function of growth voltages

4.4.8 Morphological analysis with Scanning electron microscopy (SEM)

In order to carry out the morphological characterisation of the ZnTe layers, SEM analysis has been done in the form of micrographs using 30.0 kV electron beam voltage and 30,000× of magnification. SEM images of glass/FTO/ZnTe substrates have been taken for both as-deposited and heat-treated samples grown at 1600 mV (figure 4.32(a-b)) and

1625 mV (figure 4.32(c-d)). In figure 4.32, at both growth voltages, regardless of heat-treatment, all the surfaces demonstrate agglomerations of ZnTe crystallites. From the SEM micrograph the size of the agglomerations is ranging approximately between ~200 nm to ~300 nm. Therefore, individual ZnTe crystallites are not visible in the SEM image as calculated above in table 4.4.

(a) AD at 1600 mV **(b) HT at 1600 mV**



(c) AD at 1625 mV **(d) HT at 1625 mV**

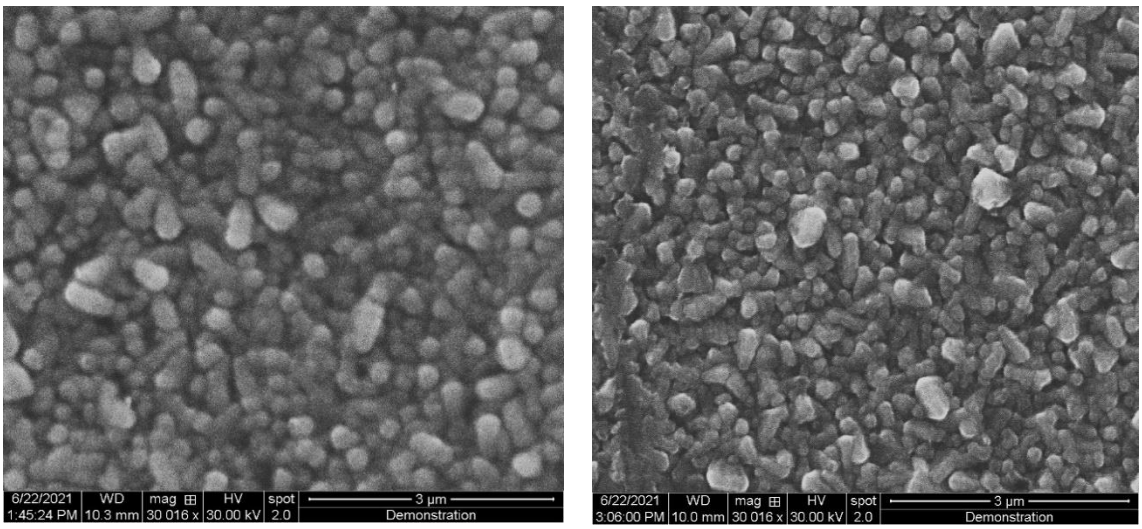


Fig 4.32 Typical SEM images of ZnTe thin films grown at 1600 mV and 1625 mV **(a, c)** as-deposited and **(b, d)** heat-treated at 300^{o} C for 10 minutes in air

Upon heat treatment, noticeable recrystallisation takes place in sample grown at 1600 mV. However, for samples grown at 1625 mV the change of crystallisation is not as drastic. This outcome is consistent with the change of bandgap due to heat-treatment demonstrated in figure 4.26 above.

4.4.9 Summary of the ZnTe electrodeposition

In this work, as a possible alternative to the previously grown ternary compounds, cathodic electrodeposition of binary ZnTe thin-films have been carried out using $ZnSO_4.H_2O$ precursor, in order to develop all-electrodeposited graded bandgap devices, starting from p-type wide-bandgap window. The grown layers demonstrated an ability to grow p-type, i-type and n-type ZnTe layers from the same bath. Transition of the conduction type is proved to be caused by the change of composition, as in p-type and n-type at Te-rich and Zn-rich conditions respectively. The layers show a hexagonal nano-crystalline structure which gets slightly improved in terms of crystallinity upon heat treatment and show almost no change in the conductivity type. The heat treated layers have a bandgap of ~2.30 eV which in agreement with the ZnTe thin-film [45]. Layers grown at 1625 mV, which is i-type in conductivity shows the best properties in terms of crystallinity, however the desired p-type window material layer can be grown at a slightly lower growth voltage with reasonably good crystallinity too. Point to be noted that electrodeposited ZnTe layers have shown a better crystallinity while grown with heptahydrate precursors, as per previous works with same electrolytic composition [35], [36], [42].

4.5 Material selection for the p-type window

In this chapter, three potential thin-film materials have been synthesized, characterised, and optimised to find a suitable wide bandgap p-type window material for the decided device design. Two ternary materials namely, CdTe:Mg (Sub-chapter 4.2) and CdMnTe (Sub-chapter 4.3) and one binary material ZnTe (Sub-chapter 4.4) have been explored. The major parameters those have been considered for material selection are post-treatment conduction type, energy bandgap and crystallinity of the layers.

In the section 4.4.6.2 it has been shown in terms of the comparative Ubach analysis that, electrodeposited ZnTe layers demonstrate the highest quality layers with the probably the lowest width of the band tail, hence least chances of having any localised electronic states or traps at a given temperature.

Table 4.5 Major material parameters of the potential ebdb layers electrodeposited at different voltages. Optimised best layers for each candidate are highlighted in blue.

Material	**Growth Voltage (mV)**	**Conduction type**		**Bandgap, E_g** (± 0.02 ev)		**Crystallinity**
		AD	Treated	E_g	E_{g2}	
CdTe:Mg	1380	p	p	2.85	-	Not found (Amorphous)
	1400	p	p	2.80	-	
	1420	p	p	2.82	-	
	1480	p	p	2.95	1.48	
CdMnTe	1370	n	p	1.72	1.45	Cubic
	1400	n	p	1.92	1.48	
	1430	n	p	1.96	1.50	
	1450	n	p	1.94	1.48	
ZnTe	1575	p	p	2.31	-	Hexagonal
	1600	p	p	2.32	-	
	1625	i	i	2.67	-	
	1650	n	n	2.11	-	

Moreover, as specified in table 4.5, though for CdTe:Mg, both the As-deposited (AD) and $MgCl_2$ treated samples show p-type conductivity with ~ 2.85 eV bandgap, the layers completely lose crystallinity with increasing Mg inclusion and PL spectra showed clear

intra-bandgap absorption point (E_{g2}) for the layers. For, CdMnTe layers, post-growth treated samples show p-type conductivity with a cubic crystallinity. But the intra-bandgap absorption edge possesses a risk of lowering absorption of photon as well as the effective barrier height of the PV device. ZnTe layers on the other hand, show all the qualities those are sought after as well as a possibility to tune the electrical conduction from p-, i- and n-type layers.

In addition, since ZnTe can be grown p-, i- and n-type from the same electrolyte, n-ZnTe can be used as the (hbdb) layer simplifying the manufacturing of graded bandgap multi-layer solar cells.

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Chapter 5

Growth and characterisation of CdTe absorber layers

5.1 Introduction

The main experimental works of this project are divided into four parts as discussed in the first chapter; three of them take care of the material selection and the last one is for device fabrication and testing. After synthesis, characterisation, optimisation, and selection of the wide bandgap p-type window layer in the previous chapter, this chapter discusses about the growth, characterisation, and optimisation of the main absorber layer, which is Cadmium Telluride (CdTe).

Electrodeposition of CdTe is an established, tested, commercially viable and reliable technique that has been implemented for a long time now [1]–[4]. Electrodeposition of device-grade CdTe is normally performed using high purity (≥5N) precursors for Cd and Te, of which typical Cd precursors include, $CdCl_2$, $CdSO_4$, $Cd(NO_3)_2$ etc and as Te-precursor, TeO_2 is most commonly used [5]–[8]. During the preparation of CdTe electrolytic bath, it is common practice that Cd-precursor takes the major portion of the bath due to its high electronegativity [9]. The current highest efficiency for the electrodeposited CdTe-based solar cells (~15.3%) is achieved from high purity (99.999%) $Cd(NO_3)_2.4H_2O$ precursor for Cd [10]. In this work, electrodeposition of CdTe has also been carried out with $Cd(NO_3)_2.4H_2O$ precursor for Cd, however a comparatively lower purity (98%) chemical has been used. Lower purity precursors are much less expensive than their high purity counterparts, but compared to 5N purity of materials, 98% purity means 2000 times more possibility of adding unwanted impurities since, 99.999% purity means 10 ppm possible impurities whereas 98% purity means 20,000 ppm impurities. Growth of semiconductors by electrodeposition is an extremely impurity sensitive process where addition of a few ppm level of impurities in the bath can drastically change the material properties of the semiconductors [11]. Hence, growth of device quality CdTe thin-films from lower purity precursors is a challenging task and this chapter attempted for that. Majorly, to mitigate the impurity issue, the aqueous bath prepared from the 98% $Cd(NO_3)_2.4H_2O$ has been put through a rigorous electro-purification process before being mixed with any other precursors.

Further to electro-purification, standard post growth treatment for CdTe has been also performed. $CdCl_2$ treatment being the most widely accepted post-growth treatment for CdTe, is not only advantageous for the layer quality but also for the overall performance of the cell. Post growth $CdCl_2$ treatment at 400^oC for 20 minutes enables recrystallization of the as grown films which increases the grain size, regularises crystallites and reduces the grain boundary induced defects in the structure. Though the mechanism is yet to be fully understood by the research community, this grain boundary (GB) passivation effect has been identified as one of the major possible reasons behind the quality improvement due to $CdCl_2$ treatment [12]–[17]. Recent computational analysis has predicted that this grain boundary passivation primarily takes place at a single particle level upon $CdCl_2$ treatment [18]. Moreover, studies also demonstrated evidence that $CdCl_2$ treatment improves the device performance not only by passivating the GBs, but also by enforcing positive contribution out from the grain boundaries too [12], [19]–[21]. The layers grown here has been also put through $CdCl_2$ treatment for the improvement of material as well as device properties.

5.2 Experimental procedure

Cadmium Telluride (CdTe) thin-film layers were grown from a 400 ml aqueous electrolytic solution containing Cd^{2+} obtained from 98% pure Cadmium Nitrate Tetrahydrate ($Cd(NO_3)_2.4H_2O$) precursor and Tellurium (Te) precursor prepared from acidic solution of 2 gm Tellurium dioxide (TeO_2) of 99.99% purity. Ultra-pure Type-II de-ionised water has been used throughout the work. First, the aqueous electrolyte was prepared from 1.5 M $Cd(NO_3)_2.4H_2O$, then the precursor solution was electro-purified for ~100 hours at a voltage lower than that of the minimum deposition voltage of Cadmium found in literature [22]. This way, elements having less electro-negativity compared to Cd can be removed from the bath. Long electro-purification has been carried out due to the commercial unavailability of very high purity (≥99.99%) Cd precursor. After the electro-purification, 3 ml of the TeO_2 solution has been added to the bath. Since TeO_2 cannot dissolve completely in water, 30 ml of concentrated Nitric acid (HNO_3) was added to the TeO_2 solution to aid its solubility. The prepared TeO_2 solution was subjected to continuous stirring and heating for ~45 minutes to obtain a very clear TeO_2 solution devoid of powder. All these chemical precursors have been purchased from Sigma-Aldrich Ltd. (UK). The pH and temperature of the solution has been kept constant at 2.00±0.02 and ~85^o C respectively following similar CdTe electrodeposition in the past

[23]–[25]. The pH has been adjusted using either very diluted nitric acid or ammonium hydroxide (NH_4OH). Two-electrode electrodeposition technique has been used for depositing the semiconductor materials on Glass/ TEC-7 Fluorine doped tin oxide (glass/FTO) substrates having sheet resistance of ~7 Ω/square. High purity carbon rod has been used as the anode whereas, cathode (working electrode) has been prepared by attaching glass/FTO substrates to carbon rod using insulating Polytetrafluoroethylene (PTFE) tape. Prior to electrodeposition, the substrates were cut into 3 cm × 2 cm dimension and rinsed thoroughly with de-ionized water after washing with soap solutions using cotton buds. The samples were later dried with nitrogen gas stream. GillAC potentiostat from ACM Instruments is used as the power source for the 2-electrode ED system. The electrolytic solution was heated and stirred using a hot plate and magnetic stirrer. Moderate stirring rate has been applied to the bath throughout the electrodeposition process.

Cyclic voltammetry has been carried out to determine an estimated range of deposition potential where Cd and Te co-deposition takes place. The deposited layers were investigated using Energy Dispersive X-ray (EDX) spectroscopy for compositional and material identification analysis and X-ray diffraction (XRD) for structural analysis and Scanning electron microscopy (SEM) for morphological analysis. Estimation of the maximum theoretical thickness of the deposited films has been performed using chronoamperometry. For characterising and optimising electrical and optical properties of the ED samples, photoelectrochemical (PEC) cell measurements and optical absorption using UV-Vis spectrophotometry have been carried out.

5.3 Cyclic voltammetric Study

Cyclic voltammograms were separately recorded for electro-purified aqueous electrolytes containing 1.5M $Cd(NO_3)_2.4H_2O$ and a mixture of 1.5M $Cd(NO_3)_2.4H_2O$ with ~0.0002M TeO_2. The reason of maintaining this drastically different composition of precursors in the electrolyte is the difference of redox potentials between Cd and Te. Te being electropositive, deposits much easily at low growth voltage whereas Cd having a high electronegativity requires high growth voltage. Hence, for stoichiometric material growth, the bath is prepared with abundance of Cd contrary to a very little inclusion of Te precursor. The pH and temperature of the solutions were adjusted to 2.00 ± 0.02 and ~85^o C respectively. The cyclic sweep is recorded with a sweep rate of 3 mVs^{-1} within a

cathodic potential range of 0.0 mV to 2000 mV. Figure 5.1 depicts a typical voltammogram data plotted with instructive symbols and legends.

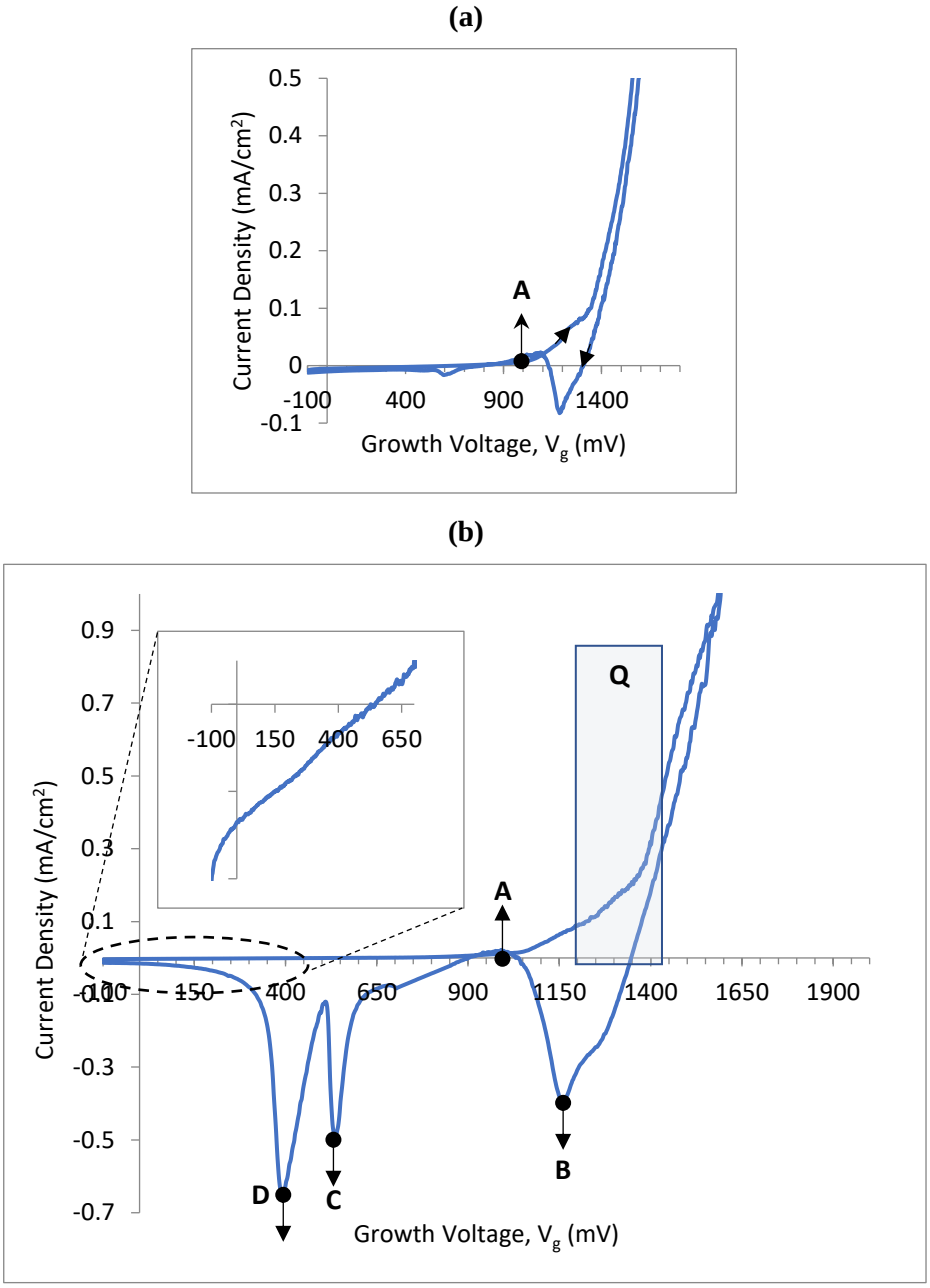


Fig 5.1 Typical cyclic voltammogram of aqueous solution containing **(a)** 1.5M $Cd(NO_3)_2.4H_2O$ and **(b)** a mixture of 1.5M $Cd(NO_3)_2.4H_2O$ and ~0.0002M TeO_2 in de-ionised water. Inset shows the typical deposition point of Te on the cathode.

Inset of the figure 5.1(b) depicts, due to the difference of redox potentials amongst the consisting ions, in the forward cycle of voltammogram, Tellurium (Te) having a redox potential (E^o) of +0.593 V (with reference to standard H_2 electrode), starts depositing at

the beginning of the process. The deposition takes place from the Te precursor, according to the electro-chemical reaction equations 5.1:

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \qquad (5.1)$$

Later, Cd having an E^o of -0.403 V (w.r.t. standard H_2 electrode) starts depositing at ~1000 mV (point A in figure 5.1(a) and figure 5.1(b)) according to the electro-chemical reaction equation 5.2:

$$Cd^{2+} + 2e^- \rightarrow Cd \qquad (5.2)$$

Hence, figure 5.1(b) shows the co-deposition of cadmium and tellurium begins from point A onward and Te-rich CdTe starts to deposit from ~1000 mV onward according to the reaction equation 5.3. As higher cathodic voltage is applied, Cd starts increasingly incorporating to the layer.

$$HTeO_2^+ + Cd^{2+} + 3H^+ + 6e^- \rightarrow CdTe + 2H_2O \qquad (5.3)$$

Therefore, it is estimated that near-stoichiometric CdTe layer can be found within a range of ~1300 mV to ~1400 mV of growth potential as depicted in the rectangle denoted by Q. From ~1400 mV onward, there is a relatively higher increment in current density visible, which indicates the possible dissociation of water.

In the reverse cycle of figure 5.1(a) and (b), the negative peak at ~1160 mV denoted by point B reconfirms the dissolving of any elemental Cd as well as dissociation of CdTe formed on the FTO surface. The dissolution of Te from the surface of the cathode occurs at the broad peaks labelled C and D. Two broad peaks must be representing two phases of Te, presumably oxidised Te and elemental Te respectively [26]. Observing the voltammogram outcomes, first it is decided that the layers are to be deposited within a range of 1300 mV to 1400 mV. The grown layers are then to be heat-treated with $CdCl_2$ at 400^{o}C for 20 minutes in air. The heat-treatment parameters have been decided based on optimisation from previous literatures [23]–[25].

5.4 X-ray diffraction (XRD) analysis

Aim of this analysis is to carry out the structural analysis of the deposited layers at different growth voltages. Philips PW X'Pert Pro diffractometer has been used with Cu-Kα monochromator having a wavelength of 1.54 Å, where the source tension and current were kept as 40 kV and 40 mA respectively. XRD spectroscopy have been carried out on as-deposited (AD) and $CdCl_2$-treated (CCT) samples grown at 1300, 1315, 1320 and 1325 four different cathodic potentials. Indexing with the JCPDS reference file 01-075-2086, it is seen in figure 5.2(a) that, at $2\Theta \approx 23.9^o$, $\approx 39.6^o$ and $\approx 46.7^o$ the as-deposited samples show XRD peaks corresponding to the diffraction from CdTe (111), (220) and (311) cubic planes. Upon $CdCl_2$-treatment, as depicted in figure 5.2 (b) an increment in the dominant peak intensities is visible compared to the AD CdTe layers. For the dominant (111) peak resulting from the preferred orientation, among different growth voltages, the trend shows that peak intensity reaches its maximum at ~1315 mV and then gradually goes down at higher growth voltages. Figure 5.2 and 5.3 depict this trend for both the AD and CCT CdTe samples. Along with the peak intensity, change of the CdTe crystallite size due to growth voltage is shown in table 5.1 for both the AD and CCT samples. Crystallite size at the preferred orientation has been calculated using Scherrer's formula given by equation (5.4).

$$D = \frac{0.9\lambda}{\beta cos\theta} \qquad (5.4)$$

where wavelength, $\lambda = 1.54$ Å, β = full width at half maximum (FWHM) of the diffraction peak in radian and θ = Bragg's angle of incidence. K = 0.9 was used since the exact value of k for the present material system is not known. The calculated crystallite size is only a comparative estimate and is likely to differ slightly.

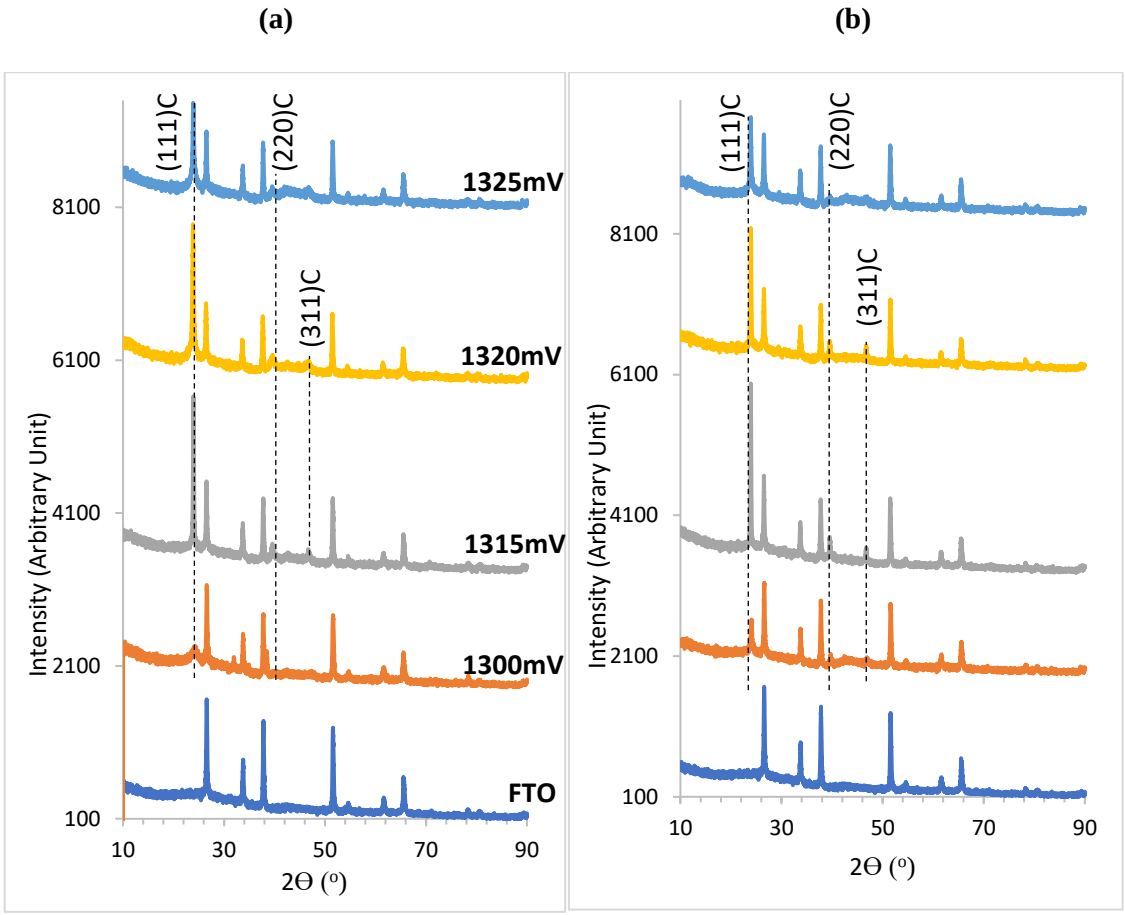


Fig 5.2 XRD patterns of CdTe thin films grown at V_g range from 1300-1325 mV **(a)** for as-deposited and **(b)** after $CdCl_2$ treatment for 20 minutes under 400º C in air.

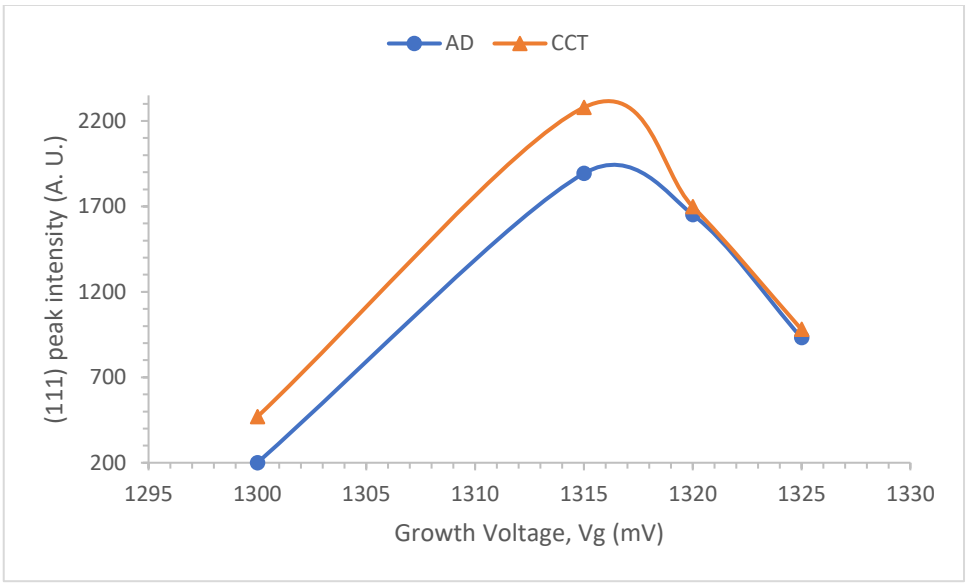


Fig 5.3 Comparative analysis of dominant peak intensities for AD and CCT layers grown at different cathodic voltages

Table 5.1 shows that the as-deposited samples grown at 1315 mV has the largest crystallite size (~37 nm) among the others. For CCT samples, the trend carries on and all the CCT samples show larger crystallite size than their as-deposited counterparts with the highest size of ~45 nm at 1340 mV. This range of crystallite size is comparatively smaller than that of the CdTe layers grown with high purity Cd-precursors [7].

Table 5.1 XRD analysis of *as-deposited* and $CdCl_2$-treated CdTe layers with the increasing V_g from 1300-1325 mV

Sample	**Growth Voltage, Vg (mV)**	**Peak Position, 2Θ (º)**	**d-spacing (Å)**	**FWHM (º)**	**Crystallite size, D (nm)**	**Lattice strain (A. U.)**	**Plane of orientation (h k l)**	**Assignments**
As-deposited	1300	24.25	1.88	0.64	13	0.0131	(111)	Cubic CdTe
	1315	23.94	1.89	0.23	37	0.0047		
	1320	23.87	1.90	0.30	28	0.0062		
	1325	23.94	1.89	0.32	27	0.0065		
$CdCl_2$-treated	1300	24.07	1.89	0.26	33	0.0052	(111)	Cubic CdTe
	1315	23.94	1.89	0.19	45	0.0039		
	1320	23.95	1.89	0.23	38	0.0046		
	1325	23.92	1.90	0.27	32	0.0055		

5.5 Chronoamperometric analysis of the CdTe layers

Chronoamperometry is an analytical technique used for electrochemical characterisation of electrolytes where change of current density over time is traced at a static applied voltage. Using a Gill AC potentiostat Chronoamperometric studies in this work were carried out where current density readings have been taken at a 3 second interval. Figure 5.4(s) below shows a typical chronoamperometric (current density vs time) plot where the applied voltage is 1315 mV for 30 minutes. Area under the chronoamperometric curve gives the theoretical amount of charge transfer which, using the Faraday's law of electrolysis according to equation (3.1), helps the maximum theoretical calculation of the thickness of the thin films. Hence, this thickness calculation has been seen to be slightly higher than the experimental measurement [7]. Furthermore, in the figure 5.4 (b), the thickness vs time curve is presented for the layers grown at 1310 mV, 1315 mV and 1320 mV which shows a linear trend of progression. From the slope of the linear fit, the rate of deposition at different deposition voltage is calculated. From the slopes, it is visible that at the applied cathodic potential of 1315 mV deposition rate is comparatively slower

amongst the other applied voltages. Point to be noted that, at this voltage the resultant layers also shown greater crystallinity. Previous observations shown that electrodeposited stoichiometric i-type layers normally deposit at a lower deposition rate [27] due to the high resistance of the intrinsic layer.

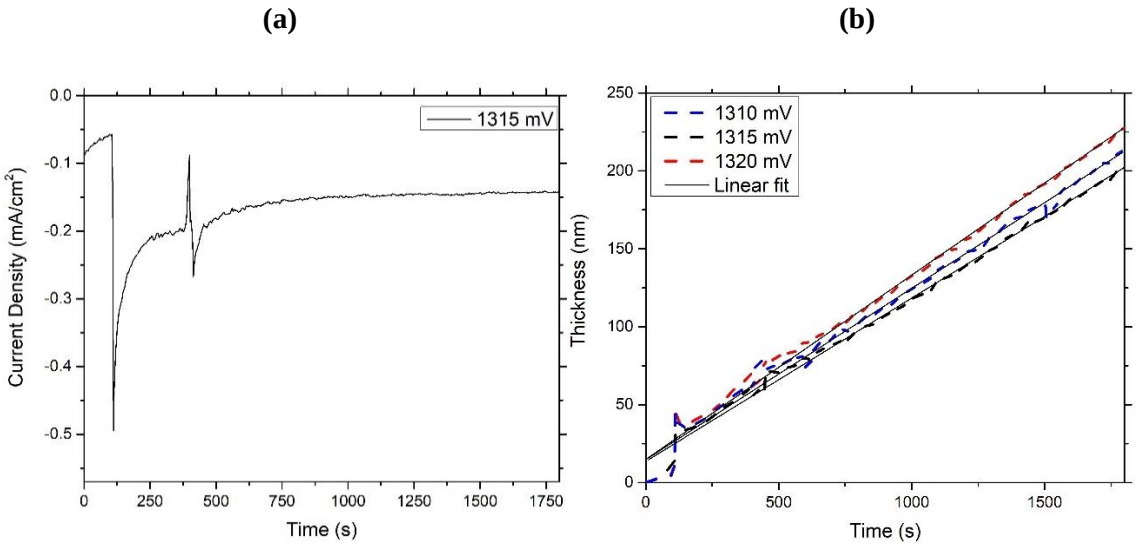


Fig 5.4 (a) Chronoamperometric (I-T) plot at 1315 mV growth potential along with (b) comparison between growth rates (thickness vs time) at different growth potentials.

5.6 Energy dispersive X-ray (EDX) spectroscopy

EDX was carried out on the as-deposited (AD) and $CdCl_2$-treated (CCT) CdTe samples grown at 1310, 1315 and 1320 mV, using the AzTec compositional analysis software associated with the Quanta 650 SEM equipment, in order to obtain the chemical composition of the samples. Figure 5.5 shows the EDX spectra of the as-deposited sample grown at 1315 mV which shows a near stoichiometric composition of Cd and Te. Table 5.2 presents the atomic composition of as-dep and CCT CdTe grown at different voltages along with their changes in Cd/S ratio. It depicts that for the both the AD and CCT layers grown at different voltages, Cd percentage increase with the increment of the growth voltage, which agrees with the cyclic voltametric analysis above. It is also observed that the layers show a tendency of having lower percentage of Cd upon $CdCl_2$ heat-treatment. This trend was visible for previous electrodeposition of CdTe works as well [7], [15], [23]. A possible explanation behind this phenomenon is that, the chloride treatment takes down the melting point of CdTe crystal and in the process the layer loses some Cd by evaporation upon the heat-treatment [28], [29]. Despite having concerns about accuracy, EDX technique and this analysis give a qualitative idea about the composition of the CdTe

films and the near-stoichiometric growth potential for the process. This identification of stoichiometry confirms the structural analysis using XRD and the achievement of highest crystallinity at 1315 mV.

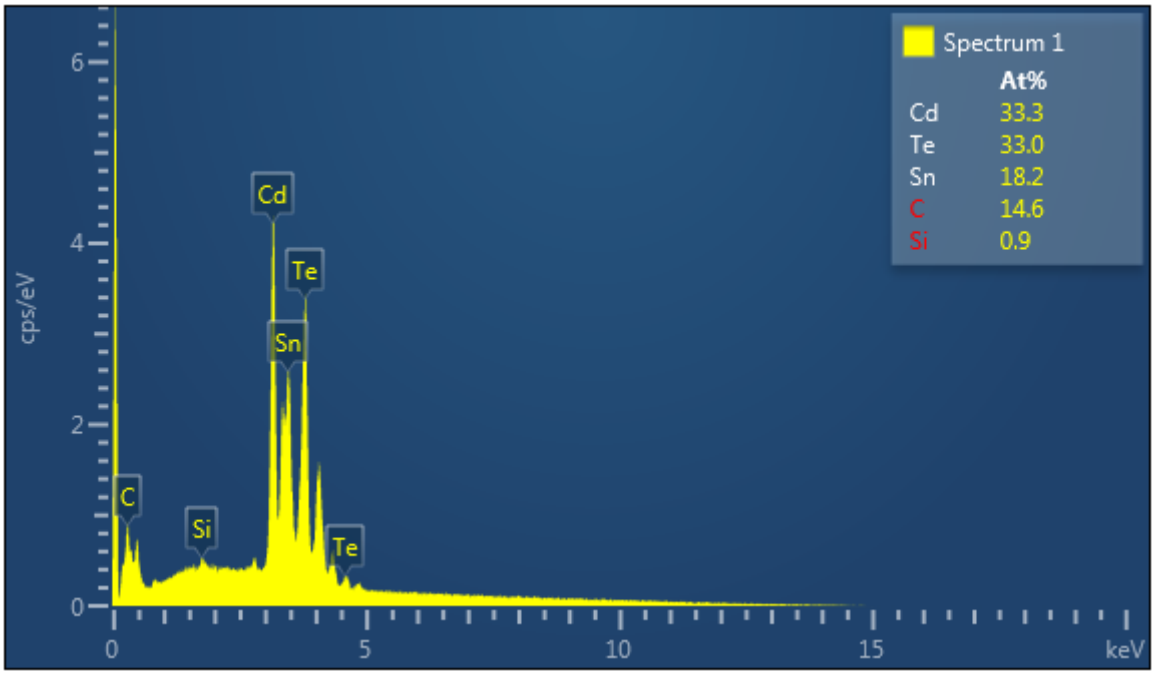


Fig 5.5 EDX spectra of the as-deposited CdTe film grown at 1315 mV

Table 5.2 Compositional analysis of as-deposited and $CdCl_2$-treated CdTe layers at different growth voltages

Sample	**Growth voltage, Vg (mV)**	**Atomic composition (%)**		**Cd/Te ratio**
		Cd	**Te**	
As-deposited	1310	49.20	50.80	0.96
	1315	50.33	49.67	1.01
	1320	51.96	48.04	1.08
$CdCl_2$-treated	1310	44.66	55.34	0.81
	1315	49.60	50.40	0.98
	1320	51.80	48.20	1.07

5.7 Photoelectrochemical Cell (PEC) measurement

PEC measurements were carried out to determine the conduction type of the electrodeposited layers. The measurement is taken by dipping a glass/FTO/CdTe layer along with another carbon rod as the counter electrode into an electrolyte prepared from 0.1M $Na_2S_2O_3$ (sodium thiosulphate) aqueous solution. As described in chapter 3, the

potential difference between the electrodes under dark (V_D) and illuminated (V_L) condition is measured to determine the conduction type of the semiconductor layer. This difference ($V_L - V_D$) represents the open circuit voltage of the solid/liquid junction and is commonly referred as the PEC signal. Polarity of the PEC signal indicates the conduction type. In this work, negative polarity of the PEC signal indicates to n-type semiconductor and positive polarity indicates to p-type semiconductor, whereas for metals, insulators, intrinsic and heavily doped semiconductors PEC signal is ideally zero [30], [31].

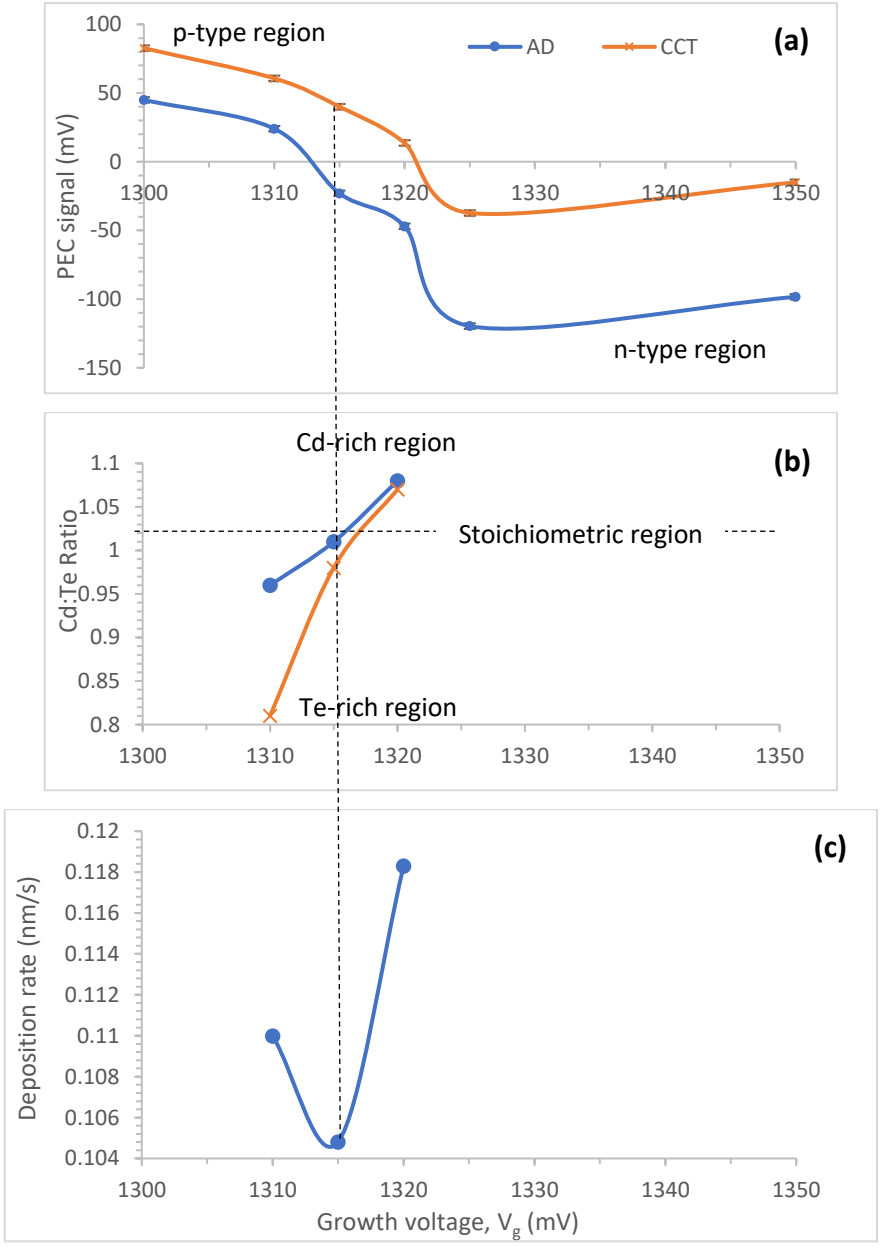


Fig 5.6 Variation of (a) PEC signal, (b) Cd:Te compositional ratio and (c) rate of thin-film growth as a function of applied cathodic deposition potential for the CdTe layers grown between 1300 - 1350 mV.

Figure 5.6 shows that the CdTe layers change in conductivity type with increasing cathodic potential. As explained in the section 5.3 at lower cathodic potential, the grown AD layers are Te-rich, hence p-type and at around 1315 mV the layers grown are nearly stoichiometric which in terms of conduction type translate into i-type material. As deposited layers grown at higher potentials than 1315 mV shows a Cd-rich composition and n-type in conductivity. As per the chronoamperometric studies above, it is also observed in figure 5.6 I is that, at the stoichiometric voltage (V_i) the deposition rate is the slowest which is consistent to the previous literature [32].

PEC measurements of the CCT-CdTe layers show a slight shift of conductivity type towards the p-type region which goes very well with the shift of Cd:Te composition depicted in 5.6 (b). Identification of the stoichiometric voltage (Vi) serves an important purpose since this enables to grown p, I and n type CdTe on top of each other from the same bath, for device fabrication.

5.8 Optical absorption analysis

5.8.1 Band gap studies with Tauc Analysis

Optical absorption study has been carried out using Carry 50 scan UV-Vis spectrophotometer, for AD and $CdCl_2$ treated CdTe layers deposited at different growth voltages. The obtained absorption data within the wavelength of 300 nm to 1000 nm, have been used to plot an alternative Tauc plot, where square of absorbance (a^2) is plotted against photon energy (hv). The intersection of extrapolated tangent line derived from the curve, gives the direct band-gap (E_g) of the studied semiconductor material.

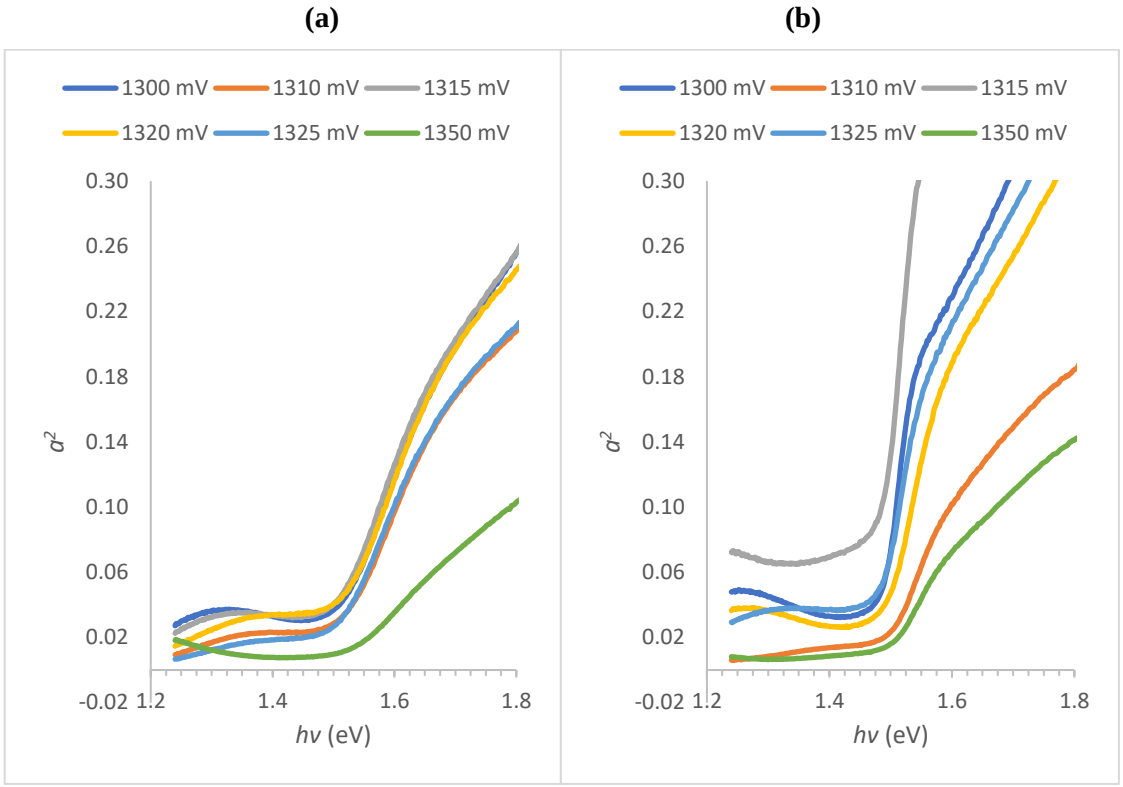


Fig 5.7 a^2 vs *hv* plots for **(a)** As-deposited and **(b)** $CdCl_2$-treated (at 400° C for 20 minutes in air) CdTe samples.

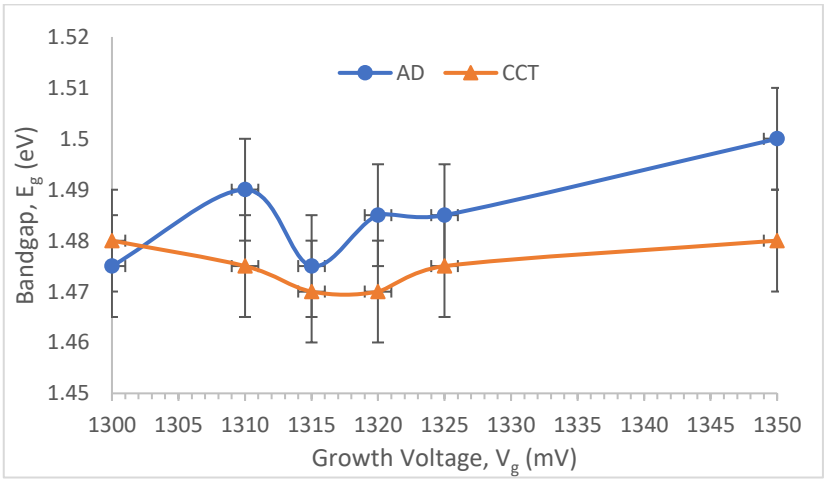


Fig 5.8 Change of bandgap for CdTe samples due to the change of growth potential

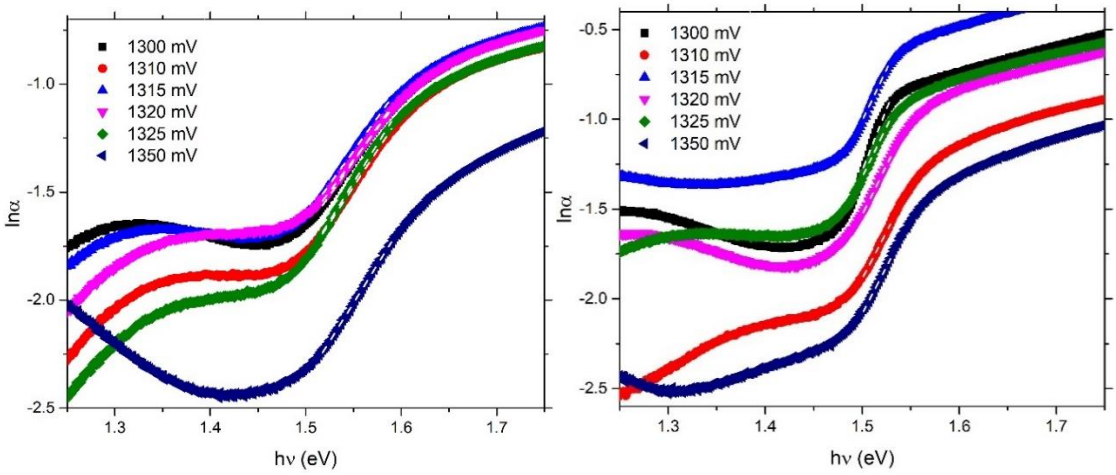
According to figure 5.7 (a) and figure 5.8, as-deposited CdTe layers show direct band-gaps ranging between ~1.47 eV to ~1.50 eV which is within the range of experimental error. $CdCl_2$-treated CdTe layers depict a similar trend as per figure 5.7 (b) and figure 5.8, but after $CdCl_2$-treatment, band-gap decreases overall compared to that of the AD layers. Band-gaps of the CCT layers range between ~1.47 eV and ~1.48 eV which also are well within the experimental error. However, the slope of the tauc plot indicates to the layer

quality at different growth voltages where the layers grown at 1315 mV shows the steepest slope at both AD and CCT condition.

5.8.2 Urbach energy Analysis

From the optical absorption data, it is also possible to qualitatively have an idea about the probable presence of band tail induced defect levels within the bandgap of the material. Though Urbach analysis more suitably predicts defect positions at the absorption edges of amorphous materials, it is also widely used for nano-crystalline materials [33]–[35]. By plotting a ln*a* vs *hv* graph where *a* is the absorption and *hv* is the photon energy, it is possible to find the slope from the linear portion of the exponential curve, which is the reciprocal of Urbach energy ($1/E_U$) [36]. As previously mentioned in section 4.4.6.2, the calculated Urbach energy (E_U) qualitatively indicates the temperature dependant width of the band tail or in other words possible absorption points near the band edge of the thin film at a particular temperature. Figure 5.9 (a) and (b) below show the ln*a* vs *hv* plot for all the AD and CCT CdTe layers. Figure 5.9 (c) depicts that E_U ranges between a narrow range of ~0.14 eV to ~0.17 eV for the AD CdTe layers grown at different growth voltages, which means that at room temperature AD-CdTe layers contain localised electronic states just ~0.14 eV to ~0.17 eV above the valence band, which also is within the range of experimental error. It is also visible that the band tail width goes even lower (~ 0.07 to ~0.09 eV) after the layers are $CdCl_2$-treated. For a material having ~1.50 eV bandgap, this band tail width is negligible in terms of device design. This reconfirms the quality of the electrodeposited CdTe layers and their further improvement upon $CdCl_2$ treatment.

(a) **(b)**



(c)

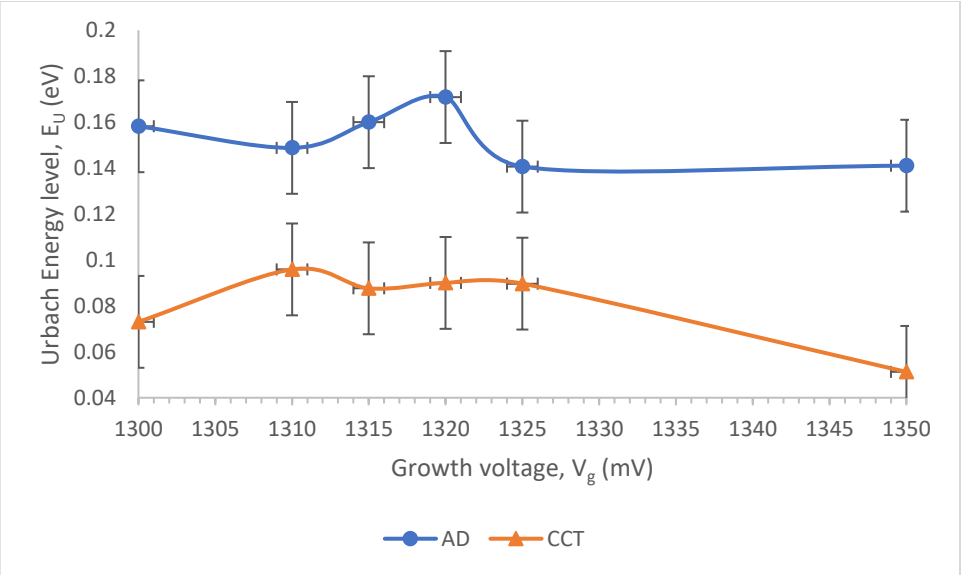
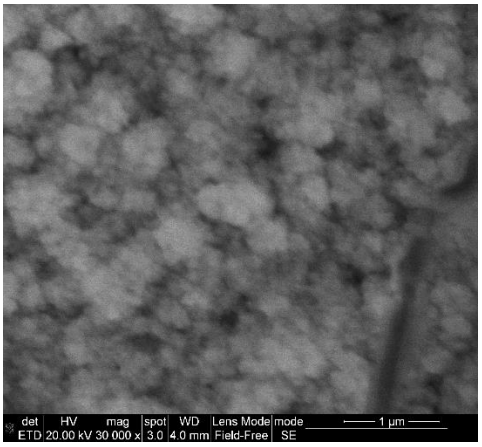


Fig 5.9 ln*a* vs *hv* plot for the **(a)** AD and **(b)** CCT CdTe layers grown between 1300 mV and 1350 mV, along with their **(c)** calculated Urbach Energies (E_U) at room temperature.

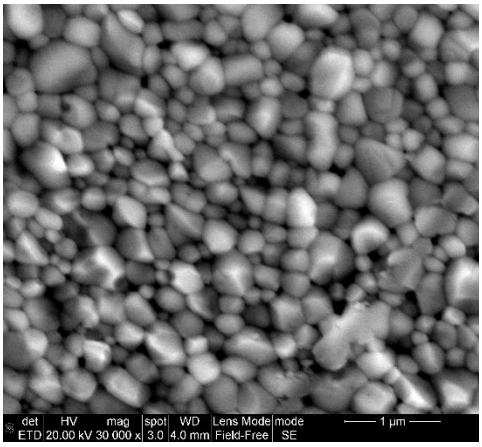
5.9 Scanning electron microscopic (SEM) analysis

Morphological characterisation of the CdTe layers has been done in the form of micrographs using Quanta 3D FEG SEM instrument using 15.0 kV electron beam voltage and 30,000× of magnification. SEM images of glass/FTO/CdTe substrates have been taken for both as-deposited and $CdCl_2$-treated samples grown at 1310 mV, 1315 mV and 1320 mV (figure 5.10). In figure 5.10 (a, c and e) all the AD-CdTe surfaces demonstrate agglomerated CdTe crystallites, which turn into clearly visible grains as shown in figure 5.10 (b, d and f) upon the $CdCl_2$-treatment. It is also visible that layers grown at V_i (1315 mV) shows the largest grain size (up to ~500 nm) after post growth treatment. The grain size is very similar to that of the CdTe layers grown from very high purity Cd-precursors [7].

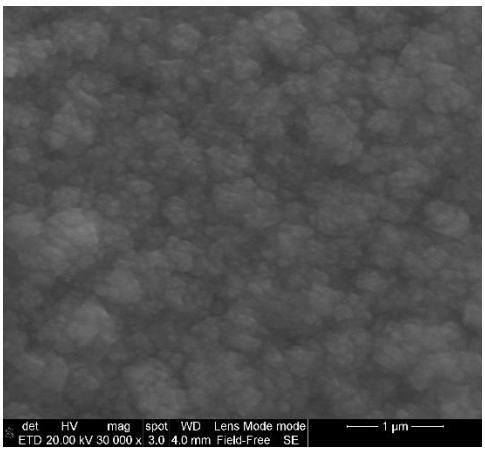
(a) AD at 1310 mV



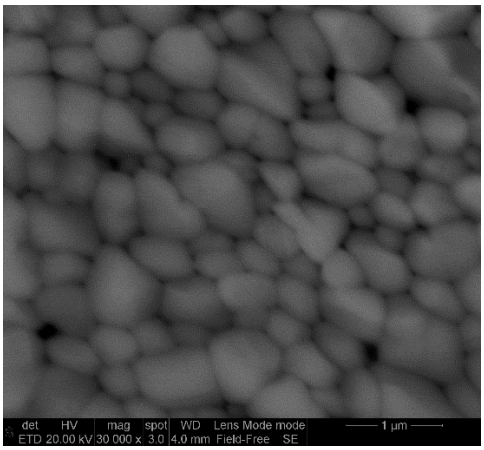
(b) CCT at 1310 mV



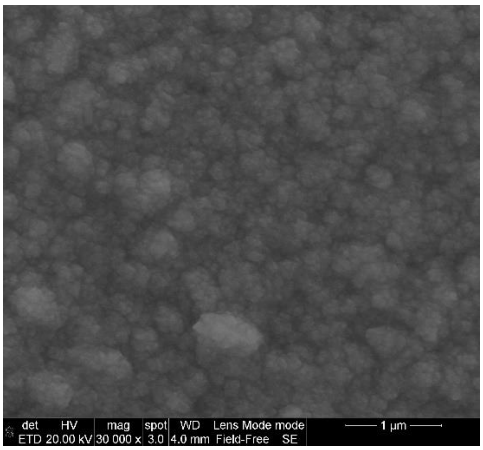
(c) AD at 1315 mV



(d) CCT at 1315 mV



(e) AD at 1320 mV



(f) CCT at 1320 mV

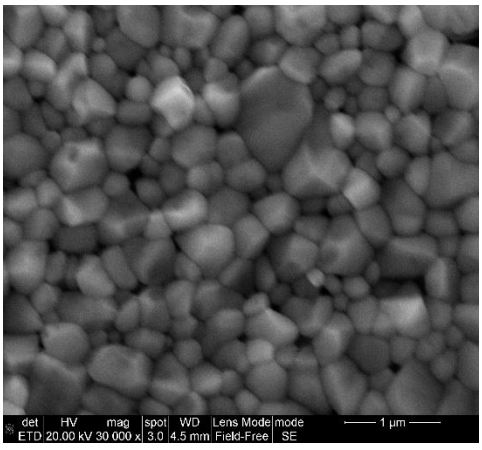


Fig 5.10 Typical SEM images of CdTe thin films grown at 1310 mV, 1315 mV and 1325 mV **(a, c, e)** as-deposited and **(b, d, f)** $CdCl_2$-treated at 400^o C for 20 minutes in air

5.10 Conclusion

In this work, the main absorber material for the designed PV cell structure, CdTe, has been electrodeposited using comparatively lower purity Cd precursor. Extensive electro-purification process has been performed to reduced possible impurities in the bath. The grown layers within the primarily selected voltage range from electrochemical analysis, have shown good cubic crystallinity, which became better upon $CdCl_2$-treatment. The layers have shown a transition in Cd:Te composition as well as in conduction type from Te-rich p-type to Cd-rich n-type CdTe layers. The growth voltages have been optimised to be ~1315 mV where stoichiometric (Cd:Te ≈ 1) CdTe is deposited having an i-type conductivity along with the best crystallinity amongst the grown layers, comparable to the previously reported CdTe electrodeposited from higher purity Cd-precursors. In terms of structural, optical and morphological properties the CdTe layers grown in this project show close proximity to their previously grown counterparts from higher purity precursors. However, chances of possible impurity inclusion detrimental for devices can still exists in the films, for which further opto-electronic characterisations such as, DC conductivity, dark IV analysis, photoluminescence (PL) etc can be carried out.

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Chapter 6

Growth and characterisation of potential wide bandgap n-type hole back-diffusion barrier (hbdb) layers

6.1 Introduction

As discussed in chapter 2, between the two proposed approaches of graded bandgap devices on n-type and p-type window materials, cells fabricated on p-type windows have a potential of achieving high performance due to its possibility of producing higher open circuit voltage (V_{oc}). This was experimentally demonstrated by achieving V_{oc} = 1.175 mV with GaAs/AlGaAs system [1] and perovskite based devices [2].

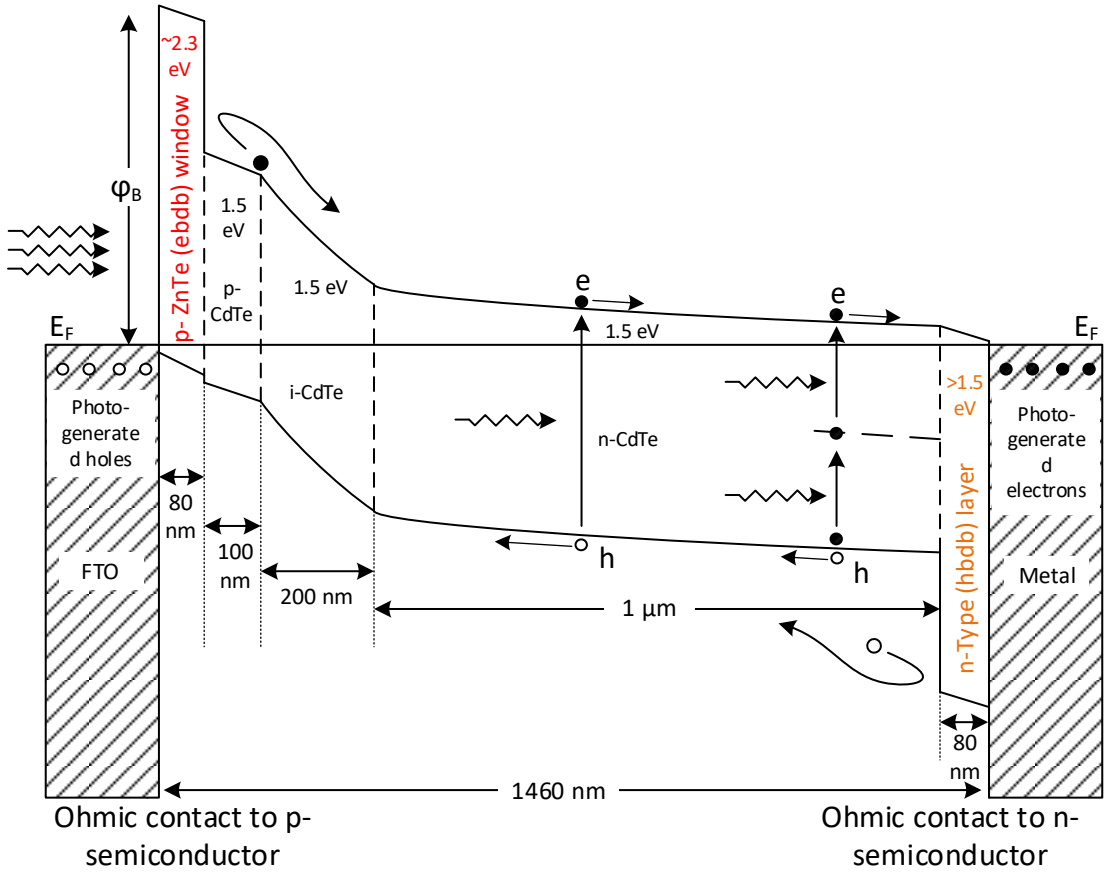

Fig 6.1 Energy band diagram drawn to scale for a short-circuit multi-layer solar cell based on p-type window material (p^+-p-i-n-n^+ structure). P^+ and n^+ layers act as electron back diffusion barrier (ebdb) layer, and hole back diffusion barrier (hbdb) layer respectively

In this project, the current efforts are focused on developing CdTe-based graded bandgap devices with p-type windows, using low-cost and scalable electro-plated materials. For multilayer GBG solar cells, apart from the regular window layer and absorber layer,

improvements can be made by including an electron back-diffusion barrier (ebdb) layer and a hole back-diffusion barrier (hbdb) layer [3]. This will minimize the recombination of photo-generated and separated charge carriers by thermionic emission over the potential barrier [3]–[5], as depicted in figure 6.1. However, point to be noted is that the device design presented in figure 6.1 is not a fully graded bandgap device, since the only gradation taking place is at the window-absorber interface. This device architecture has been chosen as an initial step to further grade the device upon expected outcome. In the Chapter 4, the author has deposited, characterised and optimised three potential ebdb layers and decided p-ZnTe to be the potential wide bandgap window layer for CdTe-based devices. In this chapter, deposition and characterisation of CdS and comparison with n-ZnTe layer have been discussed in order to decide the potential hbdb layer for the device design (fig 6.1).

6.2 Growth and Characterisation of CdS

n-CdS is widely used as the window layer in electroplated graded bandgap solar cells developed with n-window approach. The most widely used cadmium (Cd) precursor is $CdCl_2$ in this case [6], [7]. But for electrodepositing CdS as a wide-bandgap hole back diffusion barrier (hbdb) layer, precursors should be chosen very carefully because, in this case the whole glass/FTO/p-window/CdTe absorber layer would require to be submerged into the CdS electrolytic bath. Chlorine being a very strong corrosive agent and for having the strong hydrochloric acidity due to Cl^- and H^+ ions in the electrolyte, the underlying device structure can be dissolved [8]. Therefore, cadmium acetate [$Cd(CH_3COO)_2$] precursor with weaker acidity has been used in this work.

Moreover, literature suggests sodium thiosulphate ($Na_2S_2O_3$) as the most widely used sulphur precursor for CdS electrodeposition. But, this precursor tends to provide accumulation of sodium (Na), a p-type dopant in the CdS bath, which by incorporating through absorption or reaction may reduce the electrical conductivity of the CdS layer [9]. Hence, ammonium thiosulphate [$(NH_4)_2S_2O_3$] has been used as the S precursor in this work.

This work focuses on growing ED CdS with the mixture of these precursors for the first time along with investigating through the growth potential and post-annealing characteristics. The aim is to grow n-CdS to be used as an hbdb layer suitable to be deposited on glass/TCO/p-window/CdTe-absorber layer for developing graded bandgap devices in future.

6.2.1 Experimental procedure

Cadmium Sulphide (CdS) thin-film layers were grown from a 400 ml aqueous solution of 99% pure 0.3M Cadmium Acetate dihydrate [$Cd(CH_3COO)_2.2H_2O$] and 99.5% pure 0.06M Ammonium thiosulphate [$(NH_4)_2S_2O_3$] in de-ionised water. All these chemicals have been purchased from Sigma-Aldrich Ltd (UK). The pH and temperature of the solution has been kept constant at 3.00 ± 0.02 and ~ 85^o C respectively. pH of the bath for the hbdb deposition has been deliberately kept more basic than the CdTe electrolytic bath (2.00 ± 0.02) in order to avoid possible acid erosion of the absorber layer during device fabrication. The pH has been adjusted using either nitric acid or ammonium hydroxide (NH_4OH). Two-electrode electrodeposition technique has been used for depositing the semiconductor materials on Glass/ TEC-7 Fluorine doped tin oxide (glass/FTO) substrates having sheet resistance of ~7 Ω/square. High purity carbon rod has been used as the anode whereas, cathode (working electrode) has been prepared by attaching a glass/FTO substrate to a carbon rod using insulating Polytetrafluoroethylene (PTFE) tape. Prior to electrodeposition, the substrates were cut into 3 cm × 3 cm dimension and rinsed thoroughly with de-ionized water after washing with soap solutions using cotton buds. The samples were later dried with nitrogen gas. GillAC potentiostat from ACM Instruments is used as the power source for the 2-electrode ED system. The electrolytic solution was heated and stirred using a hot plate and magnetic stirrer. Moderate stirring rate has been applied to the bath throughout the electrodeposition process.

Cyclic voltammogram has been carried out to determine an estimated range of deposition potential where Cd and S co-association takes place. The deposited layers were investigated using Energy Dispersive X-ray (EDX) spectroscopy for compositional and material identification analysis, X-ray diffraction (XRD) and Raman spectroscopy for structural analysis and Scanning electron microscopy (SEM) for morphological analysis. For characterising and optimising electrical and optical properties of the ED samples, photoelectrochemical (PEC) cell measurements and optical absorption using UV-Vis spectrophotometry have been carried out.

6.2.2 Cyclic voltammetric Study for CdS bath

Cyclic voltammograms were separately recorded for electro-purified aqueous electrolytes containing 0.3M $Cd(CH_3COO)_2.2H_2O$, 0.06M $(NH_4)_2S_2O_3$ and a mixture of 0.3M $Cd(CH_3COO)_2.2H_2O$ and 0.06M $(NH_4)_2S_2O_3$. The pH and temperature of the solutions were adjusted to 3.00 ± 0.02 and ~85° C respectively. The cyclic sweep is recorded with a sweep rate of 3 mVs^{-1} within a cathodic potential range of 0.0 mV to 2000 mV. Figure 6.2 depicts a typical voltammogram data plotted with instructive symbols and legends.

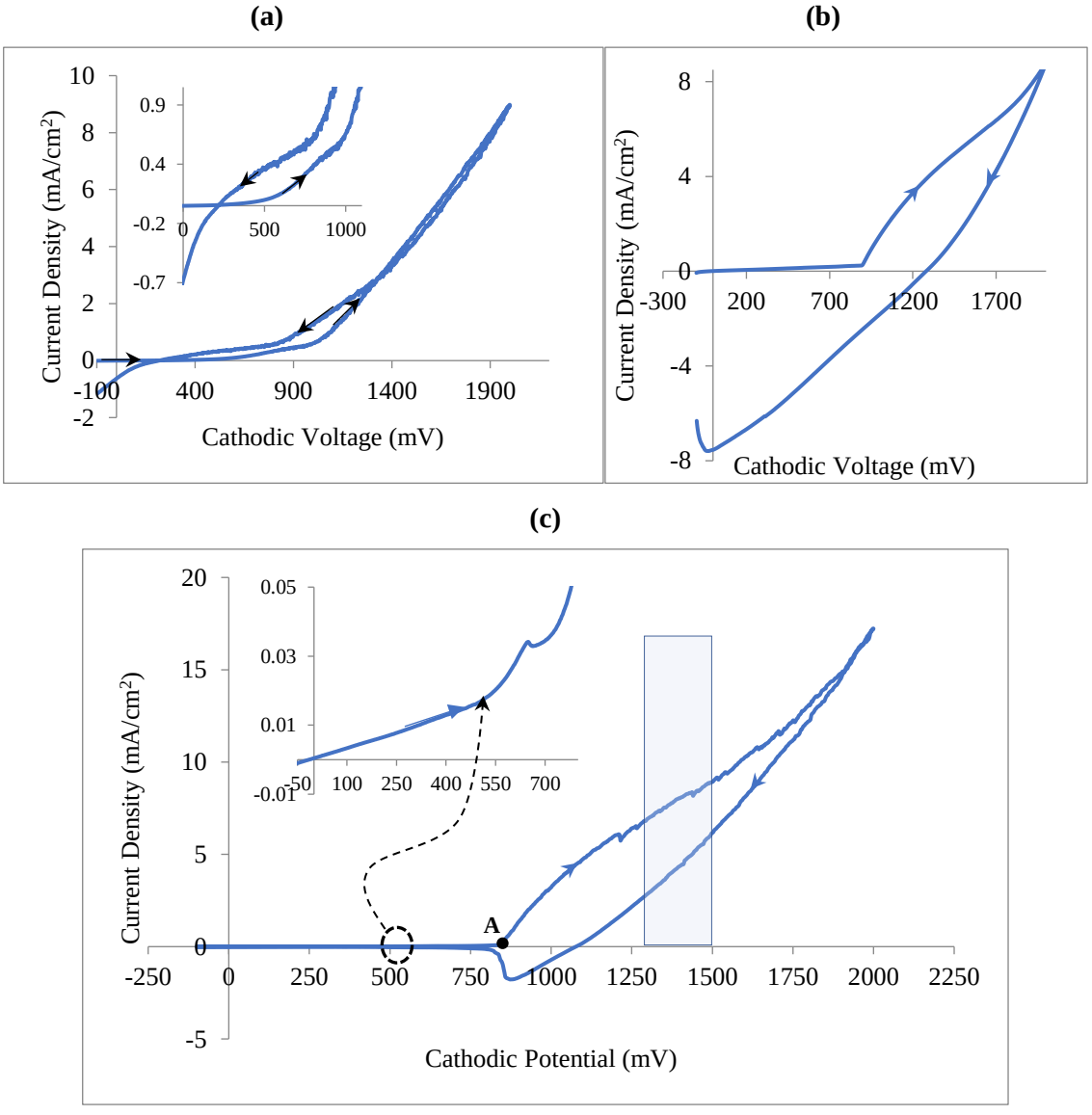

Fig 6.2 Typical cyclic voltammogram of aqueous solution containing **(a)** 0.06M $(NH_4)S_2O_3$, **(b)** 0.3M $Cd(CH_3COO)_2.2H_2O$ [cadmium acetate dihydrate] and **(c)** mixture of 0.3M $Cd(CH_3COO)_2.2H_2O$ and 0.06M $(NH_4)S_2O_3$ in de-ionised water. pH and temperature of the solution were kept at 3.00 ± 0.02 and ~85° C

Figure 6.2(a) depicts, due to the difference of redox potentials amongst the consisting ions, in the forward cycle of voltammogram Sulphur (S) having a redox potential (E^o) of +0.449 V (with reference to standard H_2 electrode) [10], starts depositing at the beginning at ~500 mV. The deposition takes place from the S precursor, according to the electro-chemical reaction equations 6.1 and 6.2:

$$(NH_4)_2S_2O_3 \rightarrow 2NH_4^+ + S_2O_3^{2-} \qquad (6.1)$$

$$S_2O_3^{2-} + 6H^+ + 4e \rightarrow S + 3H_2O \qquad (6.2)$$

Later, Cd having an E^o of -0.403 V (w.r.t. standard H_2 electrode) [10], starts depositing at ~850 mV (Figure 6.2(b) and point A in figure 6.2(c)) according to the electro-chemical reaction equation 6.3:

$$Cd^{2+} + 2e \rightarrow Cd \qquad (6.3)$$

Hence, figure 6.2(c) shows the co-deposition of cadmium and tellurium begins hereafter and S-rich CdS starts to deposit from ~850 mV onward according to the reaction equation 6.4. As higher cathodic voltage is applied, Cd starts increasingly incorporating to the layer.

$$Cd^{2+} + S_2O_3^{2-} + 6H^+ + 6e \rightarrow 2CdS + 3H_2O \qquad (6.4)$$

Therefore, it is estimated that near-stoichiometric CdS layer can be found within a range of ~1300 mV to ~1500 mV of growth potential. From 1500 mV onward, there is a relatively higher increment in current density, which indicates the possible dissociation of water.

In the reverse cycle of figure 6.2(c), the negative peak at ~850 mV reconfirms the dissolving of any elemental Cd as well as dissociation of CdS formed on the FTO surface.

6.2.3 X-ray diffraction (XRD) analysis

Aim of this analysis is to carry out the structural analysis of the deposited layers at different growth voltages. Philips PW X'Pert diffractometer has been used with Cu-Kα monochromator having a wavelength of 1.54 Å, where the source tension and current were kept as 40 kV and 40 mA respectively. XRD measurements have been carried out on 5 as deposited (AD) and heat-treated samples grown at 1420, 1430, 1440, 1450 and 1460 mV cathodic potentials. In figure 6.3(a), at $2\Theta \approx 26.6^o$ and $\approx 30.0^o$ the as-deposited

samples show XRD peaks corresponding to the diffraction from CdS (111) cubic/ (002) hexagonal and CdS (200) cubic peaks respectively. It is difficult to differentiate between CdS (111) C and (002) H plane because they coincide within 1%, therefore the XRD peak is often considered as resultant from mixed structures [11], [12]. Also, increment in the dominant peak intensity for AD CdS layers indicates the coinciding of CdS (111)C / (002)H peak with the underlying FTO (110) peak. After heat-treatment it is widely observed that CdS transforms phase from cubic/mixed to completely hexagonal CdS [7], [9]. Likewise, figure 6.3(b) shows, after the heat-treatment of the layers at 400° C for 20 minutes, whereas CdS (002) H plane still stays the preferred orientation at $2\Theta \approx 26.6^{o}$, the (200) C plane completely disappears and CdS (110) H plane comes into appearance at $2\Theta \approx 43.9^{o}$. This indicates the phase transition of the material from cubic/mixed to hexagonal. For the dominant planes resulting from different growth voltages, the trajectory shows that peak intensity keeps gradually increasing up to 1450 mV and then goes down. Figure 6.4 depicts this trend for both the as-deposited and heat-treated CdS samples. Along with the peak intensity, change of the CdS crystallite size due to growth voltage is shown in table 6.1 for both the AD and HT samples. Crystallite size at the preferred orientation has been calculated using Scherrer's formula given by equation (6.5).

$$D = \frac{0.9\lambda}{\beta cos\theta} \qquad (6.5)$$

where wavelength, $\lambda = 1.54$ Å, β = full width at half maximum (FWHM) of the diffraction peak in radian and θ = Bragg's angle of incidence. k = 0.9 was used since the exact value of k for the present material system is not known. The calculated crystallite size is only an estimate.

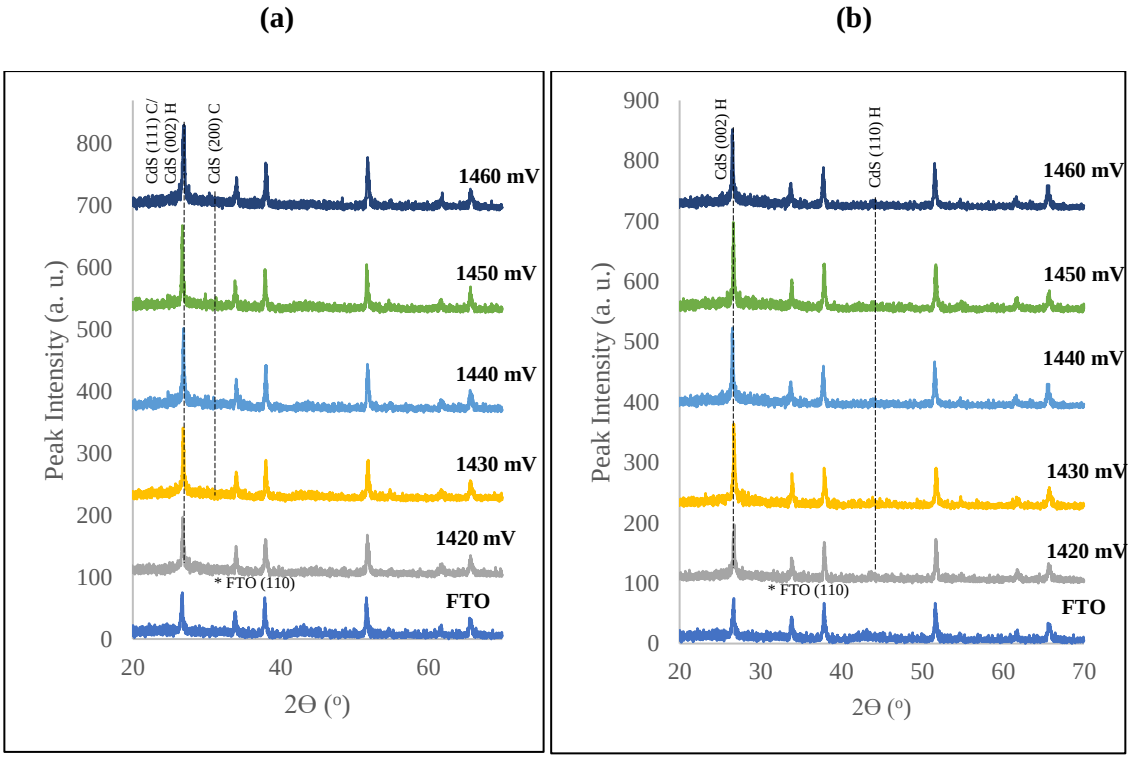

Fig 6.3 XRD patterns of CdS thin films grown at Vg range from 1420-1460 mV **(a)** for as-deposited and **(b)** after heat treatment for 20 minutes under 400º C in air

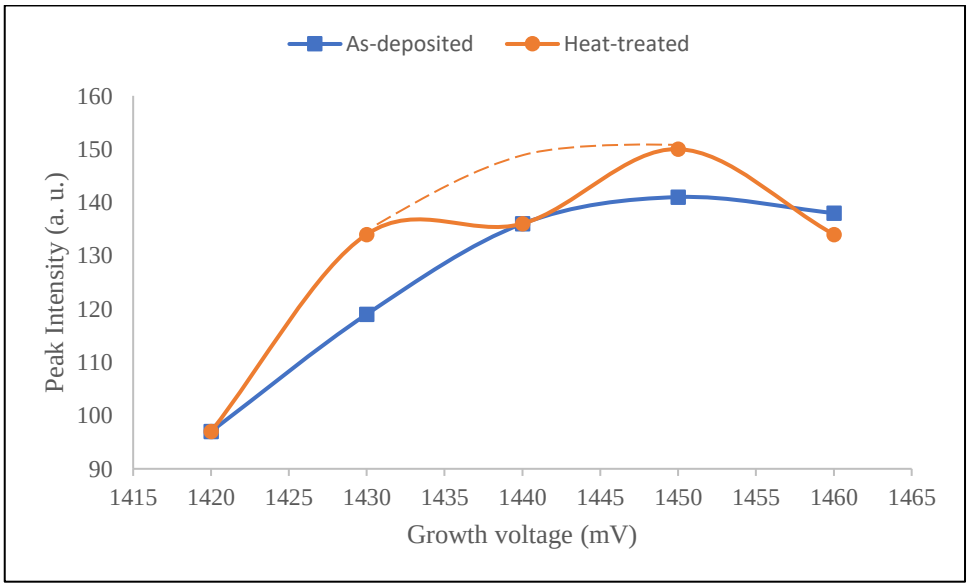

Fig 6.4 Comparative analysis of dominant peak intensities for AD and HT layers grown at different cathodic voltages

Table 6.1 shows that the as-deposited samples grown at 1450 mV has the largest crystallite size among the others. For HT samples, the trend carries on and all the HT samples show larger crystallite size than their as-deposited counterparts.

Table 6.1 XRD analysis of *as-deposited* and heat treated CdS layers with the increasing Vg from 1420-1460 mV

Sample	**Growth Voltage, Vg (mV)**	**Peak Position, 2Θ (º)**	**D-spacing (Å)**	**FWHM (º)**	**Crystallite size, D (nm)**	**Lattice strain (A. U.)**	**Plane of orientation (h k l)**	**Assignments**
As-deposited	1420	26.75	3.33	0.27	32.20	0.0049	(111)/(002)	Cubic CdS/ hexagonal CdS
	1430	26.70	3.33	0.25	34.82	0.0045		
	1440	26.54	3.36	0.23	37.57	0.0042		
	1450	26.65	3.34	0.21	40.62	0.0039		
	1460	26.54	3.35	0.34	25.08	0.0063		
Heat-treated	1420	26.77	3.33	0.24	35.85	0.0044	(002)	Hexagonal CdS
	1430	26.77	3.33	0.23	37.42	0.0042		
	1440	26.77	3.33	0.21	41.02	0.0038		
	1450	26.66	3.34	0.20	43.75	0.0036		
	1460	26.90	3.31	0.20	42.68	0.0035		

However, all CdS layers grown here on the TEC-7 glass/FTO substrates show overlaps of the dominant CdS plane with the dominant FTO (110) plane at $2\Theta \approx 26.6^{o}$. Since, the first batch of FTO substrates shown the preferred FTO orientation at $2\Theta \approx 26.6^{o}$, for reconfirmation, another CdS layer has been deposited at the best apparent growth voltage (~1450 mV) on another batch of substrate having a different preferred orientation. Figure 6.5 shows that, CdS layers grown on a substrate having a preferred orientation elsewhere, also depicts a sharp peak intensity at $2\Theta \approx 26.6^{o}$ for both as-deposited and heat-treated samples. The AD layer demonstrates cubic/mixed phase, which transforms into a hexagonal phase after heat-treatment at 400^{o} C for 20 minutes, like the previous batch shown in figures 6.3 and 6.4.

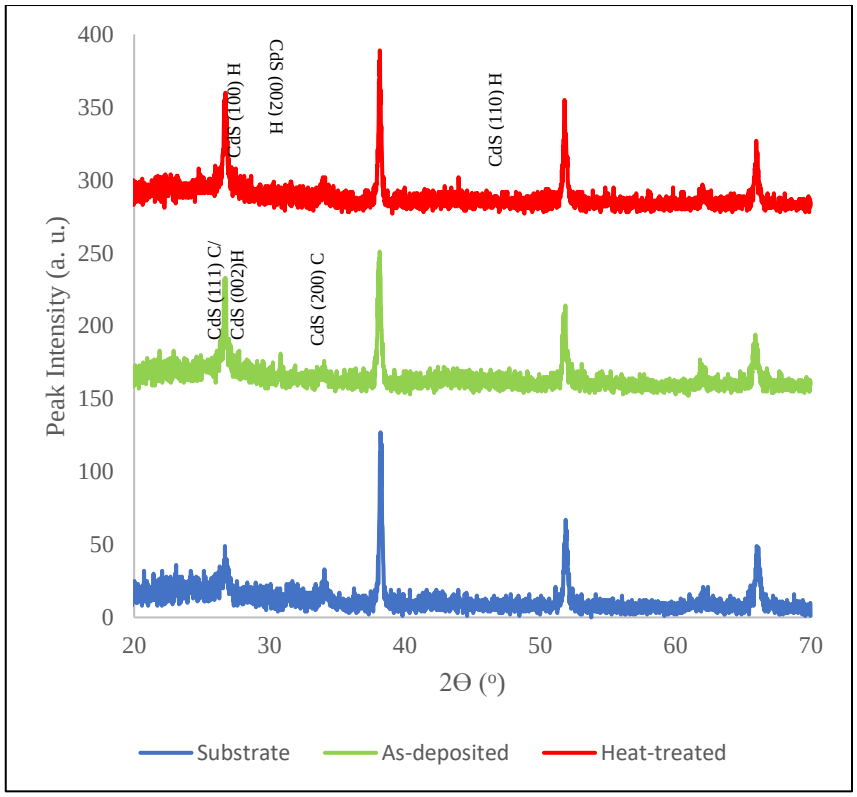

Fig 6.5 XRD patterns of CdS layers grown on alternative substrate having different preferred orientation reconfirms the above results

6.2.4 Energy dispersive X-ray (EDX) spectroscopy

EDX was carried out on the as-deposited and heat-treated CdS samples grown at 1430, 1440 and 1450 mV, using the compositional analysis software associated with the Quanta 650 SEM equipment, in order to obtain the chemical composition of the samples. The heat-treated samples were annealed at 400^{o}C for 20 minutes in air. Figure 6 shows the EDX spectra of the as-deposited and heat-treated sample grown at 1450 mV. Table 6.2 presents the atomic composition of as-dep and HT CdS grown at different voltages along with their changes in Cd/S ratio. It depicts that all the as-deposited layers are S-rich in nature regardless the growth potential, whereas after heat treatment all of them shows slight comparative decrement in S percentage which resulted the HT sample grown at 1450 mV reaching stoichiometry. Despite having concerns about accuracy, EDX technique and this analysis gives a qualitative idea about the composition of the CdS films and an assumption about the near-stoichiometric point for the process. This achievement of stoichiometry confirms the structural analysis using XRD and the achievement of highest crystallinity at 1450 mV. Any thin-film layer with only one phase tend to crystallise better during this growth process.

(a) **(b)**

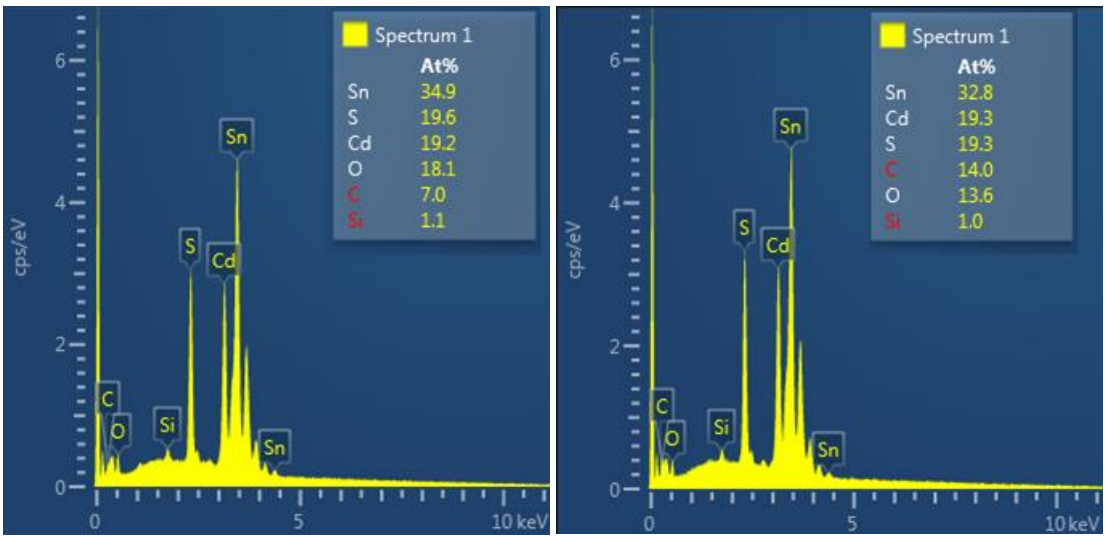

Fig 6.6 EDX spectra of the **(a)** as-deposited and **(b)** heat-treated CdS films grown at 1450 mV

Table 6.2 Compositional analysis of as-deposited and heat-treated CdS layers at different growth voltage

Sample	**Growth voltage, Vg (mV)**	**Atomic composition (%)**		**Cd/S ratio**
		Cd	**S**	
As-deposited	1430	49.61	50.39	0.98
	1440	49.23	50.77	0.97
	1450	49.50	50.50	0.98
Heat-treated	1430	49.66	50.34	0.99
	1440	49.45	50.55	0.98
	1450	50.00	50.00	1.00

6.2.5 Photoelectrochemical Cell (PEC) measurement

PEC measurements were carried out to determine the conduction type of the electrodeposited layers. The measurement is taken by dipping a glass/FTO/CdS layer along with another carbon electrode into an electrolyte prepared from 0.1M $Na_2S_2O_3$ (sodium thiosulphate) aqueous solution. The voltage difference between the electrodes under dark (V_D) and illuminated (V_L) condition is measured to determine the conduction type of the semiconductor layer. This difference ($V_L - V_D$) represents the open circuit voltage of the solid/liquid junction and is commonly referred as the PEC signal. Polarity of the PEC signal indicates the conduction type. In this work, negative polarity of the

PEC signal directs to n-type semiconductor and positive polarity directs to p-type semiconductor, whereas for metals, insulators and intrinsic semiconductors PEC signal is ideally zero. Figure 6.7 shows that all the CdS layers deposited at different cathodic potentials are n-type in conductivity as expected [6], [13]. HT samples show a stronger PEC signal compared to that of the AD samples. Strength of the PEC signal qualitatively indicates to the doping density and depletion region strength.

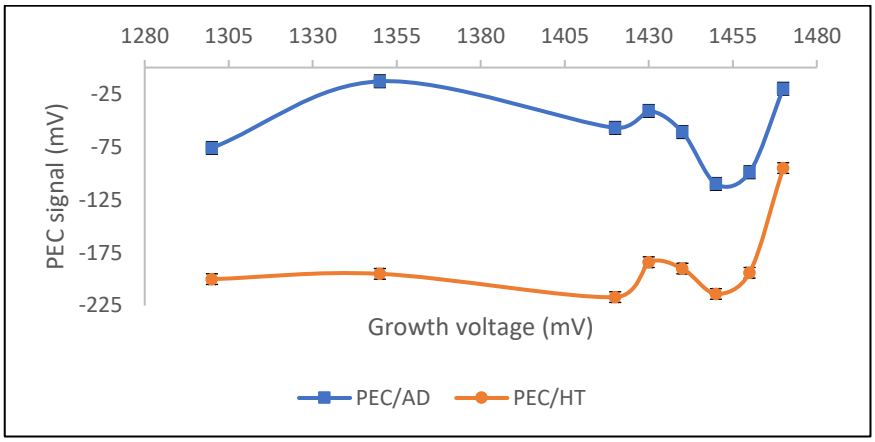

Fig 6.7 PEC signal for AD and HT CdS samples

6.2.6 Optical absorption analysis

Optical absorption study has been carried out using Carry 50 scan UV-Vis spectrophotometer, for AD and HT CdS layers deposited at different growth voltages. The obtained absorption data within the wavelength of 300 nm to 1000 nm, have been used to plot an alternative Tauc plot, where square of absorbance (a^2) is plotted against photon energy (hv) [14], [15]. The intersection of extrapolated tangent line derived from the curve, gives the direct band-gap (E_g) of the studied semiconductor material.

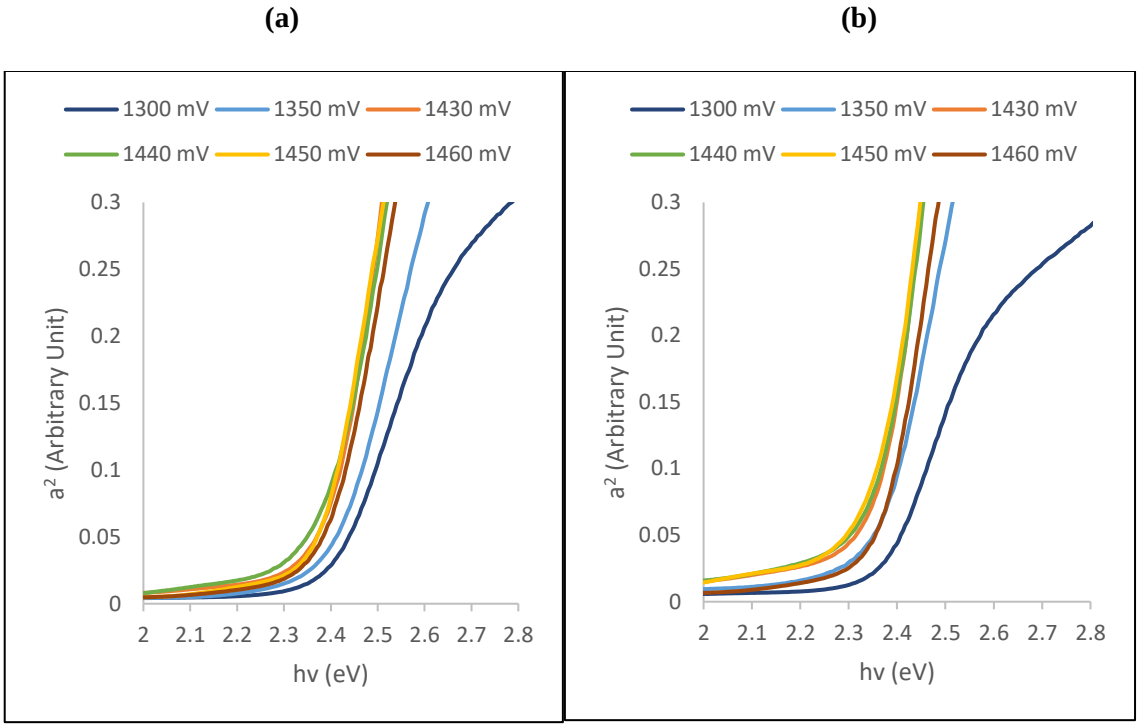

Fig 6.8 a^2 vs hv plot for **(a)** As-deposited and **(b)** Heat-treated (at 400° C for 20 minutes in air) CdS samples.

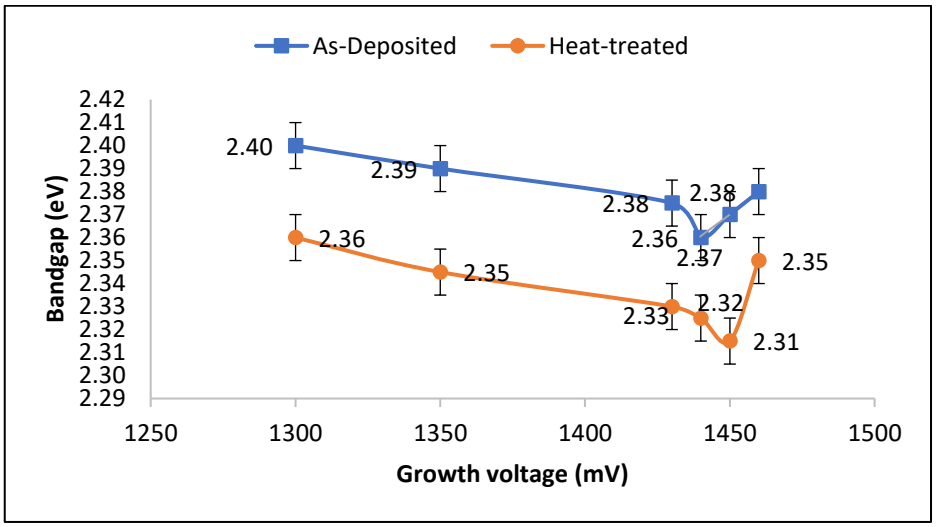

Fig 6.9 Change of bandgap for CdS samples due to the change of growth potential

According to figure 6.8(a) and figure 6.9, as-deposited CdS layers show direct band-gaps ranging between ~2.36 eV to ~2.40 eV, where the lowest band-gap value is observed at ~1450 mV of growth potential. Heat-treated CdS layers depict a similar trend as per figure 6.8(b) and figure 6.9, but after heat-treatment, band-gap decreases overall compared to that of the AD leyers. Band-gaps of the HT leyers range between ~2.31 eV and ~2.36 eV. The lowest band-gap value (~2.31 eV) for the heat-treated samples is found for the layer grown at 1450 mV and proves consistant to the bulk E_g value of hexagonal CdS; but

differs slightly from the previously measuered E_g values (~2.42 eV) for electrodeposited CdS layers in the group [7], [9], [16]. This observation is also supported by the visual appearance of the deposited layers as shown in figure 6.10. The CdS layers electrodeposited from these precursors demonstrate an orangish yellow appearance compared to the greeninsh yellow appearance of the previously electrodeposited CdS layers in the author's group [7], [14]. This indicates a possible shift in the typical absorption point of the layer from lower wavelength towards higher wavelength, and vice-versa for the band-gap energy.

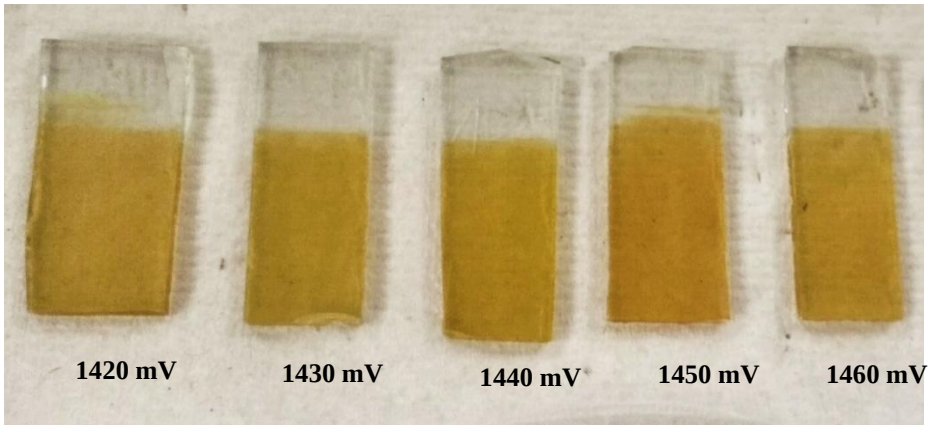

Fig 6.10 Physical appearance of the as-deposited CdS layers grown at different cathodic voltages

6.2.7 Scanning electron microscopy (SEM) analysis

In order to carry out the morphological characterisation of the CdS layers, SEM analysis has been done in the form of micrographs with Quanta 650 nano SEM instrument using 15.0 kV electron beam voltage and 32,000× of magnification. SEM images of glass/FTO/CdS substrates have been taken for both as-deposited and heat-treated samples grown at 1440 mV (figure 6.11(a-b)) and 1450 mV (figure 6.11(c-d)). In figure 6.11, at both growth voltages, regardless of heat-treatment, all the surfaces demonstrate agglomerations of CdS crystallites. From the SEM micrograph the size of the agglomerations range between ~50 nm and ~150 nm with an average grain size of ~80 nm. Therefore, individual CdS crystallites are not visible in the SEM image as calculated above in table 6.1.

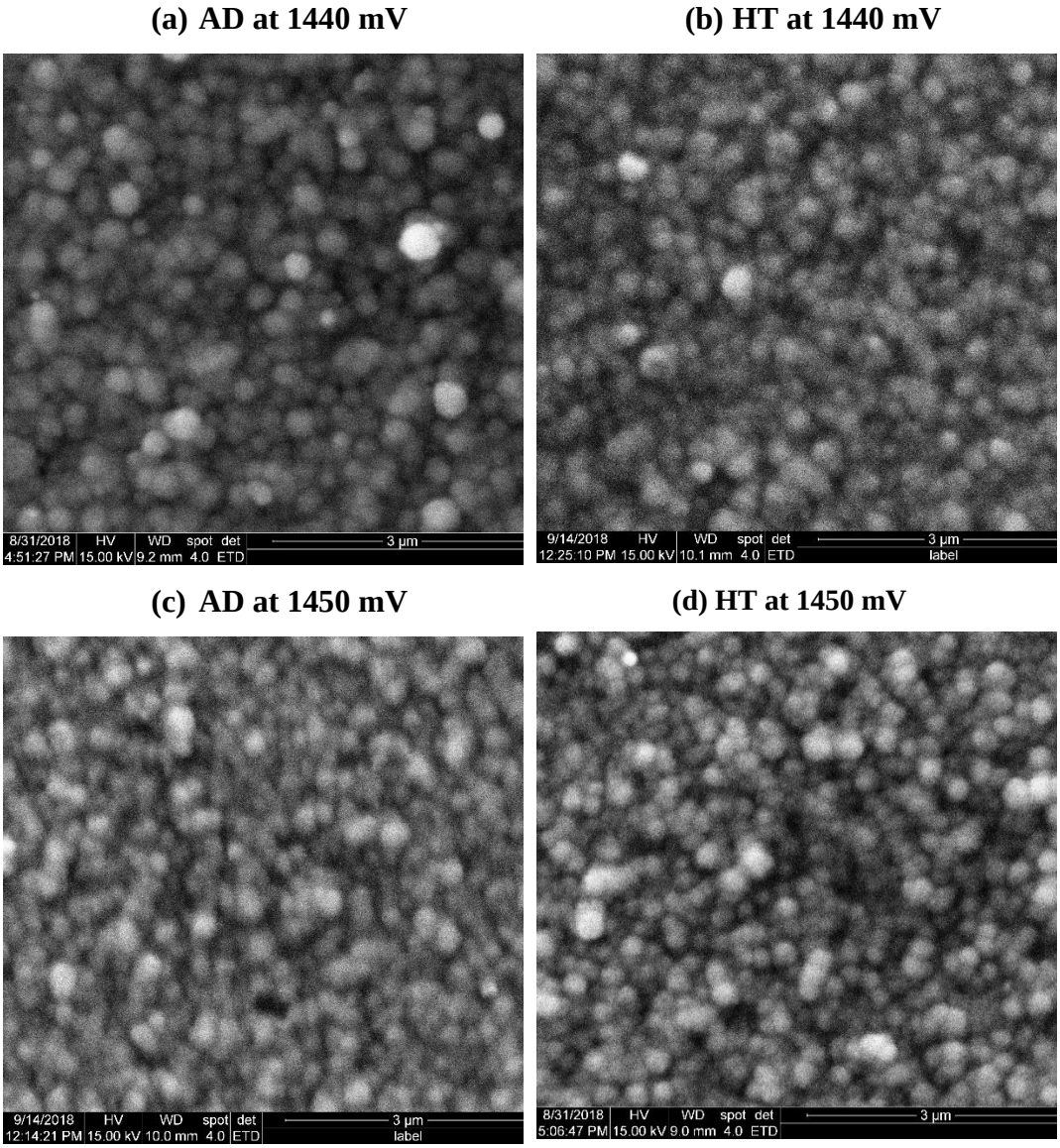

Fig 6.11. Typical SEM images of CdS thin films grown at 1440 mV and 1450 mV **(a, c)** as-deposited and **(b, d)** heat-treated at 400^{o} C for 20 minutes in air

6.3 Summary of the CdS deposition and optimisation

The main aim of this work was to electrodeposit CdS layers on top of CdTe absorber layers, in development of all-electrodeposited graded bandgap devices, starting from p-type wide-bandgap window materials. Therefore, a low acidic precursor for Cd, and Na-free precursor for S were used for the electrolyte. The optimised growth voltage was 1450 mV for experimental conditions used in this work. As-deposited materials consist of both cubic and hexagonal CdS, but turn to hexagonal CdS after heat treatment at 400^{o} C for 20 minutes in air. All the layers grown are n-type in electrical conductivity. The only

difference observed was the physical appearance of orangish colour instead of greenish yellow colour observed for CdS grown for other precursors. Accordingly, a lower bandgap energy of 2.31 eV was observed for the heat treated CdS layers. Incorporation of the layers in both graded bandgap devices based on n-type and p-type window layers are in progress.

6.4 Growth and Characterisation of n-ZnTe

As per chapter 4, ZnTe layers have been grown by mixing 2 ml of 99.995% pure TeO_2 solution into a 400 ml aqueous solution of 99.95% pure 0.015M Zinc Sulphate Monohydrate [$ZnSO_4.H_2O$]. pH of the bath for the hbdb deposition has been deliberately kept at 3.50±0.02 that is more basic than the CdTe electrolytic bath (2.00 ± 0.02) in order to avoid possible acid erosion of the absorber layer during device fabrication. Cyclic voltammogram in section 4.4.2 depicted that near-stoichiometric ZnTe layer can be found within a range of ~1500 mV to ~1700 mV of growth potential. Hence, ZnTe layers have been grown and PEC analysis showed in section 4.4.3 that layers grown at a higher voltage than that of stoichiometric voltage (1625 mV) shows an n-type conductivity upon acquiring a Zn-rich composition. Transition of elemental composition has been qualitatively proven using Sputtered Neutral Mass Spectroscopy (SNMS) in chapter 4. Whereas chapter 4 discussed technical details about the i-type and p-type materials grown at 1600 mV and 1625 mV respectively, in this chapter n-ZnTe samples of both AD and HT condition grown at 1650 mV have been analysed.

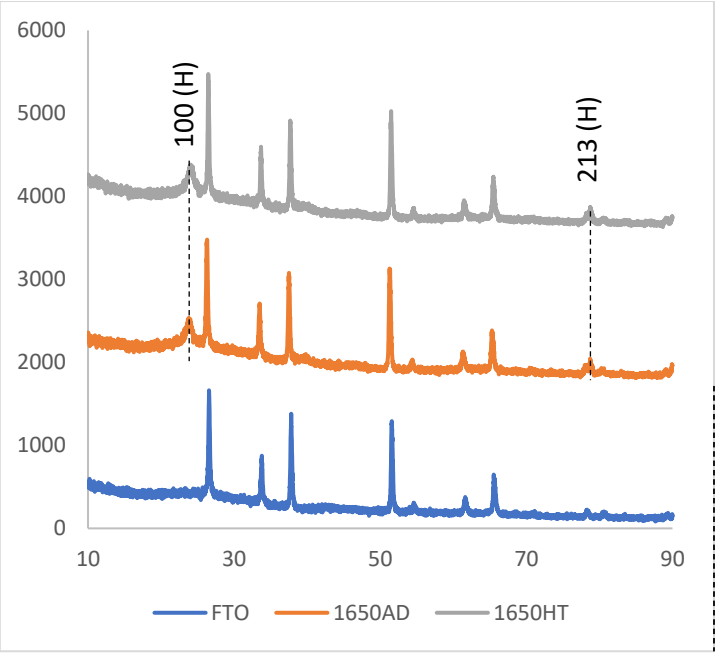

Fig 6.12 XRD patterns of as deposited (AD) and heat-treated (HT) n-ZnTe layers at 300°C for 10 minutes in air

Structural analysis of the n-ZnTe layers shows a hexagonal structure with (100) preferred orientation at $2\Theta \approx 24.00^{o}$ as depicted in figure 6.12. Both for AD and HT samples, depict (213) H orientation as well. As per Scherrer's equation, size of the crystallites for n-ZnTe layer has been estimated to be ~10 nm. Heat treatment of the layer causes a little change in the material lattice. This small change is visible in the optical absorption study in terms of a shift in the bandgap from ~1.90 eV to 2.11 eV upon heat treatment (figure 6.13).

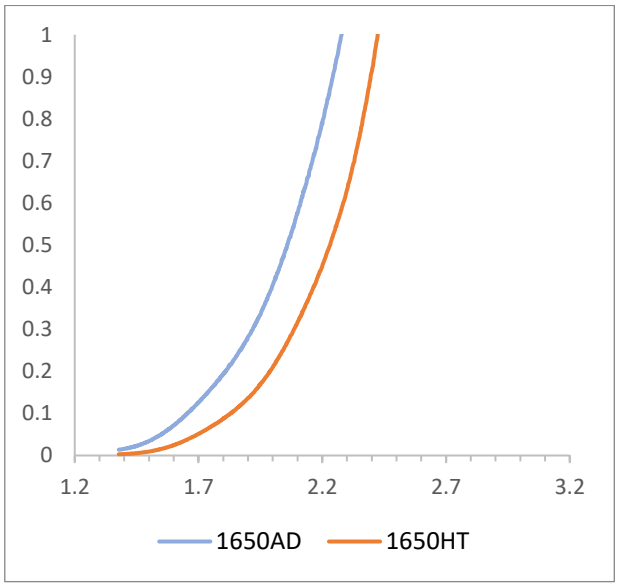

Fig 6.13 a^2 vs hv plot for As-deposited (AD) and Heat-treated n-ZnTe samples.

(a) AD at 1650 mV **(b) HT at 1650 mV**

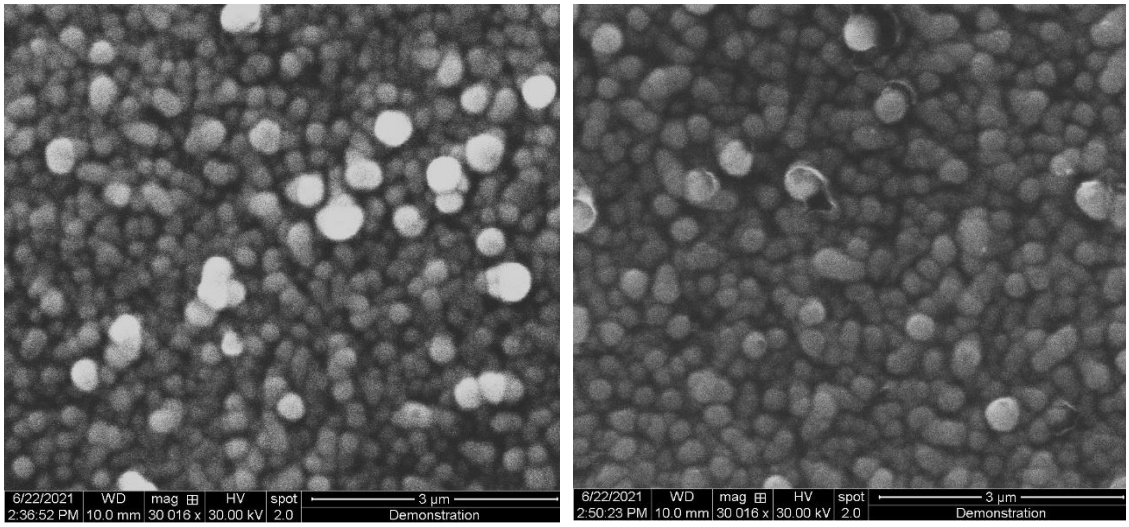

Fig 6.14 Typical SEM images of n-ZnTe thin films grown at 1650 mV **(a)** as-deposited and **(b)** heat-treated at 300^{o} C for 10 minutes in air

Moreover, morphological analysis with SEM micrographs depicted in figure 6.14 shows that n-ZnTe crystallites are not visible in the images. However, agglomeration of ZnTe crystallites is visible where the size of these nano-grains ranged between ~50 nm to ~230 nm. The AD n-ZnTe surface has an average grain size of ~82 nm whereas HT samples show an average grain size of ~86 nm. This slight change in morphology is consistent with the other changes of parameters too.

6.5 Material selection for the n-type hbdb layer

Unlike the ternary compounds, electrodeposited binary materials have shown a better outcome in terms of the required bandgap for the conceptualised device of this work. Both the materials those were grown as potential hbdb layer have shown a single bandgap greater than CdTe bandgap (>1.50 eV). Both materials are grown to be of hexagonal crystals after heat-treatment. Both CdS and ZnTe have shown n-type conduction regardless of post-treatment conditions. However, though CdS has shown an inherent n-type conduction at all growth voltages, ZnTe on the other hand has shown a transition of conduction type and layers grown at voltages greater than 1625 mV are n-type. Table 6.3 below summarises the best results of both the material growths.

Table 6.3 Major material parameters of the potential hbdb layers electrodeposited at different voltages. Optimised best layers for each candidate are highlighted in blue.

Material	**Growth Voltage (mV)**	**Conduction type**		**Bandgap, E_g**	**Crystallinity**
		AD	Treated	E_g	
CdS	1430	n	n	2.31	Hexagonal
	1440	n	n	2.32	
	1450	n	n	2.33	
ZnTe	1600	P	p	2.32	Hexagonal
	1625	i	i	2.67	
	1650	n	n	2.11	

The structural studies of the materials have revealed that CdS crystallites have a size of ~40 nm along the preferred orientation. But, n-ZnTe shows a comparatively smaller crystallite size of ~10 nm along the 100 (H) palne, though it is also possible that growth of the n-ZnTe crystals are taking place along the 213 (H) plane too. However, from the SEM morphological analysis it is visible that n-ZnTe has larger grain size compared to that of CdS, hence the periodicity of both the materials is very proximate to each other which is indicative of material properties such as electrical and device properties [17], [18].

As described in the first chapter of this thesis, this project has a definite eye for an appropriate technology implementation of PV manufacturing suitable for developing countries. Hence, while selecting any material for the proposed device structure, manufacturing convenience is a very important parameter to look for. Singh et al. back in 2012 had proposed five key criteria to consider for technology selection of photovoltaic manufacturing. Amongst these criteria, there are lowering of total cost of ownership and reduction of health and environmental safety issues [19].

Now, while comparing the two potential ebdb materials grown in this project it is obvious that, use of n-ZnTe shall surely reduce the use of toxic cadmium compared to its CdS counterpart. Therefore, ZnTe is clearly ahead of CdS for material selection on the ‘reduction of health and environmental safety issues’ ground.

Moreover, as per chapter 4 and several previous studies, ZnTe can be synthesised in both n-type and p-type conductivity from the same electrolytic bath while grown with electrodeposition, unlike CdS [20]–[22]. Now that the ebdb or window material has

already been selected as p-ZnTe layer in chapter 4, selection of n-ZnTe as hbdb layer shall certainly reduce the necessity of an extra electrolytic bath during the manufacturing process. Furthermore, due to the reduced variety of compounds in the solar cells, the procurement and supply chain shall be simpler [23]. Therefore, n-ZnTe material is able to reduce the total cost of ownership, hence has a precise upper hand over CdS to be used as the hbdb layer for the proposed device architecture in this project.

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Chapter 7

Solar cell fabrication, assessment, and critical analysis

7.1 Introduction

This chapter discusses about the fabrication process, characterisation, comparison, and critical analysis of the fabricated devices. This thesis started off with an aim to try out a novel device structure for electrodeposited solar cells based on n-type window graded band gap (GBG) architecture. It has been conceptualised that GBG devices fabricated based on wide band gap p-type window layers has a potential to show an enhanced open circuit voltage, hence better overall performance compared to their n-window counterpart [1]–[4]. Though, this architecture has been tried and tested for GaAs and Perovskite based PV cells, this was the first attempt taken to implement this device architecture with CdTe-absorber based solar cells. In order to carry out this plan, probable wide band gap p-type window materials as well as back diffusion barrier layers have been electrodeposited, characterised and optimised earlier [5]–[8]. Amongst these materials, ZnTe has shown excellent possibility to be used as both the p-type window layer and n-type back interface semiconductor. Hence for the concept device, a structure of glass/FTO/p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe/In has been decided to fabricate. Though, this device cannot be called a fully graded band gap device since the only gradation takes place is at the front semiconductor interface, this is the initial work towards developing fully GBG devices based on the concept.

To compare, evaluate and critically analyse the concept device against a conventional device based on n-window approach, another batch of solar cells have been fabricated with a structure of glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au. Apart from two of the above-mentioned batches of solar cells, several other batches of solar cells have been fabricated in order to get familiarised with the process and master the fabrication technique. As per the discussions of chapter 6, in the material selection phase for the n-type hbdb layer CdS has been synthesised and optimised. Therefore, for the practice devices, the main materials those have been used are CdS and CdTe. Moreover, CdS/CdTe based GBG devices are the most widely studied and understood structure in the Solar Energy Research Lab of Sheffield Hallam University [9], [10]. All electrodeposited solar devices based on CdS and CdTe only material exhibited a record highest efficiency of 15.3% which resulted from a glass/FTO/n-CdS/n-CdTe/p-CdTe/Au

structure [11]. Hence, for the practice devices, this tested architecture of devices have been used.

During the practice process, post-growth enhancement techniques such as $CdCl_2$ activation treatment, acidic and/or alkaline etching etc have been exercised, understood, and mastered.

7.2 Solar cell fabrication process

Standard fabrication process for electrodeposited solar cells has been performed taking the previous knowledge from the literature into account [9]. In the initiation of the fabrication process, glass/FTO substrate with a sheet resistance of 7 Ω/square has been cut into 1.5 cm × 3 cm dimension. The substrate cleaning has been carefully performed by applying soap solution using a clean cotton bud. The FTO side of the glass has been gently but thoroughly rubbed and rinsed with Type-I ultra-purified de-ionised water. This cleaning process has been repeated twice before blowing the cleaned samples dry with a forceful stream of nitrogen gas. In this section, the next main fabrication steps are described for ZnTe/CdTe based devices fabricated on both n- and p-type windows.

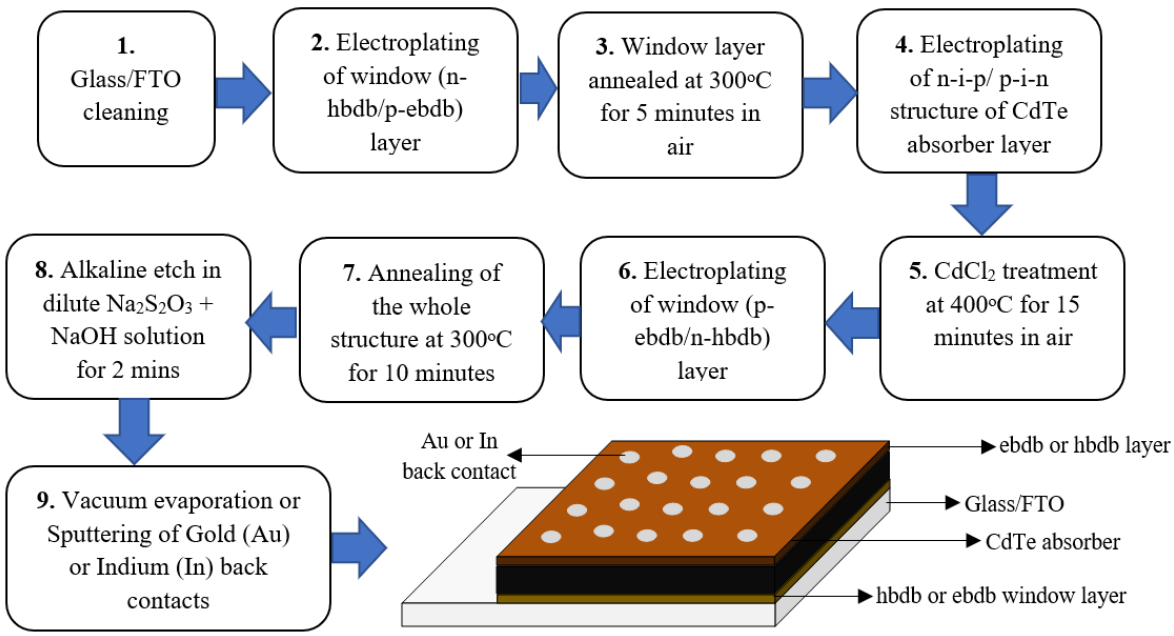

Fig 7.1 Processing steps of fabricating PV cells with the novel device structure decided for this work

After the cleaning process is over, as mentioned in the figure 7.1 above, standard electrodeposition of the chosen window layer is carried out. The electrodeposition procedure of any material layer has been clearly described with all necessary parameters

mentioned in the previous chapters. Duration of the deposition time is dependent on the desired thickness of the window layer and the deposition rate estimated using chronoamperometry in the previous chapters. Equation 7.1 is applied:

$$\text{Duration of deposition (in minutes)} = \frac{\text{Desired thickness of the layer (nm)}}{\text{Deposition rate (nms}^{-1}) \times 60} \quad (7.1)$$

After the window layer is deposited at the optimised voltage and necessary duration, the layer is taken out of the bath and rinsed with de-ionised water and dried with N_2 stream. The dried window layer sample is then put through a post growth heat-treatment. The heat-treatment parameters are investigated and decided for the necessary materials of this work. For example, CdS layers are normally annealed at 400 ^oC for 15-20 minutes, ZnTe window layers are annealed for ~10 minutes at 300 ^oC in air [9], [12]–[14]. However, since during device fabrication the corresponding layers of the devices go through different thermal treatment procedures, the heat-treatment duration is reduced often for the window layers. After the heat-treatment of the window layer, it is important that the layers are taken out of the oven and rested till cooled down completely to room temperature. This glass/FTO/window-layer is then rinsed with DI water before putting inside the electrodeposition bath prepared for absorber layer. Submerging the dry samples into the electrolyte is avoided because the dry samples may facilitate forming bubbles on the surface which may develop pin-holes on the layer.

In this work the absorber layer that is employed is CdTe and as per the required thickness of the CdTe layer having desired conduction type (p/i/n), equation 7.1 is applied to find the growth duration at a specific growth voltage (V_g). Semiconductor homojunction (p/i/n or, n/i/p or, n/p or, p/n) can easily be sequentially electrodeposited this way just by changing the growth voltage after a certain time interval. Once the expected homojunction/s of absorber layer is deposited on the window layer having an estimated desired thickness, the layer is once again taken out of the electrolyte, rinsed, and dried like before.

Then comes the most fundamentally useful post-growth treatment procedure for CdTe-based PV devices called $CdCl_2$ treatment. For $CdCl_2$- treatment, an aqueous solution is prepared by mixing 0.1 M $CdCl_2$ in 20 ml of type-1 ($\geq$18.2 MΩ.cm) DI water at room temperature. The pH level of this solution is maintained at 2.00 ± 0.02 using diluted HCl. These are optimised parameters experimentally found in the literature [9]. This solution is used for the post growth treatment of the grown glass/FTO/window-layer/CdTe-

absorber sample. Few drops of the prepared solution are applied on the material surface and then solution-damped cotton bud is used to spread the solution uniformly on the surface. The surface is then kept in room temperature to dry. Once the surface is completely dried the sample is then placed on a ceramic tray and put into the oven set at 400 ^{o}C. The heat-treatment is continued in air for 15-20 mins as observed advantageous for the device performance as per several previous works [15]–[18]. After the heat-treatment is done, the sample is then rested for cooling to room temperature and then residual chemical powder on the surface is rinsed clean with DI water.

For ZnTe/CdTe-based devices aimed in this work, the next step is to deposit a back diffusion barrier layer as discussed previously in chapter 1, 2, 4 and 6. Depending on whether the device is an n-window device or a p-window device, the p-type ebdb or n-type hbdb ZnTe layer is grown following the same procedure as before. After the deposition of this last layer, following the regular drying procedures, heat treatment of the whole sample is then performed at 300 ^{o}C for 10 minutes.

Before the metallisation of the cells an essential processing step for electrodeposited solar cell fabrication is called etching. Chemical etching is a process that helps the semiconductor-metal junction to avoid the phenomenon called Fermi Level pinning and form a good ohmic contact with the back electrode [19]–[21]. CdTe has been experimentally observed to have at least 5 typical defect levels present on its surface, depending on the compositional character of it [21]. These defect levels can play major role by pinning the Fermi level at the back metal contact with a poor Schottky diode with low barrier height, hence low open circuit voltage. Hence, to avoid leaving the back semiconductor surface with Cd-richness or Te-richness induced defect levels, layers were etched using a solution containing $K_2Cr_2O_7$ and concentrated H_2SO_4 for acid etching and a solution containing NaOH and $Na_2S_2O_3$ for alkaline etching for 2 s and 2 min, respectively, to improve the metal/semiconductor contact [9]. Studies also shown that, ZnTe too has such a tendency of exhibiting defect levels on its surface which are adjacent to that of CdTe [22]. However, for ZnTe back layer, since the last layer is very thin, acidic etching can damage the whole cell structure and/or create pin-holes detrimental for device performance. Therefore, alkaline etching is the main chemical etching employed in this fabrication process.

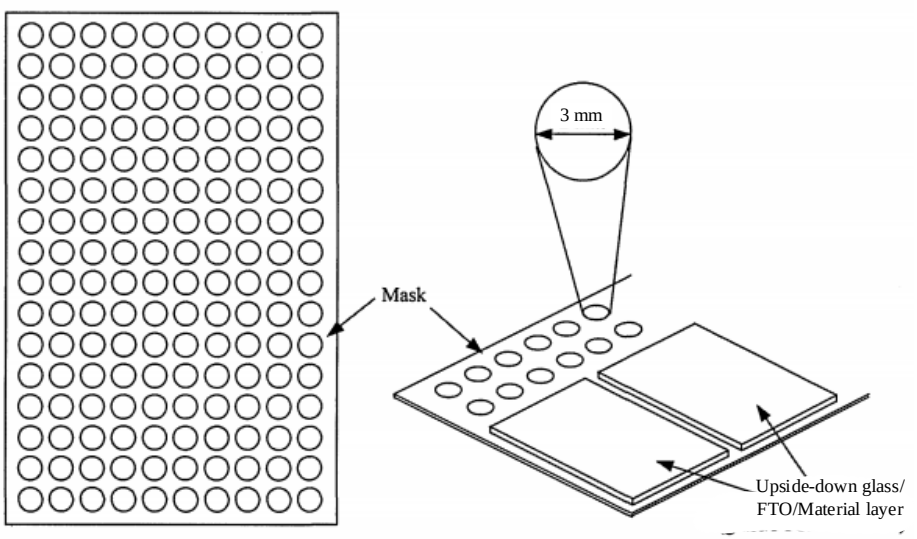

Fig 7.2 Use of mask for metallisation and arrangement of glass/FTO/material-layer samples on the mask

After the etching is over, it is essential to metallise the back surface within the earliest possible time to avoid any chance of oxidation of the surface. Depending on the conduction type of the back semiconductor layer, suitable metal (either Au or In) elements having suitable work-function is chosen. In order to minimise material waste and specification of cell area, a mask is used having regularly spaced circular openings to allow the sputtered or thermally evaporated metal particles deposit on the semiconductor surface. As per figure 7.2, the ZnTe/CdTe-based electrodeposited devices are finally prepared by metallising the semiconductor structure using a mask with 3 mm diameter openings. These circular regions represent a single solar cell having an area of 0.071 cm^2.

7.3 Glass/FTO/n-CdS/n-CdTe/p-CdTe/Au practice devices

For the familiarisation of the fabrication technique and to test the quality of the absorber materials, glass/FTO/n-CdS/n-CdTe/p-CdTe/Au structure of devices have been prepared following the procedures mentioned in section 7.2. Gold (Au) electrical contacts have been used since Au having a high work function of ≥5.1 eV tends to create ohmic contact which interfaced with p-type materials [10], [23]. Though, the interface properties are very much dependant on the nature of surface defects on the back semiconductor, choice of metal contacts is a good way of initiating the cell development.

As illustrated in the band structure of figure 7.3 The layer thickness for the CdS, n-CdTe and p-CdTe have been maintained at ~150 nm, ~1200 nm and ~35 nm respectively. These thicknesses are decided based on the works of Ojo et al, where good cell performance have been observed reaching up to an efficiency of 15.3% [11], [18]. CdS layer has been electrodeposited on cleaned glass/FTO substrate cut into a 1.5 cm × 3 cm dimension from the bath discussed in chapter 6. The applied growth voltage is 1450 mV since that exhibited the best material properties and the duration of the growth was for 15 minutes to obtain a ~150 nm film. The deposited CdS film is then heat-treated in air at 400 ^{o}C for 20 mins.

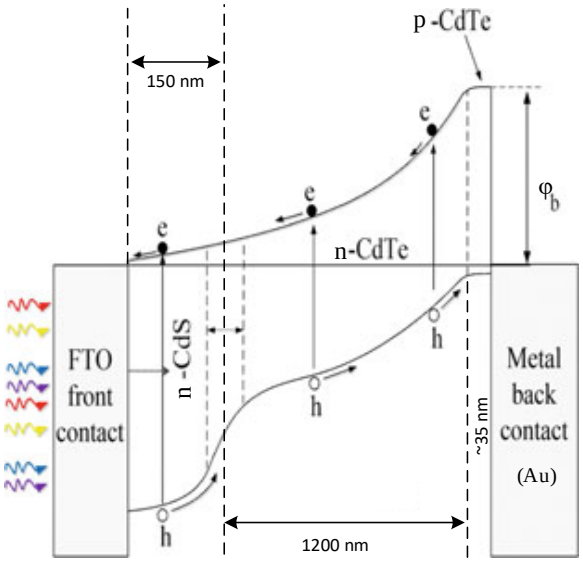

Fig 7.3 Band diagram of the typical Glass/FTO/n-CdS/n-CdTe/p-CdTe/Au practice devices (adopted and modified from [9])

The HT-CdS substrate is then submerged into the CdTe electrolytic bath having the same solution composition discussed in chapter 5 and a cathodic voltage of 1320 mV is applied for 3 hours to achieve a ~1200 nm n-CdTe film on the FTO/CdS structure. After 3 hours, the cathodic voltage is changed to 1310 mV and kept for ~8 mins to deposit a p-type CdTe film of ~30 nm thickness. The overall structure of glass/FTO/CdS/n-CdTe/p-CdTe is then taken out of the electrolyte and put through a $CdCl_2$ treatment for 15 mins at 400 ^{o}C. Here, point to be noted that, a slight possible shift of electrical conduction type towards p-region is often observed for electrodeposited CdTe layers upon $CdCl_2$ treatment, due to the compositional change in the CdTe grain boundaries [9], [18]. However, that transition is not seen to be affecting the device architecture.

After the $CdCl_2$ treatment, acidic and alkaline etching have been caried out on the semiconductor surface for 2 seconds and 2 minutes, respectively, to improve the metal/semiconductor contact. After performing the etching procedure, 3 mm diameter Au contacts of ~100 nm thickness are sputtered on the glass/FTO/CdS/n-CdTe/p-CdTe structure to finalise the device.

The devices are then characterised for their performance parameters under AM1.5 illumination using a commercially available fully automated I-V measurement system calibrated with a standard reference cell RR267MON. Amongst several practice batches of devices those were fabricated, Table 7.1 below presents the performance parameters of the champion cells from the batch that demonstrated the best outcomes for this structure. Figure 7.4 below is the illuminated I-V curve for the best efficient device in this batch with ~6% power conversion efficiency.

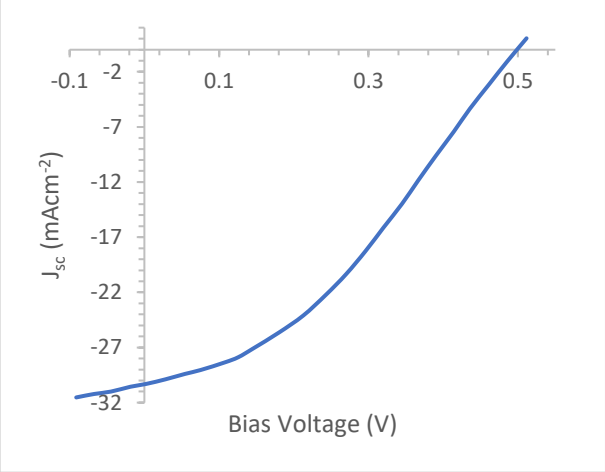

Fig 7.4 Current-voltage curve of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au champion cell under AM1.5 illumination

Table 7.1 Tabulated device parameters for the champion cells of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au architecture

Cell number	**V_{oc} (V)**	**Jsc (mAcm^{-2})**	**FF**	**η%**
1	0.542	29.7	0.31	4.97
2	0.521	28.1	0.36	5.26
3	0.502	30.1	0.36	5.41
4	0.523	30.3	0.38	5.98
Average	**0.522**	**29.5**	**0.35**	**5.41**

It is observed that the devices exhibit open circuit voltages (V_{oc}) in the range of ~500 mV to ~550 mV, short circuit current density (J_{sc}) in the range of ~28 $mAcm^{-2}$ to ~30 $mAcm^{-2}$, fill factor in the range of ~36% to ~38% and power conversion efficiency (η) in the range of ~5% to ~6%. These parameters are indeed considerably lower compared to the best performing devices with the same structure reported in the literature [11]. There may be many reasons involved those are affecting the parameters. For example, the last p-CdTe layer is included in this work to force the Fermi level pinning near the valence band in order to avoid the typical pinning positions experimentally found in n-CdTe and maintain a high barrier height thus V_{oc} [21]. But, it has been found that p-CdTe/Au interface may also exhibit Fermi level pinning if there is any native defect in the material or there are any disorder induced gap level present [24]. As discussed in chapter 5, the CdTe layers grown in this work were synthesised from 98% pure Cd-precursors. Despite, the lengthy electro-purification process, the bath may still have electronegative impurities those are not purifiable with this technique, which can indeed introduce native defects into the deposited CdTe layers and hamper the barrier height of the devices by pinning the Fermi level.

Moreover, for the same reason, there can be a higher carrier concentration caused which may reduce the effective depletion width of the device, hence the material layers staying out of the depletion region will contribute in series resistance of the device that can in turn decrease J_{sc} as well as FF [25]. Though, dark IV and Mott-Schottky analysis could not be performed for these devices to verify this explanation, these exercises have given an idea about typical device performance and a qualitative forecast of the achievable PV performance using this absorber layer.

7.4 ZnTe/CdTe-based devices with n-window approach

Since the main aim of this work is to attempt CdTe-based solar cell fabrication having p-type window layer, and the possible window layer has been selected as ZnTe because it is possible to electrodeposit with both p and n-type conductivity, glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au structure of devices have been fabricated first, for comparison between the n-window and p-window approach. The device architecture that has been illustrated in figure 7.5 below also mentions the applied growth voltages (V_g) along with growth duration to obtain the desired structure. 3 mm diameter Au contacts of ~100 nm thickness is prepared by sputtering. This multi-junction graded band-gap device

is by far the first attempt to fabricate a 5-layer electrodeposited device. Previously, electrodeposited solar cells were reported incorporating 3-layers at most [11].

The device is fabricated with a comparatively thicker n-CdTe layer with ~1 µm thickness, because the n-CdTe exhibits a better material quality as discussed in chapter 5, and Cd-rich CdTe has reported better device performances both theoretically and experimentally compared to that of its p-type counterpart [17], [26], [27].

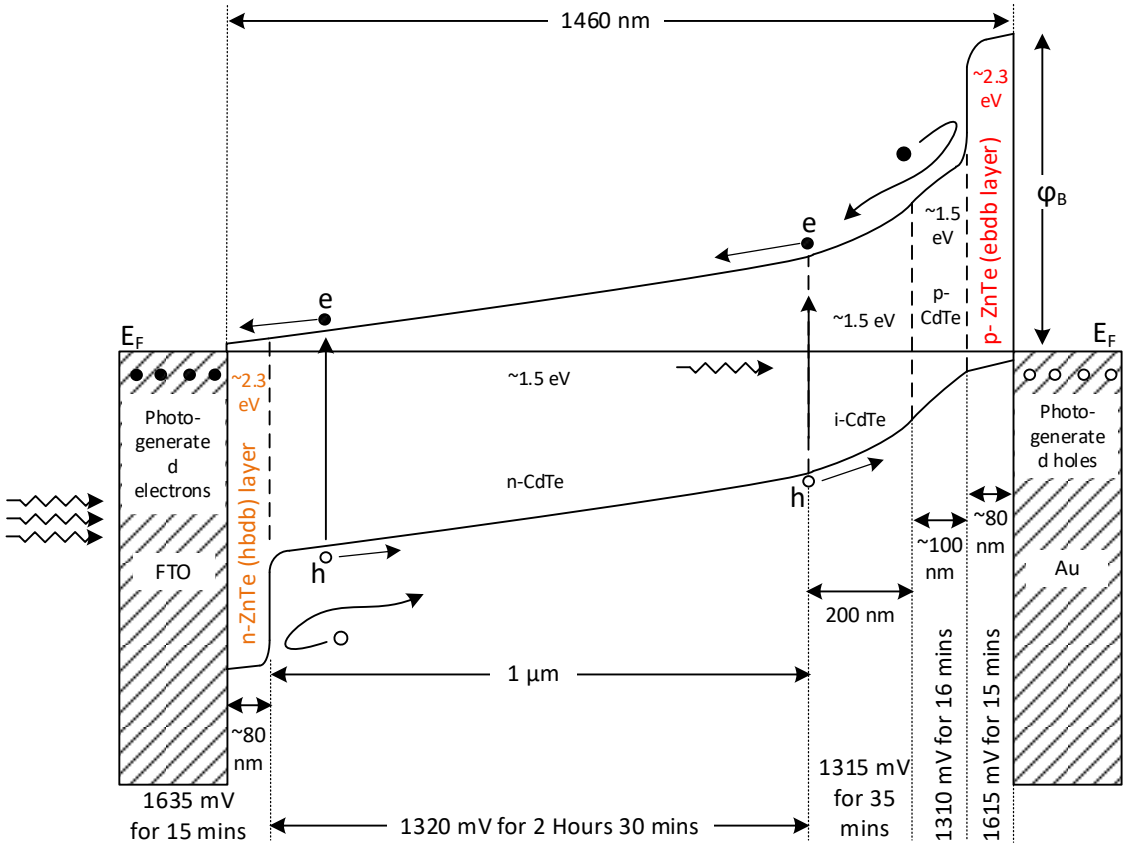

Fig 7.5 Band diagram along with applied growth parameters (growth voltage and time) for the n-window devices

The fabricated devices have been investigated using dark and illuminated I-V characterisation along with standard C-V under dark and Mott-Schottky analysis. Table 7.2 below presents the solar cell parameters obtained from I-V under AM1.5 illumination for the champion cells found from the fabricated batch. It is clear that the n-window device based on ZnTe/CdTe materials exhibit a lower performance compared to the CdS/CdTe system fabrication in section 7.3. All the cell parameters such as V_{oc}, J_{sc}, FF show a decreased values on an average.

The decline of the V_{oc} can be attributed to the native defects experimentally found in p-ZnTe/metal interfaces. It has been reported that p-ZnTe interfaced with high work function metals may pin the Fermi level at ~ 0.7 eV in reference to valence band maxima [22], which may take down the barrier height to the same level as CdTe bandgap. Then the quality of p-CdTe/p-ZnTe interface layer due to their interdiffusion may degrade and contribute to the lowering of the barrier height even further.

Table 7.2 Tabulated device parameters for the champion cells of glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au architecture

Cell number	V_{oc} (V)	J_{sc} (mAcm^{-2})	FF	η%
1	0.431	30.2	0.28	3.63
2	0.289	25.2	0.36	2.63
3	0.260	27.2	0.38	2.69
4	0.273	25.1	0.36	2.43
Average	**0.311**	**26.9**	**0.34**	**2.85**

This carrier concentration is high (~10^{16}) as found from the Mott-Schottky analysis of the champion glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au cell, presented in figure 7.7 (d). From the dark C-V plot presented in figure 7.7 (c) it is calculated that the depletion width of this cell is only ~476 nm which is less than one third of the total thickness of the cell. Hence, the rest of the un-depleted cell area works as dead mass and contributes to the high R_s.

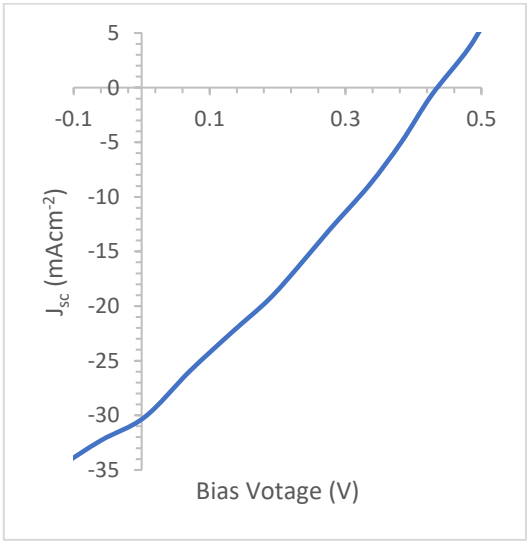

Fig 7.6 Current-voltage curve of glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au champion cell under AM1.5 illumination

Though, according to the illuminated I-V plot illustrated in figure 7.6 the champion cell exhibits a J_{sc} comparable to the CdS/CdTe-based devices above, the average J_{sc} is noticeably lower for the ZnTe/CdTe system than its CdS/CdTe counterpart. With a high carrier concentration of ~10^{16} and narrow depletion region, this low J_{sc} can be well explained. Moreover, along with the concerns regarding material quality this decline in J_{sc} may also be contributed by the i-type CdTe layer used in the middle to enhance the band bending of the cell, but in turn adding to the R_s due to its resistive nature as observed in chapter 5.

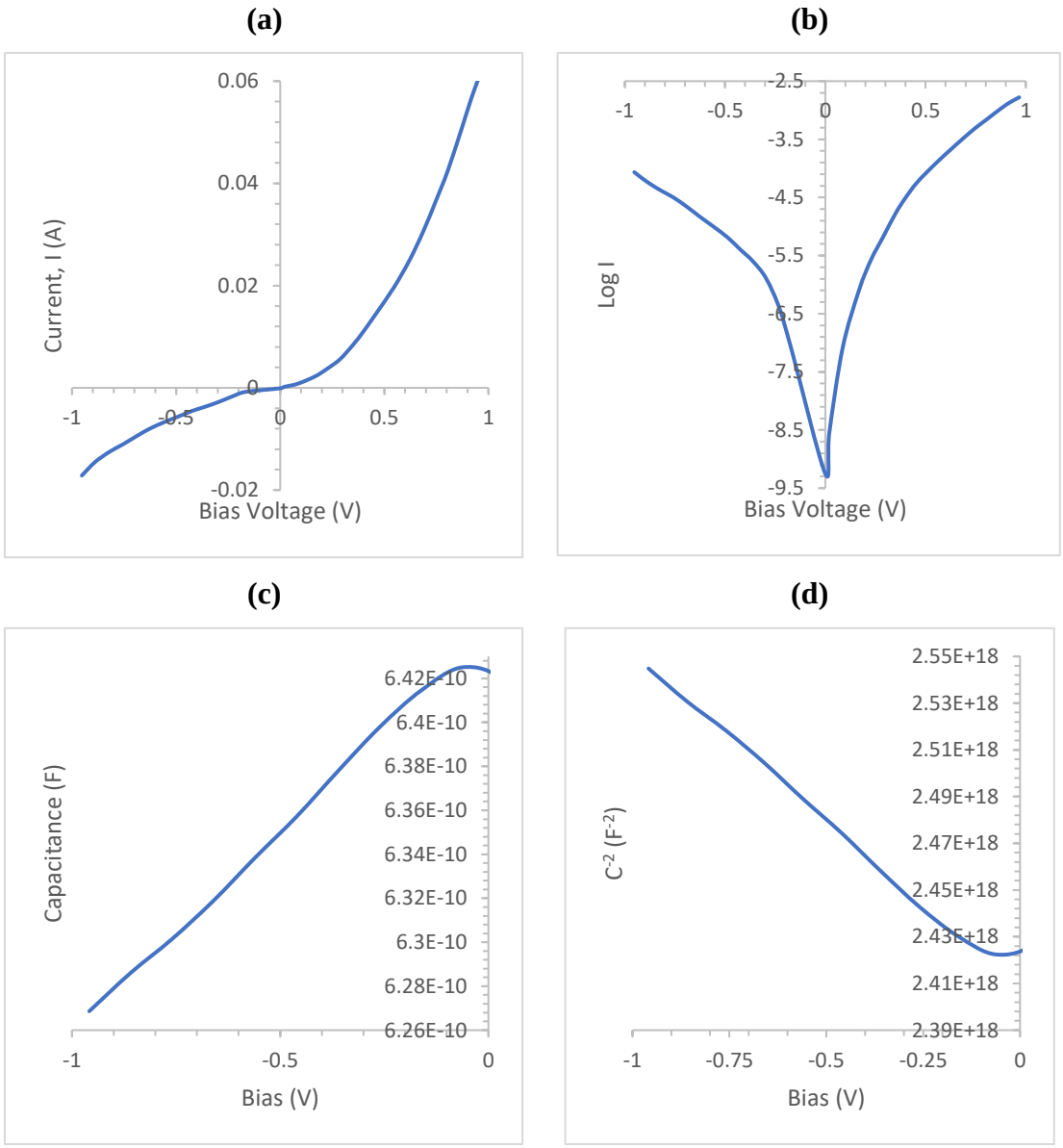

Fig 7.7 (a) Linear-linear and (b) log-linear Dark I-V curve along with (c) capacitance-voltage and (d) Mott-Schottky plotting for glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au champion cell

7.5 ZnTe/CdTe-based devices with p-window approach

The final batch of devices are the ones conceptualised at the beginning of this thesis. For the concept device, a structure of p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe has been electrodeposited on glass/FTO substrate following the processing steps mentioned in section 7.2. After the necessary etching steps, Indium (In) has been decided to be used as the back metal ohmic contact to the n-ZnTe, due to its low work function of ~4.09 eV [10], [28]. Deposition of 100 nm thick, 3 mm diameter circular In contacts were deposited using vacuum evaporation. Figure 7.8 specifies the band structure to scale, along with the growth parameters (V_g and duration) used for every layers sequentially.

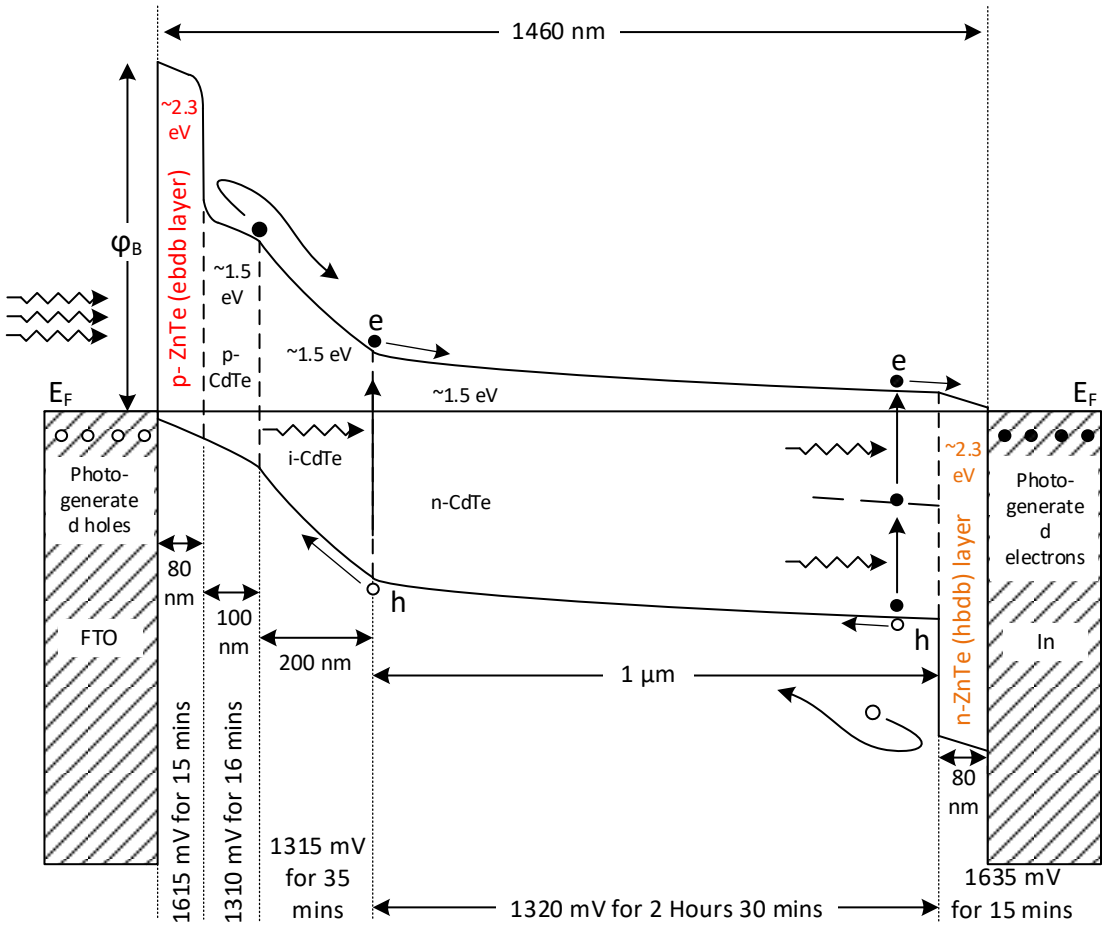

Fig 7.8 Band diagram along with applied growth parameters (growth voltage and time) for the p-window devices

Figure 7.9 illustrates the highest efficiency obtained from this batch as 5.41% along with a V_{oc} of ~562 mV, J_{sc} of 33.3 mAcm^{-2} and FF of 28%. Table 7.3 presents the illuminated I-V parameters of the other devices from this bath which show similar values of the parameters.

Table 7.3 Tabulated device parameters for the champion cells of glass/FTO/p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe/In architecture

Cell number	V_{oc} (V)	Jsc ($mAcm^{-2}$)	FF	η%
1	0.463	36.5	0.30	5.15
2	0.560	33.3	0.28	5.41
3	0.518	35.8	0.26	4.85
4	0.472	32.5	0.30	4.58
Average	**0.501**	**34.3**	**0.29**	**5.00**

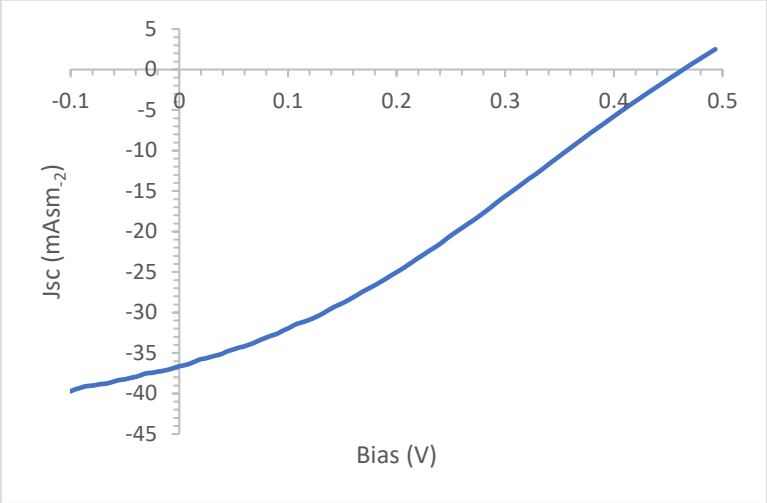

Fig 7.9 Current-voltage curve of glass/FTO/p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe//In champion cell under AM1.5 illumination

For the champion device from this batch dark I-V and C-V measurements have been performed and Mott-Schottky analysis has been executed. The plots are illustrated in fig 7.10. From the log linear representation of dark I-V measurements (fig 7.10 (b)) the ideality factor (n) of this device is calculated as 2.10, where ideally it should be $1 \leq n \leq 2$ for good cell performance [29]. This means that in this device, along with recombination-generation (R&G) and thermionic emission, the current transport mechanism may also be contributed by some tunnelling of high energy electrons through the barrier height [30]. However, because this device architecture keeps a very wide neck region, tunnelling of high energy electrons are unlikely. Hence, this high ideality factor ($n > 2.0$) may be caused by high series resistance (R_s) of the device. The reason why despite having a reasonable depletion width of ~836 nm, the device suffers from a comparatively low Fill Factor is probably that, high R_s is caused by the resistive i-type CdTe layer used in the middle.

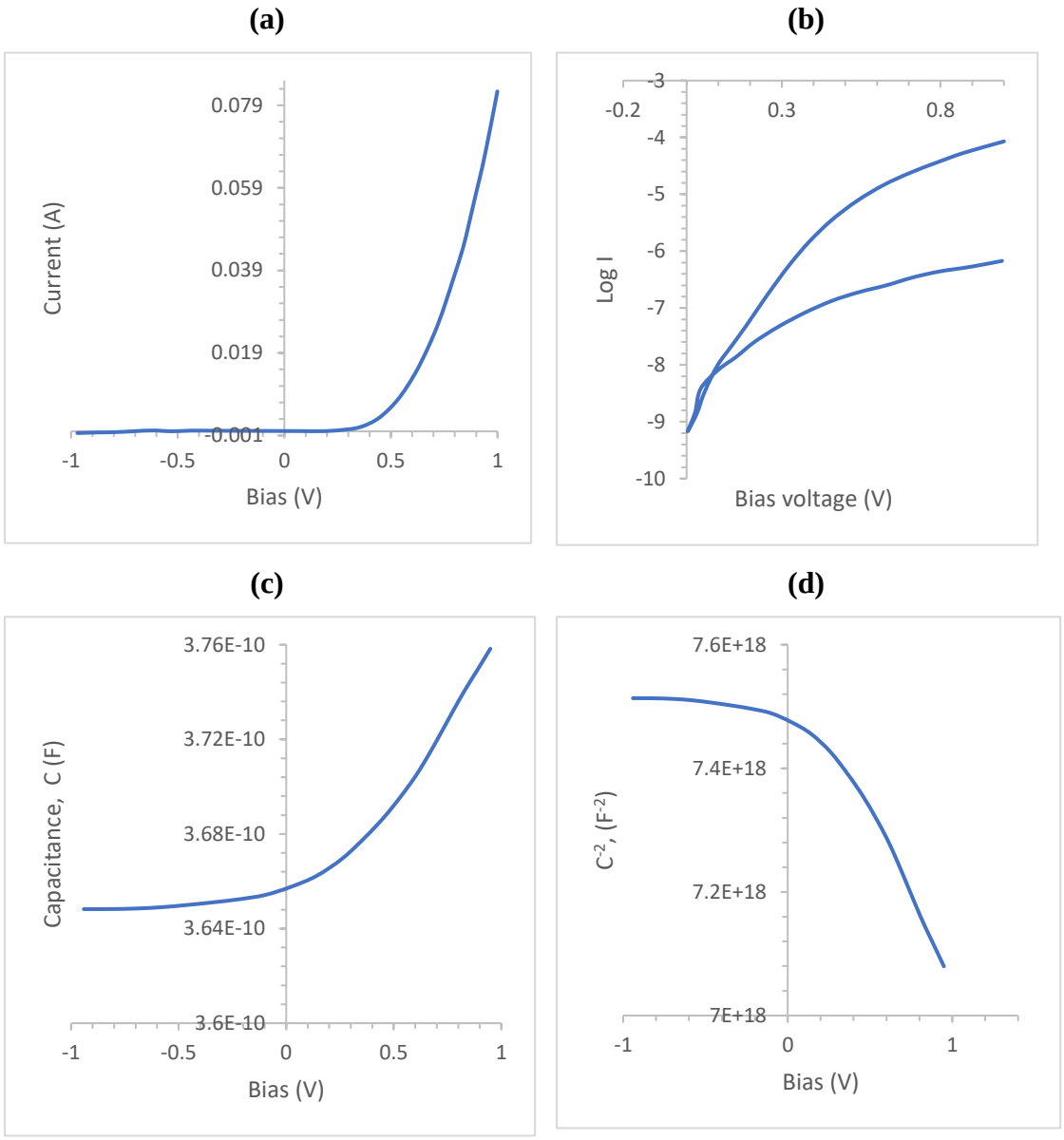

Fig 7.10 (a) Linear-linear and (b) log-linear dark I-V curve along with (c) capacitance-voltage and (d) Mott-Schottky plotting for glass/FTO/p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe/In champion cell

7.6 Comparison between n-window and p-window approach

In order to properly analyse, compare and understand the pros and cons of preparing p-window based devices, two devices using the same material layers but with altering conduction types are sequentially arranged for fabrication. The two device structures (n^+-n-i-n-p^+ and p^+-p-i-n-n^+) are almost mirror images to each other.

Table 7.4 below shows the comparison between the measured parameters of the two highest performing cells fabricated from p-window and n-window approach. It is noticed that for both the devices, the ideality (n) factor is >2.0, which is consistent with the high series resistance (R_s). Indeed, the quality of the materials used in the cells which can affect the R_s has played a role. However, the p-window device shows a comparatively better ideality factor compared to the n-window device. The rectification factor ($RF = I_F/I_R$) of the p-window device is higher than that of the n-window device which suggests a better diode quality; hence, the p-window device also demonstrates lower reverse saturation current (I_0) compared to the n-window device. Lower leakage current also attributes to the cells' capability of producing higher J_{sc} under illuminated condition. As discussed in chapter 2, p-window based devices indeed have a possibility of producing higher J_{sc} due to the possible higher contribution from impact ionisation and reduced back-diffusion [8].

The primary mechanism on which p-window approach is deemed advantageous is that it would positively impact the barrier height of the device, hence the open circuit voltage (V_{oc}). The calculated barrier height for the p-window device is indeed higher than that of the n-window device, and consequently the V_{oc} is also higher. However, the quality of the window material too has scopes of improvements and a comprehensive PL studies may be a way to definitively find possible defect states in p and n-ZnTe layers and ways to mitigate them. Point to be noted that for both the devices, the built-in voltage (V_{bi}) extracted from the Mott-Schottky (M-S) plot demonstrate unrealistically high values which are not reliable since M-S plots are primarily used for single junction Schottky devices and not for complex multi junction devices [31], [32].

Table 7.4 Summery of device parameters obtained from illuminated and dark I-V as well as C-V and Mott-Schottky analysis of devices fabricated based on p-type and n-type window

Characterisation type	**Parameter**	**p^+-p-i-n-n^+**	**n^+-n-i-p-p^+**
I-V under dark	R_{sh} (Ω)	7.9×10^5	1.39×10^5
	R_s (Ω)	4082	8070
	Log (RF)	2.1	1.2
	I_0 (A)	1.6×10^{-9}	5.0×10^{-8}
	Ideality Factor (n)	2.10	2.30
	Φ_b (eV)	>0.78	>0.73
I-V under AM1.5 illumination	J_{sc} ($mAcm^{-2}$)	33.25	30.15
	V_{oc} (V)	0.56	0.43
	Fill Factor	0.28	0.28

	Efficiency, η (%)	5.41	3.63
C-V under dark	C_0 (pF)	366	642
	W (nm)	836	476
	Carrier Concentration	1.73×10^{16}	6.02×10^{16}
	V_{bi} (V)	~13	~17

It is indeed sensible to say that none of the devices fabricated here are of the optimum device quality, hence any conclusive comparative analysis is not possible. However, because the growth conditions, electrolytic bath parameters, post-growth treatment conditions and etching conditions are all kept identical for both batches of devices, the material layers of both the device architectures (n-window and p-window approach) are likely to have identical characteristics. Since the only difference between the two devices that is deliberately maintained is the orientation of cell architecture, therefore the changes in performance and device parameters are likely to be instigated by the architecture. However, any decisive comparison between the two architectures is ideally to be carried out between high performing devices and none of these devices are particularly high performing considering their low efficiency. Therefore, though electrodeposited multi-layer graded bandgap solar cells based on p-type wide bandgap window layer has shown a better cell performance compared to that of the n-window-based devices in this particular study, a conclusive proof of concept can only be drawn after reputative comparison between batches consisting of higher layer qualities and cell performances.

7.7 Conclusion

In this chapter, the detailed procedure of device fabrication has been discussed. Before the fabrication and testing of the desired novel device based on p-type window, several practice devices have been fabricated. The practice devices are of conventional CdS/CdTe architecture based on n-type window. Parameters of the practice devices have been recorded and indicative of the possible concern regarding material quality. Following the practice exercise, two batches of ZnTe/CdTe based devices have been fabricated with mutually inverted cell architectures, one with n-window approach, other with p-window approach. Though, p-window based devices have shown better cell performance with noticeably higher V_{oc} and J_{sc} as expected, the material quality concerns along with poor cell performance remained the major drawback to conclusively consider this study a ‘proof of concept’. For both of the devices, incorporated i-type CdTe layer in the middle of the cells seemed to add deteriorating effects on the cell performance.

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Chapter 8

Conclusion: summary, challenges, and future works

8.1 Summary

This thesis incorporated the societal, commercial, environmental, scientific, and theoretical backgrounds of the work those have been at the core of this research. The work commenced with the personal motivation of the author and concluded with the implementation of the concept device that it aimed for. The main aim of the work has involved conceptualisation, designing, material selection, material optimisation and fabrication of CdTe-based thin-film solar cells with a novel device structure that has the potential to generate better performance and can be fabricated using a commercially implementable technique affordable to the developing world. Hence, electrodeposition technique has been used. Key activities and novel achievements resulted from this work are pointed below:

- In the conceptualisation phase,
  - Trends and practices in the field of CdTe based thin-film solar cells have been thoroughly studied and scientific hurdles and confusions in this field have been observed to find the areas of improvement. A novel device architecture based on p-type wide band gap window layer and suitable carrier back-diffusion barrier layers (ebdb and hbdb) has then been discussed and decided based on this literature review. This thorough review work is now published as an article [1].
- To implement the concept, in the material selection phase,
  - Mg incorporated CdTe (CdTe:Mg) ternary compound has been electrodeposited as a probable p-type wide bandgap window layer for the first time ever. It was found that although the material produces a wide bandgap required, the layer loses crystallinity as Mg is incorporated and possible intra-bandgap absorption levels arise in the material. This work is now published as a scholarly article [2].
  - Another ternary compound, CdMnTe has been electrodeposited and optimised as a probable p-type window, however, despite having p-type wide bandgap characteristics with reasonable crystallinity, this electrodeposited ternary compound also showed a tendency to reveal possible intra-bandgap absorption

point which can be deteriorating for the concept device. This work has also been published now [3].

- After identifying a common issue in the ternary electrodeposited compounds, a binary compound namely ZnTe has been electrodeposited and optimised. This compound was synthesised in both n and p-type having wide bandgap, reasonable crystallinity and no absorption point optically present within the bandgap. Hence, this material has been finally selected as the front p-window layer as well as the n-type hole back-diffusion barrier (hbdb) layer.
- Consequently, CdS layers were also electrodeposited using a low acidic precursor (Cadmium Acetate) to be used as an alternative hbdb layer. Electrodeposition of CdS has been carried out with this precursor for the first time and the findings are now published [4].
- CdTe layers with n and p-type have been electrodeposited from the same electrolytic bath, characterised and optimised using low purity precursors to be used as the main absorber layer for the device concept. Use of low purity precursor comes with an opportunity to reduce the cost of manufacturing for the solar cells.

- After the material selection is carried out, in the device fabrication phase:
  - Several batches of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au structure have been fabricated as part of the familiarisation process to the technique. Up to ~6% efficient devices were made from the batches. Quality of the absorber material is thought to be the probable cause for the low efficiency compared with previously obesrved values (15.3%).
  - According to the concept device, a batch of glass/FTO/p-ZnTe/p-CdTe/i-CdTe/n-CdTe/n-ZnTe/In solar devices have been prepared following all the necessary fabrication procedures. The highest efficiency obtained from this batch is 5.41% along with a V_{oc} of ~562 mV, J_{sc} of 33.3 $mAcm^{-2}$ and FF of 28%. Apparent inferior quality of the absorber materials as well as the incorporation of an i-type layer contributing series resistance to the devices, results in low performance of these devices.
  - To test the concept and verify the advantages of p-window approach, a batch of solar cells with inverted structure Glass/FTO/n-ZnTe/n-CdTe/i-CdTe/p-CdTe/p-ZnTe/Au have been fabricated for comparison. Based on the device

parameters obtained from several cell characterisation techniques, it has been observed that, devices having p-type window show better cell parameters.

8.2 Limitations and challenges faced

There has been unavoidable situation like the hit of the global Covid-19 pandemic, which did not only stagnate the lab work for nearly 10 months, but also took a toll on the physical, psychological, and financial situation of the global research community. This research project was no exception to that. The researcher is however grateful for the institutional support and the realistic extension of funding that enabled this work to at least reach to a reasonable point of outcome. These pandemic-induced rearrangements have hampered the research in following ways:

- This work is based on only two batches of devices with desired architecture. Device development works are generally done using numerous batches and normally it takes several combinations of device structures and fabrication attempts to reach to a point of perfection. Therefore, the reproducibility of the cell performance could not confidently tested either.
- The necessary alterations based on the measured device parameters could not be made due to the lack of time. For example, the inclusion of i-type CdTe layer in the device design was later deemed disadvantageous, but a new structure of device could not be tested and verified due to the time constrains.
- Electrodeposition baths are normally very sensitive to the maintained parameters such as, composition, temperature, pH, stirring and even duration of stirring and heat. This happens because of possible precipitation of incorporated chemical elements, irregular movement of ions etc. Because of the laboratories staying closed nearly for 10 months, the previous electrolytic baths were not ready to be used and new baths needed to be prepared which may have introduced irregularities.

Apart from the pandemic related anomalies, this work has come by some major limitations and challenges both in the technical and procurement front as well. Such as-

- Unavailability of high purity Cd precursor from the suppliers has forced the work to start with a lower purity chemical for CdTe growth. During the commencement of the lab works of this project, none of the chemical suppliers

could provide 5N quality Cadmium Nitrate precursor. Therefore 98% pure precursors were used after long sessions of electro purification, but that could not avoid the possibility of electronegative impurities in the bath, hence has visibly hampered the cell quality.

- Wide range photoluminescence study is a very useful tool for this research to find possible defect states in new materials. The wide range photoluminescence studies for this work were carried out in the laboratory of the collaborators based in the USA. Therefore, this characterisation technique was not always locally available, hence the ZnTe layers used for the ebdb and hbdb layers were not investigated for their intra-bandgap defect levels and possibility of Fermi level pinning positions is unknown.
- Gradual and controlled addition of Tellurium precursor into the CdTe electrolytic bath has been a recurring technical issue in the electrodeposition technique. The industrial arrangement used by BP consisted of a pumping mechanism to maintain a very low level of Te in the CdTe bath all the time. However, in the SHU laboratories, there has been no such technical facility available and inclusion of Te has been controlled by adding few drops of the precursor by handheld dropper after every few depositions. Hence the accuracy of the Cd:Te composition in the electrolyte is always a point of concern.

8.3 Future works

8.3.1 Probable technical improvements

- Fabrication of the concept device should be carried out using high purity (4N-5N) chemical precursors for the material deposition.
- Further electrical characterisation with DC-conductivity measurement, dark I-V and Mott-Schottky analysis of the individual material layers are advantageous to carry out before incorporating them into the device.
- Incorporation of the apparently resistive i-type layers should be minimised or avoided to investigate the device parameter. This shall also reduce the fabrication time of the device which is better for commercial implementation. The probable device structure is shown in figure 8.1 below.

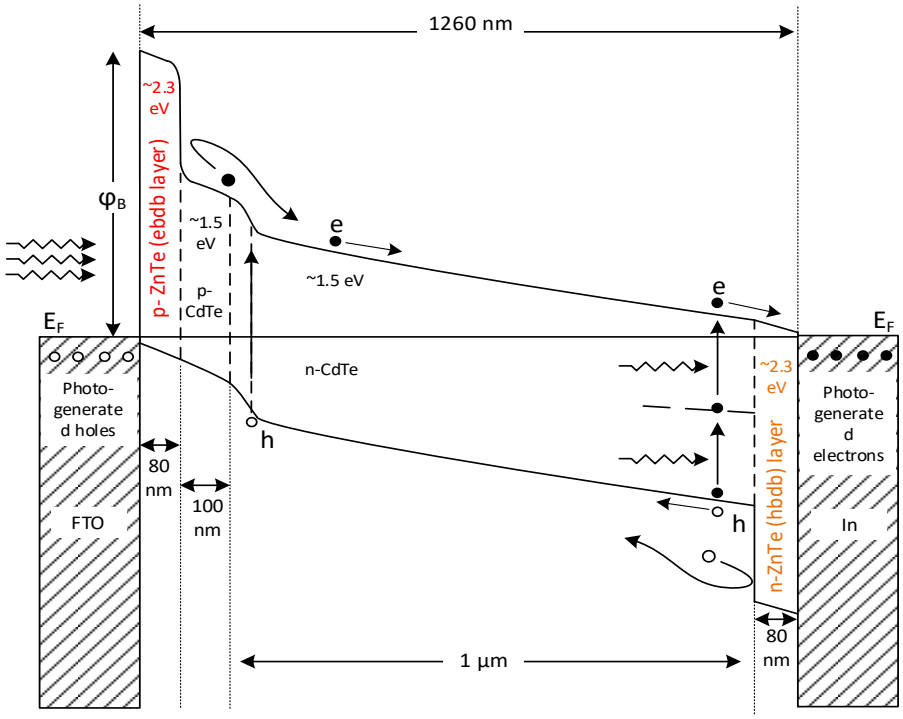

Fig 8.1 New device arrangement to be investigated for p-window based CdTe solar cellls

- Another possible advancement can be attempted using the same device structure only by altering the back contact with any kind of transparent conductive oxide layer, as presented in the figure 8.2 below. This way the device can be applicable for bifacial solar cell applications, since holds a possibility of providing even better cell performance.

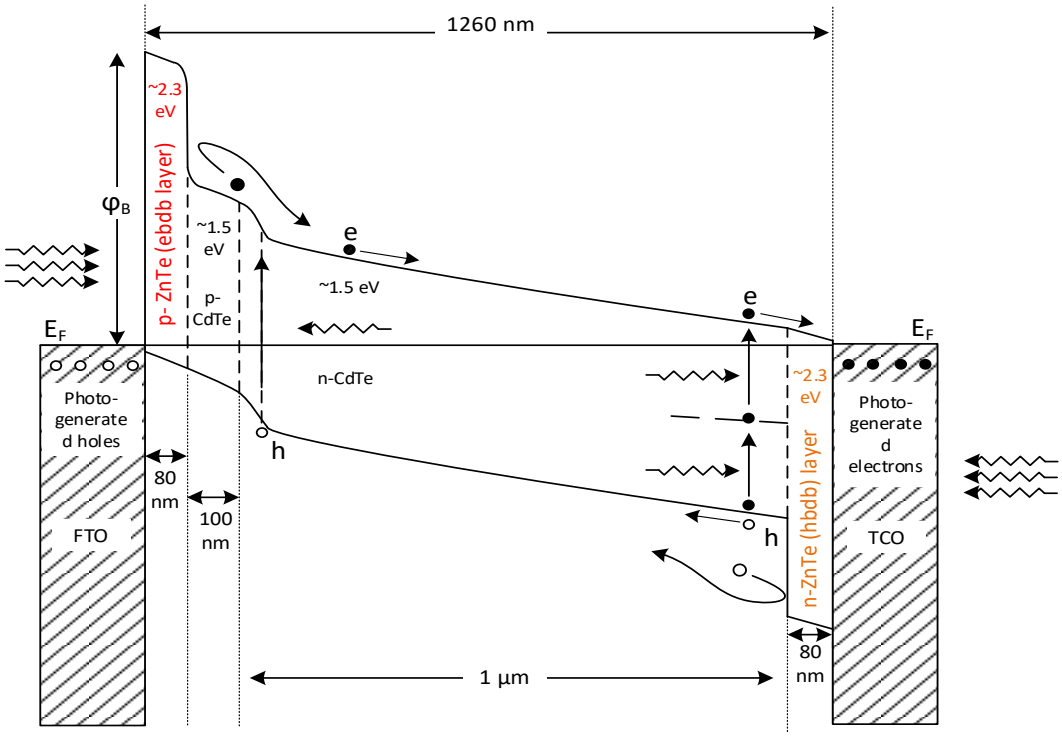

Fig 8.2 New device concept to be investigated for bi-facial CdTe solar cellls

- Here, in the first stages of graded bandgap solar cells, just one absorber layer with a constant bandgap of 1.5 eV has been used. However, CdTe absorber material can be graded by adding an additional element. For example, addition of Mercury (Hg) gradually reduces the bandgap to any desired smaller value. This way the devices can be graded further.

8.3.2 Probable societal applications

The author's group has nurtured a collective value that, scientists are not only responsible for what happens in the lab, but they also have a responsibility towards the greater society. And indeed, the use or underuse of renewable energy is not just only a technical matter, but also a socio-political matter as well. It is immensely necessary that societal approach towards the use of renewable energy needs to change for the research and policy environment to change as well. These changes are mutually inclusive. This holds true specially in the developing and less-developed parts of the world, and the developed portions cannot contemplate themselves as a remote island either. Driven by this philosophy, the possible societal applications and efforts those can be taken are:

- The 'Solar village' project that is implemented and successfully sustained and replicated within Sri-Lanka by the supervisor of this research work, can be modified according to the necessity of different other countries' local energy needs, specially for author's native country Bangladesh and implemented [5].
- A sustainable financial model in form of a 'Social Enterprise' has been discussed and formed in course of the research when the lab works were stagnated due to the pandemic. This plan has incorporated at least 4 different South-Asian and Sub-Saharan counties who are eligible for ODA funds. Hence, in the future, probable GCRF, DFID or ODA funds can be attempted to access in order to support the seed for this venture.
- The author has also submitted a funding proposal as a co-investigator in his native country to finance building an electrodeposition lab for energy material research. Given the funding is approved, there are possibilities of sharing the skills to a wider research community across the globe.

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