Series SiC MOSFET-Based Low Gain Buck Converter for Enabling Access to MVDC Network

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Abstract

Low-gain buck converters will enable low voltage loads to access high voltage DC sources by a single stage converter at very low duty cycles. SiC MOSFETs are still limited to 1.7kV commercially and by seriesing them with adequate gate driving strategy, high voltages can be switched. This paper proposes a driving circuit for series SiC MOSFETs to block higher voltages. The driving circuit provides negative off-state voltage and turn on/off transitions in less than 100ns. The low-gain buck converter performance is assessed when using a single IGBT switch and series SiC MOSFETs. A simulation is implemented and shows the superiority of the proposed driven series SiC MOSFETs with distributed voltage and thermal stresses.

1. Introduction

Wide-bandgap semiconductors devices enabled more improvements in the power electronics fields applications [1]. However, Silicon Carbide (SiC) MOSFETs provides high switching speed due to low gate capacitance, high breakdown voltage and low thermal resistance, which makes it strong candidate for medium and high voltage applications. However, Commercially available SiC MOSFETs are limited to 1700 V breakdown voltage devices. Higher voltage MOSFETs are still in the development or costly [2].

According to the work in [3], series-connected SiC MOSFETs features lower ON-resistance, higher current density, and stronger terrestrial cosmic radiation immunity than using a single high-voltage device. Therefore, the series connection of multiple SiC MOSFETs is reasonable to be investigated.

Medium Voltage DC Network (MVDC) have a huge potential in the coming future to be adopted and implemented in DC grids, for example, to couple power from offshore wind turbines to the national grid via power electronics inverters. The access of these voltages by low voltage loads still not enabled.

Fully separated drivers for SiC device equipped with isolated power supply is presented in [4] to drive series connected devices. This provides driving flexibility but challenge the power design and compactness of the design. A floating self-driving circuit is developed in [5] and [6] unitizing the DC capacitors to support switching the high side of two series switches.

Another way of driving series MOSFETs is by using the capacitive coupling [7], where the charge of a capacitor is used as a buffer to generate a driving signal to the next MOSFETs. This design facilitates using a single driving circuit.

For higher gate immunity, it is recommended to switch off the SiC MOSFET by a negative voltage., i.e. -5V. This provides more margin against false turn-on when the temperature of the MOSFET increases, and the gate voltage threshold decreases [8].

This paper will introduce how the series SiC MOSFET enables the access of very high voltages to obtain low voltages. The proof of concept will be implemented using a buck converter where the switch is exposed to high voltage stress. The paper shows a design of a series SiC MOSFET driving circuit. A three series SiC MOSFETs and a single IGBT switch are used in the buck converter design and compared by investigating the stresses on the series MOSFETs and IGBT and the distributed losses while stepping down 3kV to 48V.

2. The proposed Series SiC Driver

Fig. 1 shows the structure of the driving circuit for series MOSFETs. The circuit here servers for three MOSFETs with a single gate driver. The load is assumed to be inductive as the double pulse testing will be implemented for switching assessment.
Fig. 2 shows the turn on and turn off transition stages as well as the steady off-state of the proposed circuit.

2.1 Turn-on operation

Before turning on the MOSFETs, it is assumed that all MOSFETs were in a complete off-state. Therefore, all capacitors have initial charges. Fig. 2a illustrates how the turn on starts by providing the first MOSFET M1 with a driving signal V_G. This will charge the gate capacitance leading the

MOSFET M1 to decrease the voltage drop between its drain and source as shown as Loop1. At the same time the driving signal from V_G will be coupled through the capacitor C_{M1} to the gate of the second MOSFET M2 as denoted by Loop2. The drain D1 voltage is dropping while the signal delivered to the gate of M2 becoming sufficient to turn on M2. When MOSFET M2 becomes on, Loop3 shows the charge of C_{M2} is delivered to the gate of MOSFET M3 through the on-state resistance of M2. At ON steady state, all MOSFETs ae represented by their on-state resistances and the current flows from D3 to S1.

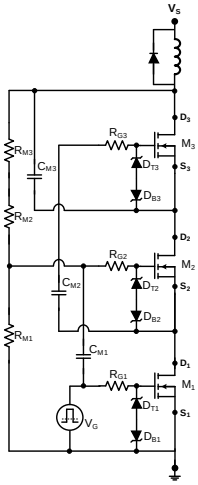

Fig. 1. Driving Series SiC MOSFETs

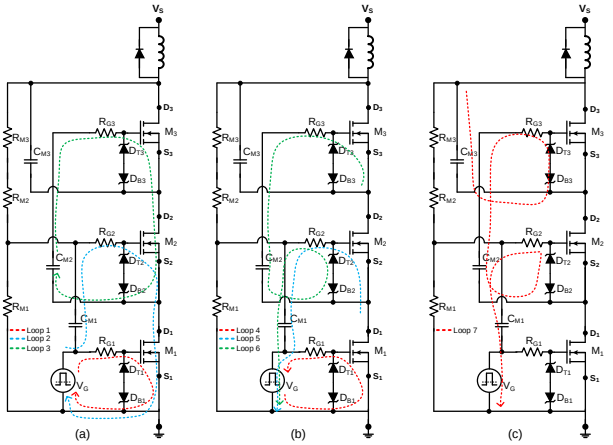

Fig. 2. (a) Turn-on Switching transition, (b) Turn-off Switching transition, (c) Steady off-state

2.2 Turn-off operation

Fig. 2b depicts the discharging paths of all gate capacitances. The operation is initiated by an off-voltage signal provided by the gate driver V_G. As shown by Loop4, the gate of MOSFET M1 will discharge and turning it off. The source node voltage at S2 of MOSFET M2 will rise leading to pushing the charge of the gate capacitance of M2 back to V_G through the capacitive coupling C_{M1} as shown by Loop5. Similar behaviour to turn off M3 through the cooling capacitors C_{M1} and C_{M2}.

The steady off-state is shown in Fig. 2c. The voltage across M1 is dominated by the ratio between R_{M1}: $(R_{M2} + R_{M3})$. Loop7 shows that the turn-off voltage for MOSFETs M2 and M3 are set by the voltage drop created by the Zener diodes D_T and D_B. The leakage currents of C_{M1}, C_{M2} and C_{M3} are used to bias these Zener diodes and maintain a negative voltage between the gate and source while in off-state.

$$I_{leakage} > I_{z(min)}$$
$$= \frac{V_s - (n-1) \times (V_{D_T} + V_{D_B}) - V_{drive-off}}{(n-1) \times R_G} \quad (1)$$

where n is the number of MOSFETs and here is 3, $V_{drive-off}$ is the off-state voltage of the gate driver, V_{D_T}, V_{D_B} are the voltage drop across the Zener diodes in operation and R_G is the gate resistance.

The steady state for all MOSFETs are as follows, assuming that the voltage across the resistor R_G is neglected,

$$V_{off-M1} = V_s \times \frac{R_{M1}}{R_{M1} + R_{M2} + R_{M3}} - (V_{D_T} + V_{D_B}) \quad (2)$$

The voltage across C_{M2} and C_{M3} are determined by

$$V_{(R_{M2}+R_{M3})} = V_s \times \frac{R_{M2} + R_{M3}}{R_{M1} + R_{M2} + R_{M3}} = V_{C_{M3}} + (V_{D_{T3}} + V_{D_{B3}}) + V_{C_{M2}} + (V_{D_{T3}} + V_{D_{B3}}) \quad (3)$$

Here it is assumed that $V_{C_{M2}} = V_{C_{M3}}$ due to similarity, Therefore,

$$V_{off-M2} = V_{C_{M2}} + (V_{D_T} + V_{D_B}) \quad (4)$$

$$V_{off-M3} = V_{C_{M3}} \quad (5)$$

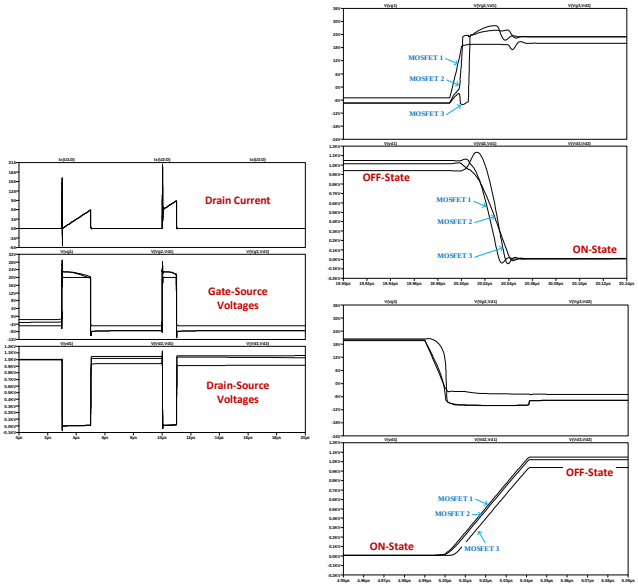

Fig. 3. Double pulse testing and its zoomed view for the turn-on and turn-off transitions.

Table 1 Parameter for the DPT simulation

Component	Value	Component	Value
V_s	3000V	D_B	6.8V
L	1000µH	D_T	22V
R_M	100k Ω	R_G	6Ω
C_M	200pF	$V_{drive-on}$	20V
MOSFETs	C2M1000170D	$V_{drive-off}$	-5V

3. Double Pulse Testing Simulation

LTspice was used to simulate switching three MOSFETs in series as in Fig. 1 with a clamped inductor load. The modelled SiC MOSFET is C2M1000170D. Wolfspeed provides the spice model. the simulation values are shown in Table 1.
The DPT waveforms are shown in Fig. 3 including the gate-source voltages and the drain-source voltages. The results depict a semi-balanced voltage sharing at off- steady state due to the existence of Zener voltages. In addition, it shows consistent dynamics of voltage and currents among all MOSFETs.

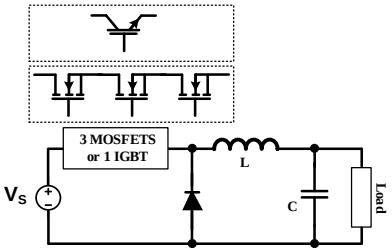

Fig. 4. Low gain buck converter

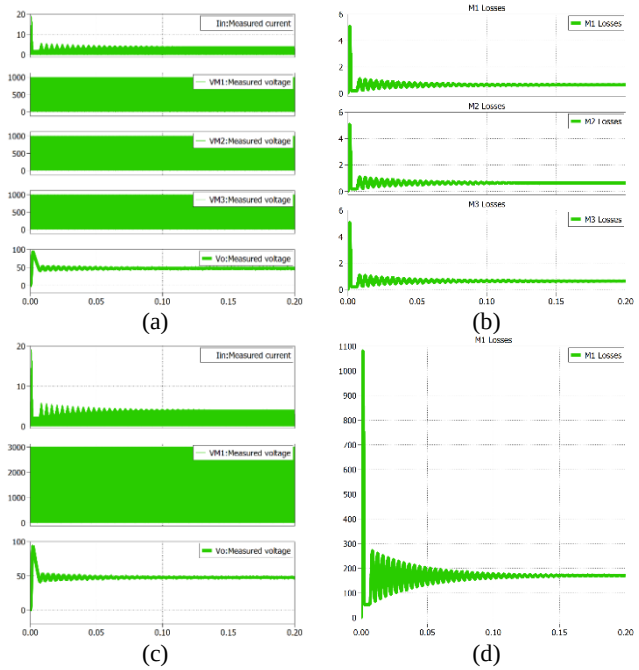

Fig. 5. (a) Output voltage and current and voltage stresses on the three MOSFETs (b) Total losses of each MOSFET (c) Output voltage and current and voltage stresses on the IGBT (b) Total losses of the IGBT

4. Simulation of Low Gain Buck Converter

The design of buck converter components is well-established in the literature and here the focus is on the performance of the power switch in the buck converter which is supplied by a high voltage as 3000V as shown in Fig. 4. The desired output voltage is 48V and load current is 3A. Therefore, the calculated steady state duty cycle is 1.6%. PLECS has been used to conduct the simulation where each power switch is equipped with similar heatsink. The inductor is 2mH and capacitor is 200μF. The diode is capable to handle the voltage stress. The PLECS models of the used power switches are provided by the manufacturers. The simulated results are shown in Fig. 5 for the output voltage, current/voltage stresses in the power switches and total losses including the switching and conduction loss. The switching frequency is selected as 10kHz. A three series SiC MOSFETS with braking voltage of 1.2kV, C2M1000170D, are used where their voltage stresses are shown in Fig. 5a, as 1kV per MOSFET, and losses in Fig. 5b as 0.64W per MOSFET. The output voltage is stable at 48V. Similarly, the three MOSFETS are replaced with a 3.3kV IGBT, FZ1200R33HE3, and the simulation results are shown in Fig. 5c where the voltage stress is 3kV and losses are calculated as 168.5W in Fig. 5d. It is surprisingly shown that the series MOSFETs outperform the IGBT switch.

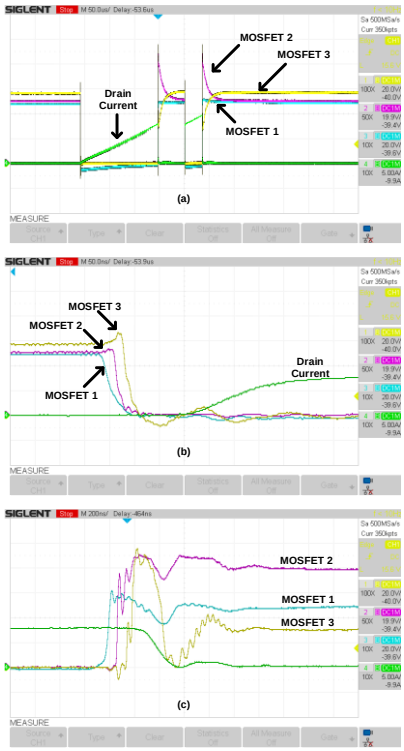

Fig. 6. Experimental DPT results (a) full waveform view for the drain current and MOSFETs' V_{DS} (b) zoom view of the on-transition and (c) off-transition

5. Experimantal Results

5.1 Double Pulse Testing

The proposed topology was built and tested experimentally to validate the design. An experimental low voltage prototype of the proposed circuit has been built for 3 MOSFETs. The conducted test is a DPT with a load inductance of 1800µH and the freewheeling diode is STPSC1206 Schottky silicon carbide diode. The input voltage is 150V with bulk capacitor array. The used MOSFETs are IRF1407 with a breaking voltage of 75V. Micsig differential voltage and current probs are used with 100MHz bandwidth. The DPT signals are produced by a microcontroller.

Fig. 6 shows the experimental results of double pulsing the three MOSFETS. As shown, they are switching properly between the on and of states and vice-versa which approves the functionality of the proposed design. It is observed that MOSFET1 has the fastest response to the pulse signal followed by MOSFET2 which is exposed to a voltage spike that might drive it in avalanche if a small voltage room was allowed in the design between the operating steady state voltage and the breaking voltage. This spike can be also avoided by the selection of a larger coupling capacitor, but this will compromise the switching speed. The off steady state voltages are not accurately balanced due to unavoidable leakage current differences between the MOSFETs in this design. The turn on switching time is 120ns while the off-transition time is 550ns. From Fig. 6b, during the on-transition, the current starts flowing through the MOSFETs when the voltages across them become zero which reveals a soft switching transition. On the other hand, the off transiting is hard switching. Table 2 shows the switching energy loss during the on and off transitions. The three MOSFETs have been replaced with a single gate driver and a single IGBT, STGB5H60DF. The table shows that the single switch has a higher turn on loss but less turn off loss. Therefore, there is a trade of between the switching losses and voltage stress for reliability objective.

5.2 Low Gain Buck Converter

A buck converter was built with an input voltage of 120V and output voltage of 20V. The duty cycle is set to 10% at a switching frequency of 30kHz and a load of 10Ω.
Fig. 7 depicts the voltage and current waveforms of the buck converter MOSFETs. It is worth mentioning that the proposed design here is used as high-side gate driving. The results show a proper switching for the three MOSFETs. The steady state voltage stresses on each MOSFET are 39V, 40V and 41V respectively. The three MOSFETs have been replaced with a single gate driver and a single IGBT, STGB5H60DF, with a breakdown voltage of 600V. The voltage and current waveforms of the IGBT are shown in Fig. 8. The voltage stress on the IGBT is 120V. Therefore, by the proposed driver, seriesing power switches was enabled to reduce the stresses and consequently the power losses during switching due to less voltage, which eventually requires less cooling requirements. It does not seem, from the results, that it has an impact on the current transient waveform and then on $^{di}/_{dt}$. However, the exposed $^{dv}/_{dt}$ at each MOSFET terminal is spread over time as shown in Fig. 6c and Fig. 7c, which contributes to increase the operation reliability of the MOSFETs. The measured $^{dv}/_{dt}$ for each MOSFET are $1\,^{V}/_{ns}$, $1.7\,^{V}/_{ns}$ and $1.6\,^{V}/_{ns}$ respectively and it is less than 50% of the maximum rating in the datasheet of $4.6\,^{V}/_{ns}$. The measured $^{dv}/_{dt}$ for the IGBT is $6.25\,^{V}/_{ns}$.

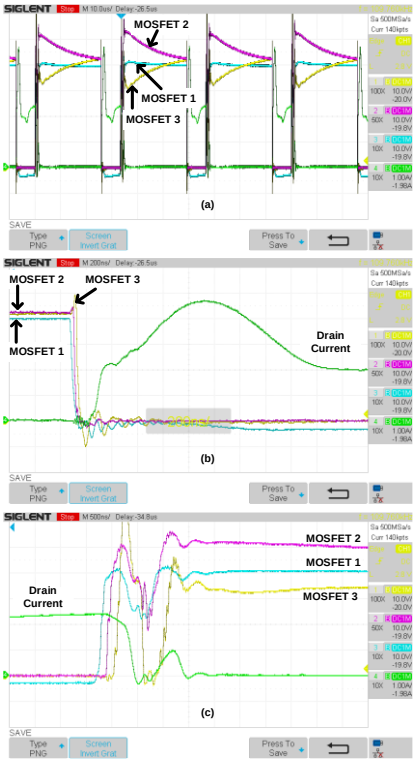

Fig. 7. Experimantal results of series MOSFETs in a buck converter (a) full waveform view for the drain current and MOSFETs' V_{DS} (b) zoom view of the on-transition and (c) off-transition

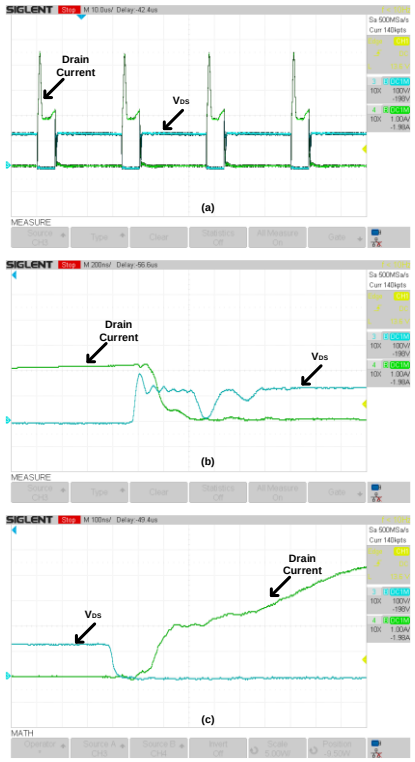

Fig. 8. Experimantal results of a single IGBT in a buck converter (a) full waveform view for the collector current and the IGBT V_{CE} (b) zoom view of the on-transition and (c) off-transition

Table 2 Switching energy loss

	MOSFET	$E_{on}(\mu J)$	$E_{off}(\mu J)$
Series	M1	0.001	27.3
	M2	0.006	19.5
	M3	0.006	27.3
Single	M1	0.047	32.4

6. Conclusion

In this paper, a low gain buck converter is used to assess the performance of series SiC MOSFET against a high breaking voltage IGBT to step down 3000V to 48V. Each MOSFET is able to block 1200V. A driving circuit is proposed with a single gate driver to be able to switch on/off the three MOSFETs. The double pulse testing validated the operation of the driving circuit. The buck converter shown high performance when it used the three MOSFETs compared with a single IGBT. In addition, the electrical and thermal stresses have been distributed leading to longer lifetime and less colling requirement.

References

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[2] K. Mainali *et al.*, "A Transformerless Intelligent Power Substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electron. Mag.*, vol. 2, no. 3, pp. 31–43, Sep. 2015, doi: 10.1109/MPEL.2015.2449271.

[3] A. Bolotnikov *et al.*, "Overview of 1.2kV - 2.2kV SiC MOSFETs targeted for industrial power conversion applications," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2015-May, no. May, pp. 2445–2452, May 2015, doi: 10.1109/APEC.2015.7104691.

[4] S. Ji, T. Lu, Z. Zhao, H. Yu, and L. Yuan, "Series-Connected HV-IGBTs Using Active Voltage Balancing Control with Status Feedback Circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4165–4174, 2015, doi: 10.1109/TPEL.2014.2360189.

[5] P. Grbović, "High-voltage auxiliary power supply using series-connected MOSFETs and floating self-driving technique," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1446–1455, 2009, doi: 10.1109/TIE.2009.2012418.

[6] P. J. Grbović, "Loss-free balancing circuit for series connection of electrolytic capacitors using an auxiliary switch-mode power supply," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 221–231, 2009, doi: 10.1109/TPEL.2008.2005579.

[7] H. L. Hess and R. J. Baker, "Transformerless capacitive coupling of gate signals for series operation of power MOS devices," *IEEE Trans. Power Electron.*, vol. 15, no. 5, pp. 923–930, Sep. 2000, doi: 10.1109/63.867682.

[8] Y. Ren *et al.*, "A Compact Gate Control and Voltage-Balancing Circuit for Series-Connected SiC MOSFETs and Its Application in a DC Breaker," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8299–8309, Oct. 2017, doi: 10.1109/TIE.2017.2711579.