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OLUSOLA, OI, SALIM, HI and DHARMADASA, I <http://orcid.org/0000-0001-7988-669X>

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One-sided rectifying p-n junction diodes fabricated from n-CdS and p-ZnTe:Te semiconductors

O.I. Olusola[1,2,*], H.I. Salim[1,3] and I.M. Dharmadasa[1]

[1]Electronic Materials and Sensors Group, Materials and Engineering Research Institute, Sheffield Hallam University, Sheffield S1 1WB, United Kingdom.

[2]Department of Physics, School of Science, The Federal University of Technology, Akure (FUTA), P.M.B. 704, Nigeria.

[3]Department of Physics, Faculty of Science, University of Zakho (UOZ), Zakho City, Kurdistan Region of Iraq.

*E-mail: olajideibk@yahoo.com Tel: +44 114 225 6910 Fax: +44 114 225 6930

Abstract

The fabrication of a one-sided p-n hetero-junction diodes have been successfully carried out using both p-type ZnTe and n-CdS semiconductors. Chemical bath deposition (CBD) and electrodeposition (ED) techniques have been used in the deposition of n-CdS and p-ZnTe layers respectively. Before the fabrication of the one-sided p-n hetero-junction diodes, the electrical properties of glass/FTO/p-ZnTe/Al and glass/FTO/n-CdS/Au rectifying structures were separately studied using capacitance-voltage (C-V) technique so as to determine the doping density of each of the thin films. The results from C-V analyses showed that p-ZnTe is moderately doped with an acceptor density of 3.55×10^{15} cm^{-3} while n-CdS is heavily doped with a donor density of 9.00×10^{19} cm^{-3}. The heavy doping of n-CdS and moderate doping of p-ZnTe will make the interface between n-CdS and p-ZnTe thin films a one-sided n^+p diode. Therefore, to fabricate the CdS/ZnTe hetero-structure, it was ensured that approximately same thickness of CdS and ZnTe thin films being used in the initial experiment to study the electrical properties of glass/FTO/n-CdS/Au and glass/FTO/p-ZnTe/Al were also used in the development of the one-sided n^+p junction diodes to obtain more accurate results. The electronic properties of the device structure were studied using both current-voltage (I-V) and C-V measurement techniques. The I-V results show that the one-sided n^+p hetero-junction diodes possess good rectifying quality with a series resistance (R_s) of ~35 Ω and rectification factors (RF) exceeding $10^{2.7}$ under dark condition. The results of the C-V analyses showed that the acceptor density of the one-sided n^+p hetero-junction diode is of the order of 10^{15} cm^{-3} while the donor density is of the order of 10^{18} cm^{-3}. The results obtained from this analysis still showed the moderate doping of p-ZnTe and the degenerate nature of n-CdS.

Keywords: One-sided n^+p junction diode, n-CdS, p-ZnTe, donor density, acceptor density.

1.0 Introduction

CdS and ZnTe are important wide bandgap II-VI semiconductor materials with direct bandgaps of 2.42 eV [1] and 2.26 eV [2] respectively. They are appropriate for applications especially in fabrication of large area electronic devices such as light emitting diodes (LEDs), thin-film solar cells and display devices. CdS is a well-known n-type semiconductor material and has found application as window layers most especially in CdTe [3] and $CuInGaSe_2$ [4] based solar cells. This material is grown using variety of techniques such as; sputtering [5], molecular beam epitaxy (MBE) [6], chemical bath deposition (CBD) [7] and electrodeposition (ED) [8]. Depending on the application, ZnTe can be a window, intermediate or a back-contact layer to thin film solar cells most especially in CdTe-based solar cells [2,9]. Other uses include; LEDs, X-ray detectors and photoresistors [2]. ZnTe is grown using different methods, such as; sputtering [10], MBE [11], ED [12] and successive ionic layer adsorption and reaction (SILAR) [13]. Mostly in the literature, ZnTe thin film materials have been generally reported to be p-type [14]. The difficulty in achieving n-type ZnTe via intrinsic doping has been mainly attributed to self-compensation [14,15] and native defects in the ZnTe material [12]. However, in one of our recent research works; we have been able to show that n-type ZnTe layers are also achievable by intrinsic doping [16].

The most widely studied II-VI binary compound semiconductors for photovoltaic applications are CdTe and CdS thin films. Both materials have been used to develop p-n hetero-junction (HJ) device structure for solar cells application [17,18]. In the recent times, other device structures have been proposed to be suitable for applications in electronic devices. Some of these structures are n-ZnSe/p-ZnTe/n-CdSe multi-layers for application in tandem solar cells [19], ZnO/ZnSe/ZnTe HJ's for application in ZnTe-based solar cells [20], p-ZnTe/n-ZnO HJ for application as light emitting diodes [21], n-CdSe/p-ZnSe HJ for diode and solar cells application [22]. The study of hetero-junction devices based on ZnTe/CdS has also been carried out by many researchers using different growth techniques for different application purposes. Aven et al. studied the growth pattern of CdS on ZnTe single crystals and showed that epitaxial deposit of CdS is obtainable only on the (111) plane of ZnTe [23]. Pfisterer and Shock [24] fabricated thin film hetero-junction photovoltaic cells based on ZnTe/CdS. The ZnTe was deposited on Ag-coated glass/CdS substrate by vacuum evaporation technique. Ota et al. [25] developed a light-emitting hetero-junction diode based on p-ZnTe single crystal substrate and n-CdS. The ZnTe and CdS thin films were grown by Bridgman and vapour epitaxy methods respectively achieving electroluminescence in both

forward and reverse bias. Also in another work carried out by Ota et al. [26], authors showed that the ZnTe/CdS hetero-junctions possess rectifying ability with high ideality factor, n = 3.40 when measured at room temperature (300 K). One vital application area that has not been fully explored for the ZnTe/CdS hetero-junction semiconductor is in the aspect of its usability in the making of a one-sided abrupt p-n rectifying diode. The fabrication of one-sided abrupt p-n junction diode have been extensively studied using III-V compound semiconductors such as GaAs, GaP [27] and elemental semiconductors such as Ge and Si [28]. Kabra et al. [29] have also been able to fabricate a rectifying nano HJ diode using a combination of II-VI binary compound semiconductor (p-ZnO) and n-Si which belongs to an elemental semiconductor. The electronic parameters obtained by Kabra et al. [29] showed that the authors successfully made p-n^+ diode from p-ZnO and n-Si.

In this paper, we have successfully demonstrated that a one-sided rectifying n^+p junction diode can be fabricated using n-CdS and p-ZnTe thin films all from II-VI binary compound semiconductors. All the electronic parameters obtained under C-V measurements attested to this situation. Also in this paper, we demonstrate that by increasing the thickness of the ZnTe layer grown in a Te-rich ZnTe electrolyte, the bandgap of the ZnTe layer can be modified.

2.0 Experimental details

In this work, CdS and ZnTe layers have been grown by CBD and ED techniques respectively. CBD technique was chosen to grow CdS thin films in this work because it has proven to be a very appropriate growth technique to deposit CdS layers for photovoltaic applications [30]. Some of the advantages of CBD technique include uniform coverage of the substrate (such as FTO) with films of low thickness [30], growth of highly insoluble binary compound semiconductors [31] and low-cost with simplicity of equipment [32]. ED technique was also used in this work to deposit ZnTe thin films because electrodeposition allows the bandgap of compound semiconductors to be easily tuned by adjusting the growth parameters [16,33]. It is also one of the suitable growth techniques to prepare continuous and thin semiconductor films [34]. Also, ED technique allows fine control of the film thickness by changing the deposition potential and time. Other advantages proffered by the technique include low temperature growth, low capital cost, simplicity, scalability and self-purification of the electrolyte during growth [35]. The CdS thin films of thickness ~45 nm was grown on conductive glass substrate as a window layer to ZnTe while the ZnTe layer of ~1.20 µm thickness was grown on CdS surfaces in a Te-rich ZnTe electrolyte. Researchers have shown

that to produce diodes of good rectifying properties from ZnTe-CdS hetero-junctions, the ZnTe must be prepared in a Te-rich condition (ZnTe:Te) [25].

The CdS thin film was prepared from CBD bath containing 45 × 10^{-3} M of cadmium acetate, 30 × 10^{-3} M of thiourea and 10 × 10^{-2} M of ammonium acetate in 200 ml of de-ionised water. The pH of the solution was adjusted to 9.10±0.02 using NH_4OH and the overall reaction was completed within 35 minutes at a temperature of 70°C. The ZnTe electrolyte was prepared by adding 0.015 M $ZnSO_4.7H_2O$ and 10 ml of dissolved TeO_2 in 800 ml of de-ionised water. For the ZnTe, the growth temperature, deposition potential and pH of the electrolyte used for electroplating were ~80°C, 1600 mV and 3.50±0.02 respectively. The CdS/ZnTe device structure was thoroughly rinsed with de-ionised water and methanol and dried with nitrogen gas before being transferred to a metal evaporator where circular gold (Au) contacts of 3 mm diameter and ~100 nm thickness were evaporated. The Au metal was used to form ohmic contacts to p-ZnTe.

The I-V characteristics of n^+p junction diodes fabricated from glass/FTO/n-CdS/p-ZnTe/Au were measured with a fully automated I-V system using Keithley 614 digital electrometer and a DC voltage source. Hewlett Packard 4284A precision LCR meter and DC voltage source were used to carry out the C-V measurements. C-V measurements were carried out at 1 MHz signal to avoid the effects of defects on capacitance measurements. The schematic diagram of the glass/FTO/n-CdS/p-ZnTe/Au hetero-junction diode is shown in Fig. 1.

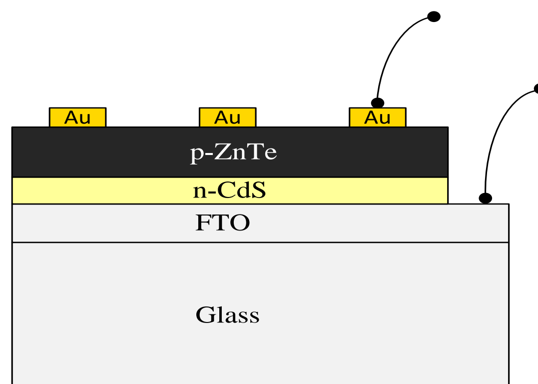

Fig. 1. Schematic diagram of the glass/FTO/n-CdS/p-ZnTe/Au structures.

3.0 Material characterisation before fabrication of p-n junction diodes

Before using the CdS and ZnTe layers for fabricating electronic devices, they were first fully characterised for their properties; full details of the growth and characterisation of CBD-CdS analysis can be found in our early publications by Chaure et. al [36] and Samantilleke et. al

[37]. Our previous communications on electroplated ZnTe semiconductors by Fauzi et.al [12] using $ZnCl_2$ precursor and Olusola et al. [16] using $ZnSO_4$ precursor elaborate more on the characterisation of ED-ZnTe thin films using different analytical techniques such as X-ray diffraction (XRD), Raman spectroscopy, UV-Vis spectrophotometry, photoelectrochemical (PEC) cell measurements, scanning electron microscopy (SEM) and 3D-atomic force microscopy (3D-AFM) techniques.

In this paper, only a summary of electrical, optical and structural properties of layers used are presented using PEC cell measurements, optical absorption and XRD techniques respectively. This is necessary to determine the right condition for achieving good optoelectronic device parameters. The PEC cell results show that CdS layers have n-type electrical conductivity while ZnTe layers are p-type in electrical conduction. The optical absorption curves of n-CdS and p-ZnTe thin films are shown in Fig. 2. The bandgap is estimated by extrapolating the straight line portion of the absorption curve to the photon energy axis when the square of absorbance is equal to zero (A^2=0). The bandgap of n-CdS as shown in Fig. 2(a) is estimated to be ~2.40 eV, this value nearly corresponds to the bandgap of stoichiometric CdS [1]. The visual appearance of CBD-CdS layer is illustrated in Fig. 3(a).

Figs. 2(b) and 2(c) show the optical absorption curves of ZnTe layers grown at different time duration of 30 minutes and 2 hours while the visual appearance of ZnTe layers grown for approximately 30 minutes and 2 hours are shown in Figs. 3(b) and 3(c) . Both layers were grown in a Te-rich ZnTe electrolyte. As shown in Fig. 2(b), the energy bandgap obtained for ZnTe layer grown for 30 minutes duration is ~2.20 eV; this value is close to bandgap reported for the stoichiometry bulk ZnTe layer.

The bandgap of Te-rich p-ZnTe (ZnTe:Te) as estimated from Fig. 2(c) is ~1.30 eV; this value deviates from the bandgap of stoichiometric ZnTe which is reported to be in the range (2.10–2.26) eV [12]. This variation is as a result of the Te-richness in ZnTe layer being used in the fabrication of the p-n junction diode. As shown in Fig. 3(b), the Te-rich ZnTe layer appears very dark in appearance thus making it to be highly light absorbing. Te being a semi-metal has a very low bandgap of 0.37 eV [38] and since the ZnTe layers were grown in a Te-rich ZnTe electrolyte for longer duration, more Te easily comes to the surface of the ZnTe layer due to the redox potential of Te atom. This phenomena causes a reduction in the bandgap from ~2.20 to ~1.30 eV providing a suitable method for bandgap grading. The optical absorption curves in Figs. 2(b) and 2(c) thus show that the bandgap of ZnTe is tunable by

controlling the deposition time, the amount of Te in the ZnTe electrolyte or simply by changing the deposition voltage. It must be noted that the deposition time also determines how much Te and Zn is deposited on the cathode.

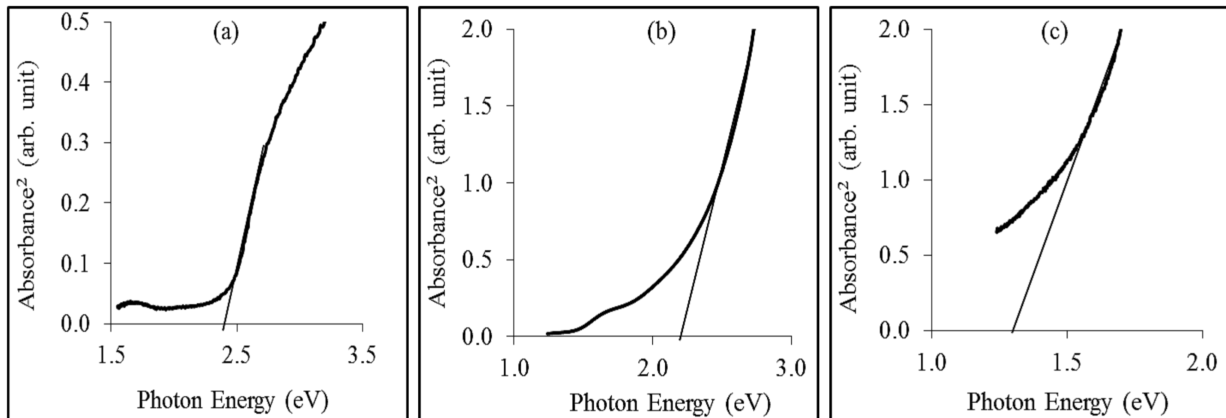

Fig. 2. (a) Typical optical absorption graphs for: (a) CdS layer annealed at 400°C, 20 minutes in air, (b) Te-rich ZnTe layer grown for 30 minutes and annealed at 300°C, 10 minutes in air and (c) Te-rich ZnTe layer grown for 2 hours and annealed at 300°C, 10 minutes in air.

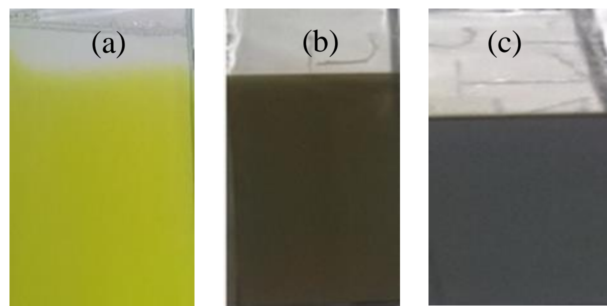

Fig. 3. Visual appearance of (a) CBD CdS and electroplated ZnTe layers grown at same cathodic potential of 1600 mV for different duration of (b) 30 minutes and (c) 2 hours.

The structural properties of the CdS and ZnTe layers were studied by using X-ray diffraction (XRD) technique. The XRD patterns were obtained by using Philips PW3710 X'pert diffractometer with Cu-K_{α} monochromator of wavelength, λ= 1.54 Å in the range of 2θ = (10-70)^{o}. Fig. 4 shows a typical XRD pattern of heat-treated glass/FTO/n-CdS structure. The annealing was carried out in air at a temperature of 400°C for 20 minutes. The diffraction pattern reveals a polycrystalline CdS thin film with cubic structure having its preferred orientation along (111) plane. It should be noted that peak with preferred orientation also coincide with the FTO peak at 2θ=26.41^{o}.

Fig. 5 shows the XRD patterns of heat-treated glass/FTO/p-ZnTe layers grown at 30 minutes and 2 hours. The ZnTe layers were annealed at 300°C for 10 minutes in air. The XRD spectra

show that the electroplated ZnTe layers are polycrystalline with hexagonal crystal structure. The preferred orientation is found to be along the (100) plane for both ZnTe layers. ZnTe peaks with lower intensities were also observed along (110) and (103) planes with hexagonal crystal structures. However, there are also Te peaks that arise as a result of excess Te in the ZnTe bath and growth duration. These Te peaks are more pronounced in the ZnTe layer grown for 2 hours and they have hexagonal crystal structures. The Te peaks occurred along (100) and (110) planes. It should be noted that both ZnTe layers grown for 30 minutes and 2 hours exhibit the prominent ZnTe peak along (100) plane. As seen in Fig. 5, the ZnTe layer grown for 2 hours is more crystalline than the ones grown for 30 minutes due to the higher peak intensity observed at 2 hours of deposition duration along preferred orientation plane. This information from the XRD analysis suggests that the low bandgap of ~1.30 eV obtained for ZnTe layers grown for 2 hours (Fig. 2(c)) may be due to the presence of additional Te peaks as revealed from the XRD measurement (Fig. 5) and as earlier explained. The presence of these Te peaks thus changes the ZnTe layer from a near stoichiometric layer to a Te-rich ZnTe layer with additional Te phase.

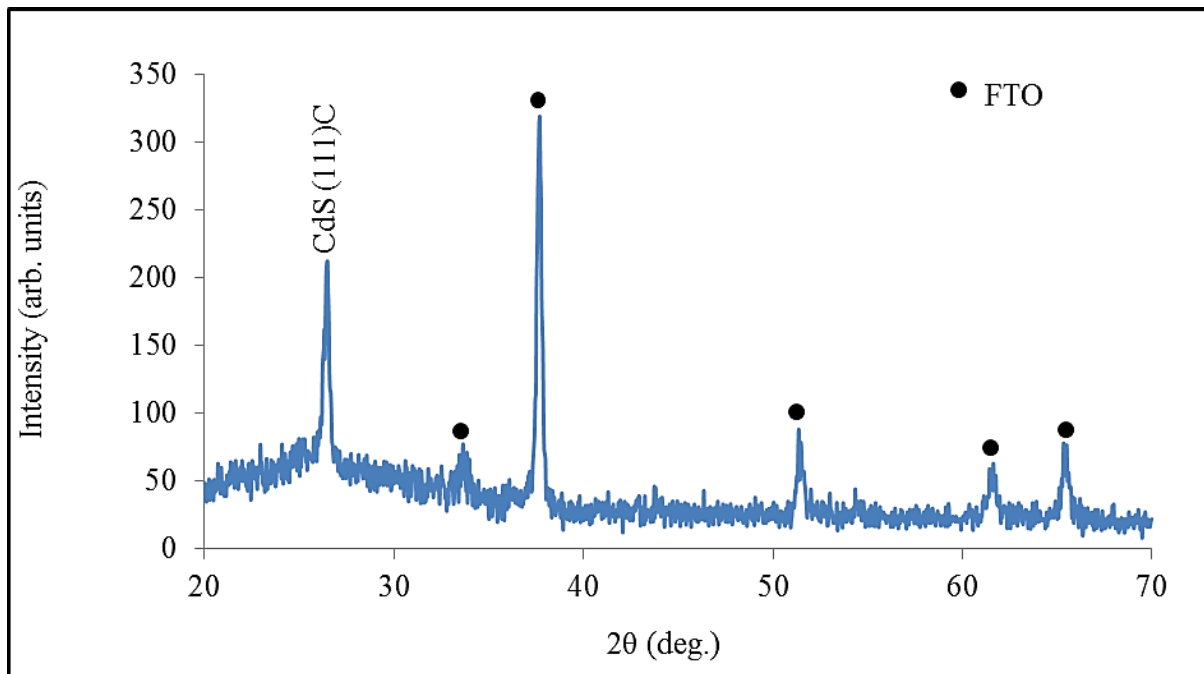

Fig. 4. A typical XRD spectrum for heat-treated CBD-CdS layer. The heat-treatment was carried out at 400°C for 20 minutes in air.

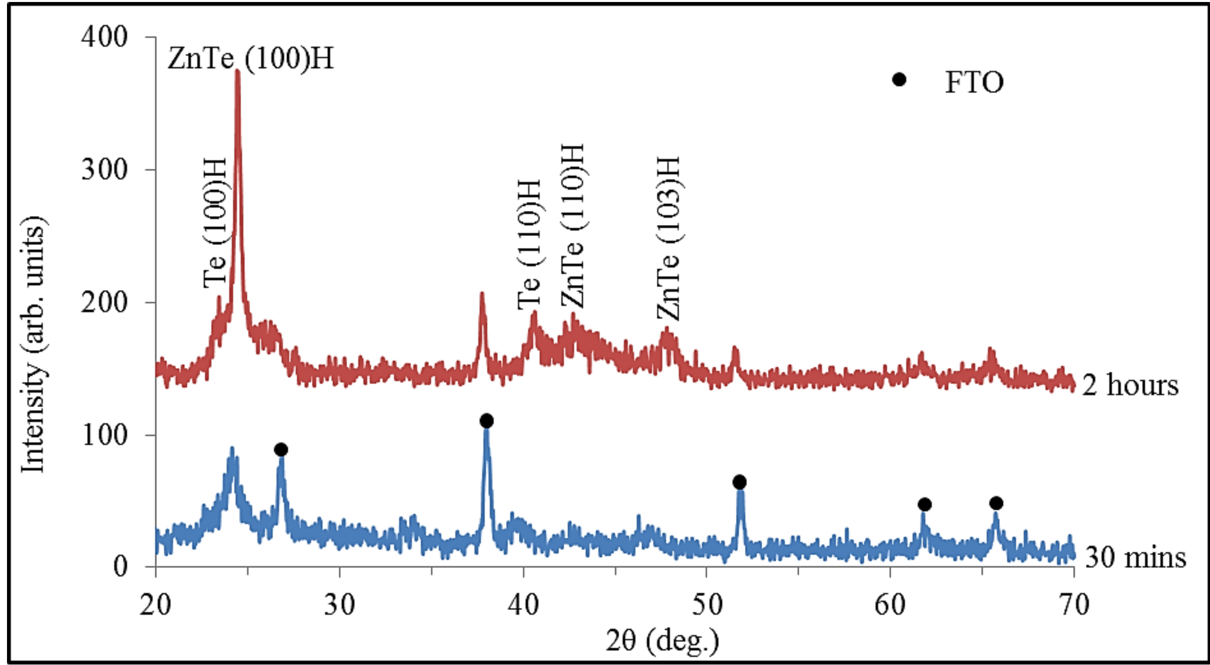

Fig. 5. XRD spectra for heat-treated ZnTe layers grown for 30 minutes and 2 hours. The heat-treatment was carried out at 300°C for 10 minutes in air.

4.0 The current-voltage characteristics of an abrupt p-n junction diode

The current-voltage (I-V) characteristics of an abrupt p-n junction diode under bias can be expressed as [28]

$$I = I_n + I_p = I_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1)$$

where I is the effective current through the diode, I_n and I_p are current arising from electrons and holes collection respectively.

Eqn. (1) can only be used for an ideal diode whose quality or ideality factor, n = 1.00 [39]. In most cases, n is not always unity because most of the fabricated diodes are not ideal in their properties. Eqn. (1) can then be re-written as shown in Eqn. (2) in order to accommodate the non-ideality nature of practical diodes.

$$I = I_n + I_p = I_s\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (2)$$

where I_s is the reverse saturation current derived from the extrapolation of the intercept of Log I at V = 0 and is described by:

$$I_s = SA^*T^2 \exp\left(\frac{-q\phi_{bo}}{kT}\right) \quad (3)$$

where k is the Boltzmann constant, 1.38×10^{-23} $m^2kgs^{-2}K^{-1}$, T is the temperature measured in Kelvin, q is the electronic charge, S is the effective surface area of the measured diode and A^* is the effective Richardson constant. ϕ_{bo} is the barrier height at zero-bias and can be deduced from Eqn. (4) once I_s is determined from the intercept of the log-linear I-V curve.

$$\phi_{bo} = \frac{kT}{q}\ln\left(\frac{SA^*T^2}{I_s}\right) \quad (4)$$

The effective Richardson constant for the ZnTe absorber layer and CdS window layer have been calculated to be 24.0 and 25.2 $Acm^{-2}K^{-2}$ respectively using Eqn. (5) [40].

$$A^* = \frac{4\pi m^* k^2 q}{h^3} \quad (5)$$

m^* is the effective mass of charge carriers and it varies from one semiconductor material to the other. For a p-type semiconductor, m^* is denoted as m_p^*; while for an n-type semiconductor, m^* is represented as m_e^*. $m_p^* = 0.20m_o$ is the effective hole mass for p-ZnTe, $m_e^* = 0.21m_o$ is the effective electron mass for n-CdS, $m_o = 9.1 \times 10^{-31}$ kg is the rest mass of electron and $h = 6.626 \times 10^{-30}$ cm^2kgs^{-1} is the Planck's constant.

The ideality factor (n) of p-n junction diode can be calculated from the slope of the log-linear I-V curve by using Eqn. (6).

$$n \cong 16.78\left(\frac{\partial V}{\partial(\log_{10} I)}\right) \quad (6)$$

4.1 I-V Characteristics of n-CdS/p-ZnTe hetero-junction diodes under dark condition.

I-V measurements provide a valuable way to test the electronic quality of a semiconductor material. These measurements were carried out using the device structure glass/FTO/n-CdS/p-ZnTe/Au. Since the device structure under consideration has a junction between the n- and p- region, it is therefore of utmost necessity to form ohmic contacts to the window layer which is n-CdS and p-ZnTe which is the absorber layer. The electron affinity of n-CdS layer

has been reported to be 4.80 eV [41] while the work function of FTO is 4.40 eV [42]. The underlying FTO subtrate to n-CdS already creates an ohmic contact to n-CdS since the work function of FTO metal contact is lower than the electron affinity of n-CdS. With regards to the p-ZnTe, its electron affinity has been reported to be 3.53 eV [43] while the work function of Au metal contact is 5.25 eV [41]. Therefore, to create an ohmic contact to p-ZnTe, a metal such as Au with higher workfunction is needed. Fig. 6(a) shows the log-linear I-V characteristics of glass/FTO/n-CdS/p-ZnTe/Au device structure. From Fig. 6(a), the rectification factor (*RF*), reverse saturation current (I_s), barrier height (ϕ_{bo}) and ideality factor (n) were determined. The *RF* which is defined as the ratio of forward current (I_F) to reverse current (I_R) at a bias voltage of ~1.0 V is $10^{2.7}$. I_s of 2.82 μA was obtained from the intercept of the Log I axis. By inserting the value of I_s into Eqn. (4), ϕ_{bo}>0.64 eV was estimated. By determining the slope of Log-linear I-V and using the obtained values in Eqn. (6), we were able to obtain an n value of 2.89. A series resistance (R_s) of ~35.0 Ω and shunt resistance (R_{sh}) of ~30.0 kΩ were obtained from the linear-linear I-V characteristics shown in Fig. 6(b).

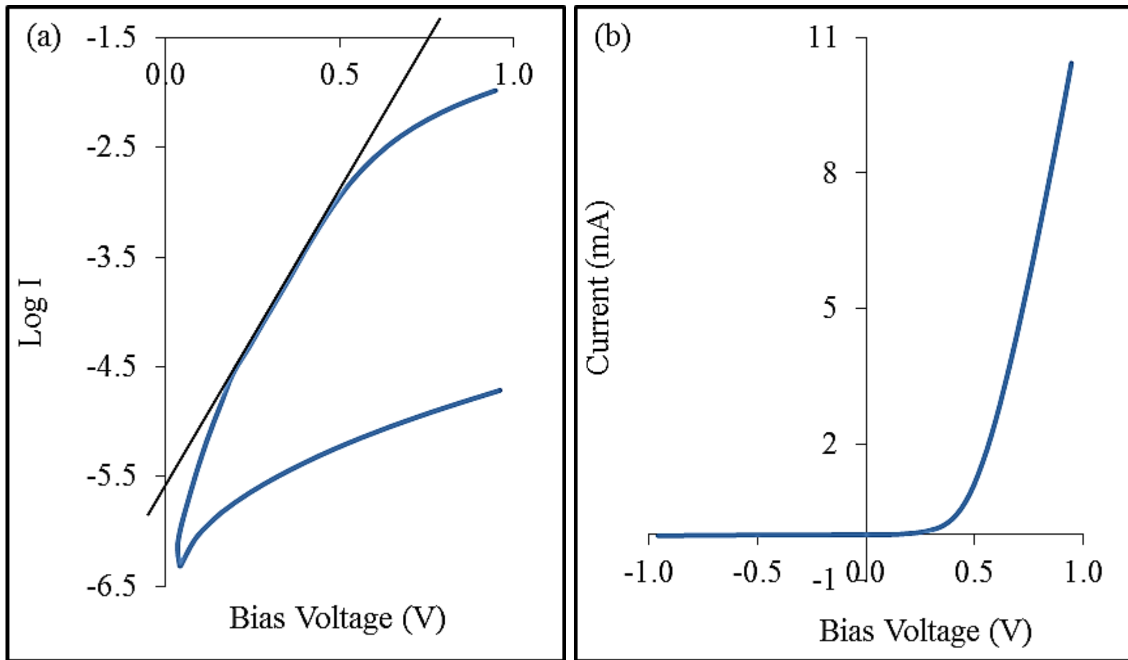

Fig. 6. I-V characteristics of the glass/FTO/n-CdS/p-ZnTe/Au diode under dark condition, (a) log-linear and (b) linear-linear.

RF is an important diode parameter that helps in determining the quality of a rectifying diode. A *RF* of ~10^2 is adequate for application in some electronic devices such as diodes and solar

cells [29,44]. The result shows that the fabricated diode possesses good *RF* of ~$10^{2.7}$ to make them suitable for application as electronic devices. I_s is an important diode electronic parameter which distinguish one diode from the other and it is a small current which flows as a result of the minority carriers in the reverse direction when bias voltage is zero. The magnitude of the reverse saturation current varies from one semiconductor diode to the other and it is a determinant of the quality of a rectifying diode [45]. For instance, I_s for a Si diode varies between ~10^{-10} to ~10^{-12} A and ~10^{-4} A for Ge diode. For the p-n homojunction diodes fabricated from glass/FTO/n-ZnTe/p-ZnTe/Au device structure by Olusola et al.[16], the I_s value was given to be in the order of 10^{-9}A. For the p-n hetero-junction diodes fabricated in this work from n-CdS/p-ZnTe, I_s is of the order of 10^{-6} A. For a diode to possess good electronic quality, the level of recombination of holes and electrons at the interface and within the bulk of the device (material) must be reduced. To achieve this, I_s which is a measure of the recombination in a device must be kept to a minimum value.

As explained by Rao et al. [46], increase in I_s may arise as a result of defects in the crystal lattice which act as recombination centres that reduce the lifetime of charge carriers. The high I_s obtained in this work may therefore arise as a result of these defects which act as trapping centres. The large n value of 2.89 shows the presence of interfacial impurities and high concentration of recombination and generation (R&G) centres in the depletion region [47,48]. Since the obtained n value is >2.00, it thus shows that tunnelling is an important current transport mechanism in the device structure [49].

5.0 Analysis of the electronic properties of fabricated device structures using capacitance - voltage (C-V) technique

Electronic parameters of thin film semiconductor devices such as depletion capacitance at zero bias (C_o), the doping concentration of the acceptors (N_A) and donors (N_D) can be found using C-V technique. Other quantities which can be deduced from the initially obtained parameters of C-V plot are: the built-in potential (V_{bi}), energy difference between the Fermi level (E_F) and the bottom of the conduction band edge (E_C) ($\Delta E = E_C - E_F$), the energy difference between the Fermi level (E_F) and the top of the valence band edge (E_V) ($\Delta E = E_F - E_V$) and the depletion layer width (W).

Prior to the fabrication of n-CdS/p-ZnTe HJ device structure, the electronic properties of Schottky diodes fabricated from glass/FTO/p-ZnTe/Al and glass/FTO/n-CdS/Au device

structures were studied using C-V technique. The C-V measurements were performed at room temperature using a frequency of 1 MHz and bias voltage of -1.0 to +1.0 V. This study was carried out to mainly determine the concentration of holes and electrons in the ZnTe and CdS thin films respectively. By undertaking this study, the doping density of each of the semiconductor materials used in this work was identified. Thus the doping density helps in determining the suitability of the semiconductor materials grown in this work to be used in the fabrication of a one-sided p-n junction diode.

Eqn. 7 (a) is applicable for a p-n junction diode where we have both the acceptors and donors [28]. The doping density (N) of the CdS and ZnTe layers can be estimated from the junction capacitance shown in Eqn. 7 (b) [28]. While applying Eqn. 7 (b) to glass/FTO/n-CdS/Au device structures, the doping density (N) becomes a donor density (N_D) while N also becomes acceptor density (N_A) for glass/FTO/p-ZnTe/Al device structures. For a one-sided p-n junction diode, Eqn. 7 (a) can be further modified to resemble Eqn. 7 (c) and 7 (d) depending on the application. For a p^+n junction diode where $N_A \gg N_D$, the doping density N becomes N_D; in this case, Eqn. 7 (a) can be simplified to Eqn. 7 (c). Likewise N becomes N_A if $N_D \gg N_A$ (n^+p) (Eqn. 7 (d)). These various applications thus allow Eqn. 7 (a) to be modified accordingly. Using Eqn. 7 (b), a graph of C^{-2} versus V can be plotted to estimate the value of N, and the built-in potential can be obtained from the intersection of C^{-2} versus V curve on bias voltage axis. The graph of C^{-2} versus V is called Mott Schottky plot, which finds application in metal semiconductor (MS) devices and one-sided p-n junction diodes [28].

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R) \times (N_A + N_D)}{e\varepsilon_s A^2 \times (N_A N_D)} \tag{7a}$$

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\varepsilon_s N A^2} \tag{7b}$$

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\varepsilon_s N_D A^2} \qquad \text{if } N_A \gg N_D \quad \{p^+n\} \tag{7c}$$

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\varepsilon_s N_A A^2} \qquad \text{if } N_D \gg N_A \quad \{n^+p\} \tag{7d}$$

In these equations, V_R is the reverse bias voltage, V_{bi} is the built-in potential, e is the charge on electron, C is the measured capacitance in Farad (F), ε_s is the permittivity of semiconductor and A is the area of the p-n junction diode, N_A is the acceptor density (or the

concentration of free holes at room temperature) and N_D is the donor density (or the concentration of free electrons at room temperature).

The width (W) of the depletion region of fabricated Schottky diodes or p-n junction diodes can be estimated from Eqn. (8)

$$W = \frac{\varepsilon_r \varepsilon_o A}{C} \tag{8}$$

Where ε_r is the relative permittivity of the material (ε_r is 10.4 for ZnTe and 8.9 for CdS [50]), ε_o is the permittivity of vacuum, A is the diode area, C is the measured capacitance at zero bias and W is the depletion width. For a fully depleted device, the depletion width is almost equal to thickness of the thin film. The depletion region forms the heart of a basic electronic device; this is where electric field is being created as a result of separation of positive and negative space charges.

The depletion width, W can also be expressed as shown in Eqn. 9 (a) [51]

$$W = X_p + X_n = \left(\left(\frac{2\varepsilon_s V_{bi}}{e} \right) \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \right)^{0.5} \tag{9a}$$

$$X_p = \left(\frac{2\varepsilon_s V_{bi}}{eN_A} \right)^{0.5} \tag{9b}$$

$$X_n = \left(\frac{2\varepsilon_s V_{bi}}{eN_D} \right)^{0.5} \tag{9c}$$

Where X_p and X_n are the distances by which the depletion region extends into the p- and n-type semiconductors respectively.

Eqn. 9 (b) is applicable to n^+p junction diodes where the doping concentration in the n-region is much greater than that of the p-region ($N_D >> N_A$). In n^+p junction diodes, $X_n << X_p$; therefore the total depletion width, $W \approx X_p$. In the same way, Eqn. 9 (c) can be used to determine the depletion width in a p^+n junction diodes where the doping concentration in the p-region is much greater than that of the n-region ($N_A >> N_D$) [39]. In p^+n junction diodes, $X_p << X_n$; therefore the total depletion width, $W \approx X_n$. Having determined W and X_p from Eqns. (8) and 9 (b) respectively, X_n can then be found by using Eqn. 9 (a). For n^+p junction diodes

where the concentration of holes in the valence band (acceptor density) is determined from the Mott-Schottky plots, the donor density can then be estimated by substituting known values of X_n and V_{bi} into Eqn. 9 (c).

Eqn. (8) can also be used in calculating the total depletion width for the p-n junction diode by using the depletion capacitance obtained from C-V plot. The estimated result from Eqn. (8) can only correspond to that obtainable from Eqn. 9 (a) if the right V_{bi} value is used. The V_{bi} is found by extrapolating the Mott-Schottky curve to the bias voltage axis at $C^{-2}=0$. [27]. The V_{bi} can therefore be accurately determined if the C^{-2} (F^{-2}) axis of the Mott-Schottky plot starts from the origin. Alternatively, the V_{bi} can be theoretically determined by applying Eqn. (17).

The effective density of states in the conduction band edge of semiconductor is given by

$$N_C = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2} \tag{10}$$

The effective density of states in the valence band edge of semiconductor is given by

$$N_V = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \tag{11}$$

The Fermi-Dirac probability function of electrons occupying the donor state is given by [28]

$$N_D = \frac{N_C}{1 + \frac{1}{g}\exp\left(\frac{E_C - E_F}{kT}\right)} \tag{12}$$

Where E_C is the lowest energy of the conduction band, E_F is the Fermi level and g is called a degeneracy factor ~2.00 for CdS donor atoms [52].

From Eqn. (12), $\Delta E = E_C - E_F = 0.693kT\ln\left(\frac{N_C}{N_D}\right)$ (13)

Eqn. (13) is therefore a very useful equation to determine the position of Fermi level in a degenerate n-type semiconductor. For non-degenerate n-type semiconductors where the

doping density is less than the effective density of states, the degeneracy factor, g in the Fermi-Dirac function is not being considered. Therefore, Eqn. (12) reduces to

$$\Delta E = E_C - E_F = kT \ln\left(\frac{N_C}{N_D}\right) \quad (14)$$

Eqn. (14) is an approximation of the Fermi-Dirac function and is mostly applied to determine the Fermi level position of a non-degenerate n-type semiconductor. Since the p-type ZnTe semiconductor used in this work is related to a non-degenerate family, Eqn. (14) can be re-written as

$$\Delta E = E_F - E_V = kT \ln\left(\frac{N_V}{N_A}\right) \quad (15)$$

$E_F - E_V$ is the difference in energy (ΔE) between the Fermi level and the top of the valence band in ZnTe.

For a p-n junction diode, the electric field, E in the semiconductor at the interface is given by

$$\mathrm{E}(x=0) = \frac{eW}{\varepsilon_s}\left(\frac{N_A \times N_D}{N_A + N_D}\right) \quad (16a)$$

For Schottky diodes fabricated from n-type and p-type semiconductors, the electric fields in the semiconductor at the MS interface are given by Eqns. 16 (b) and 16 (c) respectively. Eqns. 16 (b) and 16 (c) are also applicable to p^+n and n^+p junction diodes respectively [27].

$$\mathrm{E}(x=0) = \frac{eX_n N_D}{\varepsilon_s} \quad (16b)$$

$$\mathrm{E}(x=0) = \frac{eX_p N_A}{\varepsilon_s} \quad (16c)$$

As explained by Sze and Ng [27], most of the built-in potential and depletion region are inside the lightly doped region of the one-sided p-n junction diode. The magnitude of the built-in potential for n^+p junction diode can therefore be estimated using Eqn. (17) [27,29].

$$|V_{bi}| = \frac{|E_{max}|}{2}(W) \qquad (17)$$

5.1 Discussion of results from C-V measurements for CdS

In order to carry out C-V measurements, rectifying contacts were made by evaporating 2 mm diameter Au contacts on n-CdS layers. The C-V and Mott-Schottky plots of glass/FTO/n-CdS/Au device structure are shown in Figs. 7(a) and 7(b) respectively. As shown in Fig. 7(a), the depletion layer capacitance obtained at zero bias for the glass/FTO/n-CdS/Au device structure is 5.583 nF. By incorporating the values of the depletion layer capacitance into Eqn. (8), the width of the depletion region, *W* was estimated to be ~44.3 nm.

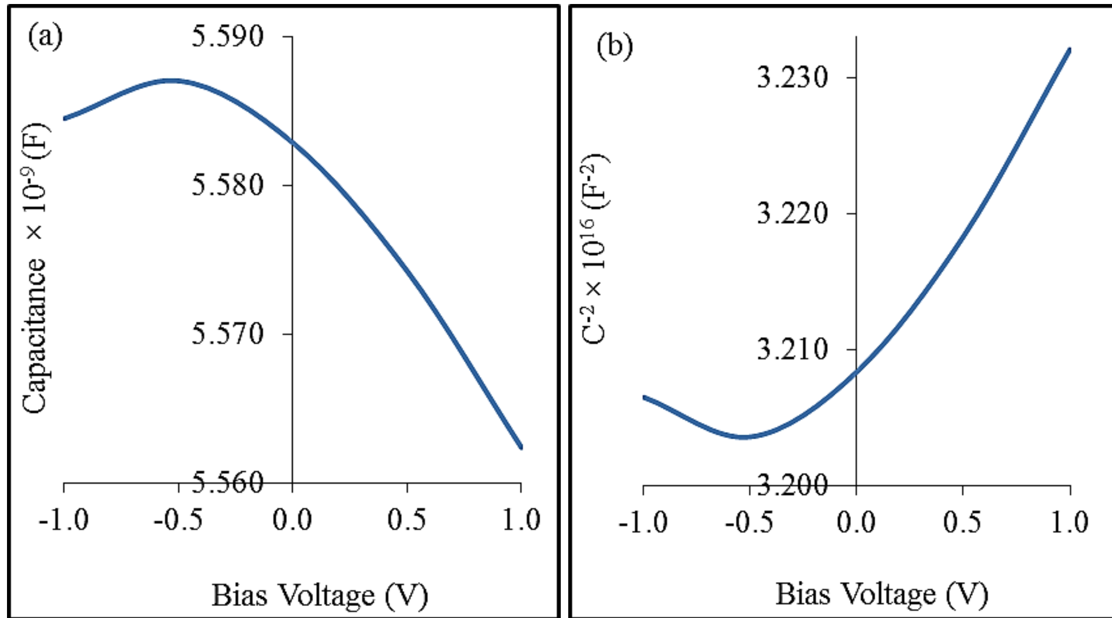

Fig. 7. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/n-CdS/Au.

Using the slope (1.79×10^{14} $F^{-2}V^{-1}$) obtained from Mott-Schottky plots in Fig. 7(b), the donor density of the CdS thin film was estimated to be 9.00×10^{19} cm^{-3}. By taking the effective electron mass of CdS to be $m_e^* = 0.21\ m_o$, the value of effective density of states in the conduction band minimum (N_C) has been found to be 2.41×10^{18} cm^{-3}. The experimental results obtained in this work show that the doping density of the CdS semiconductor is greater than the effective density of states in the conduction band of the CdS thin film. This property makes the Fermi energy level to lie within the conduction band thus making the CdS

thin film used in this work to become degenerate n-type semiconductor. The details of the C-V measurement results for Au/n-CdS Schottky diodes are shown in Table 1.

Table 1. The summary of electronic parameters obtained from n-CdS and p-ZnTe layers using C-V technique.

Electronic parameters from CV	CdS thin films	ZnTe thin films
Measured C at zero bias (F)	5.583×10^{-9}	2.620×10^{-10}
W (nm)	44.3	1100.0
E (Vcm^{-1})	8.10×10^{7}	6.81×10^{4}
N_A (cm^{-3})	------	3.55×10^{15}
N_D (cm^{-3})	9.00×10^{19}	------
N_V (cm^{-3})	------	2.24×10^{18}
N_C (cm^{-3})	2.41×10^{18}	------
$E_F - E_V$ (eV)	------	0.17
$E_C - E_F$ (eV)	-0.07	------

As explained by Neamen [28], for a semiconductor to be degenerate, the concentration of electrons (for n-type materials) or hole density (for p-type materials) should be higher than the effective density of states in the conduction band (for n-type materials) and valence band (for p-type materials). This unique property thus makes the Fermi level to be above the conduction band minimum (for n-type) or below the valence band maximum (for p-type). Also in a degenerate semiconductor, $E_C - E_F$ is $\ll kT$; that is, the Fermi level is less than kT below E_C.

To determine the Fermi level position in a degenerate semiconductor, it is important to put into consideration the degeneracy or spin factor of the degenerate semiconductor. The electron spin rotation in CdS quantum dots (QDs) was studied by Masumoto et al. and the spin factor of the electrons was found to be ~1.965±0.006 [52]. The spin factor also called degeneracy factor has been generally reported as 2.00 for donor atoms [28]. Approximating the g-factor obtained for CdS QDs by Masumoto et al. [52] to 1 decimal place, the value also tends to be equal to 2.00. Therefore in this work, g-factor of ~2.00 has been used to determine the Fermi level position in the CdS degenerate semiconductor.

As seen in Table 1, the Fermi level position ($E_C - E_F$) shows a negative value for the CdS thin film. This negative value indicates that the Fermi level position lies within the conduction band thus making E_F to be above the conduction band minimum. The graphical representation of the Fermi level position of CdS shown in Fig. 8 further illustrates that $E_C - E_F$ lies within the conduction band.

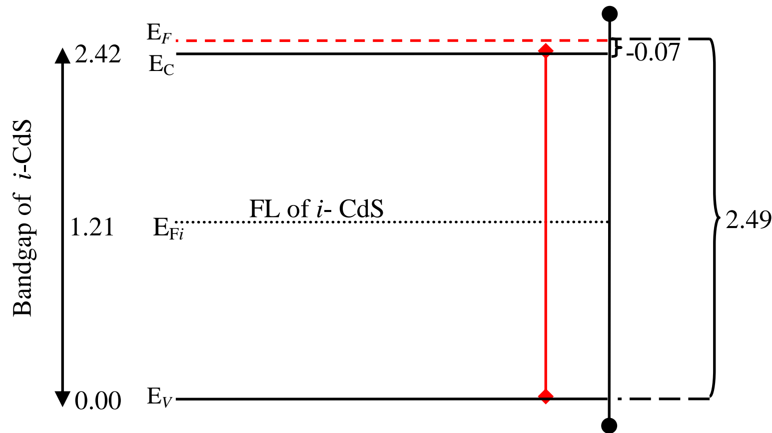

Fig. 8. Graphical representation of the Fermi level positioning for glass/FTO/CdS/Au device structure.

Thus, the fabricated CdS thin film used in this work falls in the family of the degenerate semiconductors thereby making the CdS thin film to be heavily doped as earlier discussed. Eqn. (13) has been used to determine the position of the Fermi level for the degenerate n-type CdS layer. The high doping of the CdS thin film was caused by the large concentration of donor atoms in the material. This large electron concentration arises from the fact that below E_F, the energy states are always occupied with electrons while above E_F, the energy states are mostly vacant. Therefore, since E_F is above the E_C minimum (E_{Cmin}) in the degenerate n-CdS semiconductor, the energy states below E_F are mainly occupied with donor electrons. This property of degenerate semiconductor makes it to behave in a similar manner to metals. Thus, it is expected that in degenerate semiconductors, the electric field at the metal- semiconductor (MS) interface should be higher. As seen in Table 1, the electric field in the CdS at the metal-semiconductor junction is higher than that of ZnTe. This is because of the huge concentration of mobile electrons in the CdS conduction band. Using Eqns. 16 (b) and 16 (c), the electric field for CdS and ZnTe semiconductor materials have been calculated to be 8.10×10^{7} and 6.81×10^{4} Vcm^{-1} respectively.

The width of the depletion region is equally a function of the depletion capacitance and doping concentration in the semiconductor. The higher the depletion capacitance, the greater will be the doping density in a semiconductor and the smaller will be the depletion width [28]. Table 1 shows that CdS thin film has a large depletion capacitance of 5.583 nF at zero bias, higher N_D of 9.00×10^{19} cm^{-3} and a small depletion width of 44.3 nm. This is unlike ZnTe semiconductor with moderate doping (3.55×10^{15} cm^{-3}), lesser C_o of 262 pF and higher W (1100 nm).

Since the CdS layers grown in this work have a smaller W, there is a very high tendency for electron tunnelling through the barrier to increase in the glass/FTO/n-CdS/Au MS structure. Figs. 9(a) and 9(b) show the interface where the Au metal is in direct contact with the heavily doped n-CdS thin film layer. In this situation, tunnelling may likely become the prevailing means for current transportation. Fig. 9(a) illustrates the degenerate situation where $E_C - E_F$ is $\ll kT$ while Fig. 9(b) illustrates the degenerate situation where $E_C - E_F$ is $\ll 0$ (that is negative). Fig. 9(b) is the most applicable band diagram for the degenerate n-CdS semiconductor fabricated in this work.

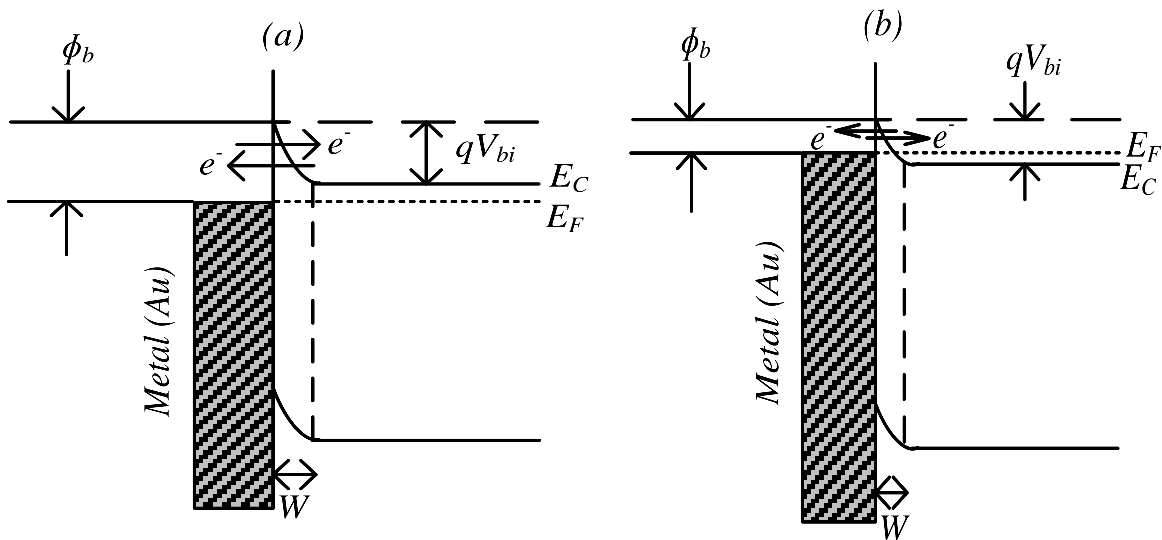

Fig. 9. Band diagram for metal/semiconductor interface with a degenerate semiconductor (a) E_C-E_F is $\ll kT$, (b) E_C-E_F is $\ll 0$

5.2 Discussion of results from C-V Measurements for ZnTe

In order to perform C-V measurements, rectifying contacts were made by evaporating 2 mm diameter Al contacts on p-ZnTe layers. Figs. 10(a) and 10(b) show the capacitance-voltage and Mott-Schottky plots of glass/FTO/p-ZnTe/Al device structure respectively. For the glass/FTO/p-ZnTe/Al device structure, the depletion capacitance (C_o) as measured from the C-V plot in Fig. 10(a) is 262 pF. By inserting the values of the depletion layer capacitance into Eqn. (8), the width of the depletion region, W was calculated to be ~1.10 µm.

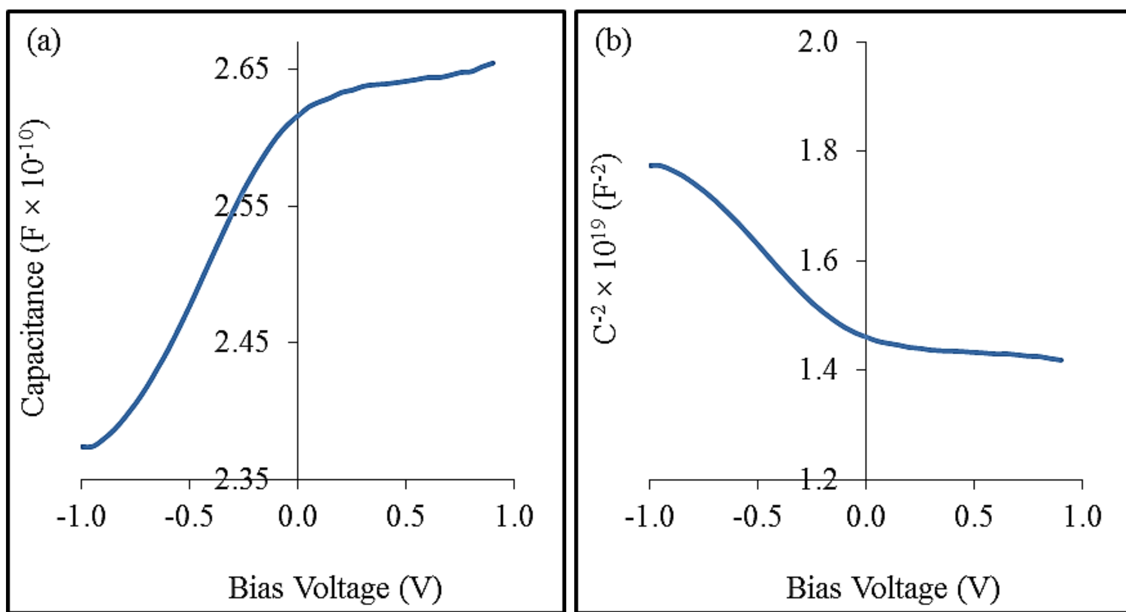

Fig. 10. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/p-ZnTe/Al.

A slope of 3.88×10^{18} $F^{-2}V^{-1}$ was obtained from the Mott-Schottky plots shown in Fig. 10(b) and with this value, the acceptor density of ZnTe layer has been calculated to be 3.55×10^{15} cm^{-3}. Using $m_p* = 0.20\ m_o$ as the effective hole mass of ZnTe, the effective density of states in the valence band edge of ZnTe thin film has been found to be 2.24×10^{18} cm^{-3}. The results obtained from this work illustrates that the concentration of holes in the ZnTe semiconductor is less than the effective density of states in the valence band edge of the ZnTe thin film. Thus the fabricated ZnTe layers used in these experiments belong to the non-degenerate p-type semiconductor with moderate doping and the position of the Fermi level lies above the valence band maximum. As also shown in Table 1, E_F - E_V for the ZnTe thin film shows a positive value which is an indication that the Fermi level position lies above the valence band

maximum. Eqn. (15) has therefore been used to determine the position of the Fermi level for the p-type ZnTe layer.

Since the ZnTe semiconductor used in this work has a moderately doped density of 3.55×10^{15} cm^{-3}, low C_o of 262 pF and large depletion width of 1100 nm, the possibility of hole tunnelling from the semiconductor into the metal will decrease in the glass/FTO/p-ZnTe/Al MS structure. Other current transportation mechanism such as emission of holes from the ZnTe semiconductor into the metal or recombination in the space-charge region may likely dominate. Fig. 11 shows the energy band diagram of the Schottky barrier formed on moderately doped ZnTe layer.

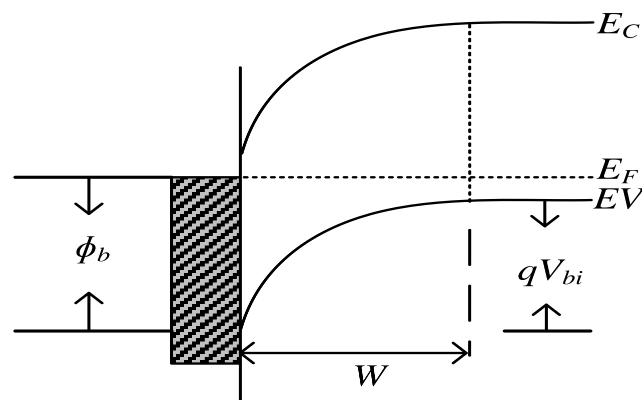

Fig. 11. Band diagram for Al/p-ZnTe Schottky diodes formed in glass/FTO/p-ZnTe/Al. Note that E_F - $E_V \gg$ kT.

Comparing Fig. 9(b) and Fig. 11 with each other, it is clear that the doping density affects the depletion width of the junction. Heavily doped material like n-CdS illustrated in Fig. 9(b) has a narrow depletion width compared to that of moderately doped p-ZnTe layer shown in Fig. 11. This in turn also affects the effective built-in potential barrier height as illustrated in both figures.

5.3 Discussion of results from C-V measurements for CdS/ZnTe hetero-junction

The C-V and Mott-Schottky plots of glass/FTO/n-CdS/p-ZnTe/Au HJ device structure are shown in Figs. 12(a) and 12(b) respectively. The depletion capacitance obtained at zero bias for the glass/FTO/n-CdS/p-ZnTe/Au device structure is 1.26 nF as illustrated in Fig. 12(a).

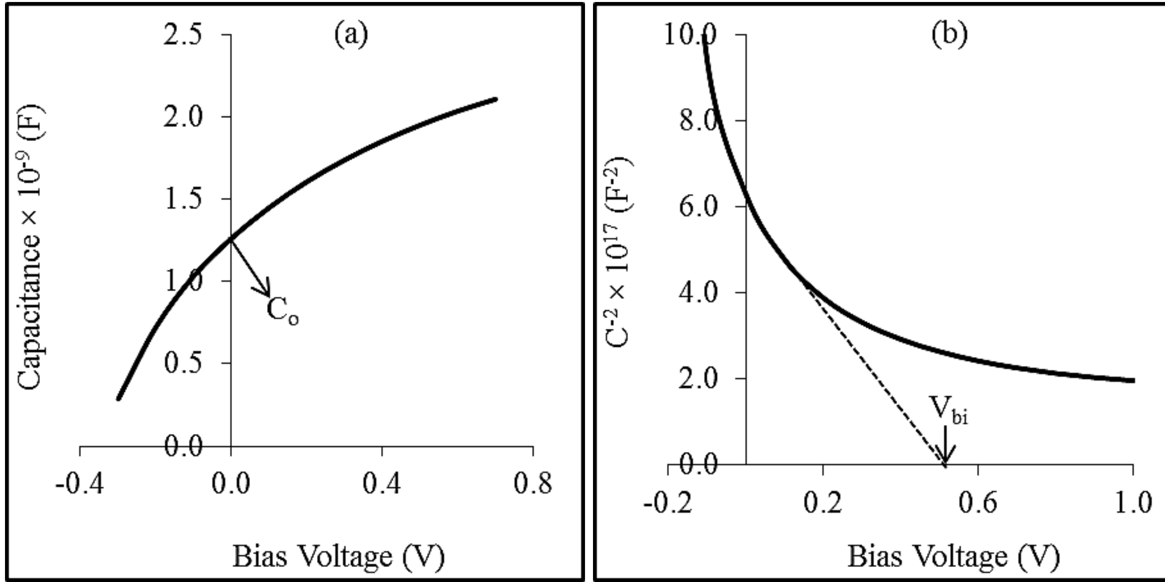

Fig. 12. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/n-CdS/p-ZnTe/Au.

By substituting the value of the depletion layer capacitance into Eqn. (8), the width of the depletion region, *W* was calculated to be 519 nm. As earlier explained, the total depletion width for the one-sided p-n junction diode can likewise be determined using Eqn. 9 (a) if the right V_{bi} value is used. The V_{bi} obtained from the Mott-Schottky plot in Fig. 12b is ~0.55 V; this value nearly corresponds with the theoretical value of ~0.58 V estimated from Eqn. (17). Also, Eqn. 9 (b) was used to find the distance by which the depletion region extends into the p-type semiconductor (that is X_p), while X_n was determined by substituting the known value of X_p into Eqn. 9 (a) (that is, X_n=W-X_p).

The acceptor density of the glass/FTO/n-CdS/p-ZnTe/Au HJ device structure was estimated to be 2.47×10^{15} cm^{-3} by using the slope (1.09×10^{18} $F^{-2}V^{-1}$) obtained from Mott-Schottky plot in Fig. 12(b). The donor density was estimated to be 3.75×10^{18} cm^{-3} by substituting known values of V_{bi} and X_n into Eqn. 9 (c). The experimental results observed in this work show that the p-ZnTe has a moderate doping while the n-CdS is heavily doped. Since the $N_D \gg N_A$, it thus shows that the fabricated hetero-junction is a one-sided n^+p junction diode. The result obtained in the n^+p HJ device structure is in good agreement with what was earlier obtained in the glass/FTO/p-ZnTe/Al and glass/FTO/n-CdS/Au device structures. Due to the high doping concentration in the n-region, the depletion width (X_n=13.0 nm) becomes very small, almost negligible. This is unlike the p-region which is moderately-doped; the moderate-

doping in the p-region thus enhances an increase in the depletion width (X_p=506.0 nm). The fabricated diode is therefore a one-sided n^+p junction diode since $N_D >> N_A$ and $X_n \ll X_p$.

The summary of electronic parameters of the fabricated n^+p junction diodes obtained by C-V measurement at room temperature is shown in Table 2. The Fermi level positions of the donor atoms and acceptor atoms were determined using Eqns. (13) and (15) respectively. The result of the Fermi level position for donor atoms show that the CdS semiconductor in the hetero-structure is degenerate since E_C-E_F is negative. For the ZnTe thin film, the Fermi level position for acceptor atoms is positive and this indicates that the E_F is situated above the E_{Vmax}. The knowledge of the Fermi level position is important in drawing the energy band diagram of the device structure; this has been further explained in section 5.4. For the abrupt n^+p junction diode fabricated from the glass/FTO/n-CdS/p-ZnTe/Au HJ device structure, the electric field at the junction has been estimated to be 2.22×10^4 Vcm^{-1} using Eqn. 16 (a). The electric field obtained for the n^+p HJ diode in this work is similar to that reported by Kabra et al. [29] for rectifying p-n junction diodes fabricated from p-ZnO/n-Si hetero-structure.

Table 2. Summary of electronic parameters obtained from glass/FTO/n-CdS/p-ZnTe/Au HJ device structures using C-V technique.

N_A (cm^{-3})	V_{bi} (V)	N_D (cm^{-3})	E_F-E_V (eV)	E_C-E_F (eV)	X_n (nm)	X_p (nm)	$W = X_n+X_p$ (nm)	E (Vcm^{-1})
2.47×10^{15}	0.55	3.75×10^{18}	0.18	-0.01	13.0	506	519	2.22×10^4

5.4 Proposed space charge density and energy band-diagram for CdS/ZnTe hetero-junction devices

By combining the n^+-CdS and p-ZnTe into a single device structure, a one-sided CdS/ZnTe n^+p junction was fabricated since $N_D >> N_A$. The knowledge of the electronic parameters in Table 2 have been used to propose the space charge density and energy band diagram of the n^+p hetero-junction device structure. Fig. 13(a) shows the probable space-charge density of n^+p junction that can be obtained after putting the two semiconductor materials together to form a device structure. Fig. 13(a) thus shows that the whole space charge layer stretches into the low-doped region of the junction. This is so because the depletion width is an inverse function of the doping concentration. From Fig. 13(a), depletion width, $W= X_p + X_n$ where X_p and X_n are the distances by which the depletion region extends into the p- and n-type semiconductor respectively. Since $N_D >> N_A$, then $X_n << X_p$; thus, the total depletion width, W

≈ X_p. The proposed energy band diagram for the n^+p hetero-junction device structure is shown in Fig. 13(b).

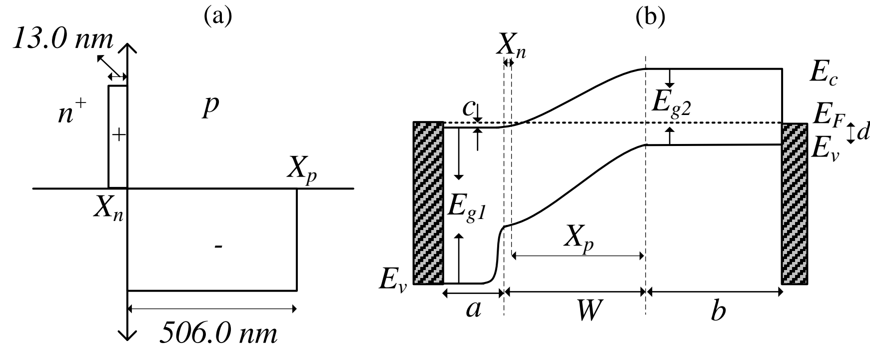

Fig. 13. (a) Proposed space charge density of one-sided CdS/ZnTe n^+p junction. (b) Proposed energy band diagram of n^+p hetero-junction device structure. E_{g1} is the CdS bandgap, E_{g2} is the ZnTe bandgap used in this work, $W = X_n + X_p$, $a+X_n$ = total thickness of CdS layer = ~45 nm, X_p+b = total thickness of ZnTe layer = ~1200 nm, $c = E_C-E_F$, $d = E_F-E_V$. Note that the above bandgap diagram is not drawn to scale.

Conclusion

The results presented in this paper show that Te-rich ZnTe layers have been successfully grown on a (111) oriented CBD CdS thin film by electrodeposition technique. The variation of Te-content in ZnTe seems to be ideal for grading of the bandgap of the layers to develop graded bandgap solar cell structures. X-ray diffraction spectrum showed that the CdS and ZnTe thin films have cubic and hexagonal crystal structures respectively. For the CdS and ZnTe layers, the preferred orientations were found to be along (111) and (100) planes respectively. The Te-richness of the ZnTe layers have been confirmed by the presence of Te peaks at (100) and (110) planes. The I-V measurements carried out on the glass/FTO/n-CdS/p-ZnTe/Au hetero-junction diode revealed its rectifying behaviour under dark condition. The C-V results showed that the p-n junction diodes fabricated from CdS/ZnTe hetero-junctions is a one-sided n^+p junction diode with $N_D >> N_A$. Work is progressing to develop solar cells using CdS/ZnTe hetero-junction layers and to also incorporate the CdS/ZnTe hetero-junction layers into a graded bandgap solar cell structure.

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