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Solar cells based on electrodeposited thin films of ZnS, CdS, CdSSe and CdTe.

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Solar Cells Based on Electrodeposited Thin Films of ZnS,

CdS, CdSSe and CdTe

Ajith R A Weerasinghe

A thesis submitted in partial fulfilment of the requirements of

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Declaration

I hereby declare that the work described in this thesis is my own work and it has not been submitted for any other award.

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I acknowledge that I am in a privileged situation so I hope and wish to utilise this situation to the benefit of fellow beings.

Abstract

The motivations of this research were to produce increased efficiency and low-cost solar cells. The production efficiency of Si solar cells has almost reached their theoretical limit, and reducing the manufacturing cost of Si solar cells is difficult to achieve due to the high-energy usage in material purifying and processing stages. Due to the low usage of materials and input energy, thin film solar cells have the potential to reduce the costs. CdS/CdTe thin film solar cells are already the cheapest on \$/W basis. The cost of CdTe solar cells can be further reduced if all the semiconducting layers are fabricated using the electrodeposition (ED) method. ED method is scalable, low in the usage of energy and raw materials. These benefits lead to the cost effective production of semiconductors. The conventional method of fabricating CdS layers produces Cd containing waste solutions routinely, which adds to the cost of solar cells.

ZnS, CdS and $CdS_{(1-x)}Se_x$ buffer and window layers and CdTe absorber layers have been successfully electrodeposited and explored under this research investigation. These layers were fully characterised using complementary techniques to evaluate the material properties. Photoelectrochemical (PEC) studies, optical absorption, X-ray diffraction (XRD), X-ray fluorescence (XRF), scanning electron microscopy (SEM), energydispersive X-ray (EDX) spectroscopy, atomic force microscopy (AFM) and Raman spectroscopy were utilised to evaluate the material properties of these solid thin film layers.

ZnS and CdS thin film layers were electrodeposited from Na-free chemical precursors to avoid the group I element (Na) to reduce deterioration of CdTe devices. Deposition parameters such as, growth substrates, temperature, pH, growth cathodic voltage, stirring rate, time and chemical concentrations were identified to fabricate the above semiconductors. To further optimise these layers, a heat treatment process specific to the material was developed. In addition, the deposition parameters of CdTe layers were further optimised. This research programme has demonstrated that electrodeposited ZnS, CdS and CdTe thin film layers have material characteristics comparable with those of the materials reported in the literature and can be used in thin film solar cell devices. Furthermore, the electrolytes were used for up to two years, reducing the wastage even further, in comparison to other fabrication methods, such as chemical bath deposition. Several large-area semiconducting layers were successfully fabricated to test the scalability of the method. Nano-rods perpendicular to the glass/FTO surface with gaps among grains in CdS layers were observed. In order to reduce the possible pinholes due the gaps, a deposition of a semiconducting layer to cover completely the substrate was investigated. $CdS_{(1-x)}Se_x$ layers were investigated to produce a layer-by-layer deposition of the material. However it was observed the surface morphology of $CdS_{(1-x)}Se_x$ is a function of the growth parameters which produced nano-wires, nano-tubes and nanosheets. This is the first recording of this effect for a low temperature deposition method, minimising the cost of producing this highly photosensitive material for use in various nano technology applications.

The basic structure experimented was glass/conducting-glass/buffer layer/window material/absorber material/metal. By utilising all the semiconducting layers developed, several solar cell device structures were designed, fabricated and tested. This included a novel all-electrodeposited multi-layer graded bandgap device, to enhance the absorption of solar photons. The device efficiencies varied from batch to batch, and efficiencies in the range (3–7)% were observed. The variations in chemical concentrations, surface states and the presence of pin-hole defects in CdS were the main reasons for the range of efficiencies obtained. In the future work section, ways to avoid these variations and to increase efficiencies are identified and presented.

Forward

Chapter 1 summarises the status of PV cell research, development and deployment. It analyses solar cell materials and growth methods, PV cell structures under current development, which can potentially improve the PV conversion efficiency while reducing the cost of manufacturing. It also looks at the status of PV applications, progress of deployment and the trends in reduction in costs. The aims and the objectives are stated in this chapter.

Chapter 2 elaborates all the experimentation and characterisation steps used in this study to improve all-electrodeposited solar cells. Material characterisation methods were carefully chosen to enhance the fabrication of solar cells in a complementary manner. The rest of the chapter highlights and discusses the experimental methods and steps employed in the preparation of semiconductor materials of ZnS, CdS, $CdS_{(1-x)}Se_x$ and CdTe. Furthermore, it investigates the main steps involved in substrate preparation and fabrication of electrodeposited solar cells.

Chapter 3 presents the wide bandgap material researched and developed in this programme to be used as a buffer layer. The material ZnS is thoroughly surveyed for its material qualities and its use in the fabrication of solar cells. The ZnS is produced from Na free precursors.

Chapter 4 presents the window layer materials researched and developed in this programme. The materials CdS and $CdS_{(1-x)}Se_x$ are produced from Na free chemical precursors. $CdS_{(1-x)}Se_x$ thin film layers are researched and developed for use in solar cells, due to the uniform growth qualities of Se.

Chapter 5 focuses on the optimisation of the only absorber layer researched in this programme, CdTe. To minimise the unwanted ion contaminations, the electrodeposition was conducted using a modified saturated calomel electrode under 3-electrode setup.

Chapter 6 presents the use of CdTe thin films as absorber layers in solar cell fabrications. Here all the other semiconductor materials researched are utilised to produce fully electrodeposited (all-ED) solar cells. Several architectures of all-ED solar cells were fabricated within this researched are discussed for a deeper understanding of the issues affecting the performance of these solar cells.

Chapter 7 summarises all the results and provides conclusions about the electrodeposition of the layers involved in this programme. This chapter also provides an overview of the issues of the all-ED solar cells fabricated under this research and finally some suggestions for future directions to improve the efficiency, reproducibility, and scalability are outlined.

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Nomenclature

Abbreviations

А	Area
AFM	Atomic Force Microscopy
AM	Air Mass
Au	Gold
CBD	Chemical Bath Deposition
CdCl ₂	Cadmium chloride
CdO	Cadmium oxide
CdS	Cadmium sulphide
CdSe	Cadmium selenide
CdTe	Cadmium telluride
CIGS	Copper Indium Gallium Diselenide
Cl	Chlorine
CSS	Closed space sublimation
C-V	Capacitance Voltage
ED	Electrodeposition
EDX	Energy Dispersive X-ray
FF	Fill Factor
FTO	Fluorine doped Tin Oxide
FWHM	Full Width at Half Maximum
НОМО	Highest occupied molecular orbital
IR	Infrared
ITO	Indium Tin Oxide

х

I-V	Current Voltage
J _{sc}	Short Circuit Current Density
LO	Longitudinal optical phonon
LUMO ·	Lowest unoccupied molecular orbital
М	Moles
MBE	Molecular Beam Epitaxy
n ₁ mole of ser	Number of electrons transferred in the reaction for the formation of one niconductor
n ₂	Idiality Factor
OPV	Organic photovoltaics
PEC	Photoelectrochemical Cell
PPL	Pinhole plugging layer
PV	Photovoltaic
R	Resistance
R&G	Recombination and Generation
R _s	Series Resistance
R_{sh}	Shunt Resistance
S	Sulphur
Se	Selenium
SeO ₃	Selenium oxide
SEM	Scanning Electron Microscopy
SnO ₂	Tin oxide
Т	Temperature (K)
TCO	Transparent Conductive Oxide
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Te	Tellurium
TeO ₂	Tellurium oxide
ТО	Transverse optical phonon
UV	Ultraviolet
Vg	Growth Voltage
V _{oc}	Open Circuit Voltage
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray diffraction
XRF	X-Ray Fluorescence
Zn	Zinc
ZnS	Zinc sulphide

Symbols

Effective Richardson constant				
Speed of light				
Magnitude of electron charge				
Internal Electric Field				
Faradays constant				
Plank constant				
Boltzmann constant				
Acceptor concentration				
Donor concentration				
Intrinsic charge carrier density				
Gas constant				
Time (s)				
Frequency				
Built in potential				
Absorption coefficient				
Wave length				
Efficiency				
Absorption coefficient				
Permittivity of free space				
Relative permittivity				
Potential barrier height				
Work function of metal				
Work function of semiconductor				

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Chapter 1. Solar energy materials, growth methods, solar cells and

status

1.1 Introduction to solar energy

All the energy sources on Earth originate from the Sun. Coal, oil and natural gas are old deposited energy sources and non-renewable. Energy sources such as photovoltaics, solar thermal, wind, hydro, geo thermal, biogas etc, are all current forms of renewable energy sources. To live in a sustainable way, it is important to consume the current energy sources rather than tapping in to the old deposited energy. These non-renewable energy sources are diminishing while causing some environmental damages. Meanwhile renewable energies are increasing their market share with some innovative approaches and technical breakthroughs. Among them solar power has achieved more than 30% growth per year [1] over the past decade. Interestingly, the use of photovoltaic modules to convert the Sun's energy directly to electricity has been growing at even faster rate, \sim 40% [2].

Ultraviolet (UV), visible and infrared (IR) are the main components of the sunlight which land on the surface of the Earth. Figure 1.1 shows the intensity of photons as a function of wavelength for the solar spectrum reaching the surface of the Earth and UV, visible and IR parts of the solar energy.

The total power of all the photons falling on any location at any given time in a unit area is called the incident irradiance [3]. The irradiance is measured in watts per unit area, Wm^{-2} and it varies according to time of the day and the location on the Earth's surface. Furthermore, seasonal and local weather patterns also have an impact on how much solar irradiance reach different locations on the Earth. The theories and calculations of irradiance are detailed in several textbooks [3,4]. The highest spectral irradiance on Earth is labelled as air mass 0 (AM0 = 1366 Wm⁻²) which is received at the upper atmosphere and AM1.5 on the surface of Earth, as shown in Figure 1.1. After various types of reflections and absorptions in the air atmosphere, the average solar

energy falling on the Earth's surface at sea level is generally taken as AM1.5. This is about 1 kWm⁻² (100 mWcm⁻²) and it is a large amount of energy, which is only now beginning to be harvested in really useful quantities.





Solar power is the most abundant and wide spread energy source in the world, the map in Figure 1.2 shows the global spread of annual sum of direct solar irradiance. Solar energy is effectively harvested in several ways: solar thermal power collected from flat plates and vacuum tubes, which is used for building and water heating. There is also concentrated solar thermal power, which is converted to electricity at commercial levels through innovative use of energy cycles [6]. Direct conversion of energy of photons from the Sun to electricity is called photovoltaics (PV). Using PV, once the energy is in the form of electricity, how it is used is a matter of personal choice. This thesis concentrates on how to harvest the power of the Sun more effectively and the ways to make photovoltaic solar cells more affordable.



Clear sky insolation incident, horizontal surface (kWh/m²/day)

7.5

2

ĉ

Figure 1.2: Global spread of annual sum of direct solar irradiance [7].

Photovoltaic solar cells 1.2

Edmond Becquerel first reported the effect of light turning into electricity in 1839. It was not until around 1920 that Einstein and Millikan explained and demonstrated the photoelectric effect [8]. By the mid 1950s [9], despite their high costs space programmes started deploying photovoltaic powered satellites due to their reliability. The oil crisis in the 1970 was the real catalyst for solar cells to be manufactured commercially for terrestrial applications.

Initial solar cells were made of high purity semiconducting materials [10]. The research started towards making silicon based solar cells after improvements in making high purity Si wafers for semiconductors by Czochralski method [11]. This availability of high purity Si made solar cells based on Si claim about 99% of the share of the world PV usage at the turn of the century, and this share is currently 80% [2]. During the last decade the world has seen solar cells made from other materials for terrestrial applications [12], especially solar panels made from cadmium telluride (CdTe) which has ~10% of the world production currently. First Solar in the USA, who only makes

CdTe based solar modules, was the largest producer of solar modules in 2011 [13]. To compare various types of solar modules with different conversion efficiencies, the convention of production cost per unit of converted power is used, %. The cost of CdTe solar modules remains the industrial benchmark for producing the cheapest PV modules at 0.75/W. Furthermore, the efficiencies of solar cells made from Si and other high purity semiconductors are difficult to improve further as the technologies have fully matured over the past 70 years, and they are approaching their theoretical limits [12]. Nevertheless, other novel designs from new optical materials have an opportunity to drive the costs down further while increasing efficiencies. Figure 1.3 shows the evolution of the cost of solar cells from earlier designs, 1^{st} generation single crystal solar cells, thin film solar cells of 2^{nd} generation, and to the latest designs with the potential to reduce the cost drastically (3^{rd} generation solar cells).





Materials with direct optical bandgap and high absorption coefficients are utilised in 2^{nd} and 3^{rd} generations of solar cells. The material layers are becoming so thin, down to the nano meter (nm) range as compared to the earlier designs consisting of ~400 µm layers [3]. Incredible economies of scale have been achieved over the last few decades, but there are limitations to achieve further using the existing technologies. Therefore, the efficiency improvements have to come from new solar cell designs, i.e., graded bandgap solar cells, multi-junction solar cells [14] and organic solar cells. The cost reductions

can be achieved from production methods such as, electrodeposition and screenprinting, which have a low use of input energy, faster throughput and less usage of materials.

The first two generations of solar cells present limitations in progress as a single device. Hence, tandem solar cells, multi-layer graded bandgap solar cells and multi-junctions device structures (Figure 1.4), are being developed to enhance the output.



Figure 1.4: Multi-layer graded bandgap solar cell which can improve the absorption of photons from the sunlight [15].

Multi-junction, *third generation* solar cells have a theoretical conversion efficiency of ~63% [16], with a large number of layers. Currently, an efficiency of ~30% for two junctions and ~33% for three junctions in solar cells have been achieved [12]. A solar cell with multi-layers, absorbing different parts of the solar spectrum (Figure 1.4) has several advantages over the 1st and 2nd generation solar cells due to the better harvesting of photons.

Publication by Shockley and Queisser [17], which is considered by many as a leading paper on solar cell efficiency, mentioned the upper efficiency limit of a p-n junction Si solar cell being 30% based on their theoretical calculations. Despite the fact that the Shockley and Queisser limit is only valid for p-n junction solar cells it is being applied to many other solar cell structures.

1.3 Solar energy materials and theory

All the materials in the world are classified in to, insulators, semiconductors and conductors based on their electrical conductivity (σ) or their energy bandgap (E_g). Conductors have no energy gap between the conduction and valence bands, this makes it possible electrons to move easily from the valence band to the conduction band on the application of an electric field at room temperature. Insulators have a much larger gap between the conduction and valence bands, so electrons cannot be transferred from the valence band to the conduction under the normal operating conditions. However, in semiconductors the energy bandgap between the valence and conduction bands are smaller than that of insulators (0.40 – 4.00 eV). Even though at room temperatures semiconductors act as insulators, with some excitation of electrons, they will leap from the valence band to the conduction band. Thus at room temperatures under an applied electric field some conduction can be obtained.

Depending on the doping and the electrical conductivity, semiconductors can be divided in to intrinsic (i-type), p-type and n-type as shown in Figure 1.5.



Figure 1.5: Different types of semiconductors, indicating the positions of the Fermi level (E_F), the conduction band (E_c) and the valence band (E_v).

Materials with direct bandgap and indirect bandgap are shown in Figure 1.6. Good optical direct bandgap materials have the minimum of the conduction band of a semiconductor at the same momentum level as the maximum of the valence band. Electrons therefore need only to overcome a smaller energy barrier in order to move into the conduction band. In the case of indirect bandgap semiconductors, the electrons have to overcome both the energy difference and momentum difference in order to enter

the conduction band. Materials, which absorb photons include, direct bandgap and indirect bandgap optical materials, polymers and nano-particles.



Figure 1.6: Main features of (a) direct and (b) in-direct bandgap transitions in semiconductors.

Materials in the semiconductor family are further divided into elemental, III-V, II-VI, ternary and quaternary semiconductors as listed in Table 1.1. Si, Ge and C are elemental semiconductors from group IV of the Periodic Table and all the other semiconductors are compounds of more than one element from different groups.

I	`ał	ble	1.	1:	Sem	icond	luctor	s ava	aila	abl	le	for	use	in	sol	lar	cell	s and	l ot	her	electric	cal	device	es.

Classes of semiconductors	Semiconductors
Elemental semiconductors	Si, Ge, C
III-V semiconductors	GaAs, GaN, GaP, InAs, InN, InP, InSb
II-VI semiconductors	CdTe, CdS, ZnS, CdSe, ZnO, ZnTe, ZnSe
Ternary semiconductors	copper indium selenide (CIS), CdSSe, CdSTe,
	CdZnTe, InGaAs
Quaternary semiconductors	copper indium gallium selenide (CIGS), copper
•	zinc tin sulphide (CZTS)

Some properties of II-VI semiconductors, such as optical bandgap, electrical conductivity type and the transmission type, are listed in Table 1.2. Knowing these properties of semiconductors is essential before designing solar cell devices.

Semiconductor	Bandgap	Photon	Electrical	Direct or
· · · ·	(eV) at	absorption edge	conductivity type	indirect Eg
• • •	room Temp.	(nm)	and a second	
CdS	2.42	504	n	Direct
CdSe	1.70	730	n	Direct
CdTe	1.45	850	p, i, n	Direct
ZnO	3.30	376	p, i, n	Direct
ZnS	3.68	335	p, i, n	Direct
ZnSe	2.82	440	p, i, n	Direct
ZnTe	2.26	548	р	Direct

Table 1.2: Some selected properties of semiconductors useful in PV device development at Sheffield Hallam energy group [4,14].

When two semiconductors with different electron affinities are brought together, band bending takes place due to the lining of the Fermi level. An electric field is formed due to the creation of potential barrier height (φ_b). The creation of electron hole pairs (EHP) takes place due to the absorption of photons with energies greater than the bandgap of the material. EHPs should be effectively separated before their recombination and passed to an external circuit.

In summary, an optimised solar cell device will absorb a wider part of the solar spectrum, create as many electron-hole pairs as possible, while minimising recombination of the generated EHPs before passing the electrons and holes to the external circuit.

Such an optimised solar cell device will have a higher φ_b , high shunt resistant (R_{sh}), low series resistant (R_s), and very low detrimental material defects with a good depletion region (W) due to having an ideal doping level of ~10¹⁵ cm⁻³ [14]. If the doping concentration is too high, tunnelling can happen and if it is too low, the electric field will be weak, leading to zero or low photocurrent. Ways to improve the device performance in practice will be discussed later in this chapter. A simplified solar cell can be considered as a current source as shown in Figure 1.7.

The materials for fabricating 2^{nd} generation thin film solar cells are manufactured by various production methods. These are discussed in the next section.



Figure 1.7: The equivalent circuit of an ideal solar cell [18].

1.4 Growth techniques of thin film solar cell materials

The growth of thin film layers can broadly be divided into two classifications as listed in detail in Table 1.3. These are physical methods and chemical methods. Furthermore, physical methods are subdivided in to vacuum evaporation and sputtering methods and chemical growth methods can be divided into gas and liquid phase methods for convenience. Electrodeposition method belongs to the latter and it is discussed in detail in section 1.4.1

Physical growth methods such as molecular beam epitaxy (MBE), laser evaporation, also known as laser ablation, closed space sublimation (CSS) and several other high temperature and vacuum methods can be classified as vacuum evaporation techniques. These methods are ideal for depositing single crystal layers (epitaxial) in the nano or micrometer range of thickness and they are not suitable for large area deposition. Their high precision and control with several hi-tech sensors make these systems very expensive. In practice, the thin films are deposited on crystalline substrates for better results. The other physical deposition method, sputtering, has several variations but mainly employs magnetrons to create strong electric and magnetic fields. The quality of the deposited films can be controlled with a high degree of precision by an expert in the field of electrodeposition. This technique is also more suitable for small area deposition. All the physical growth methods are also good for testing out new solar cell architectures.

Table 1.3: A summarised classification and a listing of thin film deposition techniques[19].

Thin film deposition techniques								
Physical	methods	Chemical methods						
Vacuum evaporation	Sputtering	Gas phase	Liquid phase					
Resistive heating	Glow discharge DC sputtering	Chemical vapour deposition	Electrodeposition					
Molecular beam	Triode sputtering	Laser chemical vapour deposition	deposition (CBD)					
Laser evaporation	Radio frequency	Photochemical vapour deposition	adsorption and reaction (SILAR)					
Arc evaporation	(RF) sputtering	Plasma enhanced	Electroless deposition					
Radio frequency (RF) heating	sputtering	deposition (PECVD)	Anodisation					
Closed space sublimation (CSS)	Face target sputtering	Organochemical vapour deposition	Spray pyrolysis Liquid phase epitaxy					
	Ion beam sputtering Ac sputtering		Sol-gel process					

Gas phase methods such as chemical vapour deposition, metal organic chemical vapour deposition (MOCVD) or metal organic vapour phase epitaxy (MOVPE) are also suitable for epitaxial growth, but the preferred substrate are crystalline materials. These methods are well established in the industry with dozens of manufacturers producing these complicated machines. Liquid phase or wet chemical methods are the most economical and they are more suitable for large area deposition. Spray pyrolysis has been used in the glass industry for decades due to its uniformity and low cost. Many substrates can be used with liquid phase growth methods. Spray pyrolysis is mainly used to deposit transparent conducting oxides (TCOs) on glass for the PV industry. For electrodeposition, this glass is coated with fluorine doped tin oxide (FTO) and is used as the substrate. Chemical bath deposition (CBD) is another successful wet chemical method with widespread use due to its simplicity and suitability in producing large area semiconductors.

A comparison of various parameters of typical semiconducting thin film deposition technologies are summarised in Table 1.4.

Method	Cost	Substrate temperature °C	Deposition rate Å/s	Grain size Nm	Scalability
ED	Very low	30 - 300	1 - 30	10 - 1000	Possible
CBD	Low	30 - 100	1 - 40	10 - 200	Possible
CSS	Moderate	300 - 700	10 - 30	10 - 200	Limited
Sputtering	High	~200	1 - 10	~ 10	Possible
PECVD	Very high	200 - 300	10 - 100	10 - 100	Limited
Thermal evaporation	Low	50 - 100	1 - 20	10 - 100	Limited

Table 1.4: Comparison of thin film deposition technologies for semiconductors [19-23].

Advantages of electrodeposition include lower processing temperatures, feasibility to scale up and due being a wet chemical method, low setup and operational costs.

1.4.1 Electrodeposition (ED)

Electrodeposited solar cells present one of the lowest cost routes for the PV industry due to three main reasons; the scalable thin film device architecture, production method has little wastage and low usage of input energy. Furthermore, this production method only requires one production line from the raw chemicals to the solar modules, reducing the start up capital required for industrial production.

This method involves the application of a suitable cathodic potential to a conducting substrate in contact with an electrolyte containing the suitable ions to deposit various semiconducting layers. A DC voltage is applied between the counter electrode (anode) and the substrate (cathode), and the cathodic potential is usually measured relative to a reference electrode. Figure 1.8 shows schematics of two different electrodeposition (ED) configurations.

There are two different versions of electrodeposition set up in use today. These are 3electrode, and 2-electrode configurations (Figure 1.8). Lower temperature aqueous electrolytes and high temperature non-aqueous electrolytes are two further differentiations. While they both have advantages and disadvantages, it is important to select the right procedure for a particular purpose. Many semiconductors are produced by electrodeposition method including II-VI and ternary semiconductors. Advantages of ED include low-cost, scalability, simplicity, the possibility of intrinsic and extrinsic doping, bandgap engineering and built in hydrogen passivation. While the advantages outweigh the disadvantages, there are some disadvantages of ED during the deposition of semiconductors. Impurity atoms such as Na and K can be infused to the material layers, which can create detrimental defect centres if the deposition potential of its ions happens to match with that of the semiconducting materials being deposited. Before the solar cells are fabricated from these layers, electrodeposited semiconducting layers must be annealed to ~400°C, otherwise the PV device parameters could be lower. However, this still has a lower use of energy compared to other deposition methods. Most of the deposited materials are amorphous or polycrystalline. Nevertheless, electrodeposition of crystalline materials has been reported [24].



Figure 1.8: Schematics of electrodeposition set-up for 2 and 3 electrode systems [25].

In this research, this method of production of semiconductors will be investigated to produce CdS and ZnS from novel routes. These semiconductors will be used to fabricate all-electrodeposited solar cells while avoiding the use of Na, which is detrimental to CdTe solar cells. The main objectives are to fabricate low cost, all-ED CdTe based solar cells while investigating the possibilities to enhance the efficiencies.

1.4.1.1 Theory of electrodeposition

Electrodeposition from ionic species, from an electrolyte on a conducting surface occurs sequentially. These sequences include ionic transport and discharge, breaking of ionligand bond and finally the deposition of atoms on to the substrate by nucleation. Now the systematic discharges of ions lead to the formation of deposits on the conducting surface. These electrodeposition steps, dictate the phase of the materials deposited, and determine whether it is crystalline, polycrystalline or amorphous.

Once all the controlling parameters are at their optimum values, and when a cathodic potential is applied, a thin film of semiconductor is electrodeposited on the cathode. Growth voltage, concentration of precursor elements, pH value of the electrolyte, growth temperature, stirring rate, electrode, and type of substrate used to deposit thin films are all controlling parameters in electrodeposition. A lower pH electrolyte permits the use of a higher deposition current density, to produce varying deposits, at a higher deposition rate [26]. However, at lower deposition current densities discharge of ions occurs more slowly, lowering the growth rate and leading to more closely packed, crystalline phases. After indentifying the optimum conditions and parameters, it is possible to have a high yield and quality from electrodeposition.

Cd and Te in the precursor chemicals undergo several reactions to form CdTe on the substrates. The equations for these reactions are as follows [27]:

1.1

Reduction of Cd;

$$Cd_{(aq)}^{2+} + 2\overline{e} \rightarrow Cd_{(s)}$$

Reduction of Te;

$$HTeO_{2(aq)}^{+} + 3H_{(aq)}^{+} + 4\overline{e} \rightarrow Te_{(s)} + 2H_2O$$
 1.2

Formation of CdTe happens as;

$$Cd_{(s)} + Te_{(s)} \rightarrow CdTe_{(s)}$$
 1.3

Then the overall cathodic reaction is;

$$Cd_{(aq)}^{2+} + HTeO_{2(aq)}^{+} + 3H_{(aq)}^{+} + 6\overline{e} \rightarrow CdTe_{(s)} + 2H_2O \qquad 1.4$$

1.4.1.2 2-electrode and 3-electrode methods

Traditionally the three-electrode method is used for electrodeposition but there are several groups who confidently use a simpler two-electrode method, which still gives good control of the important electrodeposition parameters [14]. The 3-electrode

electrodeposition method has several advantages over 2-electrode electrodeposition and vice versa. The 3-electrode deposition system has shown more stable growth current density while the 2-electrode system offers a more simplified solution to reduce unnecessary ions in the electrolyte. During this research, one is expected to gain the confidence and the understanding of electrodeposition with both methods. A schematic of the two systems are shown in Figure 1.8. Reference electrodes such as Ag/AgCl and Hg/HgCl have been used in research and industry.

1.4.1.3 Aqueous and non-aqueous electrodeposition

The use of a non-aqueous electrolyte has one main advantage, the system can operate at higher temperatures [28], which is helpful for the growth of more structured semiconductors such as polycrystalline and crystalline materials [29].

A less toxic or non-toxic aqueous electrodeposition has the advantage of lower energy consumption during the fabrication of solar cells. The use of water as the electrolyte solution also gives more control over the impurities and lowers the cost further due to less stringent environmental and recycling issues [25].

While the use of aqueous electrodeposition is advantageous on cost and other environmental aspects, it limits the use of high temperature, which tends to produce better crystalline materials. For example, molten salt-based electrodeposition of Si, ethylene glycol based systems and several other high temperature electrodeposition methods have been experimented [24].

1.5 Solar cells from semiconductors

1.5.1 p-n junction solar cells

p-n junction solar cells are fabricated as homo junctions or hetero junctions. In a homo junction solar cell, layers from the same material with the same bandgap but different electrical conductivity are used. Whereas in a hetero junction solar cell, layers from different materials with different bandgaps and doping concentrations or different electrical conductivity are utilised. Depending on the conductivity of these

semiconducting materials, further device designs have been used by researchers and in the industry.

In any solar cell design when solar photons with energy (hf) greater than the energy bandgap of the semiconductor (E_g) fall on the absorber material of the device, the photons get absorbed and bonds between atoms are broken creating electron-hole pairs (EHP). In this process electrons move towards the conduction band and the holes remain in the valence band. These charge carriers then flow towards the electrical contacts due to the existing electric field in the depletion region created by band bending within a p-n junction.

A solar cell can be fabricated in superstrate or substrate structure as shown in Figure 1.9. The basic difference is where the solar irradiance enters into the device. In a superstrate design, the sunlight enters from the glass side, it is unshaded and the back electrical contact is fabricated after all the semiconducting layers are deposited. In the substrate configuration, the sunlight enters from the opposite side to the glass, and the front electrical contact is fabricated after all the semiconducting layers are fabricated. To reduce the shading of sunlight, the front contact is fabricated in a grid type design.



Figure 1.9: (a) Superstrate and (b) substrate configurations of thin film solar cells [14].

Substrate configuration is the most basic type of solar cell in use today. Initially the III-V family of solar cells and Si based solar cells were designed on this structure. When ptype and n-type semiconductors are brought to contact, the Fermi levels of the semiconductors line up, hence the development of barrier height leading to the creation of internal electrical field happens. The main advantage is the band bending which creates a good potential barrier height. The function of a p-n homo junction solar cell and its energy band diagrams are shown in Figure 1.10 [14]



Figure 1.10: Energy band diagram of a p-n homo junction formation [14].

In a homo p-n junction solar cell, the two sides of the junction have the same bandgap ie., layers absorb the same part of solar spectrum. Therefore, there is no extra absorption of photons. At a p-n junction, the current is mainly due to four components, electron diffusion and drift, and hole diffusion and drift. The forward current is mainly due to the diffusion of excess minority carriers. The reverse current is mainly due to three reasons, electron-hole pair generation in the space charge region, diffusion of minority carriers and surface leakage current.

1.5.2 p-i-n (or n-i-p) junction solar cells

This structure is very similar to the p-n junction with the inclusion of an intrinsic (itype) semiconductor. The thickness of the i-type layer can be changed to control the width of the depletion region and to force band bending. Typically, amorphous Si solar cells have a p-i-n structure. Graded bandgap devices and tandem solar cells can be manufactured to any one of these two designs as it depends from which side the light enters the solar cell.

1.5.3 Schottky barrier (or metal-semiconductor) solar cells

When a metal layer is deposited on a semiconductor, an ohmic contact or a rectifying contact is formed. This depends on the work functions of the two materials. When an n-type semiconductor forms an interface with a metal of high work function (ϕ_m) , a Schottky barrier is formed at the metal-semiconductor interface. An ideal description of a Schottky barrier formation is depicted in Figure 1.11. If the semiconductor is p-type, a low ϕ_m metal forms a Schottky barrier, to prevent or reduce the flow of holes, (Figure 1.12). A complete description of Schottky barriers can be found in a comprehensive textbook by Rhoderick and Williams [30].



Figure 1.11: Schottky barrier formation when an ideal interface is formed between an n-type semiconductor and a high work function metal [14].



Figure 1.12: Schottky barrier formation between a p-type semiconductor and low work function metal with an ideal interface [14].

This junction can be severely affected by semiconductor defects, surface and interface states. One of the main advantages of using majority carrier n-type semiconductors is high electron density and mobility. This is because electrons are the majority carriers in an n-type semiconductor. Another issue is that at the metal-semiconductor interface Fermi level pining has been identified. Five experimentally observed Fermi level pining positions have been reported for a metal/n-CdTe interface [31]. In order to obtain higher barrier heights the conditions required to pin the Fermi level as close as possible to the valence band are being researched at present.



Figure 1.13: Experimentally observed Fermi level pining positions of a metal/*n*-CdTe interface [31].

1.5.4 Graded bandgap multi-layer solar cells

The multi-layer graded bandgap design enhances energy output by absorbing a wider range of the solar spectrum. This can be achieved by starting from wide bandgap p^+ or n^+ doped material, and gradually changing to narrow bandgap n^+ or p^+ doped materials respectively. A device fabricated with wide bandgap p^+ doped material with a gradual change to narrow bandgap n^+ doped materials was tested and the results confirmed the functioning of the device in complete darkness [32], absorbing IR radiation, and combining impact ionisation and the impurity photovoltaic effect. Optical

semiconductors with narrow bandgaps can absorb beyond the visible spectrum and more towards the IR range increasing the intake of photons. Figure 1.14 shows the band diagram of a multi-layer graded bandgap device.



Figure 1.14: Multi-layer graded bandgap diagram with capability of absorbing photons from the IR region [14].

1.6 Si based solar cells

Si is mainly fabricated in industry using two methods. These are the Czochralski (CZ) method and float-zone method. Both methods are energy intensive, making them high in cost [18]. However, due to the thorough understanding of this long researched material, high purity Si is manufactured. Si ingots with diameters larger than 15 cm are not possible to be grown economically for solar cells. This makes the manufacture of large area high purity Si based solar cells not viable. Three different solar cells from Si exist in the world today. These are crystalline Si or mono Si (c-Si), polycrystalline Si or multi Si (p-Si) and amorphous Si (a-Si). Almost all Si solar cells utilise an anti reflective coating to optimise the absorption of solar spectrum [33].

The production of semiconducting grade silicon (Si) is very well researched and many solar cell manufacturers of Si-based solar cells utilise the Si produced by the Czochralski method. It involves melting polysilicon in a crucible at 1414°C, while pulling a high purity Si seed away from the melt to create the ingots of typically ~15 cm diameter. This method is very well known and extensively documented in several textbooks [34]. Once ingots are doped appropriately to produce n-type and p-type silicon, and sliced and polished to produce wafers, they are ready for the manufacture of

solar cells. The average thickness of a Si wafer used in solar cells is from 200 μ m to 1 mm. Two main issues need to be addressed to reduce the cost of Si; i) to minimise the cost of Si during the growing and slicing process and ii) reduce the contaminations from the crucible [35,36].

1.6.1 Crystalline silicon solar cells (c-Si)

c-Si have the highest laboratory efficiency of 25.5% [4,37], and the highest module effficiency of just over 21%, and there is very little space for this efficiency level to improve. This mainly due to the theoretical limit for a single junction solar cell is about 27% [3].

While cost reductions from Si based solar cells is also limited, due to the high cost of feed stock [38], still volume related cost reductions are possible. The most pure form of silicon is used to produce c-Si solar cells making it more expensive than other forms of Si based solar cells.

1.6.2 Polycrystalline silicon solar cells (p-Si)

Polycrystalline Si semiconductors (p-Si), with an indirect bandgap are used to produce slightly cheaper and lower efficiency solar cells than c-Si solar cells. The efficiency of p-Si is about 21% [39] in lab scale devices and 18% at the module level and the global market leader. p-Si wafers are manufactured by a casting process, with contamination from casting is still an issue [35].

1.6.3 Amorphous silicon solar cells (a-Si)

Amorphous Si (a-Si) is a thin film direct bandgap semiconductor [40], and is made from randomly orientated Si, which has low manufacturing costs. a-Si thin films are mostly fabricated by sputtering, glow discharge, or PECVD deposition [40]. It can be doped for n-type and p-type electrical conduction similar to other Si semiconductors. Production methods for a-Si solar cells have become very advanced, including the fabrication of triple junction and spectrum splitting device structures [41]. It is manufactured mainly
on glass or stainless steel, but research is taking place to use a flexible substrate for a-Si solar cells [42].

The Staebler-Wronski effect (SWE) seriously impedes the performance after 1000 hours of exposure to light. This is due to the presence of weak hydrogen dangling bonds [41]. Due to the SW effect, there is a 10 - 30% drop in performance for single junction devices and 10 - 15% drop for multi-junction devices [43].

1.7 Other PV cells

Si, CIGS and CdTe based solar cell research is mostly driven by terrestrial applications and the main research objective is to reduce \$/W figure by moderate gains in efficiency. However, in high efficiency solar cells from the III-V family, the objective is to achieve higher conversion efficiencies, as their main application has traditionally been for use in space. Recently, searches in reducing the cost of power from concentrated PV generation have added the impetus for high efficiency solar cells to be manufactured for large-scale terrestrial applications. This has triggered another research drive on these high specification solar cells.

1.7.1 III-V Solar cells (GaAs, AlGaAs and GaN)

Compounds made out of elements from groups III and V of the periodic table are used in this type of solar cells. They were first developed several decades ago and since then they have become a fully matured research area. High purity materials, produced by complicated apparatus such as MBE and MOCVD, lead to a high cost of manufacturing. These solar cells have excellent conversion efficiencies, with multi-junction cells approaching ~43.5% efficiency [39]. The III-V family has a high degree of lattice matching and an anti reflection coating is always built in to these expensive solar cells [41].

1.7.2 CIGS (CuInGaSe₂) solar cells

Copper indium gallium diselenide (CIGS) material has a bandgap between 1.00 eV (pure copper indium diselenide) and 1.70 eV (pure copper gallium diselenide)

depending on indium and gallium percentages. These solar cells are mostly fabricated on cost-effective soda lime glass. A typical structure is shown in Figure 1.15. This type of thin film solar cell has been researched and scaled up with excellent laboratory level and module scale efficiencies of 20% and 14% respectively [44]. This device has the potential to achieve a wider usage in applications as it is also manufactured on flexible substrates with 18.7% efficiency [45]. For several decades, the research was based on the band diagram shown in Figure 1.16. However, with a new understanding of CIGS solar cells, new band diagrams were proposed by Dharmadasa in 2009 [46] and they are thoroughly discussed in a recent textbook [14]. These proposals make many new and improved research directions to further develop this device. Recently a flexible substrate was used to produce a printed CIGS solar cell, opening further research directions [45].







Figure 1.16: The frequently referred energy band diagram of CIGS solar cell [12].



Figure 1.17: One of the improved energy band diagrams to explain PV actions of CIGS thin film solar cells [14].

1.7.3 Dye sensitised solar cells (DSSC)



Figure 1.18: Schematic illustration of the various components in a Dye Sensitized Solar Cell [47].

Dye sensitised solar cells (DSSC) were introduced in the 1990s [48] and have a huge potential for commercial penetration due to their low material cost and cheaper production methods. DSSC is a hybrid device with organic and inorganic dyes, and classed as a 3rd generation solar cell which mimics the photosynthesis process of plants. This process explores several new concepts such as new naturally available materials, nanotechnology and molecular devices. Currently, device efficiencies are 11% and 7% for laboratory cells and modules respectively [49].

The degradation issue of solar cells due to the use of porous and wide bandgap materials, and natural dyes is under intense research at the moment. A primary material used in this solar cell is TiO_2 nano-crystals, an expensive, rare earth material and its replacement has not been successful so far [50,51]. However, in, 2012, in experiments at several research groups with the inclusion of a 2-directional high electrical resistivity material, graphene with TiO_2 produced large increases in current density indicating another research direction [52,53].

1.7.4 Organic photovoltaic (OPV) cells

Organic or molecular semiconductors are used to fabricate organic photovoltaic (OPV) cells. OPV cells imitate the nature to photosynthesis solar photons to produce electrical

energy. They have low conversion efficiencies and very low-cost to produce. The general working principle of OPV cell is in four consecutive steps. They are light absorption, exciton dissociation, charge transport, and charge collection [54]. In organic solar cells, the energy band is presented in terms of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). Here the valence band is analogous to HOMO in a molecule, whereas the conduction band is the solid-state analogue of the LUMO as compared in Figure 1.19.

Research is ongoing to increase the efficiency by reducing the charge recombinations with the use of polymers with high charge carrier motilities such as poly(3-hexylthiophene) and poly(3,4-ethylenedioxythiophene) [54]. These organic molecules can achieve chemical tailoring to alter their properties, i.e., bandgap. Recently manufacturing of OPV by role-to-role method was also demonstrated [55]. This was due to the improvements in ink-jet printing and other printing techniques leading to low-cost fabrication of large-area semiconductors. Furthermore, OPV can also be fabricated on flexible substrate for more specific applications [56].

Yet, OPV cells have several major issues to overcome apart from their low efficiency. They degrade once exposed to oxygen or water and hence despite the encapsulation the lifetime of these solar cells is limited to 7 - 10 years [57]. The heterojunction solar cell is currently considered as the most promising approach by researchers among many different organic solar cell structures. Advancements achieved since the inclusion of an inverted bulk heterojunction have increased the conversion efficiencies several folds to 10.7% and 6.8% on the laboratory level and module level respectively [49].



Figure 1.19: A comparison of inorganic semiconductors and organic semiconductors (molecular semiconductors) [58].



Figure 1.20: Cross sectional schematic of an OPV cell with an optimised bulk heterojunction. The inverted donor-acceptor interface forming the bulk heterojunction is sandwiched in between the electrodes [59].

1.7.5 CdTe based solar cells

Cadmium Telluride (CdTe) semiconductors have a direct bandgap of 1.45 eV [60]. Along with another II-VI family direct bandgap semiconductor, cadmium sulphide (CdS), CdTe is used to produce thin film solar cells. CdS has a bandgap of 2.42 eV [61] and is used as a window layer, and the CdTe acts as the absorber layer. A structure of typical CdTe based solar cell in a superstrate configuration is shown in Figure 1.21.

Direct bandgap materials have a higher coefficient of absorption hence, about 1.5 μ m of CdTe is adequate to absorb about 99% of the solar spectrum, in turn these solar cells consist of considerably less material. About 1.5 μ m of CdTe absorbs the same photons as absorbed by ~200 μ m of c-Si layer, as c-Si is an indirect bandgap material.

There is some concern with the usage of Cd in solar cells. Cd metal is a by product of copper and zinc production, and there is a production of about 26,000 tonnes of Cd annually [62]. One Ni-Cd battery uses 7 g of Cd, and an 80 W solar panel from First Solar Inc, uses 10 g of Cd. Once Cd is used in a solar panel, that amount of Cd is locked away in the panel for 20 - 30 years. This is the most productive way of using this surplus of Cd, to avoid deterioration of environment due to cadmium. First Solar has recently announced a total life cycle recycling programme for CdTe solar panels [63], the first such recycling programme of rare Earth materials. Furthermore, CdS and CdTe are both highly stable materials with melting points of more than 1000°C [64]. All these factors indicate that with the right precautions the issue of Cd can be mitigated.



Figure 1.21: The structure of commonly used CdTe based solar cell on glass [14].

1.7.5.1 Development of CdTe based solar cells

Until about a decade ago CdTe based solar cells were limited to the laboratories. Today CdTe solar cell market share has gained an impressive 10% of all the PV modules sold in the world [39]. Worldwide market analysts, researchers, and corporations have high

ambitions, for solar cells made from CdTe [12]. In 1993, Ferekides reported 15.8% [65] efficiency and the progress of CdTe based solar cells was improved to 16.5% by Wu in 2001 [66]. Since 1993 the progress in efficiency of CdTe based solar cell has been really slow, has only managed to reach an efficiency of 17.3% in 2011 by First Solar [63]. But at the end of 2012 18.3% by GE Global research labs and early 2013 18.7% by First Solar further improvements were recorded [49,67].

Most of the research groups discuss CdTe solar cells based on the band structure and diagram of Basol, i.e., glass/TCO/n-CdS/p-CdTe/Metal structure [68]. Normally FTO is used as the TCO, which has about 90% transparency. The CdS layer always provides the n-type window layer. To produce CdS, CBD is frequently used as well as sputtering, vacuum evaporation and electrodeposition. The thickness of the CdS layer used is around ~80 nm. The absorber layer, CdTe has been fabricated on a large scale by sputtering, CSS, screen printing methods and electrodeposition.

A recent understanding based on experimental knowledge has suggested that CdTe based solar cells can be an n-n junction with a large Schottky barrier [31]. Since some of the experimental steps were conducted on the basis of p-CdTe, this might have been a factor impeding the efficiency progress of CdTe solar cells. Furthermore, five experimentally observed discreet Fermi level pining positions have been reported [31], which has led to a better understanding of this device. In semiconductor-metal junctions, surface states dominate the device performance, unlike in a p-n where the junction is secured at the semiconductor interface.



Figure 1.22: Energy bandgap diagram of the CdS/CdTe solar cell as proposed by Basol based on a simple p-n junction [68].

Efforts to reduce the number of defects while producing CdTe with low series resistance are being carried out by various research groups. An increase of shunt resistant and finding a better PV active partner for CdTe, as there are some reports questioning the PV activity of CdS.



Figure 1.23: New band diagram proposed by Dharmadasa for CdS/CdTe solar cell highlighting more complex nature of this device [69].

1.7.5.2 Potential of CdTe based solar cells

The highest theoretical efficiency possible for CdTe solar cells is about 27.5% [3], but only over a half of this has been achieved so far on module level, indicating the potential room for improvements.

Once all the defect issues are identified, recombination centres or killer centres are nullified, CdTe based solar cells can deliver even more cost effective solar cells. Detrimental issues are now identified and confirmed. CdS is not a highly PV active material and providing a pinhole plugging layer, (PPL) between CdTe and the back contact metal will improve the performance of this structure even further. Some of these issues are addressed in this thesis. Furthermore, cost reductions can be achieved if all the semiconductor layers are produced by one method for example electrodeposition. So all electrodeposited CdTe solar cells manufactured with a better understanding presents a promising research direction.

1.8 PV status and applications

Before the entry of CdTe solar cells to the commercial arena, the lowest cost of electricity from PV was about \$ 5/W. However, currently it is \$ 0.75/W and \$ 1.50/W from CdTe and Si based solar cells respectively and this trend is shown in Figure 1.24. There is a high potential to reduce the cost of PV further by using solar cells made from low-cost methods such as electrodeposition or screen-printing. Once the use of innovative device structures as discussed in this chapter are fabricated, the cost of PV can be further reduced. The production of solar cells is increasing by 40% annually and output has increased by 100 fold in less than a decade from 277 MWp in 2002 to 27 GWp in 2011 [5]. Many energy analysts are predicting this increasing trend to continue [70].

The sun tracking systems further enhance the capture of solar energy throughout the day by pointing the solar panels to the optimum angle with sunrays [71]. Two tracking systems, dual axis, and single axis are in use today. While they increase the complexity of a solar power system, due to the higher conversion of sunrays to electricity tracking systems are increasingly utilised [72].



Figure 1.24: Reduction of cost of electricity from solar cells [14].

Another useful comparison indicator used by the investors of energy generation is levelized cost of electricity (LCOE), to compare the cost of 1 kWh produced by various methods, such as coal, natural gas, fossil fuel etc, is shown in Figure 1.25. The LCOE of PV is expected to be competitive against the other forms of power sources in the next few years.



Figure 1.25: The trend of LCOE from different power sources [73].

Solar cells are interconnected in series, parallel or in a combination of both to provide practically suitable voltages and currents to the consumer. A large number of applications with DC electricity are used directly from solar panels in off-grid applications. At off-grid levels, PV applications have a higher potential to change the lives of the people in a positive way in a very short time period. For example, under 'Solar Home Systems' programme by Grameen Shakti in Bangladesh one million homes were provided with PV systems improving the standard of living for many [74] and 100,000 remote homes in Mongolia have been provided with electricity within two years, improving their standard of living [75]. Also there is the 'solar village programme' in Sri Lanka which will alleviate poverty and promote sustainable living [76]. For most remote areas, the best option to generate electricity is from solar power.

When the application is grid connected, DC electricity from solar panels is converted to AC electricity through a suitable high efficiency inverter to match the frequency of the electricity grid. 85% of PV power generated in the world now is for grid connected applications [77]. Several large PV power stations by utility companies are being built every year and it is forecasted to increase substantially [77]. The first 1 GWp PV power plant in the world was recently commissioned in relatively low-irradiance Serbia as shown by the map of solar insolation on a horizontal surface over Europe in Figure 1.26 [78]. Furthermore, concentrated PV power stations using high efficiency solar cells

through Fresnel lenses are commercially viable. Two companies are already manufacturing these power plants, which can be assembled in just 2 hours up to a ratings of 75 kWp [72,73]. To enhance the capture of solar irradiance, most high-end solar power applications utilise sun-tracking methods.



Figure 1.26: The solar insolation (kWh/m²/year) on a horizontal surface over Europe [81].

All the indicators mentioned above, \$/W, LCOE, production volume and large utility level generation are indicating a huge growth in power generation by PV cells.

1.9 Aim and objectives of the research

Different deposition technologies for semiconductor material are compared in Table 1.4. It is obvious that electrodeposition offers several advantages such as scalability, low use of energy and raw materials leading to the reduction in costs. Hence, a solar cell production line needs less start up capital.

Therefore, the main aim of this research was to develop solar cells using semiconductor materials produced by electrodeposition method only. This aim can be achieved through the following objectives:

- 1. To produce Na-free CdS as a window layer.
- 2. To utilise a non-toxic ZnS material instead of conventional CdS for solar cell fabrication.
- 3. Produce CdTe absorber layers by simplified 2-electrode method.
- 4. To establish a correlation between electrodeposition growth conditions, quality of the materials and resulted parameters of solar cells.

1.10 References

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Chapter 2. Characterisation methods for solar cell materials and devices, and experimental methodology.

2.1 Introduction

In Chapter 1, the deposition methods for thin film semiconductor layers used in PV cells, the different types of solar cells, and the status of solar energy were discussed. The objectives of this whole research project can be divided into two parts: i) electrodeposition and characterisation of semiconductor grade thin films, and ii) research and development of fully electrodeposited (all-ED) solar cells, where all the semiconducting layers are grown by this method. Electrodeposition of semiconducting thin films was carried out for three buffer/window layers (ZnS, CdS and CdS_(1-x)Se_x) and an absorber layer, CdTe. Several advanced material characterisation methods were utilised in this thin film research and they are outlined in this chapter. In addition, the experimental steps needed for electrodeposition of thin films and fabricate all-ED solar cells are described in detail.

To understand how the semiconductors will function in solar cells, it is important they be fully characterised for their properties. No single method can fully characterise a thin film layer, rather several techniques are used in a complementary way. Full material characterisation steps will help to increase the efficiency of solar cells by improving the reproducibility of the materials and devices.

2.2 Material characterisation methods for thin films

2.2.1 Optical absorption

Optical absorption characterisation is a technique for calculating optical properties such as absorption, reflection, transmission of light and the energy bandgap of materials. The bandgap of the material dictates which part of the solar spectrum the semiconductor absorbs. Since it is a fast and non-destructive method, optical absorption is used as an initial step in the optimisation process of electrodeposited thin film layers. This is a useful technique in identifying the materials grown, since the energy bandgap is a unique material parameter for a semiconductor. A schematic of the optical absorption apparatus is shown in Figure 2.1. The main components of this spectrometer are: i) a suitable white light source, ii) a monochromator which decomposes white light into spectrum, iii) a sample holder to place the specimen and iv) the detector to record how much light is received from the transmitted light.



Figure 2.1: Schematic of optical absorption apparatus showing its four main parts [1].

Absorption spectra were recorded with a Cary 50 UV-VIS spectrophotometer. The optical absorption measurements data was analysed using the Stern relationship [2] as in the equation;

$$\alpha = \frac{k(hv - E_g)^{\frac{n}{2}}}{hv}$$
 2.1

where, α is the absorption coefficient, k is the Sherrer constant (0.94), v is the frequency of the photon, h is the Planck's constant (6.63×10⁻³⁴ Js), E_g is the bandgap and n takes the value of either 1 or 4. The value of n = 1 is for direct transitions and n = 4 is for indirect transitions respectively. For direct bandgap semiconductors such as CdS, ZnS, CdS_(1-x)Se_x and CdTe, the equation (2.1) becomes:

$$\alpha = \frac{k(hv - E_g)^{\frac{1}{2}}}{hv}$$
 2.2

By using $E_g = hv$ and $c = v\lambda$ [2], where, c is the speed of light (2.998×10⁸ ms⁻¹), gives

$$E_g = \frac{1242}{\lambda} \ eV \tag{2.3}$$

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The Tauc plot of $(\alpha hv)^2$ versus hv gives the direct bandgap of the semiconductor under investigation when the straight line portion of the curve is extrapolated to the hv axis [2].

2.2.2 Photoelectrochemical cell

Photoelectrochemical (PEC) cell measurement can be used to determine the electrical conductivity type of thin film semiconducting layers. It is specially suited for thin film layers deposited on conducting substrates. A solid/liquid junction is formed by immersing the glass/FTO/thin film layer in an appropriate electrolyte and the resulting voltage is measured with respect to a counter electrode. The PEC signal is determined by the difference in voltage observed under illumination and under dark conditions. Band bending taking place at the liquid/solid junction; energy band diagrams for p-type and n-type semiconductors are shown in Figure 2.2 below.



Figure 2.2: Energy band diagrams of (a) *p*-type semiconductor and (b) *n*-type semiconductor in a PEC cell arrangement [3].

The sign of the PEC signal indicates the conductivity type of the semiconductor tested. The strength or the magnitude of the signal depends on the quality of the junction, the concentration of the electrolyte, doping concentration of the solid layers and the electrolyte used. The PEC cell test is affected by surface states [4]. Both metallic and intrinsic films show low or zero PEC signals and moderately doped semiconducting layers show a large PEC signal [5]. The PEC cell system was calibrated using well-known semiconductors, n-type CdS and p-type ZnTe. In this study 0.10M (NH₄)₂S₂O₃

was used as the electrolyte solution for the PEC cell measurements. The PEC cell apparatus included a DC power source for the light bulb and a DC voltmeter.

2.2.3 X-Ray diffraction (XRD)

This is a non-destructive characterisation method. Using this method, material characteristics such as, lattice parameters, material structure, crystallite size, residual stress and film thickness can be identified. Since the 1930's, the International Centre for Diffraction Data [6] has collected a huge database of diffraction results of materials which is used to identify the samples under investigation. They are also knows as Joint Committee on Powder Diffraction Standard (JCPDS) data.

The principle behind this method is Bragg's law for X-ray diffraction (eq. 2.4) in crystallography, where λ is the wavelength, *n* is an integer, (the order of the diffraction), θ the angle between the wavevector of the incident plane wave and the lattice planes. Lattice spacing (d) can be calculated using [7].



Figure 2.3: Schematics of X-ray diffractometer showing the primary parts of X-Ray Diffraction technique [8].

XRD experimentation was conducted during this project using a Philips PW 3710 X-ray diffractometer, using CuK_{α} radiation ($\lambda = 1.5416$ Å) with a range of $2\theta = (10 - 70)^{\circ}$ for

the structural analysis of deposited films. The X-ray generator current and tension were 40 mA and 40 kV respectively.

To identify the material, the peak position of data from the XRD experiment can be compared to JCPDS data sheets. Furthermore, grain size can be calculated from the Full Width at Half Maximum (FWHM), Bragg angle, θ , and the wavelength of the x-rays, (λ = 1.5416 Å) as follows;

$$D = \frac{k\lambda}{\beta cos\theta}$$
 2.5

where, β is the FWHM of the peak corrected for instrumental broadening and k is the Scherrer constant taken as 0.94.

2.2.4 X-ray fluorescence (XRF)

X-ray fluorescence is a spectroscopic technique used to determine the elemental make up of solids. The specimen to be analysed is bombarded with high energy X-rays. The diffraction patterns of X-rays emitted due to the impact of X-rays on atoms are directed through slits to an analysing crystal. These diffracted photons with varying wavelengths are collected by the analysing crystal and then passed to the detector. A computer connected to the detector decodes the signals to match the atomic percentages from the database to the sample under investigation [9]. XRF can detect full elemental analysis from parts per billion. This technique is highly used in industry and research alike as it can be used quantitatively and qualitatively.

2.2.5 Scanning electron microscopy (SEM)

SEM is operated in a vacuum chamber to prevent scattering and absorption of electrons. It uses a high-energy (up to 40 keV) monochromatic electron beam. The beam is passed through a series of apertures, and coils before its interaction with the specimen as shown in Figure 2.4. Once the electron beam interacts with the atoms on the surface of the sample, the resulting emitted electrons are recorded by the detector. The information from the recorded electrons contains data about the sample, such as topography and grain size. These are then converted into useful information with the help of the database linked to the computer. SEM images of sample cross sections are produced to estimate the film thickness of the layers tested. The samples should be electrically conductive prior to placing on the sample stage.



Figure 2.4: A schematic of key components of the scanning electron microscope [8].

This is somewhat a destructive method due to the penetration of electrons ~ 5 nm deep into the material layer from the continuous bombardment of the high energy electron beam on the surface.

A NOVA NANO SEM 200 Field Emission Gun with an accelerating voltage of 20 kV was used to study the surface morphology of the thin film layers. The samples were prepared to be about 1 cm² and thoroughly cleaned before investigation.

2.2.6 Energy-dispersive X-ray (EDX) analysis

The elemental composition for a qualitative assessment is recorded from an energy dispersive X-ray spectroscopy gun fitted inside SEM equipment. This contains an X-ray detector which collects the X-rays emitted from the high energy electron bombardment of the SEM setup. Therefore, EDX is conducted simply by utilising a separate detector once a sample is loaded in to the depressurised chamber.

2.2.7 Atomic force microscopy (AFM)

The main components of a typical AFM are shown in Figure 2.5. The sample is loaded to the actuator, and once the cantilever tip approaches the surface near enough the Van der Waal forces cause the tip to deflect [10]. The position sensitive photodiode detector for the laser light, which is reflected on to the back surface of the cantilever, records the variations of the tip and a computer linked to the unit then converts them to meaningful data. As the tip travels along the surface of the sample during the scanning, further readings can be studied from the surface variations, for example the stresses and strains on the sample surface.



Figure 2.5: Schematic of a typical AFM instrument showing its main features [11].

AFM is mainly used for the characterisation of surface roughness and texture (topography). This advanced characterisation method can also be used to calculate the nano-size crystallites and residual stress of the surfaces tested.

To prevent images getting distorted, this apparatus should be free from vibrations and interferences, but unlike SEM, AFM does not require a vacuum chamber. There are 3 main modes when using AFM, contact mode, non-contact mode and tapping mode. Depending on the surface roughness of the sample, the correct choice of operating mode should be selected earlier in the experiment to prevent damages to the tip.

AFM measurements were conducted on a Nano Scope3 set on contact, and tapping mode.

2.2.8 Raman spectroscopy

The Raman spectroscopy technique is used in thin film research to identify the chemical phases within the material. It can be used to characterise gaseous, liquid and solids specimens. This technique is based on the inelastic scattering of light as observed by Sir. C.V. Raman in 1928, for which he won the Nobel prize two years later [12]. The molecules with changing polarisability causes the light to scatter, providing a spectral fingerprint. When more than one compound is present in the mixture, the recording will provide a superposition of each of the component. The relative intensities of the peaks can be used for qualitative analysis and a spectral library (a data base) can be consulted for quantative analysis [13].

No vacuum chamber or special sample preparations are required as it is a light scattering technique. This technique is heavily utilised in many industries as it can be operated via optical fibre cables for remote and real time sampling. The main parts of the spectrometer are; a standard optical microscope, an excitation laser, a monochromator to filter the laser light and a sensitive detector such as a charge-coupled device as listed in Figure 2.6.





Raman spectra of the samples were recorded using a RENISHAW InVia Raman microscope (courtesy of University of Leeds), with an Ar^+ laser having a wavelength of 514 nm and a power of 10 mW. The power should be controlled in order not to damage the sample surfaces. The wavenumber range for the spectroscopy used in this analysis was 100 cm⁻¹ to 2000 cm⁻¹.

2.2.9 Thickness calculations for semiconducting thin film layers

Faraday's laws of electrolysis were used to derive the equation for thickness of semiconducting thin film layers deposited by electrodeposition [15]. This method can be used to estimate the thickness.

$$T = \frac{1}{n_1 FA} \left(\frac{itM}{\rho} \right)$$
 2.6

where T = the thickness of the deposited film in cm, n_1 = the number of electrons transferred in the reaction for the formation of 1 mole of semiconductor, F = 96,485 Cmol⁻¹ is the Faraday constant, A = the area of the semiconductor in cm², i = the average current in Amperes (A), t = the time in seconds (s), M = the molar mass of the semiconductor in $g \ mol^{-1}$ and ρ = the density of the deposited film in $g \ cm^{-3}$.

2.3 Solar cell device assessment methods

2.3.1 Current-Voltage (I-V) measurement of solar cells

Current-voltage (I-V) measurements of fully processed solar cells are obtained to analyse the photovoltaic and electrical properties of the solar cells. This analysis helps us to understand the next experimental steps needed and is a measure of the device progress. I-V measurements were recorded using a Keithely 280 programmable voltage source, with a Keithely 619 multimeter. Applying one microprobe to the FTO layer (front contact) and the other probe to the Au contact (back contact), the I-V measurement can be recorded. The solar simulator containing a 250 W tungsten Halogen lamp is pre-calibrated using a standard Si solar cell with known parameter to 100 mWcm⁻² (AM1.5). The equipment can record relevant parameters to deduce opencircuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (*FF*) and efficiency (η) of the solar cells and from the dark I-V measurements, rectification factor (*RF*), diode ideality factor (*n*) and barrier height (φ_b) can be calculated.

The diagram in Figure 2.7 shows ideal I-V characteristics of a solar cell under both dark and illuminated conditions of an active solar cell.

The current density of a solar cell is given in the equation below,

$$\left(J_{sc} = \frac{I_{sc}}{A}\right)$$

2.7

From this, PV parameters such as V_{oc} , J_{sc} , FF and η can be calculated. Theoretically they are given by [16];

$$V_{oc} = n_2 \left[\phi_b + \frac{kT}{e} \cdot \ln \left(\frac{J_{sc}}{AT^2} \right) \right] \quad 2.8$$

Where n_2 = diode ideality factor, k = Boltzmann constant (1.81×10⁻²³ JK⁻¹), T = absolute temperature, e = electron charge (1.602×10⁻¹⁹ C) and A = area of the diode.



Figure 2.7: Current-voltage plots for a solar cell in dark and illuminated conditions [3]. V_{oc} is the voltage when the solar cell is illuminated at zero current. The value of the V_{oc} depends on the turn on voltage of the diode when measured under dark conditions.

Where I_{sc} = short-circuit current or when the solar cell is illuminated at zero voltage and it is equal to the photocurrent produced by incident photons.

The third solar cell parameter is the fill factor (FF) defined by,

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}}$$
 2.9

The conversion efficiency of the solar cell is then given by,

$$\eta = \frac{output \ power}{input \ power} = \frac{V_m I_m}{P_{in}} = \frac{V_{oc} \ J_{sc} \ FF}{P_{in}} \qquad 2.10$$

where, V_m = voltage at the maximum power point, I_m = current at the maximum power point and P_{in} = 100 mWcm⁻² is the power input from the incident photons under AM1.5 illumination conditions.

The series resistance (R_s) and shunt resistance (R_{sh}) can be calculated from the linear I-V plot and the effects of these on the I-V curves are shown in Figure 2.8.



Figure 2.8: The effect of R_s and R_{sh} on I-V curves of PV solar cells.

These fundamental principles are covered in many text books [2,16], so this is a brief overview.

As it can be seen from Figure 2.7 and Figure 2.8, the reduction in the series resistant (R_s) and increase in shunt resistant (R_{sh}) improves the FF of a solar cell leading to higher efficiency.

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2.3.2 Capacitance-voltage (C-V) measurements

Capicitance-voltage (C-V) measurement technique is conducted to estimate the doping concentration and the depletion width of the device. To achieve a healthy depletion region in thin film CdTe solar cells, doping concentration of a diode should ideally be 8×10^{15} cm⁻³ [16]. The capacitance measurements are recorded as a function of applied voltage across the solar cell. The depletion region and capacitance across a Schottky barrier is given by [2];

$$W = \sqrt{\frac{2\varepsilon_s}{eN_d} (V + V_d)}$$

$$C = \frac{\varepsilon_s A}{W}$$
2.11
2.12

Where, ε_s = permittivity of the semiconductor, N_d = doping concentration, V_d = diffusion voltage and these two equations are combined to get;

$$\frac{1}{C^2} = \frac{2}{\varepsilon_s A^2 e N_d} \left(V + V_d \right)$$
2.13

A $1/C^2$ vs V plot gives a straight line if the semiconductor is uniformly doped. The gradient of the straight line is used to calculate doping concentration.

2.4 Experimental Methodology

Several characterisation methods and techniques were carefully chosen in a complementary manner to understand the most paramount properties of the electrodeposited thin film layers during this intensive research programme. The properties analysed were, optical, electrical, structural, morphological and atomic composition. Experimental techniques used in this study can also be divided into material and device characterisation techniques. The main device characterization is from the I-V measurement, which provided the PV parameters of the solar cells investigated under one sun (AM1.5) illumination conditions.

The objective of this section is to describe the experimental procedure involved in preparing various semiconductors electrodeposited in this research. While there were several common elements in the preparations of various solutions, the parameters such as ionic precursors involved, molar concentrations of chemicals, growth temperatures and pH values were specific to each electrolyte.

2.4.1 Electrolyte preparation and deposition of thin films

Only de-ionized water was used during this entire research project. Chemicals used were high purity chemicals of analytical grade (99.999%). All the electrolytes were aqueous and acidic and made to a volume of 800 ml in a Teflon beaker. A glass beaker of 1000 ml was used as the outer water jacket. A graphite rod and a glass/FTO sample was used as the anode and working electrodes respectively, when the 2-electrode configuration was used as shown in Figure 1.9(a) in the Chapter 1. For ED-CdTe, the 3-electrode configuration with modified saturated calomel reference electrode (Figure 1.9(b)) was used as explained in section 2.4.1.4. To calculate the deposition current density, the growth area of each sample was recorded. The above cell was placed on a hot plate with the ability to control the speed of the magnetic stirrer.

Cyclic Voltammetry (CV) is an electro analytical technique available to study electrochemical properties of an electrolyte [17]. The experimental configuration usually uses a reference electrode, working electrode (cathode) and counter electrode (anode). This is also known as the three-electrode configuration. A two-electrode method also has its' own benefits, such as the simplicity and elimination of possibly harmful ions [18]. This voltammogram technique was conducted by scanning the applied potential in forward and reverse direction at a scanning rate of normally ~5 mVs⁻¹. This experiment allows a faster estimate of a possible deposition voltage range of the thin film [19].

The experimental range of the deposition of semiconductors was narrowed down by conducting a voltammogram using an ACM-GillAC instrument. Then a number of layers were grown in this range in order to characterise and optimise the growth voltage. This experiment narrowed the possible growth range to few hundred millivolts saving valuable time and effort from the research programme.

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2.4.1.1 Electrolyte for deposition of ZnS layers

The electrodeposition of ZnS was conducted with the 2-electrode configuration. The ZnS electrolyte consisted of 0.15M ZnSO₄ and 0.30M $(NH_4)_2S_2O_3$ to provide Zn²⁺ and S²⁻ ions respectively. The temperature was set to $85\pm2^{\circ}C$, the stirring rate was low and constant and the pH value of this bath was ultimately adjusted to 2.00±0.02 using diluted H₂SO₄ acid and NH₄OH. In this thesis, this solution is referred to as the ZnS bath.

2.4.1.2 Electrolyte for deposition of CdS layers

The electrodeposition of CdS was carried out in the 2-electrode configuration. The CdS electrolyte consisted of 0.30M of CdCl₂ and 0.03M of $(NH_4)_2S_2O_3$ for Cd²⁺ and S²⁻ ions respectively. The pH value of the bath was adjusted to 2.00±0.02 using diluted HCl and NH₄OH. The temperature was set to $85\pm2^{\circ}C$ and the stirring rate was low and constant. Some parameters and guidelines for the preparation of this electrolyte were from previous research in this extensive research programme [18]. Here, this electrolytic solution is referred to as the CdS bath.

2.4.1.3 Electrolyte for deposition of CdS_(1-x)Se_x layers

The objective of electrodepositing of $CdS_{(1-x)}Se_x$ was to search for a more uniformly grown thin film layer avoiding the pinhole formation. The same electrolyte conditions were kept for this as the CdS bath while gradually adding Se ions from an aqueous solution containing 0.03M of SeO₃. Cathodic electrodeposition was carried out at a temperature of $85\pm2^{\circ}C$, pH value of 2.00 ± 0.02 and in a 2-electrode configuration. It was reported in a previous study [18], that the addition of Se provided more uniform layerby-layer electrodeposited layers. To obtain this advantage, Se ions were added to CdS bath [20].

2.4.1.4 Electrolyte for deposition of CdTe thin films

The research on the electrodeposition of CdTe was conducted with the conventional 3electrode setup, as shown in section 1.4.1.1. The aqueous solution was prepared with 1.0M CdSO₄ of 99% purity. The pH value was 2.00 ± 0.02 and temperature was
controlled to just below 70°C as required by the manufacturer's specifications for saturated calomel reference electrodes. The pH value of the electrolyte was controlled using H₂SO₄ and NH₄OH. The standard Hg/HgCl₂ calomel electrode from Thermo-Fisher and a graphite electrode were used as the reference electrode and anode respectively. The outer electrolyte of the calomel electrode double junction was replaced with 4.0M CdCl₂ to mitigate further unwanted K⁺ ions from KCl leaking into the electrolyte. Furthermore, to remove any residue and impurities, a low growth voltage ($V_g = 0.450 \text{ mV}$) was applied to the working electrode without allowing Cd to deposit. This electro-purification was carried out for 48 hours to remove impurities from the bath. 1000 ppm CdI₂ was added to the solution for I doping. This was done to gain the advantages reported by Chaure et al [21], that the inclusion of Iodine leads to improved conductivity hence, more current is collected from the solar cell [20,21]. The work by Romeo et al also involved the use of halogens (Cl and F) to enhance the conversion efficiency [22]. TeO₂ powder was dissolved in dilute H_2SO_4 in de-ionized water until the saturation point. Following the purification, ~1 ml of TeO₂ solution was added to the 1.0M CdSO₄ solution.

After each growth, it is crucial to add ~1.0 ml of TeO₂ solution to the electrolyte using a pipette if the deposition current density is lower than expected. A deposition current density of ~ 150 μ Acm⁻² is observed to be an indication of optimum Te²⁻ level from unpublished results from this research group. This slow addition of Te²⁻ ions prevents the deposited CdTe layers becoming Te-rich and the CdTe becoming p-type in electrical conduction. This process leads to better quality CdTe layers avoiding usually observed tellurium precipitates and leading to higher performing solar cells [24].

2.4.2 Solar cell fabrication steps

The crucial steps in fabricating all ED-solar cells are detailed and analysed in this section. The optimisations of electrodeposited thin film layers should be achieved to an extremely high level before attempting to fabricate solar cells. If the thin film layers are not of high semiconductor grade quality, solar cells will not be PV active or will have poor performance. If that is the case, a researcher might be led to believe the process of electrodepositing of solar cells is not feasible. This process is continuously optimised and refined due to the improved and rapid understanding gained during this research.

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Several optional steps are also reported here. Current density should be recorded during electrodeposition of any thin film layer in order to calculate the thickness of the layer deposited. Current density is also an important indicator to understand the in-situ growth conditions.

2.4.2.1 Substrate preparation

The majority of the experimentation was carried out using glass/FTO substrates of TEC-7 and TEC-15 with sheet resistance 7 Ω/\Box and 15 Ω/\Box respectively. The FTO substrates were provided by Pilkington for research purposes. Both substrates are good candidates for the fabrication of all-ED solar cells based on CdTe with over 90% optical transparency in the wavelength of interest, between 400 nm to 800 nm. Glass/FTO sheets are known for high thermal stability and low production cost [25]. All the samples were prepared for electrodeposition in a similar procedure as described in this section.

Glass sheets were cut to an average size, $2 \times 3 \text{ cm}^2$, without damaging the FTO side, as damages may lead to pinholes. Glass/FTO samples were ultrasonically cleaned in soapy water for 15 minutes. They were then rinsed in de-ionized water, washed with dilute nitric acid, dilute acetic acid, acetone and methanol while rinsing in turn with de-ionized water. Then each sample was dried in a pressurised flow of nitrogen gas to prevent airborne particles from getting absorbed to the cleaned surface. The cleaned sample, glass/FTO working electrode was attached to a high purity carbon rod with non-contaminating Teflon tapes. The area of each sample was recorded to calculate the deposition current density. Current density is used to calculate the thickness of the thin film layers deposited while providing a gauge of the required ion addition.

2.4.2.2 Electrodeposition of semiconducting thin film layers

During the fabrication of fully-electrodeposited (all-ED) solar cell, at least two thin film layers are electrodeposited to form a solar cell. When only a window layer and an absorber layer are in use as in Figure 2.9, only two semiconducting layers forming a heterojunction are utilised to fabricate a solar cell. During this project three electrodeposited thin film layers as window layers, (ZnS, CdS and $CdS_{(1-x)}Se_x$) were experimented.

A buffer layer with a wide bandgap enhances the amount of sunlight captured by the solar cell and provides a better growth for the CdS window layer [26]. Furthermore, it is advantageous to include a good quality buffer layer in the device to reduce possible pinholes in the thin film layers. A device structure with a buffer layer is shown in Figure 2.10.



Figure 2.9: Standard glass/FTO/window layer/absorber layer/metal contact solar cell structure.



Figure 2.10: Solar cell structure with an incorporated buffer layer.

Due to the presence of pinholes in very thin films, these layers can cause short-circuit in the solar cell if the back contact metal comes in contact with the FTO front contact. A uniformly or layer-by-layer grown $CdS_{(1-x)}Se_x$ layer can prevent this when it is used as

an intermediate layer prior to the deposition of the CdTe layer. This idea was tested by fabricating a glass/FTO/CdS/CdS(1-x)Sex/CdTe/Cu-Au (back contact) device.

In the case of using a buffer layer (Figure 2.10) or intermediate layer as in Figure 2.11, a solar cell has three semiconducting thin film layers. ZnS layers were utilised as buffer layers and $CdS_{(1-x)}Se_x$ was used in the experimental settings as an intermediate layer.



Figure 2.11: Solar cell structure with an incorporated intermediate layer.

With the use of all thin film layers available under this research, one more structure was investigated. A multi-layer graded bandgap device, glass/FTO/ZnS/CdS/CdS_(1-x)Se_x/CdTe /CuAu was fabricated as illustrated in Figure 2.12 by the all-ED method. Due to the different bandgaps of these semiconducting materials, photons are absorbed from the solar spectrum from 335 nm to 850 nm as illustrated in Table 1.2 of Chapter 1. The performance of such devices will be enhanced by each semiconducting layer with different bandgap absorbing photons from a different part of the solar spectrum.



Figure 2.12: Solar cell with multi-layer graded bandgap device architecture.

2.4.2.3 CdCl₂ heat treatment

In order to enhance the properties of as deposited thin film CdS and CdTe layers, CdCl₂ heat treatment is a paramount step prior to the processing of solar cells. CdCl₂ inclusion in the annealing stage is widely reported to help reduce defects [27,33], surface passivation [27] recrystallisation [34,35], reduce the resistivity [28], hence higher mobility of charge carriers [28] increasing the life time [29]. The interfacial mixing between the two layers cause better lattice matching reducing the surface stress on the thin film layers [30] as shown in AFM studies. The increase in grain sizes when the grain sizes are smaller [31] and the locking up of grains when the grains are already larger is also reported [32]. Some researchers simply refer to this as the magic step since the most important reasons are not yet understood.

 $CdCl_2$ -methanol solution is only applied for Cd based semiconductor layers, CdS, $CdS_{(1-x)}Se_x$ and CdTe. The material layers were dipped in a methanol solution saturated with $CdCl_2$ powder, air dried and then heat treated to the relevant temperature in the air. While methanol solution is widely used by research groups [36], evaporation method is also practiced [22].

After applying $CdCl_2$ the samples are placed in a heated furnace, CARBOLITE furnace, model: ELF 11/6B. In the case of CdS and $CdS_{(1-x)}Se_x$ samples, annealing conditions

were 400°C for 20 minutes and for CdTe layers, annealing conditions were 450°C for 15 minutes. These heat treatment conditions were carefully selected and optimised. The heat treatment conditions applicable to this research are summarised in Table 2.1.

Material	ZnS	CdS	CdS _(1-x) Se _x	CdTe
Heat treatment at $(\pm 5^{\circ}C)$	350	400	400	450
Duration (min)	10	20	20	15
CdCl ₂ treated	No	Yes	Yes	Yes

Table 2.1: Summary of annealing conditions during this work for thin film layers.

ZnS samples were heat treated at 350°C for 10 minutes without the use of any chemical treatment. Even though several chemicals were investigated, so far direct heat-treatment has improved the deposited ZnS layers.

2.4.2.4 Surface etching (Oxidizing etch and Reducing etch)

Once the final n-type ED-CdTe layer is $CdCl_2$ treated and heat treated, the surface should be prepared for the fabrication of the Cu/Au back contact. In this research programme, Cd-rich surfaces were obtained prior to metallisation [24], otherwise, the solar cells will perform poorly with Cu/Au as the back contact. In order to prepare the surface, oxidizing etch and reducing etch steps must be carried out to achieve enhanced results [16, 37].

Oxidizing etch was prepared by using ~ 0.03 g potassium dichromate ($K_2Cr_2O_7$) with 0.1 ml of H_2SO_4 in 20 ml of water. For the reducing etch 20 ml of water was heated to 50°C after adding 2 pellets each (0.5 g) from NaOH and Na₂S₂O₃.

To remove any excess Te from the surface of ED-CdTe layers, a sample was dipped in the oxidising etch for about 5 seconds. After rinsing, the sample was placed in the reducing etchant for 2 minutes before washing the sample in de-ionised water. After the basic etching was applied on the ED-CdTe thin film layer, a Cd-rich surface was obtained [38]. It is reported that CdTe surfaces must be Cd-rich in order to achieve high quality Schottky barriers at metal/n-CdTe interfaces [24,39].

2.4.2.5 Back metal contact metallisation

Following chemical etching, the samples were promptly loaded to the metalizer to evaporate back contacts. The metaliser was Edward Auto 306 with two filaments and

with a quartz crystal film thickness monitor. Previous researchers of the group reported the use of 50% each of Cu and Au as the back contact due to their high work function. Cu and Au to be evaporated were placed in one of the tungsten filament boats in the vacuum chamber. A vacuum was created to the pressure of $\sim 10^{-6}$ mbar. Finally by applying current to the tungsten filaments to heat to the required temperature, Cu/Au contacts were evaporated to create the back contact. After about 30 minutes, the chamber was de-pressurised, and the fully fabricated solar cells were removed for assessment.

2.4.2.6 Measurements of PV solar cells

The main PV parameters, V_{oc} , J_{sc} , FF and η were obtained by measuring I-V characteristics under illumination as described in section 2.3. Furthermore, ideality factor, series resistance, and shunt resistance were analysed to understand the behaviour of these electrical devices.

2.4.3 Summary of the fabrication processes of all ED-solar cells

The simple electrodeposition method of fabricating solar cells is detailed in this chapter. While the process is simplified, each step requires complete understanding of the solidstate chemistry, physics, and other scientific principles. The simplified steps of all-ED solar cell fabrication are listed below to give the reader the complete concept of this simple process.

- 1. Preparation of glass samples to approximate sizes of 2×3 cm²,
- 2. Cleaning of the glass/FTO substrates as detailed in the substrate preparation section above
- 3. Rinse with methanol or basic etch (NaOH+Na₂S₂O₃) solution
- 4. Electrodeposition of buffer layer (option ZnS)
- 5. Heat treatment of the buffer layer
- 6. Rinse with methanol or basic etch (NaOH+Na₂S₂O₃) solution
- 7. Electrodeposition of window layer
- 8. Heat treatment of the window layer with CdCl₂ treatment

9. Rinse with methanol or basic etch (NaOH+Na₂S₂O₃) solution

10. Electrodeposition of absorber layer

11. Heat treatment of the absorber layer, with CdCl₂ treatment

12. Surface etching with oxidizing and reducing etch

13. Metallisation with 2 mm or 3 mm diameter back contacts, and

14. Measurements of the device PV activity and result analysis.

The steps 4 to 6 are redundant when no buffer layer was used in the device structure, further simplifying the process.

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Chapter 3. Electrodeposition of ZnS buffer layer

3.1 Introduction

This chapter presents the results of the semiconductor material ZnS researched under this programme. The objective is to produce ZnS layers suitable to be used in fully electrodeposited (all-ED) solar cells. Acidic aqueous electrolytes in the 2-electrode cell configuration were used in the process. The layers were characterised for their structural, optical, electrical, elemental and morphological properties. ZnS thin films were developed to be used as either a buffer or a window layer in a solar cell. New precursors to produce these thin film layers were selected to provide the ions required in electrodeposition. Results of the materials under optimised electrodeposition conditions are presented here. A novel chemical combination, with sodium (Na) free precursors were selected to minimise the amount of Na in the ZnS and CdTe layers. The optimised thin film layers are used in all-ED solar cells and the results are presented in Chapter 6.

3.2 Literature review of ZnS thin films

ZnS is a non-toxic, wide bandgap optical semiconductor. It is from the II-VI compound semiconductor family with a reported bandgap of 3.68 eV with both cubic and hexagonal structures [1]. ZnS layers have been extensively used in many applications in industry, such as solar cells [5,6], LEDs [2], UV-light sensors [3], gas sensors, chemical sensors, biosensors, nano-generators and in anti reflection coatings [4].

There are several objectives in electrodepositing ZnS layers as part of this research programme. Primarily this material layer was electrodeposited to investigate the effectiveness of ZnS as a buffer layer in solar cells. The surface variation of the FTO substrates used in the electrodeposition of thin films for solar cells is about ± 100 nm [7]. This causes sharp edges creating stronger electrical fields, which effects the growth of the window layer. This effect can be mitigated if a suitable uniform buffer layer is used before the window layer. Furthermore, having this semiconductor in this research programme adds the possibility of testing ZnS as an alternative window layer to CdS, as part of a multi-layer graded bandgap device structure.

ZnS layers have been previously deposited by several methods: these include thermal evaporation [11,12], vapour phase epitaxy [8], atomic layer deposition [9], spray

pyrolysis [10], laser ablation [13,14], CBD [15,16] and electrodeposition [17-19]. In this research programme, the 2-electrode configuration was chosen to minimise the complexities, which were outlined in Chapter 1. This 2-electrode method has also been used successfully in electrodepositing other semiconductor materials [20-22].

3.3 Characterisation and results of ZnS layers

After investigating the literature on ZnS, the controlling parameters such as, electrolyte ionic concentrations, the growth temperatures, the pH values, precursors, deposition times and the applied growth voltage were established. The electrolyte used to electrodeposit ZnS layers was prepared as detailed in section 2.4.1 of Chapter 2.

The electrolyte was maintained at the highest possible temperature for an aqueous electrolyte, as a high growth temperature (T_g) is expected to provide a better crystalline material. After the preparation of the electrolyte containing the relevant ions, a cyclic voltammogram was recorded. The voltammogram of the ZnS bath is shown in Figure 3.1. This voltammogram was used to deduce the approximate cathodic growth potentials to be in the range of (1200 - 1600) mV (the shaded area). Between -70 mV (point A), and 1200 mV cathodic voltage (point B), sulphur starts to deposit. From here onward, until about 1600 mV (point C), Zn with sulphur is electrodeposited. After 1600 mV elemental Zn deposition takes place as shown by a drastic increase in current density [23]. At these voltages hydrogen gas evolution also takes place in parallel on the cathode due to electrolysis of water. In the reverse scan until 1350 mV (point D), deposition of Zn and S is reduced. From here onward Zn is dissolved by 1200 mV (point E), and finally S ions are striped off from the substrate [24].



Figure 3.1: 2-electrode cyclic voltammogram of acidic and aqueous electrolyte containing ions of 0.15M ZnSO₄ and 0.30M $(NH_4)_2S_2O_3$, at temperature of $85\pm2^{\circ}C$. The stirring rate was low and constant with a pH value of 2.00 ± 0.02 .

3.3.1 X-ray diffraction (XRD) measurements

Several samples deposited at different growth voltages (V_g) and for the same growth duration (t_g) were subjected to XRD characterisation, to identify the structural properties of the ED-ZnS layers. It was reported in the literature that at lower growth temperatures (T_g) electrodeposited ZnS layers have the tendency to be amorphous [25,26].

In order to observe the structural make up of the thin film layers, comparatively thicker samples were grown; Figure 3.2 shows the typical XRD spectra of such samples. Samples grown at various cathodic voltages and for several durations all showed ED-ZnS thin film layers under these conditions to be amorphous. This is similar to a study carried out with ED-ZnS grown using ZnCl as the zinc precursor [27]. The crystallinity could not be achieved even after the heat-treatment of samples over a range of temperatures was tested.



Figure 3.2: XRD spectra of typical as-deposited (AD) and heat-treated (HT) ZnS layers deposited at 1475 mV.

3.3.2 Photoelectrochemical (PEC) cell

PEC cell tests were conducted to determine the electrical conductivity type of electrodeposited ZnS thin film layers.

A range of ZnS samples were electrodeposited and the PEC signal was measured against a carbon anode as described in section 2.2 in Chapter 2. It was possible to deposit both p-type and n-type ZnS thin film layers. The variation of PEC signal and hence the electrical conductivity against growth voltage is shown in Figure 3.3.

Growth voltage	As-deposited samples		Heat-treated samples		
	PEC signal	Conduction	PEC signal	Conduction	
(mV)	(mV)	type	(mV)	type	
1440	-4	n	-5	· n	
1445	-1	n	-10	n	
1465	-9	n	-11	n	
1470	-8	n	-20	n	
1475	-11	n	-4	n	
1480	-20	n	-6	n	
1490	-4	n	-11	'n	
1500	-7	n	-17	n	
1550	-8	n	-8	n	
1585	-66	n	-56	n	

Table 3.1: PEC signal observed from electrodeposited ZnS samples from various growth voltages for as-deposited and heat-treated layers.

Table 3.1 shows the change of electrical conduction of n-type with varying growth voltages of ED-ZnS. The samples have n-type electrical conductivity for as-deposited and heat-treated conditions.



Figure 3.3: PEC cell results of ZnS layers grown at various growth voltages showing production of predominantly n-type ZnS layers.

Optimum quality ED-ZnS thin film layers were produced at a cathodic voltage of \sim 1475 mV and were n-type in electrical conductivity. The ED-ZnS layers that showed p-type electrical conductivity were of poor adhesivity and quality. For all useful purposes, ED-ZnS thin film layers are considered to be of n-type in electrical conduction. Fang et al. also reported in their comprehensive review paper, that it is more natural to produce n-type ZnS [25]. The n-type ZnS deposited during this study had better material properties suitable for solar cell fabrication.

3.3.3 Optical absorption measurements

Optical absorption is a very useful technique in electrodeposition to optimise the growth voltage. Having identified the approximate initial growth voltages from the voltammogram in Figure 3.1, several test samples were deposited and subjected to optical absorption studies. Here the general guideline being, the closer the bandgap of the sample is to the bandgap of bulk ZnS, the closer the sample is to the optimum growth voltage.. The bandgaps of as-deposited ZnS layers are shown in Figure 3.4. It has to be noted that the background on some of the absorption spectra which could be caused by light scattering may affect slightly the obtained values of Eg. Therefore, in extreme cases of light scattering on rough surfaces or cloudy materials, the background should be eliminated.



Figure 3.4: Optical absorption curves of as-deposited ZnS layers grown for various V_g . The bandgap values for optimum quality as-deposited ZnS layers are in the range (3.88-3.94) eV. All the samples were grown for 1 hr duraton.

After annealing the ED-ZnS samples the absorption decreased and bandgap values are in the range (3.85 - 3.95) eV as shown in Figure 3.5. Within this growth region, the ZnS layers have good adhesion to glass/FTO substrates with uniform light brown colour. The best observed annealing conditions in this research was 350°C for 10 minutes, and the annealed layers became almost colourless. It is also observed that, heat-treated samples have lower absorption. This low absorption allows more photons to reach the absorber layer when used as a window layer increasing the photocurrent produced in solar cells.



Figure 3.5: Optical absorption curves of annealed ZnS layers grown at different voltages (V_g) .

To find the optimum growth time several ZnS layers were electrodeposited at 1475 mV while varying the growth duration (t_g). The ZnS samples were grown for 20, 40 and 60 minutes. They were subjected to optical absorption characterisation and the results are shown in Figure 3.6.





The absorption increased with samples grown for a longer duration. As shown in Figure 3.6, samples grown for 20 minutes did not show any absorbance and it was difficult to establish the energy bandgap. The samples grown for 40 minutes and 60 minutes had bandgaps of 3.82 eV and 3.78 eV respectively. The colour of the ED-ZnS layers grew darker with increasing deposition times.



Figure 3.7: Optical absorption curves of heat-treated ZnS layers grown for different durations.

The bandgaps of heat-treated ZnS layers are in the range of (3.92 -3.94) eV. This is a slight increase when compared to the as-deposited samples. The absorption decreased as the samples became almost colourless after annealing at 350°C for 10 minutes. As a window layer, it is beneficial to be lighter in colour to let more of the spectrum through to the absorber layer of a solar cell. Several reports in the literature show electrodeposited and CBD-ZnS of having a slightly lager band gap than that of bulk ZnS [2,8] due to the decrease in crystallite sizes and therefore due to quantum effects.

3.3.4 Scanning Electron Microscopy (SEM)

The surface finish of the thin film layers have a profound impact on the performance of the solar cells fabricated using them. To understand the nature of ED-ZnS thin film layers, surface and cross-sectional SEM studies were carried out.



Figure 3.8: SEM images at different magnifications indicating the gaps between the grains of ED-ZnS samples grown at 1480 mV cathodic voltage and at $85\pm2^{\circ}C$ (with the courtesy of collaborator at Uni. of Durham) grown for 1 hour as used in solar cell fabrication.

The high resolution SEM images shown in Figure 3.8 show the ZnS layers exhibiting grain sizes in the range of (50 - 60) nm. The ZnS grains consisted of further fine amorphous sub-grains in the order of nano-particles of ~4 nm. The coating also exhibited inter-grain porosity between the coalesced groups of ZnS grains.



Figure 3.9: Cross sectional SEM images of ZnS layers (high resolution SEM from the collaborators at Uni. of Durham).

Figure 3.9 shows the correlation of the shape of the FTO layer with the surface finish of the ZnS layers. This correlation of layers indicates the challenges faces by electrodeposition to produce more uniform semiconducting materials. Several voids created in the growth are also visible in the images. Pilkington Group, UK, deposits SiO_2 layer as a buffer layer before depositing of FTO. The thickness of SiO_2 , FTO layer, ZnS can be estimated to be ~40 nm, ~440 nm and ~230 nm respectively from this figure. The darker layers above the ZnS layer is a carbon layer deposited to create the conductivity required for SEM experiment. To protect the thin film layer from the electron beam emitted during the SEM measurements, a Pt layer was also deposited. These two layers are also clearly seen in Figure 3.9

3.3.5 Energy Dispersive X-ray (EDX) analysis



Figure 3.10: EDX spectrum of ED-ZnS layers grown on glass/FTO substrates, qualitatively indicating the presence of Zn and S in the layers.

The presence of Zn and S are shown in the EDX spectra on all the samples tested, however they are present at relatively trace levels as the main element present for the coating is Sn. A typical ED-ZnS EDX spectrum is shown in Figure 3.10, which includes Si and O that were thought to be from the glass substrate. The semi quantitative values obtained from EDX analysis software calculated the ratios between Zn and S (ignoring other elements) to between 45 and 55 atomic % respectively for a range of samples grown at different growth voltages. Since both Zn and S peaks are weak, the quantitative analysis is not accurate. Therefore, the stated atomic % should be taken as only a guide. Table 3.2 shows the Zn/S-atomic % ratios for the ED-ZnS under varying deposition conditions.

	As-depo sam	sited ZnS	Heat-treated ZnS samp	
Growth voltage (mV)	Zn%	S%	Zn%	S%
1465	45.10	54.90	45.92	54.08
1475	46.78	53.22	46.79	53.21
1495	46.94	53.06	46.72	53.28

Table 3.2: EDX semi quantitative elemental composition ratio of ED-ZnS samples grown at different growth voltages (mass %).

3.3.6 Atomic Force Microscopy (AFM)

The surface scan from AFM studies shown in Figure 3.11 helps to analyse the surface roughness of a typical ED-ZnS thin film layer. The surface roughness is heavily influenced by the surface variations from glass/FTO substrate as shown in Figure 3.9. Furthermore, such a variation should ideally be averted to reduce short circuiting of thin film solar cell devices under investigation.



Figure 3.11: 2D-AFM scan image of a heat-treated ZnS layer electrodeposited at 1475 mV.

In Figure 3.11, the AFM image shows a surface variation in the order of ± 130 nm on annealed ZnS layers. The surface variations from the glass/FTO substrates are kept, although reduced even after the deposition of ED-ZnS layers as also shown in the cross sectional SEM images in Figure 3.9.

3.4 Summary and Discussion of ZnS

The electrodeposited layers exhibited good adhesion to the glass/FTO substrates when the layers are n-type in electrical conduction. Optical absorption studies showed, the energy bandgap was in the range (3.75 - 3.95) eV. This is close to the reported value of the bandgap, 3.68 eV for bulk ZnS. The amorphous nature of the thin films was confirmed by the XRD studies. High-magnification SEM images of ZnS thin film layers showed an average grain size of ~4 nm consisting of nano-particles. As revealed by PEC studies, optimum quality electrodeposited ZnS samples were n-type under the experimental conditions of this programme. The surface variations of the glass/FTO substrates were reflected in the surface variation of the ED-ZnS thin film layers as shown by AFM and SEM studies.

The initial precipitations of excess sulphur ions in the electrolyte become stabilised once the electrodeposition was conducted on a few samples. This leads to the conclusion that the accuracy of the process for the addition of S ions, is not very critical to the electrodeposition of ZnS, which makes it unnecessary to monitor the S concentrations at a minute level in the electrolyte. This simplifies electrodeposition process even more.

Once the growth conditions for the ZnS bath were optimised, in line with Lincot's observations [28], ZnS layers from this bath primarily became *n*-type in electrical conductivity. The layers were highly adhesive, withstood annealing at 450° C for 20 minutes and large uniform layers up to 15 cm² were grown.

The ED-ZnS thin film layers were utilised in all-ED solar cell fabrications. ZnS can provide several functions in a solar cell as buffer layer, as window layer and also as a part of a graded bandgap solar cell as described in Chapter 2. The application of these optimised ED-ZnS thin film layers in all ED-solar cells are discussed in Chapter 6.

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3.5 References

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4.1 Introduction

This chapter presents the two window layers (CdS and $CdS_{(1-x)}Se_x$) researched and developed for use in electrodeposited solar cells under this programme. In both the experiments to develop the layers, acidic aqueous electrolytes with suitable chemical combinations were used in a 2-electrode configuration. The objectives of CdS electrodeposition is to produce Na free CdS thin film layers and use it as the window layer in CdTe based solar cells. $CdS_{(1-x)}Se_x$ layers were researched to produce deposition of layer-by-layer, covering the whole substrate area while minimising the pin holes to increase of the efficiency of solar cells.

4.2 Research and development of electrodeposited CdS layers

4.2.1 Literature review of CdS thin film layers

The primary objective of this research is to electrodeposit CdS thin film layers to be used in CdTe solar cells. Electrodeposition has many advantages over several other low-cost deposition methods, which were discussed in detail in section 1.4 in Chapter 1. In a suitable electrolyte, Na-free pre-cursors are used to electrodeposit CdS. Such CdS may avoid the issues faced by the inclusion of Na in CdTe based solar cells [1,2,]. Dennison in 1994 experimentally studied the detrimental effects of Na in CdTe based solar cells.

CdS is a direct, wide bandgap semiconductor from the II-VI family, which is used in many applications such as optical sensors [3] and optical devices such as solar cells [4]. Hence, it is a well-researched and widely used thin film semiconductor. CdS has excellent properties to match with CdTe to produce a stable solar cell [5]. CdS is also used in CIGS solar cells [6]. The photovoltaic effect of CdS was first reported by Reynolds in 1954 [7]. CdS exists in two structural forms, cubic (zinc blend structures) and hexagonal (wurtzite) while the bandgap is reported to be the same at 2.42 eV, hence it is a yellow/orange coloured window layer semiconductor [8]. CdS is also a chemically stable material with a high melting point of ~1400°C [9]. It is n-type in electrical conduction and difficult to be p doped to produce p-type semiconductors. Fabrication of n-type CdS window layers for CdTe and CIGS solar cells is well studied [10-12] and mostly from *Na* containing precursors, such as Na₂S₂O₃.

It is produced in several ways, such as chemical bath deposition (CBD) [13], sputtering [14], CSS [15], spray pyrolysis [16], Metal Organic Chemical Vapour Deposition (MOCVD) [17], Successive Ionic Layer Adsorption and Reaction (SILAR) [18] and electrodeposition [19,20].

CBD method produces polycrystalline CdS, generally with a cubic phase. Polycrystalline CdS is also deposited by vacuum evaporation (VE), primarily with hexagonal phases [13]. Higher temperature deposition methods, such as MOCVD, CdS thin films are reported with far better crystallinity [21] giving better results when used in CIGS solar cells in comparison to CBD-CdS [17].

Following relatively low temperature deposition methods, such as electrodeposition and CBD, CdS thin film layers are annealed before they are used as CdS window layers in solar cells [22,23]. The annealing process includes immersion of samples in a $CdCl_2$ /methanol solution before drying and heat-treating to increase many material properties of the deposited CdS layers. The effects of heat-treating of thin film layers were discussed in detail in section 2.3 in Chapter 2.

Figure 4.1 shows EDX spectroscopy, a qualitative analysis of glass/FTO substrates used in solar cells. Once the glass/FTO substrates are annealed which is a required step as described in section 2.4 in Chapter 2, it is seen that Na from soda lime glass penetrates the FTO layer. This is to be mitigated or eliminated to produce better performing solar cells.



Figure 4.1: EDX spectra of soda lime glass/FTO showing the presence of Na on the FTO surface.

4.2.2 Characterisation and results of CdS thin film layers

The electrolyte was prepared as detailed in section 2.4.2 in Chapter 2. To identify the initial growth voltage (V_g), the electrolyte was subjected to a voltammogram. It indicated that the deposition of CdS could take place from 1200 mV to 1600 mV cathodic voltage, as shown in Figure 4.2. Initially between points A and B on the voltammogram, deposition of elemental S takes place. Cd ions along with S ions get included in the deposition layer in between points B and C, followed by the deposition of elemental Cd after point C. In the reverse direction until point D, elemental Cd is deposited and dissolved simultaneously and at point D, these two processes are equal. After point D, dissolution of Cd takes place producing an electric current in the opposite direction. At lower voltages after point A, S dissolution takes place creating a negative current [24].

A previous electrodeposition study of CdS with a Na containing electrolyte on glass/FTO also reported that the optimum ED-CdS was produced in this range [20]. Precipitations were common occurrences in the electrodeposition investigations, however it was soon observed that the precipitations were not an issue once the electrolytes became stabilised in this high temperature electrolyte. As the electrodeposition of materials at higher temperatures, produce more crystalline materials, it was decided to conduct electrodeposition at the highest possible temperature for an aqueous electrolyte, $85\pm2^{\circ}$ C [25]. The voltammogram of the electrolyte containing Na free S precursors is shown in Figure 4.2.





Several samples were electrodeposited and characterised using various complementary methods to optimise the deposition parameters.

4.2.2.1 X-ray diffraction (XRD) measurements

Several ED-CdS window layers grown in the possible growth range were investigated to identify their structural makeup. XRD spectra of the samples grown in the range (1440 - 1470) mV are shown in Figure 4.3. The polycrystallinity of these material layers was visible from the weak hexagonal XRD peaks of as-deposited samples. The reflections from (100), (002), (101), (102), (110) and (103) planes were identified and are in agreements with several researchers in the field [20] indicating the deposited CdS layers are comparable.



Figure 4.3: XRD patterns of as-deposited ED-CdS layers grown at different voltages (V_g) .

As detailed in section of 2.2 in Chapter 2, all ED-CdS samples were heat-treated at 400°C for 20 minutes to improve the properties of the CdS layer. The improved crystallinity of ED-CdS after heat-treatment was indicated by the increased intensities of the XRD peaks, as shown in Figure 4.4. Structural makeup remained the same as hexagonal. It is reported in the literature that the structure of ED-CdS is hexagonal [20] and this is in agreement with the results from this experiment.

The samples grown at 1460 mV cathodic voltage had better crystallinity as shown in Figure 4.4 in comparison to the other near optimum quality samples investigated.



Figure 4.4: XRD patterns of annealed ED-CdS layers grown at different voltages (Vg).

Structural parameters such as FWHM (full width at half maximum), lattice spacing and peak positions were used to calculate crystallite size using the Scherrer equation as detailed in section 2.3 in Chapter 2. For heat-treated ED-CdS layers grown at 1460 mV cathodic voltage, various XRD parameters are summarised in Table 4.1.

Table 4.1: Summary of observed values (OV) and reported values (RV) of XRD parameters for heat-treated ED-CdS layers deposited at 1460 mV, for 1 hour.

JCDS ref.	JCDS ref. 2θ (Degrees) Lattice spacing d(Å)		pacing d(Å)	Crystallite size	FWHM	h k l	
	OV.	RV	OV	RV	D (nm)	(rad)	
01-075-1545	24.78	24.80	3.579	3.587	43.61	0.195	100
01-075-1545	26.49	26.49	3.373	3.362	52.49	0.162	002
01-075-1545	28.16	28.17	3.191	3.165	52.68	0.162	101
01-075-1545	36.62	36.60	2.467	2.453	44.87	0.195	102
01-075-1545	43.67	43.67	2.066	2.071	34.41	0.260	110
01-075-1545	47.78	46.81	1.909	1.901	34.93	0.260	103

4.2.2.2 Photoelectrochemical (PEC) cell studies

As-deposited and heat-treated ED-CdS thin film layers were subjected to PEC cell characterisation to determine the electrical conduction type. All the ED-CdS layers produced under all the circumstances in this investigation were n-type in electrical conductivity. This agrees with the reported electrical conduction type of CdS [20].



Figure 4.5: The results of PEC cell characterisation of CdS layers grown at various cathodic voltages (V_g).

Table 4.2: PEC cell values showing the electrical conduction type of as-deposited and heat-treated ED-CdS samples grown at different cathodic voltages.

Cathodic voltage	As-deposited samples		Heat-treated samples		
	PEC signal	Conduction	PEC signal	Conduction	
(mV)	(mV)	Туре	(mV)	Туре	
1300	-36	n	-19	n	
1320	-25	n	-16	n	
1360	-20	n	-28	n	
1400	-84	n	-61	n	
1420	-60	n	-50	n	
1430	-24	n	-49	n	
1445	-18	° n	-20	n	
1450	-24	n	-13	n ·	
1460	-25	n	-24	. n	
1500	-59	n	-66	n	
1560	-18	n	-14	n	
1600	-21	n	-36	n	

Both as-deposited and heat-treated samples of electrodeposited CdS layers were n-type and test samples were deposited for 40 minutes for this characterisation.

4.2.2.3 Visual appearance of CdS layers

In order to investigate the scalability of ED-CdS samples it was decided to electrodeposit samples as large as possible. These samples produced uniform layers with an area of up to 15 cm^2 , which was the limit of the apparatus. A photo of the samples is shown in Figure 4.6.



Figure 4.6: A photo of annealed electrodeposited CdS layers for different growth times $(V_g = 1460 \text{ mV})$ showing the colour change with increasing growth duration.

Once the precipitations were settled, which occurs after several depositions, it was possible to deposit larger area visually uniform samples as shown in Figure 4.6.

4.2.2.4 Optical absorption measurements

Optical absorption is an important step in identifying the optimum V_g for electrodepositing CdS. Optical absorption curves of optimised thin film layers from the CdS bath are shown in Figure 4.7. The ED-CdS had an energy bandgap 2.45 eV, very closed to reported value in the literature, 2.42 eV [26]. The deposited samples were dark yellow in colour and with high adhesivity.

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After annealing at 400°C for 20 minutes, the colour of CdS thin film layers changed from dark yellow to orange-yellow. This observation is similar to the previously electrodeposited CdS thin film layers from Na containing precursors [20].

The heat-treated samples displayed a sharper edge in optical absorption studies indicating improved absorption of light as shown in Figure 4.8. The samples grown at a cathodic voltage of 1460 mV cathodic voltage had the best absorption edge. So this growth voltage is considered to produce optimum quality ED-CdS layers under the current experimental settings. Light scattering has again showed the affect on total absorbance of light in samples shown in Figure 4.8.





The effects of growth duration on optical absorption and energy bandgap were experimented by depositing several samples for various growth times. Other growth conditions such as the cathodic voltage at 1460 mV, pH and temperature were kept constant. Optical absorption curves of these as-deposited samples are shown in Figure 4.9. The energy bandgap of these samples were slightly higher than the reported values of 2.42 eV due to being dark yellow in colour.

The heat-treated electrodeposited samples had an energy bandgap of 2.42 eV, the similar value as reported in the literature is shown in Figure 4.10. Excellent uniformity and adhesivity in the layers were observed and as the growth duration increased, higher absorbance was noticed due to the increasing darker colour in the layers.



Figure 4.9: Optical absorption curves of as-deposited ED-CdS layers grown for various durations, V_g was kept at a cathodic voltage of 1460 mV.



Figure 4.10: Optical absorption curves of heat-treated ED-CdS layers for various growth times, V_g was kept at a cathodic voltage of 1460 mV.

4.2.2.5 Scanning Electron Microscopy (SEM)

SEM images are used to identify the surface morphology of the ED-CdS thin film layers. Figure 4.11 shows SEM images of CdS layers grown for 40 minutes. After heat treatment, the CdS layers became more cemented, covering the substrates more uniformly as shown in Figure 4.11(b).



(a) As-deposited (b) heat-treated

Figure 4.11: SEM topography images of CdS layers grown at 1460 mV cathodic voltage for 40 minutes.

SEM images of ED-CdS grown for a longer duration, 60 minutes are shown in Figure 4.12, and indicate a larger grain size than the samples grown for 40 minutes as shown in Figure 4.11. More grain coalescing is also evident here. Again, after the heat-treatement the cementing effect occurs and is shown in Figure 4.12(b). At a magnification of 60,000, CdS layers seem to completely cover the glass/FTO substrates but still leaving gaps in between layer grains.



(a) As-deposited

(b) Heat-treated

Figure 4.12: SEM images of CdS layers grown at 1460 mV cathodic voltage for 60 minutes.

A high-resolution SEM image at a magnification of 120,000 is shown in Figure 4.13. Gaps between grains are clearly visible in the CdS layer, these gaps create leakage paths once these layers are used to fabricate solar cells. These images also revealed that the larger grains consists of much smaller grains (~25 nm), and therefore exhibit a cauliflower type surface morphology.



Figure 4.13: High resolution SEM images showing the topography of heat-treated CdS layers electrodeposited at 1460 mV (with the courtesy of collaborators at Uni. of Durham).



Figure 4.14: Cross sectional SEM image of glass/FTO/CdS layers showing the thickness and variations in surface roughness (with the courtesy of collaborators at Uni. of Durham).

It is also shown from the cross sectional SEM image in Figure 4.14, the surface curvature of CdS layer correlates to the surface variations of the FTO layer. This image shows the thickness of CdS layer grown for 1 hour to be \sim 140 nm. The various layers featured in a high magnification SEM image such as Figure 4.14 are detailed in section 3.3.4 in Chapter 3.

4.2.2.6 Energy Dispersive X-rays (EDX)

EDX characterisation was conducted to identify the elemental materials, which make up these thin film layers. EDX spectra of ED-CdS produced from a Na containing solution shows the presence of Na (Figure 4.15 a). However, ED-CdS from the current study, which has no Na, shows no presence of Na among EDX spectra. Once the CdTe based solar cells are made from good quality CdS layers without containing Na, it is expected to produce solar cells with better conversion efficiencies.



Figure 4.15: EDX spectra of ED-CdS from two different electrolytes; (a) from Na containing electrolyte (Na₂S₂O₃) [20] and (b) from the current study using (NH₄)₂S₂O₃ as the Na free S source.

4.2.2.7 Atomic Force Microscopy (AFM)

The surface scan images from AFM show that the heat-treated layers (Figure 4.16 b) are more uniform than as-deposited (Figure 4.16 a) thin film CdS layers. This is similar to the SEM image results of Figure 4.11 and Figure 4.12, after heat-treatment the ED-CdS layers became more uniform.



(a) As-deposited(b) heat-treatedFigure 4.16: AFM images showing ED-CdS surface morphology of as-deposited and heat-treated CdS layers grown at 1460 mV.

The AFM image in Figure 4.17 shows the surface variation of the sample measured. A sample of heat-treated ED-CdS grown at 1460 mV cathodic voltage was characterised using AFM. A surface variation of ± 70 nm was recorded, indicating an improvement of surface variation as compared to the layers, which was ± 105 nm as shown in Figure 4.18.



Figure 4.17: AFM images showing the surface variations of heat-treated CdS layers grown at 1460 mV for a duration of 1 hour.



Figure 4.18: AFM image showing the surface variation of glass/FTO substrate for comparison reasons.

3D-AFM phase images demonstrated highly ordered and tightly packed CdS nano-rods oriented perpendicular to the glass/FTO substrates as shown in Figure 4.19. The diameter of nano-rods are ~20 nm in agreement with the grains shown by the high resolution SEM image as shown in Figure 4.13. The large phase shift in Figure 4.13 indicates the presence of voids between hard CdS rods. The gaps between nano-rods lead to the formation of pinholes, which will in turn reduce the performance of PV devices made from these materials, therefore these gaps need to be minimised.



Figure 4.19: 3D-AFM tapping mode phase image of ED-CdS grown at 1460 mV cathodic voltage on glass/FTO substrate (with the courtesy of collaborators at Institute of Org. Catalysis & Electrochemistry, Kazakhstan).

4.2.2.8 Raman Spectroscopy



Figure 4.20: Raman spectra of (a) bulk CdS and (b) synthesised CdS nanoparticles in the range of 200 to 700 cm⁻¹ [27].

Figure 4.20 Shows Raman spectra of CdS bulk and nanoparticles as published in reference [27]. CdS is identified in the literature by the two peaks mostly in between $300 - 305 \text{ cm}^{-1}$ and $600 - 606 \text{ cm}^{-1}$ [28]. These represent the first and second order longitudinal optical phonons (1LO) and (2LO) respectively [19]. Defect free CdS materials only have these two peaks [29,30].

The observation of the two peaks at 301 cm⁻¹ and 606 cm⁻¹ from the CdS material grown at a cathodic voltage of 1460 mV is shown in Figure 4.21 and indicates this material is defect free and comparable with other high quality CdS. 1LO and 2LO are clearly within the acceptable range as reported in the literature [31]. So the Raman finger printing method for materials also confirms the high quality of the ED-CdS layers fabricated under this programme. The samples from this study had the same two peaks, indicating the layers were CdS.



Figure 4.21: Raman spectra of heat-treated ED-CdS grown at 1460 mV cathodic voltage on glass/FTO substrate, with peaks at 301 and 606 cm⁻¹ (with the courtesy of collaborators at Uni. of Leeds).

4.2.3 Summary and results of the electrodeposited CdS layers

Electrodeposition of CdS thin film layers was carried out to produce semiconductor quality window layers to use in fully electrodeposited solar cells. Chemical precursors, $CdCl_2$ and $(NH_4)_2S_2O_3$ were used in the electrodeposition to produce high quality CdS layers. An acidic aqueous electrolyte in a simple 2-electrode configuration was used in this study. The vital growth parameters such as deposition temperature, pH value, and growth voltage were optimised. The electrodeposited CdS layers were n-type in electrical conductivity, hexagonal polycrystalline in structural make up and have an energy bandgap of 2.42 eV. EDX spectrum showed the absence of Na in the CdS layers from this study, which is due to the use of a sulphur source free from Na as expected. SEM cross sectional images show a surface variation similar to that of the FTO layers, while high magnification SEM topography show cluster like formations on the surface with some visible gaps. It was also observed that 3D-AFM scans of ED-CdS layers produced under this programme consists of nano-rods with gaps in between. This observation has the potential to cause a reduction in performance once the PV devices are fabricated, and will be discussed in Chapter 6.

Raman spectroscopy for the CdS layers also provided further indicators that the CdS layers produced under this study was of high quality. 1LO and 2LO peaks were reported at 301 cm⁻¹ and 606 cm⁻¹ and are comparable to the high quality CdS produced by other semiconductor fabricating methods.

The material properties obtained from various complementary characterisation methods showed the ED-CdS layers from this study are comparable with reported material properties in the literature. Furthermore, the deposited layers were highly adhesive and withstood the heat-treatment required for CdTe solar cells fabrication. The potential for scalability was confirmed by the deposition of larger area samples. Samples with an area up to 15 cm^2 were grown, which was the maximum area possible to grow under the current experimental conditions.

These optimised layers were used in the production of solar cells and the results are presented in Chapter 6.

4.3 Electrodeposition of $CdS_{(1-x)}Se_x$ nano structured thin film layers

4.3.1 Literature review of CdS_(1-x)Se_x layers

Cadmium chalcogenides from the II-VI semiconducting group are a technically important class of materials due to their wide variety of applications in optoelectronic devices [16]. With a direct bandgap and a high coefficient of absorption, a family of these layers can match the maximum span of the solar spectrum [32]. CdS/CdSe structures have a high potential for photonics devices due to their operation in the visible range of the solar spectrum.

There are reports that Se²⁻ containing materials can be electrodeposited in an epitaxial manner with ZnSe as an example [33]. Furthermore, the SHU solar energy group has observed that, their electrodeposited window layers; CdS and ZnS do not have an epitaxial growth orientation, and therefore the objective was to search for such a material. The quality of Se to nucleate in the preferred orientation (111) is to be explored while keeping the qualities of CdS as CdTe grows preferentially on CdS [34]. One of the objectives in this project is to find a good, uniformly grown intermediate bandgap layer to be used in CdS/CdTe solar cells to cover pinholes while avoiding the voids or gaps, which are present in some CdS layers [35]. Such a solar cell device structure has the potential to increase the conversion efficiency.

The ability to engineer the bandgap of semiconductors can be utilised to produce solar cell devices with enhanced conversion efficiencies [36]. To alter the bandgap, electrodeposition can be used to control the ternary element of the semiconductor at a fraction of a cost compared to other expensive semiconductor growth methods [37]. Low-cost chemical bath deposition (CBD) cannot be used for bandgap engineering in semiconductors as it is a batch process [32]. CdS and CdSe semiconductors have bulk bandgaps of 2.42 eV and 1.75 eV respectively and both have n-type electrical conductivity [38]. By incorporating a controlled amount of Se in the CdS layers the bandgap of these layers can be tailored from ~2.42 eV to ~1.75 eV producing CdS_(1-x)Se_x [37]. So in different alloys of this semiconductor, photons from different parts of the solar spectrum get absorbed in order to enhance the absorption, reduce the thermalisation process and hence increase J_{sc}. CdS layers absorb photons in the solar spectrum at ~520 nm, the other parts of such a ternary semiconducting layer absorbs photons from 520 nm - 700 nm [37].

 $CdS_{(1-x)}Se_x$, layers have been grown by different thin film growth methods. CBD [39], spray pyrolysis [16], physical vapour transport [40], chemical vapour deposition [41] and electrodeposition [42,43] are some examples.

Thin film layers with Se ions are possible to be electrodeposited in a layer-by-layer growth mode, as in CdSe and ZnSe [44]. Optimal layers should have high adhesion and the ability to withstand heat treatments of up to $\sim 450^{\circ}$ C if they are to be used in heterojunction thin film solar cells, [43] or in high quality sensory applications.

4.3.2 Characterisation and results of ED-CdS_(1-x)Se_x thin film layers

The $CdS_{(1-x)}Se_x$ bath was prepared as described in section 2.3 in Chapter 2 and a voltammogram was then recorded. A voltammogram for the deposition of $CdS_{(1-x)}Se_x$ was conducted as shown in Figure 4.22, using an ACM-GillAC potentiostat over the range from 100 mV to -2000 mV at a scan rate of 5 mVs⁻¹. When the cathodic voltage is gradually increased until point A (~1200 mV), some S (E_o = 140 mV) and Se (E_o = - 110 mV) ions are deposited on to the glass/FTO substrates. Between points A and B (~1500 mV) Cd ions are gradually included along with S and Se ions. Beyond point B elemental Cd can be deposited in addition to the CdSSe alloy. The rapid increase of current is due to alloy formation, elemental Cd deposition and the electrolysis of water. During the reverse scan, until point C, all above depositions take place producing a

positive current, but at voltages below point C, Cd dissolution occurs and hence a negative current flow between points C and D.



Figure 4.22: 2-electrode cyclic voltammogram of aqueous electrolyte containing 0.30M CdCl₂, 0.03M (NH₄)₂S₂O₃ and 0.03M SeO₃ at pH = 2.00 ± 0.02 and T_g = $85\pm2^{\circ}$ C.

This voltammogram was used to identify the approximate cathodic deposition voltage to be in the range of (1150 - 1650) mV. Material layers were grown at constant cathodic voltages between 1150 mV and 1600 mV in order to grow a stable $CdS_{(1-x)}Se_x$ alloy compound. These were then characterised using XRD and optical absorption in order to optimise the growth voltage. These optimised layers were then studied using other techniques to learn more about the layers.

To achieve optimum quality material, careful and continuous observations were carried out while noting the visible quality, peeling off effects and uniformity of colour. These electrodeposited samples were annealed at 400°C for 20 minutes.





Structural properties of $CdS_{(1-x)}Se_x$ derived from XRD are given in Table 4.3. Crystallite sizes are calculated from the Scherrer equation as given in section 2.3 in Chapter 2. Grain sizes vary from (27 – 66) nm. Presence of CdO_2 peak in the $CdS_{(1-x)}Se_x$ samples was also observed for samples grown for one hour duration.

for heat-treated	ated ED-CdS _{$(1-x)$} Se _x layers deposited at 1380 mV cathodic voltage.						
JCDS ref.	2θ (Degrees)		Lattice spacing d(Å)		Crystallite size	FWHM	h k l
	OV	RV	OV	RV	D (nm)	(rad)	
00-040-0838	24.03	24.56	3.702	3.620	65.3	0.130	100
00-049-1490	25.57	26.09	3.482	3.412	65.5	0.130	002
00-050-0721	27.27	27.53	3.270	3.237	43.8	0.195	101
00-049-1459	39.47	36.34	2.282	2.247	27.2	0.325	102
00-050-0721	42.26	42.99	2.138	2.102	45.7	0.195	110
00-050-0720	45.28	46.89	2.003	1.936	34.6	0.260	103

Table 4.3: Summary of observed values (OV) and reported values (RV) of XRD data for heat-treated ED-CdS_(1-x)Se_x layers deposited at 1380 mV cathodic voltage.

1.824

28.1

0.325

200

00-050-0720

49.46

49.34

1.831

The optimised samples of $CdS_{(1-x)}Se_x$ thin films show more of a balance in the S and Se ratios (S = 0.48 and Se = 0.52) as in Figure 4.23, and are matched to the hexagonal structure from the JCDS data sheets as given in Table 4.3 [40]. The films, which were grown at 1380 mV, were polycrystalline hexagonal structure, when grown for longer time, the peaks were more prominent in the (100) preferred orientation. Mariappan [45] reported a similar result in 2012.

4.3.2.2 Photoelectrochemical (PEC) cell

Photoelectrochemical (PEC) cell measurements were conducted to determine the electrical conductivity type of the $CdS_{(1-x)}Se_x$ layers.

As with CdS and CdSe layers, $ED-CdS_{(1-x)}Se_x$ layers were always n-type in electrical conduction as reported by Murali in 2010 [42]. The results are presented in Figure 4.24 and the values are listed in Table 4.4.



Figure 4.24: PEC results of heat-treated ED-CdS_(1-x)Se_x layers grown from an aqueous electrolyte in the range of (1150 – 1460) mV cathodic voltage showing the n-type electrical conduction of CdS_(1-x)Se_x.

Cathodic voltage (mV)	PEC signal (mV)	Conduction type
1150	-30	n
1250	-14	n
1310	-27	n
1360	-22	n
1380	-20	n n
1390	-14	n
1400	-30	n
1410	-24	n .
1450	-36	n
1460	-38	n

Table 4.4: PEC signal for heat-treated $CdS_{(1-x)}Se_x$ layers deposited at various cathodic voltages.

PEC results for heat-treated ED-CdS_(1-x)Se_x samples showing n-type electrical conduction. These results are graphically shown in Figure 4.24.

4.3.2.3 Optical absorption (OA)

The energy bandgap of the thin film semiconductor was analysed using a Cary 50 UV-VIS spectrophotometer.





Optical absorption curves of ED-CdS_(1-x)Se_x layers showed clear absorption edges and high absorption lines. They are good indications of high quality optical material [37]. The optical bandgap of the layers varied, depending on the S and Se ion ratios as expected. The layers with good physical properties and the ones that responded well to the heat treatment were cathodically deposited at 1380 mV. Such layers have better optical absorption properties and produce a bandgap of 2.10 eV as shown in Figure 4.25.

4.3.2.4 Scanning Electron Microscopy (SEM)

A FEI NOVA nano-SEM 200 Field Emission Gun with accelerating voltage of 20 kV was used to obtain images of the $CdS_{(1-x)}Se_x$ surfaces. Cross sectional images were also obtained to estimate the $CdS_{(1-x)}Se_x$ film thickness. The SEM was also used in conjunction with an Oxford Instruments EDX analysis system to obtain elemental spectra for the thin films deposited using different voltages.



(a) $CdS_{(1-x)}Se_x$

(b) CdS

Figure 4.26: A typical SEM topography of optimum quality as-deposited $CdS_{(1-x)}Se_x$ and CdS layers.

Many morphological variations were observed when the growth time was gradually changed. When the deposition time was varied at a growth voltage of 1380 mV cathodic voltage from 20 minutes to 60 minutes, the morphology evolved from nano-wires, nano-tubes to nano-mesh like features. This clearly shows that growth time, along with effective annealing, can modify the surfaces of $ED-CdS_{(1-x)}Se_x$ layers at a nano level. This is potentially a suitable material for nano technology, which can be

electrodeposited at a low temperature, lowering the cost of producing it further. Figure 4.26 shows a typical as-deposited $CdS_{(1-x)}Se_x$ layer and CdS layer. Other morphological layers are shown in, Figure 4.27: (a), (b), (c) and (d), this behaviour of $CdS_{(1-x)}Se_x$ was previously reported only by one growth technique at a very high temperature of 800°C [40]. A $CdS_{(1-x)}Se_x$ sample which was grown for 2 hrs shows more uniform growth Figure 4.27 (d). No pinholes were visible due to better wetting qualities of the $CdS_{(1-x)}Se_x$ layers. However, the samples grown for 2 hrs were very dark in colour indicating a much higher absorption leaving little light to be absorbed by the CdTe layer. Figure 4.28 is an SEM cross sectional image showing the complete covering of the whole glass/FTO substrate, and clearly shows no loosely bound particles.



Figure 4.27: Various SEM topographies of evolving $CdS_{(1-x)}Se_x$ with nano structures; (a) Nano-wires at 20 min, (b) Nano-tubes at 40 mins, (c) Nano-mesh at 60 mins and (d) uniformly covered layer after 2 hr growth.

Morphological evolution from nano-wires, nano-tubes to nano-sheets, covering the whole surface without pinholes is observed. This is similar to the results of Kim (2009) who used physical vapour transport to grow $CdS_{(1-x)}Se_x$ at 800°C [40].



Figure 4.28: Cross sectional SEM of $ED-CdS_{(1-x)}Se_x$ layers (with the courtesy of collaborators at Uni. of Durham).

The cross sectional image from SEM shows (Figure 4.28) a uniform layer growth with possible voids between FTO and $CdS_{(1-x)}Se_x$ layer. To produce high performing solar cells these voids should be mitigated. The sample shown was grown for 2 hours and has a thickness of ~500 nm.

4.3.2.5 Energy Dispersive X-rays (EDX) spectroscopy

To identify the elemental understanding of the makeup of the layers, EDX characterisation was carried out for elemental analysis of the ED-CdS_(1-x)Se_x thin film layers. Figure 4.29 shows the elemental make up of CdS_(1-x)Se_x showing the presence of Cd, S and Se along with several other elements which come from the glass/FTO substrate. Furthermore, element Na, which is reported to be harmful for CdTe based solar cells is not present. Na was avoided by using chemical precursors, which were free from Na.



Figure 4.29: EDX spectra showing the presence of Cd, S and Se in the electrodeposited thin film layers.

4.3.2.6 Atomic Force Microscopy (AFM)

AFM studies were carried out to analyse the surface variations of the $CdS_{(1-x)}Se_x$ thin film layers using a Nano Scope3, set on semi-contacting mode. The scan of the surface variations, as well as the topography of $CdS_{(1-x)}Se_x$ layers were recorded to understand the finished qualities of the heat-treated materials.

AFM studies show that the ED-CdS_(1-x)Se_x thin film layers have good surface uniformity in comparison to ED-CdS layers. The surface variation of CdS_(1-x)Se_x layers are more uniform than that of similarly grown CdS layers as shown in Figure 4.17. CdS and CdS_(1-x)Se_x have surface variation of \pm 70 nm and \pm 30 nm respectively according to the AFM surface scans (Figure 4.17 and Figure 4.31).



(a) Peaks and valleys

(b) the surface topography

Figure 4.30: AFM image of a heat-treated $ED-CdS_{(1-x)}Se_x$ thin film layer showing the surface variations.



Figure 4.31: AFM scan showing the surface variation of $ED-CdS_{(1-x)}Se_x$ grown at 1380 mV cathodic voltage for a duration of 1 hour.

The surface variations of $ED-CdS_{(1-x)}Se_x$ was the lowest among the materials under investigation in this project. A surface variation of ±30 nm is shown in Figure 4.31.

4.3.2.7 Raman spectroscopy

Raman spectroscopy was conducted using 514 nm wavelength filter on a heat-treated ED-CdS_(1-x)Se_x grown on a glass/FTO substrate to compare the quality of this material to CdS_(1-x)Se_x grown on borosilicate glass [46]. As shown in Figure 4.32 the peaks reported were a match with the peaks reported by Azhniuk et al [46]. The peaks of 204 cm⁻¹, 275 cm⁻¹, 413 cm⁻¹ and 485 cm⁻¹ from the ED-CdS_(1-x)Se_x layers correspond with the peaks of 204 cm⁻¹, 288 cm⁻¹, 406 cm⁻¹ and 492 cm⁻¹ respectively with the CdS_(1-x)Se_x layers from Azhniuk's work. The close correlation of Raman studies on two different CdS_(1-x)Se_x layers further indicates, ED-CdS_(1-x)Se_x layers are of comparable chemical composition with CdS_(1-x)Se_x layers produced for other applications [47].



(a) $CdS_{(1-x)}Se_x$ on borosilicate glass

(b) $CdS_{(1-x)}Se_x$ on glass/FTO substrate

Figure 4.32: Raman spectra of $CdS_{(1-x)}Se_x$ layers grown on borosilicate [46] and on glass/FTO substrate (this work) for comparative purpose.

4.3.3 Summary of electrodeposition and characterisations of CdS_(1-x)Se_x

 $CdS_{(1-x)}Se_x$ thin films were successfully electrodeposited in an aqueous acidic solution. The layers were annealed to the much-needed higher temperatures for use in CdTe based solar cells. The thin films are n-type in electrical conduction and the optical bandgap of an optimum quality layer is ~2.10 eV. The best $CdS_{(1-x)}Se_x$ layers were deposited at a cathodic voltage of 1380 mV producing layers with excellent adhesivity, reproducibility and a balanced S and Se ion ratio (0.48 and 0.52 respectively). The samples grown were polycrystalline and hexagonal. Samples up to an area of 15 cm² were produced with good surface uniformity. This was the maximum area possible to grow within the current experimental settings. This indicates that this material is very suitable for large area electrodeposition for use in a variety of applications. The chemical composition of ED-CdS_(1-x)Se_x layers is comparable with the CdS_(1-x)Se_x layers produced by other research groups.

Electrodeposited CdS layers on glass/FTO/CdS_(1-x)Se_x had uniformity and growth issues but the deposited CdTe layers on glass/FTO/CdS_(1-x)Se_x substrates were very uniform under the optimised conditions. So structures where the CdS_(1-x)Se_x layers were functioning as buffer layers were not stable. Hence ED-CdS_(1-x)Se_x layers were more suitable as window layers. It was possible to grow CdTe layers to produce all-ED solar cells using CdS_(1-x)Se_x as a window layer with some encouraging initial results. However the use of CdS_(1-x)Se_x as an intermediate layer led to peeling off on the corners during the growth of the third electrodeposited semiconducting layer, ED-CdTe.

Controlling the growth conditions to produce various nano morphologies at a lower temperature is also presented in this report. The evolving morphologies as a function of deposition conditions was observed and reported. The morphology is a function of growth conditions showing nano-wires, nano-tubes and nano-sheets. These morphologies were observed under low temperature growth conditions for the first time. This observation opens the possibility of lower temperature deposition of this nanomaterial.

4.4 References

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Chapter 5. Electrodeposition and optimisation of CdTe absorber layer

5.1 Introduction

Ten years ago, more than 99% of solar cells sold in the world were made from Si [1]. However, within a decade ~15% of solar cells produced in the world are now thin film solar cells [2]. The largest share of the thin film solar cell market belongs to CdTe based solar cells [2]. As indicated in Chapter 1, CdTe based solar cells are the most costeffective amongst all the solar cells. The cost of these solar cells can be further reduced, if the material wastage is reduced. Material wastage is one of the biggest costs in any solar cell manufacturing process. A continuous process such as electrodeposition has low or no wastage costs. Furthermore, cost reduction by increasing the conversion efficiency is targeted by many research groups [3,4]. Within this research group, both these streams to reduce production cost and ways to increase efficiency are being researched.

As elaborated in section 1.7.4 in Chapter 1, the semiconducting material CdTe has suitable properties to make low-cost solar cells. CdTe is also used heavily in other applications due to its good optical absorption qualities [5]. Alloys containing Hg in CdTe are used in infrared sensors and alloys with ZnS are used as X-ray and gamma ray detectors [6]. CdTe can be produced as n-type, i-type or p-type, depending on the doping and growth conditions. This versatile optical material is primarily researched and developed for its use in solar cell applications. About 1.5 μ m of thin film CdTe can absorb more than 90% of the incident solar radiation due to its high absorption coefficient contributed by its optimum energy bandgap and high electron mobility ~1100 cm²V⁻¹s⁻¹ [2]. Therefore, the common use of this compound is by forming a hetero junction with CdS, in a thin film solar cell [2].

The successes in many research laboratories have led to CdTe based solar cells with efficiencies of 18.3% [7] and ~14.5% being produced at laboratory and module levels respectively [8]. First Solar Inc, a manufacturer of CdTe based solar cells has become the industry benchmark for low cost solar modules.

CdTe is produced in both macro area (larger area) and micro area (smaller area) and only large area fabrication has the potential to lower the manufacturing cost of solar cells. The deposition methods of CdTe include non-vacuum methods such as, CVD, spray pyrolysis, printing methods and electrodeposition. In this study electrodeposition, using a 3-electrode configuration was conducted. Detailed description of CdTe based solar cells were presented in section 1.7.5 in Chapter 1.

5.2 Characterisation and results of CdTe thin film layers

A glass substrate with a coated transparent conducting oxide (TCO), is the chosen substrate for most CdTe based solar cells. The substrate used in this project was glass/FTO which has more than 90% transmission, with excellent thermal stability and a low sheet resistance of ~15 Ω/\Box . This low sheet resistance leads to low series resistance once the solar cell is fully processed. Next, the CdTe absorber layer is deposited on an optimized semiconducting window layer to process solar cells. In order to optimise the deposition conditions during the experimental stages, CdTe is deposited on glass/FTO samples for experimental purposes to analyse and characterise the material layers. The layer is electrodeposited for 2-3 hours while varying the growth potential slightly [9]. The Faraday equation was used to estimate the time needed to grow the layer to the required thickness, ~1.5 µm when used in solar cells, and depending on the current density and growth time (t_g) could be about 4-6 hours.

The preparation of an electrolyte containing 1.0M CdSO₄, CdI₂ and TeO₂ was detailed in section 2.4.1 in Chapter 2. The pH value was adjusted to 2.00 ± 0.02 and the temperature was set to 70°C as per the operating guidelines of the saturated calomel electrode [10]. This saturated calomel electrode was modified for several advantages as detailed in section 2.4.1.4 in Chapter 2. To understand the chemical activities of the electrolyte, at several key stages, voltammograms were conducted in the range -100 mV to 1200 mV cathodic potentials at a scan rate of 5 mVs⁻¹. The key stages for recording voltammograms were, before and after the addition of TeO₂ and after the inclusion of CdI₂ for iodine doping. Iodine was added to dope the CdTe layers and to capitalise on the positive effects of infusing this halogen into the ED-CdTe layers [11,12]. It is also expected to provide n-doping and increase the conductivity, leading to a higher collection of current generated at the optimum concentration levels [13]. The voltammogram for CdSO₄ solution after electro purifying for 2 days is shown in Figure 5.1. As this figure shows, no deposition takes place until about 730 mV cathodic voltage as no current density is shown. From this point, elemental Cd starts to deposit and during the reverse potential, elemental Cd is dissolved again at about a cathodic voltage of 730 mV and at lower potentials.



Figure 5.1: 3-electrode cyclic voltammogram of 1.0M CdSO₄ electrolyte with pH = 2.00 ± 0.02 and temperature at 70°C before the addition of TeO₂ and CdI₂ with reference to a modified saturated calomel electrode.

In the electrolyte prepared for electrodepositing of CdTe layers, the reduction of elemental Te begins around 500 mV cathodic voltage. This voltammogram is shown in Figure 5.2. It is observed that the current density starts to increase from the cathodic voltage at point A shown in Figure 5.2. At point B, Cd is deposited along with Te, hence CdTe is deposited between points B and C. After point C elemental Cd deposition with possible hydrogen evolution occurs at the cathode [14]. During the reverse voltammogram at point D, E and F elemental Cd, Cd in CdTe compounds and elemental Te respectively are dissolved back to the electrolyte solution. So the initial range for electrodepositing of CdTe layers can be identified as from 680 mV to 730 mV cathodic potentials. Identifying the initial growth voltages was also aided by some previous work at Sheffield Hallam solar energy laboratory [15].





Several samples of ED-CdTe were produced at different growth voltages for various characterisations. These samples were grown for a growth duration (t_g) of 2 hours.

5.2.1 X-ray diffraction (XRD) method

In order to identify the material phases and the structure of the ED-CdTe layers grown in this project, the samples were subjected to XRD characterisation as described in section 2.2 in Chapter 2.

All the as-deposited samples were identified as CdTe with a cubic, (111) preferred orientation. Other weak phases were also observed, depending on the growth voltages. As shown in Figure 5.3, the other observed peaks were all cubic, (200), (220), (222), (331) and (420). These other peaks observed were at $2\theta = -27.8^{\circ}$, -39.7° , -46.9° , -63.2° and -65.0° . They were identified from the JCPDS 01-075-2086. The mixed phased (Mixed phase) represented in Figure 5.3 can be linked with JCPDS 00-036-0890 and 01-076-1007 as a mixture of Cadmium Tellurium Oxide and Cadmium Tellurate. Similar results were reported in the literature by Bonilla *et al* [16] and Romeo *et al* [17]. The peak at 37.9° is attributed to FTO as these samples were grown for two hours and can be compared with Figure 4.3 on Chapter 4.

The best crystallinity was identified for a sample grown at a cathodic voltage of 698 mV.



Figure 5.3: XRD peaks of as-deposited CdTe layers at various V_g and $t_g=2$ hours.

Upon heat-treating the CdTe samples at 450° C for 15 minutes, the crystallinity of the deposited layers increased and the peak at C(111) became more prominent. The peaks of non-optimum quality samples collapsed or became less intense. This may have been due to the material loss during heat treatment process via sublimation. XRD measurements indicated the samples grown at a cathodic voltage of 698 mV have the best crystallinity as shown in Figure 5.4.



Figure 5.4: XRD peaks of heat-treated CdTe layers grown at various V_g and $t_g=2$ hours.

The main diffraction peak was at $2\theta = 23.64^{\circ}$ which corresponded to preferred orientation along the (111) plane of a cubic phase as identified by JCPDS of 01-075-2086.

The samples grown at 698 mV cathodic voltage has the highest intensity of this prominent peak as shown in Figure 5.5. This observation further indicates the optimum ED-CdTe layers are grown at 698 mV cathodic voltages. The mixed phase containing a mixture of Cadmium Tellurium Oxide and Cadmium Tellurate was also almost diminished but the FTO peak was still visible at 698 mV cathodic voltage in these heat-treated ED-CdTe samples.






5.2.2 Photoelectrochemical (PEC) cell



This pattern, electrodeposition of p-type semiconductors at lower cathodic voltages and electrodepositing n-type semiconductors at cathodic voltages was observed under three

different sets of experiments for heat-treated CdTe samples. These repeated tests increase the probability of reproducibility of reported PEC results.

Electrical conductivity of the deposited CdTe samples was tested using the PEC cell experiment as detailed in section 2.2 in Chapter 2. The results are shown in Figure 5.6 and Table 5.1. As-deposited samples were all n-type in electrical conductivity while samples deposited at a cathodic voltage of 693 mV or lower cathodic voltages were p-type when heat-treated. At lower cathodic voltages p-type electrical conductivity represents Te richness in the layers.

At $V_g = 698$ mV cathodic voltage, the material is stoichiometric and therefore shows the best crystallinity, and the electrical conduction is close to i-type. When the material becomes Cd-rich above 698 mV cathodic voltage, the material becomes n-type in electrical conduction. Below 698 mV cathodic voltage, the material layers become Terrich and hence become p-type in electrical conduction.

In this work, the presence of iodine (I_2) also affects the deposition of the material layer. If iodine replaces Te atoms in some of the CdTe molecules, this will act as n-type dopant. Therefore, the materials will tend to be more n-type as shown in this work. The overall conductivity type depends on both effects; the amount of iodine in the film and the composition of CdTe layer. The scan was conducted from a cathodic voltage of 688 mV to 706 mV to identify the possible i-point, which can be utilised to fabricate p-i-n devices as discussed in section 1.7 in Chapter 1. Since this electrolyte is doped with CdI₂, a natural tendency to produce n-type CdTe layers was observed. This was also observed in the literature [11].

Table 5.1 displays a summary of electrical conductivity with reference to the growth voltages for both as-deposited and heat-treated samples.

Growth voltages	AD sa	mples	HT sa	mples
(mV)	PEC value (mV)	Conduction type	PEC value (mV)	Conduction type
688	-101	\mathbf{n} . The second se	15	. p
689	-154	n	5	p
690	-99	n	-51	n
691	-109	n ^a	22	р
692	-132	n	-8	n
693	-134	n	9	p
694	-125	n	-10	n
695	-116	n	-2	n
696	-140	n	-26	n
697	-84	n	-76	n
698	-125	n	-13	n
699	-114	n	-60	n
700	-72	n	-32	n
701	-86	n	-28	n
702	-146	n	-14	n
703	-102	n	-33	n
704	-90	n	-32	n
705	-91	n	-33	n n
706	-136	n	-108	n

Table 5.1: Summary of PEC results showing the electrical conductivity of ED-CdTe samples.

5.2.3 Optical absorption

Evaluation of the bandgap of deposited optical thin film layers was carried out by using optical absorption as shown in Figure 5.7. The cathodic voltage growth range was further reduced once more optimised samples were identified. As shown in Figure 5.7, amongst the as-deposited samples, the sample deposited at 698 mV cathodic voltage had the best bandgap (1.48 eV) and a sharper absorption edge. The Stern relationship as described in section 2.2 in Chapter 2, was used to calculate the bandgap of both as-deposited and heat-treated samples. The square of absorbance versus photon energy was plotted, and used to estimate the bandgap from the absorption edge. It is evident in Figure 5.7 and Figure 5.8 due to scattering, the complete absorption was prevented. In heat-treated samples as shown in Figure 5.8, the absorption edge sharpened and the bandgap decreased to match closer to the reported bandgap values of CdTe. This is attributed to the materials becoming optimum quality by way of reducing intrinsic defects and improving crystalline quality.



Figure 5.7: Optical absorption curves of as-deposited ED-CdTe layers grown at various growth voltages on glass/FTO substrates.



Figure 5.8: Optical absorption curves of heat-treated ED-CdTe layers grown at various growth voltages on glass/FTO substrates.

Table 5.2 shows the summary of the bandgaps estimated for as-deposited and heattreated CdTe layers deposited at different voltages. It can be seen that after the heattreatment the ED-CdTe thin film layers obtained better optical properties.

$V_{g}(mV)$	Bandgap of AD samples (eV)	Bandgap of HT samples (eV)
695	1.50	1.46
697	1.49	1.45
698	1.48	1.45
699	1.49	1.45
701	1.50	1.45

Table 5.2: Bandgap of electrodeposited CdTe samples for various growth voltages.

Scanning Electron Microscopy (SEM) 5.2.4

It is important to understand the surface topography of ED-CdTe layers as this is where the back contact will be fabricated. SEM images of as-deposited and heat-treated samples are shown in Figure 5.9, these images have a magnification of 60,000 and show the granular nature of the films.



(b)

Figure 5.9: Typical SEM monographs of CdTe layers grown on glass/FTO substrates (a) for as-deposited and (b) for heat-treated layers ($t_g = 4$ hrs).

It is clear the grain sizes increase after heat treatment. The largest grains of as-deposited CdTe are ~300 nm and that of heat-treated layers are ~1000 nm. These values are comparable to the grain sizes reported in the literature [18].



Figure 5.10: A high resolution SEM image of CdTe layers showing the gaps between the grains ($t_g = 4$ hrs) (with the courtesy of collaborators at Uni. of Durham).

Figure 5.10 shows an SEM image of a heat-treated ED-CdTe layer with a higher magnification (150,000). It can be identified from this image, that coalescing small grains of the size ~100 nm form the large agglomerations. The appearance is cauliflower type and the gaps between the agglomerations are clearly visible. These gaps are detrimental for device fabrication, since the back contact could short circuit the device through these narrow gaps. Either these gaps should be removed or blocked using an insulating layer to prevent the back contact material short-circuiting the device in order to fabricate produce good PV devices.



5.2.5 Energy Dispersive X-rays (EDX) spectroscopy

Figure 5.11: EDX spectra for heat-treated CdTe samples showing the presence of elemental Cd and Te.

Energy dispersive X-ray spectroscopy provided a qualitative elemental assessment of the deposited CdTe layers. All the samples showed the presence of Cd and Te with clearly identifiable peaks as in Figure 5.11.

5.2.6 Atomic Force Microscopy (AFM)



(a)



Clear

Figure 5.12: A typical AFM scan images of a heat-treated ED-CdTe layer deposited on glass/FTO substrates at 697 mV cathodic voltage. (a) AFM Peaks and valleys representation (b) surface variation representation

Several samples were subjected to an AFM investigation to understand the surface variations of the ED-CdTe thin film layers. Due to the rough surface variation, the AFM was used in tapping mode to prevent damages to the AFM tips and to produce better images. Figure 5.12(a) shows the surface variation topography of ED-CdTe layers, these high surface variations are also seen in Figure 5.12(b) and are in the order of ± 100 nm.

The large grain sizes visible in the SEM images (Figure 5.9) make the surface finish of the CdTe layers rough as shown in Figure 5.12. The peaks to valleys surface variation of ED-CdTe is shown to be in the order of ~200 nm due to the large grain sizes.

5.2.7 Raman spectroscopy

The molecular structural properties of ED-CdTe layers produced under this study were analysed and compared with the use of Raman spectra analysis. The phases of CdTe, Te and Cd can be identified by this non-destructive technique. Heat-treated ED-CdTe samples grown at 698 mV cathodic voltage were characterised at room temperature using an excitation wavelength of 514 nm to produce Raman spectra as shown in Figure 5.13. The changes in Raman spectra indicate the changes in molecular structure. In comparison to the Raman spectra of heat-treated ED-CdTe layer, the molecular structure was modified by chemical etching as shown in (ii) and (iii) curves of Figure 5.13 [19]. The prominent peak at 122 cm⁻¹ represents pure tellurium [20]. The two peaks identified at 142 cm⁻¹ and 164 cm⁻¹ are related to CdTe layers and these correspond to the fundamental transverse (1TO) and longitudinal optical phonons (1LO) respectively [20]. The Raman technique can be used to identify CdTe layers which are Cd-rich [19]. All these peaks are similar to those reported by other researchers in the field [21]. As it can be seen in the curves (ii) and (iii) of Figure 5.13, A1(Te) peak becomes less prominent with longer etching. As Amirtharaj indicated [19] this technique can indicate a research direction to remove the excess Te from CdTe and possibly, to make CdTe layers Cd-rich.



Figure 5.13: Raman spectra of (i) heat-treated ED-CdTe layer grown at 698 mV cathodic voltage, (ii) ED-CdTe after 2-minute basic etching and (iii) ED-CdTe after 4-minute basic etching.

5.3 Discussion of electrodeposition of CdTe thin film layers

The electrodeposition of CdTe layers in the 3-electrode configuration was successfully conducted by using a modified saturated calomel electrode. While it is possible to produce p-type, i-type and n-type ED-CdTe layers, this study found that the best quality CdTe layers grown were n-type in electrical conduction. Iodine doping in this study also encourages n-type electrical conductors and it is also reported by Lincot, that in cathodic deposition, n-type semiconductors are more likely to get deposited since electron transport is involved [22]. Optical absorption confirmed that the samples grown at 698 mV cathodic voltage had the best absorption and the optimum bandgap comparable with that of bulk CdTe ($E_g = 1.45$ eV). XRD studies showed that CdTe layers electrodeposited at a cathodic voltage of 698 mV had the best crystallinity and were cubic in structure. SEM images indicated that CdTe grains varied in sizes from ~300 nm to ~1000 nm grown on glass/FTO substrates. This technique with high-resolution images highlighted that there are some gaps visible between the grains of

ED-CdTe. From the high resolution SEM images it was also observed the larger agglomerated grains of ~1000 nm consist of smaller grains of ~ 100 nm. The surface molecular structure of heat-treated, chemically etched ED-CdTe layers contain some Te-richness and this can be controlled by an optimised chemical etching process to prepare a more Cd-rich surface as required to produce better PV devices. The molecular structural properties of ED-CdTe layers found to be comparable with CdTe layers reported in the literature by Raman spectra studies. This technique can be further explored to aid in producing Cd-rich ED-CdTe surfaces, which are more conducive to produce better performing PV devices.

The gaps in CdTe thin film layers are not conducive to solar cells and should be minimised, blocked or passivated to improve the quality of solar cells made from this material. All ED-CdTe solar cells need uniformly grown material layers without spaces, otherwise back contact metal can short the devices. All-ED solar cells fabricated using these optimised CdTe thin film layers are presented in Chapter 6.

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6.1 Introduction

CdTe based solar cells are currently the most cost effective solar cells in the market. The cost of these solar cells has been below 1 \$/W since 2010 [1]. This achievement of low-cost CdTe solar cells is remarkable in such a short research period compared to the long established research into Si solar cells, which have been in commercial production for several decades with a mature understanding of the materials and devices. CdTe solar cells have the potential to increase the efficiency and the production cost can be reduced further [2].

A fully-electrodeposited production path presents considerable potential to improve efficiency, and more importantly to reduce the manufacturing cost, due to the low use of materials and energy consumed during the production process. Several different structures have been experimented, researched, and analysed for their advantages and disadvantages.

A detailed introduction to CdTe solar cells and the electrodeposition process was given in Chapters 1 and 2. This programme covered several issues at a very deep level; the mastering of electrodepositing of semiconductors from raw materials, characterisation and optimisation of these semiconductors, and experimenting with several new solar cell structures proposed by Sheffield Hallam University solar energy research group. This chapter presents the results of fully electrodeposited CdTe based solar cells fabricated under this programme.



Figure 6.1: The structure of standard solar cell, glass/FTO/CdS/CdTe/Cu-Au fabricated in SHU solar energy group, where all the semiconducting layers are produced by electrodeposition method.

All the electrodeposited solar cells in this research have several parameters, which were kept as constants. They are: the substrates of glass/FTO and their preparation, the 3electrode configuration for electrodepositing the CdTe absorber layer, the thickness of the absorber layer ~1.5 µm controlled using the growth time and deposition current density, the CdCl₂ treatment process, the surface etching process to prepare the CdTe surface finish to be Cd-rich and the metallisation of back contact. All these parameters are detailed in section 2.4 in Chapter 2. The variables investigated were: chemical precursor combinations, various growth conditions of the semiconductors, different buffer layers, window layers and the optimised deposition conditions for the CdTe absorber layer. A vigilant approach was maintained to avoid any impurities contaminating the electrolytes. As Denison reported in 1994, Ag and Na can have a drastic detrimental effect on the efficiency of CdTe based solar cells, hence a Ag/AgCl reference electrode was not used [3]. Instead, a Hg/HgCl saturated calomel electrode was used after replacing the KCl solution with CdCl₂ electrolyte in the outer jacket of the reference electrode to reduce K ion contamination. The group I element K, must have the same detrimental effect as Na, which drastically reduce the efficiency of CdS/CdTe based solar cells [3,4].

6.2 Solar cells using ZnS layers

Under this investigation, ED-ZnS layers of both n-type and p-type were observed. However, only the n-type ZnS layers were used to fabricate solar cells as the p-type ZnS layers were not stable under the high temperature heat-treatment as also identified by Lincot [5]. The ZnS layers had an energy bandgap of \sim 3.80 eV, were amorphous in structure and n-type in electrical conduction. These n-type layers were used to fabricate all-ED CdTe based solar cells.

This ZnS optical semiconductor was utilised in CdTe based solar cells in two different ways, depending upon its function in the device; (i) the ZnS was used as a buffer layer in CdS/CdTe solar cells with the structure of glass/FTO/ZnS/CdS/CdTe/Cu-Au (back contact) and (ii) as a window layer in CdTe solar cells with the structure of glass/FTO/ZnS/CdTe/Cu-Au (back contact). In Chapter 3, the results of growth and characterisation of ED-ZnS layers were reported. The optimum growth conditions for the ZnS layers were 1475 mV cathodic voltage, pH value 2.00 ± 0.02 and at a temperature of $85\pm2^{\circ}$ C.

The conditions of ED-ZnS needed for use in solar cells can be marginally different to that of the optimum quality ED-ZnS thin film layers. To investigate this, all-ED CdTe solar cells were fabricated by varying the ZnS growth voltage near to its optimum value, while keeping the other conditions constant. The basic solar cells using ZnS and CdTe with the structure, glass/FTO/ZnS/CdTe/Cu-Au (back contact) were fabricated. After recording the device parameters of these devices, only the primary parameters of solar cells (V_{oc} , J_{sc} , FF and efficiency) produced using ZnS layers grown at different voltages are shown in Figure 6.2.

 V_{oc} , J_{sc} , FF and efficiency were plotted as a function of the growth voltage of ZnS. While the optimum growth voltage for ZnS is at a cathodic potential of 1475 mV, the best quality solar cells were produced at a cathodic voltage of 1480 mV. This may be due to the possibility of a higher presence of Zn at higher cathodic voltages, as shown by EDX studies in Chapter 3.



Figure 6.2: The performance curves of all-ED CdTe based solar cells produced with various ZnS growth voltages, ED-CdTe at $V_g = 697$ mV and $t_g = 4$ hours with the structure of glass/FTO/ZnS/CdTe/Cu-Au (back contact).

The effect of growth duration for the ZnS layers on the performance of CdTe solar cells was investigated. All-ED solar cells were fabricated with ZnS layers grown for different durations while keeping all other fabrication conditions constant. Figure 6.3 shows the primary parameters for these devices. V_{oc} , J_{sc} , FF and efficiency were plotted as a function of growth durations of ZnS.



Figure 6.3: The performance curves of all-ED CdTe based solar cells produced with various ZnS growth times, ED-CdTe at $V_g = 697$ mV and $t_g = 4$ hours with the structure of glass/FTO/ZnS/CdTe/Cu-Au (back contact).

While the solar cell fabricated with a ZnS layer grown for 30 minutes had the best fill factor, other solar cell parameters, such as V_{oc} , J_{sc} and efficiency were best for solar cells fabricated with the ZnS layers grown for 45 minutes. The corresponding thickness values of ZnS layers are shown in Table 6-1.

Growth times of ZnS layers	Thickness	Growth rate
(minutes)	(nm)	$(nm min^{-1})$
15	33	2.20
30	62	2.07
45	86	1.91
60	111	1.85

Table 6-1: Thickness of ED-ZnS layers grown for different durations.

The thickness of ZnS layer used to produce the best solar cell was \sim 86 nm, this was calculated using the Faraday equation as detailed in section 2.3 in Chapter 2.

6.2.1 Solar cells using ZnS as buffer layers

When a ZnS layer is used in a CdS/CdTe solar cell, i.e., before the depositing of the CdS layer, ZnS is utilised as a buffer layer. The structure of the solar cell is glass/FTO/ZnS/CdS/CdTe/Cu-Au (metal contact). The device parameters of the best solar cell using ZnS layers as a buffer layer is shown in Figure 6.4. The performance parameters for this device were $V_{oc} = 620 \text{ mV}$, $J_{sc} = 27.2 \text{ mAcm}^{-2}$, FF = 0.36 and an efficiency of 6.1%. The improvement in fill factor was noticeable when compared with the device parameters of ZnS/CdTe solar cells, where ZnS was used as the window layer. Series resistance and shunt resistant of this device was calculated to be 12.2 Ω cm⁻² and 5294 Ω cm⁻² respectively.



Figure 6.4: Device parameters of the best PV device with the structure of (glass/FTO/ZnS/CdS/CdTe/Cu-Au) using ZnS as a buffer in solar cell. The growth conditions for the semiconducting layers were, ZnS; $V_g = 1480 \text{ mV}$, $t_g = 30 \text{ mins}$, CdS; $V_g = 1455 \text{ mV}$, $t_g = 20 \text{ minutes}$, and CdTe; $V_g = 697 \text{ mV}$, $t_g = 4 \text{ hours}$.

Under optimum growth conditions, CdS layers grow uniformly on the heat-treated ZnS layers. The ZnS layers were heat-treated at 350°C for 10 minutes. These solar cells displayed good surface uniformity throughout the growth of all three semiconductors

used in these devices and they withstood the high temperature heat-treatment of the CdTe layers before the surface etching process.

6.2.2 Solar cells using ZnS as window layers

The ZnS layers were used in CdTe based solar cells, having a structure of glass/FTO/ZnS/CdTe/Cu-Au (metal contact). The electrodeposition of CdTe layers directly on the ZnS layer was only possible for heat-treated ZnS layers. Device parameters for the best solar cell using ZnS layers as a window layer are shown in Figure 6.5. The device parameters for this PV cell were $V_{oc} = 576$ mV, $J_{sc} = 30.8$ mAcm⁻², FF = 0.33 and an efficiency of 5.9%. The improvement of current density was noticeable when compared with the device parameters of CdTe solar cells, where ZnS was used as the buffer layer. Series resistance and shunt resistant of this device was calculated to be 13.2 Ω cm⁻² and 3805 Ω cm⁻² respectively.



Figure 6.5: Device parameters of the best PV device with the structure of (glass/FTO/ZnS/CdTe/Cu-Au) using ZnS as a window layer in a CdTe solar cell. The growth conditions for semiconducting layers were, ZnS; $V_g = 1480 \text{ mV}$, $t_g = 45 \text{ min}$ and CdTe; $V_g = 697 \text{ mV}$ and $t_g = 4$ hours.

6.3 Solar cells using CdS layers

The device configuration glass/FTO/CdS/CdTe/Cu-Au (back-contact) has been fabricated by several groups as discussed in section 4.2 in Chapter 4. During this investigation, all-ED CdTe based solar cells were fabricated and it was expected that this device structure would produce good device parameters, as CdS enhances the performance of CdTe based solar cells [6]. For use as a window layer, CdS was electrodeposited from a different chemical precursor combination. This chemical precursor combination did not contain any Na to avoid Na contamination, which can be detrimental in CdTe solar cells [4]. ED-CdS layers with an energy bandgap of ~2.42 eV, having a polycrystalline hexagonal structure and n-type in electrical conduction were used to fabricate all-ED CdTe based solar cells.

In Chapter 4, growth and characterisation details were presented for ED-CdS. The optimum growth conditions were at a cathodic voltage of 1460 mV, the pH value was optimised to be 2.00 ± 0.02 and the temperature was kept at $85\pm2^{\circ}$ C.

The growth voltage of CdS for use in solar cells can be slightly different to that of optimum quality ED-CdS thin film layers. To investigate this, all-ED CdTe solar cells were fabricated by varying the CdS growth voltage near to its optimum value, while keeping the other conditions at constant values.

Figure 6.6 shows the primary solar cells parameters V_{oc} , J_{sc} , FF and efficiency as a function of growth voltages of CdS. The optimum growth voltage for CdS is at cathodic potential of 1460 mV, the best quality solar cells were produced at a cathodic voltage of 1455 mV. This pattern was observed within the research group for many materials, as the conditions for a CdS layer suitable for use in CdTe based solar cells can be slightly different to the conditions to produce the best CdS semiconductor layers.

The highest fill factors were observed at higher cathodic voltages, where as the other parameters were observed at a cathodic potential of 1455 mV.

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Figure 6.6: The performance curves of all-ED CdTe based solar cells produced with various CdS growth voltages, ED-CdTe at $V_g = 697$ mV and $t_g = 4$ hours with the structure of glass/FTO/CdS/CdTe/Cu-Au.

The effect of varying the growth times of CdS layers on the performance of CdTe solar cells was also investigated. Several all-ED solar cells were fabricated with CdS layers grown for different times while keeping the other fabrication conditions constant. Kosyachenko stated it is difficult to electrodeposit CdS layers below ~50 nm without pinholes [7] and it was observed that CdS layers were colourless up to 10 minutes of electrodeposition. This indicates that the duration of growth needs to be ~15 minutes to improve the device efficiencies of solar cells made from CdS layers. So at least ~80 nm of CdS layer was used in when fabricating solar cells, which represents 15 – 20 minutes of deposition under the current experimental settings. The longer the growth duration, the thicker the deposited semiconducting layer as illustrated in Table 6-2. In the literature it is reported that the thickness of the CdS layer most suitable for the production of CdTe solar cells is ~(80 -100) nm, which is comparable to the results of this study [8].

Growth times of CdS layers	Thickness	Growth rate (nm min ⁻¹)		
(minutes)	(nm)			
15	87	5.8		
30	167	5.6		
45	250	5.6		
60	300	5.0		

Table 6-2: Thickness of ED-CdS layers grown for different durations.

The optimum growth conditions for using CdS layers in CdTe solar cells were identified as 1455 mV cathodic voltage and 15 minutes of deposition to produce an ~80 nm CdS layer.

The device parameters of the best solar cell using CdS layers as a window layer is shown in Figure 6.7. The device parameters for this device were $V_{oc} = 625 \text{ mV}$, $J_{sc} = 36.1 \text{ mAcm}^{-2}$, FF = 0.30 and efficiency 6.8%. The improvement in current density was noticeable in CdS/CdTe solar cells. This may be because CdTe layers grow preferentially on CdS layers with better lattice matching [9]. Series resistance and shunt resistant of this device was calculated to be 21.4 Ω cm⁻² and 2515 Ω cm⁻² respectively.



Figure 6.7: Device parameters of the best PV device using CdS as a window layer in a CdTe solar cell. The growth conditions for the semiconducting layers were, CdS; $V_g = 1455 \text{ mV}$, $t_g = 15 \text{ minutes}$ and CdTe; $V_g = 697 \text{ mV}$ and $t_g = 4 \text{ hours}$.

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Material	$R_s \Omega cm^{-2}$	$R_{sh} \Omega cm^{-2}$	AFM R _{ms} (nm)	
ZnS	13.2	3808	90.3	
CdS	21.4	2515	35.2	
ZnS/CdS	12.2	5294	35.2	

 Table 6-3:
 Selected surface parameters for ZnS and CdS layers

As shown in Table 6-3, these surface roughness values from AFM measurements correlate with the values of series and shunt resistances (R_s and R_{sh}) of the solar cells produced from these materials. Solar cells with a ZnS buffer layer in ZnS/CdS solar cell structure yield the best R_s and R_{sh} values leading to the highest fill factor as shown in Figure 6.2.

The growth conditions and PV parameters of CdTe solar cells can be further improved with more extensive and longer experiments. As CdS enhances the efficiency of CdTe solar cells [6], the solar cells with a CdS layer have to be investigated further. Several research groups have produced very encouraging efficiencies for CdTe solar cells, even with amorphous CdS [10]. Duffy reported electrodeposited CdTe solar cells with 6% [11] but the CdS was produced by CBD method. All-electrodeposited CdTe solar cells are not yet heavily researched but CdTe solar cells by electrodeposition and another method have been reported with efficiencies as low as 2% even in 2013.

6.4 Solar cells using $CdS_{(1-x)}Se_x$ layer

The use of an epitaxially grown window layer could solve the pinhole problem in CdTe solar cells. Because electrodeposited ZnSe layers grow epitaxially, the inclusion of Se into CdS to produce $CdS_{(1-x)}Se_x$ was attempted to fabricate layer-by-layer grown semiconducting layers of $CdS_{(1-x)}Se_x$ [11]. $CdS_{(1-x)}Se_x$ layers produced under this programme did not provide the layer-by-layer deposition required to fabricate high efficiency solar cells without pinholes. However, it was possible to grow good nano-crystalline, ED-CdS_(1-x)Se_x thin film semiconducting layers successfully with desired structural, optical and electrical properties; this material layer can be used in various applications [12].

 $CdS_{(1-x)}Se_x$ thin film layers were used for three different functions in the experimental solar cells under this programme.

All-ED solar cell structures using $CdS_{(1-x)}Se_x$ layers: To test the suitability of $CdS_{(1-x)}Se_x$ layers in all-ED solar cell fabrications, three device structures were electrodeposited based on observations that it was possible to electrodeposit CdTe layers on ED-CdS_(1-x)Se_x with no peeling off issues. These device structures were discussed in section 2.4.2.2 in Chapter 2.

Three different functions performed by $CdS_{(1-x)}Se_x$ were, as a buffer layer, as intermediate layer and as a window layer as described below.

(i) $CdS_{(1-x)}Se_x$ as a buffer layer: glass/FTO/ substrate was used to fabricate a very thin layer of ED-CdS_(1-x)Se_x, just enough with few Se atoms to initiate nucleation of the CdS growth by electrodeposition. Then the all-ED device structure as shown in Figure 2.12, (glass/FTO/CdS_(1-x)Se_x/ CdS/CdTe/Cu-Au) was fabricated. The devices were very weak and inconsistent.

(ii) $CdS_{(1-x)}Se_x$ as an intermediate layer: glass/FTO/CdS was used as substrate to deposit ED-CdS_(1-x)Se_x layers followed by the fabrication of all-ED graded bandgap device structure of , glass/FTO/CdS/CdS_(1-x)Se_x/CdTe/Cu-Au as shown in Figure 2.13. It was observed that this structure experienced difficulties such as non-uniformities and peeling off. During the growth of the ED-CdTe layer, it was only possible to grow CdTe to half the required thickness. This device had very low device parameters, $V_{oc} = 320$ mV, $J_{sc} = 11.0$ mAcm⁻², FF = 0.25 and $\eta = 0.9\%$. This may be due to the absorber layer lacking the optimum required thickness of ~1.5 µm hence not being able to absorb the necessary amount of photons.

(iii) $CdS_{(1-x)}Se_x$ as the window layer: a glass/FTO/CdS_(1-x)Se_x/CdTe/Cu-Au device was produced. In this structure as shown in Figure 2.11, CdTe layers were successfully electrodeposited to the required thickness, hence it recorded better PV cell parameters, $V_{oc} = 520 \text{ mV}$, $J_{sc} = 17.8 \text{ mAcm}^{-2}$, FF = 0.40 and $\eta = 3.7\%$. Table 6-4 summarises the functions of ED-CdS_(1-x)Se_x layers in different solar cell structures, along with the PV parameters observed for each device structure.

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Table 6-4: Summary of preliminary studies of solar cell structures using $CdS_{(1-x)}Se_x$ for different functions.

Solar cell device structure	Function of CdS _(1-x) Se _x layers	V _{oc} (mV)	J _{sc} (mAcm ⁻²)	FF	η
glass/FTO/CdS _(1-x) Se _x /CdS/CdTe/Cu-Au	Buffer layer	No good	layers due to	growtł	n issues.
glass/FTO/CdS/CdS _(1-x) Se _x /CdTe/Cu-Au	Intermediate layer	320	11.0	0.25	0.9%
glass/FTO/CdS _(1-x) Se _x /CdTe/Cu-Au	Window layer	520	17.8	0.40	3.7%

6.5 Initial fully-electrodeposited graded bandgap ZnS/CdS/CdS $_{(1-x)}$ Sex /CdTe solar cell

Using all the layers developed and optimised in this programme, it is possible to fabricate multi-layer graded bandgap devices. The multi-layer graded bandgap device was electrodeposited with four semiconducting layers with the structure of glass/FTO/ZnS/CdS/CdS_(1-x)Se_x/CdTe/Cu-Au. The device structure was illustrated in Figure 2.14. The device parameters for four devices are summarised in Table 6-5.

Table 6-5: The device parameters of graded bandgap glass/FTO/ZnS/CdS/CdS $_{(1-x)}$ Sex/CdTe/CuAu (back contact) devices.

Device.	V _{oc} (mV)	J_{sc} (mAcm ⁻²)	FF	Efficiency η %
1	0.550	12.5	0.43	3.0
2	0.535	14.7	0.44	3.5
3	0.565	12.5	0.43	3.0
4	0.545	13.5	0.43	3.2

Significant improvements in fill factor values were noticed for these devices. The fill factor values increased by about 25% while there were some losses in J_{sc} . If this reduction of J_{sc} is to be attributed to the internal recombination of electron hole pairs, this can be minimised if the layers are grown uniformly.



Figure 6.8: Cross sectional SEM images (with and without layer identifiers) of graded bandgap device with the structure glass/FTO/ZnS/CdS/CdS_(1-x)Se_x/CdTe/ (by the courtesy of collaborator at Uni. of Durham).

The thicknesses of layers of the device shown in Figure 6.8 were, ~40 nm, 400 nm, 266 nm, 200 nm, 90 nm and 470 nm for SiO₂, FTO, ZnS, CdS, CdS_(1-x)Se_x, and CdTe layers respectively. These four electrodeposited layers of the multi-layer graded bandgap device are clearly visible in the Figure 6.8. This SEM image also indicates the possible intermixing of electrodeposited layers specially CdS_(1-x)Se_x and CdS layers. This growth confirms the possibility of manufacturing of multiple semiconducting layers by electrodeposition method. The growth issues of these devices could be addressed as part of a longer investigation.

In order to improve the efficiencies of electrodeposited solar cells further, several factors need to overcome. Recombination of EHPs can be reduced by producing gap-free semiconductors or inclusion of a pinhole-plugging layer to the device structure to prevent the recombination. This will also produce solar cells with lower series and higher shunt resistances resulting in higher fill factor values. These devices need to be researched further, to optimise the effects of other growth conditions, such as the growth time needed for the desired thickness of individual semiconducting layers. Once these conditions are further optimised it should be possible to produce higher efficiency all-ED solar cells.

6.6 Summary of electrodeposited CdTe based solar cells

Several structures of CdTe based solar cells were fabricated in search of higher efficiency all-electrodeposited solar cells. Four different semiconductors (ZnS, CdS, $CdS_{(1-x)}Se_x$ and CdTe) were electrodeposited to complete the solar cell structure. The structures include several single junction solar cells such as glass/FTO/CdS/CdTe/Cu-Au (back contact), glass/FTO/ZnS/CdTe/Cu-Au (back contact) and glass/FTO/CdS_(1-x)Se_x /CdTe/Cu-Au (back contact) and multi-junction solar cell structures such as glass/FTO/ZnS/CdS/CdTe/Cu-Au (back contact), glass/FTO/ZnS/CdS/CdS_(1-x)Se_x /CdTe/Cu-Au (back contact), glass/FTO/ZnS/CdS/CdS_(1-x)Se_x /CdTe/Cu-Au (back contact), glass/FTO/ZnS/CdS/CdS_(1-x)Se_x /CdTe/Cu-Au (back contact), glass/FTO/ZnS/CdS/CdS_(1-x)Se_x /CdTe/Cu-Au (back contact). The main parameters of the above structures are summarised in Table 6.6.

Table 6-6: S	Selected	parameters	for sola	ar cells	produced.
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Solar cell structure	V _{oc}	J _{sc}	FF	Efficiency
	(mV)	$(mAcm^{-2})$		η %
glass/FTO/CdS/CdTe/Cu-Au	625	36.1	0.30	6.8
glass/FTO/ZnS/CdTe/Cu-Au	576	30.8	0.33	5.9
glass/FTO/CdS _(1-x) Se _x /CdTe/Cu-Au	520	17.8	0.40	3.7
glass/FTO/ZnS/CdS/CdTe/Cu-Au	620	27.2	0.36	6.1
glass/FTO/ZnS/CdS/CdS _(1-x) Se _x /CdTe/ CuAu	535	14.7	0.44	. 3.5

As shown in Table 6-6, the highest fill factor is achieved for multi-junction graded bandgap solar cells; and consistently high J_{sc} values are observed in solar cells designed using CdS as the window layer. The second highest fill factor (0.36) is for glass/FTO/ZnS/CdS/CdTe/Cu-Au devices which correspond well to the lowest series resistance and highest shunt resistances among the investigated solar cells (see Table 6.4). To increase the solar cell efficiency further, more uniform semiconductor layers without nano-scale gaps should be consistently produced. The use of a buffer layer prior to the deposition of a conventional window layer gives promising results and could be considered as the direction for further research.

The first attempt of fabrication of all-ED multi-layer graded bandgap solar cells was made. Such cell gave higher fill factor values while rather low value of J_{sc} . This is most likely due to the increase of carriers recombination on the boundaries between layers as shown in the high definition SEM images.

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7.1 Conclusions

ZnS semiconductor as a buffer or window layer

During this research, ZnS layers from an aqueous electrolyte at 85°C temperature were successfully electrodeposited avoiding the use of Na containing chemicals. For the first time the chemical combination of $ZnSO_4$ and $(NH_4)_2S_2O_3$ was used in a 2-electrode configuration. The use of the electrolyte at high temperature resulted in sulphur precipitations, which stopped after few hours of deposition. The optical bandgap of electrodeposited ZnS layers grown in this study was comparable with the reported optical bandgap of bulk CdS material. This material is highly transparent, uniformly electrodeposited on FTO substrates, and amorphous in structure. While it was possible to electrodeposit p-type ZnS semiconducting layers, the optimum quality ZnS layers were n-type in electrical conduction. The highly adhesive ZnS layers were used in several different device structures of fully-electrodeposited solar cells. ZnS layers can be used as a buffer layer in CdS/CdTe solar cells, as a window layer in CdTe solar cells and also as a part of a multi-layer graded bandgap device structure. These initial structures produced efficiencies of ~6.1%, ~5.9% and ~3.5% respectively. While all these device fabrications were possible to achieve, further optimisation is needed to improve the vital solar cells parameters, i.e., V_{oc} , J_{sc} , FF, hence leading to commercially viable solar cells.

CdS semiconductor as a window layer

The novel chemical combination of $CdCl_2$ and $(NH_4)_2S_2O_3$ was used in the electrodeposition of CdS in a 2-electrode configuration. Precipitations of sulphur particles stopped during the first few hours of deposition. Following the cessation of precipitations, uniform CdS layers were deposited without further issues due to the precipitations. This electrolyte was continuously utilised for electrodepositing CdS layers over eighteen months without having to make a new electrolyte with care full replenishment of the required ions. This long life span of the electrolyte is an indication of the electrodeposition as a low-cost deposition method. The electrodeposited CdS layers had hexagonal structure, in contrast to the cubic structure reported by CBD. This

hexagonal structure is coherent with previous reports from the same group from different pre-cursors containing Na and under different growth conditions by electrodeposition [1]. The optical bandgap measured with this novel CdS was similar to the reported figures in the literature. The electrodeposited CdS thin film layers were highly adhesive, hence it was possible to electrodeposit CdTe thin film absorber layers on to the CdS layers to produce fully-electrodeposited (all-ED) solar cells. Solar cells with PV parameters, $V_{oc} = 625$ mV, $J_{sc} = 36.1$ mAcm⁻², FF = 0.30 and $\eta = 6.8\%$ were fabricated. When a buffer layer was used with a CdS layer the FF provided more encouraging values in all-ED CdTe based solar cells.

Furthermore, the observation of nano-rods with gaps in between the CdS layers can contribute to pinholes, hence short-circuiting in the devices. To mitigate this, either the nano-rods should be tightly packed in the direction perpendicular to the glass/FTO surface or the layer-by-layer deposition of thin film layers should occur.

$CdS_{(1-x)}Se_x$ semiconductor as a window layer

The semiconducting ternary thin film layer, $CdS_{(1-x)}Se_x$, provided another option as a window layer. This research was a result of the search for the deposition of layer-bylayer semiconductor to avoid pinholes. As with CdS electrolyte, there were precipitations after the addition of sulphur ions. Due to the complexities of controlling the S/Se ion ratio, thin films with various morphologies were observed including nanowires, nano-tubes and nano-sheets, under different growth conditions. These morphologies were previously only fabricated at very high temperatures of 800°C for nano-technological applications [2]. Stable $CdS_{(1-x)}Se_x$ layers were electrodeposited at 1380 mV cathodic voltage with high adhesivity with the chemical composition of $CdS_{0.48}Se_{0.52}$. Thin film layers grown at these conditions were n-type in electrical conduction and hexagonal in structure. It was possible to electrodeposit CdTe on to $CdS_{(1-x)}Se_x$ layers, hence several different all-ED solar cell structures were fabricated with best conversion efficiency of ~4%.

CdTe semiconductor as an absorber layer

The electrolyte for this deposition of CdTe layers did not have any precipitations and experimented at 70°C using a modified saturated calomel reference electrode. Optimisation of CdTe layers from the three-electrode method provided polycrystalline,

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highly absorbent and adhesive thin films. The deposited thin films were cubic in structure with the highest XRD peak with the preferred orientation of (111). Due to the addition of CdI_2 , most of the heat-treated samples were *n*-type in electrical conduction, while some *p*-type CdTe thin film layers were observed at lower cathodic voltages. Under the ideal Te ion concentrations, the reproducibility of CdTe thin film layer was very high.

Fully-electrodeposited solar cells were fabricated using the ED-CdTe layer as the absorber layer. The layers were grown for 4 - 5 hours and used to fabricate solar cells with other electrodeposited semiconductor layers grown in this study. This growth duration represented ~1.5 µm thick CdTe layers under the explored experimental conditions.

Solar cell devices and processing

Several different solar cell device structures were fabricated and investigated from the raw chemicals and glass/FTO substrates to the final PV devices under this programme. This empowers a researcher with the understanding to evaluate any semiconducting material and any solar cell fabrication method with high confidence in semiconductor and device issues. Each step was investigated in order to gain a deep understanding of the fabricated solar cells. The performance of the PV devices was measured using I - V characterisation from which the efficiency of the solar cells and other device parameters were calculated. Each step was improved with many iterations as the research progressed, while minimising the shortcomings to enhance the device parameters.

It was identified, that the bottlenecks for the development of high efficiency solar cells were the V_{oc} and FF. The devices with a buffer layer consistently produced better fill factor values. To improve the V_{oc} , pinning the Fermi level at a more suitable level closer to the valence band by addressing the back contact issues should be investigated [3].

AFM and SEM characterisations indicated that the thin film layers have gaps between the grains in some areas, which can only be seen under larger magnifications. Nanorods in CdS layers with gaps, and very fine non-uniformities of ZnS and CdTe layers resulted in short-circuiting of the final solar cell devices. This may be the main cause for the lower efficiencies of the initial solar cells produced. The possible ways to increase the efficiencies and improve the reproducibility are discussed in the future work.

7.2 Future work

The future direction to improve electrodeposition of solar cells can be categorised into two areas. They are (i) to increase the highest efficiency by improving the quality of the thin films, and (ii) to increase the reproducibility by understanding the device and processing issues. Several of the growth issues addressed here will also increase the reproducibility of solar cell devices.

The glass/FTO substrates have a direct effect on the electrodeposition of semiconducting layers. It is shown by AFM scans that FTO surfaces have a variation of $\sim \pm 100$ nm with several sharper peaks. Under electrodeposition, these peaks create high electric fields above them, which lead to non-uniform deposition of materials and columnar growth. A way to reduce this unevenness caused by FTO layers can be investigated to produce more uniform semiconductor layers.

Several SEM images show surface contaminations in semiconducting layers. The contaminations can be reduced by the use of ultrasonic cleaning immediately prior to the electrodeposition of semiconducting layers. High magnification cross sectional SEM images also showed several voids at the interfaces of different layers, which may be due to the non-conductive contaminations. A systematic experiment to establish this claim or the effect of ultrasonic cleaning can be conducted easily within the current experimental facilities. This may also lead to increase in reproducibility.

It is seen from the current study, the presence of gaps in between the grains of the ED semiconducting materials. As this is not helpful to produce good quality solar cells, the possibility of depositing semiconductors in a layer-by-layer manner should be further explored. The electrodeposition of semiconductors with the use of Se [4] has shown the layer-by-layer deposition [5] avoiding this issue of gaps. This can be further investigated by producing all-ED solar cells with CdSe as the window layer [6], as there have been several reports of ED-CdSe layers.

To increase the reproducibility of the semiconducting layers, the electrolytes must be maintained at the same conditions throughout a set of experiments. Real time monitoring of pH values, growth temperatures, and most importantly the concentrations of chemical precursors is a challenging task. This monitoring to improve reproducibility

could be achieved with the aid of an ion specific field effect transistor (ISFET). Already ISFETs are used to monitor in-situ pH values, temperature and ionic levels in many applications [7]. While it is possible to identify S ions with ISFETs, there are no ISFETs currently to recognise the other ions used in this research programme, i.e., Cd, Zn, Te and Se. The development of an ionic membrane specific to an ISFET is somewhat a different research direction involving the sol-gel technique [8]. Nevertheless, the addition of such a monitoring level to electrodeposition programmes would significantly improve the reproducibility of the thin film layers and eventually solar cell devices. Hence, it would also contribute to the gradual increase of overall solar cell efficiency. An expert researcher in electrodeposition can only find the growth conditions to produce semiconducting layers. An ISFET can record the concentration of specific ion at that optimum condition. It may take several growths once this critical ion balance is perturbed to achieve it again. An ISFET calibrated under the optimum growth condition will give the researcher an indication of which ion needs to be added and in what quantity, to maintain this critical ion balance. This process is similar to controlling the pH value. Without such a device, controlling three elements is even more challenging. Hence it is recommended to avoid using more complicated experiments for example, the electrodeposition of $CdS_{(1-x)}Se_x$, ternary thin film layers until such a time when good indicators of ion concentrations in the electrolytes are available.

To produce good quality solar cells, thin film layers without pinholes or gaps between the grains should be deposited. A pinhole-plugging layer (PPL) [9] can be deposited to block pinholes and prevent short-circuiting the devices prior to the back contact metallisation. To investigate this effect the development of a semiconducting polymer layer, Polyaniline by electrodeposition is recently started within SHU solar energy group. This will lead to the fabrication of hybrid solar cells [10] more importantly with the high performance by reducing or eliminating short-circuiting of diodes.

Buffer layer-incorporated PV structures fabricated during this research, consistently produced devices with higher FF values. In this programme, the FF parameter is the main bottleneck to increase the efficiency, so the inclusion of a buffer layer to the standard PV structure can further be investigated [11]. Within the current experimental facilities, this can be achieved in three different ways. They are by the using of two window layer semiconductors available under this programme, (i) the device structure of glass/FTO/ZnS/CdS/CdTe/Cu-Au and using two layers of the same semiconductor

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with the device structures of (ii) glass/FTO/ZnS/ZnS/CdTe/Cu-Au and (iii) glass/FTO/CdS/CdS/CdTe/Cu-Au [12].

Solar cells produced with Cd-rich CdTe layers produce better PV performances after the back metal contact is fabricated. To produce such layers, the right etching conditions can be identified with the aid of Raman spectra analysis [13].

These thin film layers can be experimented further for scalability and large area manufacturability by electrodepositing in larger volume of electrolytes and fabricating solar cells with 5 mm or 1 cm diameter. A record of yield can be implemented to understand the reproducibility and uniformity further. Since under this research programme good quality devices are routinely processed, a record of total processing time excluding the drying and waiting times can provide interesting comparison with other processing methods leading to further improvements in the entire process [10].

All-ED solar cells have several issues to be addressed before they become a commercial reality as investigated in this programme. Achieving the PV parameters of $V_{oc} > 850$ mV, $J_{sc} > 30$ mAcm⁻², FF = 0.75 and η in excess of 20% is realistic. However, this can only be achieved once these elusive growth conditions are identified for each semiconductor and future solar cells are reproduced under those growth conditions repeatedly. The expectations are high on achieving these objectives to reduce the cost of electricity from the Sun.
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List of Publications

Journal articles

O. K. Echendu, A. R. Weerasinghe, D. G. Diso, F. Fauzi and I. M. Dharmadasa, "Characterization of n-Type and p-Type ZnS Thin Layers Grown by an Electrochemical Method," *Journal of Electronic Materials*, January 2013.

I. M. Dharmadasa, D. G. Diso and A. R. Weerasinghe, "Nano-rod nature of CdS window materials used in thin film solar cells," Submitted to *International Journal of Smart and Nano Materials*, February 2013.

A. R. Weerasinghe O. K. Echendu and I. M. Dharmadasa, "Electrodeposition of n-type $CdS_{(1-x)}Se_x$ to use as an intermediate layer in thin film solar cells," (*to be submitted* June 2013).

A. R. Weerasinghe O. K. Echendu and I. M. Dharmadasa, "Electrodeposition of n-type CdS from two different sulphur precursors to use in thin film solar cells," (to be submitted July 2013).

Conference papers

O. K. Echendu, <u>A. R. Weerasinghe</u>, D. G. Diso, F. Fauzi and I. M. Dharmadasa, "Concentration dependence of the electrical conductivity type of electrodeposited ZnS thin films," *CMMP-2011 J. of Phys. Conference series. IOP*, Dec 2011.

<u>A. R. Weerasinghe</u>, O. K. Echendu, D. G. Diso and I. M. Dharmadasa, "Study of electrodeposited ZnS thin films grown with $ZnSO_4$ and $(NH_4)_2S_2O_3$ precursors for use in solar cells," *Solar Asia 2011 Proceedings, IFS- Kandy*, Sri Lanka, 2011.

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I. M. Dharmadasa, L. Gunaratne, <u>A. R. Weerasinghe</u> and K. Deheragoda, "Solar Villages for Sustainable Development," *APSL Research Symposium, Sheffield*, 2012.

<u>A. R. Weerasinghe</u>, O. K. Echendu, F. Fauzi and I. M. Dharmadasa, "Electrodeposition of n-type $CdS_{(1-x)}Se_x$ to use as an intermediate layer in thin film solar cells," *UK* Semiconductors conference, July 2012.

<u>O. K. Echendu</u>, A. R. Weerasinghe, F. Fauzi and I. M. Dharmadasa, "Electrodeposition of n-type and p-type ZnS Thin Films from Two Different Zn^{2+} Precursors," *UK* Semiconductors conference, July 2012.

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