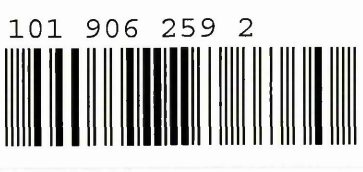

ELECTRONIC PROPERTIES OF DEFECTS IN SILICON AND RELATED MATERIALS

NIKI MITROMARA

A thesis submitted in partial fulfilment of the requirements of
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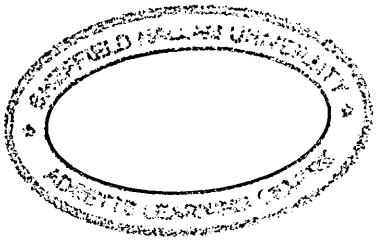

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Declaration

The work described in this thesis was carried out by the author in the Materials and Engineering Research Institute, Sheffield Hallam University. The author declares that this work has not been submitted for any other degree. The work is original except where acknowledged by reference.

The Author

Niki Mitromara

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To the four people I consider family.

Your presence in my life is a blessing.

Abstract

Efforts in the current semiconductor industry are focused on the production of smaller, more efficient and inexpensive devices of higher packing density. As silicon is the dominant semiconductor implemented for the fabrication of the majority of semiconductor devices, perpetual research has focused on the improvement of its properties and the realisation of the most efficient structures. This thesis presents the electrical characterisation of two different diode structures that are important for the present and future generations of electronic devices.

The first part of the thesis is focused on the electrical characterisation of Ultra-Shallow Junction (*USJs*) Si diodes. Both p^+n and n^+p USJ structures that contained different implants were examined. These were very highly doped and intended to simulate the situation where a doping well is formed after heavy doping in Si for the fabrication of transistors currently used in Complementary-Metal-Oxide-Semiconductor (*CMOS*) technology. The implanted USJ diodes were provided by NXP, Belgium and contact deposition was performed before their electrical characterisation as part of this project. Subsequently the p^+n and n^+p USJ diodes were characterised by the use of Capacitance-Voltage (CV), Current-Voltage (IV), Deep Level Transient Spectroscopy (DLTS) and high resolution Laplace DLTS (LDLTS). DLTS and LDLTS are very powerful spectroscopic techniques for the profiling of defects in the bandgap of a semiconductor as well as for the identification of the electrical signatures of these defects. Transient-Enhanced Diffusion (TED) related defects were detected in these diodes as the presence of mainly carbon-related interstitial complexes was observed. In addition, certain vacancy or vacancy-dopant related levels were also discerned.

The second part of this thesis presents the electrical characterisation from Schottky p-diamond/p-Si and p-diamond/n-Si p-n diodes. These diodes were readily provided, grown by the Chemical Vapour Deposition (CVD) technique, for the electrical characterisation that was performed as part of this project. The purpose of characterising both Schottky and p-n diamond on Si diodes was to detect defects near the surface of the films and near the interface with Si and hence provide a comparison between defects present at the beginning and end of growth. More defects were found near the interface with Si and the majority of observed defects were related to extended defects while the presence of grain boundaries in polycrystalline diamond was discussed.

Contents

List of publications

Journal publications – accepted for publication

1) N. Mitromara, J.H. Evans-Freeman and R. Duffy, "Laplace Deep Level Transient Spectroscopy of ultra shallow implanted junctions in Si", accepted for publication in IEEE Xplore after presentation at the IUMRS-ICEM 2008 International Conference on Electronic Materials, Sydney, Australia.

2) Karen D. Vernon-Parry, Jan H. Evans-Freeman, Niki Mitromara, and Paul W. May, "High Resolution Deep Level Transient Spectroscopy of p-n diodes formed from p-type polycrystalline diamond on n-type silicon", accepted for publication in IEEE Xplore after presentation at the IUMRS-ICEM 2008 International Conference on Electronic Materials, Sydney, Australia.

Journal Publications – Published

1) N. Mitromara, J.H. Evans-Freeman, C. Gädtke, P.W. May, "High resolution Laplace deep level transient spectroscopy of p-type polycrystalline diamond", phys. stat. sol. (a) *205* (2008) 2184-9.

2) N. Mitromara, J.H. Evans-Freeman, and R. Duffy, "Deep Level Transient Spectroscopy of ultra shallow junctions in Si formed by implantation", Solid state phenomena, *131-33*, (2008) 497-502.

3) J.H. Evans-Freeman, D. Emiroglu, M.A. Gad, N. Mitromara and K.D. Vernon-Parry, "Deep electronic states in ion-implanted Si", Journal of materials science, *41*, 3, (2006) 1007-1012

Chapter 1: Introduction

1.1 Overview

Semiconductors are the main driving force behind the rapid and well established success of the electronics industry. Modern electronic devices are the outcome of continuous innovation and research and constitute one of the most profitable markets presently. The properties of many semiconductors have been explored since the beginning of the last century, such as germanium (*Ge*) which however was found to have leakage and heating problems. Since the establishment of silicon (*Si*) in the 1930s as the material with the most favourable properties, the semiconductor industry advanced with incredibly fast rates, only to be further increased by the introduction of the Metal-Oxide-Semiconductor-Field-Effect-Transistor (*MOSFET*) in 1960 [1]. Continuous increase in integration density driven by Moore's Law, entails perpetual efforts towards reduction in semiconductor device dimensions and provides great challenges. These lie in the increase of the performance and capabilities of the devices, while significantly decreasing their cost and energy consumption.

Almost fifty years later, Si is still the dominant semiconductor material used in electronic devices. It is however widely understood that its physical limits in the increasingly sophisticated Integrated Circuits (*ICs*) are soon to be reached. The ever-growing requirement for downscaling of device dimensions gives rise to complicated physical phenomena. The behaviour of electrons deviates from the classical particle form when only a few atomic layers of the semiconductor are necessary for the fabrication of ultra-thin structures and quantum analysis is then required to control the operation of the device. More importantly, increased gate leakage current, dopant diffusion and carrier and lifetime degradation are increasingly significant obstacles in the functionality of MOSFETs.

As scaling increases, the presence of defects in the semiconductor can be detrimental to the device performance and a vast amount of research has been performed to characterise, identify, and eliminate them or successfully control their behaviour. Moreover, a wide range of experimental techniques have been developed to ensure

adequate information of the properties of these defects can be obtained and is subsequently used in order to produce beneficial device characteristics. In addition to the study of defects, investigation of novel semiconducting materials has increased during the last few decades in order to provide an alternative to the problems the Si semiconductor industry is facing. These materials have to either have sufficiently good properties to replace Si or must be compatible with the modern Complementary-Metal-Oxide-Semiconductor (*CMOS*) technology which is based on Si. Such research has recently focused on wide bandgap semiconductors as they possess exceptional physical and electrical properties for either light emission or power devices. High carrier mobility, high power capability and operation under harsh environments, such as high temperature, make these materials very promising candidates for future generations of electronics. The implementation of these materials alone, is however impeded by the years of experience against the well characterised properties of Si. In addition the inability at present, to produce very high quality or large area of single crystals of most these semiconductors, suggests that more research is required.

In view of achieving reduced-size microelectronic devices, investigation of ultra-shallow Si structures and thin film diamond based devices have been examined in this project. In order to achieve smaller devices, very highly doped Si has been provided by NXP in Belgium, resulting in Ultra-Shallow Junctions (*USJ*s). The use of such structures is imposed by the requirements of present and future generation of semiconducting devices though many challenges lie in the complicated nature of such materials. Successful characterisation of the defects and handling of the properties of USJs may lead to the improvement of these structures which are already being used by the current Si CMOS technology. Defect characterisation was performed using one of the most suitable techniques for this purpose, namely Deep Level Transient Spectroscopy (*DLTS*).

The same capacitance transient based technique, developed in 1974 [2], was also implemented for the profiling of the thin diamond films. The latter were synthesized by Chemical Vapour Deposition (*CVD*), a method which has been studied for a few decades but has only produced fruitful results in diamond recently [3, 4]. The challenges involved with the characterisation of devices based on diamond emanate

from the polycrystalline nature of most of these films and the large bandgap which requires high temperature for the investigation of possible defects.

1.2 Aims of the project

This project is based on Si ultra-shallow junction diodes and synthetic thin diamond films grown on Si substrates. Therefore two different semiconductor technologies had to be investigated. The main aims of the project include:

1. Studying the nature and properties of defects in Si.
2. Studying the properties of wide bandgap semiconductors and in particular diamond for the fabrication of diamond diodes on Si substrates.
3. Electrical characterisation of p^+n and n^+p ultra-shallow junctions using DLTS and high-resolution Laplace DLTS (*LDLTS*).
4. Electrical characterisation of p-type diamond on p-type Si Schottky diodes using DLTS and LDLTS.
5. Electrical characterisation of p-type diamond on n-type Si p-n diodes by the same techniques in order to provide and in-depth analysis of the CVD grown diamond film.
6. Drawing conclusions about USJs and diamond diodes that will enhance scientific knowledge and assist in the future study and implementation of such structures.

1.3 Outline of the thesis

Chapter 2 provides an overview of defects present in Si. The role of impurities and defects such as point defects, extended defects and dislocations is examined and the effect they produce on Si crystals and Si devices. Finally current technological problems such as Transient Enhanced Diffusion of Boron are addressed and a literature research of ultra-shallow junctions is provided.

Chapter 3 is an introduction to wide bandgap materials. Their properties, originating from the large bandgap, are described as well as the reasons for their possible ability to replace Si in devices. Furthermore, research is focused on diamond as the material of choice in this project, its origin and growth techniques and the properties of defects commonly found.

Chapter 4 describes the diode structure and operation focusing on p-n and Schottky diodes. Subsequently the experimental techniques used for the electrical characterisation of all the diodes in this project are described. These include Capacitance-Voltage (*CV*), Current–Voltage (*IV*), DLTS and LDLTS measurements.

Chapter 5 presents the fabrication and processing details of the p-n and Schottky diodes made for this project, both for the USJ and diamond structures. In addition, the technical details of the system used and the specification of the diodes are given.

Chapter 6 shows the results of the electrical characterisation of the p^+n USJs on Si using CV, IV, DLTS and LDLTS.

Chapter 7 illustrates the results of the electrical characterisation of n^+p USJs using CV, IV, DLTS and LDLTS.

Chapter 8 demonstrates the results obtained from the characterisation of defects in the Schottky and p-n diode structures of diamond films on Si.

Chapter 9 summarizes the results and provides conclusions about the two very different semiconducting diodes investigated in this project. Conclusions are drawn about the defects present in Si USJs and in the diamond films deposited on Si. Finally future work based on these results is suggested.

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Chapter 2: Defects in Silicon

2.1 Introduction

Silicon is currently the most widely used semiconductor in the electronics industry and has been extensively examined for decades. This is because it is found in abundance in the earth's crust and very high purity silicon is now being produced. Silicon has a relatively small bandgap of ~1.14eV at room temperature which is suitable for controlling its semiconducting properties. The presence of impurities introduced on purpose or inadvertently, also affects the physical and electrical properties of silicon. Depending on the nature of these impurities, deep or shallow levels within the bandgap of silicon are formed. These often function as "stepping stones" for electrons to be promoted from the valence to the conduction band and hence contribute to conduction. As shallow impurities in Si are usually fully ionised, the concentration of carriers, when impurities are present, is different to that of intrinsic silicon. Impurities are therefore often used as a method to manipulate the conductivity of silicon devices. In addition, other defects such as point or extended defects or dislocations are commonly present after certain treatments. These can trap free carriers and hence have an overall effect on conduction.

Defects have usually a detrimental effect on the device properties, such as current leakage, which can lead to device degradation. In order to control the characteristics of Si devices, it is essential therefore either to prevent defect formation or to possess the ability to govern their behaviour. The purpose of this chapter therefore is to provide a detailed review of the research that has been performed on the study of defects in Si. In particular, the effects of irradiation and implantation are examined as these are the most commonly used methods for introducing foreign atoms into the Si lattice. Finally the effect of heavy implantation doses for the formation of ultra-shallow junctions is considered as it is a recent area of interest. The need for shallow junctions arises from the continuous effort to reduce the size of electronic devices, while maintaining control over the device properties and hence is an integral part of the modern semiconductor industry.

2.2 Energy levels

At temperatures above absolute zero, some electrons in most semiconductors and in particular in Si, can acquire enough energy to cross the energy barrier from the valence to the conduction band. As the temperature rises the number of electrons promoted to the conduction band increases and consequently the number of holes left in the valence band increases accordingly. Apart from this thermal generation of electron-hole pairs (*e-h*) other processes, such as optical and electrical excitation, can be used to create excess carriers and hence to increase the conductivity of the material. In thermal equilibrium however, the rate of thermal generation of e-h pairs is balanced by their recombination rate. This ensures that there is no excess population of electrons or holes and the overall conduction of the material is stable.

Recombination takes place by the electron dropping either directly back to the valence band, or to a deep level in the bandgap where it subsequently captures a hole from the valence band in order to complete the e-h annihilation process [1]. The energy released by either the direct or indirect recombination via energy levels can be dissipated in three ways. The radiative process entails the emission of a photon during recombination. The non-radiative process involves either emission of a phonon, where the energy is dissipated in the crystal lattice, or Auger recombination where the energy is imparted to a third mobile carrier (electron or hole). At a recombination centre, the probabilities of electron and hole capture are virtually equal in order to result in the elimination of the e-h pair. Therefore their behaviour is more predictable and can be more easily controlled, which is vital for semiconductor devices. Efficient recombination centres often arise from metal impurities.

A deep level can act as a carrier trap or a recombination centre depending on its position in the bandgap and its emission or capture rate. Electron or hole traps have a high probability of capturing their respective carriers and releasing them after some time and under certain conditions. Therefore for instance at an electron trap the capture rate of an electron is much more dominant than the capture rate of a hole. Electron traps are therefore usually located closer to the conduction band, where electron capture and release can be more efficient. Similarly hole traps are usually closer to the valence band. In addition, electron traps are majority carrier traps in an n-type semiconductor

while hole traps are minority carrier traps. In the same way, in a p-type semiconductor hole traps are majority traps and electron traps are minority traps. Deep levels that behave as carrier traps have often a detrimental effect on semiconductor device characteristics. This is due to the fact that they alter the conductivity properties of the semiconductor by capturing free carriers and thus reducing the concentration available for conduction. The opposite effect of increased carrier density is experienced when carriers are released from traps and consequently conduction is enhanced. The major challenge associated with carrier traps in the bandgap of a semiconductor lies in effectively controlling the carrier capture and release, as well as predicting the trap's behaviour under specific conditions.

Shallow levels may also be present in the bandgap of a semiconductor and as the term implies, they are located closer to either the conduction or valence band than deep levels. In Si they usually originate by incorporation of atoms from the neighbouring groups III and V of the periodic table when these substitute Si atoms in the crystal lattice. Group V atoms have one electron in their outer shell that is not bound in a covalent bond and after replacing a Si atom they become donors as they can contribute this electron for conduction. Similarly group III atoms are acceptors in Si since they introduce holes and cause p-type conductivity. Donors are positive when ionized since they are missing their extra electron and acceptors have a negative charge when ionized as they have gained an electron. Shallow donor or acceptor levels in Si saturate the conductivity above 150K as they are then fully ionized.

Very commonly in Si, deep level defects are introduced by impurities belonging to groups of the periodic table other than III and V. However, intrinsic deep levels such as vacancies and interstitials are almost definitely present after certain processes used for semiconductor device fabrication and doping. High-energy particle irradiation and ion-implantation cause a wide range of lattice defects that introduce deep levels and quite frequently extended defects in the bandgap. Other techniques such as diffusion and oxidation can also increase the concentration of recombination centres. These affect many of the properties of the semiconductor and govern conduction, as will be seen in the following sections. Nonetheless they are essential for the doping or optimization of

the characteristics of semiconductors and much research has been performed to properly analyse the defects they produce.

2.3 Crystal Defects

Ideally the atoms in a semiconductor occupy specific lattice sites and are arranged in a periodic manner. However in real crystals, the presence of lattice defects or the thermal vibration of atoms can cause deviation from periodicity. Such imperfections include point or extended defects and dislocations. As the nature of these defects becomes more complicated, it is harder to control the properties of the semiconductor. There are three basic point defects that are currently important to investigate, namely vacancies, interstitials and substitutional impurities. A vacancy, as the word implies, appears when an atom moves away from its regular site. Even though vacancies are due to lack of an atom, they can carry electronic charge in the same manner that a hole is positively charged because it is the lack of an electron. Interstitials are atoms that sit on an interstitial site in the crystal and can be either from the same element as the crystal (self-interstitials) or from a different species. Substitutional impurities are atoms of a different species that substitute atoms of the host element in the crystal lattice and bond with them in a regular fashion, usually introducing new states in the bandgap. When an atom leaves its regular site and migrates to the surface leaving a vacancy behind, it is called a Schottky defect, while if an atom moves away from its site to occupy an interstitial site creating a vacancy-interstitial pair, it is then called Frenkel defect [1, 2]. An illustration of these defects is shown in Fig. 2.1

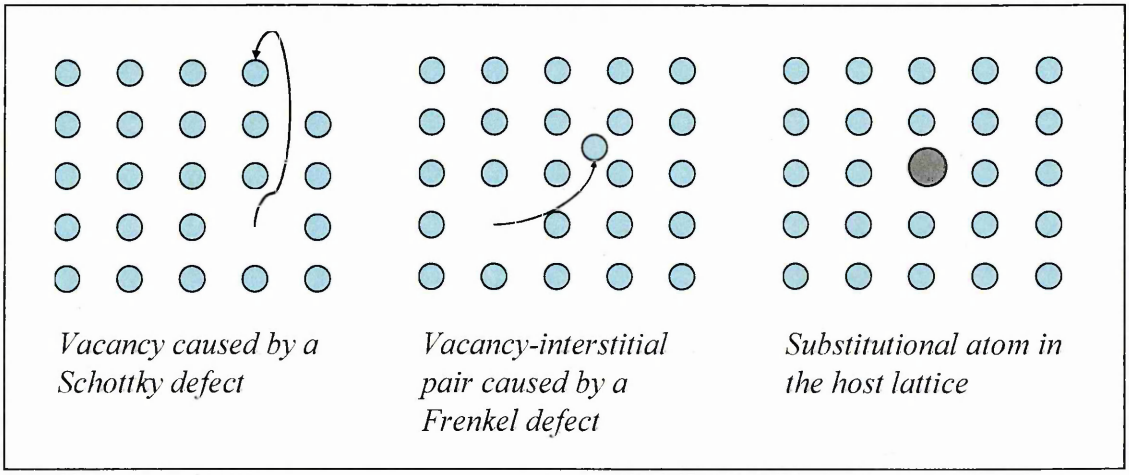

Figure 2.1: Schottky, Frenkel and substitutional defect in a semiconductor lattice

In Si in particular, these defects can be present during growth and their concentration is relatively small. However, if implanted, the most common way of introducing them on a larger scale is by doping. Doping is very important as it allows blending of the properties of two elements or more and hence can enhance the characteristics of the semiconductor. Most importantly, it is necessary for the formation of p-type and n-type semiconductors and hence for the fabrication of most semiconductor devices. However, the doping atoms inevitably cause displacement of the host atoms and introduce new energy states in the bandgap. In addition, as dopants are forced into the crystal, they increase the concentration of vacancies, interstitials and substitutional atoms. The atoms of heavier impurities more frequently occupy substitutional sites, while lighter atoms can most commonly be found at interstitial sites [1]. Although point defects appear to be the simplest form of crystal imperfection, they can often be found in larger aggregates. They can therefore form clusters of defects which have a much more complicating nature and are harder to examine or eliminate.

Dislocations are line defects that form when stress higher than the elastic limit of the crystal is applied. In this case, part of the crystal can slip relative to another part of the crystal forming dislocations. When the slip occurs in the direction of the applied stress, screw dislocations can be formed. However, if the atomic plane where the slip takes place is at right angles to the direction of the applied stress, then edge dislocations are created [1]. Moreover, the high impurity content formed by implantation damage may result in dislocation loops. Dislocations exhibit a dynamic behavior, as they can interact with other dislocations, they can change with the application of further applied stress or heating treatment and they can also dissociate into partial dislocations. Therefore they affect the electrical properties of the semiconductor by introducing electronic states in the bandgap in relation with other impurities or near the dislocation core. These are caused by dangling bonds that are created when dislocations form or dissociate. In addition, excess strain is imposed on the lattice due to an electric field around the dislocations [3]. Hence dislocations have an impact on the carrier lifetime, density and mobility in a semiconductor.

Another type of defect is a stacking fault, which is associated with the way the atoms bond in the crystal lattice. A stacking fault is generated when the sequence, with which

the atoms are bonded in the lattice of the semiconductor, is altered. Higher complexity defects such as twinnings and inclusions are called gross defects as they can involve several atomic planes. A twinning is identified as one part of a crystal forming a mirror image of another adjacent part, while the two parts remain in contact at the bounding surface. Twinning usually encompasses a high concentration of dislocations and can be formed due to mechanical shear. During growth, small particles of metals or dielectrics, called inclusions, can be absorbed into the crystal. Inclusions often interact with dislocation sites by forming precipitates. Inclusions have been observed at substitutional sites in Si after ion implantation of heavy metallic atoms, after spontaneous precipitation of the metal impurity located at the peak of the implant [4]. Twinning and inclusions during Si growth can be more easily prevented, as the conditions for their formation can be controlled and mechanical shear or metal impurities can be avoided. However, dislocations and stacking faults may occur even under normal growth conditions and can be generated in particular by the required doping process. Ion-implantation damage may not only create dislocations and stacking faults, but may also lead to even more stable extended defects after their interaction with point defects or after annealing.

Dislocations, as well as their interaction with point defects, have been extensively examined in silicon. In addition, Si deformation has been shown to produce point defects apart from dislocations, while the activation energy of the resulting defects depends on the initial strain applied and the doping of the material [5]. However, the majority of point defects generated during the applied strain can be annealed-out at high temperatures (~900°C), which enables a more precise study of the dislocations. Low temperature annealing of Si under stress appears to straighten the dislocation networks, though high temperature annealing after deformation decreases their density. The importance of controlling the deformation strain and temperature is emphasized by the fact that high deformation levels lead to more dangling bonds [3]. This may lead to acceptor states in n-type Si which in turn can cause Fermi level pinning below the mid-bandgap [5].

Various techniques have been implemented for the investigation of the nature, properties and electrical activity of dislocations, as well as to study their dissociation

and interaction with other defects. Transmission Electron Microscopy (*TEM*), Scanning Electron Microscopy (*SEM*) and Hall effect measurements can provide information on the dislocation density, structure and number of carriers captured on dislocation levels respectively [6, 7]. Electron-Paramagnetic Resonance (*EPR*) has been extensively applied to plastically deformed Si in order to examine the paramagnetic centres (*D-centres*) that are created during deformation. EPR results have been combined with Deep Level Transient Spectroscopy (*DLTS*) and the Electron Beam Induced Current (*EBIC*) mode of SEM in order to determine the electrical activity from dislocations and their capture and emission characteristics [6-9].

The D-centres that have been observed at the core of dislocations after deformation, have been shown by EPR to be associated with dislocation dangling bonds [7]. This result can be expected, since dislocations stem from broken crystal bonds along a lattice plane, but it also demonstrates that D-centres are localized in dislocation cores or in their vicinity. Of course the obtained EPR signal from such plastically deformed material may be due to the dangling bonds near or inside dislocations or may be due to clusters of point defects situated elsewhere in the crystal [8]. Therefore techniques such as DLTS that investigate the capture kinetic processes from defects are necessary to resolve the nature of these defects. Due to the fact that defects at a dislocation core are in very close proximity, carrier capture can be described as preferential. Hence the initial capture process may appear point-defect like, but only certain defects are filled that perhaps are located at more electrostatically favorable positions at the dislocation. Following this initial capture, a strong repulsive Coulomb potential will develop around the dislocations, which will gradually prohibit further carrier capture [7]. As this electrostatic potential varies continuously with time during carrier capture or emission, the resulting transient process will deviate from a typical exponential. In fact this non-exponential capture has been observed to have logarithmic time dependence as the number of filled deep levels is proportional to the logarithm of the filling time [8]. DLTS can still be used in such cases since relevant models have been developed for logarithmic transients from defects in heterostructures or alloys that can also be implemented in Si [8, 10, 11]. The electric field that arises in the depletion region of the semiconductor during DLTS measurements, can have the effect of slightly lowering the

height of the potential barrier around the dislocations, thus improving carrier capture or emission, or it can induce tunneling [7, 12].

As already mentioned, the density of dislocations in Si decreases after annealing because they dissociate into partial dislocations [5]. The EPR signal and DLTS spectra associated with D-centres appear reduced after annealing, which leads to the conclusion that reconstruction of dangling bonds at the dislocation core or around the dislocation has taken place [7]. DLTS spectra reveal that deep levels originating from point defects or point defect clusters usually disappear after high temperature annealing, if the defects are not located inside or close to dislocation sites. A similar reduction in the DLTS spectrum has been observed after annealing of deformed Si containing metallic impurities [9]. Metallic impurities are known to segregate or precipitate at dislocations giving rise to deep levels that severely affect the minority carrier lifetime [9, 13]. Impurities such as Fe, Ni, Cu and Au tend to form bonds with common Si dopants (e.g. B) and cause a decrease in the carrier lifetime when these bonds are broken. It has been observed that impurities at a dislocation core may have different electronic properties than in the ideal Si lattice. In particular, research on Ni contamination of Si containing dislocations has revealed that Ni creates energy states in a broad band instead of giving rise to a single energy level [9]. Finally, under the influence of an electric field introduced by techniques such as DLTS, redistribution of metallic impurity atoms along dislocations has been detected.

Despite the fact that defects caused by dislocations are very difficult to characterize, their interaction with point defects may also lead to electrically active levels. At dislocation cores there is much higher defect diffusivity than at other parts of the crystal and vacancies tend to migrate there. Glide dislocations dissociate into Shockley partials which are separated by stacking fault ribbons [6, 14]. Stacking fault ribbons however, have been reported to also participate in the vacancy migration mechanism [15]. Moreover as their size is larger than that of dislocations, any electrical activity from stacking fault ribbons would dominate the electrical behaviour of the semiconductor. As determined from EBIC analysis, stacking fault ribbons do not exhibit any significant electrical activity at room temperature even though their identification becomes difficult due to their low energy [6]. However, it is found that at stacking faults, the formation

energy of vacancies and self-interstitials, such as the [110]-split interstitial in Si, is lower than in the bulk [14]. This usually stems from the fact that at the stacking fault the point defect lies in a more relaxed structure than in the regular crystal lattice. A direct consequence of the lower formation energy of these defects at a stacking fault, is that after irradiation the latter could act as a sink for point defects. Hence after irradiation, the concentration of defects at stacking faults might be higher compared to that at dislocation cores [14]. The most important defects caused by the main doping technique in Si, namely ion-implantation will be examined in the following sections. Finally, high energy irradiation, such as that which occurs in particle detectors, will initially be considered.

2.4 Irradiation-related defects in Si

During irradiation of Si high energy particles, such as electrons, protons or neutrons are directed onto the semiconductor, collide with the host atoms and create an excess of Frenkel defects. These vacancies and interstitials are mobile at room temperature and thus migrate to different parts of the crystal. No excess ions are introduced through irradiation and the majority of the produced vacancy-interstitial pairs recombine in the bulk or at the surface. However, vacancies or interstitials that have avoided recombination either aggregate forming clusters or interact with impurities already existing in the crystal such as the commonly found C or O, P or B, depending on the conductivity of Si. Some of the resulting defects are stable and immobile at room temperature and tend to anneal out just above room temperature often leading to the formation of higher order defects or even extended defects. Nonetheless, irradiation is a useful excess carrier lifetime control technique which has been extensively used in industry since it can be applied after device fabrication. Although, recombination centres formed by irradiation are useful for controlling the device properties, they have been shown to anneal out, not only at high temperatures, but also with time [1].

2.4.1 Defects in p-type irradiated Si

A multitude of defects have been detected using a wide range of techniques in irradiated Si. The main defects induced by electron (e) irradiation in p-type Si include the divacancy signal, the carbon-oxygen-vacancy ($COVV$) level, sometimes referred to as the K-centre and the carbon substitutional-carbon interstitial pair (C_s-C_i). These

defects are not always present depending on the resistivity of Si used, the irradiation temperature and dose and the annealing treatment. Studies of carrier lifetime after electron bombardment of p-type Si, have revealed a level at ~0.21eV above the valence band, ascribed to the positive charge state of the divacancy, common to low resistivity, oxygen and carbon lean crystals [16]. Recombination in high resistivity e-irradiated crystals has been shown to be dominated by a level at 0.27eV attributed to the K-centre [17]. However, the position of this centre in the bandgap of p-type Si is usually measured at 0.35-0.38eV by other studies, thus differing in value, as Electron Paramagnetic Resonance (*EPR*), Deep Level Transient Spectroscopy (*DLTS*) and Thermally Stimulated Capacitance (*TSCAP*) techniques have shown [16, 18-20]. Under high-injection conditions the K-centre is positively charged and remains at this charge state for some time after the bias is turned off, resulting in an increase in the effective doping concentration [18, 21].

EPR and DLTS studies have shown a correlation between the K-centre and the C_s-C_i pair in p-type electron irradiated Si. The latter defect is formed when a mobile Si interstitial is trapped by a substitutional carbon, resulting in an interstitial carbon after annealing just above room temperature which is subsequently trapped by another substitutional carbon. Upon further annealing, DLTS revealed that the C_s-C_i peak at ~0.27eV above the valence band reduces while at the same time the K-centre peak at 0.39eV increases [22]. Hence it was proposed that annealing causes the breaking of the C_s-C_i pair after which the carbon-interstitial enhances the concentration of the K-centre. Similarly, in p-type proton (H^+) irradiated Si, DLTS measurements revealed a carbon-oxygen interstitial complex (C_iO_i) with activation energy at 0.35eV above the valence band. This level is present at low concentrations immediately after the H^+ bombardment, although its concentration increases with time [23]. The concentration of the C_s-C_i pair at 0.27eV however, reduces accordingly, indicating that the C_i is responsible for the growth of the C_iO_i complex in what appears to be an almost linear transformation. Hence the carbon interstitial is responsible for increasing the concentration of the K-centre in p-type electron irradiated Si, while in proton irradiated p-type Si it has the same effect on the carbon-oxygen interstitial complex.

In hydrogenated p-type e-irradiated Si another level has been detected with activation energy 0.28eV above the valence band [24]. This level only arises after annealing and is suggested to result from the hydrogenation of the K-centre and hence is due to a hydrogen-related complex, most likely attributed to the donor state of VOH. Electron traps have also been detected in p-type e-irradiated Si after annealing at 0.27eV below the conduction band, ascribed to an interstitial defect of oxygen and boron [19].

2.4.2 Defects in n-type irradiated Si

The identification of defects in n-type irradiated Si is much better documented due to the extensive research that has been performed. The main defects introduced both by electron and proton irradiation in n-type Si are the vacancy-oxygen (*VO* or *A-centre*), the doubly negative charge state of the divacancy ($V_2^{=}$) and the singly negative charge state of the divacancy (V_2^{-}) [25-28]. The A-centre is formed when migrating monovacancies, which are mobile at room temperature, get captured by interstitial oxygen atoms (O_i) and its activation energy has been determined by a vast amount of studies at ~0.18eV below the conduction band [29-32]. The A-centre has a large capture cross-section ($9*10^{-15}cm^2$) and can often be used as a monitor of the concentration of vacancies since O_i is usually the main impurity in Si [30]. The same studies yielded an activation energy of 0.23eV for the double negative charge state of the divacancy and 0.41eV for the singly negative charge state. It was found that the surface of irradiated n-type Si acts as a sink for vacancies, while their concentration increases with depth up to a saturation value and then remains constant for larger depths [25]. In addition, it was observed that the production rate of divacancies decreases at high electron irradiation doses. Furthermore, studies of vacancy related defect production yielded a decreasing tendency with increasing proton irradiation flux [26].

Interaction of vacancies with dopants usually yields a vacancy-dopant centre. In particular in n-type e-irradiated Si the phosphorus-vacancy centre (*VP* or *E-centre*) is very commonly found and has been detected at ~0.45eV below the conduction band. The fact that it is located very close to the single negative divacancy level (0.41eV) means that it is difficult to resolve through typical electrical studies. However, the implementation of high resolution techniques, such as Laplace DLTS (*LDLTS*) and the

fact that the dissociation energy of the E-centre (at ~180°C) is lower than that of the divacancy have allowed the separation of these two levels [27, 29]. In n-type e-irradiated Si of high carbon content an additional defect is usually resolved overlapping with the A-centre that originates from a carbon substitutional-carbon interstitial pair and has an activation energy ~0.16eV below the conduction band [20, 27]. In addition, after annealing intended to dissociate the E-centre, the C_s-C_i complex also reduces in concentration in e-irradiated n-Si, while the formation of a new C_s-C_s level at 0.21eV below the conduction band is revealed [33]. High annealing temperatures above 350°C in n- and p-type Si can result in thermal double-donors being formed. These have an effect on the doping concentration as they are usually very shallow levels and can therefore exchange carriers very easily with the conduction or valence band [18].

In the case of proton-irradiated n-type Si, apart from the typical vacancy-related defects other hydrogen-related levels have been detected [26, 34]. These are located at 0.32eV and 0.45eV below the conduction band. The former level exhibits similar annealing behaviour to the well-characterised VO centre and appears in samples with high oxygen content. Therefore it was attributed to a VOH complex. The same conclusion, concerning the level at 0.32eV was reached by hydrogenation of e-irradiated n-type Si [24, 35-37]. Hydrogenation has the effect of passivating the VO centre and hence reducing its concentration while introducing a level deeper in the top half of the Si bandgap. The VOH complex has an emission rate that is lower than that of the A-centre as was determined by LDLTS analysis [36].

The second hydrogen-related level at 0.45eV is located near the singly negative divacancy level and the E-centre but has been successfully resolved and attributed to a V_2H complex [34, 36]. It exhibits similar annealing behaviour to the divacancy in particular in oxygen lean samples and does not appear after helium irradiation which indicates that it contains hydrogen. EPR and LDLTS studies have revealed a VH complex almost with the same activation energy as the V_2H complex and close to the E-centre. Finally, higher order vacancy-hydrogen complexes (VH_2, VH_3, VH_4) have been identified using Fourier Transform Infra-red spectroscopy (FTIR) in proton or deuterium irradiated n-type Si [38].

Neutron irradiation has also been applied to Si detectors exhibiting typical vacancy-related defects such as the A-centre and the different divacancy charge state defects [39]. A much deeper level at ~0.54eV below the conduction band, which was attributed to a different charge state of the double vacancy was detected, as well as two deep levels closer to the valence band. As will be examined in the following section, high energy particle-irradiation may introduce crystallographic defects, which may lead to the presence of extended defects.

2.5 Ion-implantation defects

Ion-implantation is the bombardment with different ion species intended to produce Si with certain properties. It is the most widely used technique at present for the doping of Si and hence for controlling its conductivity and for the formation of semiconductor devices, although less aggressive plasma doping is being developed by equipment manufacturers. A very broad range of dopants has been employed including the main dopant impurities B, P, As, C and Sb. Others such as Si, Ge, Sn, and Er are used for pre-amorphizing implants, light emitters or to increase radiation hardness in detectors. Very frequently throughout the literature, ion implanted Si is compared with e- or proton irradiated Si in order to distinguish between the main defects and impurity related defects. However, the significant difference between irradiation with electrons (or protons) and ions, is that in the latter case the ion stays in the sample creating a further defect. Once again in ion-implanted Si, due to the bombardment with foreign species, vacancies and interstitials are created by the collisions that are very mobile at room temperature and may therefore form other defects. In addition, subsequent annealing is necessary for the activation of the dopants and often results in more stable or higher order defects. The very frequently observed phenomenon of Transient Enhanced Diffusion (*TED*) of B or other dopants, involves diffusion of the dopant species away from the implanted region very rapidly. This results in a very broad profile and is the origin of formation of complicated extended defects. In modern semiconductor technology where very well contained dopant profiles are required offering the possibility of reducing the device dimensions, TED of dopants is undesirable and will be examined in the following section in detail.

Typically the same vacancy-related defect levels are created in ion-implanted and irradiated Si, although vacancy clusters may also arise. The VO centre and the different charge states of the divacancy are usually present, as well as the vacancy-dopant (E centre) level located very close to the singly negative divacancy. In n-type B implanted Si, the substitutional carbon-interstitial carbon complex is also detected overlapping with the A centre [30]. Another level arises at 0.35eV below the conduction band which is usually detected as a long tail extending at lower temperatures next to the singly negative divacancy defect in a DLTS spectrum. This level has been reported in B, C or Si doped n-type Si and is being associated with a low order defect containing carbon [31, 32, 40, 41]. The concentration of this level with depth revealed that it has a broader profile extending towards the surface than the singly negative divacancy level, indicating that it is not due to migrating vacancies but less mobile species such as carbon which may form carbon interstitials and hence interact with impurities. Due to the fact that it appears to anneal out at low temperatures (150°C), it is more likely that it is not due to a complex of carbon involving divacancies [32]. However, this level is not present after implantation with heavier dopants such as Sn [40].

Vacancy-related defects caused by ion-implantation of different mass atoms have shown that the implantation temperature has an effect on the production rate of the vacancies. In particular, as the implantation temperature increases the concentration of defects involving vacancies increases [40]. Moreover the concentration of vacancy-related defects increases with dose rate for light dopants. For higher mass dopants, a threshold dose rate was observed after which the production rate of vacancies decreased with increasing dose rate. This is ascribed to the fact that the interstitials originating from heavier dopants require more time to diffuse due to the long collision cascades and can therefore recombine with vacancies faster [41].

Detailed research has been performed in detecting clusters of defects arising from ion-implantation before annealing in an effort to predict stable complex levels caused by annealing. Dopants of increasing ion mass (Si, Ge, Er) revealed high concentration of defects located at ~0.4eV below the conduction band which was shown to originate from a complex of defects rather than a point defect [27, 42, 43]. Analysis of these levels with high resolution LDLTS and capture cross-section measurements while

varying the fill pulse length, demonstrated exponential capture with time, indicating a complex of defects or an extended defect that was not removed by annealing. Earlier work on Er implanted Si had shown a multitude of donor states whose luminescence was shown to increase after annealing [44]. A multitude of interstitial clusters was also observed both in n- and p-type Si after high temperature annealing [45].

A different study on metal impurities and the distinction between two very close spaced levels was achieved by LDLTS measurements of Au in n-type Si [46]. This work did not involve ion-implantation but diffusion of Au and subsequent hydrogenation of the surface. However, it is mentioned here to discuss defect levels arising from the incorporation of Au and to demonstrate the high resolution capability of LDLTS. One of the four charge states of the Au-H complex in n-type Si, namely the G4 complex, is believed to have a very similar electrical signature as the Au acceptor level estimated between 0.55-0.56eV below the conduction band. LDLTS allowed the accurate spatial identification of the G4 complex and the gold acceptor at ~0.54eV and ~0.56eV respectively below the conduction band [46, 47].

In p-type Si implanted with a high dose of C a defect level not involving vacancies was detected at 0.41eV above the valence band possessing a large capture cross section [48]. Upon annealing, the initial level that exhibited interstitial behaviour was seen to cluster with oxygen interstitials forming the C_iO_i interstitial complex at ~0.38eV above the valence band. Complex behaviour was observed after DLTS measurements for the formation and evolution of this level [48, 49]. Exponential capture with time was detected and a large capture cross-section after high temperature annealing at 450°C indicating the stability of this level at high temperature. Implanted p-type Si has been shown to yield complex levels related to the background B doping. In particular, at 0.26eV above the valence band a boron interstitial–carbon substitutional complex (B_iC_s) has been revealed. Another deeper level at 0.45eV above the valence band can also be detected and is attributed to an interstitial complex that embodies B [28]. These levels arise when the B content is significantly larger than the carbon concentration. In this case interstitial B will be formed rather than interstitial carbon which promotes the formation of B–related levels.

Low dose implantation of p-type Si with different atoms, including H, B, Si and Ge, indicated that the defects produced are not related to the dopant impurity, contrary to n-type Si implanted with H where the VOH and V_2H complexes are formed [50]. Apart from the positive charge state of the divacancy and the C_iO_i interstitial complex that are well characterised, another deep donor level is present at 0.52eV above the valence band, possibly due to a metallic impurity incorporated during growth, such as Cu. The resulting level may be due to an interaction between the carbon-oxygen interstitial and the metal impurity. At increased implantation doses however, the concentration of the seemingly point defect-like levels increases to a point that higher order complexes are formed [49, 50].

High resolution studies of the vacancy-dopant level arising around 0.44eV below the conduction band for different dopants (P, As, Sb), were successful in separating these levels from the divacancy as well as differentiating amongst these, when a combination of dopants were implanted in the same sample [51]. This clearly demonstrated the efficiency of the LDLTS technique although it was noticed that the presence of many implants in the same sample, have the effect of altering the electrical signature of the E-centres compared to single or double implants. Finally a breakthrough study involving a combination of DLTS and Minority-carrier transient spectroscopy (*MCTS*), revealed the presence of a donor level in the bandgap of Si attributed to the phosphorus-vacancy level [52]. This donor level is located at 0.27eV above the valence band and its detection was possible due to the injection of both minority and majority carriers achieved optically through MCTS. The presence of this level will affect the modelling of dopant diffusion in Si which is known to be associated with the E-centre.

2.6 Transient Enhanced Diffusion

It has been observed that ion-implantation results in the formation of a vacancy-rich region extending from the surface of the implanted Si to the peak of the implant and a subsequent interstitial-rich region until the end-of range of the implant [28, 30]. Moreover studies have shown that the dopant concentration arising from ion-implantation is not always contained in the original implanted region, but dopants such as B tend to diffuse deeper into the substrate. An anomalous transient diffusion is particularly observed after high temperature, short-time anneals which leads to

broadened B profiles [53]. This phenomenon comes in contrast to the well-controlled, steep dopant profiles that are required for shallow-junction fabrication required by the downscaling of semiconductor devices. For B doping in particular, it is known that after implantation, substitutional B atoms are introduced in the host lattice which then tend to diffuse away from the implanted region. This is achieved because the B atoms are known to couple with interstitial Si atoms, which were generated during implantation. Hence, the now mobile, B interstitial complexes cause dopant diffusion [54].

Unlike irradiation with high energy particles which eventually does not introduce any foreign atoms in the host lattice, ion implantation causes an increase in the concentration of charged ions, mobile or immobile, at the particular implantation temperature. These interact with the created vacancies and interstitials often causing their annihilation while a residual interstitial population is usually observed in the aftermath, even following sufficient annealing upon which most vacancy-related defects have dissociated. Moreover, rapid thermal annealing (*RTA*) is known to cause the initial clusters of defects that were created during implantation to agglomerate into larger clusters [53]. Dissociation of these clusters results in the release of trapped interstitials increasing their concentration. Since point defects such as interstitials, are highly mobile they tend to enhance transient dopant diffusion. An additional trapping of host interstitials is caused by extended defects when they are present after high temperature annealing. A variety of techniques, such as TEM, Secondary Ion Mass Spectrometry (*SIMS*), DLTS and photoluminescence (*PL*) have been implemented for the observation of Transient Enhanced Diffusion (*TED*) in Si and for the identification of its origin [49, 55-58].

High resolution images have shown that large extended defects can exist in the region of the implant where transient diffusion is taking place. These were identified as rod-like or {311} defects, although after higher energy implants or higher temperature anneals even dislocation loops may be distinguished [58]. These {311} defects are formed through precipitates of interstitials and are known to unfault into dislocation loops after very high temperature annealing [59]. The {311} defects trap Si interstitials that have diffused into the bulk after the initial dissolution of point defect clusters that were

formed during implantation. During annealing these defects undergo Ostwald ripening which involves constant capture and emission of interstitials leading to a saturated concentration and subsequent re-emission of interstitials. The concentration of {311} defects eventually reduces during annealing while their size has been observed to increase [58]. As these interstitials diffuse away into the bulk or towards the surface they couple with dopants thus generating mobile dopant interstitials, which then diffuse away causing enhanced diffusion [54]. Less dopant diffusion has been observed for high carbon containing Si, as interstitials pair with carbon instead, resulting in fewer mobile interstitial-dopant pairs.

A number of interstitial clusters of defects have been observed after implantation and annealing of p-type and n-type Si [45]. When the implantation dose increases, a higher interstitial population is available resulting in the formation of more thermally stable clusters. The same result is also reached when lower impurity concentration is ensured as fewer interstitials are trapped by impurities. A wide range of studies have been performed in order to produce reduced TED in B doped Si. Recently F^+ implantation has been shown to eliminate TED and even reduce B thermal diffusion. Dislocation loops in the interstitial region of the fluorine implant are presumed to trap interstitials and hence reduce TED. Similarly small vacancy-fluorine clusters are suggested to contribute to the suppression of B thermal diffusion [60-62].

2.7 Ultra-Shallow Junctions

The general trend of reducing the size of integrated circuits (*IC*s) requires a reduction in the size of devices and as a direct consequence the semiconductor device dimensions also have to shrink. This also increases the device packing density and frequency response and the current drive. The latter inversely depends on the channel length (L) of Metal-Oxide-Semiconductor-Field-Effect-Transistors (*MOSFET*s). As the electric field throughout the device should be maintained constant, reducing L, causes a roll-off of the threshold voltage which can be diminished if the junction depth is also decreased. This is the main drive behind the constant need for achieving shallower junctions. In the simple diode configuration, this also means a reduced depletion region width which can be accomplished if high doping concentration is implemented. However, careful adjustment of the doping conditions is necessary in order to control

the depth of the junction and methods for eliminating TED are of high technological importance.

Different methods have been devised for the formation of ultra-shallow junctions (*USJs*). Plasma immersion, where the substrate to be doped is immersed in plasma containing the dopant species before high voltage is momentarily applied, is one of the techniques investigated. It is a quick and inexpensive method requiring only low implantation energy and has been applied using a AsH_3 plasma source. Due to the use of arsenic, a steep concentration-depth profile was achieved near the ~90nm wide n^+p junction with the substrate and a two-step anneal ensured dopant activation [63]. Electrical characterisation was performed using current-voltage measurements and it was concluded that low implantation energy (<10keV) and long anneal times (>60s) may result in junctions containing less trap centres [63]. 50nm-wide p^+n USJs were realised by decaborane ion implantation and demonstrated promising results by exhibiting low TED and thermal diffusion of B [64]. Low energy (5-15keV) As ion implantation was performed for the formation of n^+p USJs followed by high temperature (650-950°C) annealing and TEM was used for the analysis of extended defects at the implantation end-of range. Dislocation loops were detected, with increased density for higher temperature anneals, which also dissolved at higher temperatures for higher energy implants. Lower energy implants resulted in shallower dopant concentration profiles which also exhibited less As-TED with however higher sheet resistance [65].

Point defect engineering has been used by high energy Si co-implantation to inject vacancies in ion-implanted Si which eventually annihilate part of the interstitial population and result in reduced TED and sharper junctions [66]. A different study examined the effects of B implantation into preamorphised Si followed by solid-phase epitaxial growth (*SPEG*) which showed that self-interstitial emission from the implanted layer occurring during SPEG controls dopant-interstitial clustering [67]. Finally ultra-low energy ion-implantation, in the order of 500eV-1keV, has been investigated for the formation of shallow junctions where low sheet resistance values were achieved [68]. The challenge in such a low energy regime is developing appropriate annealing schedules yielding high dopant activation.

2.8 Conclusion

This chapter initially discussed the main properties of deep and shallow levels as well as recombination centres in Si. Doping and impurity incorporation were considered next, as well as the generation and identification of point defects. A wide range of crystallographic and impurity-induced extended defects, such as dislocations, stacking faults and inclusions were presented. These are often found after the intensive processing and doping methods required by the current semiconductor device fabrication. The defects generated by irradiation and implantation were investigated extensively and phenomena such as transient-enhanced diffusion of dopants were considered. These have a serious effect on the device performance, ability to control dopant activation, and eventually the size of the devices required to provide high efficiency structures. Finally, the requirements for ultra-shallow junction-based devices were given and methods that have lead to successful implementation of such structures were detailed, while certain challenges associated with such efforts were outlined.

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Chapter 3: Diamond properties and defects

3.1 Introduction

For more than a century, silicon has been the most widely studied semiconductor material. Elaborate investigation of its properties, characteristics and defects has been performed and techniques have been developed to control and enhance its features. The vast majority (99%) of semiconductor devices presently used and fabricated by the electronics industry require the implementation of Si. This material however has reached its maximum potential and physical limitations, mostly stemming from its small bandgap (1.12eV), low carrier mobility and poor thermal conductivity, indicating that different materials are necessary for the future generations of electronics particularly for power electronics and RF applications. These limitations have driven the recent expanding interest in wide bandgap materials (*WBG*). Due to the inherent properties of these materials arising from their wide bandgap, efforts have focused on the research and fabrication of devices implementing WBG semiconductors in order to overcome obstacles currently faced by the Si semiconductor technology. Such devices would have improved characteristics enabling high temperature operation, high switching frequency, high power and voltage capabilities and may allow higher packing densities in the design of ICs, while at the same time device failure will be reduced. Moreover WBG materials are promising candidates for optoelectronic applications such as light emitting devices and lasers that cover a wider range of the electromagnetic spectrum. Before this point is reached however, WBG semiconductors have to be thoroughly investigated, widely reproducible characteristics have to be ensured and fabrication and production costs have to be minimised. In addition much work is required in order to develop the necessary techniques to control the properties of these semiconductors and to enable compatibility with current Si-based technology. The present work examines the electrical properties of semiconducting diamond as the most promising wide bandgap material for electronic applications after a short overview of the necessity of such research and the availability of other materials. The structure, properties and growth techniques of diamond are explored and a detailed analysis of the defects present in this material is given.

3.2 Need for wide bandgap materials

The growing need for higher efficiency, voltage and power ratings in modern semiconductor devices and the increasing problems from the implementation of Si, entail an urgent requirement for materials with better properties. One of the major limitations of Si is temperature, since above 150°C there are excessive conduction losses. In addition the need for heatsinks or cooling systems in order to maintain devices such as power converters below the maximum temperature for operation can be expensive, space consuming and size-limiting [1]. Furthermore the heat produced by the devices themselves contributes to the overall harsh environment operation that Si semiconductor devices undergo, coupled with increased switching losses and high forward and reverse current leakage. WBG materials have exhibited reduced current losses compared to Si at high temperatures and can be used at these temperatures potentially eliminating the need for cooling mechanisms or snubbers to reduce switching losses. WBG semiconductors such as different polytypes of silicon carbide (SiC), gallium nitride (GaN) and diamond have outstanding electrical properties and can contribute to the improvement of current semiconductor devices and eventually replace Si. Table 3.1 shows the predicted physical properties of these materials compared to Si and gallium arsenide (GaAs), that are currently being used [1].

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.54
Dielectric constant, ε_r	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field, E_c (kV/cm)	300	400	2500	2200	2000	10000
Electron mobility, μ_n ($cm^2/V \cdot s$)	1500	8500	500	1000	1250	2200
Hole mobility, μ_p ($cm^2/V \cdot s$)	600	400	101	115	850	850
Thermal conductivity, λ ($W/cm \cdot K$)	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity, V_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7
Breakdown voltage V_B (V)		2	56	46	34	514

Table 3.1: Physical properties of Si, GaAs and important wide bandgap semiconductors

The breakdown voltages for the materials illustrated in Table 3.1 for a typical p-n diode were calculated from the corresponding properties of each material using Eq. 3.1 as follows [1, 2]:

$$V_B \approx \frac{\varepsilon E_C^2}{2qN_D} \qquad \text{Eq. 3.1}$$

where ε is the relative permittivity (dielectric constant * permittivity in vacuum ε_0) of the materials in Table 3.1, E_C is the electric breakdown field and N_D is the doping density. The values of breakdown voltage for all materials were calculated for the same doping density and then normalised to that of Si for comparison. Hence the values shown in Table 3.1 indicate that diamond has the highest breakdown voltage which is 514 times greater than that of Si. Consequently much higher doping densities can be used in these semiconductor materials while at the same time avoiding diode breakdown at low voltages. Some of the most important properties of the WBG materials shown in Table 3.1 and the areas where their implementation would be most advantageous in semiconductor devices are briefly explained in the following sections.

3.2.1 High temperature operation

As already mentioned electronic devices for certain applications have to be able to operate at high temperatures. In particular devices used in power systems and transportation or for aerospace and military operation should be able to maintain their electrical characteristics at high temperatures so that device failure can be prevented [1]. In contrast to Si where carriers may obtain sufficient energy to be promoted to the conduction band at high temperatures, in WBG semiconductors this is not possible until much higher temperatures. Another very important aspect of device operation is the intrinsic carrier concentration (n_i) which increases with temperature. This can be verified from Eq. 3.2 [3].

$$n_i^2 = N_C N_V \exp(-E_g / kT) \qquad \text{Eq. 3.2}$$

where N_C and N_V are the effective density of states in the conduction and valence band of the semiconductor respectively, E_g is the bandgap, k is Boltzmann's constant and T is the temperature. The intrinsic carrier concentration therefore exponentially increases

with temperature while it reduces for larger bandgap semiconductors. In order to further discuss the importance of temperature on n_i Fig. 3.1 shows the intrinsic carrier densities of Si and different WBG materials (SiC polytypes and diamond) with temperature [4].

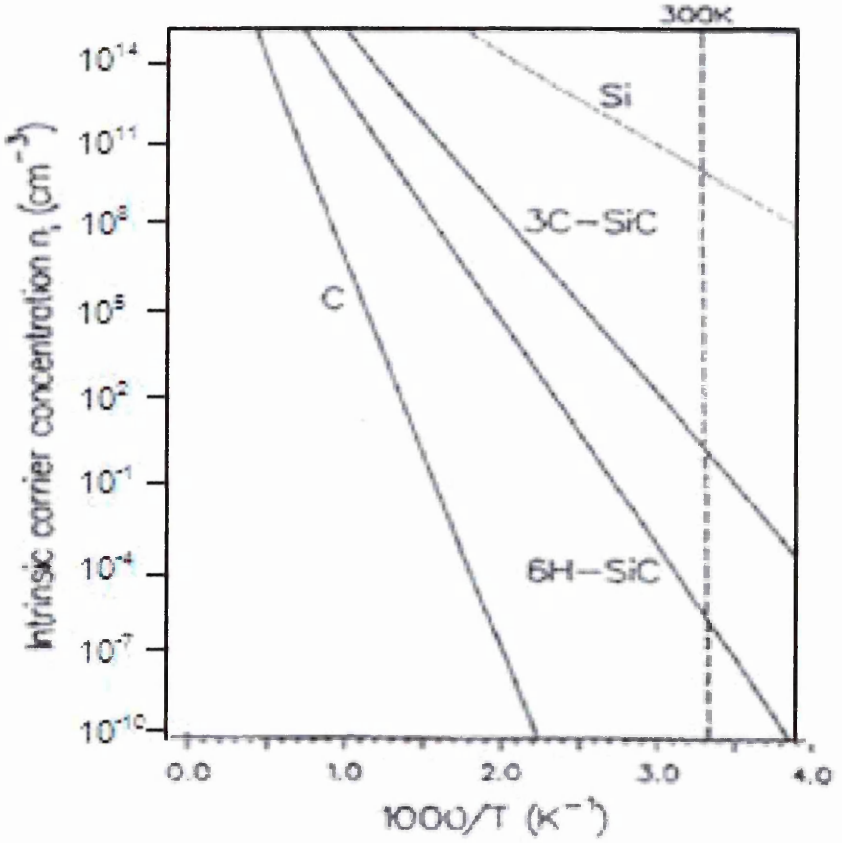

Fig. 3.1: Intrinsic carrier concentration plots of Si, diamond and SiC polytypes against the reciprocal of temperature [4].

As expected due to its small bandgap Si has the most temperature dependent n_i out of these materials. At room temperature the intrinsic carrier concentration of Si is about $1*10^{10}cm^{-3}$ but it rapidly increases to about $1*10^{15}cm^{-3}$ when the temperature reaches around 550K. In a semiconductor device where doping is used to control the properties of the material, a high value of n_i entails that the device characteristics may be dependent on the intrinsic carrier density rather than the doping density. Although this is relative to the magnitude of the doping concentration, it now becomes apparent that in Si devices at temperatures higher than 500K, it is the intrinsic concentration that may dominate the device characteristics instead of the doping density. This in turn suggests that Si at high temperatures in these devices will tend to behave more as an intrinsic semiconductor and the designed doping will have no effect in the properties of the

material as the Fermi level will be comparable to the intrinsic Fermi level. Moreover n_i continues to increase with temperature and is about $10^{17}cm^{-3}$ at 750K, which would make it comparable to the doping density of even highly doped Si. In contrast, as seen from Fig. 3.1, diamond has an extremely low intrinsic carrier concentration, which even for temperatures as high as 1500K does not reach $10^{13}cm^{-3}$. Hence diamond based structures would entirely eliminate the danger of the intrinsic concentration governing the device's performance.

The leakage current of rectifying contacts, which is related to the minority carrier population, should be greatly reduced for WBG materials where the intrinsic carrier concentration is very low. An important current leakage mechanism is thermonic emission which depends on the metal-semiconductor barrier height of Schottky contacts. The barrier height however, is also related to the bandgap of the semiconductor and practically its magnitude can be up to three quarters of the bandgap depending on the metal used. For Si in particular the maximum barrier height can be 0.9eV for metals such as Pt while for the frequently used Al this value is around 0.6eV [3]. For wide bandgap materials however the barrier height is much larger which limits the leakage current due to thermionic emission. In addition the carrier density with energy higher than the barrier height that can contribute to thermionic emission increases exponentially for higher temperatures while it decreases for larger Schottky barrier heights [3, 4]. Therefore Schottky barrier contacts of WBG semiconductors have lower thermionic emission related leakage currents. Moreover some WBG materials such as GaN and diamond have higher carrier mobility than Si, which is an important factor in device operation as it is directly related to the current. Above room temperature however, mobility starts to decrease due to phonon scattering, reducing the value of current through the device and hence materials with higher mobilities may be more suitable for higher temperature applications [5]. Therefore as temperature is an integral part of many semiconductor device parameters and influences the device performance and lifetime, it is critical to implement WGB materials which possess better characteristics for high temperature operation than Si.

3.2.2 High electric breakdown field

Unipolar devices such as MOSFETs and Schottky diodes have lower conducting and switching losses than the currently used insulated gate bipolar transistors (*IGBT*) and p-i-n diodes. However they are not used in applications such as transportation where high voltage or power ratings are necessary, because higher breakdown voltages require larger areas to sustain the high electric field, which in turn incurs higher costs [1]. Table 3.1 demonstrates that WBG materials have higher electric breakdown field than Si or GaAs, which as shown from Eq. 3.1 is required for the manufacturing of devices with higher breakdown voltages and hence they can be useful for the fabrication of FET and Schottky diodes with high voltage ratings. Due to the high electric breakdown field of WBG semiconductors, higher doping concentrations can be used even for high breakdown voltage, which also entails that the drift region of power devices can be made thinner and will have lower resistance. The thickness of the drift region (W) can be expressed from Eq. 3.3:

$$W = \frac{2V_B}{E_C} \qquad \text{Eq. 3.3}$$

For a given value of breakdown voltage (V_B), the width of the drift region can be found, for different electric fields that correspond to different semiconductor materials from Table 3.1. As a result, SiC p-n junction drift regions can be almost 7 times thinner than those made of Si, while diamond drift regions can be 33 times thinner. Since diamond possesses the highest value of breakdown field it offers more flexibility in the fabrication of devices while varying the doping density, the thickness of the drift layer, the breakdown voltage or even the breakdown mechanism. The fact that WBG materials can produce thinner drift regions can also assist the reduction of losses in reverse operation mode as the storage of minority carriers can be expected to be lower. Finally another device parameter that can benefit from the high electric field of WBG materials is the on-resistance of the drift region as it is inversely proportional to the field. Especially at high breakdown voltages where contact or channel resistance can be neglected, WBG semiconductors can have on-resistance values orders of magnitude smaller than Si [1].

3.2.3 High saturation drift velocity

Under the influence of a small electric field, the carriers in a semiconductor will move along the field with a drift velocity in addition to their thermal velocity. This drift velocity (U_d) is given by Eq. 3.4 [3]:

$$U_d = -\mu_n E \qquad \text{Eq. 3.4}$$

where E is the electric field, μ_n is the electron mobility and the minus sign denotes the drift velocity of electrons that move opposite to the direction of the field, although the same equation without the negative sign holds for holes in the valence band. Eq. 3.4 therefore shows that the drift velocity of carriers is proportional to the mobility. Therefore for WBG materials which possess higher carrier mobility than Si, it is clear that the drift velocity of the carriers will be higher. In addition the linear dependence of the drift velocity on the electric field in Eq. 3.4 holds for low electric fields while as the electric field becomes larger, U_d increases less rapidly and finally approaches a saturation drift velocity (U_S) [3]. The high-frequency switching capability of a semiconductor material is directly proportional to the saturated drift velocity. Consequently WBG materials are expected to yield higher frequency switching than Si based devices, since their saturated drift velocities are more than twice larger than that of Si. Since transistors are frequently designed to operate as switches in digital applications the transit time of minority carriers across the base of the transistor must be reduced. Hence designs for high frequency transistors incorporate small base widths. The use of WBG semiconductors may facilitate these designs since, as previously discussed, thinner base regions can be achieved, whilst maintaining high breakdown voltages due to the high supported breakdown fields. Furthermore the higher mobility values of WBGs lead to quicker removal of minority carriers from the base region for these transistors. For diodes fabricated by WBG semiconductors, high drift velocities also mean that the charge can be removed faster from the depletion region of the diode, which entails smaller reverse recovery current and hence shorter reverse recovery time [1, 3]. Moreover, even devices based on changing conductance, such as pulse generator core switches, can improve by the implementation of WBG materials due to the higher mobility values.

3.2.4 High thermal conductivity

As the features in electronic devices get smaller, power consumption and heat generation have become an increasing problem. Thorough planning for the heat dissipation needs to be taken into account in the fabrication, development and packaging of semiconductor devices in order to avoid device failure. In addition to high temperature operation and internal device losses, user input such as overclocking of computer components has to be considered. As already mentioned WBG semiconductors have superior properties that can be exploited in devices where high temperature operation is required. Another significant feature of certain WBG materials and in particular SiC and diamond is their high thermal conductivity which reflects their ability to dissipate the heat flux. Especially, diamond has 15 times better thermal conductivity than Si and can potentially be used for cooling systems and heatsinks.

The thermal conductivity (λ) of a material is inversely proportional to the thermal resistance from junction-to-case ($R_{th\text{-}jc}$). An efficient heatsink should have high thermal conductivity in order for the $R_{th\text{-}jc}$ to be small, which denotes that the heatsink dissipates power without rising in temperature much higher than its surrounding air. It is important for the heatsink to easily conduct heat so as to prevent the temperature of the semiconductor device from rising abruptly [1]. Table 3.1 shows that diamond has the best thermal conductivity of all WBG materials, which suggests that devices based on diamond, may potentially even avoid the need for a cooling system. Finally such devices or heatsinks may allow higher packing densities due to diamond's exceptional thermal management properties.

3.3 Wide bandgap semiconductors

Before semiconducting diamond is examined as the wide bandgap material with the best electrical properties as seen from Table 3.1, other important WBG semiconductors that have already been implemented in certain electronic devices are briefly presented in this section. SiC and GaN have long been investigated in order to improve their growth techniques and device fabrication methods, as well as to enhance their properties, in an effort to alleviate some of the problems that are currently faced by the Si industry.

3.3.1 Silicon carbide

Silicon carbide has been the focus of the most elaborate study in comparison to the rest of the WBG semiconductors, due to its well known potential for high temperature, high power, high frequency and radiation resistant applications. High electric field strength, high thermal conductivity and high electron saturated velocity are some of SiC's most attractive characteristics accompanied by the large number of SiC polytypes available. The latter are differentiated by the stacking sequence of each tetrahedrally bonded Si-C bilayer and are composed of one or a combination of three crystallographic categories namely cubic, hexagonal and rhombohedral. While the cubic polytype 3C-SiC is not currently available in bulk form, 4H-SiC and 6H-SiC, which have a mixture of cubic and hexagonal bonding, have been commercially available in bulk wafer form for the past 15 years [6].

Growth of single crystal (*SC*) SiC suitable for electronic applications has been much more difficult than polycrystalline growth. In addition, vapour phase growth techniques are preferred compared to liquid phase methods mainly due to the very high temperatures and high pressure required for solution growth [7]. During the physical vapour transport (*PVT*) technique, SiC powder is sublimed at high temperatures and Si and C-containing gas species are then re-crystallized into a single crystal seed at a slightly lower temperature. The growth behaviour can drastically change by even a slight temperature shift or modification in the species distribution, as growth takes place in a quasi-closed graphite crucible. Consequently the main challenges of this widely used technique are controlling the temperature and the gas species concentration fields, which affect the polytype transition, mass transfer and defect formation amongst other parameters. Micropipes, which are bulk defects that propagate the length of the boule from the seed crystal, are the main impediment of SiC. Moreover the ingot purity depends on the purity of the SiC powder and hence the difficulty here lies in obtaining pure SiC boules while controlling the doping level. Small wafers with low dislocation densities (~100cm^{-2}) have been achieved demonstrating the possibility of eliminating structural defects [8] while larger wafers have also successfully been produced. The current industrial wafer size is 3 inch wafers establishing SiC as the WBG semiconductor with the most mature market and availability [7]. A different vapour phase technique currently rising in value is the high temperature chemical vapour

deposition (*HTCVD*) process. Its main advantages include continuous source material supply, the ability to grow long ingots, control of the C/Si ratio and the availability of high purity gases. Other techniques such as halide-CVD, modified-PVT and continuous feed-PVT are still under development because they offer further control of certain growth parameters over the standard PVT sublimation process [7]. The liquid phase growth method offers the advantage of lower dislocation densities compared to other techniques. However, the low C solubility in silicon at temperatures below 1800°C leads to major difficulties such as the handling of liquid Si at high temperatures and the control of the growth front. Although certain solutions have been proposed to confront these issues further research is necessary before production can start [7].

Epitaxially controlled doping and hot ion implantation are implemented for the doping of SiC. N is most commonly used for n-type doping of SiC while p-type doping is achieved by incorporation of Al, B, Be, Ga, O or Sc. The challenges of ion implantation of SiC include the choice of the optimum temperature implant and high temperature anneal. In addition, B can be more suitable for p-type doping than Al due to the fact that it is lighter and consequently the damage caused in the lattice is less severe and more controlled. Although epitaxial doping does not inflict any lattice damage, ion implantation offers the advantage of selective doping [6]. An important property of SiC is the ease with which oxidisation to SiO_2 can occur, which also renders it compatible with the Si fabrication technology. Nevertheless high interface and oxide trap densities have been observed, and obstacles such as oxide breakdown in certain configurations require further research and development.

The reliability and low resistivity of ohmic contacts is crucial for high temperature and high frequency operation. Ohmic contacts on p-type SiC are fabricated by Al/Ti alloys although due to the fact that Al oxidises easily, alternative methods including boron-carbide (B_4C) have been developed. Ohmic contacts on n-type SiC are formed from a variety of silicides and carbides where Ni_2Si has been observed to have low specific contact resistance which becomes even lower at higher temperature (500°C) [6]. The metal-semiconductor barrier height is an important factor in the fabrication of Schottky contacts for high temperature operation and for high voltage switching applications. For SiC Schottky contacts the barrier heights depend on the quality of the surface, the

deposition method, the conductivity, the polytype and on whether the surface is Si or C-face. High barrier heights have been achieved with Au or Ni for Schottky contacts on Si-face SiC while a variety of other metals can also be used (NiCr, Pt, Ti, Mg, Co, Al, Hf, Pd) [6].

SiC has only 1% and 3% lattice mismatch with AlN and GaN respectively, in addition to the large number of available polytypes, which demonstrate the vast potential of this semiconductor in heterojunction-based devices. SiC as a WBG semiconductor can produce higher output power in microwave and power devices compared to Si or GaAs and RF, and high frequency SiC devices are rapidly approaching commercialization. Metal-semiconductor field effect transistors (*MESFETs*) have already exhibited record power densities, although surface passivation is required to eliminate surface trapping effects [4]. Due to the fact that electron mobility reduces at high temperatures, the channel current of SiC MESFETs at 300°C is only around 55% of that at room temperature. Hence careful design and simulation of these devices is necessary [9]. SiC metal-oxide-semiconductor field effect transistors (*MOSFETs*) have at least two orders of magnitude lower on-resistance than their Si counterparts, which will enable their application in circuits where higher voltage and current ratings are required. However, further work should be undertaken to evaluate the reliability and breakdown behaviour of oxides on SiC before their implementation in commercial applications.

The use of SiC for the fabrication of diodes suitable for microwave applications or with rectifying properties has recently been investigated [10]. In particular, improved performance was observed in devices such as the impact-avalanche-transit-time (*IMPATT*) diode, where the critical field, saturation velocity and thermal conductivity are very important parameters for the amplitude of the microwave signal. Higher efficiency can potentially be obtained from double-velocity IMPATT diodes based on Si-SiC heterojunctions since the aforementioned parameters have higher values for SiC. Due to the higher saturation velocity in SiC, the resistance of the drift region, where the heterojunction is located, becomes negative for a wider frequency range than in single velocity Si IMPATTs, resulting in an increase in the magnitude of the microwave power [10]. Similarly the higher saturation velocity of SiC compared to Si or GaAs can be advantageous for barrier injection transit-time (BARITT) and tunnel transit-time

(TUNNET) diodes, where higher frequency performance can be achieved due to the fact that the charge carriers move at their saturation velocities after tunnelling [4]. Measurement of SiC Schottky diodes indicates lower forward voltage and higher breakdown voltages (~ 5000V) compared with Si Schottky diodes (~100V). In addition higher voltage-blocking capacity has been observed while reduced drift layer thickness than in Si-based diodes is required. Suitable materials for reduced barrier Schottky contacts and annealing conditions have been investigated to improve thermal stability [4]. Finally, the main impediment of forward-bias drop degradation with time for SiC p-i-n diodes has been studied and attributed to stacking faults and techniques are being developed to overcome this problem [11].

3.3.2 Gallium Nitride

Gallium nitride (GaN) has an even wider bandgap than SiC, higher saturated electron drift velocity, higher carrier mobility and higher electric breakdown field compared to Si. A broad range of devices fabricated from GaN or from a combination of AlGaN/SiC heterostructures, encompass high-electron mobility transistors (*HEMT*s), short wavelength optoelectronic devices, lasers, and heterojunction and switched diodes which have exhibited very promising characteristics [4]. A GaN-based blue laser diode is used in the recently developed Blu-ray disc technology. Compared with Si and SiC, GaN Schottky diodes have the advantage of negligible reverse recovery current and hence lower switching losses. The most important disadvantage of GaN is the lack of a native oxide which is an essential requirement for the fabrication of MOS devices. In addition difficulty in growing GaN wafers has led to thin layers of the material being epitaxially grown on SiC or sapphire [1]. Lattice mismatch between GaN and SiC or sapphire substrates introduces a high density of threading dislocations and techniques such as lateral epitaxial overgrowth and cantilever epitaxy, have been utilized in order to reduce their density. Moreover technological developments have resulted in crack-free GaN surfaces, the discovery of p-GaN and eventually the fabrication of p-n junction light emitting diodes (*LED*s), with applications in blue and green LEDs, violet laser diodes and ultraviolet photodetectors [12]. N-type doping is usually achieved with Si, while magnesium is used for p-type doping. The introduction of dopant species results in point [13] and cluster defects that need to be fully characterised and reduced

as they act as luminescence quenching centres [4]. A further drawback in the use of GaN is its low thermal conductivity (lower than Si) that entails poor heat dissipation, which is a significant hindrance for high power, high temperature device operation. Growth of GaN on the aforementioned sapphire or SiC substrates, improves the overall thermal conductivity of the structure.

Heterojunctions such as GaN/SiC and AlGaN/SiC grown by different techniques, have been investigated in order to provide improved performance in LEDs, laser diodes, heterojunction bipolar transistors (HBTs) and heterostructure-field-effect transistors (HFETs). For the n-p configuration of the GaN/SiC diodes, a low turn-off voltage has been widely observed. This was attributed to a tunnelling assisted recombination process, arising from the conduction band offset, which leads to high electron and hole concentrations near the conduction and valence bands respectively [14]. Schottky barrier measurements enabled calculation of the negative conduction band offset which is considered responsible for the low turn-on voltage.

Research has also focused on heterointerfaces such as GaN/AlGaN with different Al compositions for the fabrication of diodes and transistors. These involve the formation of a two-dimension electron gas (*2DEG*) in GaN where it was suggested that the Schottky barrier height may be temperature dependent [4]. Electrical characterisation of such diodes indicates that the conduction band offset is mostly independent of the Al composition, however effects such as the tunnelling assisted recombination process previously observed in GaN diodes, should appear reduced for increased Al incorporation. Further work on the GaN/AlGaN heterojunction involves the development of low resistance ohmic contacts for applications in transistors. A metal structure based on Ti/Al/Mo/Au yielded satisfactory results although optimisation of the annealing process is required [4]. Hence while GaN optoelectronic devices have been studied more thoroughly and are commercially available, additional work is needed for the development of GaN-based devices for different electronic applications.

3.4 Diamond

The structure and origin of diamond are presented in this section. In addition, the most relevant growth techniques are explained and its properties are introduced.

3.4.1 Diamond origin and structure

The word diamond originates from the Greek root *adamas*, meaning invincible, which denotes the fact that diamond is one of the hardest natural materials known. It is one of the few materials that have industrial application and can also be used as a gem stone. Its growth in nature requires very specific conditions. It can be formed under high pressure (between 45-60 Kbars) but relatively low temperature is required (900–1300°C). These conditions are met either very deep in the lithospheric mantle or at meteorite impact craters. Diamond is the allotrope of carbon in which all carbon atoms are tetrahedrally sp^3 bonded and it crystallises in the face centred cubic lattice. Some sp^2 bonding may be included due to re-bonding of broken bonds causing electrical conduction in diamond. It is a very wide bandgap material (5.5eV) that can be considered as an insulator but when doped it exhibits semiconducting properties. N-type diamond doping uses nitrogen or phosphorus as the dopant species while p-type doping is achieved by boron incorporation. Doping creates donor and acceptor levels situated deep in the bandgap of diamond and therefore exchange of carriers with the valence and conduction bands does not occur unless finite energy is provided. Consequently diamond has almost no conduction at room temperature which however can be increased at higher temperatures and also depends on the doping concentration. Diamond has a broad optical transparency, ranging from the deep ultra-violet to the far infra-red due to its large bandgap which gives rise to its insulating behaviour at room temperature [15]. The wide bandgap and very strong sp^3 bonding result in a material of extreme hardness with outstanding chemical, mechanical and electronic properties. However, the full potential of diamond has not been reached because processing and control of its properties require high temperatures, as is the case for SiC. Nevertheless recent progress has yielded promising results as will be seen in the following sections.

3.4.2 Natural diamond classification

Pure natural diamonds are expected to be transparent and colourless. However, most diamonds found are not colourless due to the fact that they contain crystallographic defects including impurities and structural defects that cause the coloration. Depending on the nature or quantity of defects and on their ability to absorb or transmit light, diamonds are categorised into two main types.

Type I diamonds: The main impurity in these diamonds is nitrogen and the majority of natural diamonds are of this type. They absorb in both the infrared and ultraviolet region, from 320 nm and can have visible absorption spectrum. Depending on the nitrogen content and bonding Type I diamonds are separated as:

- Type Ia: Are diamonds containing a high concentration of nitrogen atoms (~0.3%), in pairs or grouped in evenly distributed aggregates. Almost 98% of gem diamonds are of this type.

- Type Ib: Nitrogen atoms in these diamonds are dispersed throughout the crystal in isolated sites. While natural Type Ib diamonds are rare, they can be synthesized industrially containing less nitrogen by substitution of nitrogen by carbon atoms.

Type II diamonds: Diamonds in this category contain very few nitrogen impurities and are very rare in nature. They transmit light in the ultraviolet region below 225nm and have no discernible visible absorption spectrum.

- Type IIa: These diamonds are very rare and contain structural anomalies arising through plastic deformation during crystal growth.

- Type IIb: They are extremely rare in nature but can be synthesised industrially. Type IIb diamonds contain scattered boron within the crystal matrix and are p-type semiconductors unlike other diamonds that are mostly insulators.

3.4.3 Synthetic diamond growth

The method used since the 1950s and developed earlier than that, to produce diamond is the High-Pressure-High-Temperature (*HPHT*) technique. As the name suggests this technique implements very high pressure (5GPa), produced by large belt or cubic presses and high temperature (~1500°C), to create conditions suitable for diamond growth similar to those that exist in the earth's mantle. This technique can grow single crystal diamond up to a few mm in size from metal solvated carbon under HPHT conditions. The continuous improvement of this technique over the years has led

to crystals with very high purity and crystallographic structure perfection similar to that of natural type-IIa diamond. In addition HPHT can be implemented for high quality single crystal epitaxial film growth on the (100) faces of synthetic diamond. The small diamond crystals grown by HPHT have been very widely used in machine and cutting tools after hardening and sintering. However, larger area diamond films are necessary for electronic applications as well as a more cost effective growth method.

The second most commonly used method for synthetic diamond growth is the chemical vapour deposition (*CVD*) technique. Efforts to synthesise diamond from the gas phase under much lower pressure than that needed in HPHT originated in 1958. Improvement of growth rates, the discovery that any deposited graphite can be etched by atomic hydrogen and the ability to use different substrates for diamond growth, were some of the most important advances that followed [16]. CVD creates the necessary environmental circumstances for carbon atoms in a gas to be deposited on a substrate in crystalline form. The mixed gas species diffuse towards the substrate after thermal (hot-filament) or plasma (microwave, dc, rf) activation. The activation process creates ions and electrons which together with the entire set of particles are involved in complex reactions. Only part of the mixed gas volume will successfully react with the substrate to form diamond as adsorption back into the gas phase is also possible. During CVD growth the desired doping can be incorporated into the diamond film by including the required dopant atoms into the gas mixture. Fig. 3.2 shows diagrams of a hot-filament and a microwave plasma CVD reactor [16].

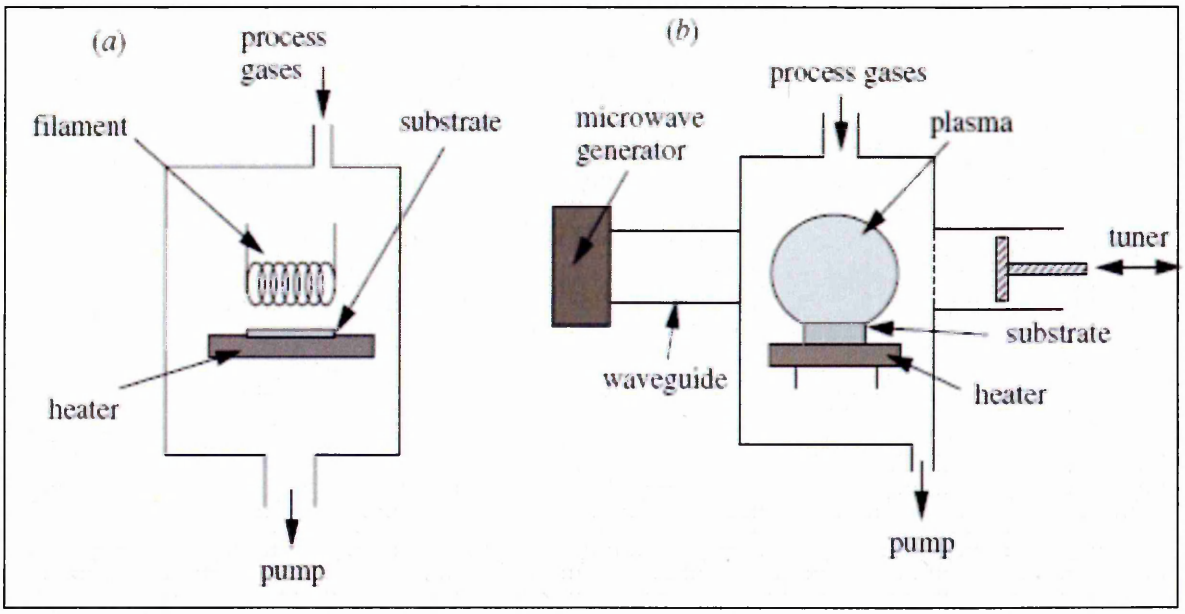

Fig. 3.2: Examples of a) hot-filament and b) microwave-plasma CVD reactors [16]

Hot-filament chemical vapour deposition (*HFCVD*) growth takes place in a vacuum chamber implementing a substrate heater to bring the substrate up to a temperature of 700–900°C. The hot filament is heated at temperatures in excess of 2200°C and is located a few millimetres above the substrate. Good quality polycrystalline diamond films can be grown with HFCVD at an approximate rate of 1-10μm/h and at a relatively low cost. One of the disadvantages of this technique is that the filament is sensitive to oxidising or corrosive gases, therefore limiting the variety of gas mixtures that can be employed [16]. However, recent advances in the HFCVD technique have made possible the growth of small single crystal diamonds under specific conditions, which after further research may be the onset of larger scale single crystal growth for electronic applications [17].

For microwave plasma chemical vapour deposition (*MPCVD*) growth, microwave power is coupled into the chamber via a dielectric window in order to create a discharge. The microwaves couple energy into gas phase electrons, which in turn transfer their energy to the gas through collisions. This leads to heating and dissociation of the gas molecules, the formation of active species, and finally diamond deposition onto a substrate, which is immersed in the plasma. Some of the advantages of MPCVD compared with other growth techniques include higher power and higher achievable growth rates (>10μm/h) and the potential to use a wide variety of gas mixtures due to the fact that no filaments are required. Recent advances using MPCVD have been reported for the growth of single-crystal diamond, where the substrate stage design and methane concentration have been optimised [18]. High quality diamond at high growth rates (50-150μm/h) was achieved while varying the reactant gas pressure, concentration and substrate temperature for enhanced growth and crystal purity [19]. Common prerequisites for CVD techniques involve the use of substrates with melting points higher than that required for diamond growth (>700°C), to avoid deposition of other forms of carbon and that the precursor gas (CH_4) has to be diluted in an excess of hydrogen [16].

3.4.4 Diamond properties

As was seen in Table 3.1 diamond has the most amazing properties compared to all the other WBG semiconductors with definite superiority to Si and GaAs. Because of

the large bandgap and electric breakdown field of diamond, diodes with very high breakdown voltages can be feasible. However, mostly low breakdown voltage diodes have been demonstrated due to the inability to control the impurities present in the material. The strong bonding and high atomic density of diamond generally prevent the incorporation of much larger atoms in the crystal. The most commonly found impurities include hydrogen, nitrogen, boron and silicon although hydrogen is known to bind with some of the impurities, thus rendering them inactive. Therefore well-designed incorporation of impurities is necessary to produce high breakdown voltage diodes. Annealing of the diamond films (>700°C) has been shown to remove the hydrogen and very high breakdown voltage Schottky diodes (6000V) have been recently reported [20].

Intrinsic properties of diamond such as high carrier mobilities combined with the high breakdown field can be implemented in the fabrication of power diodes and high frequency transistors where exceptional performance can be anticipated. In particular natural semiconducting diamond has the potential in such applications due to its high purity. This is because scattering mechanisms caused by extended and point defects limit mobility, especially during high temperature operation. High quality HPHT or CVD diamond can also have improved properties and is currently available commercially. However polycrystalline and highly oriented diamond produced by these techniques has reduced electron and hole mobilities due to the energy barriers at grain boundaries [21]. Single crystal diamond approaches the properties of natural diamond although large area production is a major disadvantage. High quality homoepitaxial, single crystal MPCVD diamond grown on 100-oriented HPHT substrates, has exhibited very high electron (4500 cm^2/Vs) and hole (3800 cm^2/Vs) mobilities, demonstrating significant potential for use in electronic devices [22].

Both natural and synthetic diamond have extreme mechanical hardness and wear resistance. The technological progress in synthetic diamond growth has made it much more affordable and therefore its application in cutting tools for non-ferrous materials has greatly increased. Other important properties include low thermal impedance and compressibility and superb resistance to chemical corrosion. In addition, the high saturation carrier velocity at high electric field as well as the wide bandgap and the low

dielectric constant enable fast switching operation and can reduce capacitive loading at high frequencies [4]. Moreover diamond has the highest sound velocity among all materials due to the fact that it possesses the highest Young's modulus (90GPa), which indicates the stiffness of the material. Hence signals can propagate faster in diamond devices, which make it attractive for surface acoustic wave (*SAW*) device applications. CVD diamond can be very useful for such applications where thin films can be combined with ZnO layers, which account for the lacking piezoelectricity in diamond. Certain companies are already implementing diamond based SAW filters in mobile phone equipment [4, 16].

The high packing density of electronic devices in modern circuits causes large volumes of heat flux which has to be dissipated appropriately in order to avoid overheating and eventual device failure. Diamond possesses high thermal conductivity and stability at high temperatures and pressures and is an excellent electrical insulator, which can be used for the rapid removal of local heating [15]. Consequently a variety of thermal management applications of diamond have surfaced such as submounts for integrated circuits, heat spreaders for high-power laser diodes or even as substrate material for multi-chip modules. Therefore the use of diamond can yield higher packing densities and improve the reliability of devices at high temperatures. Furthermore its use as an insulator can be ideal for low losses at millimetre-wave frequencies [4, 16].

Due to diamond's distinctive optical properties arising from its wide bandgap, research focus has been oriented towards the production of optoelectronic devices. Transmitters are of special interest for effective light emitting structures in electro-optical systems. Light emitting diamond structures yielding electroluminescence of different colours has already been observed that could lead to diamond-based laser diodes in the visible spectrum as electroluminescence of the H3 centre was obtained [23]. In addition its optical transparency may be implemented for the realisation of optical windows transparent over an extremely wide range of wavelengths. The wide band gap of diamond combined with its radiation hardness and high break-down field is used to realize detectors for UV radiation, nuclear radiation and high-energy elementary particles. Elaborate research has been performed on the deep and shallow defects present in natural and polycrystalline diamond that influence the performance of

irradiation exposed detectors [24, 25]. Thermally stimulated current (TSC) and photoconductivity techniques have been applied for the investigation of such defects in diamond detectors. It has been shown that the presence of shallow levels has more impact on the device performance and that post growth techniques can greatly enhance important material parameters such as mobility and carrier lifetimes [26].

Differences in the properties of natural and synthetic diamond arise from the growth techniques used to produce synthetic diamond and are related to the impurity incorporation during growth. In particular, the resistivity of natural diamonds can be much higher (10^{16} Ωcm) than that of CVD diamond (10^{6} Ωcm) at room temperature, although as the temperature increases, the resistivity of natural diamond (type-Ib) can be even lower than that of B-doped synthetic films [5, 27]. Hydrogen is implemented for passivation of deep traps and results in lowering the resistivity of these films, although subsequent annealing may lead to increased resistivity by expulsion of hydrogen. Moreover, the activation energy of B in natural p-type semiconducting IIb-diamond has been found to be 0.36eV [28], while it has been reported much lower for B-doped films (0.11eV) [29]. In addition, the orientation of homoepitaxially grown B-doped diamond films can have an effect on the carrier concentration and mobility of the material. For instance, films grown on (100) oriented substrates have higher mobilities and better crystallinity than those grown on (110) substrates for the same amount of B incorporation during growth [29].

Negative electron affinity: The electron affinity (χ) of a semiconductor is defined as the energy difference between the conduction band (E_g) edge and the vacuum level. For most commonly used semiconductor surfaces the vacuum level lies above the conduction band and hence these materials have positive electron affinity (*PEA*). This creates an energy barrier for electrons that prevents them from leaving the surface of the material. In the case where surplus of energy is provided by photoexcitation, electrons that have been promoted to the conduction band, gradually lose their energy by inelastic collisions with other electrons and phonons. The thermalised electrons will not have enough energy to overcome the potential barrier and to exit the material into the vacuum due to the PEA. Only electrons at the surface and within the inelastic scattering length

may be able to overcome the barrier and reach the vacuum level as photoelectrons [30]. On the contrary, if the vacuum level lies below the conduction band minimum at the surface of a semiconductor, then this surface exhibits negative electron affinity (*NEA*) with $\chi<0$. In this case thermalised electrons can be emitted from the surface into the vacuum. If the electrons were excited by photoexcitation, a photoemission spectrum can be detected whose analysis can be used to investigate properties and defects of the bulk of the semiconductor and not just the surface. This is because in surfaces that exhibit NEA, the escape depth of the electrons is the diffusion length, which is larger than the scattering length, thus allowing for examination of the bulk of the semiconductor [30]. Fig. 3.3 shows the band diagram of a material exhibiting negative electron affinity, where E_V is the valence band maximum, E_g is the bandgap and hv is the energy of the photon.

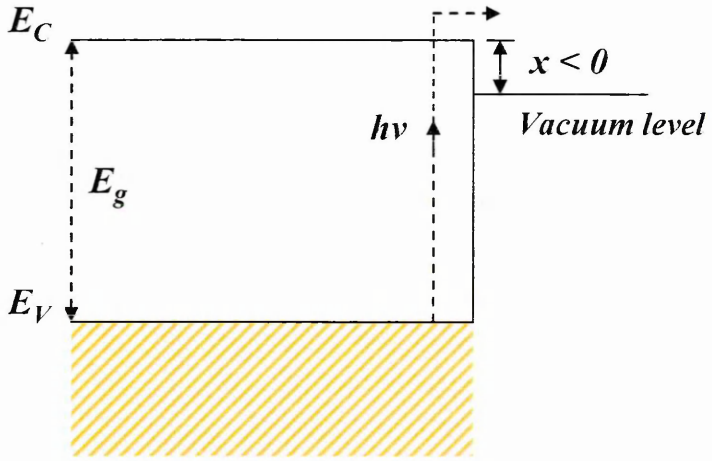

Fig. 3.3: Typical semiconductor surface showing negative electron affinity

IIb-type natural (111) diamond with p-type conductivity has been shown to exhibit NEA through photoemission and secondary-electron energy distributions [31]. A large quantum yield was obtained for a broad phonon energy range attributed to a combination of NEA and the large bandgap of diamond. The presence of NEA on the (111) diamond surface was later associated with the presence of hydrogen on the surfaces [32]. The hydrogen on the surface desorbs at about 900°C, leading to the reconstruction of the diamond surface and hence to the loss of the NEA and the appearance of a positive electron affinity [15]. The reconstructed surface is considered to be hydrogen free and it is also related to the appearance of intrinsic surface states. A difference between the impact of atomic and molecular hydrogen was reported

indicating that atomic hydrogen restores the as-polished electronic diamond surface structure. Investigation of the mechanics leading to electron emission from NEA surfaces, reveal that exciton break-up at the surface greatly contributes to the total electron yield for near-bandgap excitation photon energies. Moreover this is believed to be the dominant photoelectric mechanism driving emission from as-polished (111) diamond surfaces [33, 34].

Further research on p-type natural diamond with (100) surface orientation also showed surfaces displaying NEA which was related to hydrogen termination of the surface unsatisfied bonds resulting to dihydride-terminated surfaces. Photoemission spectroscopy measurements, after annealing of the diamond wafers at different temperatures, demonstrated NEA as the annealing temperature increased. The onset of NEA was observed after a temperature anneal at 1035°C while desorption of oxygen and simultaneous surface reconstructure were also detected [32, 35]. Synthetic diamond can also be prepared to display NEA and experiments have been carried out on intrinsic, B-doped p-type and P-doped n-type CVD diamond [36]. Total photoyield spectroscopy revealed optically induced electron transitions from the valence band maximum, directly to the vacuum level, in samples with low defect concentrations and independent of the position of the Fermi level. The negative electron affinity was calculated at -1.1eV. Particularly in n-type diamond, an upward band bending at the surface is caused by a layer of ionised P donors near the surface arising from the diffusion of electrons into the vacuum.

Doping: The tight bonding of carbon atoms in diamond makes incorporation of dopant species difficult. Large substitutional dopant atoms may also introduce lattice distortion and become the centre of point of clusters of defects. In addition only relatively small atoms are required in order to replace carbon in vacancy sites. As diamond has a very large bandgap it is necessary to ensure that doping can introduce relatively shallow donor or acceptor levels that can enhance conduction even at room temperature. Furthermore conventional doping techniques such as diffusion have not shown promising results while ion-implantation, routinely used in Si doping, can cause larger defects that are hard to remove by annealing [15]. The combination of the above

factors, limit the dopant species and methods that can be used to effectively dope diamond in a controllable manner.

Hence most frequently B is used as the p-type dopant introducing an acceptor level at 0.37eV above the valence band. Possible n-type doping may be achieved with N, which is frequently found in natural diamonds, but has a very deep donor level at 1.7 eV which impedes donor activation even at high temperatures. In synthetic diamond films doping with N is achieved by introducing N_2 or nitromethane in the precursor gas during diamond growth [37]. N incorporation is believed to enhance the grown diamond film quality. Certain alkali such as Li and Na may have potential for n-type doping by occupying interstitial sites and contributing to conduction with their outer electron, though experimental results have shown high resistivities and have not been conclusive or reliable [5]. Co-doping of diamond with B and S, O or H has been considered to yield shallower acceptor or donor levels than simple B doping. This is due to the fact that energy levels of isolated impurities tend to shift at lower donor or acceptor levels when complexes are formed. Particularly intense H passivation of B doped epitaxial layers has shown n-type conductivity although high temperature (~650°C) processing caused the original p-type conductivity to return [15]. Recently P doping has been successfully accomplished introducing a much shallower donor level than N which however differs in activation energy amongst studies from 0.4-0.6eV with experimental values being higher than the theoretical calculations [38].

B has been the most widely used and characterised doping species in diamond. Despite the fact that its acceptor activation energy is relatively small compared with other diamond dopants, it is still sufficiently high resulting in incomplete ionisation of the doping concentration [5, 39]. As already mentioned, the rare IIb-type natural diamond contains B and has often been used for homoepitaxial growth and characterisation of synthetic diamond films [28, 40-43]. B doping is most frequently used for the growth of p-type synthetic diamond films grown by the different CVD techniques. This is achieved by the incorporation of B in the gas mixture in the form of B_2H_6 most commonly or $(CH_3)_3B$ [20, 44]. Low energy B implantation is usually implemented for the formation of ohmic contacts near the surface of the diamond as will be explained

later. This results in a thin graphitized layer that can be removed before contact deposition.

Successful n-type, P-doped diamond films homoepitaxially grown on synthetic type-Ib substrates of (111) surface were recently achieved [38]. This signified a breakthrough in the ability to produce n-type conductivity diamond films with a shallow donor level although it appeared growth was somewhat restricted to the (111) orientation of the diamond. P doping was introduced by the incorporation of phosphine (PH_3) as the dopant source during diamond MPCVD growth. Low methane concentration and higher than ordinary substrate temperature were required for the formation of high quality polycrystalline diamond films that allowed the detection of the donor level at 0.43eV. This discovery subsequently led to the formation of p-n diamond diodes epitaxially grown on (111) single crystal diamond substrates [44]. These exhibited relatively low leakage currents (10^{-10}A), and high mobilities for (111) epitaxial layers but high resistivity which may not allow high frequency operation. Ultra-violet light emission was observed and the B and P levels were reported at 0.37eV and 0.59eV respectively. More recently photoelectrical optical absorption techniques combined with optimised P doping conditions revealed the existence of new levels, pointing out the need for careful selection of doping concentrations [45]. Finally, P doping of (001) single crystal diamond films was demonstrated based on plasma enhanced CVD yielding an activation energy of 0.58eV for the donor level [46]. As different methods of P doping which do not include PH_3 but are based on organophosphorus materials were explored, in an effort to reduce the vapour pressure during growth, it was shown that hydride phosphorus source gases should be preferred [47].

Electrical contacts: The aforementioned superb properties of diamond establish it as one of the most important candidates capable of fulfilling the requirements for ever-growing high power and frequency electronic devices operating under harsh conditions. Hence, the development of suitable electrical contacts, Schottky and ohmic, that allow the maximum potential of diamond's properties to be utilized are of high importance. Theoretically, rectifying contacts should have a sufficiently large barrier height that prevents any leakage current under reverse bias conditions. For natural p-type semiconducting diamond, non-reactive metals such as gold or aluminium are used for

the fabrication of Schottky contacts [48]. However, in polycrystalline diamond, the same metals may often produce ohmic contacts depending on several factors such as the diamond surface treatment before metal deposition, the doping level near the surface, or the deposition and annealing temperatures. Natural (IIb) diamond Schottky diodes exhibiting excellent rectification fabricated by Au, Pt or phosphorus-doped polycrystalline Si have been realised [41]. Very low leakage current, of a few pA, was measured for the Au contact diode, while that of the remaining diodes was even lower. The forward current-voltage (*I-V*) characteristics indicated that carrier transport was not only governed by thermionic emission but evidence of deep states was apparent.

Schottky Al or Au diodes on MPCVD grown polycrystalline diamond demonstrated the potential for high temperature operation, high breakdown voltage and low leakage current twenty years ago [49]. The resistivities of the undoped polycrystalline films were found to be comparable to those of undoped single-crystal diamonds leading to similar activation energies of deep acceptor levels. Furthermore extensive studies on Schottky diamond diodes employing different metals have been performed for the calculation of their work functions and electronegativities [50]. Most metals were found to yield Schottky contacts on as-grown polycrystalline diamond in the absence of any previous surface treatment, with the exception of Pt, Au, Cu and Ag. The application of different surface treatments was devised to change the surface termination from hydrogen to oxygen-terminated and this had an effect on the type of contact formed on diamond. This can be achieved by, exposition to O_2 plasma or treatment in a CrO_3 in H_2SO_4 at 200°C followed by a rinse in a 1:1 solution of H_2O_2 (30%) and NH_4OH (70%) at 90°C. This caused the previously ohmic contacts formed by Pt, Au, Cu and Ag to demonstrate rectifying properties, with similar I-V characteristics to the Schottky diodes formed by the majority of the other as-deposited metals without the oxidization treatment. In addition, a subsequent short 5 min exposition to a H_2 plasma reverts the oxidisation effect on these diodes, to once again yield ohmic characteristics. Therefore adsorption of oxygen has the effect of changing the surface properties of diamond producing Schottky electrical contacts for a wide range of metals.

Since most metals when deposited individually on the as-grown diamond surface will produce a Schottky contact, the fabrication of ohmic contacts is more difficult and requires careful investigation. Good ohmic contacts should only cause a small or negligible potential drop compared with the rest of the device and should hence have low resistance. However, such contacts are difficult to produce due to the large barrier heights that generally form when metals are deposited on wide bandgap materials such as diamond. Moreover the dangling bonds on the surface of diamond give rise to surface states, which have the effect of pinning the Fermi level at the surface and have more influence on the barrier height than the work function of the metal [51]. Additional problems for the formation of ohmic contacts include poor adhesion of noble metals and smooth surfaces that yield low conductivity. Deliberate roughening of the surface before metal deposition has been shown to enhance conductivity. Furthermore the method of deposition of transition metals has been widely implemented to enhance the diffusion of Au, Pt, Cu or Ag. Transition metals such as Ti or Ta have a strong affinity for carbon and form low resistivity carbides, which enhance the diffusion of noble metals that are subsequently deposited [52].

For natural and polycrystalline semiconducting diamond heavy doping by ion-implantation near the surface of the diamond has been used to reduce the width of the potential barrier at the metal/semiconductor interface which results to enhanced tunnelling and improved conduction. A thin graphitized layer that forms due to the implantation damage can be chemically removed by a 30 min boil in CrO_3 + H_2SO_4 solution at 200°C before the bilayer of a transition/noble metal is deposited. In this method, parameters such as the implantation dose and temperature are crucial for the fabrication of low resistivity ohmic contacts [53]. Ti/Au contacts were reported to deliver good ohmic contact performance while annealing of the contacts is necessary for the more desirable lower resistivity effect. It was generally observed that Ti/Au or Ta/Au contacts require a 1 hour temperature anneal at around 850-880°C to exhibit optimum ohmic characteristics although further annealing had no effect on the properties of the ohmic contacts [52, 53].

Studies on the effect of B implantation near the surface, in order to facilitate the formation of ohmic contacts, have shown that the sheet resistivity of the polycrystalline

diamond films reduces by at least an order of magnitude after implantation [54, 55]. Metallization was achieved by r.f. sputtering of Ti/Au or Ta/Au bilayers and a subsequent 10 min annealing at 500°C resulted in a reduction of the specific contact resistivity by three orders of magnitude ($\sim 1*10^{-6}\ \Omega cm^2$). The effect on the same annealing of simple Au ohmic contacts was also determined and yielded a two orders of magnitude decrease of the contact resistance ($\sim 5*10^{-4}\ \Omega cm^2$). It was concluded that the effect of r.f. sputtering of the bilayer ohmic contacts was to facilitate interdiffusion between Au and the diamond films which was further enhanced by the annealing, resulting in much lower resistivities. Research on the filament temperature during diamond HFCVD growth has showed that it is possible to obtain either Al ohmic or Schottky contacts just by increasing the filament temperature during growth [48]. Rectifying Al contacts were obtained at the highest filament temperature of 2373 K while it was also shown that any amorphous carbon content of the diamond films decreases as the filament temperature increases from 2173 K to 2373 K.

3.4.5 Defects in diamond

Defects in semiconductors degrade the performance and lifetime of devices, especially if they are introduced unintentionally and prevent the control of the device characteristics. As diamond has a large bandgap the characterisation of defects present becomes more difficult or requires high temperature measurements. Defects in natural diamonds are usually caused by impurity inclusions. However, the many different growth methods of synthetic diamond entail that the defects present are more complicated, harder to characterise and often inherent to the growth process.

3.4.5.1 Grain Boundaries

Grain boundaries are inherent in synthetic polycrystalline diamond and while their size can be controlled by different parameters, such as the growth rate and species of the gas mixture, they are an unavoidable outcome. As a result considerable research has been performed in order to investigate their morphology and their effects on the diamond films. Several symmetrical and asymmetrical junctions have been observed to form at grain boundaries, quite often inducing stress on the diamond films and causing high dislocation densities to propagate through it [56]. Grain boundaries restrict the motion of carriers by limiting their mean free path and act as conducting paths for the

current flow due to the high concentration of defects that they contain. In polycrystalline diamond grain boundaries may contain sp^2-bonded carbons or may be combined with hydrogen or other impurity atoms. Molecular dynamics simulations have shown that the ground-state atomic structure of a typical high-energy grain boundary in diamond has a large fraction of sp^2 bonded atoms [57]. This structure gives rise to localised bands within the band gap eventually causing multiphonon assisted hopping conduction. As a result, field electron emission can be observed due to the morphology pits caused by the grain boundaries [58].

It has been shown that even very low levels of defects within the grains, associated with the aforementioned small concentrations of non-diamond carbon, are capable of strongly degrading the thermal conductivity of diamond below room temperature [59]. Films with smaller grains usually have higher concentration of defects since the latter tend to be concentrated at grain boundaries. Therefore it is difficult to distinguish between the effects of grain boundaries and other defects. Very interesting research has demonstrated how trapped charge at grain boundaries can dramatically alter the electric field profile within poly-CVD particle detectors, which is one of the main areas of application of diamond films [60]. Higher temperature operation or high electric fields that penetrate into the grains have been proposed to yield improved device performance. As grain boundary defects also affect the behaviour of optoelectronic devices, a thorough understanding of their properties and effects is crucial [61].

3.4.5.2 Other defects

B in diamond occupies the well characterised acceptor level at 0.37eV. However, research has confirmed that the activation energy of the B acceptor level changes with B concentration of the diamond films [5, 29, 39, 62-64]. In particular, as the B doping increases the final B concentration increases yielding a higher ionisation coefficient [29]. Moreover as the B concentration increases the activation energy of the acceptor level decreases, due to impurity band conduction while the effect of grain boundaries becomes weaker [64]. DLTS and optical-DLTS (ODLTS) have revealed the existence of more than just the B acceptor level in HPHT grown diamond. A distinct level at 1.25eV above the valence band is detected by ODLTS related to an optical transition of 0.9eV from the B acceptor level. The level at 1.25eV is attributed to the A-

aggregate, consisting of a pair of substitutional nitrogen atoms that has been detected by Raman and several other optical related studies [65].

Nitrogen is a commonly found element in natural diamonds and it plays a significant role in the defect formation in synthetic diamonds as it can be present in the CVD growth process. Its complex with a vacancy in diamond, forming the N–V centre, is of great interest as being a promising candidate for the formation of bits as required for quantum computers [15]. The N–V centre has been related to irradiation damage of diamond as shown by optical studies, although it has often been confused with the substitutional nitrogen atom.

Hydrogen also plays an important role in defect formation in diamond as it is present during most methods of diamond growth in the gas mixture. In addition it forms complexes with B (BH pairs) after deuteration when it is trapped by B acceptors [66, 67]. Therefore hydrogen diffusion is inhibited by the presence of B in diamond films and the electrically active B content hence appears reduced. However, this complex has been reported to dissociate at sufficiently high temperatures. The onset of the dissociation of B-H pairs in diamond occurs at 550 °C indicating a significantly higher thermal stability of these pairs in diamond compared to silicon. The estimated dissociation energy of the B-H pair has been reported to be 2eV.

3.5 Conclusion

This chapter initially presents the main properties of wide bandgap materials in order to emphasize their potential in modern semiconductor devices. In addition a detailed description is provided about the most important wide bandgap semiconductors that are currently under research, namely SiC, GaN and diamond. The properties of diamond are explained in detail as it is the material used for a part of this project. Its origin and classification as well as the methods of fabricating synthetic diamond are presented. Fabrication of contacts on diamond and doping techniques are subsequently discussed. Finally, defects in diamond films have been explained as well as grain boundaries that are present in polycrystalline diamond films and affect its electrical properties.

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Chapter 4: Background theory and measurement techniques

4.1 Introduction

The semiconducting diode is one of the most important electronic devices suitable for a very broad range of applications. Different types of diodes have been developed to match the requirements of a demanding and constantly increasing semiconductor market. However, the basic principles of diode operation are similar irrespective of the application and will be examined in this chapter in order to facilitate the understanding of the experimental results that will be examined later. The first section of this chapter will introduce the p-n diode that forms when two semiconductors of opposite conductivity come in contact. The Schottky diode will be examined subsequently in order to demonstrate the main notions behind a metal-semiconductor contact. Finally the experimental techniques that were used for diode characterisation, namely Current-Voltage (IV), Capacitance-Voltage (CV), Deep Level Transient Spectroscopy (DLTS) and High-resolution Laplace Deep Level Transient Spectroscopy (LDLTS) will be examined in order to complete the required theoretical background for interpretation of the measured diodes.

4.2 The p-n diode

When a p-type and an n-type semiconductor come in contact, there will be diffusion of electrons from the n-region towards the p-region as well as diffusion of holes from the p-region towards the n-region [1, 2]. This will result in a concentration gradient around the interface. In addition, the electrons that diffuse into the p-side can easily recombine with the existing holes there, and at the same time holes that have diffused into the n-side can recombine with some of the electrons that are in abundance in the n-region. Furthermore, as electrons diffuse into the p-side, they leave behind positively charged donor ions, and similarly while holes diffuse into the n-side, they leave behind ionised acceptors with a net negative charge. Because these ions on both sides of the junction are not mobile but are gathered near the junction on their respective sides, a layer of negative space charge has now developed on the p-side near the junction, while a layer of positive space charge has arisen on the n-side and near the

junction. Therefore this space charge region around the junction is depleted of mobile carriers and hence is called the depletion region. In the depletion region there is therefore a potential difference that causes an electric field which is directed from the positively charged donor ions toward the negatively charged acceptors. This field impedes further diffusion of majority carriers but assists the flow of minority carriers. So while holes are diffusing from the p-side to the n-side and leaving negative acceptors behind, the field is getting stronger and holes that are already near the depletion region on the n-side tend to drift with the field creating a drift hole-current directed from the n-side to the p-side. In the same way, while electrons diffuse from the n-side to the p-side, electrons that are near the p-side of the junction tend to drift back to the n-side under the influence of the electric field. In thermal equilibrium, there is a balance between the diffusing and drifting electrons and holes and hence there is no net current flowing across the junction. The electric field causes a potential difference that is reflected in the height difference of the conduction (E_C) and valence (E_V) bands of the n- and p-sides, and is called the built-in voltage (V_D). The Fermi level is now flat throughout and the conduction and valence bands have bent to accommodate the alignment of the Fermi level. The energy band diagram of the p-n junction in equilibrium is illustrated in Fig. 4.1.

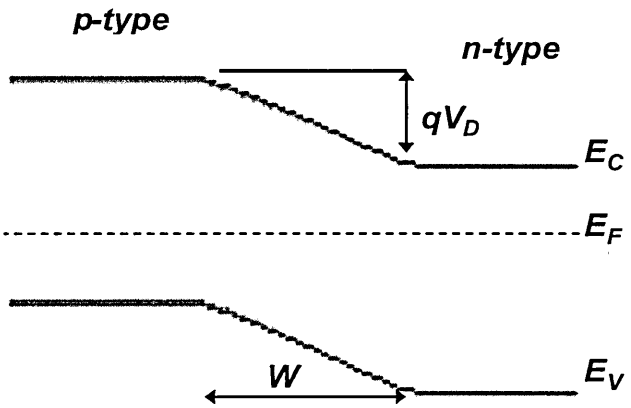

Fig. 4.1: Energy band diagram of a p-n junction in thermal equilibrium

When a voltage (V_F) is applied to a p-n junction, current flows across the junction. If positive voltage is applied to the p-side of the junction then the junction is forward biased. Since the p-side has an excess of holes, when positive bias is applied the holes are repelled toward the junction where they encounter the negatively charged acceptor ions and neutralise them. Likewise, electrons that are repelled from the n-region travel

toward the junction and neutralize some of the positively charged donors. Therefore the depletion region becomes narrower and the potential barrier lowers. Consequently (V_D) is now reduced. The applied voltage appears entirely across the depletion region since this region has higher resistance than the p- and n- regions. This is because it is depleted of mobile carriers and mainly populated by the charged ions. Therefore the potential barrier qV_D is lowered by V_F and the width of the depletion region is reduced. Since the barrier height is lowered, the majority carriers from either side can now more easily diffuse across the junction, while the minority carriers are practically unaffected. Therefore the diffusion current increases while the drift current of minority carriers is not affected. This is how a p-n diode begins to conduct current under forward bias. When the applied bias V_F reached the value of V_D the diode is said to have turned on. The effect of forward biasing on the energy band diagram of the diode is illustrated on Fig. 4.2:

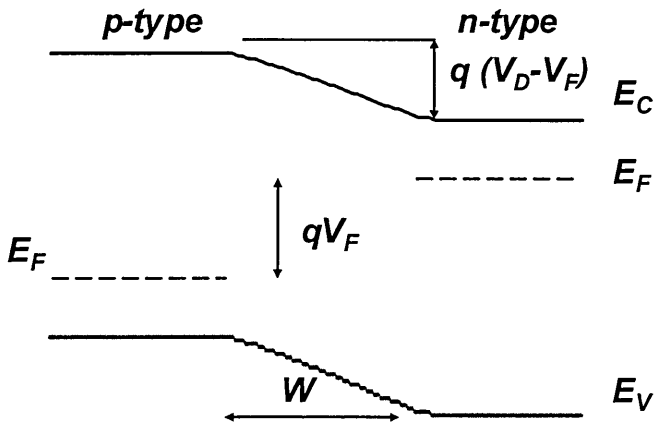

Fig. 4.2: Energy band diagram of a p-n junction under forward bias

When negative voltage (V_R) is applied to the p-side, the junction is reverse biased. In this case holes in the p-side are attracted towards the contact where the negative bias is applied and similarly electrons move in the opposite direction. Consequently the majority carriers on either side move further away from the junction leaving more ionised acceptors and donors behind. Hence the depletion region widens and the potential barrier height increases so it is more difficult more majority carriers to diffuse over to the other side. Therefore the majority carrier current is decreased while the minority carrier drift current is virtually unaffected. Only a very small number of minority carriers under these circumstances can reach the depletion region, and this is

why the reverse current, which is also called leakage current, is very small in an ideal diode. The energy diagram of the p-n junction under reverse bias is shown in Fig. 4.3.

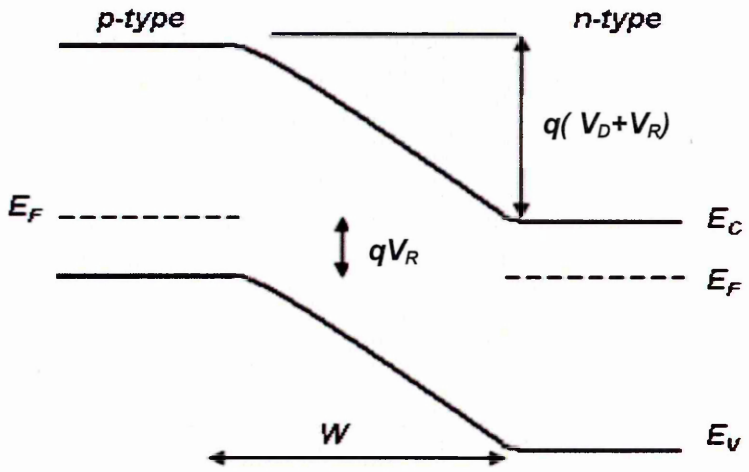

Fig. 4.3: Energy band diagram of a p-n junction under reverse bias

From the above, it is clear that the depletion region width of a p-n junction is dependent on the applied bias and also on the concentration of donors or acceptors that are ionized within the depletion region. This dependence is described by Eq. 4.1 [2].

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_s(N_D + N_A)(V_D - V_A)}{qN_DN_A}} \qquad \textit{Eq. 4.1}$$

where ε_0 is the permittivity of vacuum, ε_s is the relative permittivity of the semiconductor, N_D is the donor concentration, N_A is the acceptor concentration, V_D is the built-in voltage and V_A is the applied bias, which in the previous discussion was either V_F for forward bias or V_R for reverse bias. If one of the sides of the junction is a lot more highly doped than the other, then one of the ion concentrations is a lot larger than the other and the depletion region width is all on one side of the junction. For instance, if $N_A >> N_D$ then Eq. 4.1 simplifies as follows:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_s(V_D - V_A)}{qN_D}} \qquad \textit{Eq. 4.2}$$

This equation is very commonly used in modern asymmetrical junctions where one side of the junction is a lot more heavily doped than the other. The equation that gives the depletion region capacitance (C_j) is:

$$C_j = \frac{C_0}{\sqrt{1+\frac{V_A}{V_D}}} \qquad \textit{Eq. 4.3}$$

Where C_0 is the value of C_j for zero applied bias given by:

$$C_0 = A\sqrt{\frac{\varepsilon_s q(N_A N_D)}{2(N_A+N_D)V_D}} \qquad \textit{Eq. 4.4}$$

Substituting Eq. 4.1 and 4.4 in Eq. 4.3 yields:

$$C_j = \frac{\varepsilon_s A}{W} \qquad \textit{Eq. 4.5}$$

The last expression is the general expression for the capacitance of a parallel plate capacitor with cross-sectional area A. This indicates that the depletion region junction capacitance can also be described by a similar analogy if a small voltage is applied, although the depletion region junction capacitance varies in a non-linear manner with the voltage. From the above discussion it is obvious that if the capacitance of the depletion region in relation with the voltage is experimentally found, the width of the depletion region can subsequently be calculated. The p-n diode current (I) is given by Eq. 4.6 below for an applied voltage V_A.

$$I = I_s[exp(\frac{V_A}{V_T}) - 1] \qquad \textit{Eq. 4.6}$$

Eq. 4.6 relates the current and voltage in a diode. The physical quantities of Eq. 4.6 are defined as follows.

- V_T is the thermal voltage. V_T = kT/q
- k is the Boltzmann's constant = 1.38×10^{-23} joules/Kelvin
- T is the absolute temperature in Kelvin
- q is the magnitude of the electronic charge = 1.6×10^{-19} Coulomb
- I_s is the reverse saturation current and is given by:

$$I_S = qAn_i^2\left(\frac{D_p}{N_d L_p} + \frac{D_n}{N_a L_n}\right) \qquad \textit{Eq. 4.7}$$

where D_p and D_n are the hole and electron diffusion coefficients respectively, N_d and N_a are the donor and acceptor concentrations respectively, L_p and L_n are the hole and electron diffusion lengths respectively and n_i is the intrinsic carrier concentration of the semiconductor. A final important parameter useful for the calculation of the depletion region width or junction capacitance is the built-in voltage V_D, that arises from the alignment of the Fermi levels when the two semiconductors join to form a p-n diode, as previously mentioned. This is given by Eq. 4.8.

$$V_D = \frac{kT}{q} ln\left(\frac{N_D N_A}{n_i^2}\right) \qquad \textit{Eq. 4.8}$$

The above equation illustrates the dependence of the built-in voltage on the acceptor and donor concentrations on both sides of the junction near the interface. From Eq. 4.6 and 4.7 it can be seen that in the forward direction the current rises exponentially with bias while in the reverse direction it saturates to a value I_s. Fig. 4.4 below shows the ideal diode current-voltage characteristic that follows Eq. 4.6 and demonstrates the forward and reverse regions of operation of the diode.

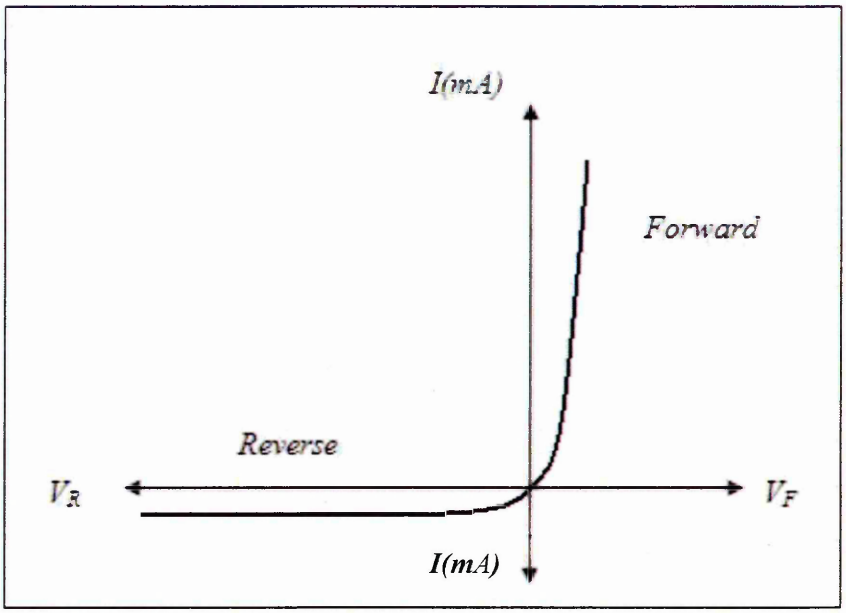

Fig. 4.4: Ideal current-voltage characteristic of a p-n diode.

4.3 Schottky barrier diode

The term Schottky barrier refers to a metal-semiconductor interface with rectifying properties. When a metal and a semiconductor come in contact in thermal equilibrium their Fermi levels have to align which results in energy band bending of the semiconductor side. Certain notions should be established initially for the understanding of this configuration. The work function $q\varphi$ is the energy required to bring an electron from the Fermi level to the vacuum level. Hence for a semiconductor the work function would be $q\varphi_s$ and for a metal the work function is $q\varphi_m$. The difference φ_m - φ_s is called the built-in voltage (V_i) of the Schottky barrier and $q\varphi_B$ is the barrier height from the metal toward the semiconductor. The electron affinity of the semiconductor $q\chi$ is the energy difference between the conduction band edge E_C and the vacuum level. To illustrate these notions Fig. 4.5a below shows the band diagrams of a metal and semiconductor before they come in contact while Fig. 4.5b shows the arrangement of the bands after the metal and semiconductor are in contact and thermal equilibrium has been established.

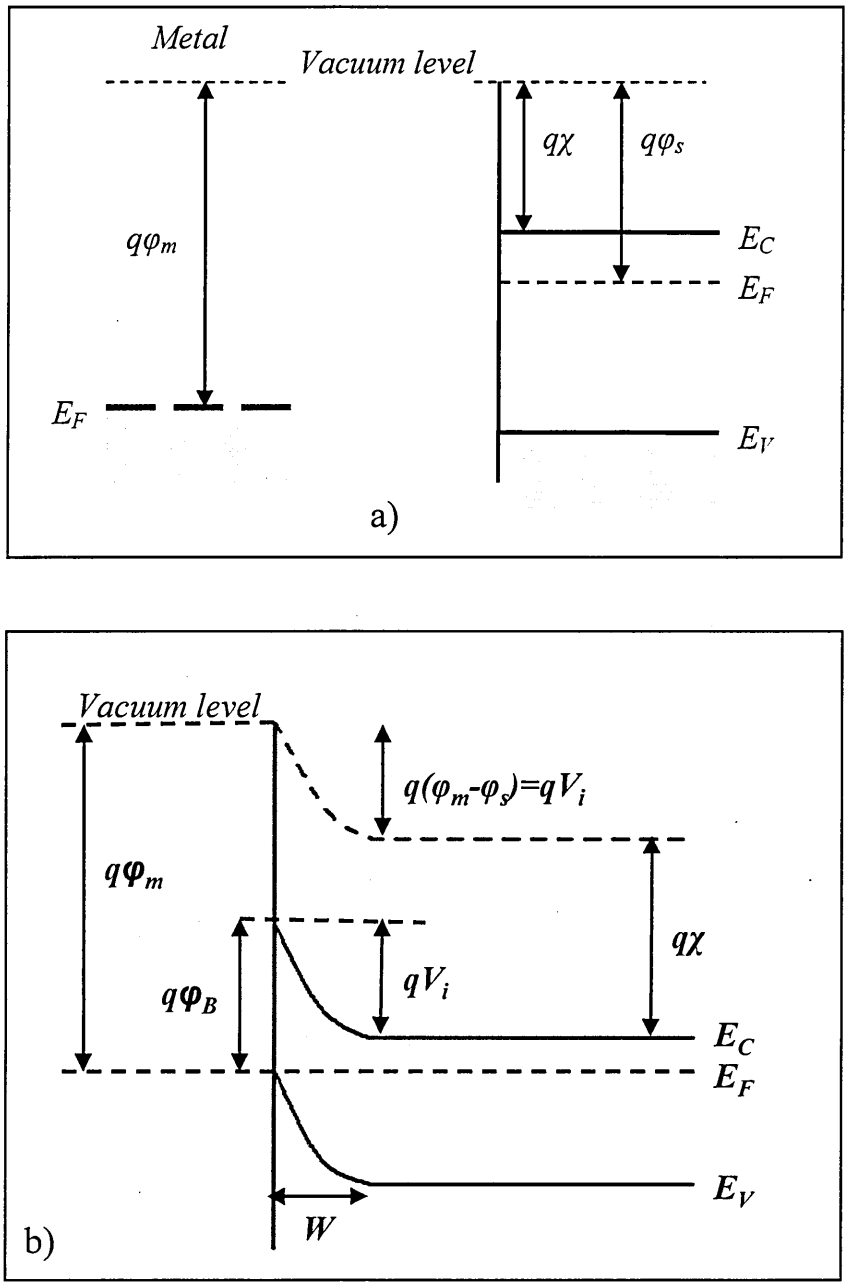

Fig. 4.5: The energy band diagram of: a) A metal and a n-type semiconductor before contact, b) after contact and in thermal equilibrium

The above diagram is valid for an n-type uniformly doped semiconductor. Here it is assumed that the metal work function is greater than the semiconductor work function. When the metal and semiconductor are brought into contact as shown in Fig. 4.5b, electrons from the conduction band of the semiconductor flow into the metal in order to cause alignment of the Fermi level. The conduction and valence band bending are due to this effort for alignment of the Fermi level. In addition the vacuum level of the semiconductor seems to approach the vacuum level of the metal and has the same bending as the conduction and valence bands. If this was a p-type semiconductor the

band bending would be downwards instead of upwards but the same rules and analysis apply to both situations. When electrons flow into the metal they leave positively charged donors behind which extend into the semiconductor up to a width W as shown in Fig. 4.5b, while the negative charge of the electrons that has diffused inside has settled very close to the interface. There is an electric field that arises between the electrons and the positive donors that are left in the semiconductor near the surface. The difference between the metal and semiconductor work functions is in fact equal to the band bending. Therefore: $\varphi_m - \varphi_s = V_i$, the built-in voltage. Also from Fig. 4.5b it can be seen that: $q\varphi_s = q\chi + (E_C - E_F)$ and consequently the effective barrier height $q\varphi_B$ is:

$$q\varphi_B = q\,V_i + (E_C - E_F) \qquad \textit{Eq. 4.9}$$

The above expression is the Schottky approximation and gives information about the energy barrier that carriers have to surpass in order to establish conduction between the semiconductor and the metal. In thermal equilibrium only a small fraction of conduction band electrons have enough energy to overcome the potential barrier and flow into the metal causing a current directed from the metal toward the semiconductor I_m. An equal and opposite current I_s directed from the semiconductor to the metal arises due to electrons that flow into the semiconductor from the metal.

However, when the semiconductor is biased negatively with respect to the metal by a voltage V_F, the barrier $q\,V_i$ for electrons is lowered by $qV_i - qV_F$. A greater amount of electrons are being pushed toward the barrier which they can now surmount since it has become lower. Therefore the current I_m is now different than its equilibrium value and greater than I_s, which remains unaffected and the Schottky junction is forward biased. Furthermore with the application of bias the metal and semiconductor Fermi levels are no longer aligned. The opposite happens when the semiconductor is biased positively with respect to the metal by a voltage V_R. Under this reverse bias condition, electrons are pulled away from the metal-semiconductor interface and the potential barrier is now increased so it is more difficult for electrons to cross it and flow into the metal. I_m is now reduced in comparison to I_s which remains unaffected and a net current flows from the semiconductor to the metal. This is called the reverse current. The effect of voltage application on the Schottky barrier is shown in Fig. 4.6 below, for an n-type semiconductor.

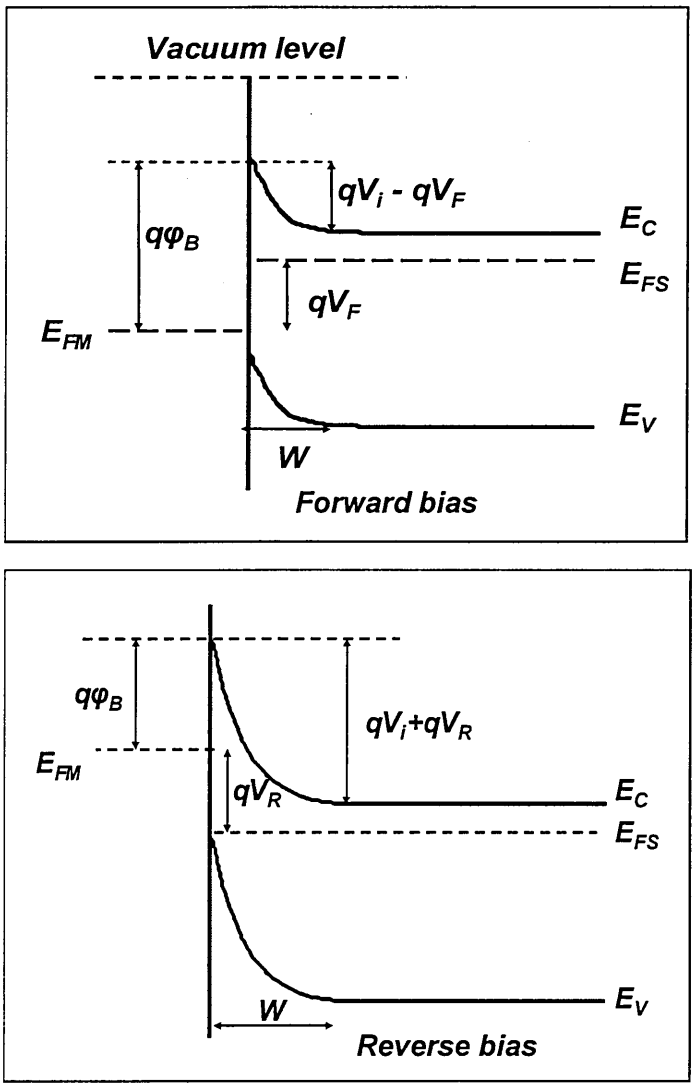

Fig. 4.6: Schottky barrier under forward (top) and reverse bias (bottom)

From the above discussion it can be seen that this is a rectifying contact. In general when the metal work function is greater than the semiconductor work function the Schottky barrier is a rectifying contact for a n-type semiconductor. If the opposite is true, then the contact is non-rectifying and it is called an Ohmic contact. For a p-type semiconductor, the Schottky barrier is a rectifying contact when the semiconductor work function is greater than the metal work function. An important phenomenon that influences the performance of a Schottky diode is the Fermi level pinning. It has been observed that in certain semiconductors such as Si and Ge the barrier height $q\varphi_B$ is independent of the metal work function $q\varphi_m$. According to what is known as the Bardeen approach on this phenomenon, in covalently bonded semiconductors such as Si and Ge the atoms on the surface do not have neighbouring atoms on the vacuum side with which to form bonds, so every surface atom has one dangling bond. Dangling

bonds are responsible for the formation of surface states, which are distributed within the forbidden energy bandgap. These states pin the Fermi level at the surface and influence the barrier height. P-n junctions do not suffer from this phenomenon as the actual junction is "buried".

As mentioned earlier in the p-n junction diode section, Eq. 4.2 represents the width of the depletion region when the doping concentration of one of the sides of the junction is much higher than the other. Hence the depletion region width is then only dependent on the concentration of the lowest doped side and hence the depletion region appears almost entirely on the side of the junction with the least concentration. In Schottky diodes, the metal does not have a bandgap and cannot support an electric field since it is not a semiconductor thus the depletion region appears entirely into the semiconductor. The same equation applies in Schottky diodes for the evaluation of the depletion region width, which is mainly only dependent on the doping concentration of the semiconductor and the applied bias. Hence, by applying bias to a Schottky diode and profiling only through the semiconductor depletion region we can determine the width of the depletion region. In the same manner, Eq. 4.3-4.5 are also applicable facilitating the evaluation of the depletion region capacitance. So from a capacitance-voltage (*C-V*) characteristic of a Schottky diode, the depletion region width and the doping concentration can easily be determined. Combining Eq. 4.2 and 4.5 we have for an applied bias V_A:

$$\frac{1}{C^2} = \frac{2(V_i - V_A)}{A^2 q \varepsilon_0 \varepsilon_s N_D} \qquad \textit{Eq. 4.10}$$

The above relation implies that when the semiconductor is uniformly doped, a plot of $1/C^2$ versus V_A gives a straight line from which it is possible to obtain the doping concentration. However when N_D varies with distance like in a non-uniformly doped semiconductor the plot of $1/C^2$ versus V_A does not give a straight line. However, from the slope of the characteristic at any given point into the depletion region and from the width W which is obtained from Eq. 4.5 for any applied bias, it is still possible to determine the doping concentration. The current-voltage (*I-V*) characteristic of a Schottky diode is given by a similar relation to that of a p-n diode.

$$I = I_S[exp(\frac{V_A}{\eta V_T}) - 1] \qquad Eq.\ 4.11$$

Where I_S is again the saturation current which is given by Eq. 4.12.

$$I_S = AA^*T^2\, exp\left(\frac{-q\phi_B}{kT}\right) \qquad Eq.\ 4.12$$

where, A is the area of the diode, A^* is the effective Richardson's constant given by $A^* = 4\pi q m_e k^2/h^3$ with m_e being the electron effective mass, h is Planck's constant and η is the ideality factor which has the value of 1 for ideal Schottky diodes. The ideality factor may be higher than 1 depending on the barrier height, the tunnelling of carriers through the barrier, or e-h pair recombination in the depletion region. In addition it depends on temperature and the reverse bias and hence often deviates from unity. Its maximum value is 2.2. The diode current can be limited by certain factors such as emission processes and tunnelling. The latter will be described in the following section.

The above discussion about p-n and Schottky diodes demonstrates the way that the basic electrical measurements CV and IV are performed. The combination of Eq. 4.2-4.5 can be implemented to determine the junction capacitance of the diode as the latter is directly related to the applied bias. In addition, the depletion region width can be found from the same set of equations and the slope of Eq. 4.10 will yield the carrier concentration. Finally Eq. 4.6 and 4.11 can be used in IV measurements of p-n and Schottky diodes respectively.

In degenerate semiconductors, the depletion region is very narrow and electrons can often tunnel into the metal through the barrier. When electrons near the Fermi level tunnel into the metal, the process is called field emission, while when they tunnel at the top where the barrier is thinner the process is called thermionic field emission. If electrons are emitted into the metal over the barrier the phenomenon is called thermionic emission. Thermionic emission of electrons over the barrier is determined by the density of available states into the metal and is controlled by the drift and diffusion processes.

4.4 Tunnelling in diodes

Tunnelling was initially associated with junction breakdown in p-n diodes [1, 2]. When a reverse bias is applied to a heavily doped p-n junction, the depletion region becomes very narrow and a high electric field exists in it. There are no free carriers in the depletion region since all electrons are in the valence band. Because the depletion region is so narrow, the free electrons in the valence band have no particular difficulty in crossing the junction and are then promoted into the conduction band. The process is also aided by the reverse bias electric field but if the junction is narrow enough it can even occur without it. However, the electrons do not get promoted to the conduction band of the side of the junction they are originally in, but cross over to the conduction band of the other side of the junction. This results in leakage current, which is more pronounced the higher the electric field is. The diode tunnelling process described above is shown in Fig. 4.7 [1].

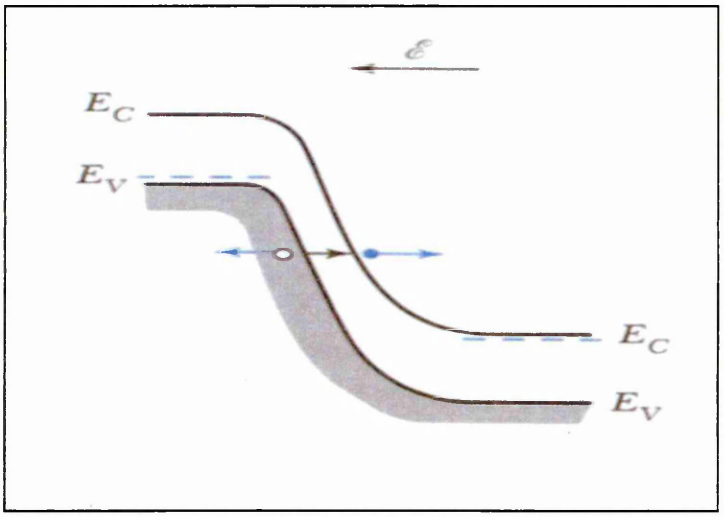

Fig. 4.7: Tunnelling process in diodes [1]

4.5 Deep Level Transient Spectroscopy

Different techniques using capacitance measurements have widely been used for the study of semiconductors and in particular for the investigation of defects in their bandgap [3-6]. These include Thermally Stimulated Capacitance (TSCAP) and Photocapacitance which either exhibited low sensitivity or were only suitable for the characterisation of deep levels or the extraction of optical parameters and thus did not have broad application. Luminescence has good sensitivity and speed although it is mostly intended for determining the properties and chemical identities of shallow impurities and therefore can only be used indirectly to study non-radiative processes.

Other techniques such as Thermally Stimulated Current (TSC) and Admittance Spectroscopy were widely used although the latter is not suitable for characterizing minority carrier traps. Deep level transient spectroscopy (DLTS), introduced in 1974, offered improvements in many aspects of defect characterisation and quickly replaced many of the aforementioned techniques [6]. It exhibits higher sensitivity and is easier to use while results are produced fast and facilitate analysis. Moreover it can be implemented for the study of a very broad range of defects lying at various depths within the semiconductor. DLTS is a capacitance transient thermal scanning technique which takes advantage of reverse-biased p-n junction structures in order to observe and characterise defects in a region depleted of mobile carriers [7, 8].

4.5.1 DLTS description and setup

In DLTS, an initial non-equilibrium charge state is prepared for a p-n junction or a Schottky barrier, and the capacitance transient associated with the return to this initial state of the occupation of the deep level is recorded. The junction is initially kept under reverse bias in order to create space charge conditions. As the depletion region does not contain any free carriers, trap levels are originally empty. A momentary forward pulse will collapse the space charge region, making majority carriers available for capture. When the application of the pulse is terminated and the reverse bias is restored, the junction capacitance has been reduced as majority carriers have been trapped in the space charge region. Subsequent applied bias will cause the re-emission of the trapped carriers into their respective carrier bands, once again producing a change in the measured junction capacitance. The capacitance transients, which have an exponential time dependence, occur due to the thermal emission of these trapped carriers, when the junction bias is returned to the steady state value after the short filling pulse. The change from the steady state caused by the applied bias is responsible for filling the traps with carriers and changing the level of occupation of the traps, which in turn promotes emission that is detected through the capacitance change. This capacitance change can be either positive or negative depending on whether the initial carrier population of the trap has been increased or decreased. Hence an increase in trapped minority carriers is known to produce an increase in the junction capacitance [6]. Fig. 4.8 shows the change in capacitance and the sign of the transient during the filling and emptying process of a minority carrier trap and a majority carrier trap respectively.

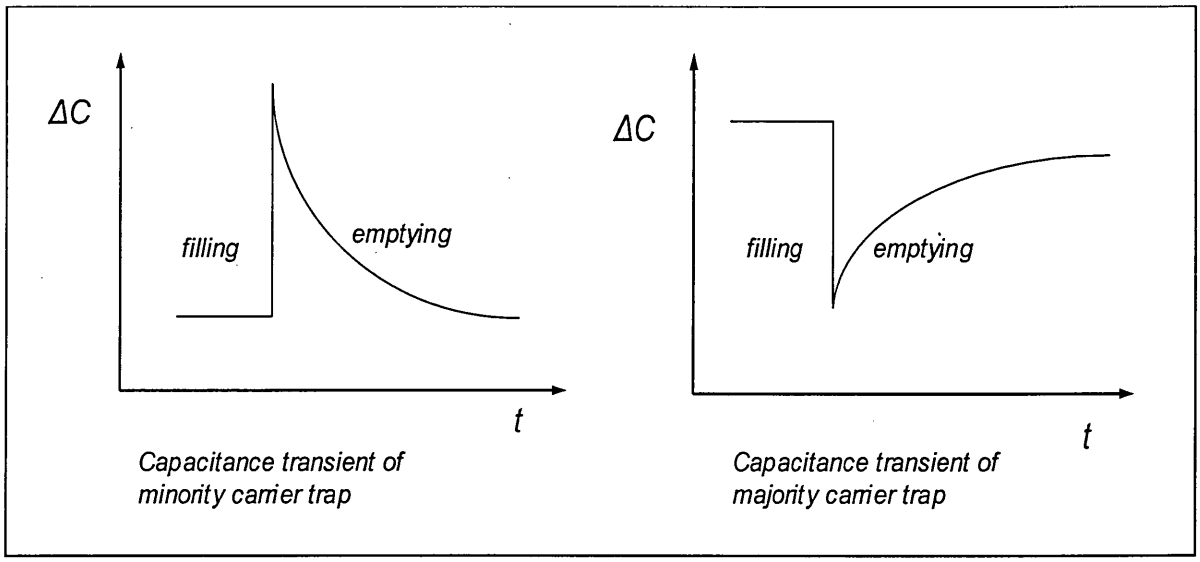

Fig. 4.8: Capacitance transient due to a minority or majority carrier trap

DLTS is a high frequency junction capacitance technique, where an emission rate window can be set causing the measurement apparatus to respond only when there is a transient with a rate within this window. The deep level traps are forced to emit at higher emission rates when more energy is provided to the system and this is achieved at higher temperatures. Similarly at lower temperatures the system will have less energy and the traps are only able to emit at lower rates. Thus, while the temperature is varied, the emission rate of the trap is accordingly changing and the measurement apparatus will detect a response peak at the temperature where the trap's emission rate is within this set rate window. This quality makes DLTS a powerful spectroscopic tool that can measure the activation energy, concentration and capture cross section of carrier traps in a semiconductor.

A trap is considered as majority carrier trap if it is full of minority carriers and thus can capture majority carriers, while a minority carrier trap, is empty of minority carriers. Two types of fill pulses are generally used in order to introduce carriers in the depletion region and fill the traps. A majority-carrier pulse is used to introduce majority carriers into the depletion region by reducing the diode bias from the initial reverse bias condition. This situation is illustrated in Fig. 4.9 as an example for the depletion region of an n^+p diode where the majority carriers are holes.

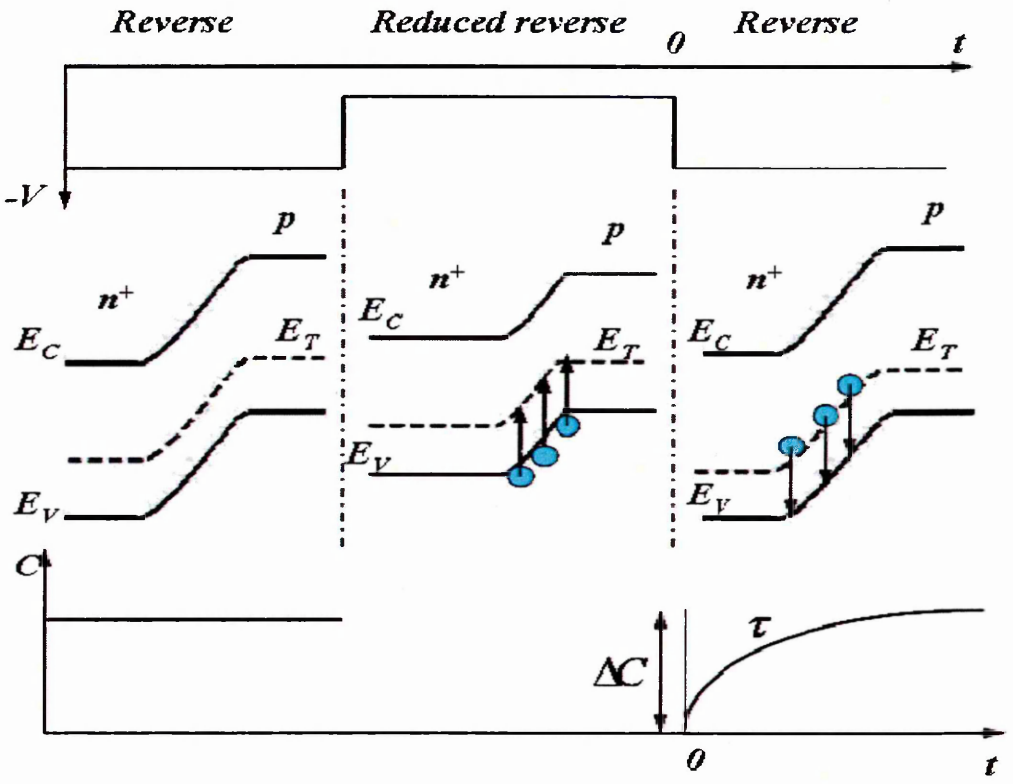

Fig. 4.9: Filling of a majority carrier trap by a majority carrier pulse in an n^+p diode

The depletion region in the asymmetric n^+p diode configuration of Fig. 4.9 lies on the p-side of the junction as this contains lower doping. The junction is kept under reverse bias initially and the hole trap level above the valence band is empty of holes. With the application of the fill pulse which reduces the reverse bias, holes are being introduced into the depletion region and captured by the trap, thus the junction capacitance momentarily reduces. This can be verified from the combination of Eq. 4.2 and 4.5 since the capturing of the holes by the trap, will decrease the carrier concentration and as a result the capacitance will also reduce. As the pulse is removed, the holes will gradually be emitted back into the valence band. However, this process will take place slowly resulting in a capacitance transient with time constant (τ), which in fact represents the emission rate (e) of the trap, as seen from the above diagram [6]. The valence and conduction bands are denoted by E_V and E_C respectively in the above figure, E_T is the trap level and ΔC is the difference of the junction capacitance caused by the application of the fill pulse.

For the case of a minority carrier trap, an injection pulse is used to apply forward bias and to inject minority carriers into the depletion region. This can be seen from Fig. 4.10 below.

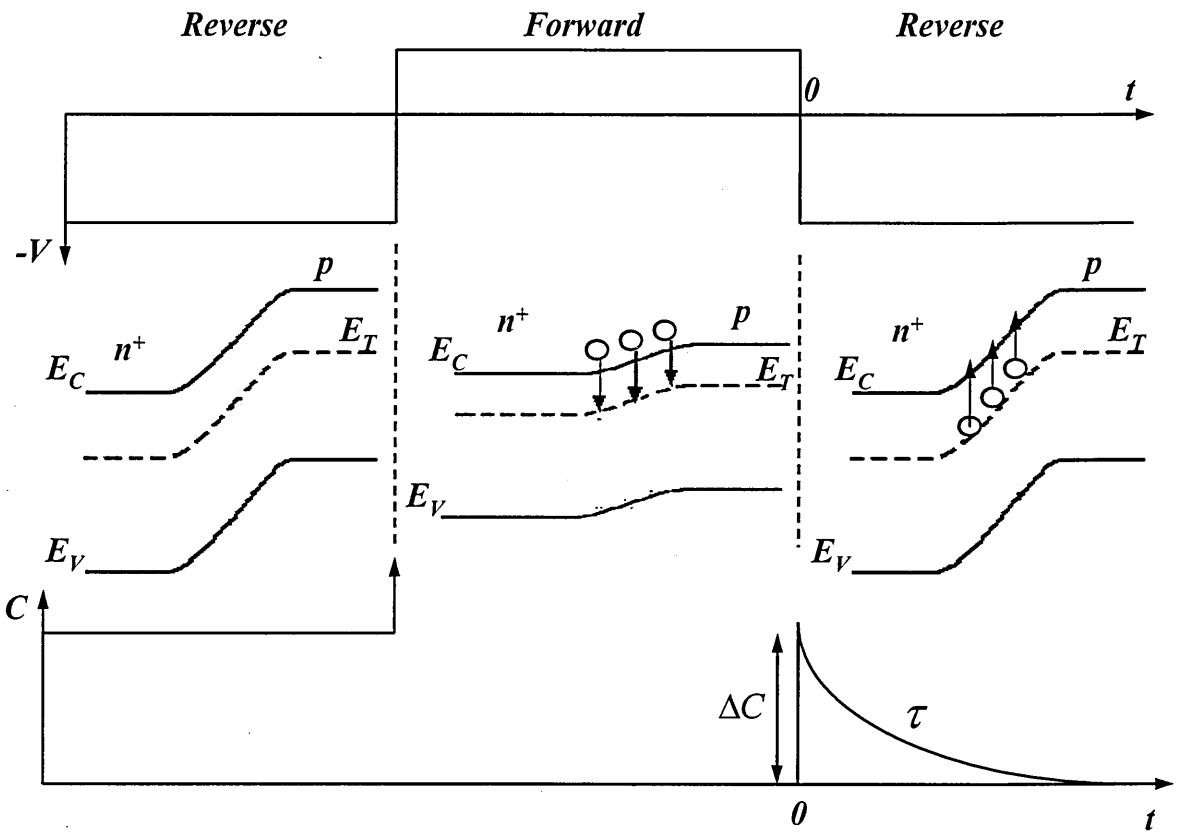

Fig. 4.10: Filling of a minority carrier trap by a minority carrier pulse in an n^+p diode

An injection pulse introduces both minority and majority carriers since the depletion region is forward biased and the junction barrier may have collapsed [7]. Depending on the capture rates or cross section of the respective traps, a minority transient may be observed.

The DLTS set-up consists of a sensitive capacitance meter with good transient response, one or two pulse generators, a dual gated signal integrator, a variable temperature cryostat and a temperature controller. The system's response and results are recorded on a computer where the input parameters can be adjusted and the data is stored. A positive or negative peak plotted against temperature indicates the existence of a trap, while the size of the peak is proportional to the concentration of the deep centre and the sign of each peak denotes whether it is due to majority or minority carrier traps. It is very important to implement a high stability cryostat and establish accurate communication with the temperature controller as any change in temperature before the end of the fill pulse will affect the occupation of the trap levels. In addition, the use of the dual gate signal integrator is required to be very accurate as it is responsible for the determination of the DLTS rate window and the signal averaging that provides noise reduction. Fig.

4.11 shows the use of the double boxcar (double gated signal integrator) implemented in DLTS for the setting of the rate window and the extraction of the capacitance difference from the transient. Details of the equipment specifications used in this project will be presented in the following chapter.

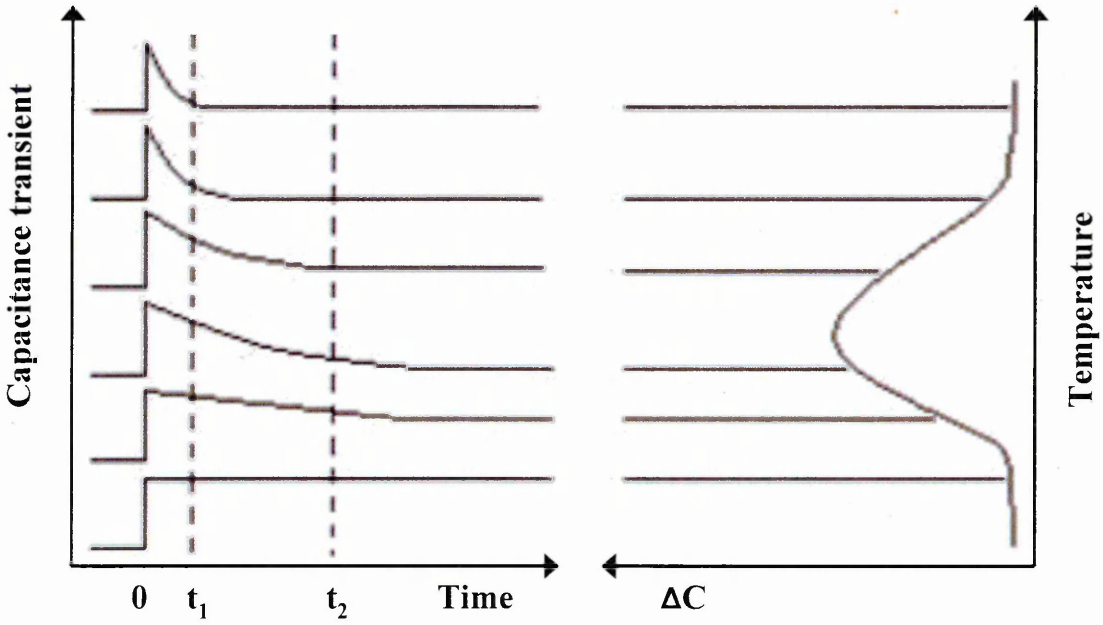

Fig. 4.11: DLTS signal resulting from capacitance transients at different temperatures with the use of a double boxcar. The difference in capacitance at times t_1 and t_2, is displayed on the DLTS spectrum

The times t_1 and t_2 denote the rate window set by the double boxcar in Fig. 4.11. The capacitance difference from each transient at a different temperature is plotted on the DLTS spectrum. This difference is in fact the change in capacitance $C(t_1) - C(t_2)$ and this will be maximum when the emission rate matches the system's time constant. The capacitance difference over the capacitance change due to a pulse applied at $t=0$ by the signal $S(t)$ is given by:

$$S(t) = \frac{C(t_1) - C(t_2)}{\Delta C(0)} \qquad \text{Eq. 4.13}$$

The same signal causes the exponential capacitance transient that is sampled at the two time instants t_1 and t_2 as shown by Eq. 4.14.

$$S(t) = e^{\frac{-t_1}{\tau}} - e^{\frac{-t_2}{\tau}} \qquad \textit{Eq. 4.14}$$

From Eq. 4.14 the maximum of the inverse transient rate constant τ_{max} which is in fact the set rate window for the scan that will detect an emission rate e from a trap, can be acquired:

$$\tau_{max} = (t_1 - t_2)[\ln(\frac{t_1}{t_2})]^{-1} = e^{-1} \qquad \textit{Eq. 4.15}$$

It is important to notice that in Eq. 4.15, just by varying t_1 and t_2 different rate windows can be used for each scan. The most suitable way to achieve this is to vary t_1 and t_2 while keeping their ratio t_1 / t_2 constant. In this way the logarithmic part of Eq. 4.15 will be a constant and the shape and size of the peaks on the $C(t_1) - C(t_2)$ versus T plot will not be affected. In this manner the only effect on the peaks obtained when t_1 and t_2 have changed but their ratio is kept constant, is a slight shift on the temperature scale. As mentioned earlier for the traps to emit at higher emission rate more energy in the system is required, and this is obtained at higher temperatures. This is reflected by a shift to the right on the temperature scale at higher rate windows where the traps can acquire more energy to emit carriers at higher rates. This is a very important conclusion as by setting different rate windows it is possible to record and monitor the emission rate of a trap with respect to temperature alone, which subsequently allows calculation of the activation energy of a trap.

4.5.2 Trap parameters

If a carrier trap is completely filled due to a saturating injection pulse or a large majority carrier pulse, the concentration of the trap can be easily calculated from the total capacitance change which is given by Eq. 4.16.

$$N_T = 2\frac{\Delta C}{C}(N_A - N_D) \quad \text{for a } n^+p \text{ diode or p-type Schottky barrier device}$$

$$N_T = 2\frac{\Delta C}{C}(N_D - N_A) \quad \text{for a } p^+n \text{ diode or n-type Schottky barrier device.} \qquad \textit{Eq. 4.16}$$

where N_T is the trap concentration, N_A-N_D and N_D-N_A are the net ionized impurity concentrations, ΔC is the change in capacitance produced from the change in the trap occupation and C is the quiescent capacitance of the diode under reverse-bias conditions. As was pointed out earlier, when one side of a p-n diode is a lot more highly doped than the other, the depletion region appears almost entirely on the low-doped side and the same analogy holds for Schottky diodes where the depletion region lies entirely in the semiconductor. Therefore in Eq. 4.16 either the donor or acceptor concentrations are necessary for the calculation of the trap population as the low doped side can either be a p-type or n-type semiconductor.

The emission rate of a trap (e) is proportional to a Boltzmann factor and hence changes exponentially and rapidly with temperature and is given by Eq. 4.17 as follows:

$$e = \frac{N_C V_{th} \sigma}{g} exp(-\frac{\Delta E}{kT}) \qquad \textit{Eq. 4.17}$$

where, σ is the capture cross section, V_{th} is the mean thermal velocity, N_C is the effective density of states, g is a degeneracy factor, k is Boltzmann' s constant, T is the temperature value and ΔE is the energy difference between the trap level and the respective energy band (conduction band or valence band). To find the activation energy (ΔE) of a trap a semi-logarithmic plot of e/T^2 versus $1/T$ can be prepared, which ideally results in a straight line. The slope of this plot will yield the activation energy. Hence all experimental methods are designed to provide the *(e, T)* pairs necessary to achieve such a plot. By repeating the thermal scan with different known rate windows several *(e, T)* pairs can be obtained that give a more accurate evaluation of the activation energy.

DLTS also allows the extraction of information about the carrier capture cross section which defines the capability of the trap to capture free charge carriers. Capture cross section measurements are achieved by varying the fill pulse length. Application of a long fill pulse entails that the trap will be saturated by carriers while a short fill pulse means that the trap will not have time to fill completely. By measuring the occupancy of the trap while varying the fill pulse length by known time intervals the capture cross

section (σ) can be determined. Eq. 4.18 describes the carrier capture cross section (σ_n) of an electron trap.

$$\frac{\Delta C_\infty - \Delta C(t)}{\Delta C\infty} = exp(-\sigma_n V_{th} n)t \qquad Eq.\ 4.18$$

where $\Delta C\infty$ is the capacitance when the trap is completely filled, $\Delta C(t)$ is the capacitance at time t, n is the electron concentration and V_{th} is the thermal velocity at the temperature of the peak of the DLTS spectrum. The thermal velocity is given by:

$$V_{th} = \sqrt{\frac{3kT}{m^*}} \qquad Eq.\ 4.19$$

where m^* is the effective mass (of an electron in this case). The thermal velocity has the value of ~10^7cm/s at room temperature. For the capture cross section measurements, consecutive DLTS scans are performed around the peak temperature of the trap maximum by reducing the fill pulse length t. When a point is reached where the trap fails to fill the DLTS peak maximum will appear reduced. A graphical representation of $\ln[(\Delta C\infty - \Delta C(t))/\Delta C\infty]$ versus time should yield a straight line for a point defect, the slope of which is equal to $(\sigma_n V_{th} n)^{-1}$. From this slope the electron capture cross section can be determined. As was seen in a previous chapter, carrier capture from an extended defect obeys a time-dependent relationship, which usually yields a non-linear slope when Eq. 4.18 is used. This is due to the Coulomb potential that arises around the defect that prevents further carrier capture after a period of time. Therefore the capture from such defects cannot be described by the aforementioned relationships but DLTS can still be used to identify such defects. The basis on which the simplicity of the acquisition of the measurements lies in DLTS is the assumption of exponential capacitance transients obtained from the traps. However, non-exponential transients are also known to arise in samples with multiple, closely spaced deep levels with comparable emission rates. In this case determination of the trap parameters cannot be done using the previous equations, although techniques have been developed for analysing such transients [9, 10].

Variations of DLTS, such as charge-DLTS (QDLTS), isothermal capacitance DLTS and current-DLTS, have also been developed for the study of deep levels in semiconductors [11]. The disadvantage of some of these techniques is that they only allow investigation of one type of carrier traps (majority or minority) at a time. In addition some research has been focused on the improvement of the DLTS method by using more advanced measurement equipment such as modified capacitance meters or A/D converter cards to digitize the capacitance transients, thus minimizing the data collection or analysis time [12, 13]. Finally DLTS has been very useful for the study of alloys or plastically deformed semiconductors, although the difficulty of separating closely spaced traps has lead to a high resolution technique as will be seen in the following section [14, 15].

4.6 Laplace Deep Level Transient Spectroscopy

Although DLTS is a very important technique with great sensitivity, it is known to have an insufficient time constant resolution for the separation of multiple, closely spaced, decaying exponential components. The calculation of activation energies from DLTS has an error margin of $\pm$ 50meV. In addition, in many cases of closely spaced traps featureless or very broad characteristics are obtained that cannot be separated by application of different biasing conditions. Therefore certain deconvolution methods have been implemented to achieve the separation of such traps, while using different analogue or digital approaches. Laplace DLTS (*LDLTS*) is the most recent and successfully applied high resolution spectroscopic technique.

LDLTS works by digitizing the capacitance output and averaging many transients to reduce the noise level. Several thousand capacitance transients are averaged in this way, in an effort to yield a signal to noise ratio (S/N) above 1000. The capacitance transients resulting from trap emissions are digitized with the aid of digital signal processing and are recorded at a fixed temperature. Each sample from the capacitance transient is stored and processed by an A/D converter and therefore a high range of memory is necessary. Moreover, LDLTS is an isothermal technique where the selected temperature stems from the peak produced by the DLTS measurement [15].

Subsequently a range of algorithms implementing an inverse Laplace Transform is used to obtain the emission rates present in the transient. The choice of algorithms, have to satisfy criteria such as, being able to produce accurate amplitude and emission rate

analysis, as well as to be able to process both decaying and increasing transients perhaps even at the same time. Three different algorithms are used which are based on the Tikhonov regularization method, differing only in the way the regularization parameters are defined. The algorithms are CONTIN, FTIKREG and FLOG and were either obtained from a software library and modified for the requirements of LDLTS or were developed specifically for the LDLTS system [16-18]. Therefore a complete and comparative study of emission rate is provided which increases the accuracy of the outcome in the LDLTS spectra. Finally a sharp peak is produced for an exponential transient indicating the amplitude of the peak at a well defined emission rate hence making the trap emission rate easily available.

A high stability cryostat is one of the main requirements for LDLTS as any change in temperature during the measurement can cause differences in the emission rates of a trap. For instance, for the determination of emission from a 100meV level, a stability of $\pm$ 50mK is required [19]. Larger temperature shifts will introduce noise which can be detrimental for the accuracy from such a shallow level.

A very accurate calculation of the emission rate of a trap level will also enable a more precise calculation of its activation energy. Thus very closely spaced traps that were previously undetermined, such as the gold acceptor and the G4 gold-hydrogen complex in Si, dangling bond levels and the vacancy-oxygen level were successfully resolved [19, 20]. As a technique with very high potential LDLTS has found many other applications [21-23].

4.7 Conclusion

This chapter presented the necessary theoretical background associated with the physics of diode operation. Both p-n and Schottky diodes were initially examined and capacitance-voltage and current-voltage measurements of these diodes were considered. In addition, Deep Level Transient Spectroscopy, one of the most important techniques for deep level characterisation was presented. The technique was described together with the necessary equations for the extraction of significant parameters, concerning deep levels in semiconductors. Finally the improved technique of Laplace DLTS was introduced, which significantly improves emission rate determination and enhances the characterisation prospects of the thermal capacitance scanning technique.

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Chapter 5: Fabrication and experimental set-up

5.1 Introduction

Two very different sets of samples were examined in this project using the techniques detailed in the previous chapter. The first part was associated with the electrical characterisation of Ultra-Shallow Junctions (*USJs*) in Si. Such structures are necessary, as explained in chapter 2, so as to allow reduction of the junction depth in an effort to avoid short channel effects in MOSFETs. As a result, very narrow junctions are formed within very highly doped materials. The devices under investigation in this part of the project are therefore p^+n and n^+p USJ diodes in Si. This chapter provides the specifications for these diodes and describes their fabrication. Secondary Ion Mass Spectrometry (SIMS) profiles for these diodes will be shown to provide information about the doping and comparison with the experimental electrical analysis. The second part of this chapter is related to the diode fabrication and background information of thin diamond films on Si substrates. Details of the HFCVD grown diamond films are provided and the formation of the diode structure is illustrated. Finally the equipment and experimental set-up used for the characterisation of all these diodes is described.

5.2 Specifications of USJ diodes

The p^+n and n^+p USJ diodes were provided by NXP, Leuven, Belgium. The substrates were n-type and p-type Si respectively, of high industrial quality. For the formation of the p^+n structures, high dose and low energy B implantation was performed for the p^+-side and lower dose, but higher energy implants of P and As for the also highly doped n-side to simulate a n-well. The n^+p samples underwent a high dose, low energy As implantation for the highly doped n^+-side and lower dose and higher energy B implants for the formation of the p-side to simulate a p-well. The p^+n structures were formed on n-type Czochralski (CZ) silicon substrates with a resistivity of 16-24 Ω-cm and the n^+p structures on p-type CZ silicon substrates with a resistivity of 15 Ω-cm to avoid formation of two junctions. However, it should be mentioned here that the n-side doping of the p^+n structures is much higher than that of the n-substrate and similarly the p-side doping of the n^+p structures is higher than that of the p-substrate, as the formation of a doping well was desired. All implantation was

performed by NXP. Five p^+n samples were prepared that contained different combinations of dose and implantation energy and P or As and P implants for the formation of the n-side. One of these samples only had a high B doping for the formation of the p^+-side, while the n-side was kept undoped for reference purposes and to allow investigation of the substrate. Similarly three n^+p samples were provided that had different B dose and energy implants, one of which was kept as a reference sample by having solely a high As implant. This arrangement allowed the investigation of USJs with different doping levels. The exact implantation and annealing details of these samples are shown in Table 5.1 as provided by NXP. All implants were performed through a 5nm thin screen oxide.

				Samples							
	Dose $*10^{13}$ (cm^{-2})	**Energy (keV)**	**Dopant**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**
Implant n^+	600	10	As						X	X	X
Damage anneal (5min)	1100°C								X	X	X
Implant p	9.3	100	B						X		
	4.3	100	B							X	
	1.2	180	B						X	X	
Implant p^+	500	10	B	X	X	X					
	500	5	B				X	X			
Implant n	9.3	250	As					X			
	2	250	As				X				
	20	230	P			X					
	4.3	230	P		X						
	0.2	230	P		X	X	X	X			
Activation anneal	1050 °C	60sec		X	X	X					
	1050 °C	10sec					X	X			
	1100 °C	0sec							X	X	X

Table 5.1: Implantation and annealing specifications of the p^+n and n^+p samples. Data as provided by NXP

In Table 5.1, S2-S6 are the p^+n samples with sample S2 as the reference sample and S7-S9 are the n^+p samples with sample S9 as the reference. After the fabrication of Ohmic contacts to these samples, as described in the next section, CV and IV measurements

were performed on each diode of every sample. The diode with the best characteristics was then chosen, that displayed the best CV results, least leakage current and highest breakdown voltage from the IV characteristics, and further measurements including DLTS and LDLTS were performed on this diode. For the sake of simplicity therefore, the number of the sample as shown in Table 5.1, will be used throughout the following chapters, to distinguish the diode with the best characteristics chosen from that particular sample. For instance, the notation S2 means the best diode of sample 2. Upon investigation of Table 5.1 it is seen that the n-side of diodes S4 and S6, out of the p^+n diodes, should have the highest doping as these contain P, and As and P implants respectively, performed with the highest dose and energy. From the n^+p diodes, S7 has had the highest B dose implants and hence the highest doping of the p-side. SIMS profiles for these diodes were also provided by NXP. Fig. 5.1 shows the SIMS profiles of diodes S3 and S4 that only have B and P implants while Fig. 5.2 shows those of diodes S5 and S6 that also contain As implants. Finally Fig. 5.3 shows the SIMS profiles of the n^+p diodes S7 and S8. SIMS of the reference diodes S2 and S9 were not available.

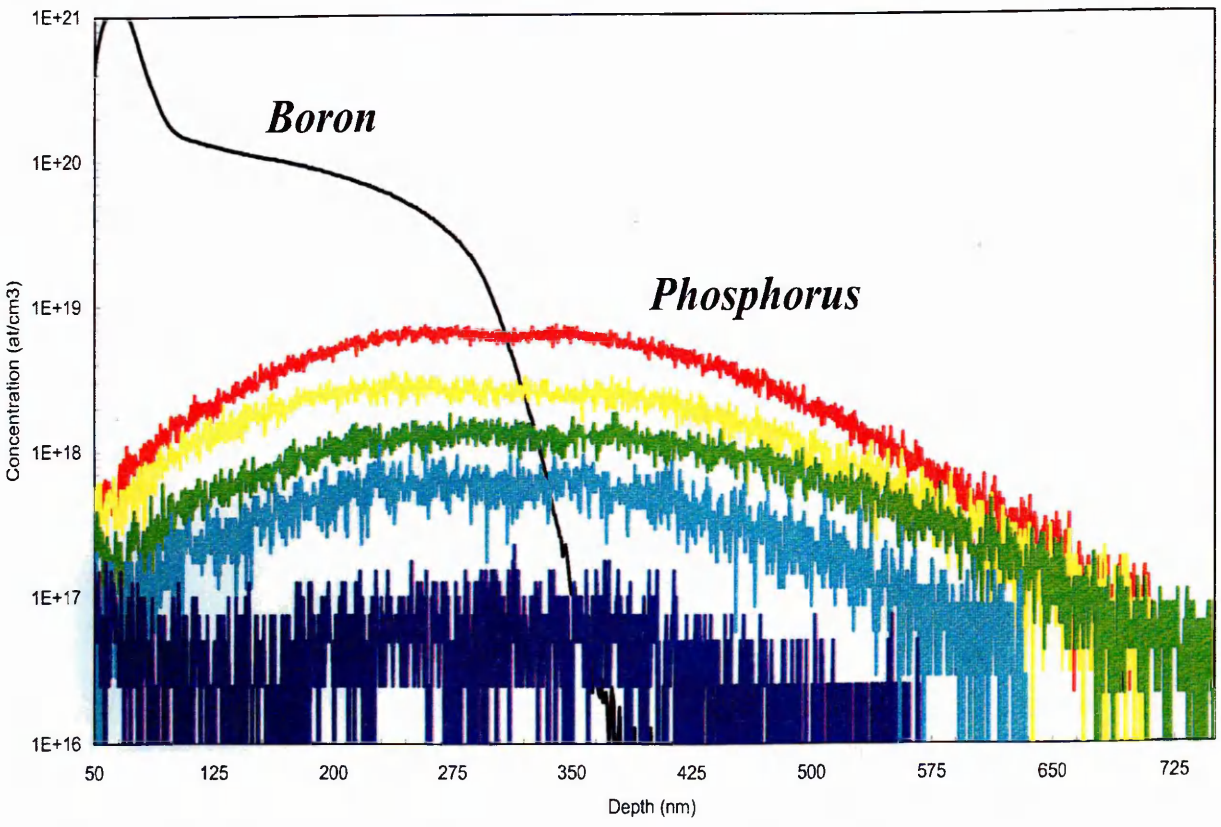


*Fig. 5.1: SIMS profiles for p^+n diodes **S3 (green line)** and **S4 (red line)** as supplied by NXP. The remaining spectra do not correspond to diodes examined in this work*

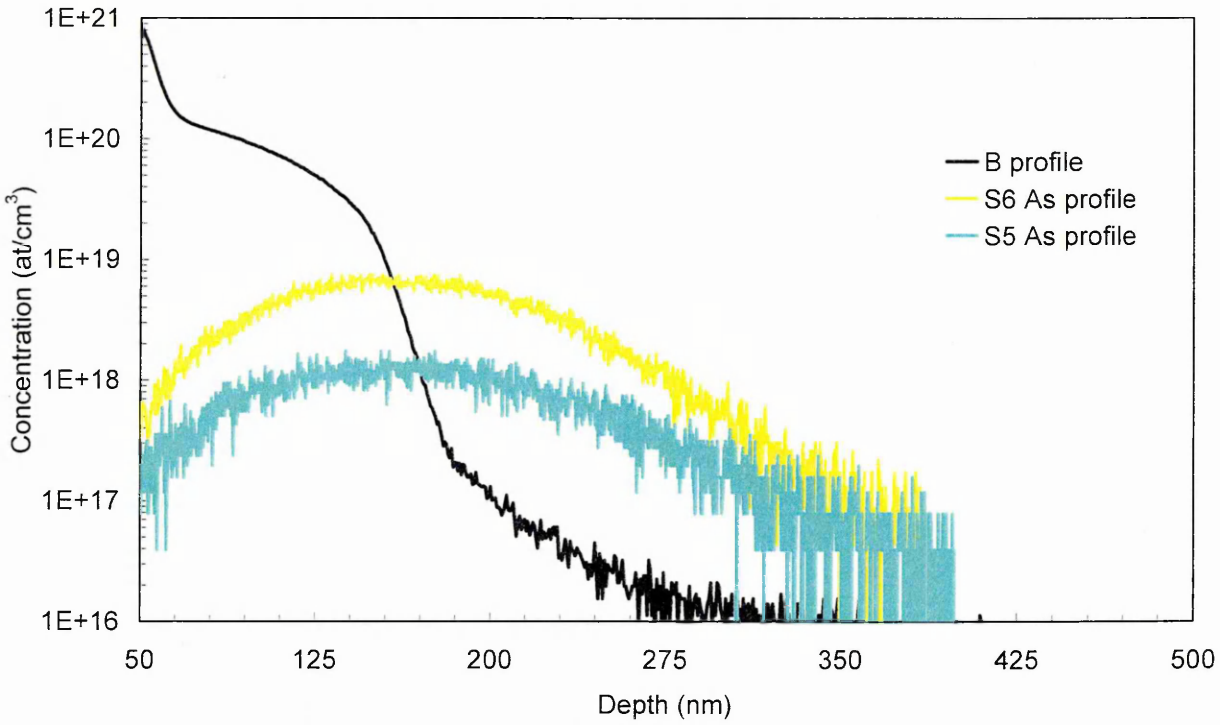


Fig. 5.2: SIMS profile for p⁺n diodes S5 and S6, supplied by NXP

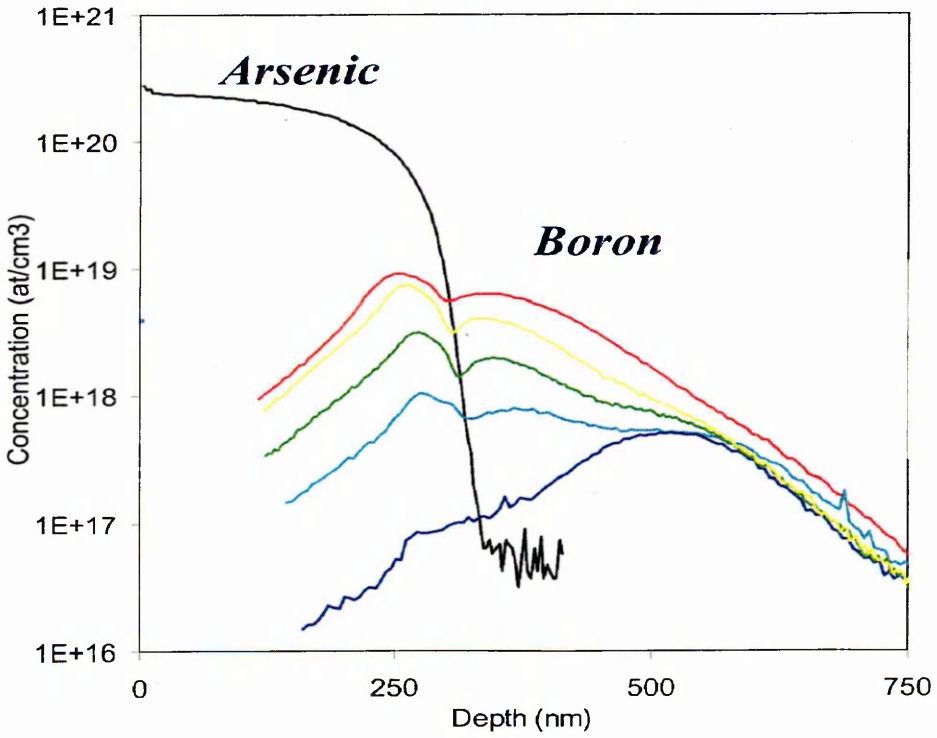


*Fig. 5.3: SIMS profile for n⁺p diodes **S7** (**yellow line**) and **S8** (**green line**), supplied by NXP*

The SIMS profiles measure the concentration of dopant atoms, unlike CV measurements which provide information about the ionized carrier concentration within the depletion region of the diode, under applied bias. For this reason SIMS also measures the doping content from the surface of the sample, while the concentration-

distance (N-x) profiles extracted from CV measurements reveal the carrier concentration profile with depth, from the p-n junction interface. This is because the CV measurements sample the low doped side which exists from the p-n junction and towards the substrate.

Certain comments can be made from careful examination of the SIMS profiles which will be helpful in the analysis of the experimental results in the following chapters.

- As a general rule, the resulting doping concentration is five orders of magnitude higher than the implantation dose.
- The n-side of the p^+n diodes and the p-side of the n^+p diodes have also high doping which is expected to affect the relationship with their respective substrates.
- Fig. 5.2 shows that transient enhanced diffusion (*TED*) of B is present in diodes S5 and S6 as the doping profile reveals diffusion of B atoms deep into the n-side at the end of range of the implant. Although it is not clear from the SIMS characteristic this may also be taking place in diodes S3 and S4.
- As TED is detected very close to the depletion region (~100nm) in S5 and S6, this volume may be accessible for examination by DLTS measurements.
- The As implant for the formation of the n^+p diodes resulted in a much steeper profile than the B implant of the p^+n diodes.
- At the depletion region (~ 300nm from the surface) of the n^+p diodes, a small decrease of the B concentration is observed near the interface with the n^+-side.

5.3 Ohmic contacts to the USJ diodes

The fabrication of the ohmic contacts to the USJ diodes involved cleaning, contact formation and bonding. Cleaning required the following steps:

- The samples were placed consecutively in trichloroethylene, then in acetone and finally in methanol in an ultrasound bath for 5 minutes each time and eventually rinsed in de-ionized (*DI*) water.
- A 2:1 Sulphuric acid: Hydrogen Peroxide treatment for 10 minutes followed and another DI-water wash.
- A 5-minute immersion in 10% HF and DI-water dip.

- RCA1 treatment was performed which involved: Immersion in a 1:1:5 Ammonia solution: Hydrogen Peroxide: Water for 10 minutes at ~70°C and then in DI water.
- RCA2 treatment involved boiling in a 1:1:6 Hydrochloric Acid: Hydrogen Peroxide: Water solution for 10 minutes at 70°C and a DI water dip.
- Finally a 15-second dip in 48% HF for removal of any native oxide, subsequent dip in methanol and blow drying with nitrogen were carried out.

For the p^+n diodes the front contact on the p-side was formed by Au evaporation through a patterned mask with holes 1mm in diameter. This provided the front ohmic contacts with a diode area of $0.785mm^2$. Al was evaporated on the rear side of these diodes to form the ohmic contacts.

The front contact of the n^+p diodes was fabricated by evaporation of Al through the patterned mask and the back contact by Au evaporation. A vacuum evaporator was used for these evaporations where the samples are placed in a vacuum chamber and the metal to be evaporated is placed on a tungsten filament. As current passes through the filament with the application of bias at its terminals the metal melts and is eventually deposited on the samples. A typical diffusion evaporator is shown in Fig. 5.4 [1].

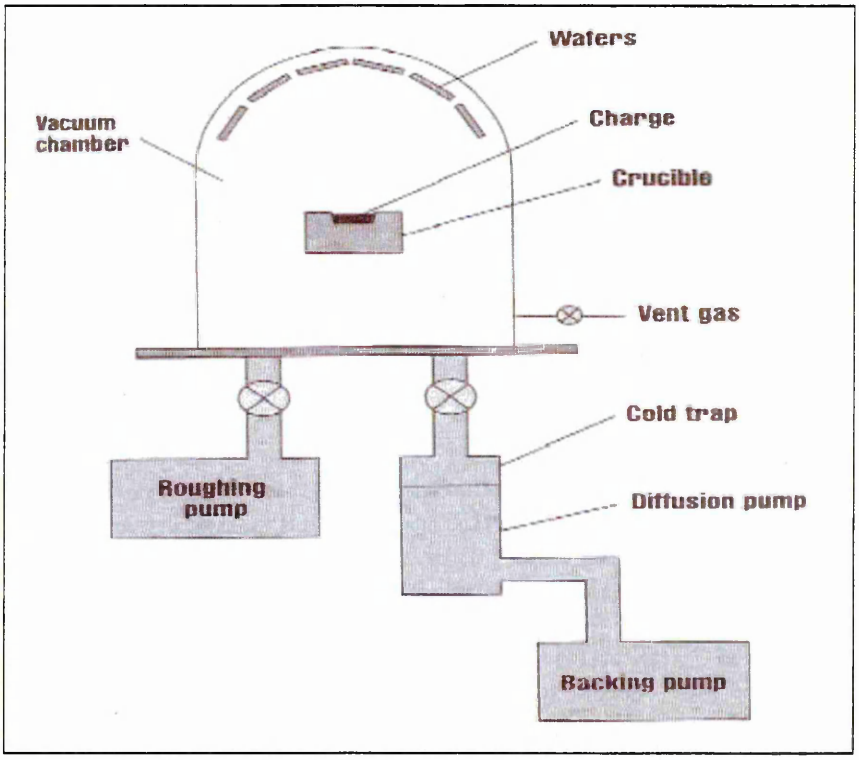


Fig. 5.4: Schematic diagram of a vacuum evaporator [1]

For bonding the rear contact of the samples is secured with silver paint on ceramic that has gold contact pads on its surface to assist conduction. The front contact of the diodes is then bonded with thin gold wires on the gold pads of the ceramic. This ensures that the diode surface remains intact during measurements.

5.4 Specifications of diamond diodes on Si

Two types of diamond diodes on Si were investigated. P-type diamond films on p-type Si substrates which result in Schottky diodes and p-type diamond films on n-type Si which form p-n diodes. P-type {111} Si wafers with resistivity 0.1-1 Ωcm and n-type {100} silicon with 1-20 Ωcm resistivity were used as the substrates. The diamond films were grown by Dr. P.W. May in the hot-filament chemical vapour deposition (HFCVD) reactors at the University of Bristol. Different amounts of diborane (B_2H_6) were added to the gas mixture during growth in order to achieve films with different conductivities. Diamond growth was carried out at a process pressure of 20 Torr using 1%CH_4/H_2 as the process gases. The films were grown for 7.5 hours at a growth rate of ~0.5μm/h yielding a thickness of ~3-4μm. One of the diamond films on n-type Si was kept nominally undoped and intended for use as a control sample. Table 5.2 shows the B doping of the diamond films for both Schottky and p-n diodes as provided by a SIMS calibration graph and absorption measurements performed by Dr. May.

	Diamond film	B concentration in diamond (cm^{-3})
p-n diodes	JEF1	$7*10^{18}$
	JEF2	$6*10^{20}$
	JEF3	$7*10^{21}$
	JEF4	Background doping only
Schottky diodes	JEF6	$1.9*10^{20}$
	JEF7	$2.1*10^{20}$
	JEF8	$5.8*10^{20}$
	JEF9	$7.6*10^{20}$

Table 5.2: B concentration of HFCVD grown diamond films

Semiconducting diamond and in particular polycrystalline diamond and its properties were discussed in detail in chapter 3. However, it will be mentioned once more that despite the very high doping of these diamond films, the measured carrier concentration is expected to be low as due to the large bandgap of diamond, even a shallow acceptor such as B has low ionisation at temperatures below 300K. However, it still proved possible to carry out CV measurements. The purpose of examining both Schottky and p-n diodes is to investigate different regions of the diamond films for potential defects. The volume examined in Schottky diodes lies adjacent to the surface of the film in contact with the metal, while for p-n diodes a depletion region arises where the interface of two different semiconductors is formed. By profiling at these two different regions of polycrystalline diamond films, more information about the nature of defects as growth proceeds will be revealed. To ensure that any observed defects are present in the diamond films, in particular in the p-n diodes, high quality Si single-crystal substrates were used. These were manually abraded before deposition using 1-3 μm diamond grit. The film identification (i.e. JEF1) will be used in the following chapters to refer to the diode with the best CV and IV characteristics on which DLTS and LDLTS measurements were performed.

5.5 Fabrication of diamond-silicon diodes

The fabrication included cleaning, a diamond surface treatment and deposition of appropriate metal contacts. Cleaning involved the following steps:

- Degreasing the diamond and Si surfaces by 5 minute immersion and ultrasound baths successively in trichloroethylene, acetone and methanol.
- Removal of metallic impurities in a solution of 1:1:5, NH_4OH: H_2O_2: H_2O for 10 minutes at 70°C and subsequent DI-water wash.
- Removal of organic impurities in a solution of 1:1:6, HCL: H_2O_2: H_2O for 10 minutes at 70°C and DI-water rinse.

The surface of the diamond is usually hydrogen terminated after HFCVD growth, since the surface is an abrupt ending of growth and unsatisfied bonds are present. However, hydrogen causes increased surface conductivity reducing the current passing though the film. Hence oxygen passivation was applied using a plasma asher for a few seconds (5-10s) resulting in the removal of the hydrogen.

Subsequently metal contacts were deposited on the diamond and Si for the formation of diodes either by evaporation or rf sputtering. Sputtering involves plasma (oxygen or argon) generation in high vacuum, caused by the heating of the source gas, bombardment of the chosen metal target by the gas particles accelerated by a magnetic field and eventual deposition of a thin layer of the metal on the surface of the sample from detached metal atoms. Sputtering metal deposition is more accurate and controlled than metal evaporation as it can be monitored.

- Ohmic contacts on the p-type diamond were formed by rf sputtering of a sandwich layer of Ti/Pt/Au in the ratio of 20nm/30nm/300nm through a patterned mask of 1mm in diameter holes [2].
- Annealing of the sandwich Ti/Pt/Au contacts is a necessary step following the sputtering, as the formation of a thin layer of TiC with the surface is very significant for the subsequent diffusion of Pt and Au. Hence these contacts were annealed at 673K in vacuum for 20 minutes in order to achieve good ohmic contacts.
- Schottky contacts were formed on the p-diamond by Al evaporation through the patterned mask of 1mm in diameter holes.
- Ohmic contacts on the rear Si side were also formed by Al evaporation.

Bonding of the Schottky and p-n diodes was performed as described earlier for the USJ diodes, on ceramic with gold surface pads using silver paste. Front Schottky or ohmic contacts from each diode to the gold on the ceramic were formed with gold wires to protect the diode surface during measurement.

5.6 Experimental set-up

The equipment used for the electrical characterisation of both USJ and diamond diodes included:

- A Boonton 72B Capacitance meter was used for the CV and DLTS measurements
- A Keithley 6487 Picoammeter/Voltage Source is used for the IV measurements.
- A Lakeshore 340 Temperature controller for setting and controlling the temperature during measurements.

- An Edwards oil pump for pumping the system to vacuum and an Edwards ADG high vacuum indicator for monitoring the pressure of the sample chamber.
- An Advanced Research Systems (ARS) 4HW Cryostat.
- A computer for controlling the parameter settings and recording the results including the LDLTS software and a Labview-based programme for the IV measurements.

Two different sensors were used to monitor the sample temperature inside the vacuum chamber and the ambient temperature inside the chamber. Their output was fed back into the temperature controller in order to maintain a constant temperature or the appropriate rate of temperature change during measurements. A silicon sensor was used for measurements from 20-480K and a high temperature platinum sensor for measurements from 70-690K.

5.7 Conclusions

This chapter presented the specifications and fabrication methods of the diodes examined in this project. This was essential as very different sets of diodes have been investigated. First, details of both the p^+n and n^+p Ultra-Shallow junction diodes in Si were provided, together with the necessary SIMS profiles that illustrate their doping concentrations. The fabrication method of contacts to these diodes was also described. As the second set of diodes involved a wider bandgap semiconductor, different fabrication techniques had to be implemented and these were explained here. In addition, the specifications of these diodes were given and key points were outlined about the properties of diodes that are different to those made on Si. Finally, the set-up used in the investigation of these diodes was detailed.

References

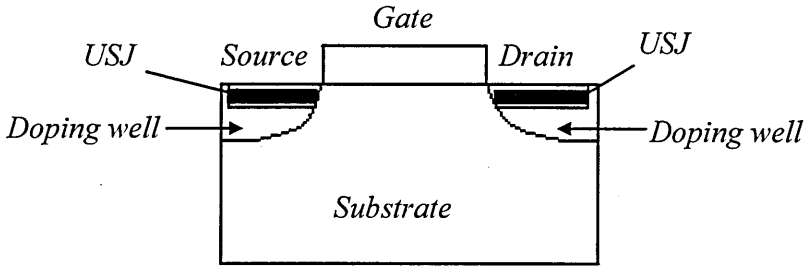
[1] R. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory (Prentice Hall International Inc, 1999).

[2] Y. Chen, M. Ogura, T. Makino, S. Yamasaki and H. Okushi, Semiconductor Science and Technology 20 (2005) 1203.

Chapter 6: Experimental results from p$^+$n Ultra-shallow junctions

6.1 Introduction

This chapter presents results obtained from the investigation of p$^+$n Ultra-Shallow Junctions (*USJs*) in Si. As mentioned in chapter 2, a reduction of the p-n junction depth is required in modern transistors in order to avoid short channel effects. These are caused by the aggressive scaling of the device dimensions which require a decrease in the channel length of MOSFETs. The following diagram illustrates the position of the ultra-shallow junctions within the structure of a transistor.



Schematic 6.1: The location of the ultra-shallow junctions in a transistor

The doping well in the USJ diodes that will be examined here originates form the multiple implants. For the p$^+$n USJs the n-side is also heavily doped with concentration much higher than that of the substrate to simulate the doping well. The high doping of both the p$^+$ and n- sides is designed so as to result in the shallow junction according to Eq. 4.2. However when the junction depth is very narrow, phenomena such as tunnelling or thermionic emission may be taking place. In addition, a narrow depletion region increases the possibility of diode breakdown and this will be examined here. The implantation details of these diodes were shown in chapter 5 together with the SIMS profiles that described their doping levels. In this chapter the electrical characterisation of these p$^+$n USJ diodes, whose fabrication was described in the previous chapter, will be shown. This involved CV, IV, DLTS and LDLTS measurements. The notation for the distinction of the diodes will involve a number which corresponds to that of Table 5.1 for each sample. The aim of this work, as previously mentioned, is to perform electrical characterisation of these industrially important structures and in particular to examine the applicability of DLTS and LDLTS to such small volumes and junction depths.

6.2 Control diode S2

This diode had a B implant alone on the n-type substrate which makes it a typical asymmetric p+n diode. By examining the CV and the resulting concentration-distance (N-x) profiles, the background doping of the n-type substrate can easily be determined. In addition DLTS will reveal if any deep levels can be found in the substrate, although such defects are not expected from high quality commercial Si which forms the n-side in this diode. Fig. 6.1 shows the CV results from diode S2 in this control sample and Fig. 6.2 shows the resulting N-x profiles at the same temperatures. These were taken as the temperature reduced from 300K. For clarity only a few of these characteristics are shown.

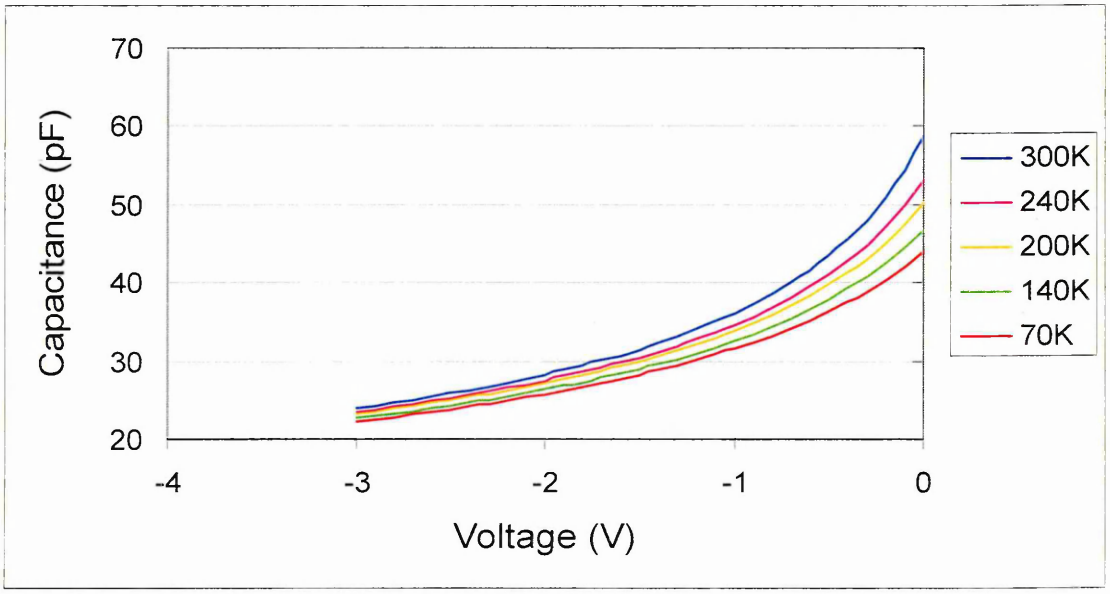


Fig. 6.1: CV plots at different temperatures of diode S2

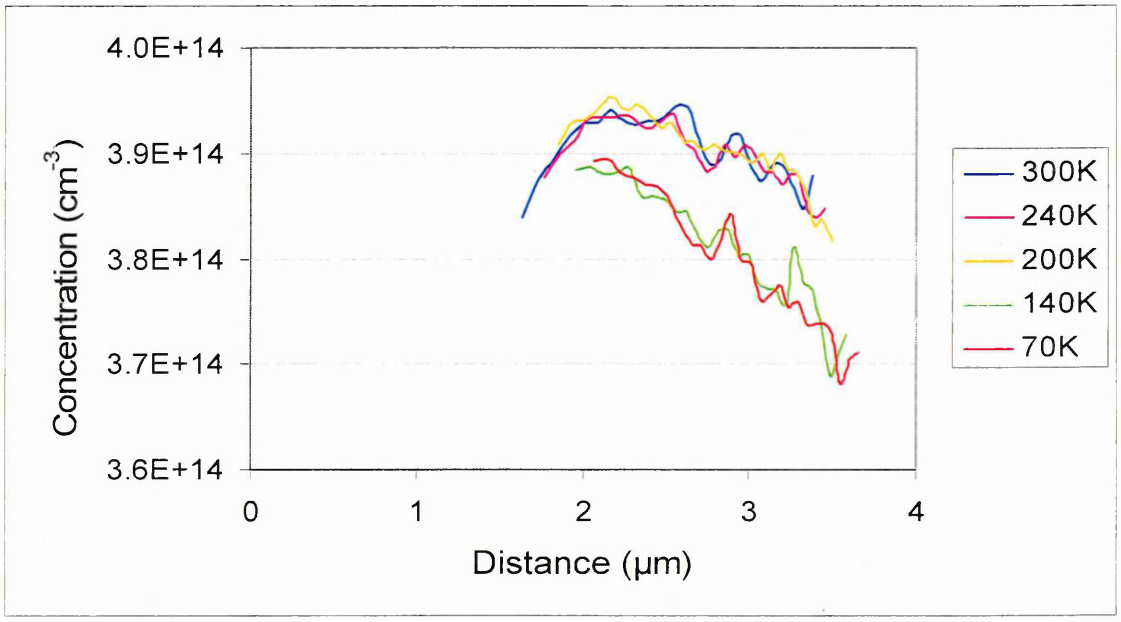


Fig. 6.2: N-x plots at different temperatures of diode S2

In Fig. 6.2 the distance on the x-axis is the depth measured from the interface of the p^+ and n-sides not from the surface of the diode. Hence the zero denotes the junction at this interface. This is because as mentioned in chapter 5, N-x results obtained from CV, measure the carrier concentration within the depletion region under the application of bias. On the contrary the SIMS profiles shown in chapter 5 measured the concentration of the dopants in the implanted region and hence covered a volume from the surface until the end of the implant. Fig. 6.1 shows that as the temperature decreases, the capacitance decreases, which is to be expected for a normal p-n diode since fewer dopants are ionised at lower temperatures. This can be verified from Fig. 6.2 where the carrier concentration reduces as temperature decreases. The effect on capacitance can be explained if Eq. 4.2 and 4.5 are taken into account, where for lower carrier concentration, the depletion region width increases while the capacitance decreases. The p-side of this sample has been heavily implanted and effectively all of the depletion region will appear on the n-side. The p-side doping dose is $5*10^{15}cm^{-2}$, which as a general rule, will result in approximately 5 orders of magnitude higher carrier concentration. Fig. 6.2 shows that the n-side carrier content is about $3.9*10^{14}cm^{-3}$ hence around 5-6 orders of magnitude lower than the p-side. From the same figure it can be seen that a depth of 2μm from the interface is being profiled, which on the SIMS profile of Fig. 5.1 for these p^+n samples would correspond to a depth deep inside the substrate and hence is not shown. Therefore any defects detected at this depth would be in the substrate, although none are expected. To complete the capacitance measurements, Fig. 6.3 illustrates the capacitance-temperature (*C-T*) measurements for S2.

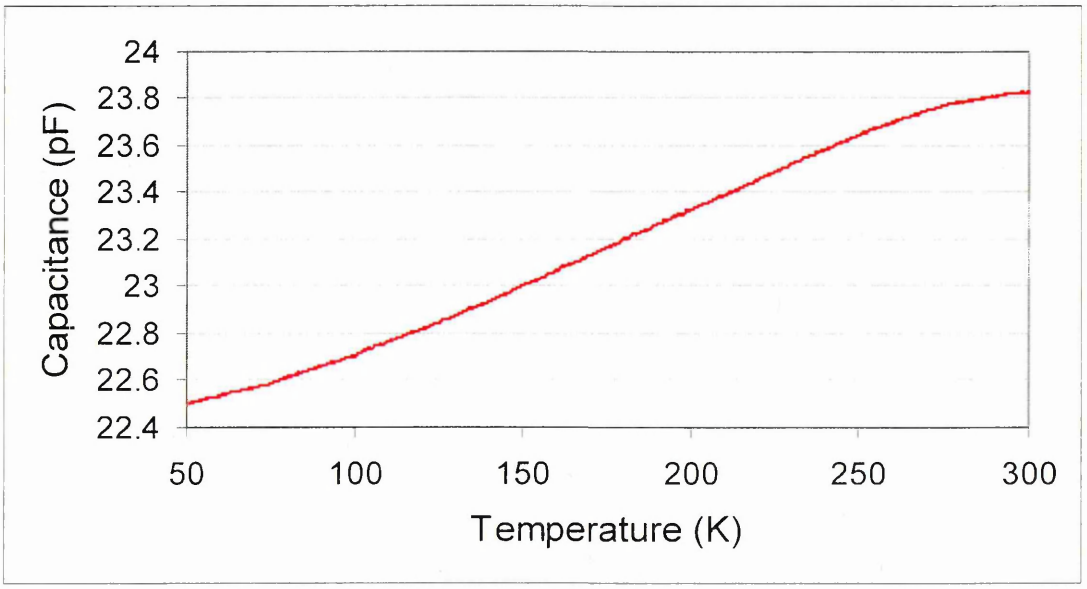


Fig. 6.3 C-T measurements of S2 from 50-300K under -3V reverse bias

The capacitance is reducing as the temperature drops as expected and the capacitance values are in accordance with Fig. 6.1 at -3V. This is an indication of a good diode. The IV measurements of S2 at different temperatures are shown in Fig. 6.4. The reverse current is very small and is not very clear on this scale. However, as the temperature decreases from 300K the reverse current also reduces. It has a value of 50nA at 300K, 40nA at 200K and 30nA at 100K at -3V. The forward current also gradually reduces with decreasing temperature as expected and it has a value of 3.6mA at 300K, 2.6mA at 200K and just 1.3μA at 70K at 1V forward bias. In general, the IV characteristics indicate good diode-like behaviour with low reverse current of consistently decreasing magnitude as the temperature reduces. Hence the leakage current of the diode is very low, in the order of nA, which suggests that there may not be any trap levels capturing carriers in the bandgap. However this is examined in detail by the DLTS measurements that follow.

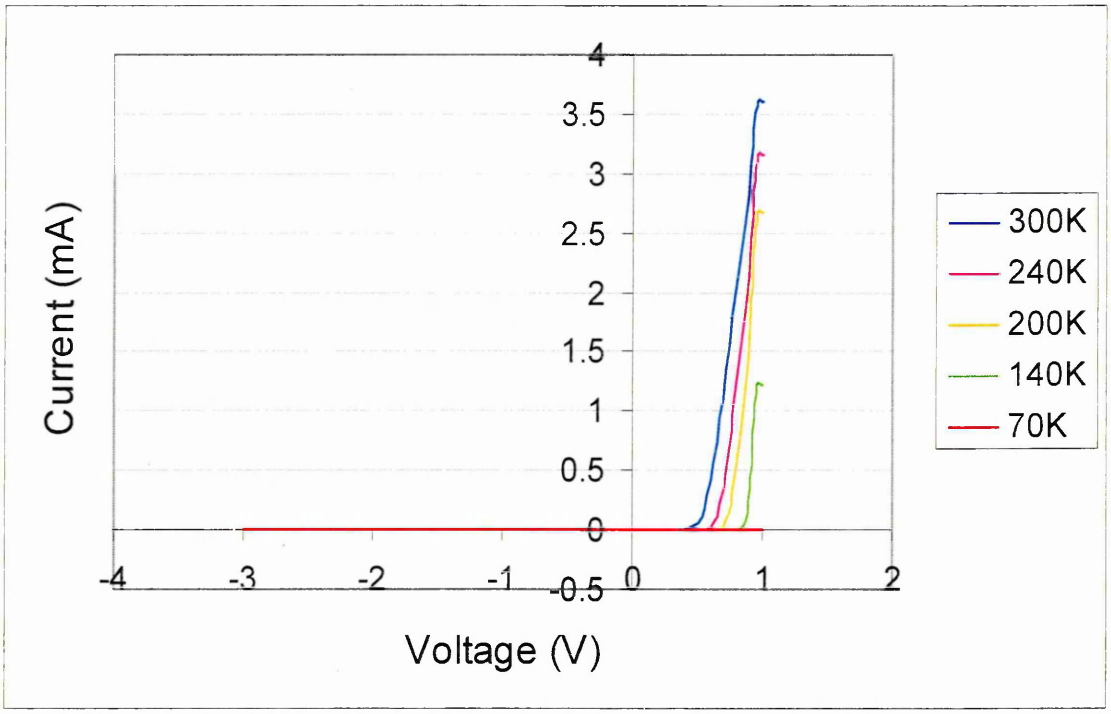


Fig. 6.4: IV measurements of S2 at different temperatures

DLTS was performed under reverse bias and with different fill pulse biases to investigate both majority and minority carrier traps. Both small and large positive fill pulses were applied in order to introduce holes, or both electrons and holes by collapsing the depletion region momentarily but no traps were detected in the DLTS spectra. Two examples with small and large positive fill pulse are shown in Fig. 6.5.

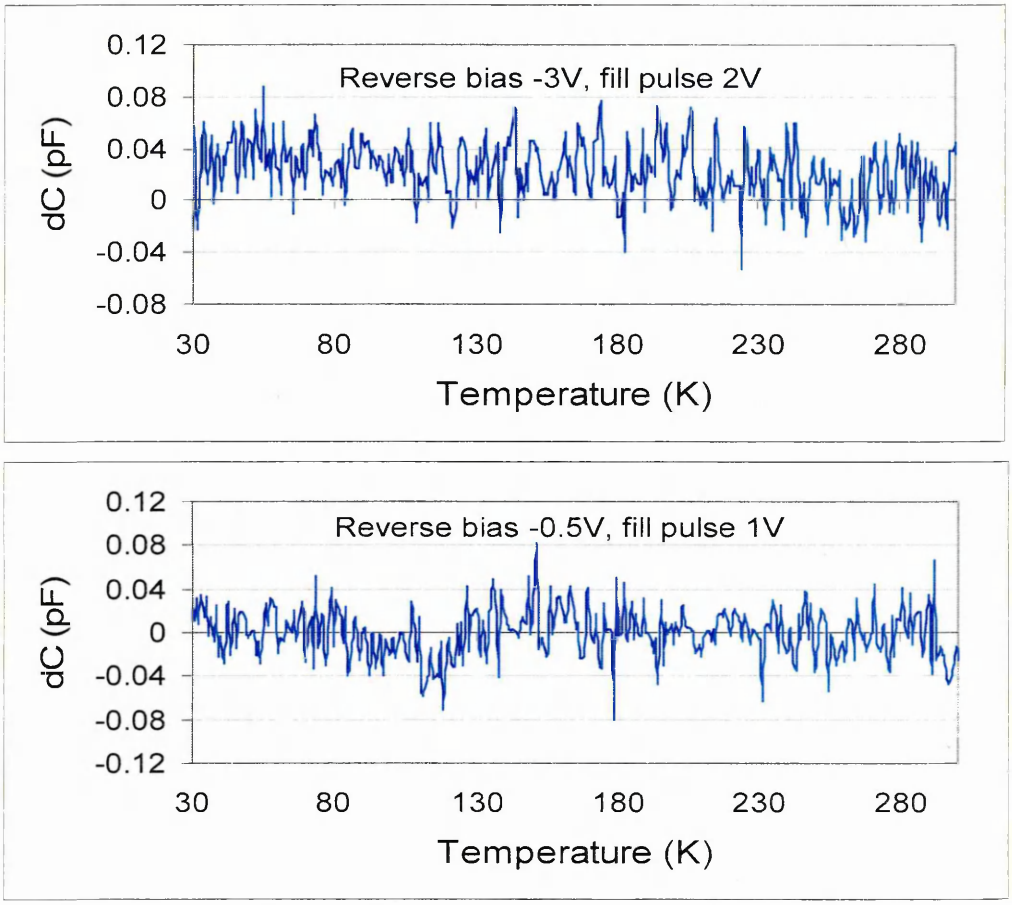


Fig. 6.5: DLTS spectra for S2 with small positive fill pulse (top) and large positive fill pulse (bottom)

Fig. 6.5 shows that no traps were revealed by DLTS in diode S2 and hence no carrier traps should exist in the substrate. Therefore in the following diodes any trap levels will be due to the combination of B with other dopants.

6.3 Diode S3

Diode S3 has the same B implant as the control diode but it also has two additional P implants. The SIMS profile that was shown in Fig. 5.1 (green line) yielded a P concentration of $1*10^{18}cm^{-3}$. Fig. 6.6 shows the CV and N-x profiles obtained for S3 at different temperatures. The CV characteristics of S3 are very peculiar and show that the capacitance is generally very large (in nF). As the temperature decreases the capacitance increases, which is the opposite from what is expected as that would imply that carriers have more energy at lower temperatures. In addition, the capacitance initially increases and then abruptly decreases at a certain bias. For instance at 300K any bias below about -0.7V brought the capacitance to zero and this is the reason larger bias was not applied. The onset of this abrupt capacitance drop however, appears to take effect at slightly higher biases as the temperature reduces.

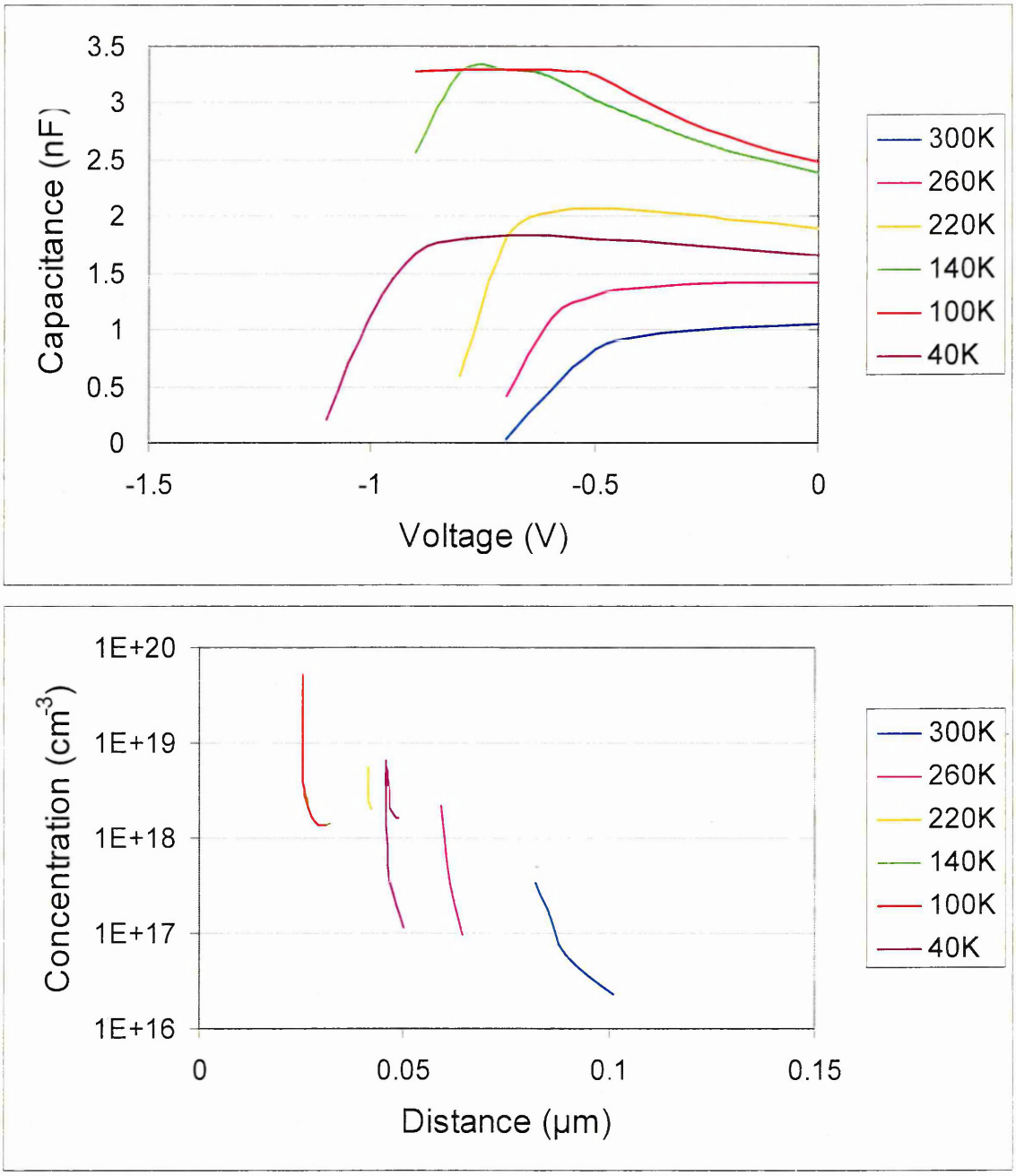


Fig. 6.6: CV (top) and N-x (bottom) profiles of diode S3 at different temperatures

The contacts and the polarity of the connection were verified several times to ensure this phenomenon was not a system error. Moreover the concentration profiles shown in Fig. 6.6 also reveal unconventional diode characteristics. The carrier concentration at 300K is in the order of $1*10^{17}cm^{-3}$ so it appears to be an order of magnitude smaller than that of the SIMS profile. However, it should be mentioned that the CV measurements reveal carrier and not doping concentrations. Also the remaining N-x profiles at lower temperatures appear unreasonable since the carrier concentration is increasing in a very abrupt manner not only with applied bias but even as the temperature decreases.

In order to explain these results it is essential to investigate the structure of this sample. It consists of a low doped n-type starting material with concentration $3.9*10^{14}cm^{-3}$, as measured from the control diode S2, a high doped n-type region of about $1*10^{18}cm^{-3}$ as can be seen from the SIMS profile and a very highly doped p-side with a concentration of approximately $3*10^{19}cm^{-3}$. It is therefore clear that the implanted n-side is much more highly doped than the n-type starting material (bulk). It can hence be suggested that because of the large difference in electron concentrations between these two regions, there arises another depletion region between the starting n-type material and the phosphorus doped n-side. Since the n-region is much more highly doped than the starting material there will be a Fermi level difference which is reflected by the conduction and valence band offset at the $n\text{-}n^-$ interface. To illustrate this phenomenon, Fig. 6.7 shows the energy band diagram for this sample at equilibrium. It should be mentioned that a similar configuration is expected to occur in the remaining diodes irrespective of their doping level, as long as all implants introduce more dopants than that of the substrate.

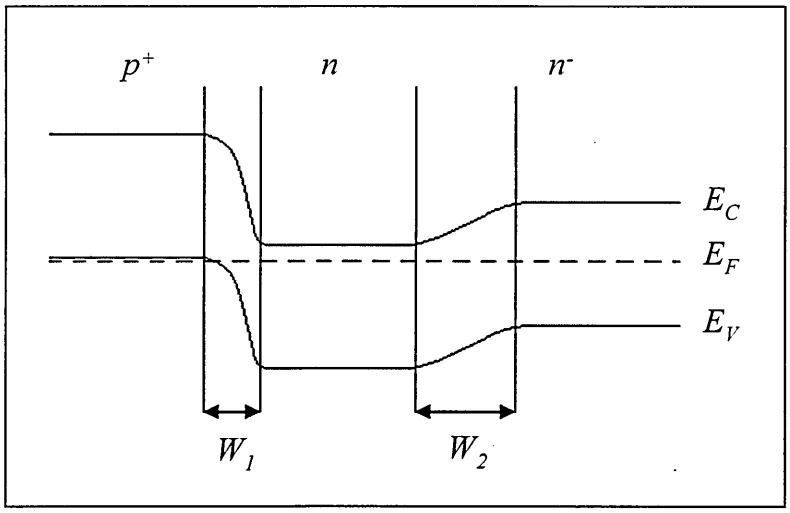


Fig. 6.7: Energy band diagram for S3 in equilibrium (not to scale)

To examine how significant this band difference is, calculations were performed to estimate it. These were also performed at lower temperatures taking into account that the carrier concentration and other parameters such as the bandgap value, change with temperature and also that the p-side is almost degenerate due to its very high doping. To find the position of the Fermi level E_F on either side of both junctions the following ionisation probability equation was used.

$$E_F = E_i \pm kT\,ln(\frac{N}{n_i}) \qquad \text{Eq. 6.1}$$

where, E_i is the intrinsic Fermi level, n_i is the intrinsic carrier concentration at each temperature and N is the acceptor or donor concentration depending on the side of the junction for which the calculation is performed. Using equation 6.1 it was found that due to the high doping, the p-side is almost degenerate and this is the reason the Fermi level is shown to be slightly into the valence band. Figures 6.8 and 6.9 show the conduction band (CB) difference for the p$^+$n and n-n$^-$ junctions respectively from calculations of the Fermi level. These calculations were performed for all of the samples and the following figures correspond to all p$^+$n diodes S3-S6.

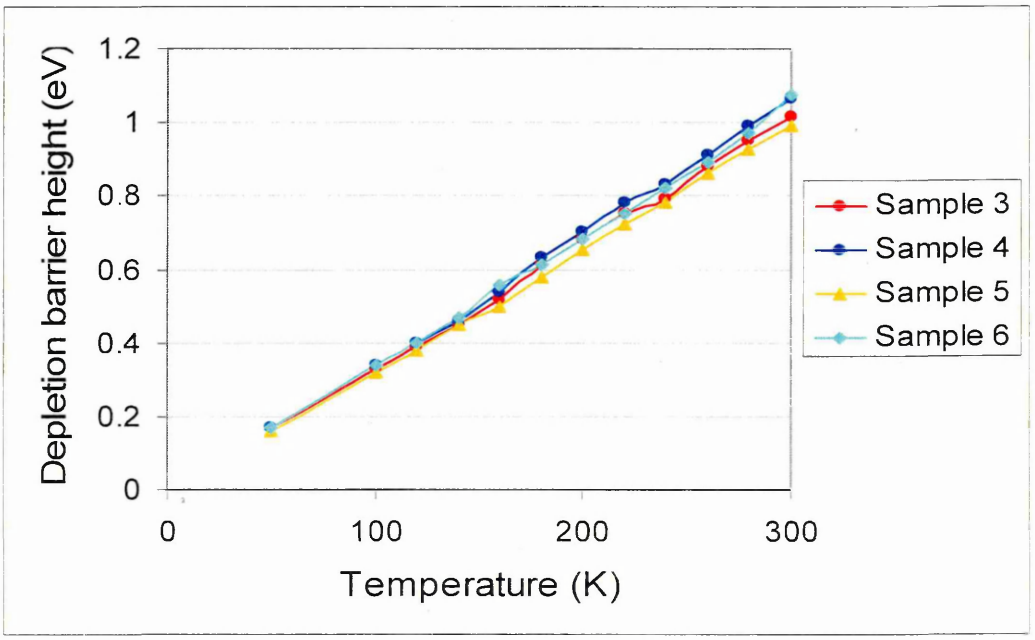


Fig. 6.8: p+/n CB barrier height with temperature

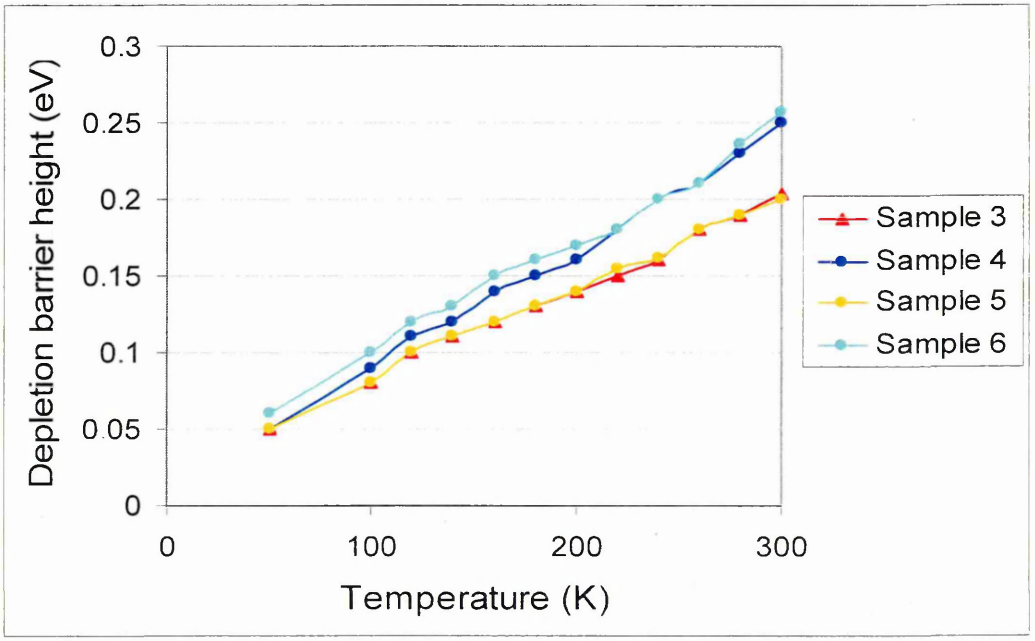


Fig. 6.9: n/n- CB barrier height with temperature

Fig. 6.8 shows that the potential barrier at the ultra-shallow p^+n junction at room temperature in equilibrium is larger than 1eV which is comparable with the bandgap of Si (1.12eV) and it linearly decreases as the temperature decreases for all diodes 3-6. This is due to the large doping concentration of the p^+ side and it can be seen that even at the very low temperature of 50K there is still a barrier height of 0.2eV even in the absence of an applied bias. By examination of Fig. 6.9, the barrier height of the $n\text{-}n^-$ junction is 0.2eV for diodes 3 and 5, which have lower doping on the n-side, as can be seen from the SIMS profiles, than for diodes 4 and 6 at room temperature. The barrier height at this temperature for diodes 4 and 6 is 0.25eV. The suggestion that there is another depletion region between the starting material and the n-side is therefore valid and in particular the barrier height is about 1/5 of the Si bandgap for diodes 3 and 5 and 1/4 of the bandgap for diodes 4 and 6, which is a significant value. However, as mentioned earlier, in this sample there are two depletion regions and hence two capacitances and therefore these theoretical calculations may not reflect the actual potential barrier difference as they were performed independently for each junction. Nevertheless, they are proof of the existence of the two junctions and they are indicative of the barrier height values with respect to the bandgap.

Throughout the following the capacitance of the p^+n depletion region will be C_1 and that of the $n\text{-}n^-$ junction C_2. Similarly, W_1 is the width of the p^+n depletion region and W_2 the width of the $n\text{-}n^-$ depletion region. Therefore it seems that the two capacitances are in series in this diode and hence the total measured capacitance will be given by:

$$C_{TOT} = \frac{C_1 C_2}{C_1 + C_2} \qquad \text{Eq. 6.2}$$

The above equation shows, that in the case where the capacitances are hugely different from each other, the smaller capacitance is the dominant one and hence the total capacitance will be virtually equal to the smaller capacitance. Therefore the measured capacitance in this and the following samples is given by a more complicated formula than that of a usual p-n diode and this is the reason the CV results are different. Hence from this point forward, "normal" polarity of experiments is defined for the case where the USJ is put into reverse bias.

During normal polarity measurements negative bias is applied to the p-side of the ultra-shallow junction. By consideration of Fig. 6.7 in the normal polarity configuration the p^+n junction is reverse biased but the $n\text{-}n^-$ junction is forward biased. In reverse bias the p^+n depletion region widens and the potential barrier increases since the holes on the p-side are attracted to the negative contact and electrons from the n-side are attracted to the positive (ground potential) contact on the n-side. On the other hand the $n\text{-}n^-$ depletion region is now forward biased which means that the potential barrier has lowered considerably, or has flattened. The band diagram of the sample under reverse bias is shown in Fig. 6.10.

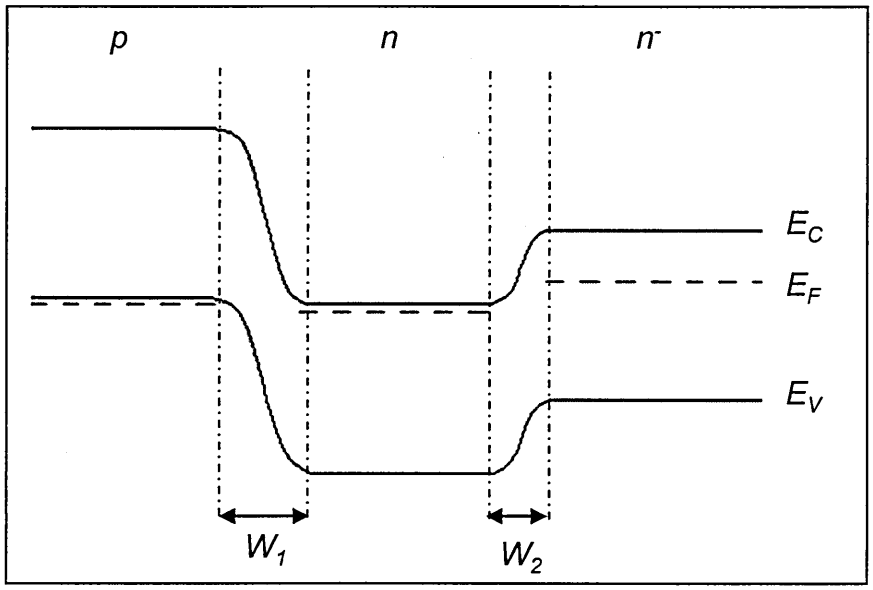


Fig.6.10: Energy band diagram of diode S3 under reverse bias

From Eq. 6.2 and by investigation of Fig. 6.10 which shows the diode under reverse bias, it can be seen that the $n\text{-}n^-$ depletion width has reduced since this junction is forward biased. Considering the low concentration of the substrate n^- and consequently the large size of this depletion region in equilibrium, it is expected that W_2 may still be larger than W_1, even in normal polarity conditions, although depletion region width calculations are necessary to confirm that. The measuring equipment is of course trying to measure the reverse biased junction, but there may still be a contribution from the $n\text{-}n^-$ junction. This is the reason the CV and N-x results appear so complicated because they contain components from both depletion regions. In this polarity, the $n\text{-}n^-$ junction that is forward biased is not essentially turned on until a bias of 0.73V, which corresponds to the built-in voltage. Therefore until this bias is achieved the system is measuring a combination of the two depletion region capacitances. After the $n\text{-}n^-$ depletion region is flat the measured capacitance should be the one of the p^+n junction.

That is why at room temperature the lowest reverse bias that could be applied is virtually 0.7V. This value corresponds to the built-in potential which is temperature dependent and slightly increases as the temperature decreases. The equation describing the built-in voltage is given by:

$$V_{bi} = \frac{kT}{q} ln(\frac{N_A N_D}{n_i^2}) \qquad \text{Eq. 6.3}$$

where, N_A and N_D are the acceptor and donor concentrations. As the temperature decreases the intrinsic concentration n_i, rapidly decreases resulting in a small increase of the built-in potential, even though N_A and N_D are also decreasing.

The presence of two depletion regions could provide the opportunity to investigate two different volumes of these p^+n diodes. Therefore apart from the above configuration of a "normal" polarity where the p^+n junction is reverse biased and the $n\text{-}n^-$ junction is forward biased, polarity could be reversed to examine the $n\text{-}n^-$ junction. The first configuration will be hence called normal polarity, and the reverse configuration opposite polarity for the remaining of the chapter. Opposite polarity measurements would mean that the diode is essentially forward biased if there was only one depletion region. However, in this case the p^+n junction is forward biased and the $n\text{-}n^-$ junction is reverse biased. The band diagram for the opposite polarity case is shown in Fig. 6.11.

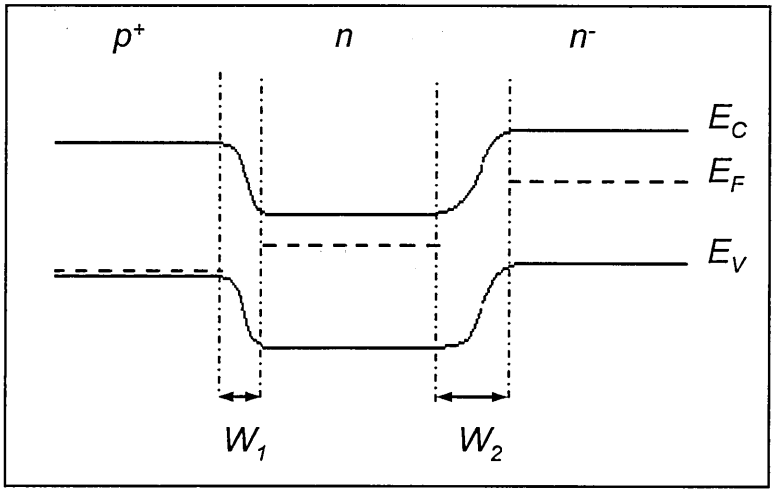


Fig. 6.11: Energy band diagram of S3 under opposite polarity configuration

The width of the reverse biased $n\text{-}n^-$ depletion region has increased, the potential barrier is higher, and electrons are repelled from the negative contact and are being pushed into

the n-region. Also as the p^+n junction is forward biased and hence the potential barrier there has lowered. Measurements were performed with both configurations for all the p^+n diodes, where possible. Fig. 6.12 and 6.13 show the CV and N-x profiles obtained with the polarity reversed. These show that the capacitance at 300K without any bias is large (nF) and continues to increase as the temperature decreases until it finally decreases at the lowest temperature of 40K. This is once again opposite from what is expected for a normal diode but here the capacitance contribution from both depletion regions needs to be taken into account.

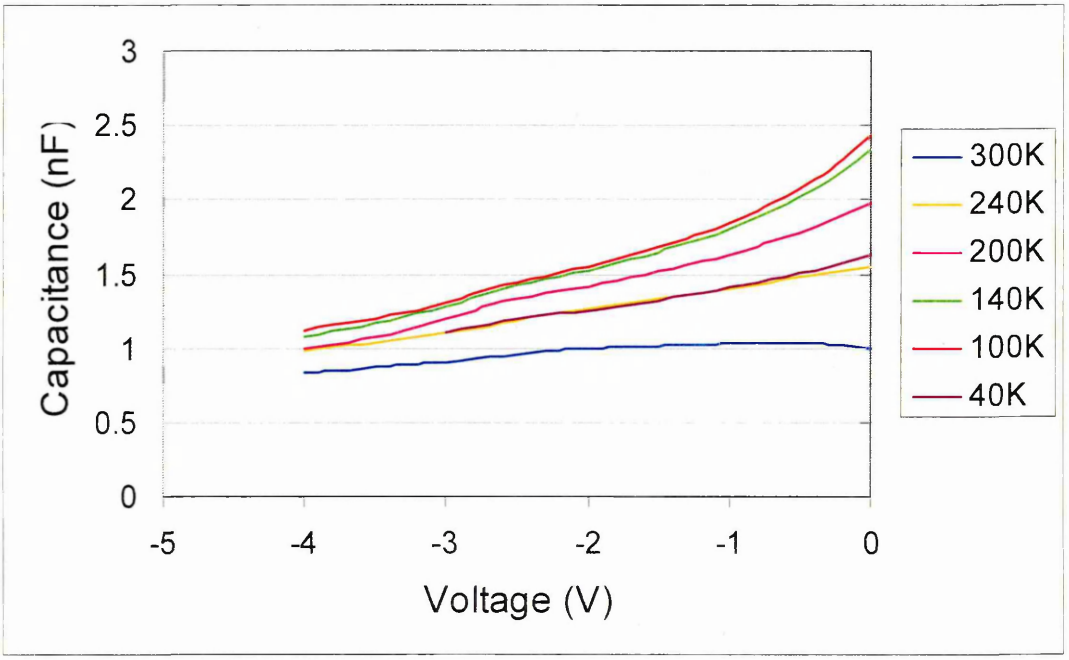


Fig. 6.12: CV measurements of S3 with opposite polarity

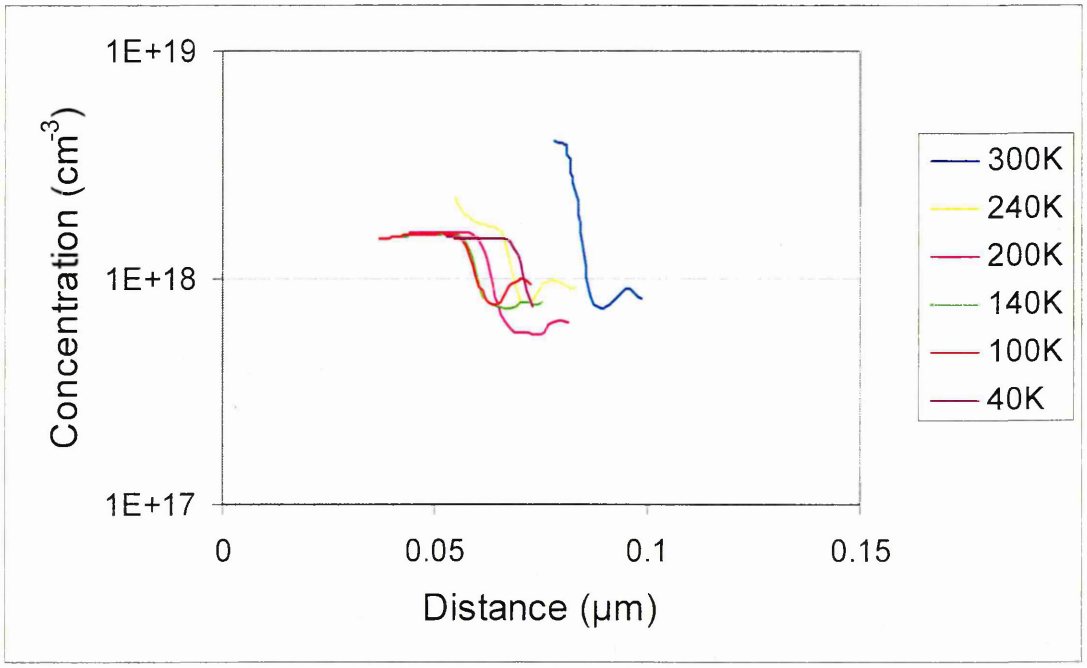


Fig. 6.13: N-x profiles of S3 with opposite polarity

Furthermore in this opposite polarity configuration the capacitance decreases as the reverse bias increases in magnitude, with a minor exception at room temperature, as it should be the case for a diode. The opposite happens in the original configuration of the normal polarity. The N-x results also appear to be more reasonable since the carrier concentration seems to decrease with increasing depth more slowly. Also with this polarity the concentration slightly decreases with temperature as should be the case. The carrier concentration as measured from the opposite polarity configuration, is more comparable to the SIMS value of $1*10^{18}cm^{-3}$ but as again the CV data indicate that the capacitance is due to two depletion regions, this value is not entirely accurate. It is interesting to note however, that the depth profiled both in the normal and opposite polarity (50-100nm) is almost the same as can be observed from Fig. 6.6 and 6.13. Once again, since this was obtained from N-x measurements, this means that the depth of the depletion region scanned is from 50nm to 100nm from the interface between the p^+ and n-sides and not from the surface of the diode. However, as the normal polarity should be investigating the p^+n depletion region and the opposite polarity the $n\text{-}n^-$ junction, the similarity between the depths profiled with normal and opposite polarities may be coincidental. On the other hand this may be an indication that in this diode under both configurations the same depletion region is being profiled. This will be later confirmed from the DLTS measurements. Fig. 6.14-6.16 show the IV results from diode S3 both with normal and reverse configuration with a magnified view of the reverse current under normal polarity for ease of comparison.

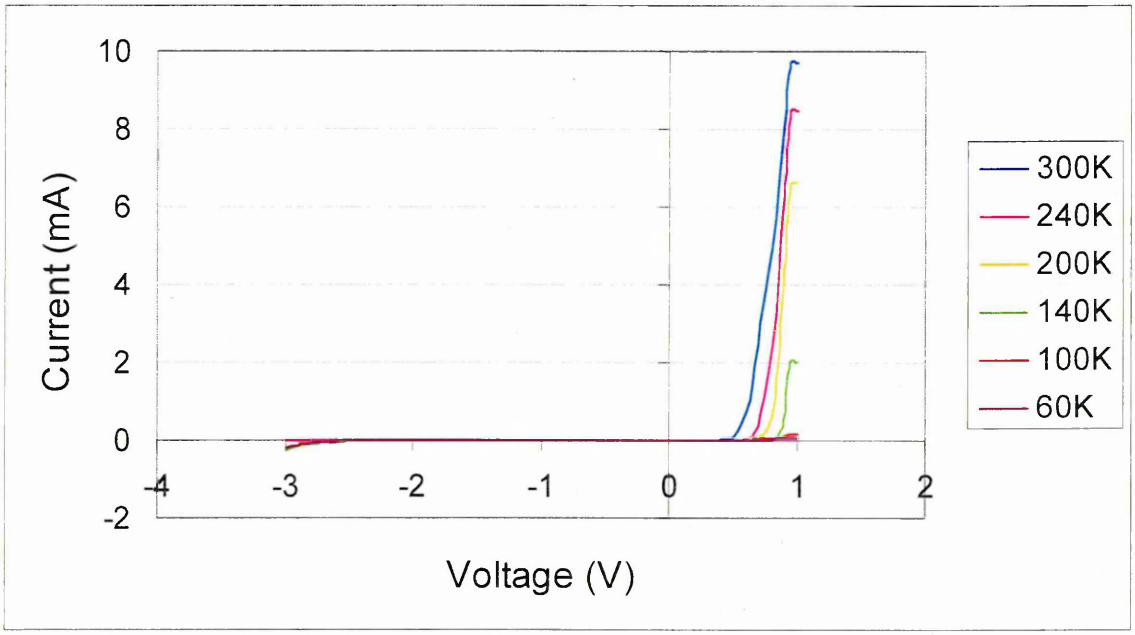


Fig. 6.14: IV measurements of S3 at different temperatures with normal polarity

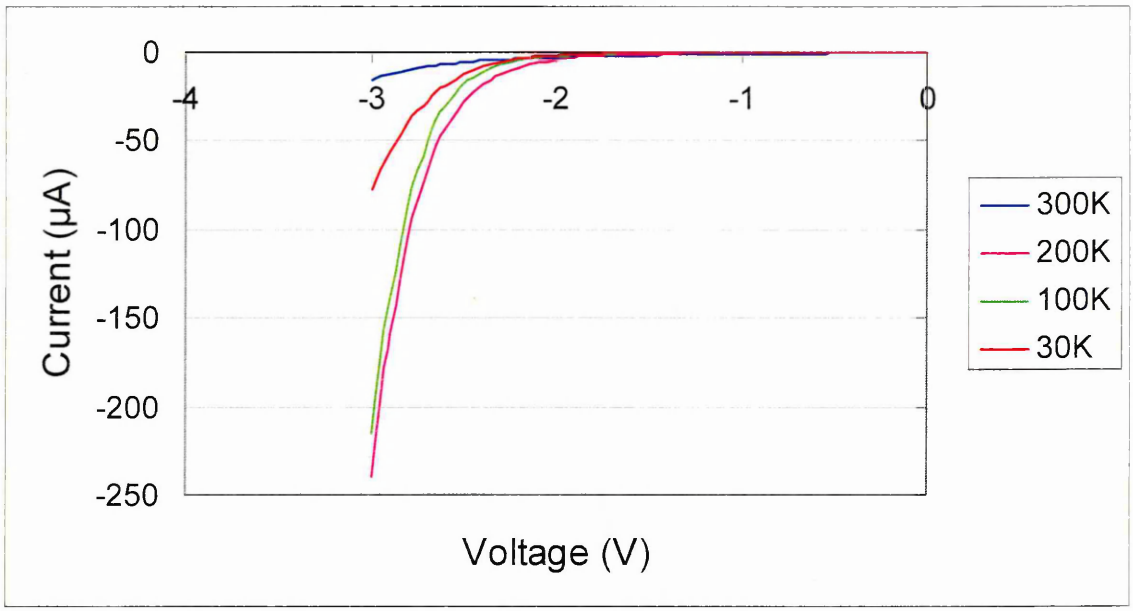


Fig. 6.15: Reverse current of S3 at different temperatures with normal polarity

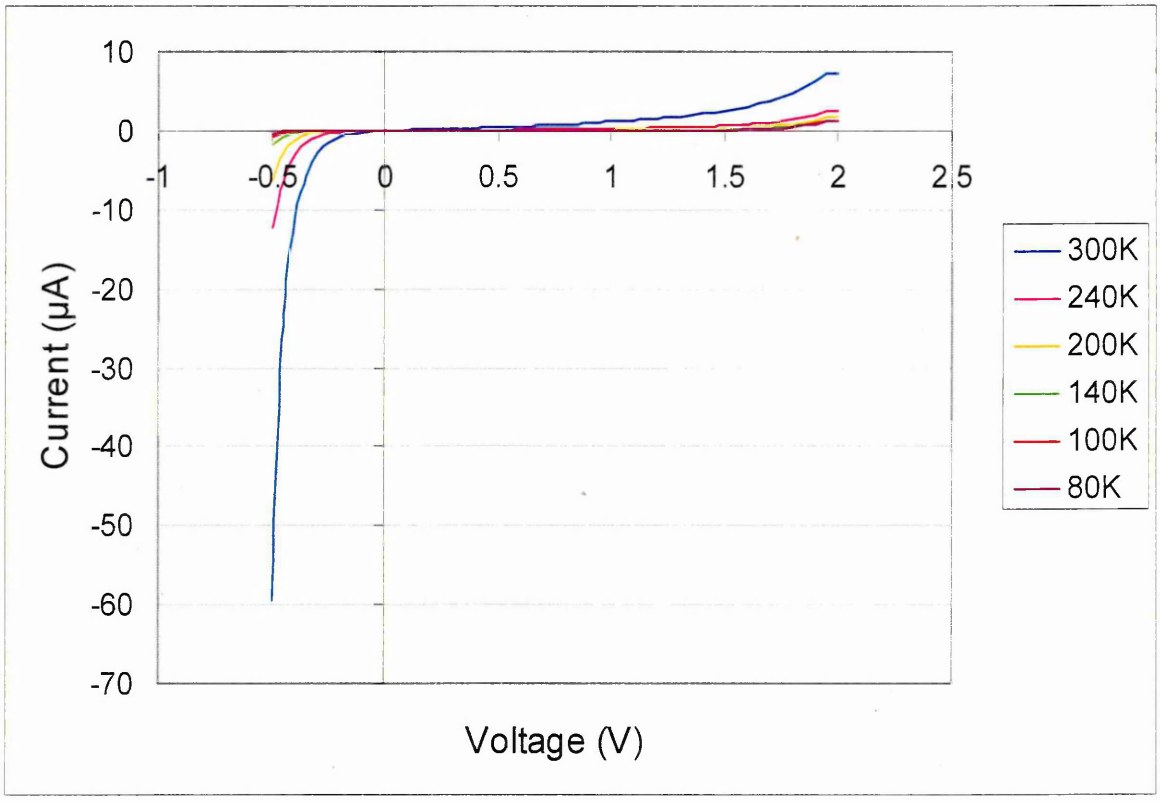


Fig. 6.16: IV measurements of S3 at different temperatures under opposite polarity

From Fig. 6.14 it can be seen that the forward current which is in the order of mA at first, gradually reduces with decreasing temperature as expected. In addition it rises abruptly with increasing forward bias. The reverse current is shown for four temperatures on a bigger scale in Fig. 6.15. It can be seen that this leakage current exhibits an abnormal behaviour. It has a magnitude of 15μA at room temperature then at

200K is shown to be much larger and below this temperature is starts reducing again as it should be the case when the temperature reduces. The reason for the sudden increase of the reverse current in Fig. 6.15 between 300-200K is not clear but it can be suggested that until that temperature the potential barrier that still exists in the n-n$^-$ depletion region prevents the flow of electrons in the diode. At 200K the potential barrier, of 0.14eV from Fig. 6.9, may have been flattened with the applied bias, since the n-n$^-$ depletion region is forward biased, and this junction is now conducting. Subsequently, it starts to gradually decrease as the temperature reduces. The breakdown voltage at a reverse current value of 1μA has been plotted against temperature to investigate the breakdown mechanism in this diode and this is shown in Fig. 6.17.

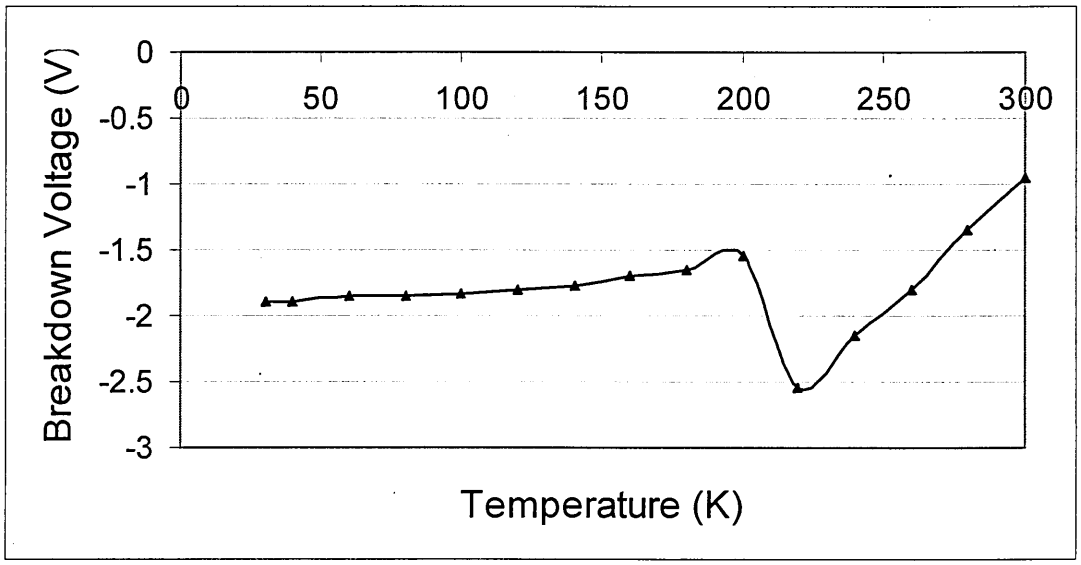


Fig. 6.17: Breakdown voltage of diode S3 at I_R=1μA under normal polarity configuration

It is again obvious that around the temperature of 220K there is a sudden increase in the reverse current. However, the overall tendency of the breakdown voltage to decrease in value with increasing temperature suggests that there is tunnelling in this diode and in addition it has been shown that the p-side is degenerate. In the normal polarity set-up, when the p^+n junction is reverse-biased, the bottom of the conduction band on the n-side is facing the top of the valence band on the p-side. It may be proposed therefore that it is easy for electrons to tunnel through the depletion region, which explains the breakdown characteristic of Fig. 6.17.

The IV results of Fig. 6.16 exhibit a very rapidly reducing reverse current but a very slow exponential rise in the forward current. Although the reverse current at room temperature is increasing very quickly with bias and measurements were performed

with a maximum of -0.5V to avoid breakdown, the leakage current is of the order of μA so the diode could not suffer irreversible damage. The forward current has a lot smaller value than in the normal polarity measurements, rises very slowly with increasing bias and decreases with reduced temperature as is expected for normal diode operation. The reverse current is large at first but also consistently reduces with reducing temperature. In the opposite polarity when the p^+n junction is forward biased the top of the p-side valence band is now below the bottom of the conduction band on the n-side. But since the potential barrier has been considerably lowered, minority carriers (electrons) from the n-side may be injected over the barrier towards the p-side causing an increase to the thermal current. This is a similar situation to the thermionic emission that takes place in heavily-doped forward biased Schottky diodes. Most importantly however, the junction under reverse bias is now the $n\text{-}n^-$ depletion region. Hence electrons from the bottom of the conduction band on the n-side may be able to tunnel through the junction into the valence band of the n-substrate. The breakdown mechanism in this opposite polarity case was investigated with temperature and this is shown in Fig. 6.18 for a reverse current of 0.12μA.

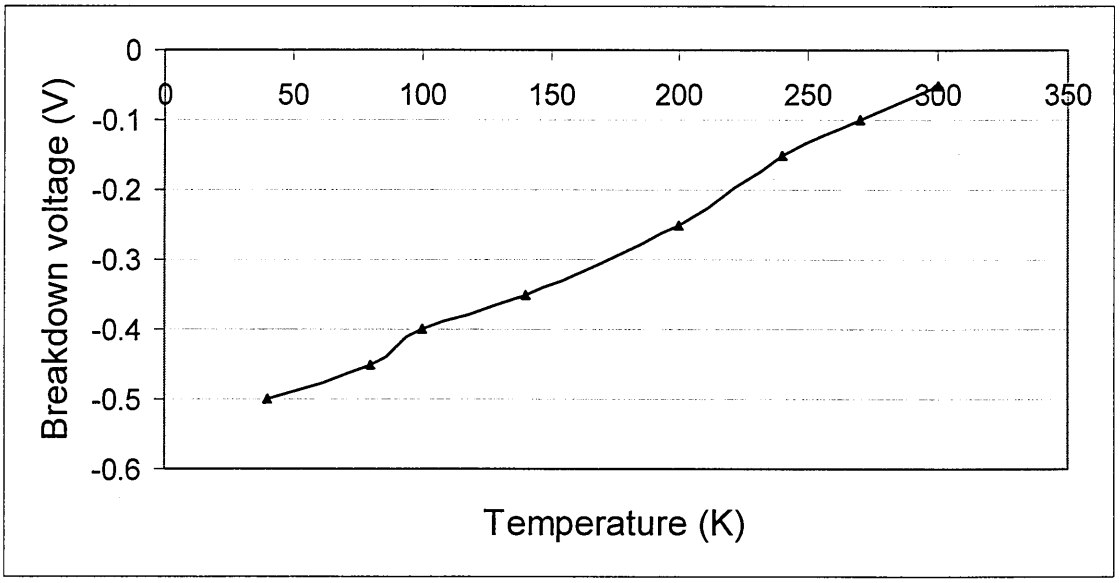


Fig. 6.18: Breakdown voltage with temperature for S3 with opposite polarity at I_R=0.12uA

Once again tunnelling is exhibited by diode S3 in the opposite polarity configuration. In this situation however, it is most likely taking place at the $n\text{-}n^-$ depletion region. The breakdown voltage is again seen to decrease in value with increasing temperature in a consistent manner indicating potential breakdown due to tunnelling. The C-T characteristic of S3 is shown in Fig. 6.19 using -0.5V reverse bias.

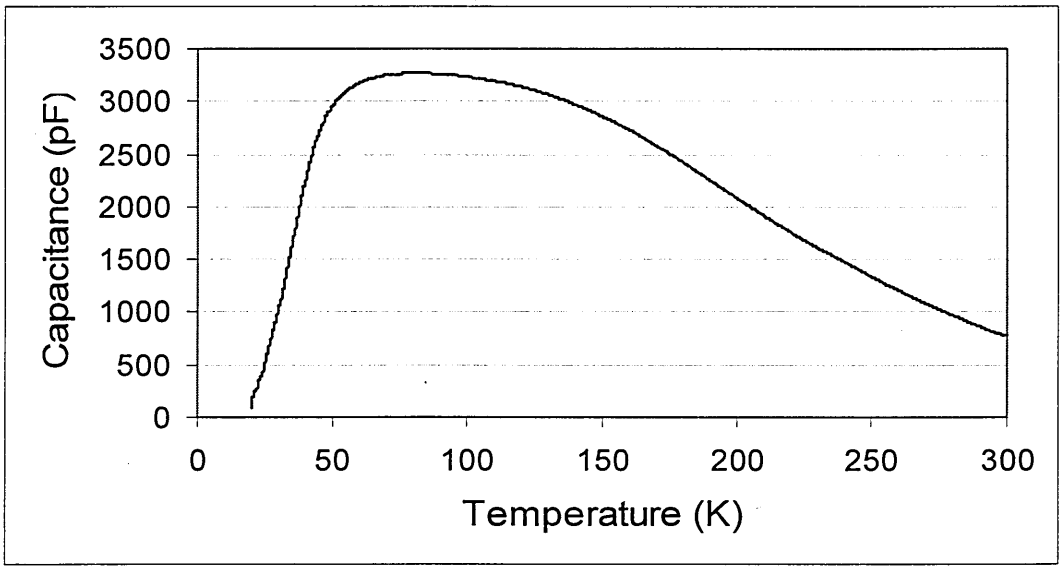


Fig. 6.19: C-T scan of diode S3 from 300K to 20K with 0.5V reverse bias

Fig. 6.19 shows that the capacitance is increasing as the temperature reduces until about 80K, which is contrary to what is expected from a normal diode, as that would suggest that the carrier concentration is also increasing with reduced temperature. The same behaviour was observed in the characteristic for both normal and opposite polarity and is due to the fact that there are two depletion regions with two capacitances in series, as already shown. It is not possible to deconvolute the two capacitances without calculating each separately and this is discussed below.

Returning to equation 6.2 it is worth noticing that since the two depletion regions are in the same sample and have the same cross-sectional area (A) an attempt to find the actual value of each of the capacitances C_1 and C_2 could be useful. The equations that give these capacitances in relation to the depletion region widths are:

$$C_1 = \frac{C_{TOT}(W_1 + W_2)}{W_1} \qquad \text{Eq. 6.4}$$

$$C_2 = \frac{C_{TOT}(W_1 + W_2)}{W_2} \qquad \text{Eq. 6.5}$$

In these equations C_{TOT} is the total capacitance as measured from the CV measurements and the formulae result from the general equation which describes the capacitance as

being inversely proportional to the depletion region width, as stated in chapter 4 and repeated here.

$$C_{TOT} = \frac{\varepsilon_s A}{W} \qquad \text{Eq. 6.6}$$

where ε_s is the permittivity of Si equal to $1.053*10^{-12}$F/cm. Finally the depletion region width for each junction with applied bias is:

$$W = \sqrt{\frac{2\varepsilon_S (V_{bi} - V_R)}{qN_D}} \qquad \text{Eq. 6.7}$$

where, V_{bi} is the built-in voltage of the junction, V_R is the applied bias and N_D is the carrier concentration of the less highly doped side of the depletion region. After the width of each depletion region is found, the value is substituted back into equations 6.4 or 6.5 to find the exact value of each capacitance. Calculations like these were performed for this sample at room temperature. Since the carrier concentration values, measured by CV, were due to the series capacitance, values that more closely matched the SIMS profile were used to find the depletion region widths. The built-in voltage required in Eq. 6.7 was found from Eq. 6.3. The following set of tables show the calculated results for different biasing conditions, for both polarities and showing the concentrations used to find W_1 and W_2 and C_1 and C_2 while the total capacitance is as measured from the CV experiments.

Diode S3 Normal polarity

V_{bi} = 1.017V at Junction 1, V_{bi} = 0.73V at Junction 2
with $p^+=3*10^{19}cm^{-3}$, $n=1*10^{18}cm^{-3}$ and $n^-=3.9*10^{14}cm^{-3}$

	300K				
Bias (V)	W_1 (nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{tot} (nF)
0.3	42	1.2	28	0.977	0.944
0.4	43	1	21	0.93	0.89
0.5	45	0.88	16	0.81	0.77
0.7	47	0.3	0.14	0.02	0.02

Diode S3 Opposite polarity

V_{bi} = 1.03V at Junction 1 and V_{bi} = 0.74V at Junction 2
with $p^+=3*10^{19}cm^{-3}$, $n = 2*10^{18}cm^{-3}$ and $n^-=3.9*10^{14}cm^{-3}$

	300K				
Bias (V)	W_1 (nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{tot} (nF)
0.3	22	1.87	88	1.037	1.0255
0.4	20	1.96	101	1.039	1.029
0.5	18	2	116	1.041	1.0317
0.7	15	2.2	153	1.04	1.033
0.9	9	2.4	275	1.035	1.031
1	4	2.4	618	1.03	1.0294

Table 6.1: Calculations of depletion region widths and capacitances for diode S3 both with normal and opposite polarity configurations. C_{tot} is measured from the CV experiments

These calculations were limited by the built-in voltage of the forward biased junction depending on the polarity. In the normal polarity case at 300K W_2 is decreasing but its respective capacitance C_2 is also decreasing with bias which is the opposite from what equation 6.5 dictates. However, this is due to the rapid decrease of the total capacitance value. The ultra-shallow junction capacitance C_1 has a very large value due to the high doping and the small depletion width with both normal and opposite polarities. The closest the two capacitances can reach is during normal polarity at the maximum forward bias (0.7V) of the n-n^- depletion region. It is then seen that C_1 is only 7 times larger than C_2 while for any other bias their difference is much larger. As C_2 is the smaller capacitance, due to its large width, the general conclusion of all these calculations is that the system is mostly measuring this capacitance. This result confirms that the smaller capacitance dominates the measurements although a contribution from both capacitances is always present.

DLTS was performed for this sample with both normal and opposite polarity for different reverse bias values and fill pulses. The results shown here are the most representative of this diode. Fig. 6.20 shows DLTS plots with reverse bias -0.7V and fill pulse 1V measured in the normal polarity configuration. The DLTS spectra looked the same as the one shown in Fig. 6.20 even for a positive fill pulse lower than 0.7V. The spectra of Fig. 6.20 were taken at a rate window of $50s^{-1}$.

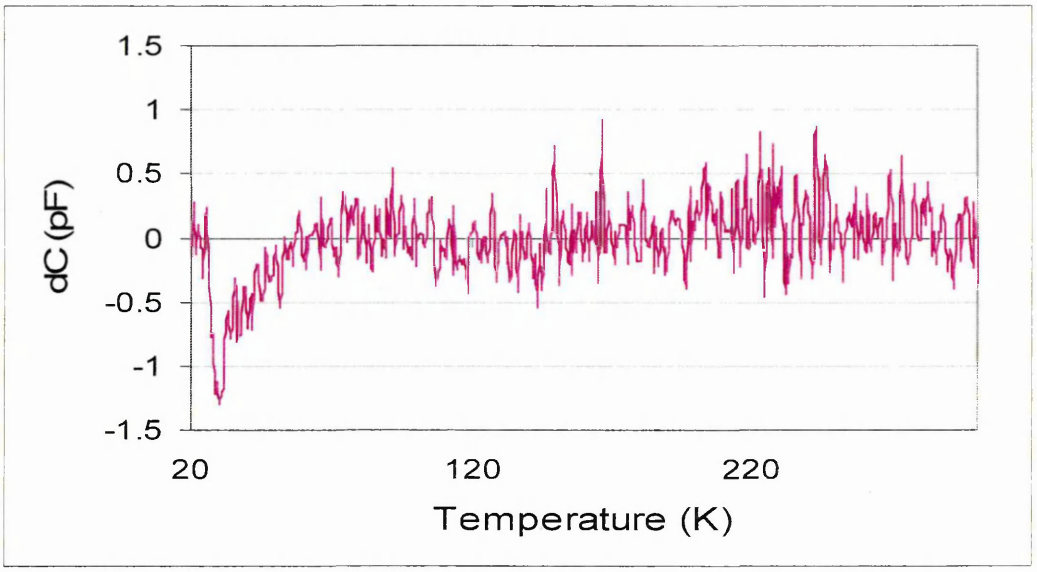


Fig. 6.20: DLTS spectra of diode S3 with rate window $50s^{-1}$, reverse bias -0.7V and fill pulse 1V under normal polarity conditions

Despite the heavy doping on the n-side there appears to be only a minority carrier trap (hole trap), due to a negative capacitance transient, at about 30K. Many different biasing conditions were used to confirm this result, including applying a smaller fill pulse of 0.5V that would normally expose majority carrier traps, if present. The peak of the trap does not shift to lower temperatures for reduced rate windows but follows the opposite pattern. This is an indication that it may not be from a point defect. Fig. 6.21 shows the DLTS spectrum of the same diode with opposite polarity, reverse bias -2V and fill pulse 1V and for the same rate window of $50s^{-1}$.

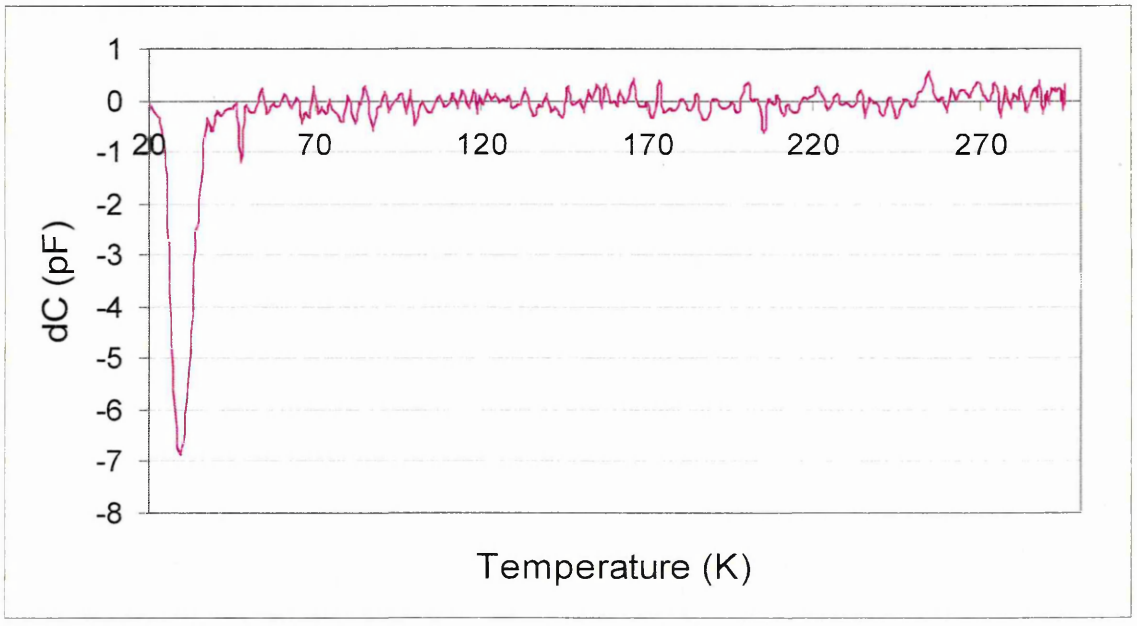


Fig. 6.21: DLTS spectrum of S3 under opposite polarity, reverse bias -2V, fill pulse 1V and at rate window $50s^{-1}$

Scans with larger fill pulse of 2V and also a negative fill pulse -1V, produced the same result. Fig. 6.21 shows the same minority (hole) trap as the one obtained with normal polarity only that with the opposite polarity setting, the signal is much larger and well defined and hence less noisy. No other traps are detected. In addition it should be mentioned that the peak of this trap in this case does move to lower temperatures for lower rate windows as should be the case for a point defect. Therefore, although this sample is very highly doped it does not seem to contain any electron traps but only a hole trap. However, if the above analysis and calculations for this sample are taken into account, this hole-trap is actually in the $n\text{-}n^-$ depletion region under opposite polarity measurements. The presence of a hole trap at this low temperature is not expected since most carriers will not be ionised. It may be suggested that as the doping-well in these USJ diodes is generally highly doped, perhaps there is carrier confinement at the p^+n junction, resulting in a triangular well similar to that of a quantum well.

LDLTS was also performed on these minority traps to obtain more accurate emission rates and investigate the number of traps. Fig. 6.22 shows the LDLTS results for the hole trap at around 30K. The opposite polarity configuration was chosen for this set of measurements as both polarities yield the same result but it is more well-defined with opposite polarity, reverse bias -2V and fill pulse 1V.

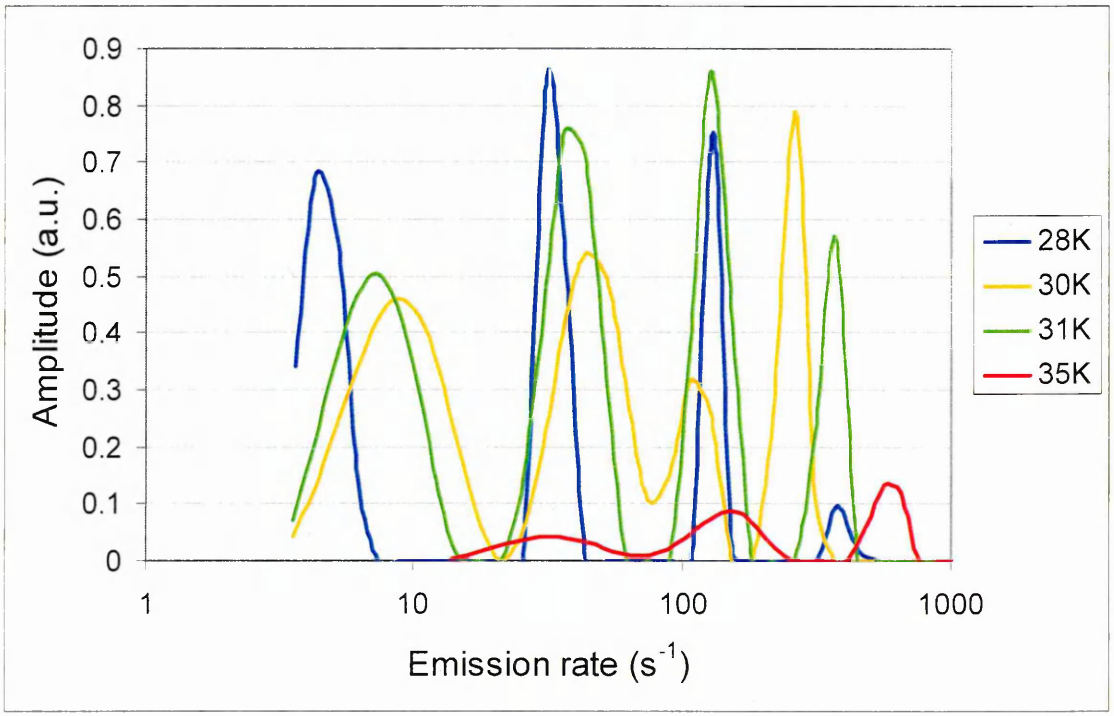


Fig. 6.22: LDLTS spectra of S3 for the hole trap at 30K under the same conditions as the opposite polarity DLTS scan.

The capacitance transients obtained for all of these temperatures were minority carrier trap transients, as expected. As mentioned earlier the emission rate of a trap should increase with temperature for a point defect as it obtains more energy to emit faster at higher temperatures. However, the four, closely spaced in emission, rates observed almost at each temperature, do not increase as the temperature rises in a consistent manner. In addition, they reduce in amplitude or disappear as the temperature increases therefore the observed emission rates are not proof of many hole traps very closely spaced. These however, may be due to carrier confinement due to an energy band discontinuity, similar to a quantum well, as they are very closely spaced in emission. Finally the activation energy for these levels could not be found by taking the emission rate-temperature (e,T) pairs and plotting them in a semi-logarithmic plot of $\ln(e/T^2)$ versus 1/T, as their evolution with temperature was not point defect-like. Although opposite polarity scans in DLTS showed the emission rate of the trap increasing with temperature, this was not observed from LDLTS when the individual emission rates were resolved. Therefore in diode S3, the P implantation did not produce enough damage to yield electron traps, or else due to the complicated diode structure of two capacitances in series, it was not possible to profile the damaged volume with either polarity.

6.4 Diode S4

In this diode the p-side has exactly the same doping as in S3, but the n-side has been implanted with a higher P dose and therefore the implanted n-side has a higher electron concentration. This is about $6*10^{18}cm^{-3}$ according to the SIMS profile. Therefore it is expected that the potential barriers at both the p^+n and $n\text{-}n^-$ interface are higher. Indeed their values are 1.064eV and 0.253eV respectively which means that the p^+n barrier height is comparable to the bandgap even at equilibrium as can be seen from Fig. 6.8. The energy band diagram at equilibrium for diode S4 can be seen in Fig. 6.23. From the band diagram of diode S4 it is obvious that due to the high concentration of the n-side the Fermi level is closer to the conduction band than in S3 and the barrier height of both depletion regions is larger. The p-side is once more degenerate as it has the same B doping as that of S3. In this diode as well, both normal and opposite polarity measurements were possible. The CV and concentration-distance profiles of S4 are shown in Fig. 6.24 for the normal polarity configuration and the corresponding CV and N-x profiles with opposite polarity are shown in Fig. 6.25.

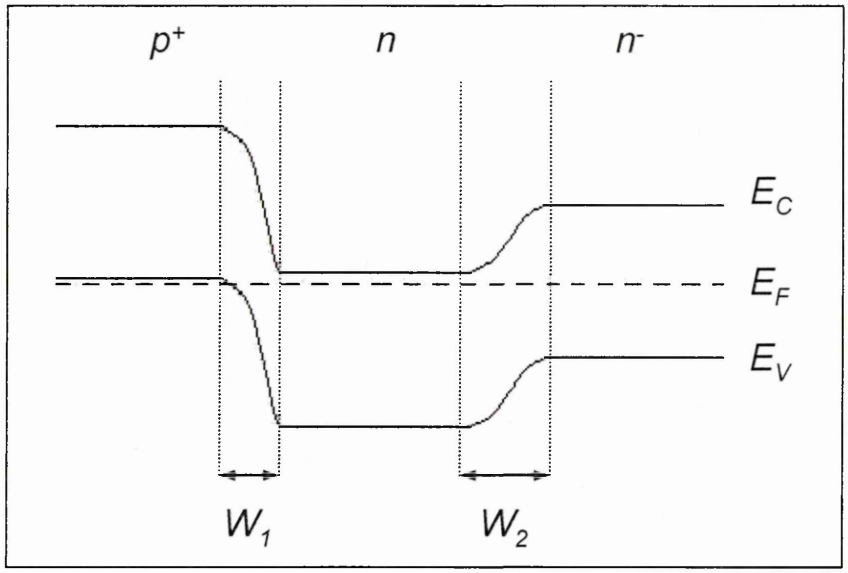
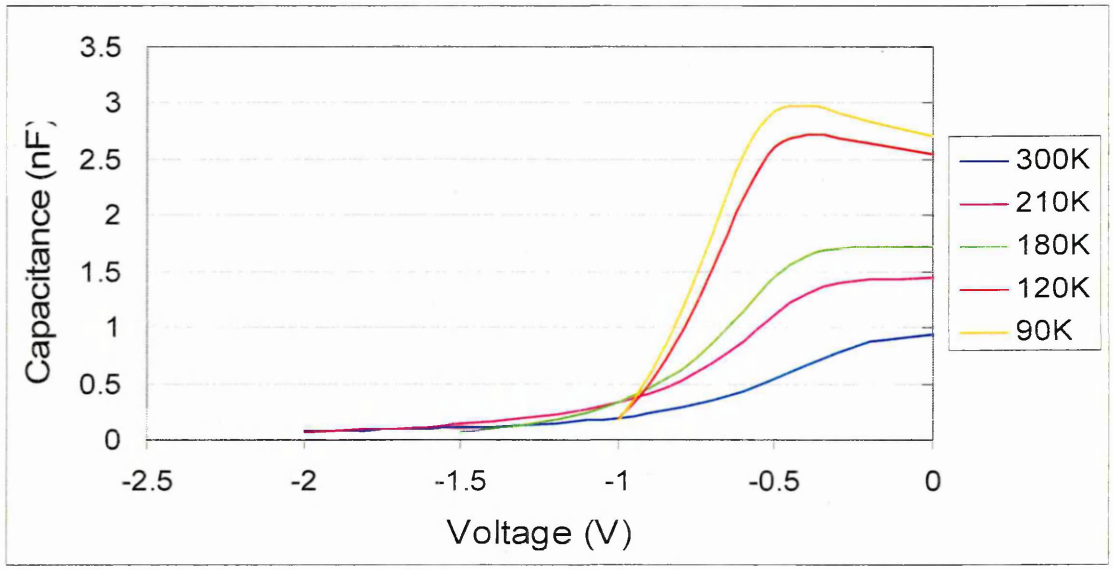


Fig. 6.23: Equilibrium band diagram of diode S4 (not to scale)



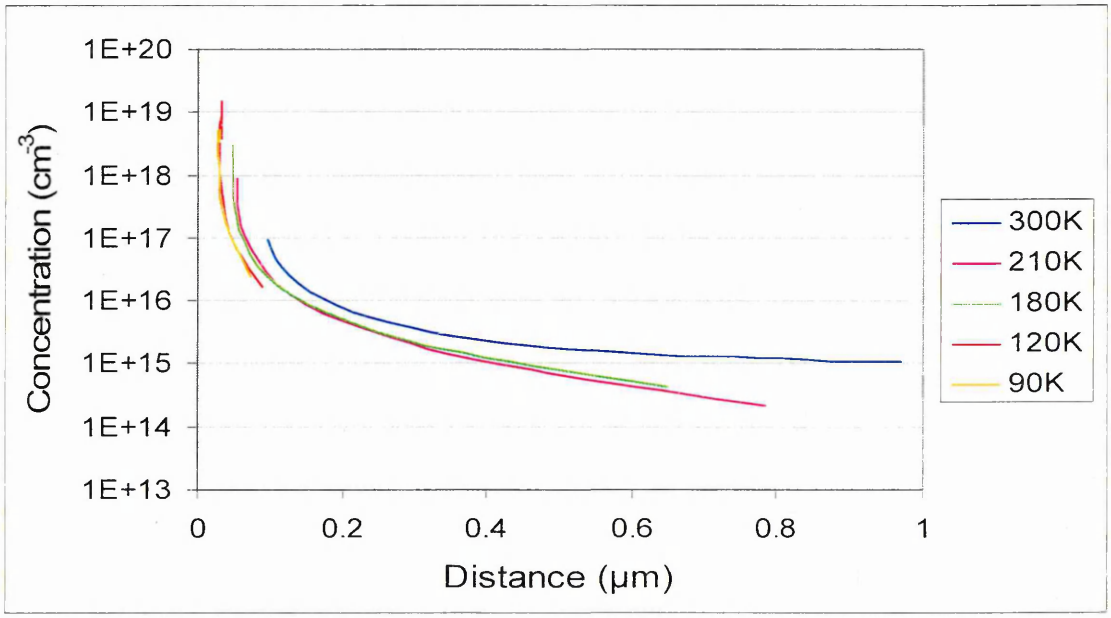


Fig. 6.24: CV and N-x profiles of diode S4 at different temperatures under normal polarity

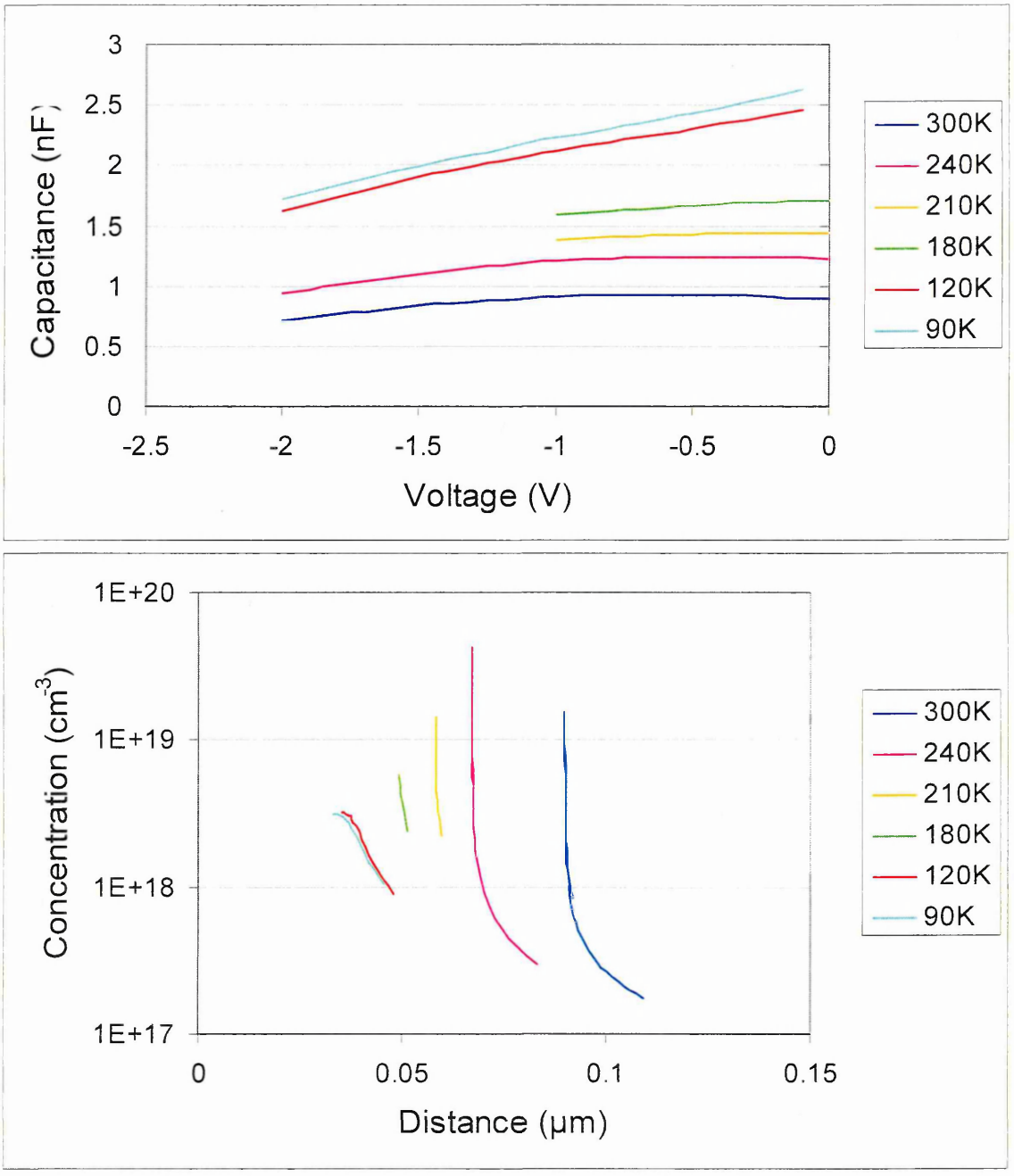


Fig. 6.25: CV and N-x profiles of diode S4 at different temperatures under opposite polarity

The normal polarity CV characteristics resemble those of diode S3 with the capacitance initially almost increasing and then abruptly decreasing with reverse bias. The abrupt decrease however, takes place at a lower reverse bias of ~0.4V but is not as rapid as that of S3. The initial capacitance in the absence of bias is increasing as the temperature decreases, contrary to expected diode-like behaviour. In addition, in this diode the capacitance does not drop to zero at low reverse bias but has a finite value until a bias of -2V except at very low temperatures. The peculiar CV characteristics must once again be attributed to the fact that two capacitances in series are present due to the two depletion regions and the total capacitance is described by Eq. 6.2. This renders the

measurement of each capacitance difficult and makes the result more complicated. The N-x characteristics with normal polarity seem to give a low carrier concentration deeper into the depletion region, which however rises almost exponentially with bias near the interface. A comparison with the SIMS profile value of $6*10^{18}cm^{-3}$ is very difficult as the N-x measurements do not yield one particular carrier concentration. At low reverse bias the carrier concentration is 2-3 orders of magnitude lower than the SIMS profile. However, at higher reverse bias and near the interface, the concentration is more comparable with SIMS. Another point to notice is that the depth scale of the normal polarity characteristics shows that the measurement is profiling a large volume, 100-800nm from the p^+n interface, deeper into the n-side perhaps even down to the substrate at least at low reverse voltage. Hence for DLTS with this polarity it would be better to use a higher reverse bias to examine an area closer to the p^+n interface.

The opposite polarity CV plots of S4 show less bias dependence of the capacitance than the normal polarity data. The capacitance is still very large and once again increasing with reduced temperature, opposite to what expected from a typical diode. The effect of two capacitances is apparent in these characteristics as well, indicating that despite the high reverse bias the p^+n barrier is not flat when this junction is forward biased. The concentration profiles indicate once again an abrupt change with bias, however not as steep as in the normal polarity case. Particularly at high temperatures the concentration rises very rapidly within a very small profiled volume of the depletion region. The junction depth profiled seems to be only ~10nm judging from the volume covered at each temperature. On the contrary the normal polarity N-x scans showed a very broad depletion region profile even though the ultra-shallow junction was reverse biased and the p^+n junction should be profiled. Hence it appears that under normal polarity it is the $n\text{-}n^-$ depletion region that is being profiled and opposite polarity investigates the p^+n depletion region. However, this cannot be verified as the total measured capacitance C_{TOT} reflects the combination of the two depletion region capacitances. Therefore these results were repeated for verification and the same outcome was obtained.

Comparison of the N-x results of either polarity with the SIMS profile that was provided for this diode (Fig. 5.1 red line) is not therefore possible. In the opposite polarity case the profiled depth is between 30 and 110nm from the junction while for normal polarity the covered depth is between 30 and 2400nm. This was not the case for

S3 where it appeared that under both biasing configurations the same depth was being profiled. It is worth observing that in this sample due to the high doping of the n-side one sixth of the p^+n depletion region extends on the p-side and for the same reason at the $n\text{-}n^-$ interface the depletion region is now more in the substrate than in the previous sample.

The CT scan for this diode is shown in Fig. 6.26 where it is seen that the capacitance increases with temperature until about 80K and then decreases. This scan is with opposite polarity as the same result was obtained for normal polarity as well. A similar curve of increasing capacitance for reducing temperature was obtained for S3 where the maximum capacitance was also very large (a few nF).

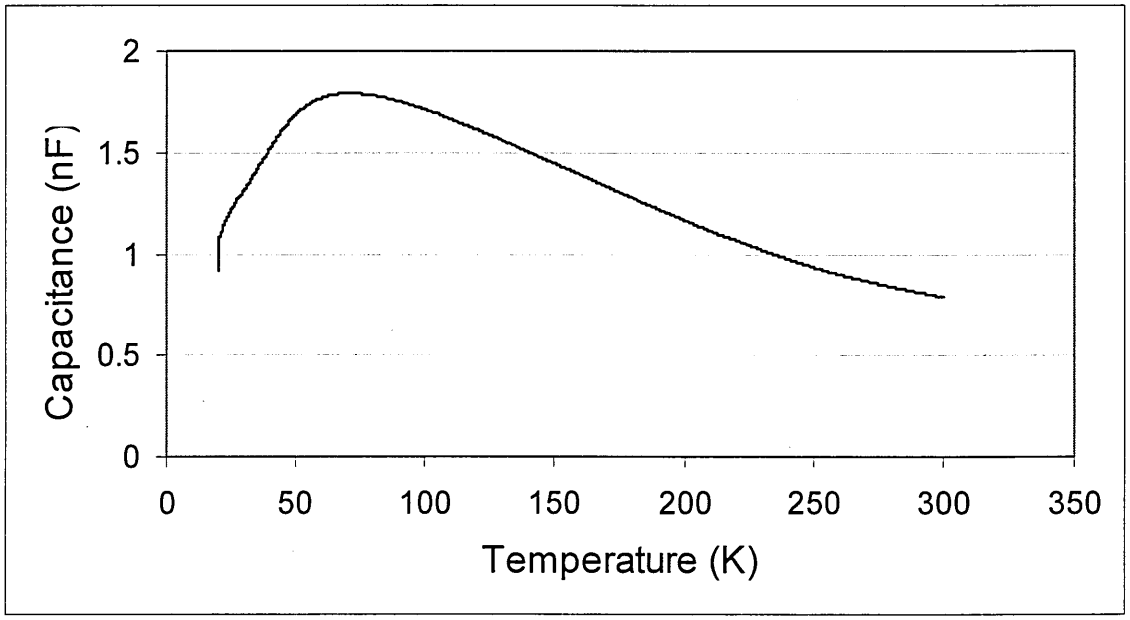


Fig. 6.26: C-T scan of S4 with -2V reverse bias and with opposite polarity

Calculations were performed in an attempt to determine the exact capacitance and depletion width values for both junctions with both polarities. The results are shown in the following table. The concentration used for the n-side was that of the SIMS profile as the N-x profiles were due to a combination of two depletion region capacitances. Therefore the doping content from the SIMS profile of Fig. 5.1 (red line) seems more suitable for these calculations.

Diode S4 Normal Polarity

V_{bi} = 1.063V at Junction 1, V_{bi}= 0.77V at Junction 2,
with $p^+=3*10^{19}cm^{-3}$, $n=6*10^{18}cm^{-3}$ and $n^-=3.9*10^{14}cm^{-3}$.

	300K				
Bias (V)	W_1 (nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{tot} (nF)
0	16.7	1.6	90.7	0.947	0.9377
0.3	19	1.3	54	0.794	0.7821
0.4	19.6	1.11	38	0.674	0.662
0.5	20	0.95	26	0.55	0.54
0.6	21	0.75	16	0.445	0.433
0.7	21.5	0.48	8	0.364	0.3488
1	23		0.36		0.19806
2	28		0.295		0.076383

Diode S4 Opposite Polarity

V_{bi} = 1.063V at Junction 1, V_{bi}= 0.77V at Junction 2,
with $p^+=3*10^{19}cm^{-3}$, $n=6*10^{18}cm^{-3}$ and $n^-=3.9*10^{14}cm^{-3}$.

	300K				
Bias (V)	W_1 (nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{tot} (nF)
0	16.7	1.6	86	0.898	0.88909
0.3	14	1.9	125	0.925	0.91806
0.4	13.2	2	141	0.93	0.92364
0.5	12	2.1	163	0.933	0.92736
0.6	11	2.15	182	0.934	0.92918
0.7	9.7	2.22	213	0.932	0.92846
0.8	8.3	2.3	257	0.928	0.92553
0.9	6.5	2.37	336	0.922	0.91998
1	4	2.44	557	0.913	0.91181

Table 6.2: Calculations of depletion region widths and capacitances for diode S4 both with normal and opposite polarity

For the calculations of W_1 in this sample a more elaborate form of Eq. 6.7 was used and that is because in this diode 1/6 of the depletion region at the p^+n interface extends on the p-side since the carrier concentration of the n-side is much higher. Therefore the concentration of both acceptors N_A and donors N_D should be included in this equation as follows:

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi}-V_R)}{q}\frac{N_D+N_A}{N_D N_A}} \qquad \text{Eq. 6.8}$$

From the above set of tables it can be seen that under normal polarity, W_1 is increasing with bias, since this junction is reverse biased and W_2 is decreasing, as it is forward biased. The opposite occurs for opposite polarity, as expected. From Eq. 6.2 that gives the total capacitance, it is obvious that with opposite polarity the two capacitance values are so different that C_2 is definitely the dominant one, while with normal polarity there may be a contribution from C_1 as well especially at high biases. Therefore the opposite polarity may be used to investigate the traps at the n-n^- depletion region. DLTS with normal polarity may give traps that are on the n-side, if not in the p^+n depletion region, since this junction is in reverse bias.

As the n-side is quite highly doped, the valence band top on the p-side is facing the bottom of the n-side conduction band. Therefore in this sample it is expected that there is even more tunnelling of carriers. In order to investigate this, IV measurements were performed and the results are shown in Fig. 6.27

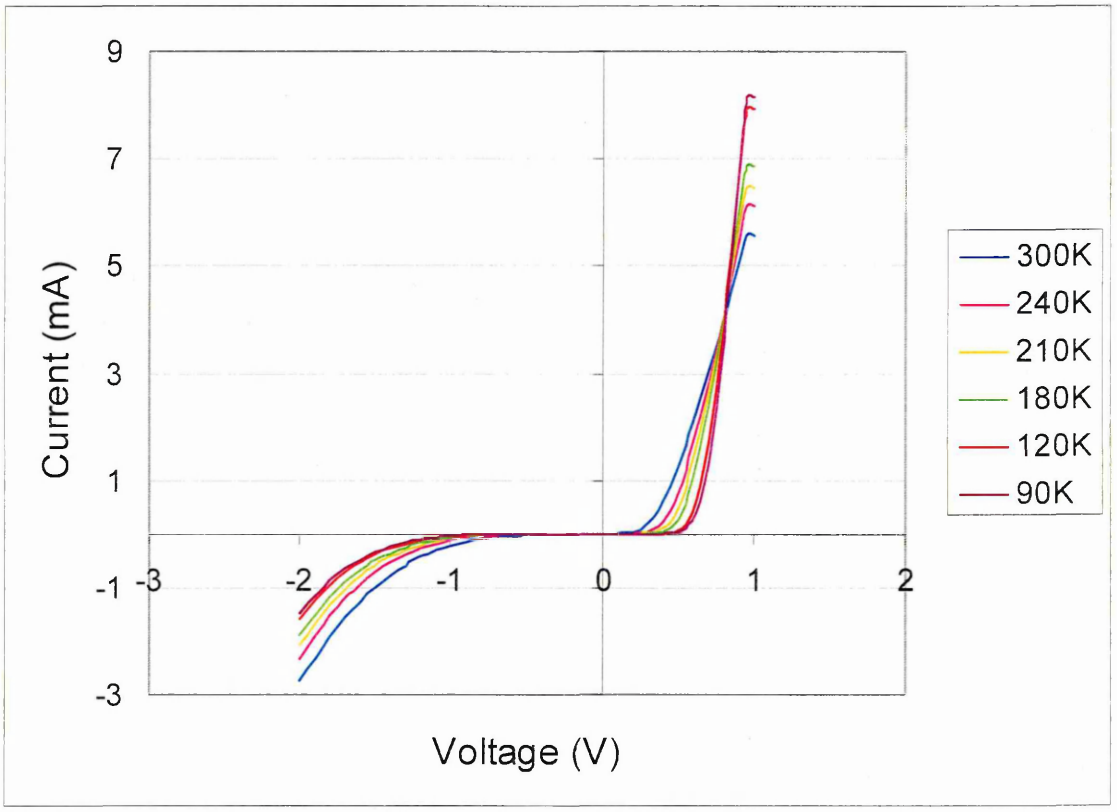


Fig. 6.27: IV plots for S4 at different temperatures under normal polarity.

From these IV curves measured under normal polarity it is obvious that there is a lot of leakage current, which is increasing as the reverse bias is increasing. However, the reverse current reduces as the temperature decreases, indicating that fewer dopants are ionising, as expected. This is opposite to what was taking place in the previous diode

S3. The forward current is also high and contrary to what expected is increasing as the temperature decreases. In S3 with both polarities the forward current was seen to decrease with temperature. To investigate the breakdown mechanism of the diode, the breakdown voltage is plotted against temperature at a reverse current of 1mA and the result is shown in Fig. 6.28. The results indicate that tunnelling is again taking place since the voltage increases in value with decreasing temperature.

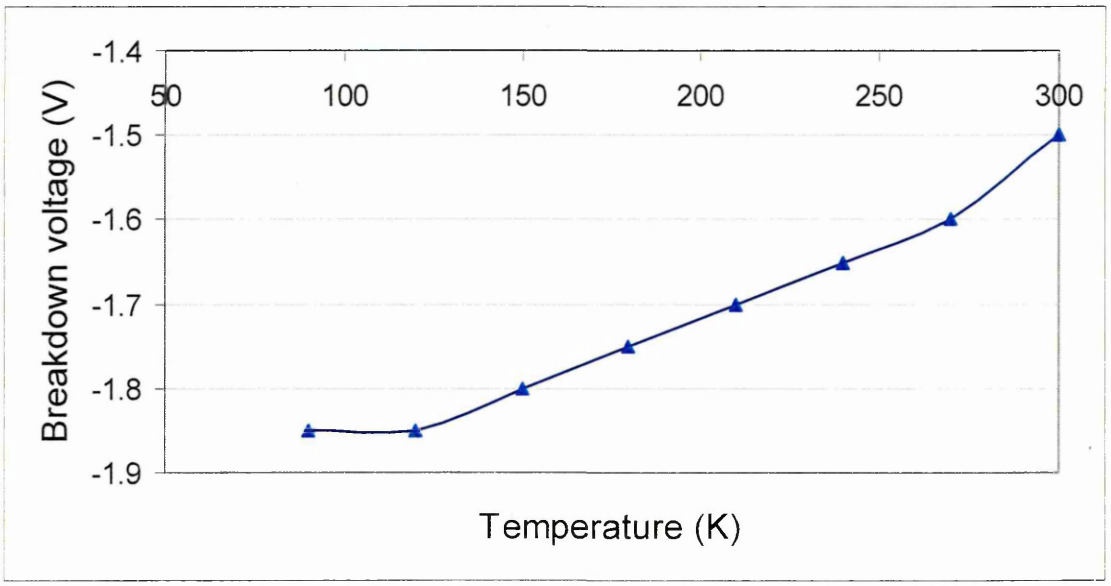


Fig. 6.28: Breakdown voltage with temperature of S4 at 1mA

Opposite polarity IV measurements were also performed and are shown in Fig. 6.29 at different temperatures.

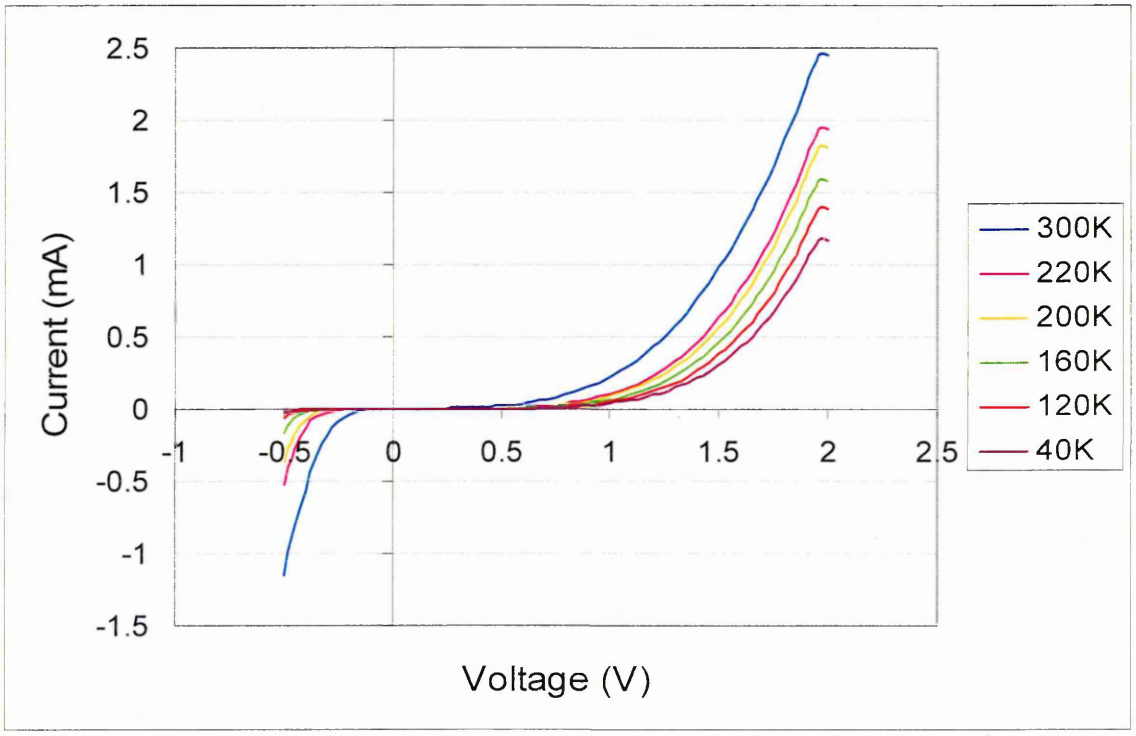


Fig. 6.29: Opposite polarity IV measurements for S4 at different temperatures

In the opposite polarity configuration the forward current is smaller than with normal polarity and consistently reduces as the temperature increases. A similar consistent decrease with temperature occurs for the reverse current. Even though with opposite polarity the p^+n junction is forward biased, it seems that this potential barrier is still present and once more minority carrier injection may be taking place when a large negative bias is applied to the n-side.

DLTS experiments were performed with different reverse bias values and fill pulses and with both polarities. The fill pulse was varied in order to uncover any electron or hole traps present in the depletion region. A positive fill pulse reduces the reverse bias and introduces majority carriers (electrons) in the depletion region, while a negative fill pulse enhances the reverse bias and hence may uncover minority carrier traps (hole traps). In this case of the large reverse bias, the bottom of the conduction band on the n-side should be facing the top of the valence band on the p-side and hence tunnelling may be taking place. Fig. 6.30 shows the DLTS under normal polarity, reverse bias -2V and fill pulse 1V and Fig. 6.31 shows the DLTS with fill pulse -1V at different rate windows.

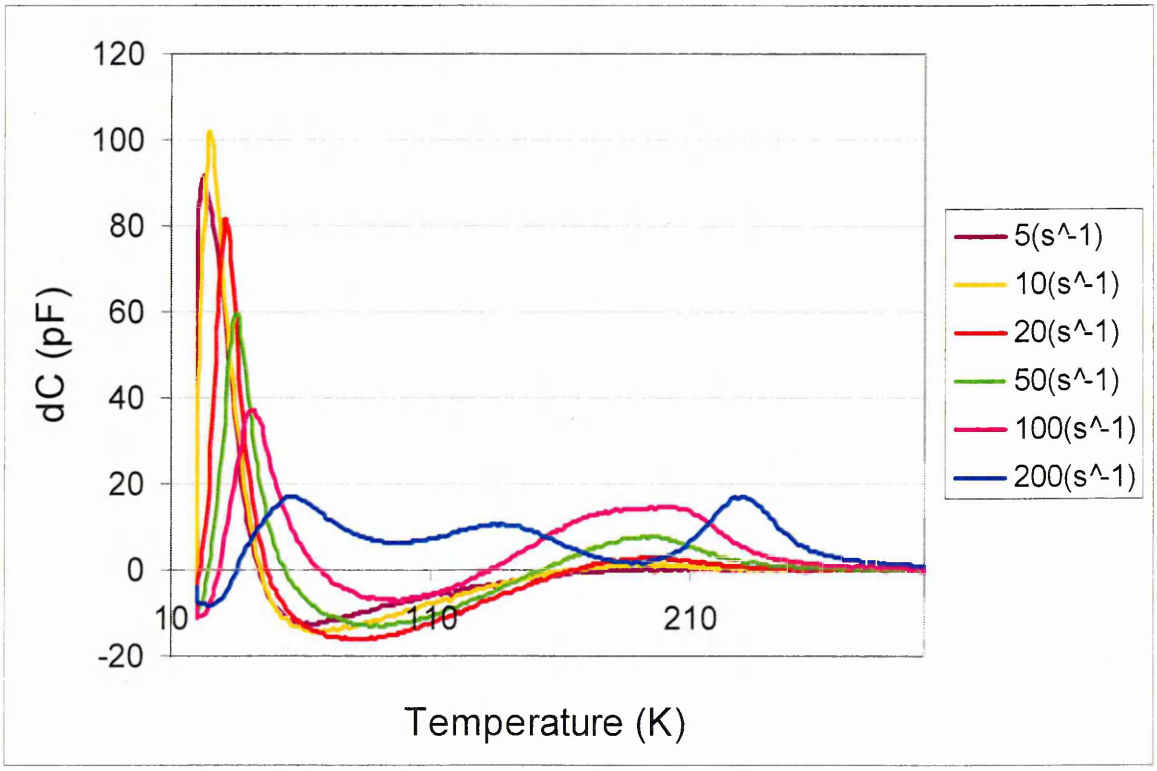


Fig. 6.30: DLTS spectra of S4 with reverse bias -2V and fill pulse 1V

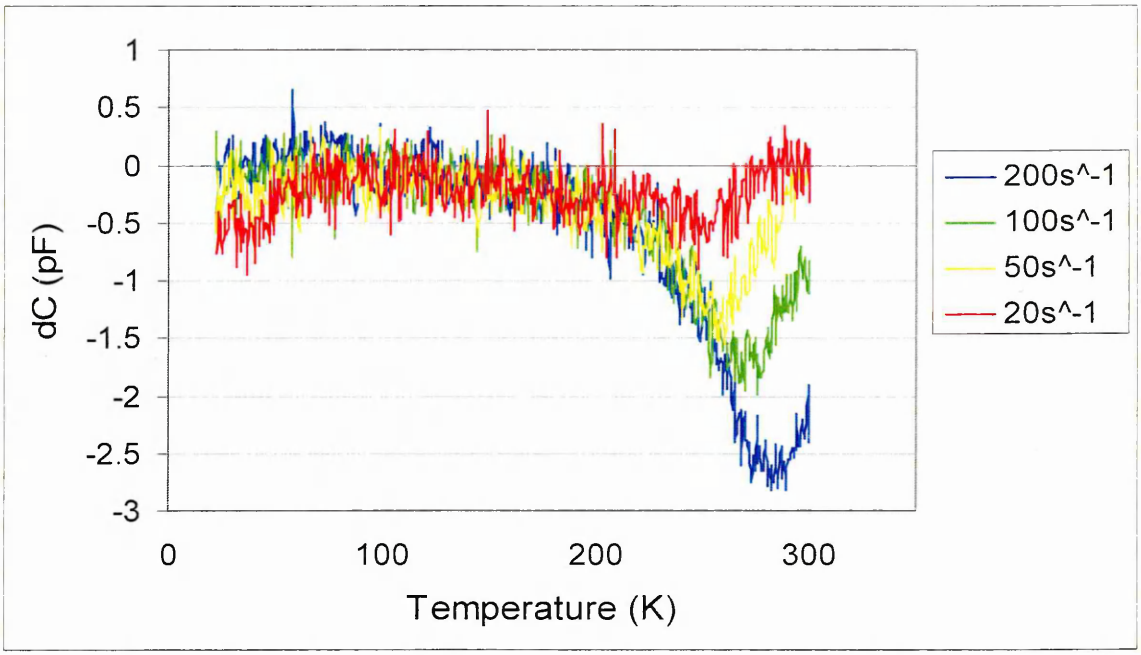


Fig. 6.31: DLTS spectra of S4 with reverse bias -2V and fill pulse -1V

In Fig. 6.30 there are three majority carrier traps in the DLTS spectrum at a rate window of $200s^{-1}$. However, the middle peak reduces and seems to disappear for smaller rate windows. From a closer look though, this peak joins the first peak and at lower rate windows they appear as the same peak. The peak of every trap shifts to lower temperatures with decreasing rate windows as expected since the traps have less energy to emit carriers. It has already been mentioned that this depletion region is about 28nm wide at -2V, of which 4.6nm lies on the p-side. Therefore the detected traps could be either hole traps from the p-side or electron traps from the n-side of the depletion region. However, the N-x characteristics with normal polarity indicated that the volume profiled with bias -2V is about 600nm from the p^+n interface for the high temperature peak. Although these results stem from a combination of capacitances and are not expected to be accurate, they are still an indication that the majority carrier traps are more likely to be due to electron traps. The activation energy of the high temperature majority trap in the DLTS spectra was calculated from the Arrhenius plot of Fig. 6.32.

The Arrhenius plot yielded an activation energy of 0.22eV which could be due to implantation damage, as it is close in energy to the doubly negative charge state of the divacancy, although it is found at a higher temperature than usual [1]. This may be due to the fact that the high temperature DLTS peak at lower rate windows than $200s^{-1}$ contains a contribution from the middle temperature peak. The presence of the low temperature, large peak at about 50K has a very low activation energy of 0.01eV, which

cannot be accurate due to the error margin of ± 50meV in DLTS. In addition, it is found far below the usual temperature of the very common A-centre, which is typically 0.17eV. Hence its origin cannot be adequately determined from DLTS. However, it should be mentioned that it resulted from a majority capacitance transient.

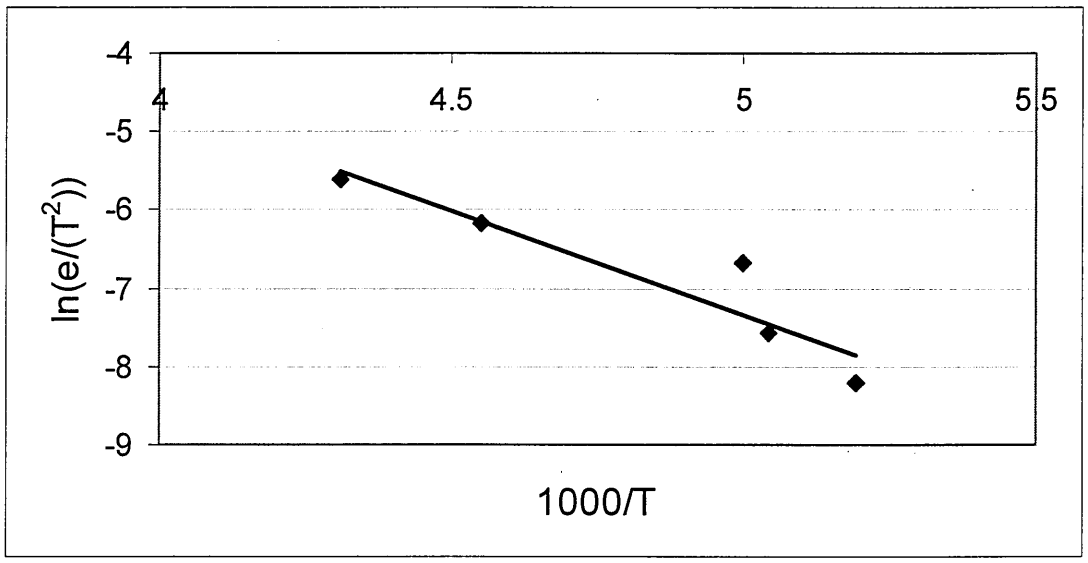


Fig. 6.32: Arrhenius plot of the high temperature DLTS peak with normal polarity, reverse bias -2V and fill pulse 1V

When a fill pulse of -1V is applied with normal polarity a minority trap around 270K is revealed as seen from Fig. 6.31. The peak is shifted to lower temperatures for lower rate windows and the activation energy for this trap was found to be 0.68eV. The Arrhenius plot for this trap is shown in Fig. 6.33.

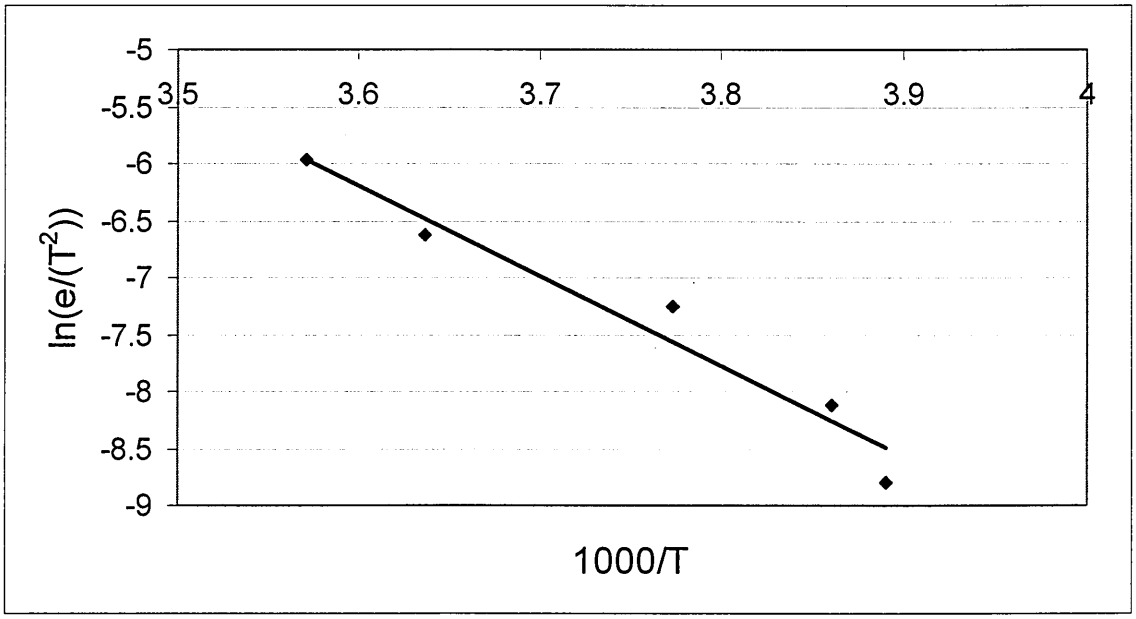


Fig. 6.33: Arrhenius plot for minority trap obtained with normal polarity, reverse bias -2V and fill pulse -1V

This trap is a minority carrier trap on the DLTS spectrum. However, a complicated situation arises due to its large activation energy. If the n-side is profiled at this bias, then this trap must correspond to a hole trap due to B implantation damage. Given its large activation energy (0.68eV) however, it is actually located at 0.44eV below the conduction band on the n-side. This coincides in energy with the value of the E-centre due to the phosphorus-vacancy or the singly negative charge state of the divacancy [2-4]. On the other hand observation of the biasing conditions that revealed this trap, indicates that the p^+n depletion region is under a large reverse bias. In addition, as already mentioned one sixth of this junction lies on the p-side. Hence the bottom of the conduction band on the n-side is adjacent to the valence band on the p-side and there is certainly tunnelling, as already shown. Hence electrons from the n-side can be tunnelling either to the valence band or most likely directly to levels in the bandgap on the p-side. The negative fill pulse applied to obtain this trap from Eq. 6.8 causes this depletion region to widen with a value of 32nm, 5.3nm of which lies on the p-side. Therefore if the p-side is being profiled, this minority carrier trap is an electron trap located at 0.68eV below the conduction band. A similar energy level has been reported in p-type Si as an interstitial complex that embodies B at 0.45eV above the valence band [1]. This discussion about the origin of this trap may be resolved depending on the LDLTS spectra that will be shown shortly for this trap. This depends on whether point defect-like or complex emission spectrum is obtained from LDLTS.

DLTS with opposite polarity was also performed on S4. Fig. 6.34 shows the DLTS spectra measured with opposite polarity, reverse bias -2V and fill pulse 1.5V for two rate windows. Fig. 6.34 shows that DLTS revealed three small majority traps. In the opposite polarity configuration, the $n\text{-}n^-$ depletion region should be reverse biased while the p^+n depletion region is forward biased, though the potential barrier is not entirely flat. Hence the volume scanned should be near the $n\text{-}n^-$ interface where implantation damage due to P may be observed. Hence the three majority carrier peaks should be ascribed to electron traps. Their signal is quite small and noisy but 4 necessary rate window measurements were successfully performed. Activation energy calculations were hence attempted at least for the two higher temperature peaks. The Arrhenius plots for these two traps are shown in Fig. 6.35.

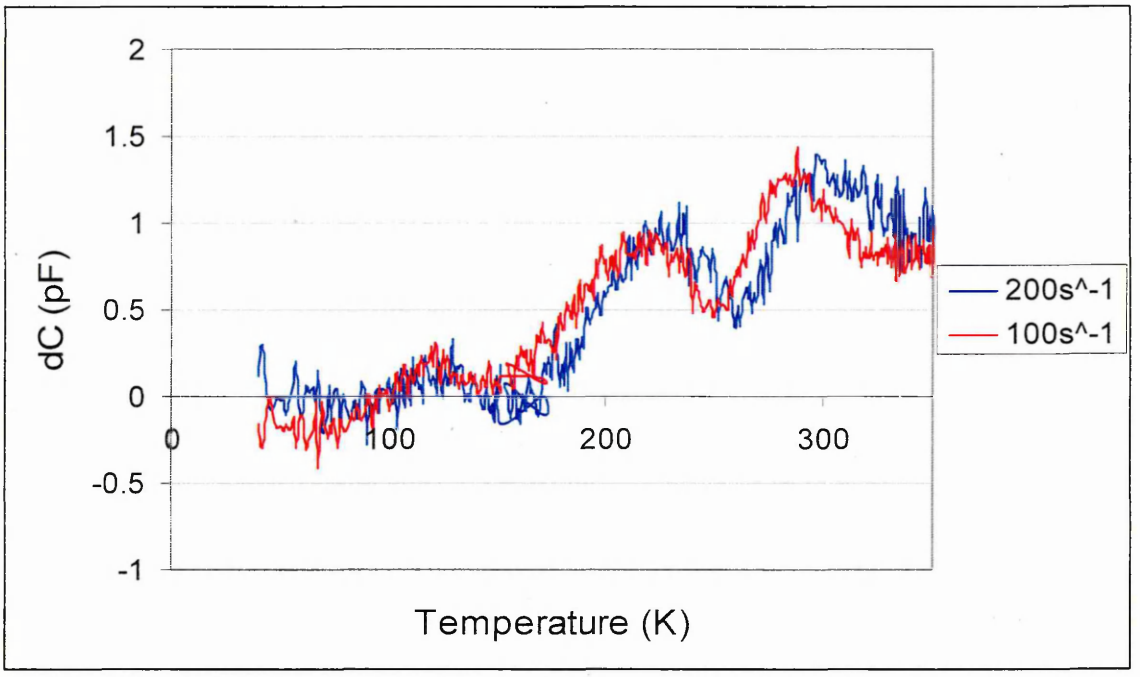


Fig. 6.34: DLTS of S4 with opposite polarity, reverse bias -2V, fill pulse 1.5V at rate windows 200 and 100s^{-1}.

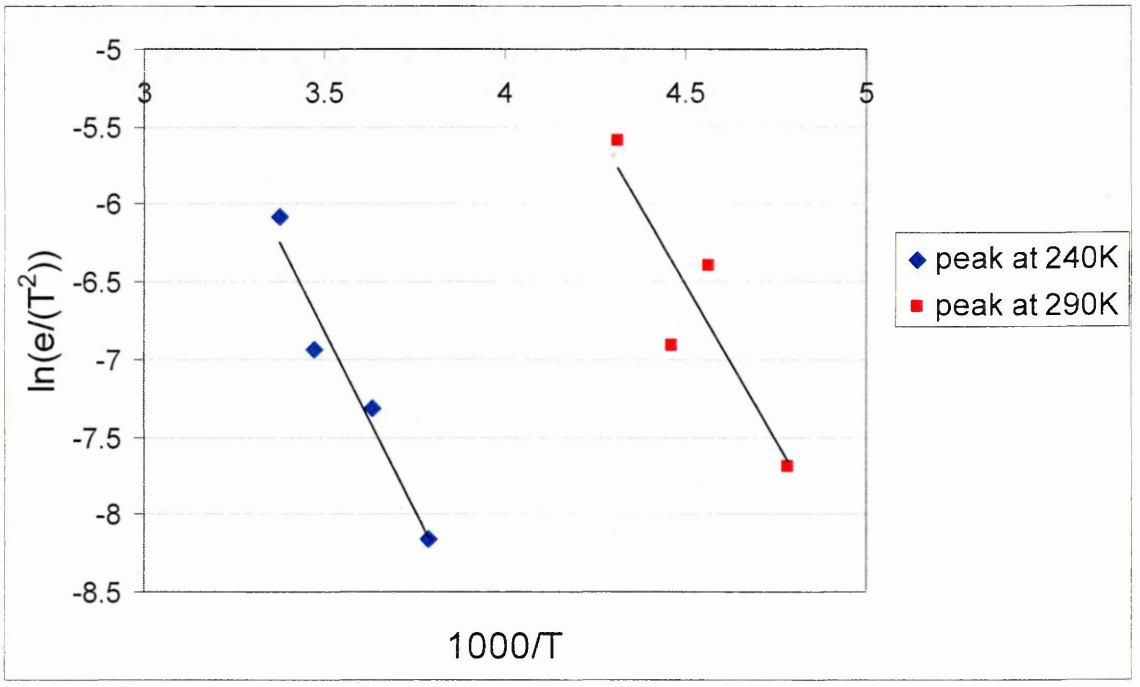


Fig. 6.35: Arrhenius plots for the two higher temperature peaks of DLTS of diode S4 with opposite polarity.

The high temperature peak yielded an activation energy of 0.4eV and 0.34eV was found for the peak at 240K. As these defects are located on the n-side then the former may be due to the singly negative divacancy overlapping with the VP centre and the latter due to a carbon substitutional related defect [2, 3].

Finally LDLTS was performed for the defects measured under normal polarity, as their location and origin was harder to resolve. LDLTS results will be displayed in 3-D view where necessary, in order to facilitate comparison and comprehension in the remaining of this and in the following chapters, otherwise the results will be displayed in 2-D format. Fig. 6.30 indicated the presence of three majority carrier traps with reverse bias -2V and fill pulse 1V. Fig. 6.36 shows the LDLTS of the low temperature large peak at 50K. It consists of one or two emission rates at each temperature which however do not change consistently with temperature. When the temperature increases from 35K to 40K the peak emission decreases indicating that this is not a point defect. Hence its activation energy from LDLTS could not be determined and calculation from the Arrhenius plot in DLTS yielded a very low value compared to the error margin of DLTS.

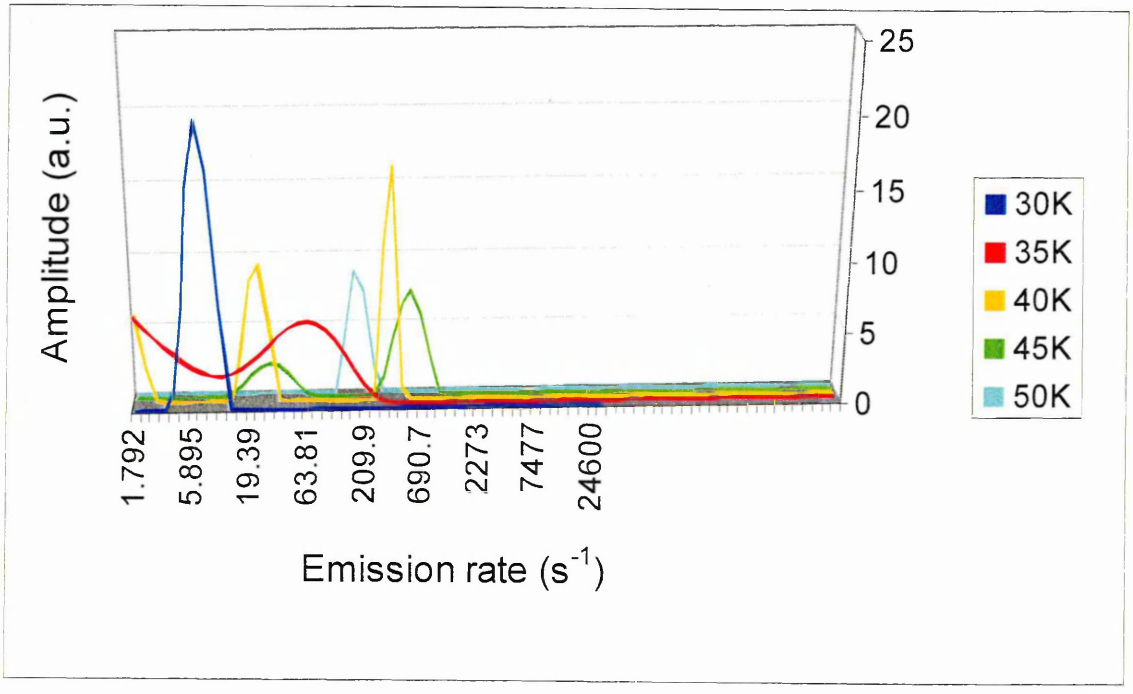


Fig. 6.36: LDLTS spectra for low temperature peak of Fig. 6.30 with normal polarity, reverse bias -2V and fill pulse 1V

LDLTS was also performed for the high temperature peak of Fig. 6.30 at several temperatures that the trap covered as this level could be due to two defects that appeared merged at lower rate windows. Fig. 6.37 shows a selection of the LDLTS spectra for clarity as a total of fifteen measurements were performed. The LDLTS spectra confirm that two emission rates are present at each temperature. In addition, the emission rate increases as the temperature increases. Therefore the activation energy of these defects can be calculated and it is likely that these emissions are due to point defects. The level

with an emission rate of $200s^{-1}$ was found to have an activation energy of 0.1eV while the activation energy of the lower emission rate defect is 0.2eV. It is worth mentioning here that DLTS was only able to detect the low emission rate and yielded an activation energy of 0.22eV which is quite similar to that obtained from LDLTS. However, the latter technique was able to resolve the presence of two separate levels.

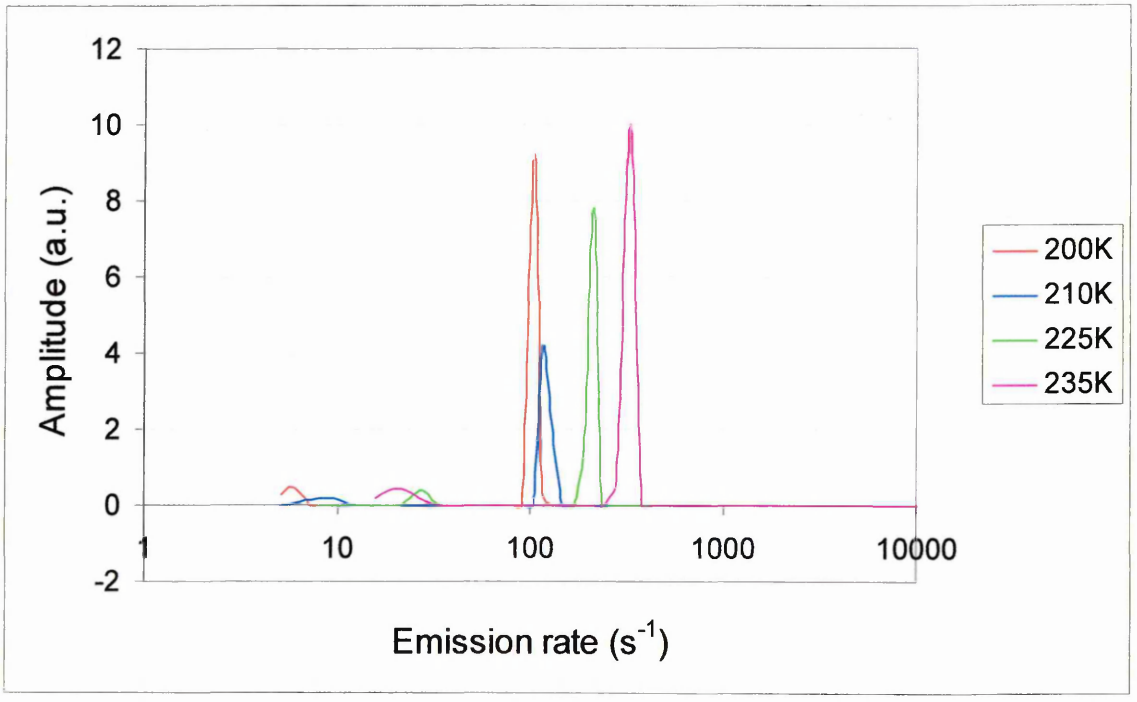


Fig. 6.37: LDLTS spectra of the high temperature peak of Fig. 6.30 for diode S4 with normal polarity, reverse bias -2V and fill pulse 1V

The minority carrier trap obtained from normal polarity with reverse bias -2V and fill pulse -1V was also studied with LDLTS in order to attempt identification of the origin of the defect and also determine whether it is located on the p- or n-side. LDLTS scans were performed over a wide range of temperatures from 250K-290K in steps of 5K. A selection of these results is shown in Fig. 6.38, for clarity. LDLTS yielded a minority capacitance transient for all the examined temperatures, as expected. There is one emission rate detected at all temperature scans, centred at around $4000s^{-1}$. As the emission rate does not change with temperature it is concluded that this level is not a point defect, otherwise a consistent increase in emission rate would be observed with increasing temperature. Therefore this level could be due to a cluster of defects. It is postulated that this level is due to an interstitial complex that embodies B located on the p-side of the $p^{+}n$ junction and at 0.45eV above the valence band, as indicated from DLTS.

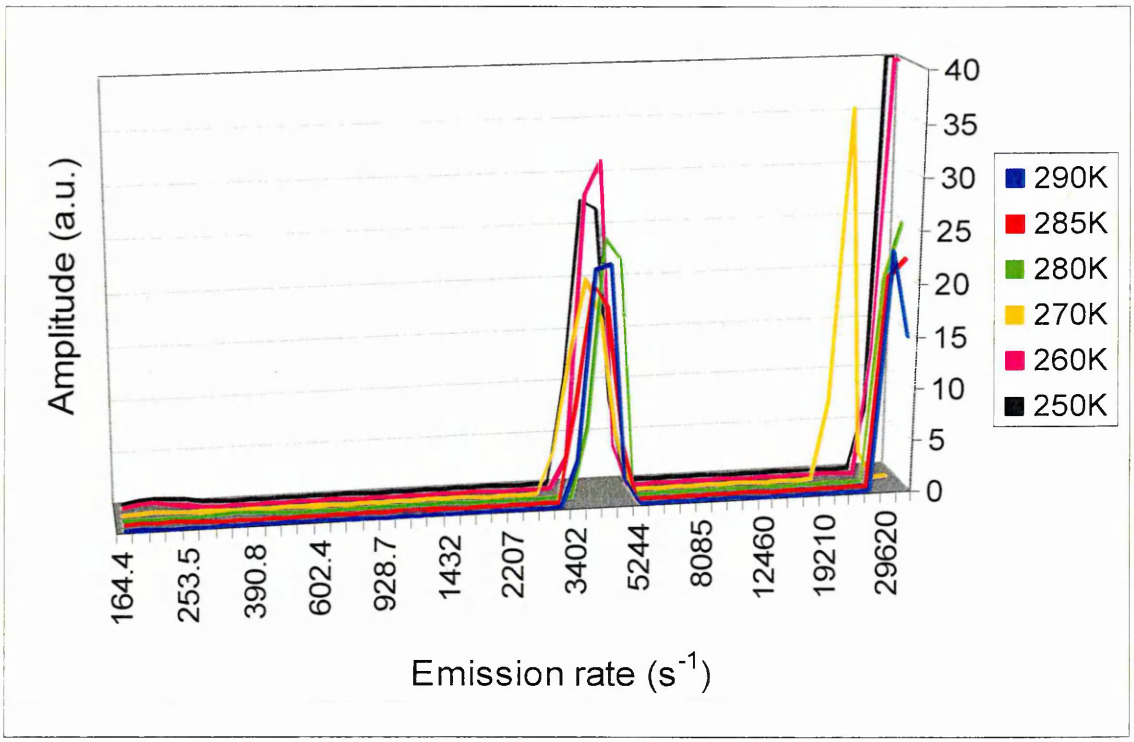


Fig. 6.38: LDLTS spectra for diode S4 corresponding to the DLTS minority peak of Fig. 6.31 obtained with normal polarity, reverse bias -2V and fill pulse -1V

6.5 Diode S5

Diode S5 has been implanted with both P and As but at half the B implantation energy of the previous two diodes. In addition, the implantation dose of both As and P is even lower than that of diode S3 hence it is expected that the doped n-side is not as heavily doped as in the previous diodes. Furthermore, from the SIMS profile of Fig. 5.2 it is seen that the B concentration is a bit lower for this diode. Finally, it should be mentioned that for this diode opposite polarity CV, N-x and IV measurements were not possible and did not yield meaningful results which indicates that the diode is working most efficiently with normal polarity. Suggestions for this will be given after the results have been presented. The CV and N-x results obtained for S5 are shown in Fig. 6.39.

The CV characteristics show that in this diode the total capacitance measured is smaller than in the previous diodes although still in the order of about 1nF. The capacitance is increasing when the temperature is decreasing but less rapidly. The shape of the characteristics is that of a normal p-n diode reducing with increased reverse bias. This indicates that the total capacitance is affected less by the contribution of the n-n$^-$ depletion region, which is to be expected since the n-side is much less doped in this diode.

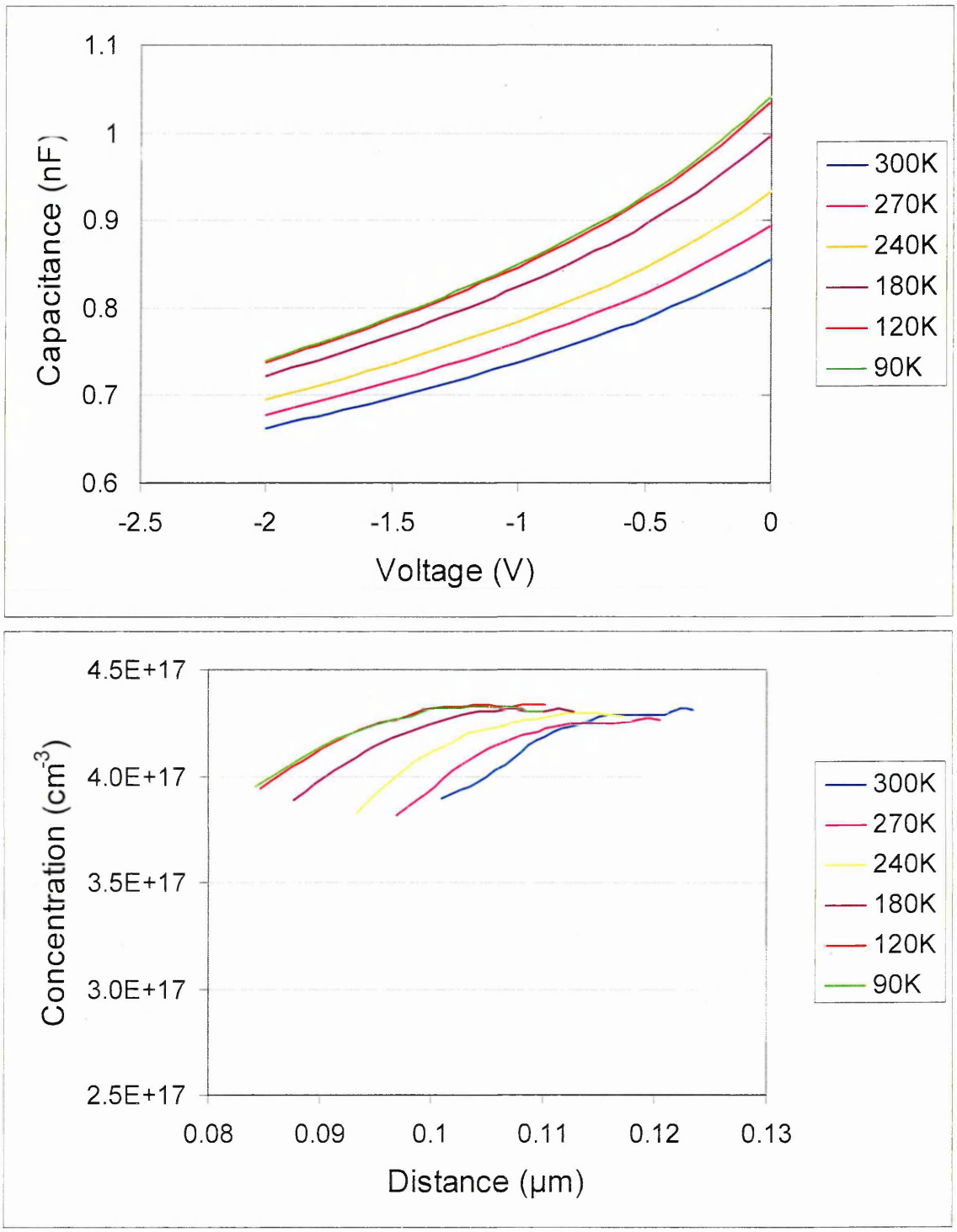


Fig. 6.39: CV and N-x characteristics of S5 at different temperatures

The carrier concentration, as seen from Fig. 6.39, remains almost the same as the temperature decreases and there is not a large bias dependence as with the previous diodes. The volume profiled is 100nm from the p^+n junction at room temperature and the applied bias of -2V indicates that the depletion region width at this bias is 20nm. The carrier concentration remains virtually uniform along the depletion region and is about $4*10^{17}cm^{-3}$ possibly due to the As implant which usually provides a more box-

like doping profile compared to P. It appears that as the temperature reduces, an area closer to the depletion region interface is being profiled. Because the n-side is less highly doped than previous samples, the p^+n depletion region is expected to be wider and hence its capacitance should be smaller and perhaps more comparable to the $n\text{-}n^-$ depletion region capacitance. Hence from Eq. 6.2 it can be seen that the total capacitance is now more dependent on the ultra-shallow junction capacitance. Hence the ultra-shallow depletion region is being profiled when a reverse bias is applied to the p-side. The C-T measurement obtained for S5 is shown in Fig. 6.40 from 300-30K. The capacitance is seen to rise as the temperature reduces, which is contrary to what should be taking place in a diode, as this indicates that more carriers are available at lower temperatures. The increase in capacitance is less rapid in this diode compared to that of diodes S3 and S4.

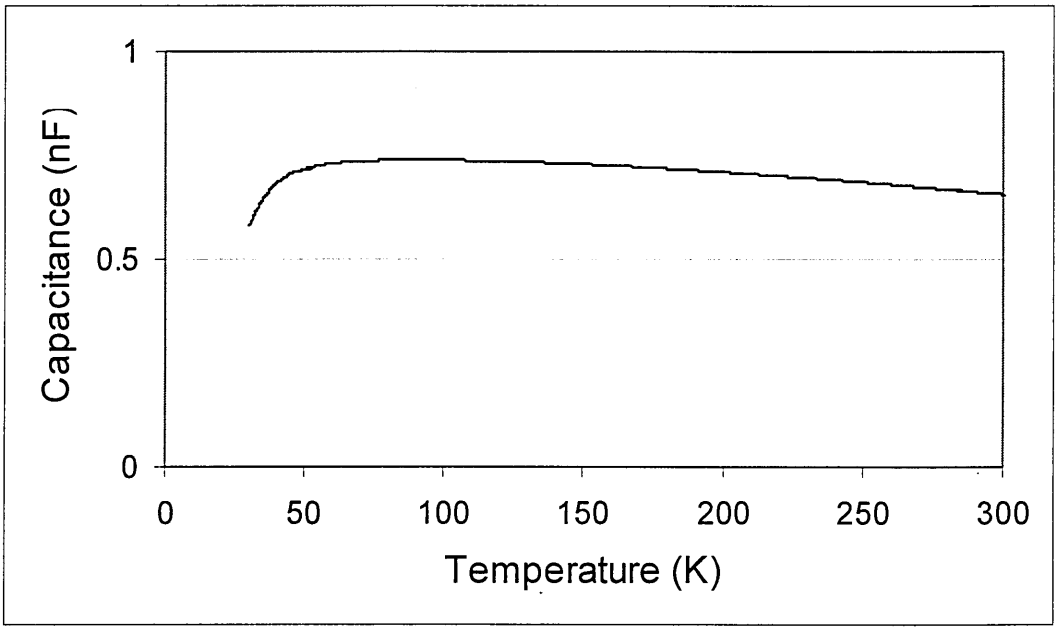


Fig. 6.40: C-T scan of diode S5

Fig. 6.41 shows the equilibrium band diagram for diode S5 which shows that the $n\text{-}n^-$ depletion region is smaller in the absence of bias due to the lower carrier concentration on the n-side. The potential barrier at the p^+n depletion region, from Fig. 6.8, is smaller than in previous diodes and in fact it was found to be 0.97eV which is less than the bandgap of Si. Also the p-side is no longer degenerate and the Fermi level is slightly above the valence band. The previous conclusions about the effect of less doping of the n-side on the diode can be verified by the calculations of depletion region width and capacitance calculated at room temperature shown in Table 6.3.

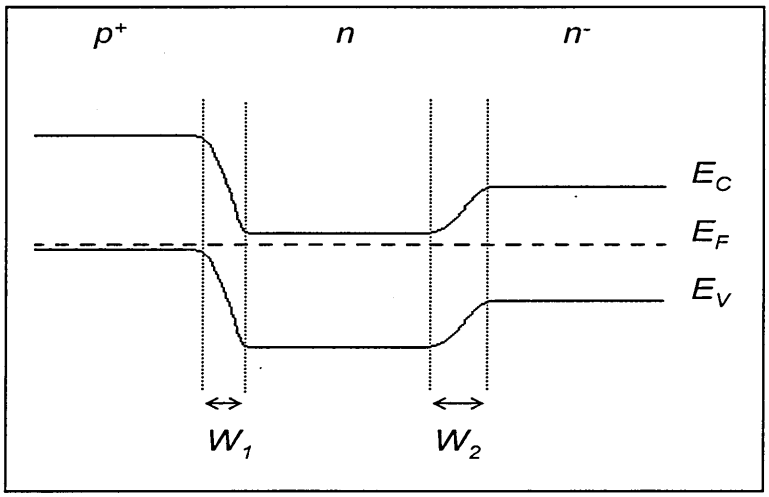


Fig. 6.41: Band diagram of S5 in equilibrium (not to scale)

V_{bi} = 0.97V at Junction 1 and V_{bi} = 0.71V at Junction 2,
with $p^+=1*10^{19}cm^{-3}$, $n=4*10^{17}cm^{-3}$ and $n^-=3.9*10^{14}cm^{-3}$

	300K				
Bias (V)	W_1 (nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{tot} (nF)
0	50	1.54	27	0.88	0.856
0.3	58	1.17	17	0.85	0.81
0.5	62	0.84	11	0.84	0.788
0.6	64	0.61	8	0.858	0.777
0.7	66	0.58	7.5	0.854	0.767

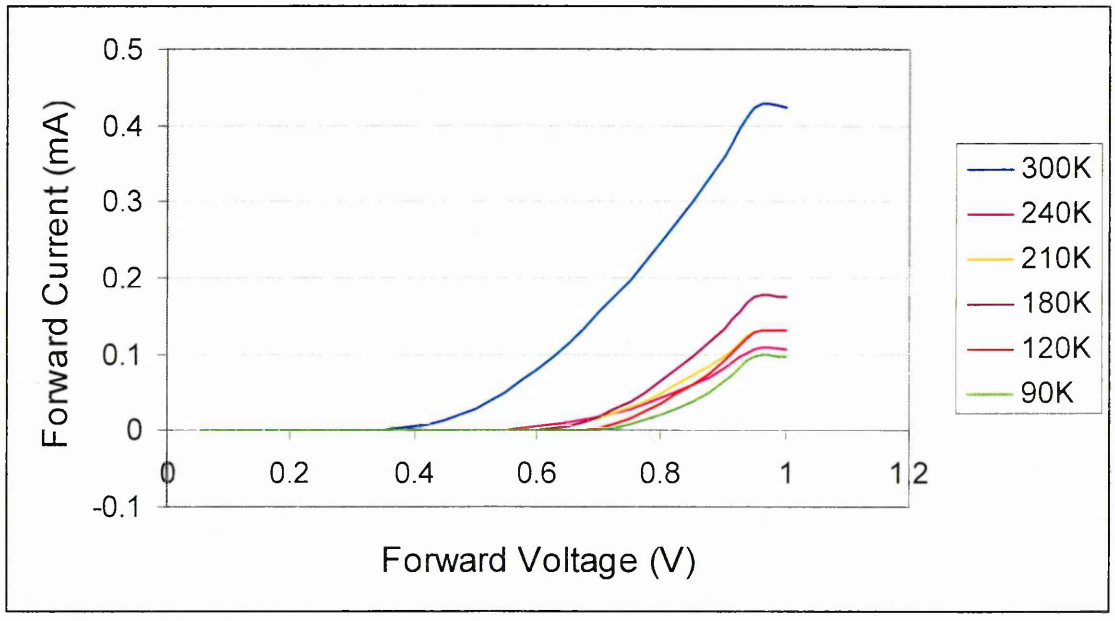
Table 6.3: Depletion region widths and capacitances calculations for diode S5

Comparing the depletion width W_1, of the p^+n depletion region from Table 6.3 with that of Table 6.2 and 6.1 it is obvious that in S5 this junction is much wider even when no bias is applied. The N-x characteristics indicated that the depth of the depletion region profiled from 0-2V of reverse bias is 20nm. However the calculations showed a value at least three times larger. Therefore even though the n-side doping of this diode is lower than that of the other diodes and the capacitance dependence with bias is more diode-like, theoretical calculations and capacitance dependence with temperature suggest that the $n\text{-}n^-$ depletion region capacitance still governs most of the device's characteristics. Table 6.3 confirms that the total capacitance is generally lower than the $n\text{-}n^-$ depletion region capacitance but still comparable.

From the carrier concentration values obtained from the N-x values and the SIMS profile for this diode it can be calculated that, less than 4% of the depletion region lies on the p-side of the ultra-shallow junction. In addition, the N-x measurements suggest that the volume profiled is at a depth of 100nm from the p^+n junction interface as seen

in Fig. 6.39, while the calculations showed that the width of the p^+n depletion region is 50nm at zero bias. Therefore it is not the p^+n depletion region that is being profiled by these measurements but a volume slightly deeper into the As-doped n-side. Returning to the provided SIMS profile of Fig. 5.2 for this diode it can be seen that the depletion region is at a depth of about 170nm from the surface. Therefore the CV and N-x characteristics are profiling from a depth of 270-290nm which is actually the end-of-range of B damage. The DLTS scan should therefore reveal whether there are any hole traps due to this implantation damage as well as any potential electron traps deep into the n-side. Both the p- and n-sides have a lower doping concentration in this diode than in the previous ones, and the barrier height at the p^+n interface was found to be 0.97eV which is also smaller than that of S3 and S4 and less than the bandgap.

Fig. 6.42 shows the IV characteristics of diode S5 obtained at different temperatures. The forward (top) and reverse (bottom) currents are plotted separately for ease of observation. Both the forward and reverse currents of Fig. 6.42 are smaller than in any other diode previously examined. The forward current decreases with temperature below 300K but not very consistently. A similar observation can be made for the reverse current although the IV results indicate a low leakage current. However, the reverse current has its least value at room temperature, increases slightly as the temperature reduces to 240K and then reduces again. A similar behaviour was observed from the reverse current in diode S3. This can be due to the fact that these two diodes have lower doping than diodes S4 and S6 as seen from the SIMS profiles. Hence no significant tunnelling of carriers is expected to be taking place in this diode.



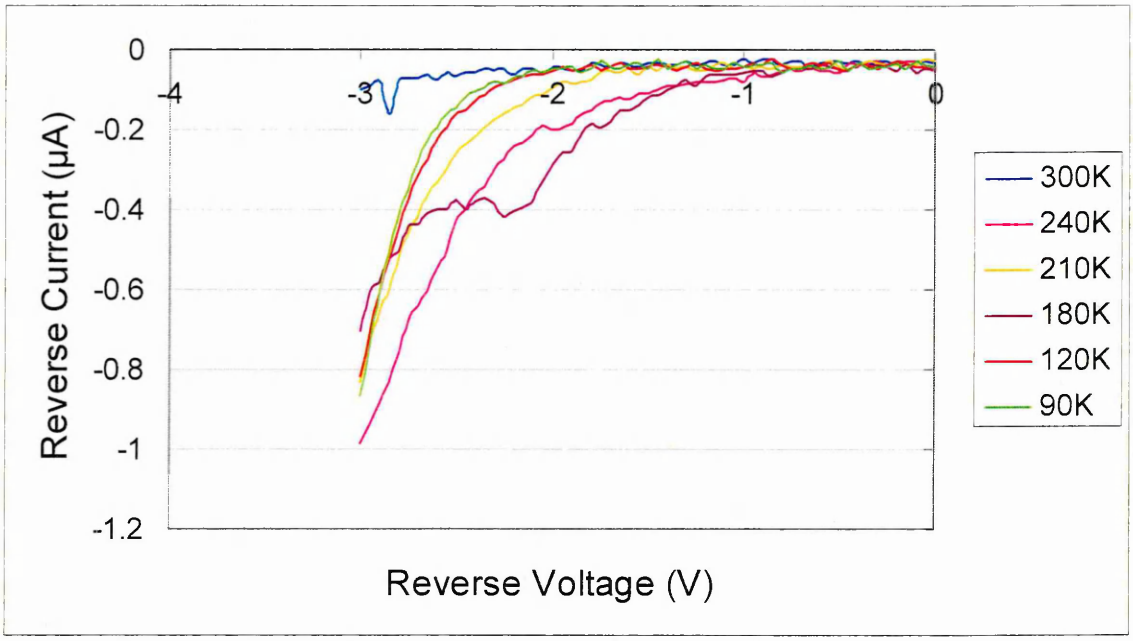


Fig. 6.42: IV characteristics of diode S5. The forward (top) and reverse (bottom) current are plotted separately

DLTS for S5 was performed with reverse bias -2V and different fill pulses. A negative fill pulse did not reveal any traps, while for a positive fill pulse there was only one large minority trap. This appeared with fill pulse 1V and to further investigate the trap subsequent scans were performed with an even larger fill pulse of 2V. A large positive fill pulse should momentarily collapse the p^+n depletion barrier and introduce both majority and minority carriers. However, as the $n\text{-}n^-$ depletion region is then reverse biased it appears that more electrons were injected to the n-side. Therefore the minority trap was even larger with higher positive fill pulse.

The DLTS spectra obtained for S5 with reverse bias -2V and fill pulse 1V are shown in Fig. 6.43. It can be seen that a large minority carrier trap for S5 is detected resulting from a minority capacitance transient. The trap covers a wide temperature range from 130K to about 300K for the higher rate windows. The peak maximum is around 200K and shifts towards lower temperatures for smaller rate windows as expected, since the traps have less energy to emit carriers as the temperature reduces. The peak is asymmetric with the low temperature side, remaining almost fixed for all rate windows. This effect has been observed before from diodes containing dislocations or extended defects, although it may not be indicative of such defects in diode S5 [5]. The activation energy of the minority trap was found to be 0.32eV. A more accurate value was determined from the application of the large positive fill pulse of 2V whose

Arrhenius plot is shown in Fig. 6.44. This is because a large positive fill pulse momentarily forward biases the p^+n junction and introduces both minority and majority carriers thus saturating the observed trap.

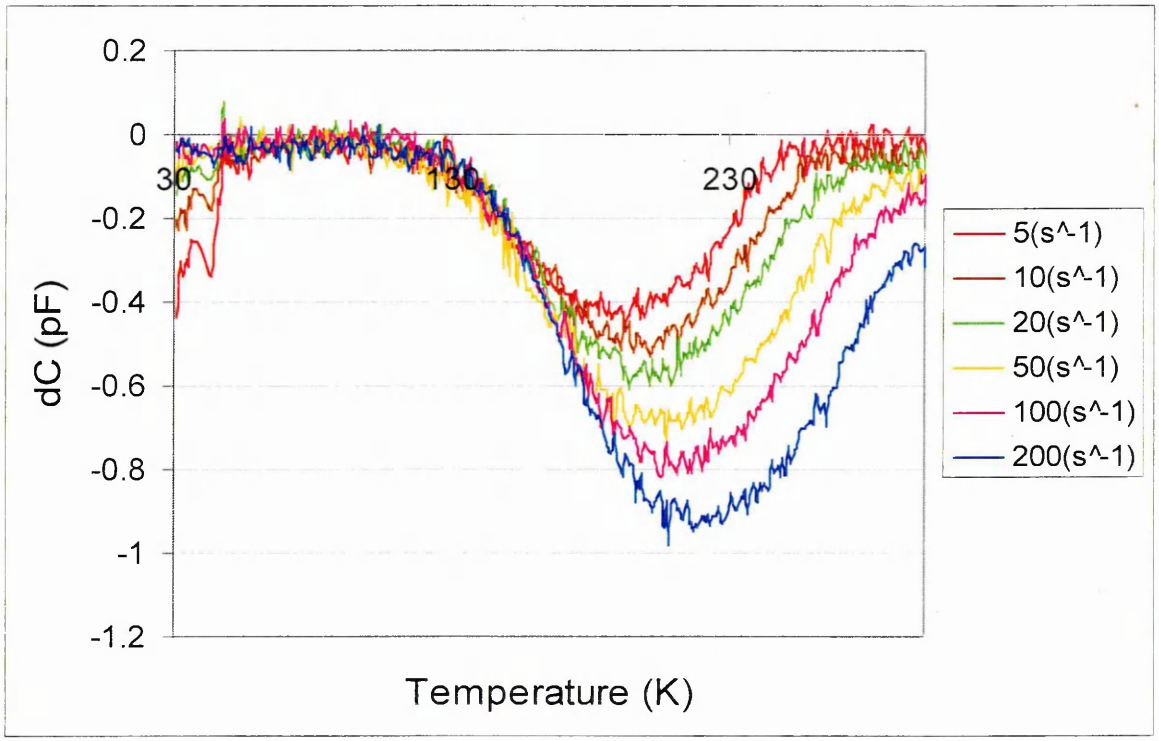


Fig. 6.43: DLTS spectra of diode S5 obtained with reverse bias -2V, fill pulse 1V

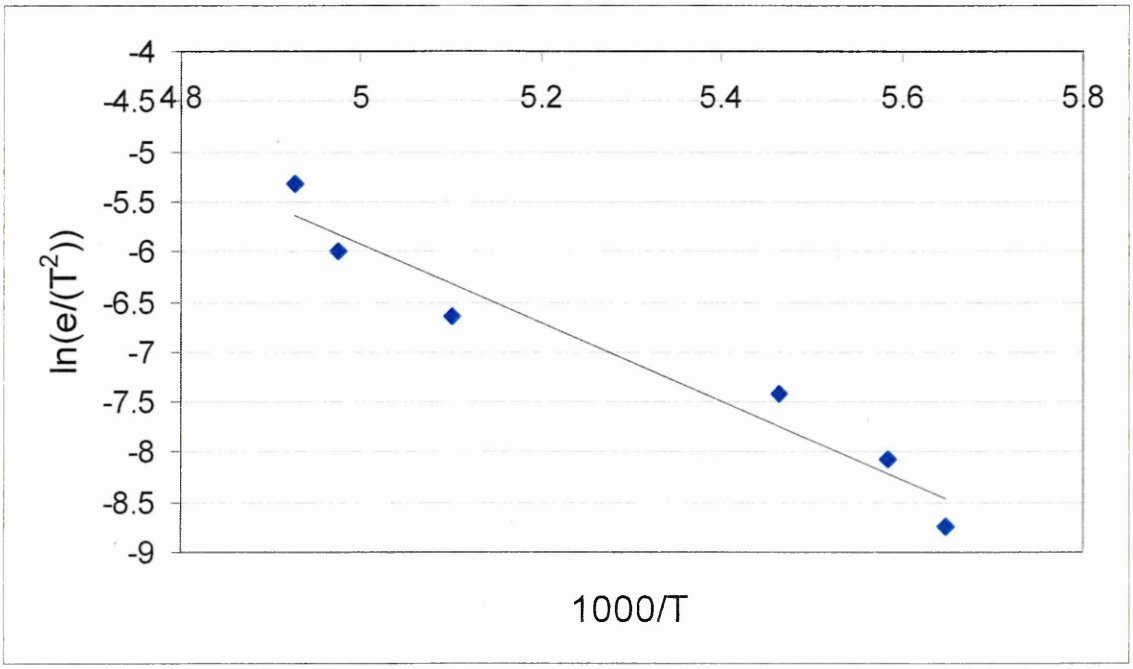


Fig. 6.44: Arrhenius plot of minority trap obtained with reverse bias -2V and fill pulse 2V for S5

The value obtained from the Arrhenius plot of Fig. 6.44 is 0.34eV and it is very similar to that acquired with fill pulse 1V. As this minority trap is located on the n-side, according to the previous discussion stemming from the SIMS and N-x profiles, it is hence a hole trap and is due to B implantation damage. A similar level with an interstitial nature, ascribed to carbon-oxygen complexes, has been observed with almost the same activation energy in B implanted p-type Si [1]. As the hole trap observed is broad on the temperature scale, it is most likely to contain more than one closely spaced level and this was investigated with LDLTS.

Fig. 6.45 shows the LDLTS spectra of the minority carrier trap, which was detected with DLTS with biasing conditions of -2V reverse bias and 1V fill pulse. LDLTS scans were performed around the peak temperature of the trap and a selection of these results is displayed here, for clarity.

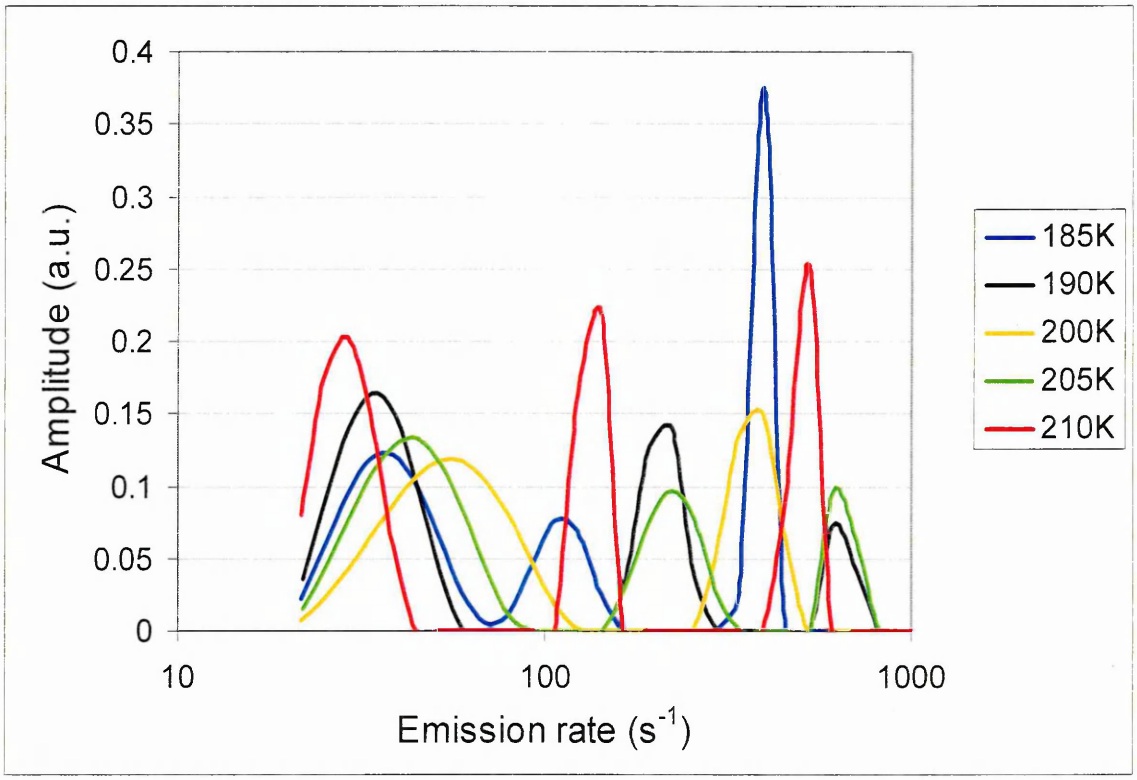


Fig. 6.45: LDLTS spectra of minority trap around 200K in diode S5

Three emission rates have been resolved by LDLTS, which are spaced closely in emission for each temperature. However, the emission rate of all three peaks does not increase consistently as the temperature increases. Therefore these separate levels do not exhibit point defect behaviour. This is in agreement with their assignment to a carbon-oxygen complex from DLTS [6]. As their emission did not increase with temperature,

activation energy calculations cannot be performed from LDLTS. However, this is proof that the asymmetric peak obtained by DLTS, contains more than one levels with complex behaviour.

6.6 Diode S6

This diode had the same P implant as S5 but a higher As implantation dose. However, the electron concentration of the n-side is not expected to be as high as that of S4, since a higher implantation dose was used for S4. From the SIMS profile the carrier concentration of this diode is about $5*10^{18}cm^{-3}$. Normal and opposite polarity CV, N-x and IV measurements were possible for this diode. Fig. 6.46 shows the CV and N-x characteristics with normal polarity and Fig. 6.47 shows the same characteristics when opposite polarity is used.

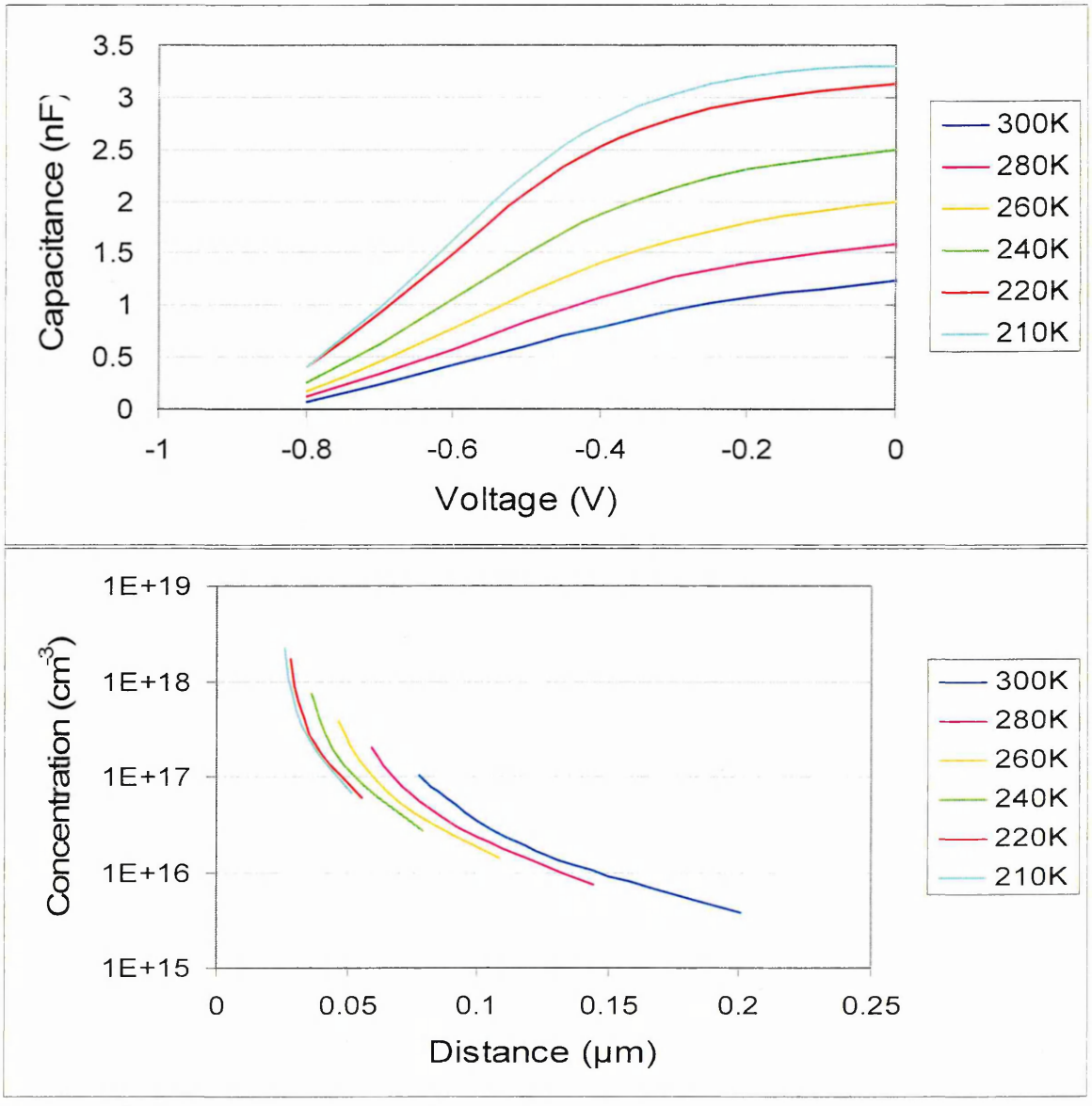


Fig. 6.46: CV and N-x profiles of diode S6 at different temperatures with normal polarity

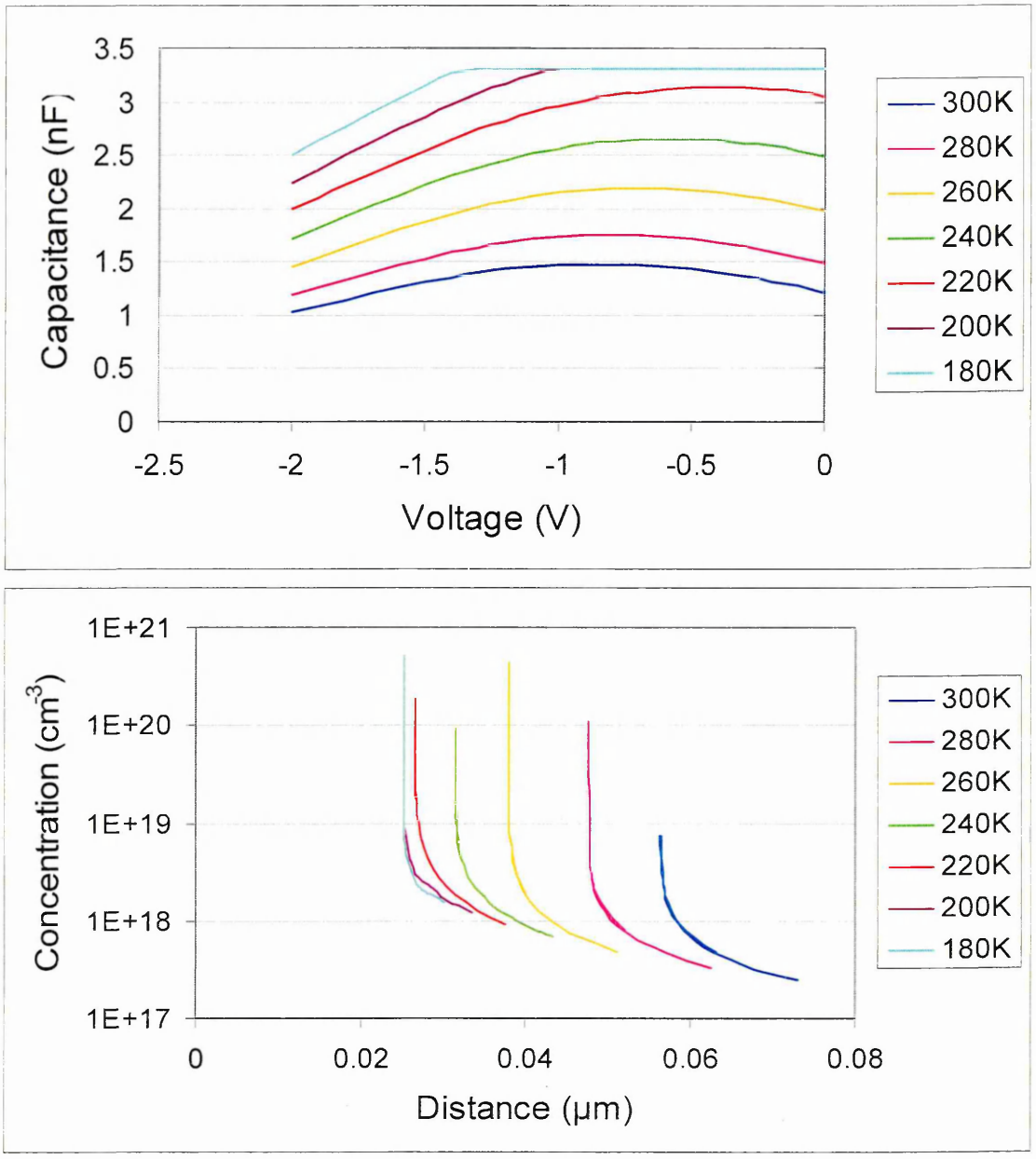


Fig. 6.47: CV and N-x profiles of diode S6 at different temperatures with opposite polarity

It was only possible to perform measurements down to a temperature of about 180K as the capacitance of the diode increased very rapidly and the capacitance meter's maximum range is 3.3nF. A very high capacitance was observed with either polarity which is very bias dependent in the normal polarity configuration. Hence a reverse bias below -0.8V made the capacitance zero. With opposite polarity it was possible to use higher reverse bias of -2V as the capacitance initially increases before it starts to reduce at higher reverse biases. It is proposed that this is the effect of two series capacitances, due to the two depletion regions. Once again as the temperature decreases, the capacitance increases which is contrary to normal diode behaviour. The carrier concentration profiles are very similar to that of the highly doped S4. With opposite

polarity an almost exponential increase in concentration is taking place at high reverse biases, while the normal polarity also indicates a very rapid increase. Finally from the depth profile of Fig. 6.47 it is seen that, when opposite polarity is applied, a volume (~30nm) closer to the interface of the depletion region is being measured than in the case of the normal polarity. For instance if the room temperature N-x characteristics are compared between the two polarities it seems that with normal polarity a depth of 70-200nm below the interface is being measured, which according to the SIMS profile of Fig. 5.2, is within both the B and As end-of-range region. In S5 the profiled region was 100-120nm from the interface at 300K which only covered the beginning of the B end-of-range.

For opposite polarity in diode S6 a depth of 57-73nm from the interface is being profiled at 300K. Therefore it appears that normal polarity continues profiling from where opposite polarity ended. Nevertheless, it should be noted that this is a complex diode with two capacitances in series and it is difficult to accurately state which depletion region the results correspond to, since the capacitance of the $n\text{-}n^-$ depletion region has the smaller value and appears to be dominating according to Eq. 6.2. The C-T scan of diode S6 is shown in Fig. 6.48 and illustrates the very rapid increase of capacitance with reducing temperature. This was performed under a reverse bias of -0.8V and allowed observation of the capacitance rise even below 180K.

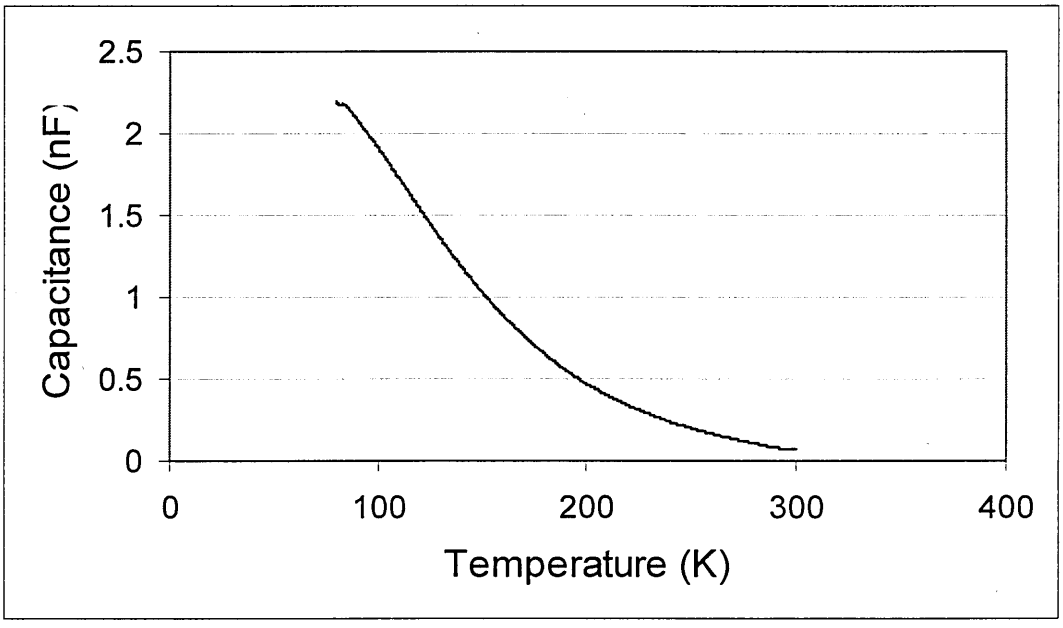


Fig. 6.48: C-T scan of diode S6 under normal polarity and with reverse bias -0.8V

Fig. 6.49 shows the IV results for S6 with normal polarity at different temperatures.

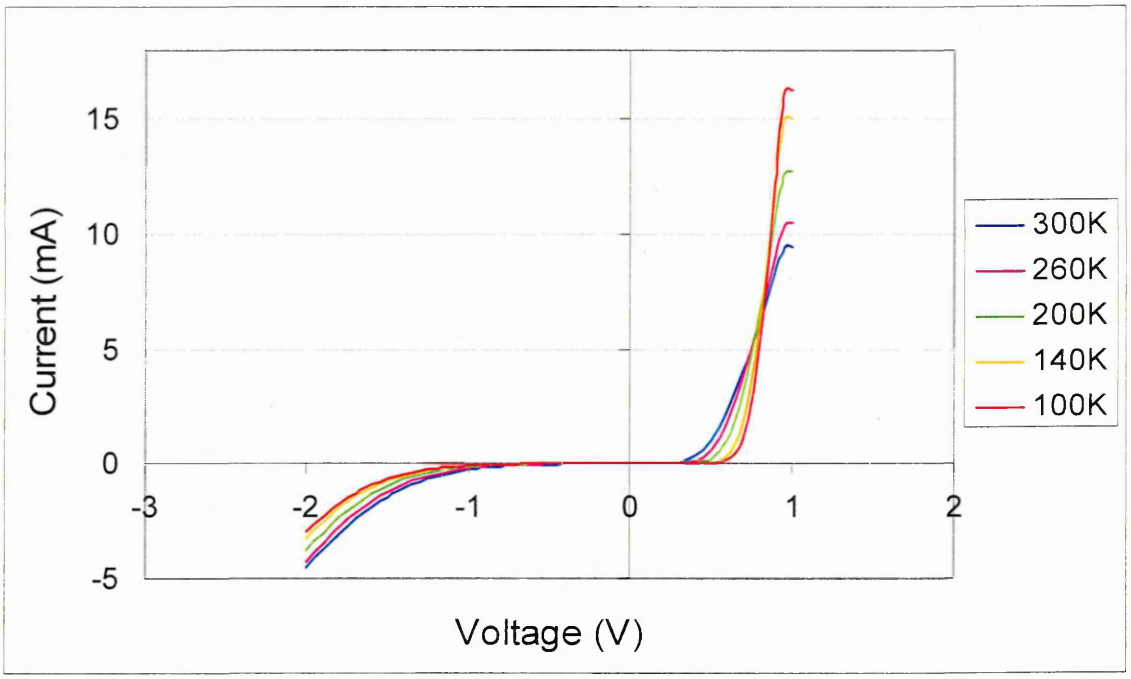


Fig. 6.49: IV measurements of diode S6 under normal polarity

Compared to the highly doped diode S4, the IV results from diode S6, show an even higher forward current. Until a forward bias of 0.8V the current at 300K is higher and decreases with temperature. At 0.8V the forward current has the same value at all temperatures. However, in the same way as in S4, the forward current at 1V is increasing as the temperature decreases with its lowest value being at room temperature (9.4mA). The reverse current however, is considerable at room temperature but steadily reduces as the temperature decreases. The breakdown voltage dependence on temperature for the reverse current at 2mA is shown in Fig. 6.50.

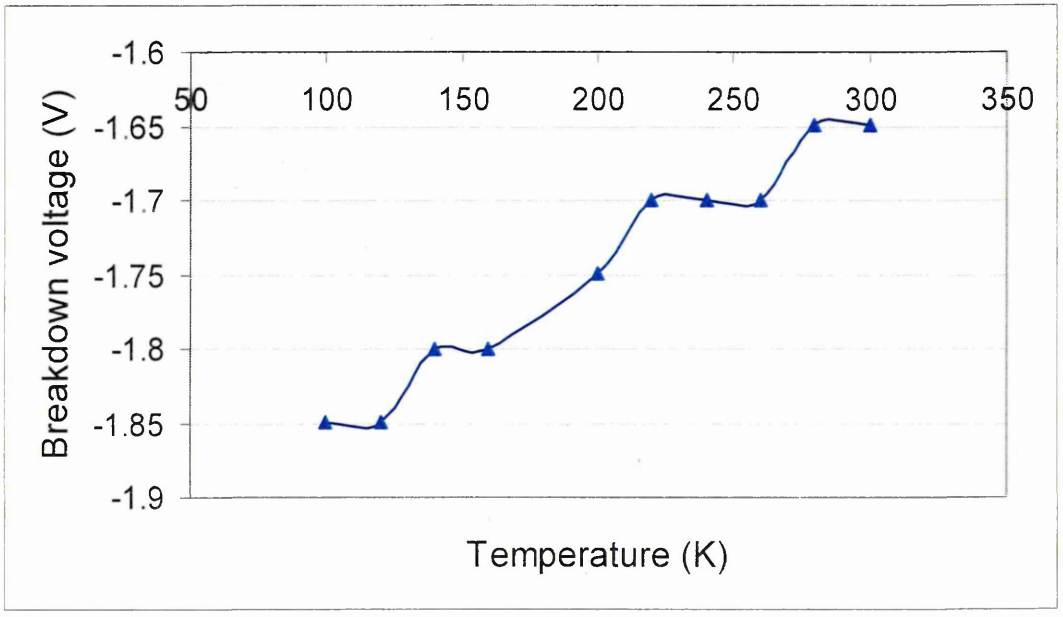


Fig. 6.50: Breakdown voltage, as a function of temperature, from normal polarity IV measurements at 2mA of reverse current

The above figure indicates that tunnelling is taking place in S6, similarly to diode S4 and as the temperature reduces the breakdown voltage appears to increase in steps. The opposite polarity IV measurements are shown in Fig. 6.51. With opposite polarity the reverse current characteristic is that of Zener breakdown indicating that there is more tunnelling and the forward current rises less exponentially indicating that there is thermal current due to minority carrier injection. The magnitude of the forward current is lower with opposite polarity. Compared with the highly doped S4, both the forward and reverse current in diode S6 are higher with both normal and opposite polarity. The barrier height of both, the p^+n and $n\text{-}n^-$ depletion regions is higher in this diode than any of the investigated p^+n diodes, as seen from Fig. 6.8. Therefore, tunnelling is a possible breakdown mechanism in this diode. Fig. 6.52 shows the breakdown voltage with temperature of the reverse current at 1mA. As the breakdown voltage increases in value with decreasing temperature almost linearly, this is indicative of tunnelling.

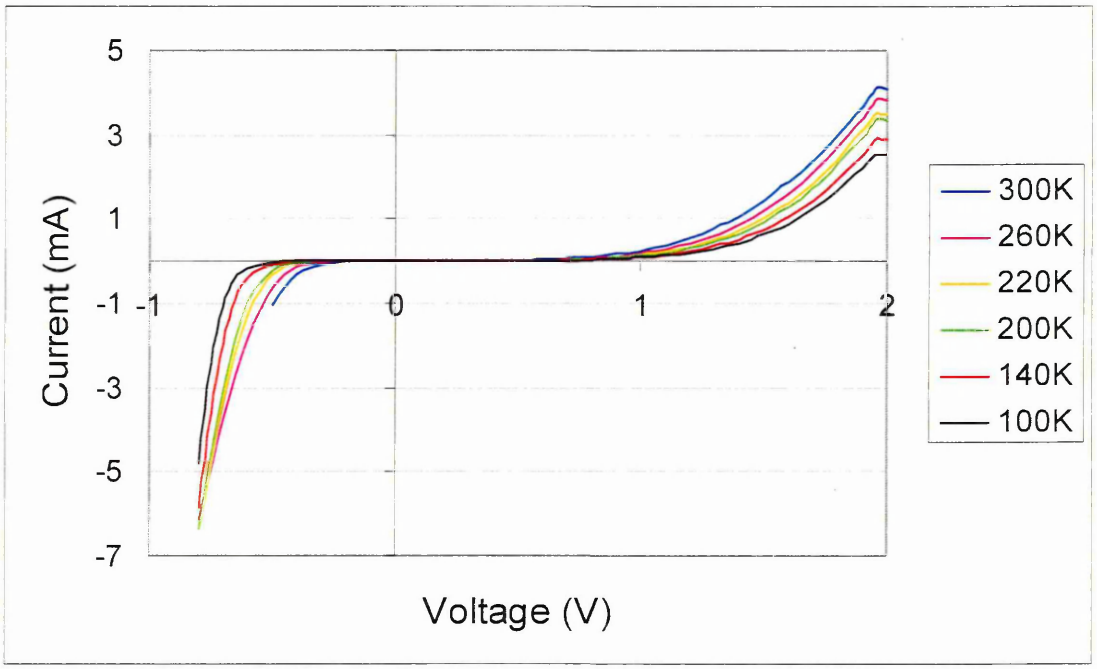


Fig. 6.51: IV characteristics of diode S6 with opposite polarity

The p-side in diode S6 is highly doped but not degenerate and the n-side is very highly doped. From the carrier concentrations as seen from the SIMS profile of Fig. 5.2, it is deduced that one third of the depletion region is in the p-side of the ultra-shallow junction. The energy band diagram for S6 is shown in Fig. 6.53. It can be observed that the Fermi level on both the p- and n-sides is very close to the respective carrier band. The application of even a small reverse bias therefore, is likely to cause tunnelling.

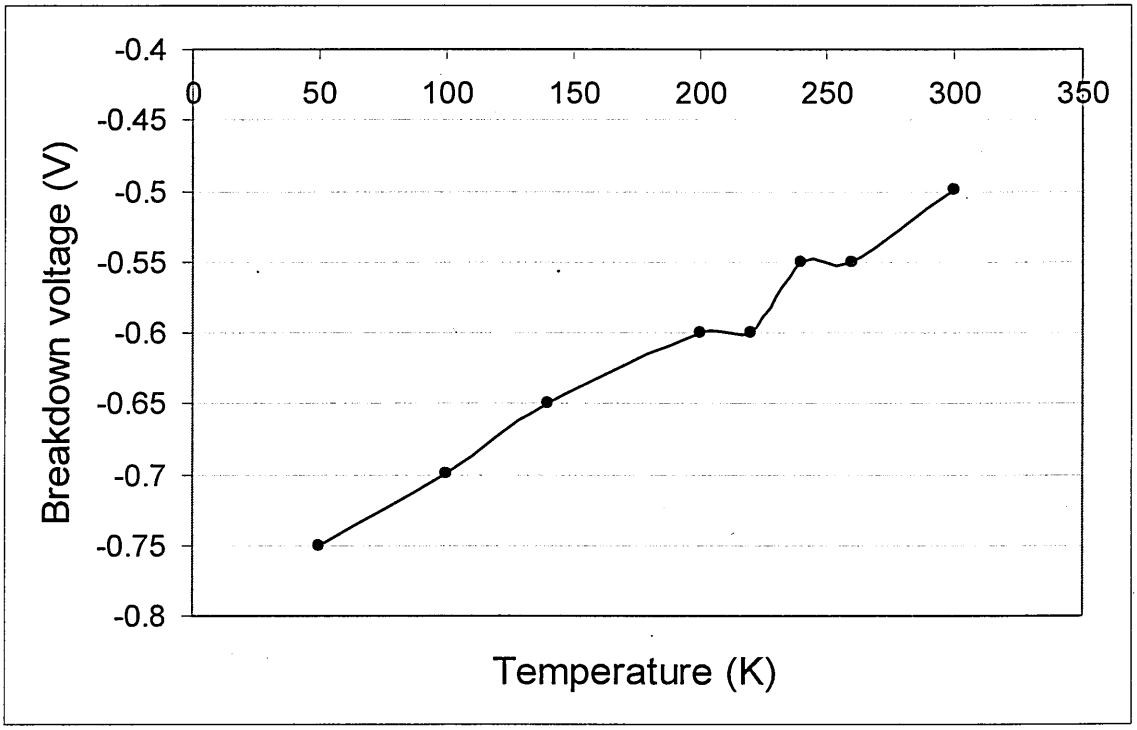


Fig. 6.52: Breakdown voltage dependence on temperature for diode S6 with opposite polarity

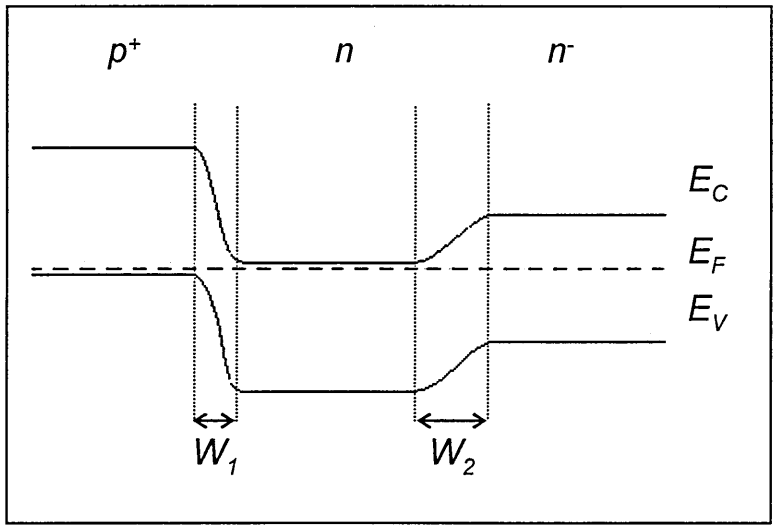


Fig. 6.53: Energy band diagram of S6 in equilibrium (not to scale)

The following table shows the calculated values of depletion region widths and capacitances for this sample using Eq. 6.8 since the depletion region extends by a third on the p-side at the p^+n interface.

Diode S6 Normal Polarity

V_{bi} = 1.03V at junction 1 and V_{bi} = 0.77V at junction 2

with $p^+=1*10^{19}cm^{-3}$, $n= 5*10^{18}cm^{-3}$ and $n^-=3.9*10^{14}cm^{-3}$

	300K				
Bias (V)	W_1 (nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{TOT} (nF)
0	20	1.6	100	1.25	1.2388
0.3	23	1.25	52.5	0.967	0.94949
0.4	23.7	1.11	38	0.81	0.79261
0.5	24.5	0.95	24	0.63	0.61046
0.6	25.4	0.75	12.7	0.43	0.41665
0.7	26	0.48	4.5	0.24	0.23037

Diode S6 Opposite Polarity

V_{bi} = 1.03V at junction 1 and V_{bi} = 0.77V at junction 2
with $p^+=1*10^{19}cm^{-3}$, n= $5*10^{18}cm^{-3}$ and n-=$3.9*10^{14}cm^{-3}$

	300K				
Bias (V)	W_1(nm)	W_2 (um)	C_1 (nF)	C_2 (nF)	C_{TOT} (nF)
0	20	1.6	98	1.226	1.2114
0.3	17	1.9	154	1.375	1.3626
0.4	15.7	2	179	1.41	1.399
0.5	14.4	2.1	210	1.44	1.4295
0.6	13	2.15	242	1.46	1.453
0.7	11.4	2.22	287	1.477	1.4693
0.8	9.5	2.3	360	1.48	1.4777
0.9	7	2.37	502	1.483	1.4783
1	3.4	2.44	1056	1.472	1.4698

Table 6.4: Depletion region widths and capacitances calculations for diode S6

Table 6.4 shows that with normal polarity C_1 is rapidly decreasing with bias and therefore its contribution to the total capacitance is more significant. In the opposite polarity configuration, where the n-n^- depletion region is reverse biased, a large volume of 2.44μm is being profiled according to the calculations. Hence it is more likely that any As implantation damage may be revealed by DLTS.

DLTS was performed in this diode with normal polarity and positive and negative fill pulse. The lowest reverse bias that could be applied was 0.8V because the capacitance drops to zero below this value. In both cases, normal polarity measurements yielded the same minority carrier trap which was more pronounced when a positive fill pulse followed the initial reverse bias. This is due to the fact that under a positive fill pulse the potential at the p^+n junction is lowered and minority carriers can be injected. Opposite polarity measurements were also performed with positive and negative fill

pulses and a set of majority carrier traps were revealed with a large positive fill pulse. This is due to the fact that the p+n depletion region must have collapsed from the application of such a large forward bias and hence majority and minority carriers are being injected. Fig. 6.54 shows the DLTS spectra with normal polarity and positive fill pulse and the Arrhenius plot that produced the activation energy of the trap. A reverse bias of -0.8V was applied with a fill pulse of 1V and only some of the higher rate windows are shown for clarity.

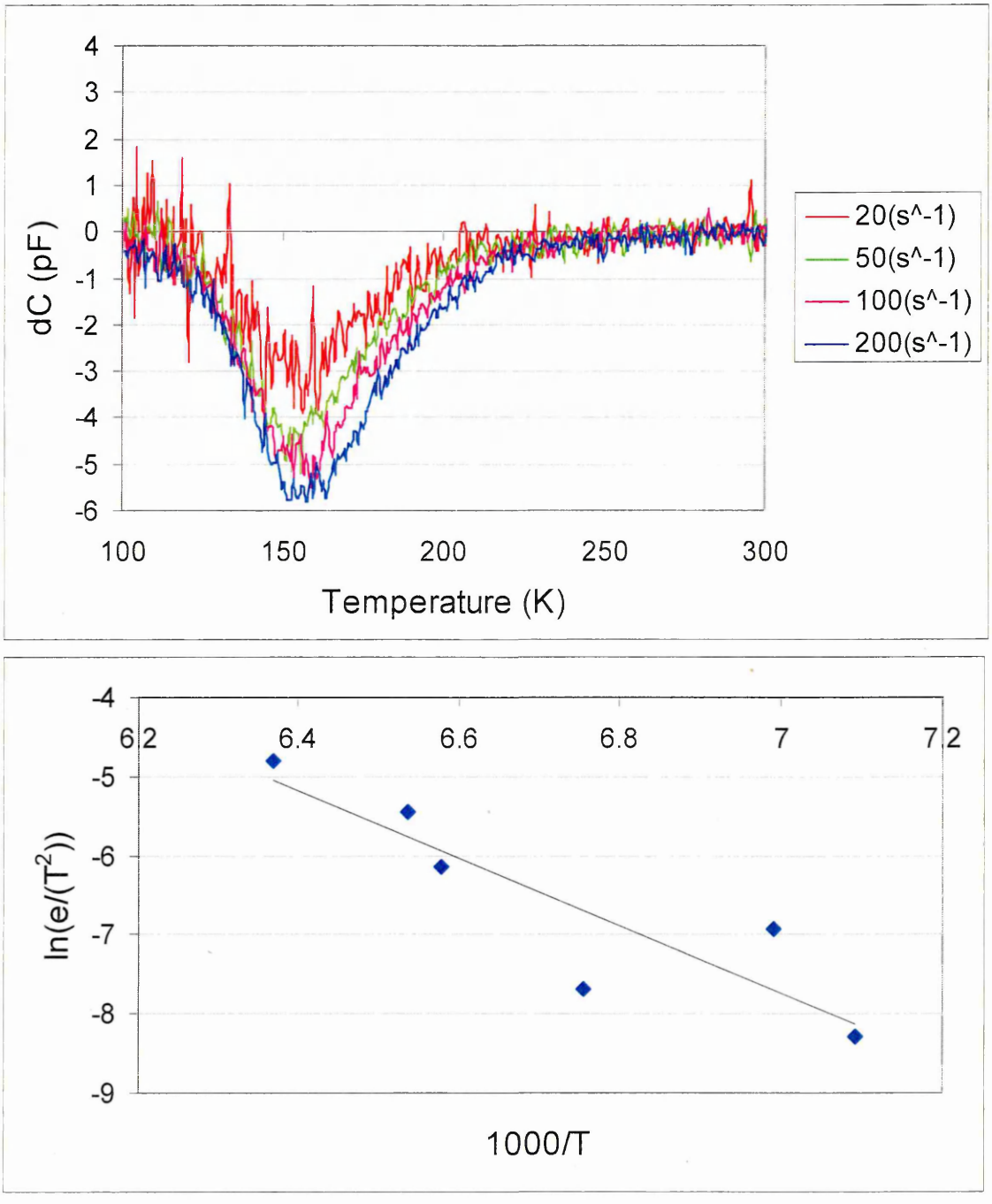


Fig. 6.54: DLTS spectra of diode S6 with normal polarity, reverse bias -0.8V and 1V fill pulse (top) and corresponding Arrhenius plot (bottom)

The DLTS of S6 reveals a large minority trap, similarly to diode S5. Again this peak covers a wide temperature range from 120-200K. As only a third of the p$^+$n depletion region lies on the p-side in this diode, it is likely that this trap is a hole trap due to B implantation damage on the n-side. This is further supported by the fact that according to the N-x profile, normal polarity scans a volume of 100-150nm from the p$^+$n interface which corresponds to the B end-of range. The activation energy found from the Arrhenius plot was 0.36eV. Hence it could be attributed to the carbon-oxygen complex that lies at about 0.36eV above the valence band.

Fig. 6.55 shows the DLTS spectra obtained with opposite polarity, reverse bias -2V and fill pulse 1.5V.

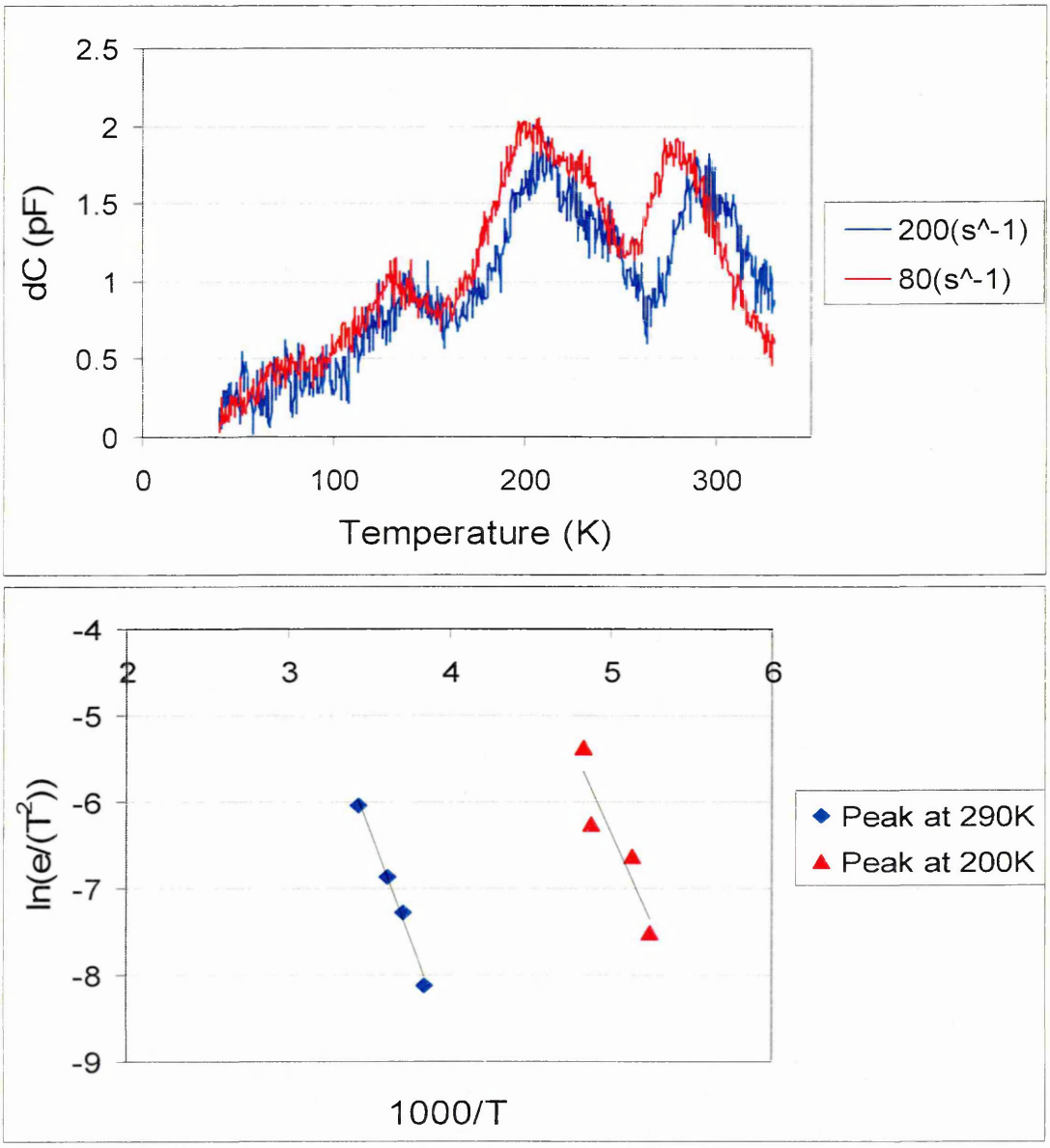


Fig. 6.55: Opposite polarity DLTS of S6 with reverse bias -2V, fill pulse 1.5V (top) and Arrhenius plots of the peaks at 200K and 290K

At least three different defect levels were detected, which correspond to defects in the n-side or the n-n⁻ depletion region due to the high As and P implants. Of these three peaks the one at the lowest temperature was small and the signal had more noise at lower rate windows. Hence its activation energy could not be determined. The Arrhenius plot of the two higher temperature defects is also shown in Fig. 6.55. Only two rate windows are shown in Fig. 6.55 for clarity. However, this is sufficient to demonstrate the presence of at least three defect levels at 130K, 200K and 290K. The peak at 130K was too noisy at lower rate windows. The activation energies found from the Arrhenius plots for the defects at 200K and 290K were 0.36eV and 0.43eV respectively. As these are defect levels on the n-side, they can be attributed to a carbon-interstitial complex for the 0.36eV defect and the arsenic-vacancy overlapping with the singly negative charged state of the divacancy, for the 0.43eV level [1].

LDLTS was performed using normal polarity with the same biasing conditions as the DLTS of Fig. 6.54 in order to investigate the nature of the large minority peak at 150K. A minority capacitance transient was acquired consistently at each temperature. Some of the obtained results are shown in Fig. 6.56 in 3-D view.

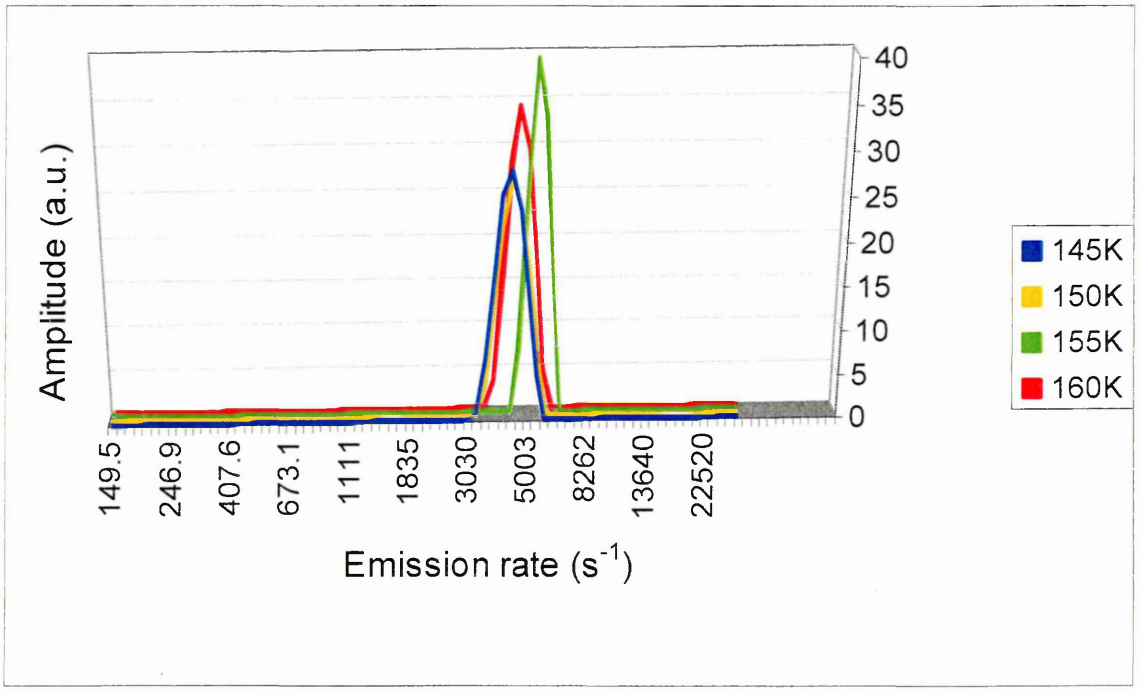


Fig. 6.56: LDLTS of diode S6 with normal polarity, reverse bias -0.8V and fill pulse 1V

As can be seen from the LDLTS spectra, the emission rate of the defect does not change with temperature. In addition any change does not follow a consistent pattern. Hence it is concluded that this emission is not due to a point defect but more likely an extended

defect. It is possible therefore that this emission is due to a carbon-oxygen complex, as suggested from DLTS experiments, as it does not exhibit temperature dependent emission [6].

6.7 Conclusion

This chapter investigated the electrical characteristics of p^+n ultra-shallow junctions in Si buried in a doping-well. It was concluded that the high doping required in order to develop such structures results in very complex phenomena as far as the energy distribution of the carrier bands is concerned. Two depletion regions arise, one at the shallow junction and one with the substrate, that result in two capacitances in series, the smaller of which governs the device characteristics. However, due to the presence of two depletion regions in the same diode, application of both reverse and forward bias is possible. This enables profiling of defects at different depths within the structure, which can lead to a more detailed knowledge of the deep levels involved. The experimental results illustrated that the high doping generated a range of defects, such as the VP, V^-, V^{-2} and carbon substitutional-carbon interstitial levels, which are common in n-type Si. These were detected by the use of the opposite polarity configuration on the most highly doped diodes and were present irrespective of As content, since P implantation sufficed for their generation. Finally, minority traps were detected in all the studied diodes, which were shown to be due to extended or complex defects involving B, when the sole dopant was P, or C where As doping was present.

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Chapter 7: Experimental results from n^+p Ultra-shallow junctions

7.1 Introduction

This chapter presents the experimental results of n^+p Ultra-shallow junctions in Si. As mentioned previously, very highly doped USJs arise from the different implants used to simulate a p-type doping well. These diodes are expected to have a similar behaviour to the p^+n structures that were examined in the previous chapter, due to the high doping. The very high doping on the n-side was achieved by high dose implantation of arsenic (As) and the p-type doping of the p-side resulted from a combination of boron (B) implants for each of the diodes. The p-side of one of the diodes was kept undoped for reference purposes and to allow investigation of the p-type substrate. All the specifications associated with these diodes as well as their fabrication procedure were described in chapter 5, together with the SIMS profile that was provided with the samples. The latter was shown in Fig. 5.3 and will serve as a guide of the doping content of the diodes and will be compared with the carrier concentrations found by the CV measurements. The diodes were characterised using the CV, IV, DLTS and LDLTS techniques similarly to the p^+n USJs of the previous chapter.

7.2 Control diode S9

Diode S9 has a single As implant for the formation of the n-side and the p-type substrate only contains the background doping. Therefore it can be used as a reference diode and CV measurements will reveal the carrier concentration of the substrate. This can be used to determine the barrier height of the remaining diodes where the p-side is more highly doped with B. Fig. 7.1 shows the CV characteristics obtained for S9 at different temperatures. These indicate that the capacitance steadily decreases as the temperature reduces from 300K to 60K at zero applied bias. In addition, at each temperature, the capacitance is gradually reducing with increasing reverse bias in a normal diode-like manner. Finally it can be noticed that the capacitance at room temperature is generally small. This is expected as in this diode the depletion region is entirely on the low doped p-type substrate since the n-side is very highly doped.

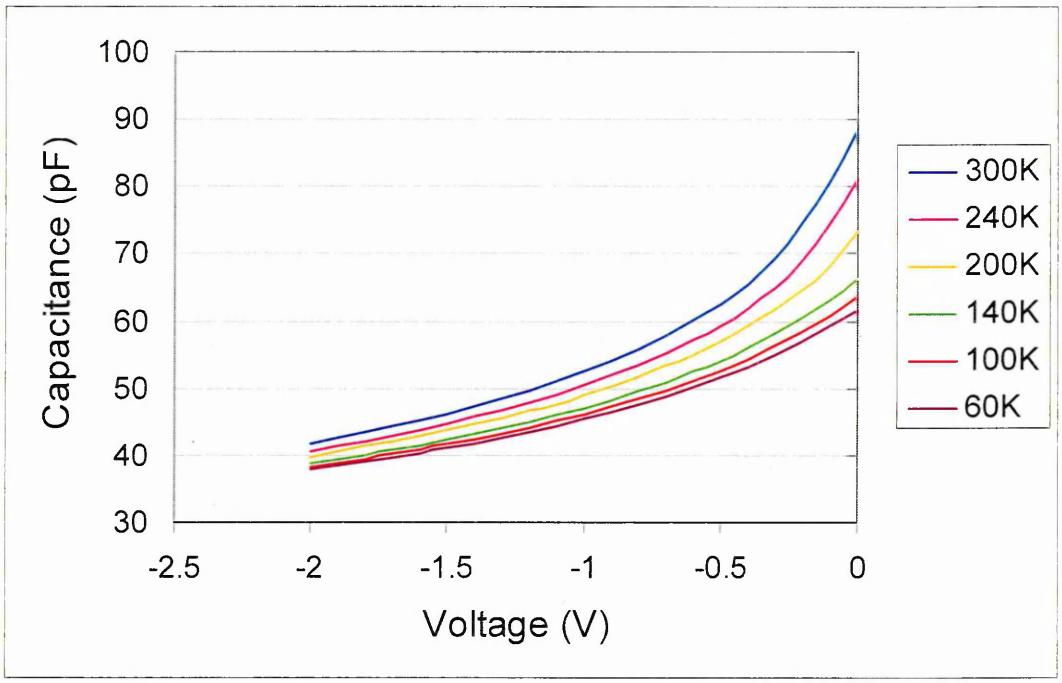

Fig. 7.1: CV characteristics of control diode S9 at different temperatures

To verify these assumptions the carrier concentration with depth (*N-x*) profile for diode S9 is shown in Fig. 7.2.

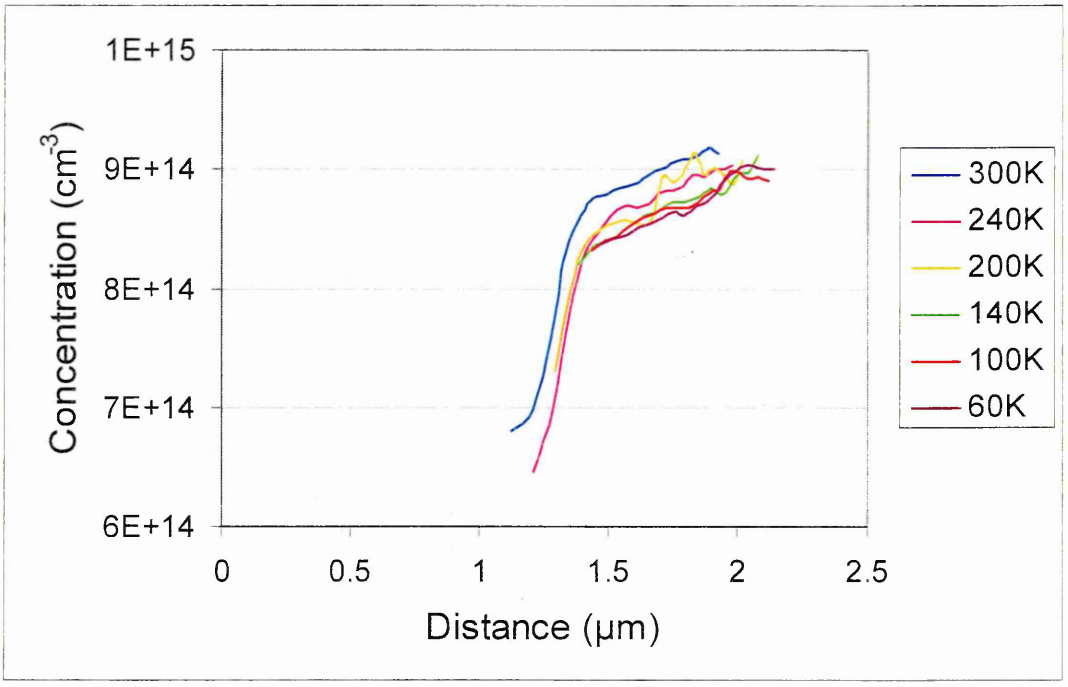

Fig. 7.2: N-x characteristics of control diode S9 at different temperatures

The x-axis of the N-x profiles shows the profiled depth from the n$^+$p junction interface, unlike the SIMS profiles which show the doping concentration with depth beneath the diode surface. The N-x characteristics for this diode reveal a carrier concentration of $7*10^{14}cm^{-3}$-$9*10^{14}cm^{-3}$ which is slightly reducing with temperature as expected, since

fewer carriers are contributing to conduction at lower temperatures. Also for any particular temperature the concentration of carriers slightly increases as the reverse bias increases. Using Eq. 4.2 from chapter 4, it was calculated that the depletion region width in the absence of bias is 1.26μm and gradually increases to 2.1μm for a reverse bias of -2V. This result is indeed reflected in Fig. 7.2. It can also be observed that the depth profiled by these N-x measurements is deeper than about 1.2μm from the interface between the n^+- and p-sides. This is because the doping of the n^+-side is almost six orders of magnitude larger than that of the p-side substrate. Therefore the depletion region appears entirely into the p-side and covers a large depth even at zero applied bias. Hence no As-implantation damage is expected to be observed. However, DLTS for this diode was performed and will provide a clearer picture about any deep centres into the substrate that should be taken into account for the remaining highly doped n^+p diodes. Finally, the observed carrier concentration of around $8.5*10^{14}cm^{-3}$ is the value that is going to be used for any further calculations involving the carrier concentration of the substrate.

The capacitance of the diode was measured as the temperature reduced from 300K to 40K and under reverse bias -2V and the obtained result is illustrated in Fig. 7.3.

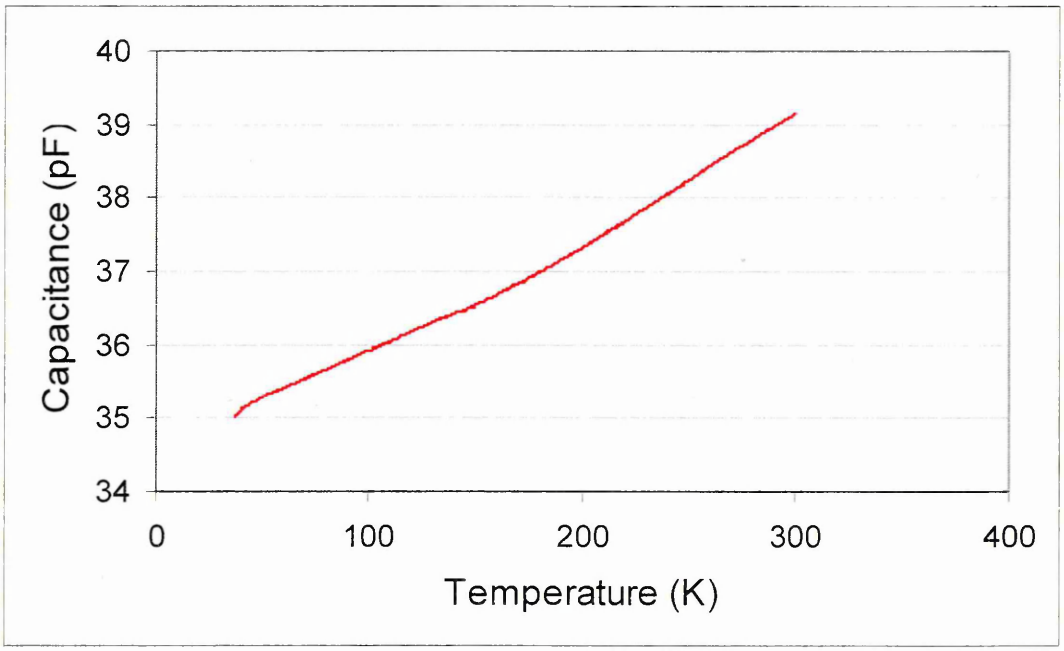

Fig. 7.3: C-T scan from 300K to 40K of diode S9 under reverse bias -2V

Fig. 7.3 shows that the initial capacitance at room temperature has a value of about 39pF when reverse bias of -2V is applied. This value decreases almost linearly when the

temperature reduces as many carriers freeze-out at lower temperatures and cannot conduct current. Fig. 7.4 shows the IV results obtained when the diode was swept from 1V to -4V, at different temperatures with the inset showing the reverse current at selected temperatures in order to facilitate observation, as it is too small compared to the forward current. In addition, Fig. 7.5 shows the reverse current at -3V as the temperature reduces.

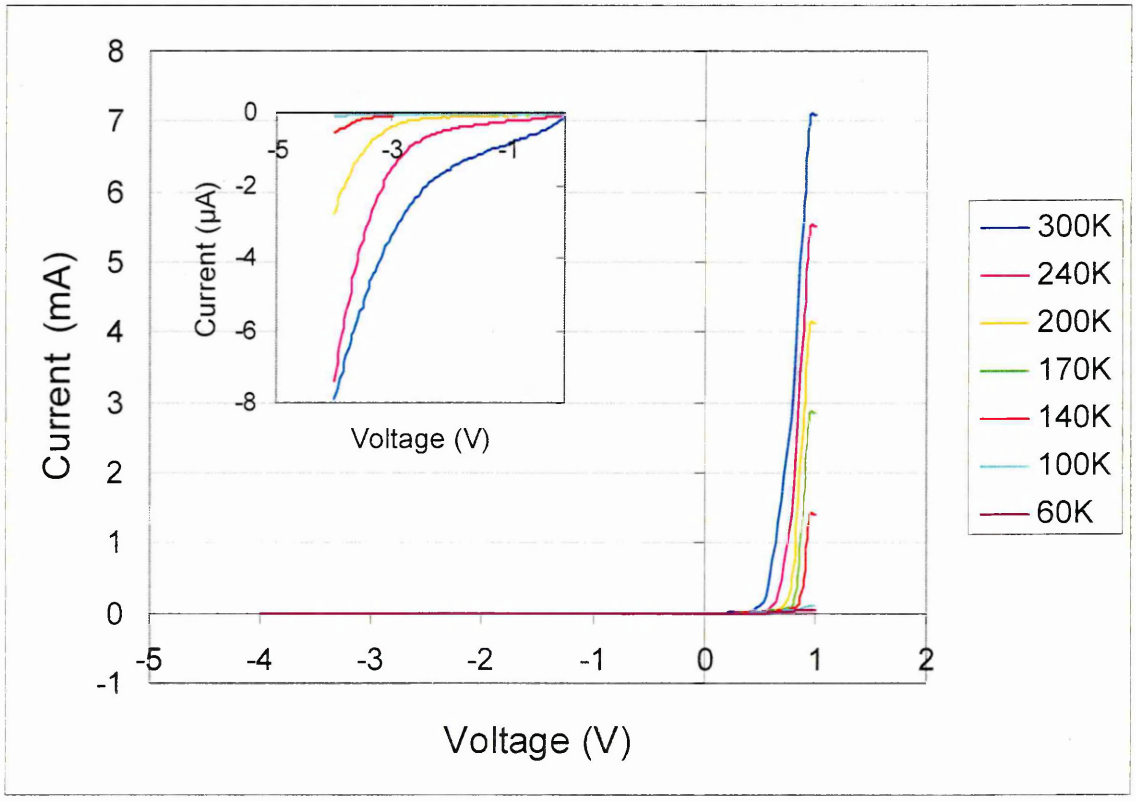

Fig. 7.4: IV characteristics of control n+p diode S9 at different temperature. The inset shows a magnified view of the reverse current at selected temperatures

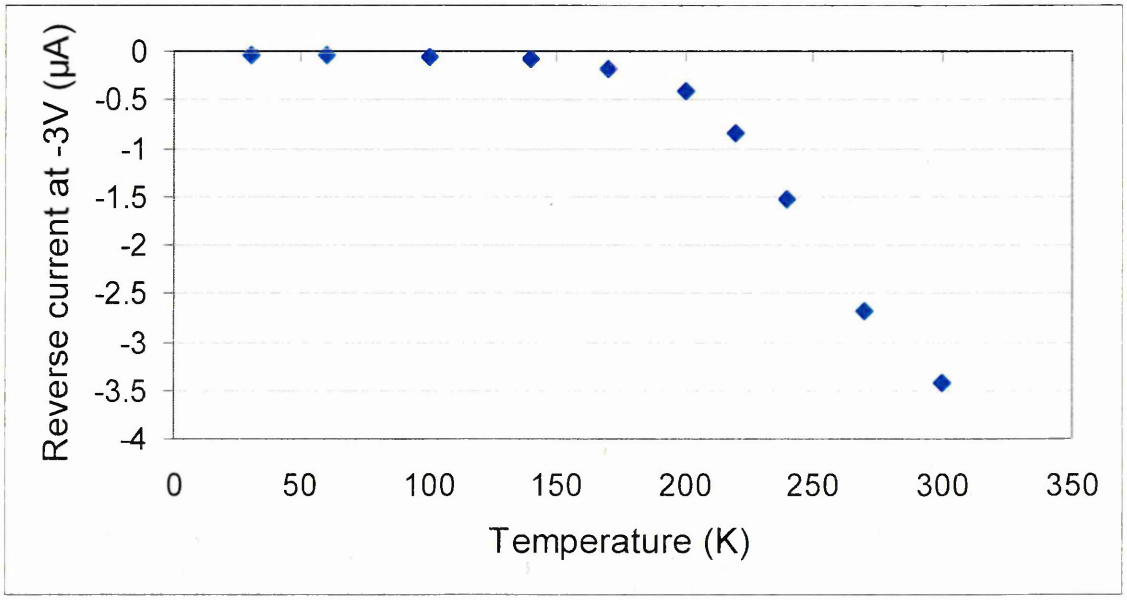

Fig. 7.5: Reverse current for diode S9 at -3V with temperature

From the IV characteristics of Fig. 7.4 it can be seen that the forward current is 7mA at room temperature and at 1V forward bias but it is steadily reducing as the temperature is dropping as expected. Similarly the reverse current is about 7.8μA at room temperature at -4V but reduces down to 58nA when the temperature drops to 100K. The reverse current at -3V reduces from 3.5μA at 300K to 35nA at 30K thus decreasing by 100 times within this temperature range. Therefore this can be considered a very good diode with very low leakage. It is worth noting that according to the SIMS profile of Fig. 5.3 for all these n^+p diodes, the n^+-side is very highly doped and Fermi level calculations showed that the n^+-side is slightly degenerate (by 8meV). This should become even more pronounced under the higher reverse bias of -4V. Also the Fermi level on the p^--side was calculated at 0.28eV above the valence band. This suggests that the barrier height at the depletion region for this diode is 0.848eV, which is quite large. The barrier height magnitude was also confirmed by calculating the built-in voltage (V_{bi}) for this diode using Eq. 4.8.

As mentioned earlier, no deep levels due to As are expected to be observed in the depletion region of this diode since As is a heavier atom and is expected to cause damage closer to the surface and within the n^+-side, while the profiled volume is deep into the p^--side. Therefore DLTS is not expected to reveal any significant traps. This was confirmed by the measurements with application of both positive and negative fill pulse. Fig. 7.6 shows the DLTS spectra at a rate window of $200s^{-1}$ with large positive, small positive and negative fill pulse.

From Fig. 7.6 it is obvious that irrespective of the biasing conditions or the magnitude of the fill pulse no majority or minority carrier traps were detected by DLTS as expected. If any traps are present in the p-substrate their concentration must be too small. As the substrate is high quality p-type Si however, it is unlikely that any defects are present. Therefore LDLTS was not applied to diode S9 since no trap levels were detected by DLTS. The investigation of this control diode yielded very significant results since the carrier concentration of the substrate was determined, which will allow the calculation of barrier heights in the B implanted diodes. Finally it was confirmed that no intrinsic deep levels are present in the substrate and if these are detected in the following diodes, they will be due to B or As implantation damage.

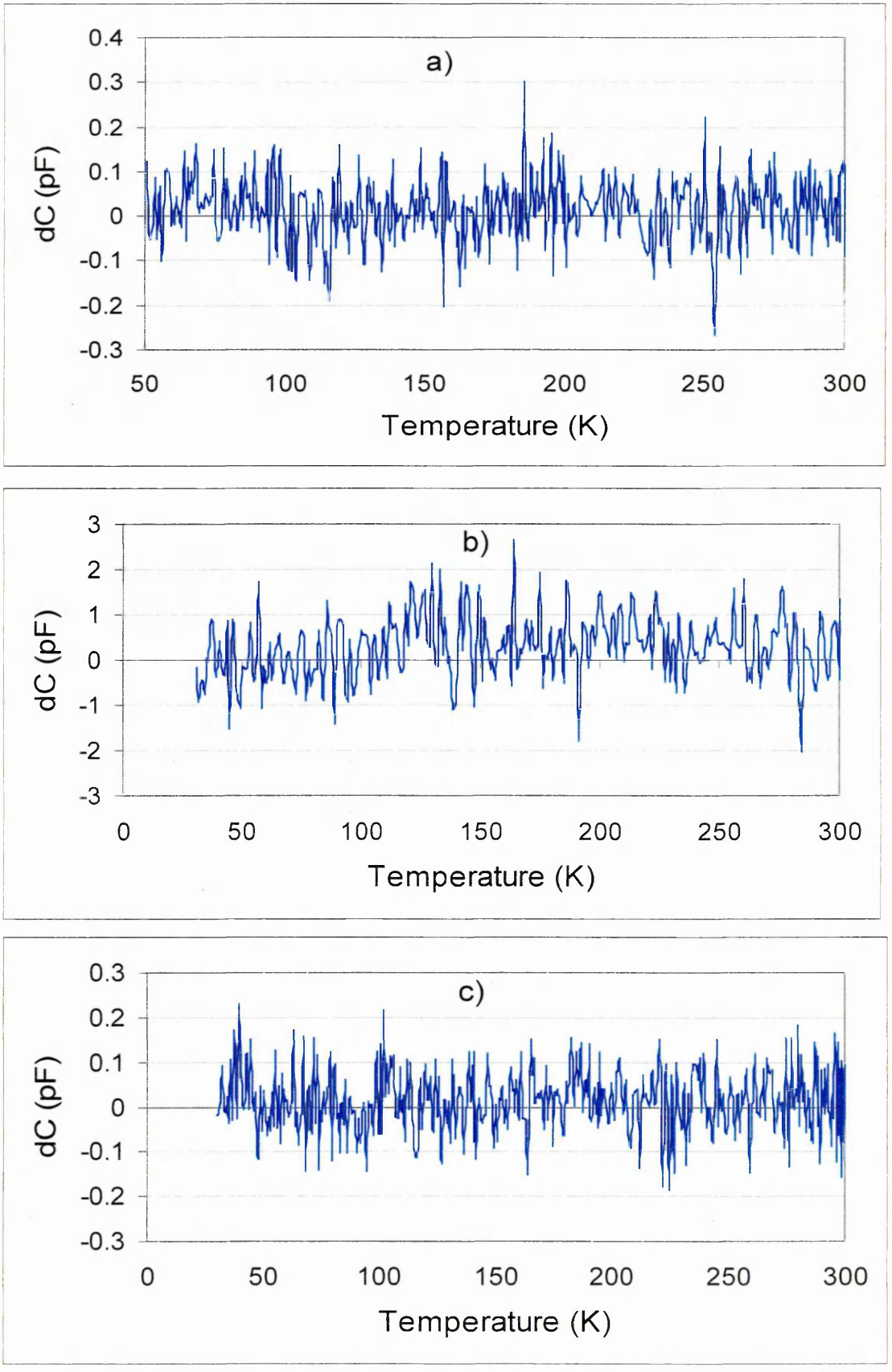

Fig. 7.6: DLTS spectra of diode S9 with rate window 200s^{-1} and a) reverse bias -3V and large positive fill pulse 2V, b) reverse bias -3V and small positive fill pulse 0.5V and c) reverse bias -2V and negative fill pulse -1V.

7.3 Diode S8

Diode S8 had two relatively low dose B implants so as to form a shallow n^+p junction in a simulated doping well, as seen from Table 5.1. The SIMS profile for this diode in Fig. 5.3 shows a doping concentration of around $1*10^{18}cm^{-3}$ on the p-side. As the p-substrate has about four orders of magnitude lower doping, two depletion regions are expected to have formed, similarly to the p^+n diodes that were examined in the previous chapter. One junction is between the highly doped n^+-side and the highly doped p-side and one between the highly doped p-side and the p-type substrate. The same situation exists in diode S7, which will be examined later. Once again, to correctly examine these diodes, Fermi level calculations were carried out at different temperatures for both depletion regions and the results are displayed in Fig. 7.7.

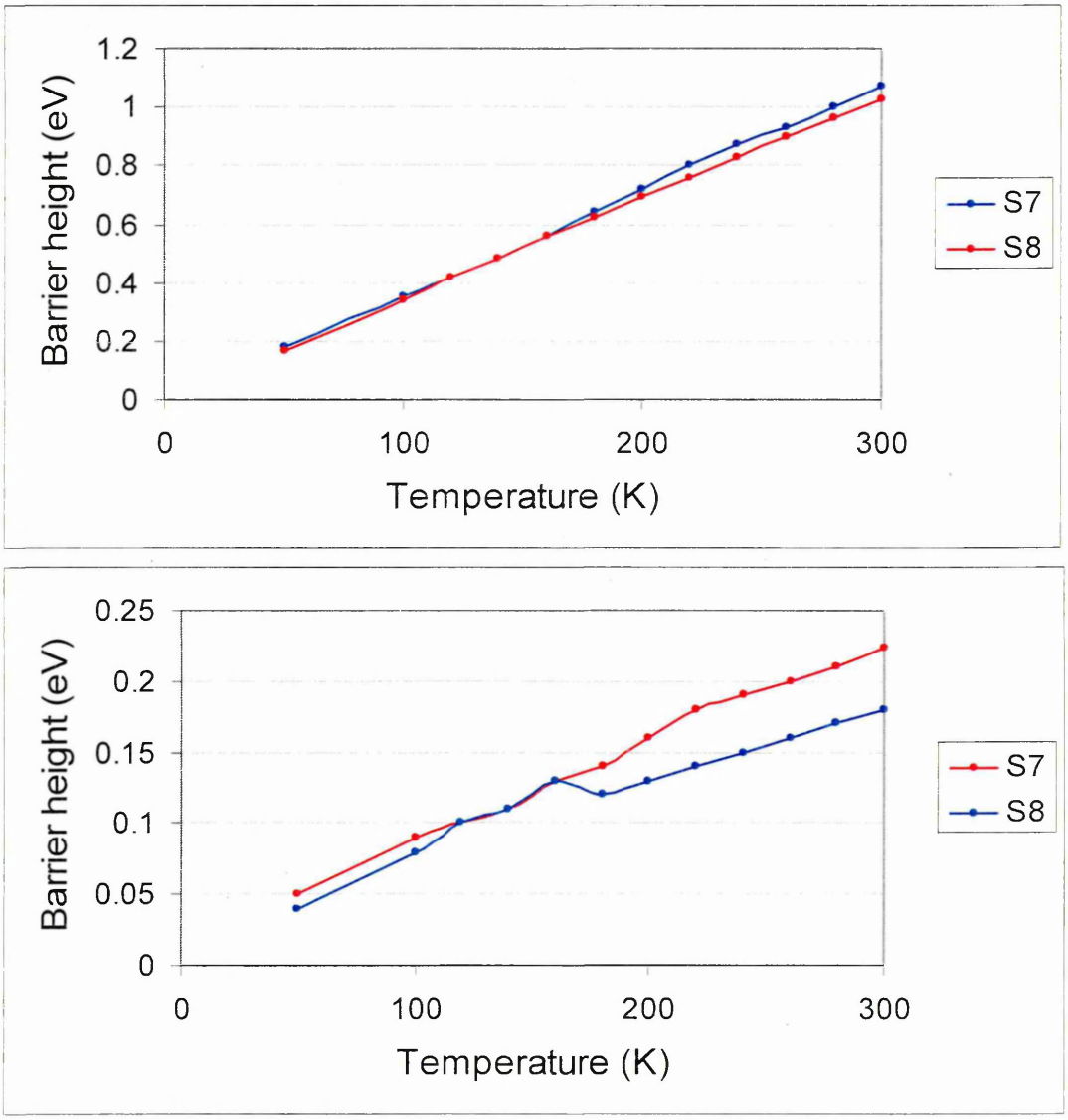

Fig. 7.7: Valence band barrier heights with temperature at the n^+-p (top) and p-p^- (bottom) depletion regions

In this case however, as the depletion region lies on the p-side, Eq. 7.1 was used to determine the Fermi level in relation to the valence band for the p-side, where N is the acceptor concentration.

$$E_F = E_i - kT\,ln(\frac{N}{n_i}) \qquad \text{Eq. 7.1}$$

For the n-side Eq. 6.1 was used with N as the donor concentration. From Fig. 7.7 it can be seen that the potential barrier at the n$^+$p depletion region at room temperature is quite large, almost approaching the bandgap of Si. This is due to the fact that both sides are quite heavily doped. The barrier height is decreasing with temperature as expected, however, even at 50K there still is a barrier of 0.2eV. The p-p$^-$ barrier height is much lower at room temperature, since both sides are p-type. In S8 the p-p$^-$ barrier height is lower than in S7, though at very low temperatures it almost disappears for both S8 and S7. Therefore contribution from both depletion regions is expected to influence the characteristics of these diodes especially at higher temperatures. At this point it would be useful to examine the band diagram of diode S8 at equilibrium. This is illustrated in Fig. 7.8.

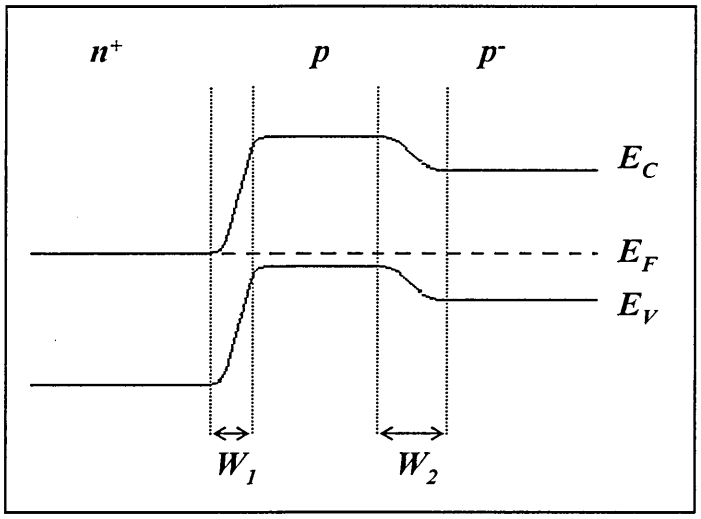

Fig. 7.8: Equilibrium band diagram of S8

In the above diagram the two depletion regions are labelled W_1 for the n$^+$p and W_2 for the p-p$^-$ junction. This notation will be used henceforth for these diodes. Using Eq. 4.2, the width of these two depletion regions in the absence of any bias was found. W_1 was found to be 37nm with a built-in bias of 1.03V and W_2 was 1.07μm with a built-in bias of 0.747V. The fact that W_2 is larger is depicted in the above diagram and leads to the conclusion that similarly to the p$^+$n diodes, the capacitance may be a combination of the

capacitances of the two depletion regions, according to Eq. 6.2. The Fermi level on the n-side is 0.008eV inside the conduction band. On the p-side the Fermi level is 0.1eV above the valence band and on the p^--side substrate it is 0.28eV above the valence band. Due to the presence of two depletion regions, measurements with normal and opposite polarity were performed for diodes S8 and S7 as in chapter 6 for the p^+n diodes.

The CV results of diode S8 at several temperatures are shown in Fig. 7.9.

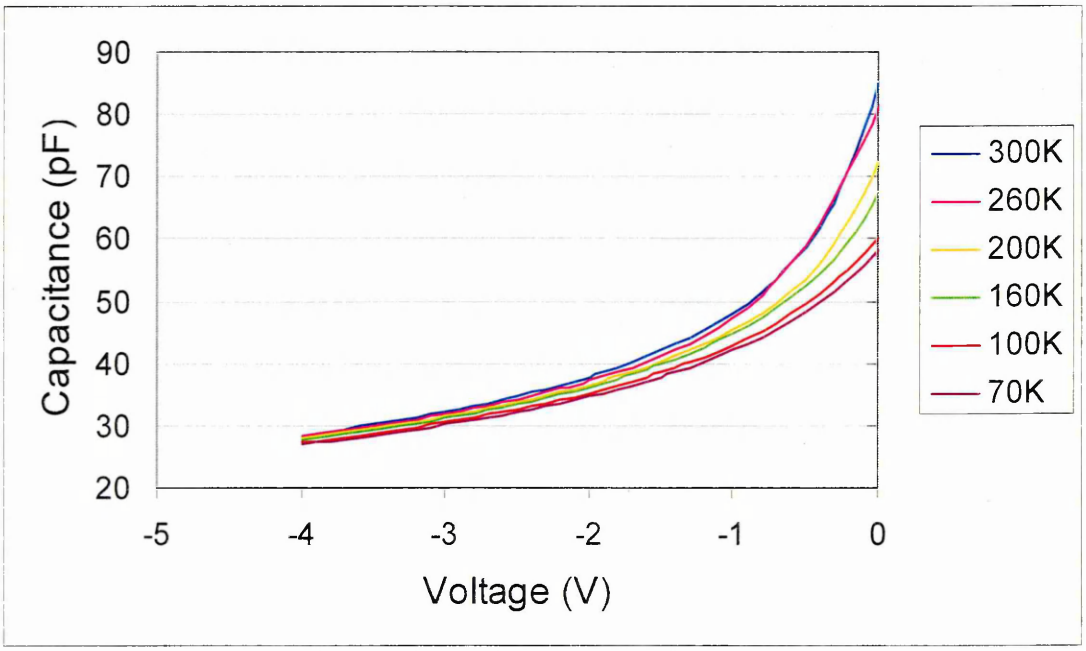

Fig. 7.9: CV characteristics of diode S8 at different temperatures

The capacitance of diode S8 is generally small and similar to that of the control diode S9. It is seen to steadily decrease as the temperature reduces, although at high reverse bias the capacitance values converge to about 30pF irrespective of the temperature. Nonetheless, the CV characteristics indicate typical diode-like behaviour and no indication of the presence of two separate depletion capacitances is apparent. Opposite polarity CV measurements were also attempted but no meaningful results were obtained and hence it is concluded that normal polarity sufficed for the characterisation of this diode. The C-T measurement of diode S8 with reverse bias -2V is shown in Fig. 7.10 in order to further investigate the dependence of the capacitance on the temperature. This characteristic reveals again a very similar behaviour to that of the reference diode S9 as the capacitance decreases almost linearly as the temperature reduces.

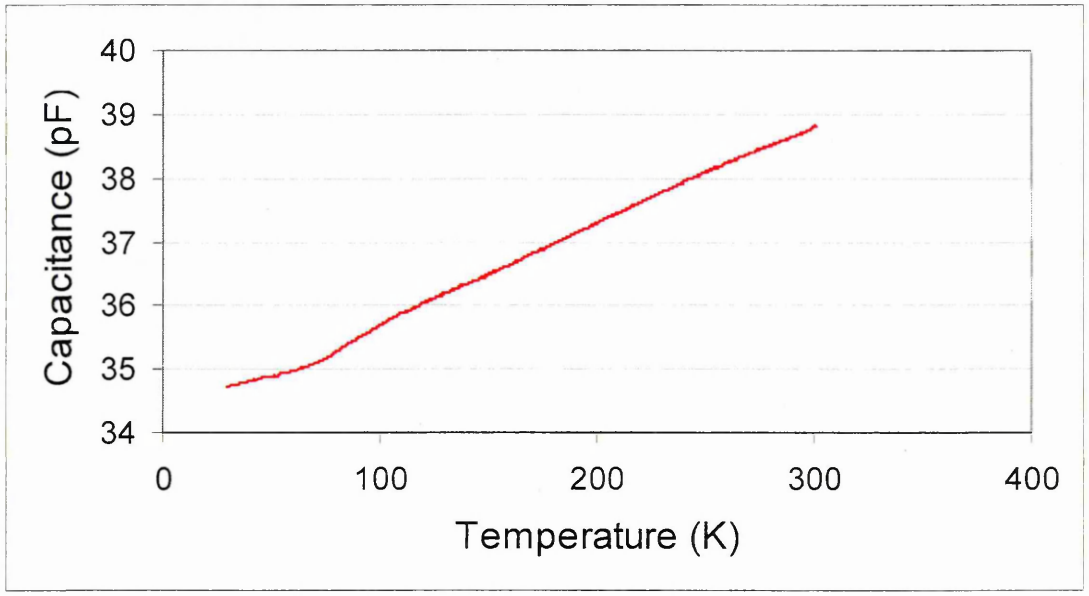

Fig. 7.10: C-T scan of diode S8 under -2V reverse bias

The carrier concentration profile of diode S8 is shown in Fig. 7.11 at different temperatures.

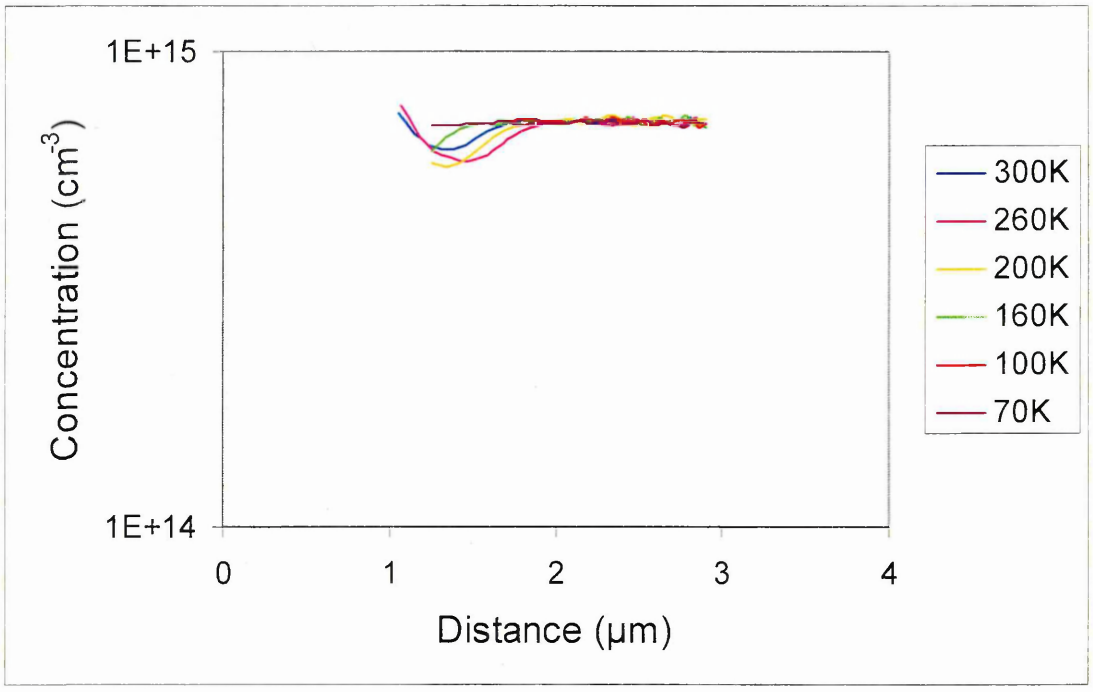

Fig. 7.11: Carrier concentration profiles of diode S8

The carrier concentration of diode S8 as seen from the above characteristics is very low and similar to that of diode S9. A value of around $7*10^{14}cm^{-3}$ is obtained from Fig. 7.11, which is almost three orders of magnitude lower than that of the SIMS profile of Fig. 5.3 (green spectrum) for this diode. This result suggests that it is not the ultra-shallow n^+p depletion region that is being measured, despite the fact that this junction should be reverse biased. As the carrier concentration is much closer to that of the p-

substrate it must be the p-p⁻ junction whose capacitance is being measured. This is also confirmed by Fig. 7.11, where a large depletion width of about 2μm is being profiled and which is located at around 1μm from the interface. This may be explained if the energy band structure of the diode under reverse bias is considered as shown in Fig. 7.12.

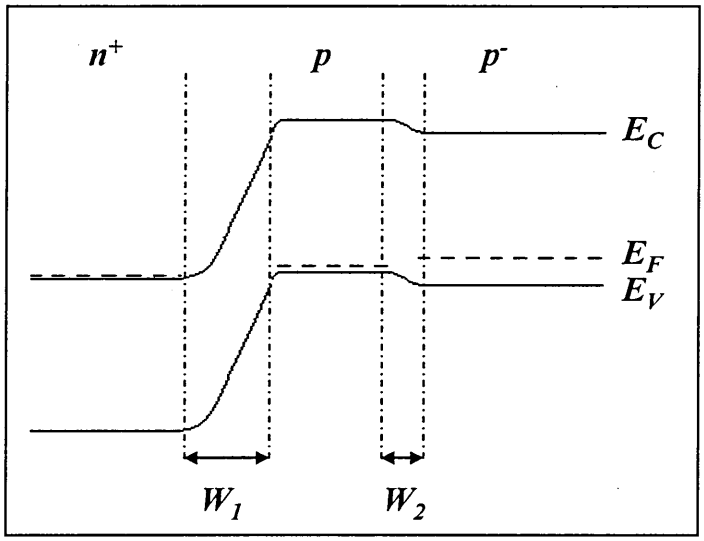

Fig. 7.12: Energy band diagram of diode S8 under reverse bias

As can be seen the n⁺p depletion region is much wider under reverse bias while at the same time the p-p⁻ depletion region has now become smaller because this junction is forward biased. It is therefore possible that the potential barrier at the p-p⁻ junction disappears and the concentrations of the two sides become uniform as holes on the p-side are swept by the electric field. However, even after the p-p⁻ junction becomes flat, the volume scanned seems to be very deep into the p-side and in particular into the substrate, if the depth and carrier concentration indicated by the N-x profiles are taken into account. In addition, the capacitance measured is very small indicating that it corresponds to a large depletion region width. Therefore DLTS measurements are most likely to detect traps due to the B end-of range implants or deeper.

The IV characteristics obtained for this diode are shown in Fig. 7.13 together with an expanded view of the reverse current at selected temperatures. The forward current reduces gradually as the temperature reduces, and has smaller magnitude than that of the reference diode S9. In addition, the reverse current seems to be small. It is 100nA at room temperature and at -4V reverse bias, then increases suddenly at 260K and then starts to gradually reduce. As it has such a small value, there is some noise

superimposed with the signal at lower temperatures. However, the sudden increase at 260K and the fact that it is even lower than that of diode S9, are apparent.

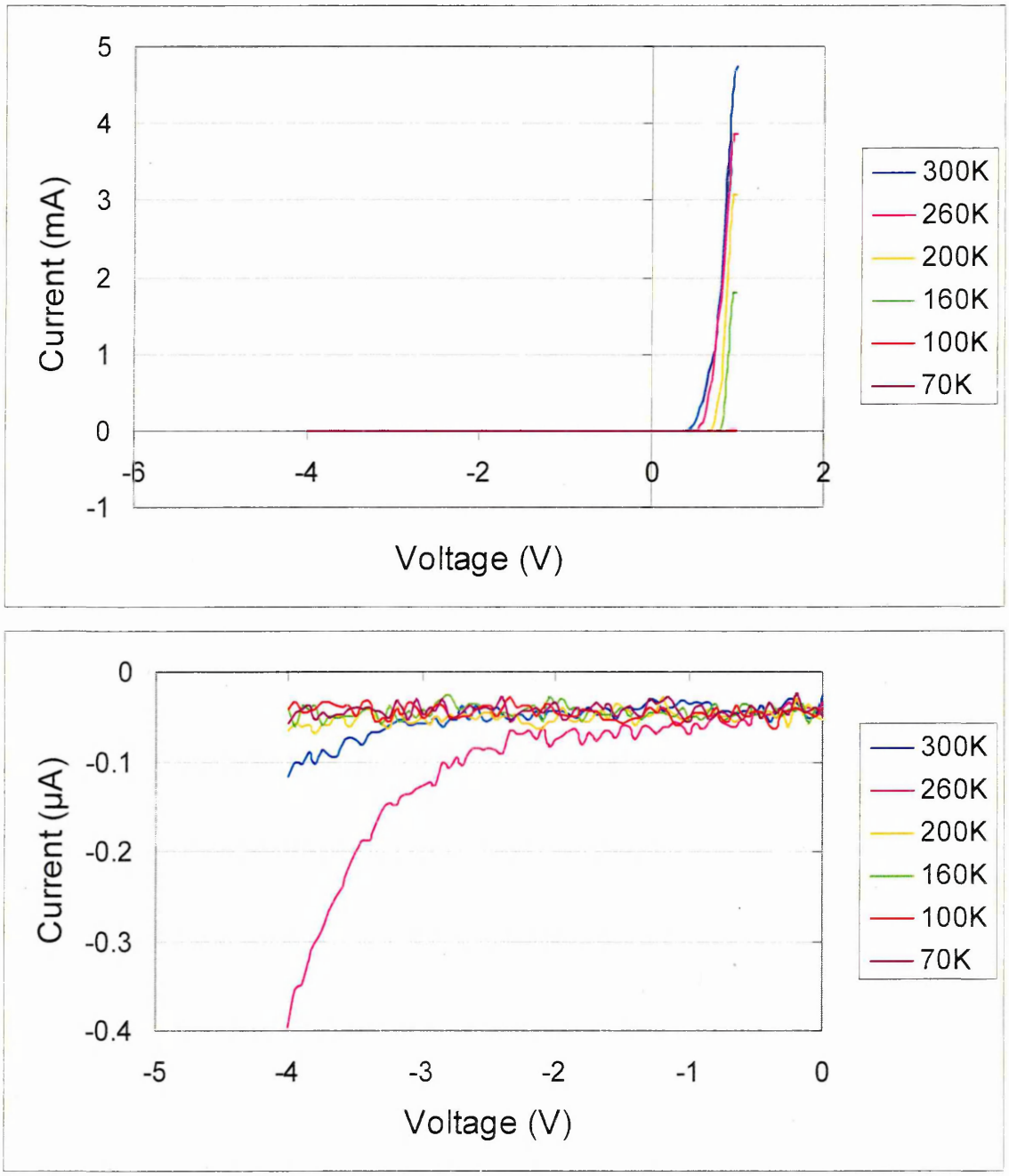

Fig. 7.13: IV characteristics of S8 at different temperatures and expanded view of the reverse current

DLTS measurements were performed on this diode with both positive and negative fill pulses and with opposite polarity. The opposite polarity and the normal polarity with negative fill pulse did not reveal any traps. This is because a negative fill pulse is only further increasing the reverse bias already applied to the diode. Deep levels were only revealed when a small or a large positive fill pulse was applied to the diode. The results with a small positive fill pulse of 0.5V are shown in Fig. 7.14.

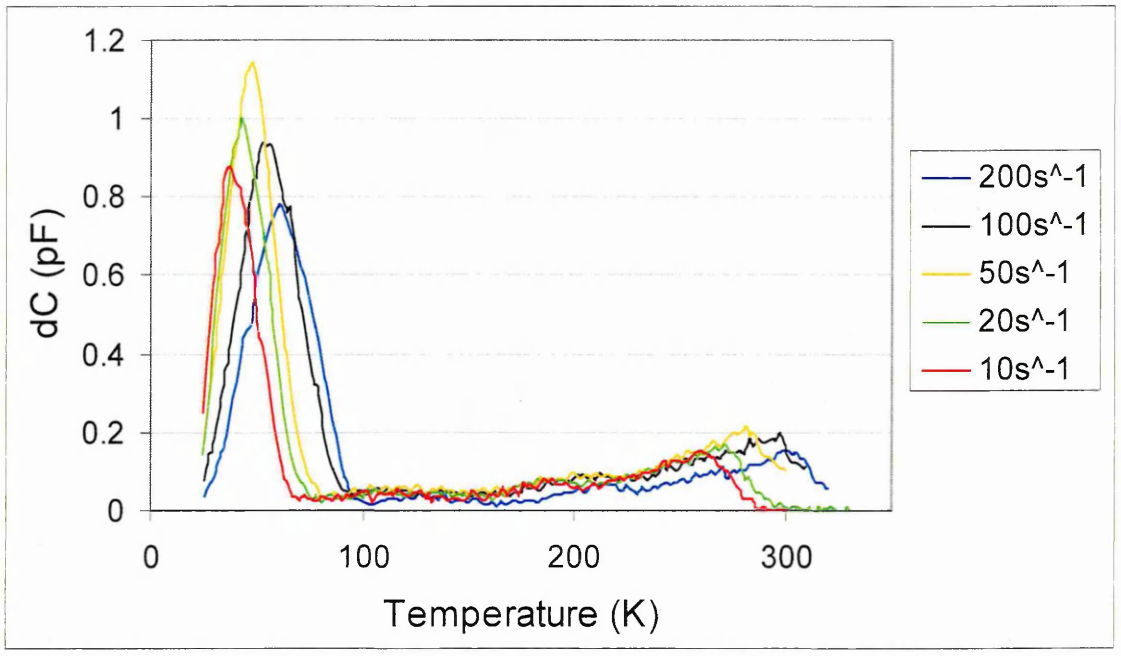

Fig. 7.14: DLTS spectra of diode S8 with reverse bias -2V and fill pulse 0.5V

The small positive fill pulse has the effect of reducing the reverse bias of the diode and introducing majority carriers (holes) into the depletion region. This is true irrespective of which depletion region or depth of the p-side is being profiled. Hence it is most likely to observe majority (hole) traps with such a pulse as confirmed from the Fig. 7.14. A broad spectrum of peaks that possibly covers more than one defect is detected at high temperatures around 300K and a narrower but larger peak is revealed at about 50K. Measurements with different small positive fill pulses (i.e. 0.1V) verified the presence of the broad peak at high temperatures although the peak at 50K was not always present. As this peak appears at a very low temperature where dopant ionisation is reduced, the presence of this peak and of such magnitude is unexpected. Therefore it will not be considered further because its activation energy (18meV) is very small and within the experimental error range of ± 50meV of DLTS. The broad peak around 280K has a very long shoulder extending towards lower temperatures, suggesting the presence of multiple defects, which is consistent with the typical DLTS spectra observed from implanted p-type Si [1]. The Arrhenius plot for this trap is shown in Fig. 7.15. The activation energy of the peak at around 280K was found to be 0.4eV above the valence band, since this majority carrier emission is on the p-side. Comparing with literature this may be due to an interstitial complex that embodies B, although its activation energy is somewhat lower than expected (0.45eV). This is most likely due to the fact that DLTS is measuring the combined emission of more than one level [1]. In

addition, the assignment of this trap to an interstitial complex is more accurate as the interstitial population is expected to be deeper into the implanted region than that of vacancies in particular if transient enhanced diffusion of B is involved [2, 3].

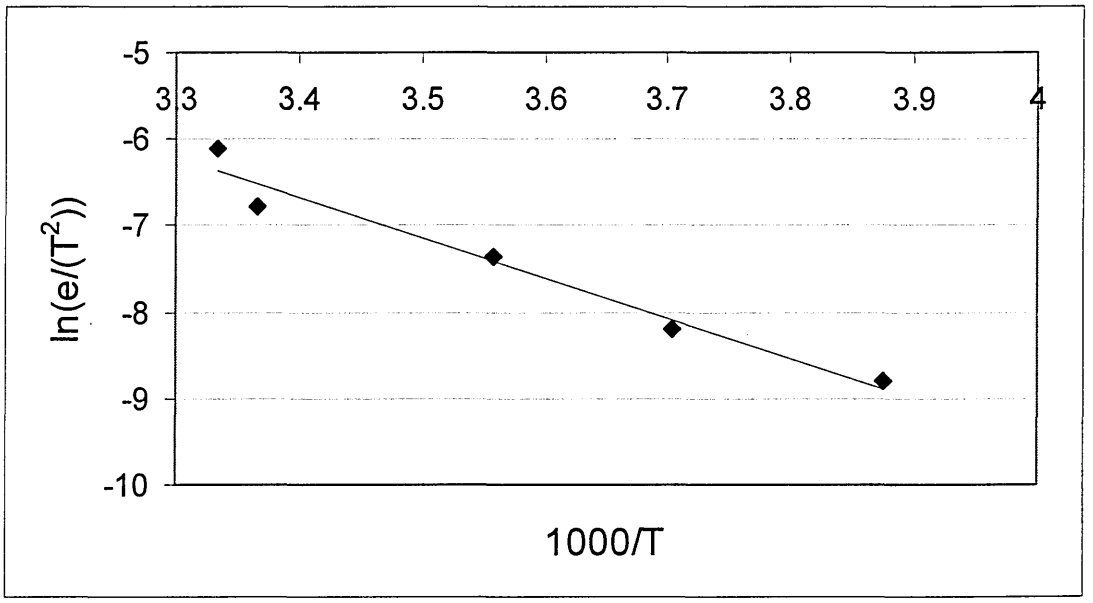

Fig. 7.15: Arrhenius plot of the peak at ~280K of the DLTS spectrum of S8 obtained with a fill pulse of 0.5V

When a larger positive fill pulse is applied to the diode the initial reverse bias is sufficiently reduced and electrons are being pushed away from the n^+ contact and into the depletion region. If the fill pulse is large enough, usually of the same value as the reverse bias, the diode momentarily operates in forward bias for the duration of the pulse and hence both majority and minority carriers are being injected into the depletion region. It is therefore possible to detect a minority carrier trap under the application of a large positive fill pulse since its occupation momentarily increases, while a minority transient is associated with the return of the trap's occupation to equilibrium. This is confirmed by the DLTS spectra of Fig. 7.16 where a minority carrier trap was observed for a large positive fill pulse of 2V with reverse bias of -2V. Only one rate window is shown here for clarity as the signal is slightly noisy. However, the minority trap is clear and the existence of the trap was confirmed by further scans with the same biasing conditions. Moreover a larger positive fill pulse of 3V yielded the same minority carrier trap. Since this minority carrier trap is on the p-side it is suggested that it is an electron trap. Activation energy calculations were possible, although not very accurate due to the high noise levels. The Arrhenius plot of this trap is shown in Fig. 7.17.

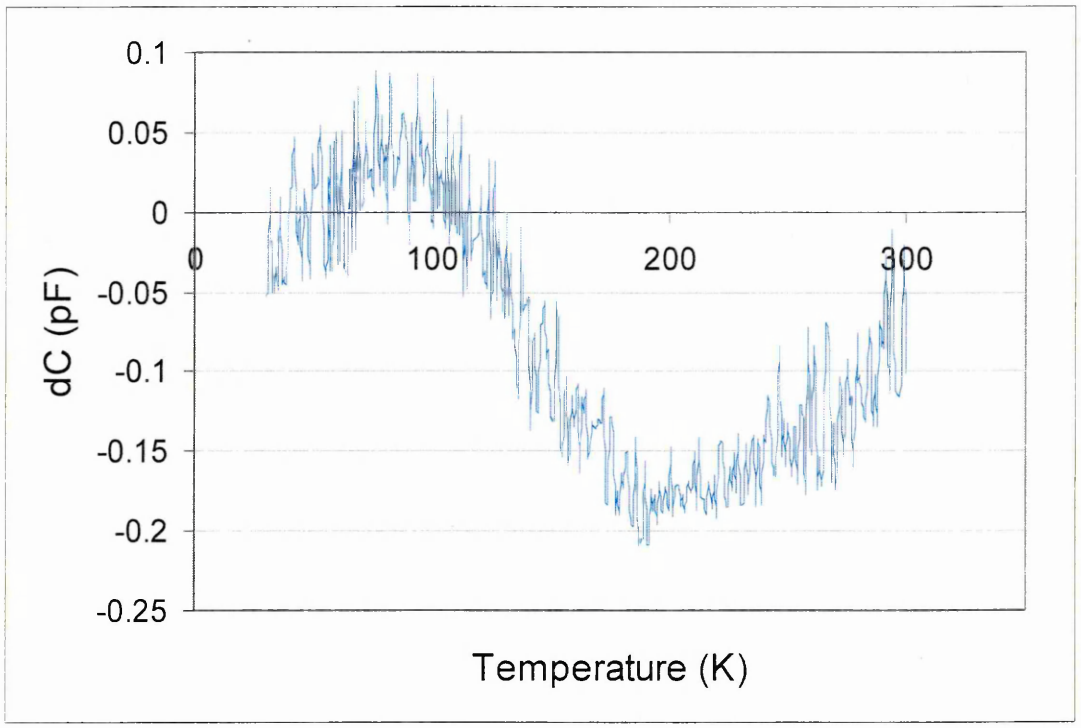

Fig. 7.16: DLTS spectra of diode S8 with large positive fill pulse 2V, reverse bias -2V and with rate window $200s^{-1}$

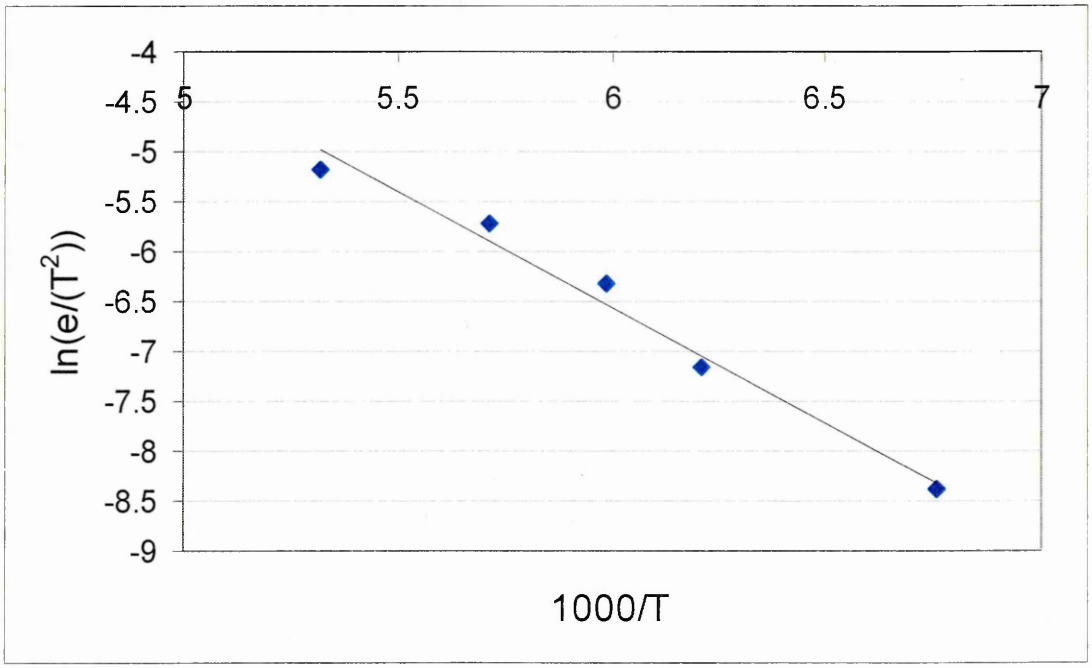

Fig. 7.17: Arrhenius plot for diode S8 from DLTS with large positive fill pulse of 2V

The Arrhenius plot of Fig. 7.17 yielded an activation energy of 0.2eV and since this emission is due to an electron trap it is hence located at 0.2eV below the conduction band. To further investigate the origin of this electron trap LDLTS has to be applied since as an electron trap in the p-side it is difficult to identify.

LDLTS was performed at a range of temperatures around the peak temperatures of the DLTS traps, both for the case of the small and the large positive fill pulse. These results are shown respectively in Fig. 7.18 and 7.19.

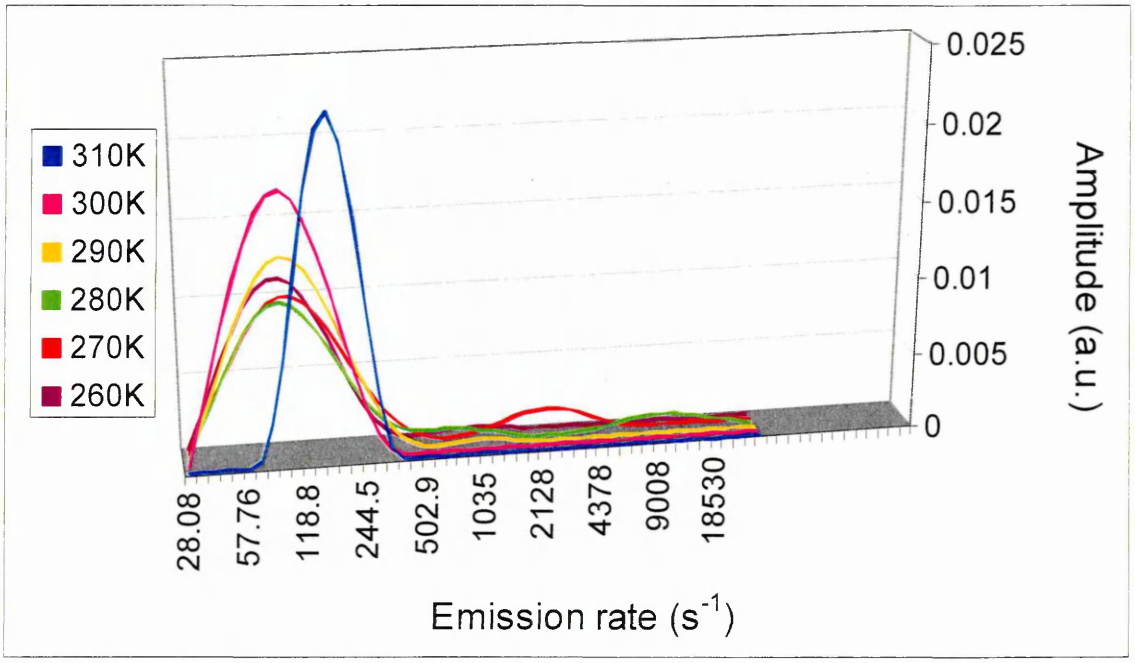

Fig. 7.18: LDLTS results for S8 of the broad hole trap around 280K of Fig. 7.14 obtained with a small positive fill pulse

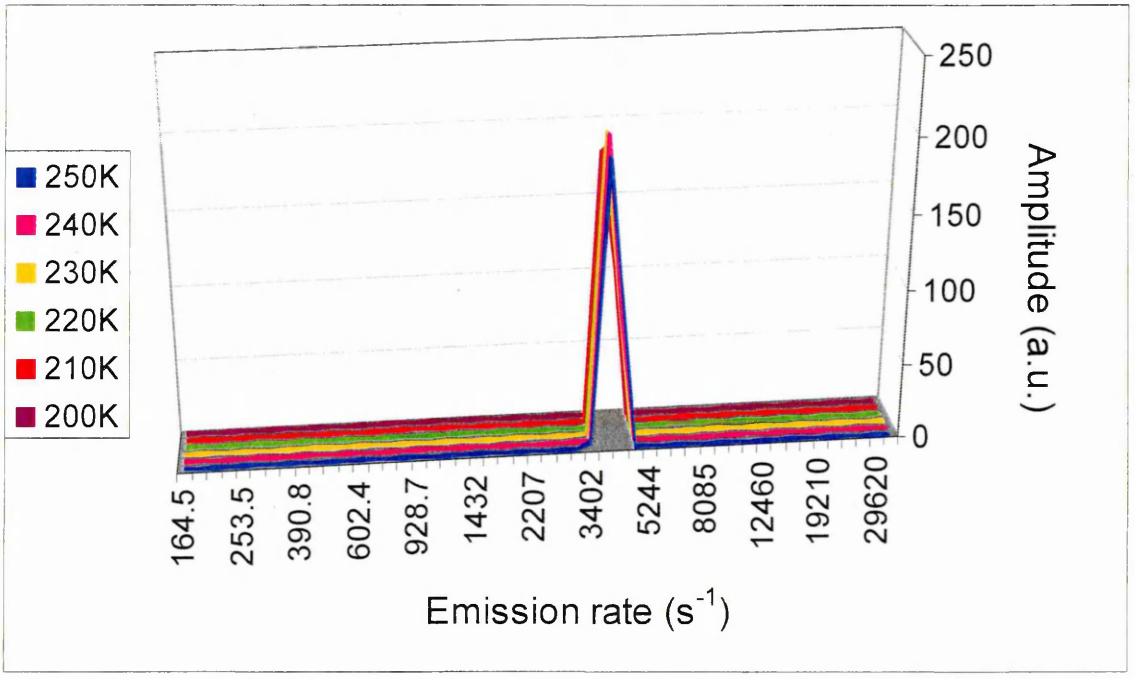

Fig. 7.19: LDLTS spectra for diode S8 of the minority trap of Fig. 7.16 obtained with a large positive fill pulse of 2V

Fig 7.18 shows that at the temperature range of 260-300K two defects are detected by LDLTS. The low emission rate defect has higher intensity and its emission is centred

below $100s^{-1}$, while the higher emission level has very scattered emission usually above $1000s^{-1}$. A majority transient was obtained for all these scans confirming that these are due to hole traps. The emission rate from these levels however, did not consistently decrease as the temperature decreased. Therefore it was not possible to construct Arrhenius plots from LDLTS and calculate the activation energies of these levels, despite the fact that their peak height changes with temperature. In addition, the signal obtained was small as can be verified from the amplitude of the LDLTS peaks indicating a low concentration of these defects. However, the fact that more than one levels were resolved with LDLTS at this temperature range, is in agreement with the DLTS assignment to a complex of defects.

The LDLTS spectra of Fig. 7.19 were obtained at each temperature from a minority carrier transient for a large positive fill pulse. One emission rate is present at $\sim 4000s^{-1}$, which is almost identical for all the measurements irrespective of the temperature change. The fact that the emission rate of this minority carrier trap does not change at all with temperature indicates that this is not a point defect but the observed emission is possibly due to an extended defect. Therefore the nature of this electron trap cannot be identified by these measurements and the activation energy obtained from DLTS cannot be verified.

7.4 Diode S7

Diode S7 has the same As implant as the previously examined n^+p diodes but the B implantation dose was more than twice that of S8. The SIMS profile of Fig. 5.3 yields a B doping of about $5*10^{18}cm^{-3}$ at the interface with the n^+-side. Hence both the n^+p and $p\text{-}p^-$ depletion region potential barriers are expected to be larger. From Eq. 4.2 the n^+p depletion region width is expected to be smaller than that of S8 in the absence of bias and the width of the $p\text{-}p^-$ depletion region is expected to be larger. Therefore in this diode there will be a capacitance contribution from both depletion regions with the smallest capacitance dominating according to Eq. 6.2. Consequently opposite polarity measurements may be necessary for the characterisation of S7. Fig. 7.20 illustrates the equilibrium band diagram for this diode.

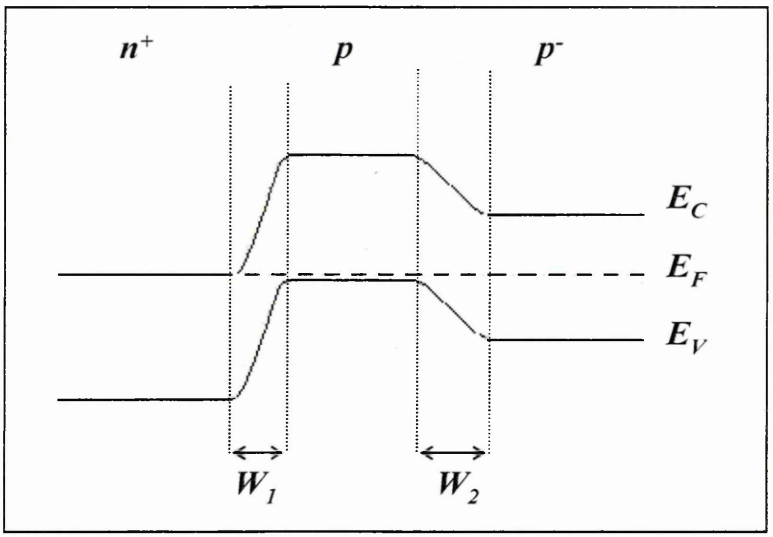

Fig. 7.20: Equilibrium band diagram of S7

The p-side on the above diagram is heavily doped and calculations revealed that the Fermi level is located 0.056eV above the valence band, while in diode S8 it was at 0.1eV above the valence band. To accommodate this difference the potential barrier of the depletion regions has now increased. The CV and N-x characteristics obtained for this diode with the normal polarity configuration at different temperatures are shown in Fig. 7.21 and 7.22 respectively.

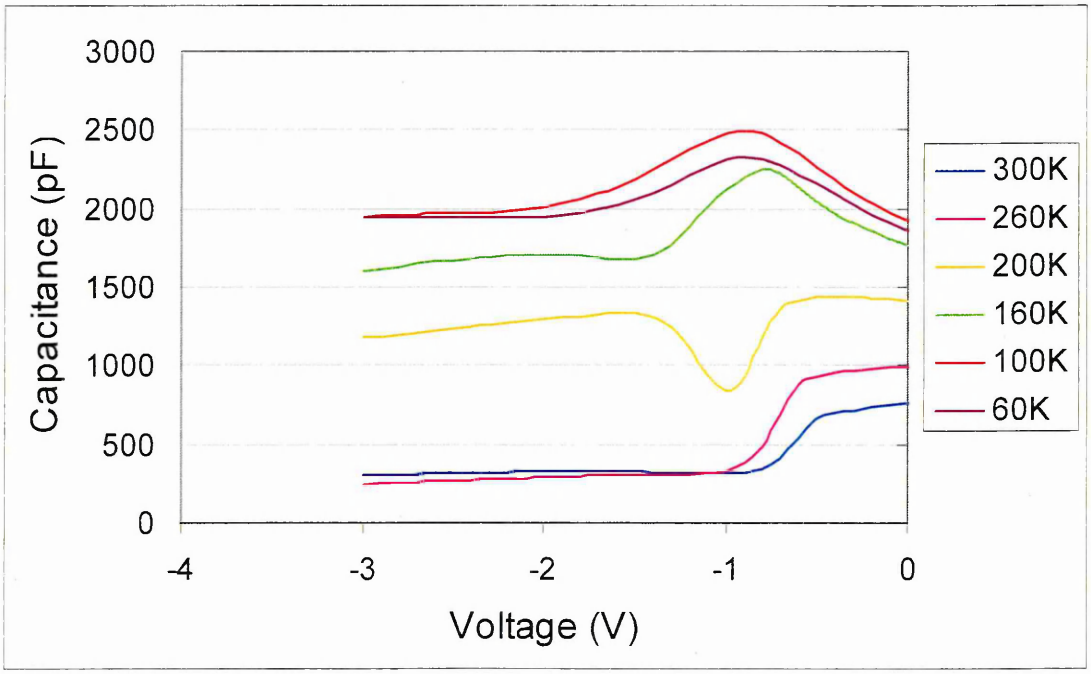

Fig. 7.21: CV characteristics of diode S7 under the normal polarity configuration at different temperatures

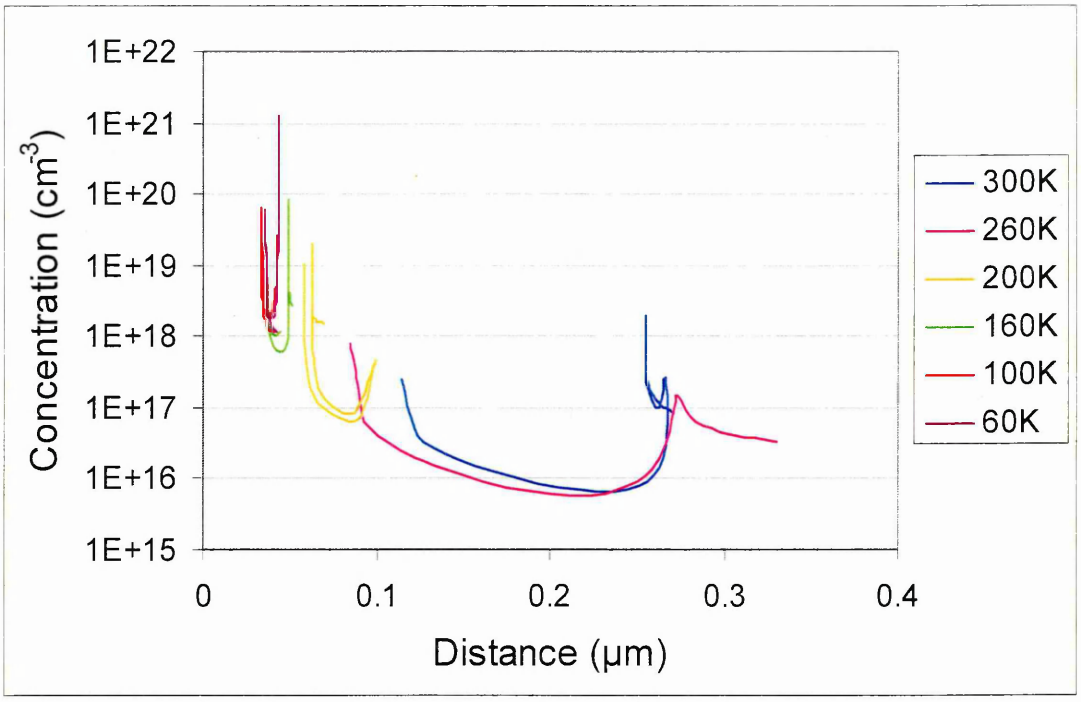

Fig. 7.22: N-x characteristics of diode S7 with normal polarity at different temperatures

The CV characteristics of Fig. 7.21 exhibit very large capacitance compared to that of diodes S8 and S9. In addition, as the temperature decreases the capacitance is increasing until the temperature of 100K. The CV plots do not resemble those of a normal diode and this is the result of the total capacitance being a combination of the capacitances of the two depletion regions that exist in this diode. From the temperature of 300K down to 200K the capacitance initially decreases slowly and at about a reverse bias of -1V it starts increasing again. The opposite happens at temperatures below 200K. The capacitance is significantly increasing until the bias reaches about -0.8V and below this bias the capacitance is decreasing. The N-x characteristics are equally complex since the concentration appears to be increasing as the temperature reduces and at each temperature the concentration exhibits an irregular behaviour. The carrier concentration cannot be extracted from these measurements since the N-x characteristics vary with applied bias in such a complicated manner. Hence it is more accurate to use the doping concentration as indicated by the SIMS profile for this diode for calculations of depletion region width. The profiled volume, as suggested by the N-x plots lies about 0.1µm from the interface. Although the n^+p depletion region is reverse biased with normal polarity and this junction should be profiled by the CV measurements, it is clear that both capacitances contribute to the CV characteristics and hence it is not possible as yet to determine where the profiled volume lies. As the $p\text{-}p^-$ depletion region is forward biased with normal polarity its depletion region width

should be reducing. Thus its capacitance should be increasing and perhaps the peculiar CV characteristics can be attributed to the fact that the capacitance of this depletion region increases sufficiently to become comparable to that of the ultra-shallow n^+p depletion region. In order to illustrate the behaviour of the total measured capacitance of diode S7 with temperature Fig. 7.23 shows the C-T scan for this diode with an applied reverse bias of -3V.

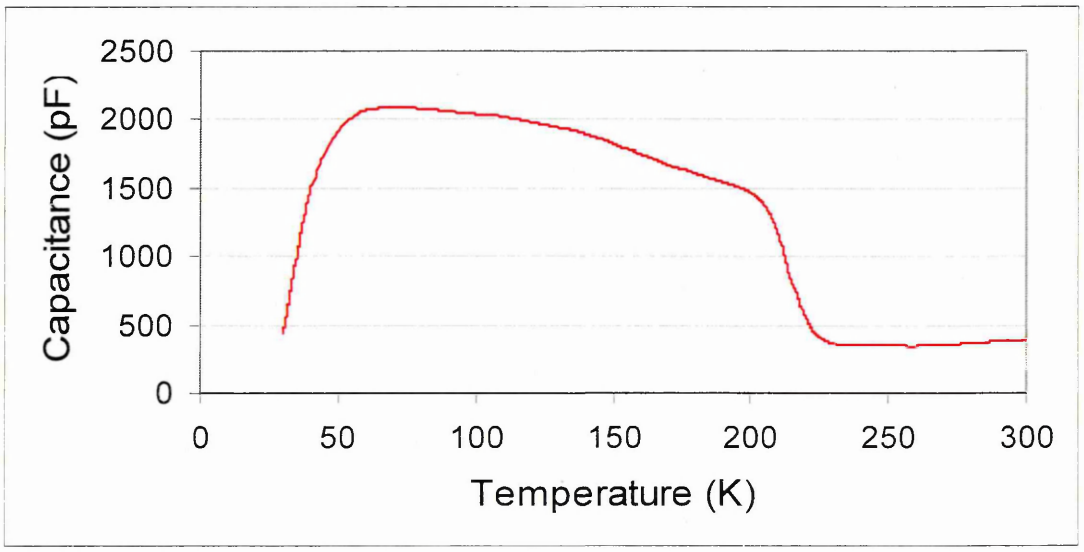

Fig. 7.23: C-T scan of diode S7 under reverse bias of -3V

Fig. 7.23 shows that the measured capacitance of the diode decreases initially from 300K as the temperature reduces to about 230K, then suddenly starts to increase and continues increasing until the very low temperature of 60K, similarly to the p^+n diodes of the previous chapter. The band diagram of S7 with normal polarity is shown in Fig. 7.24 in order to facilitate analysis of the results with this configuration.

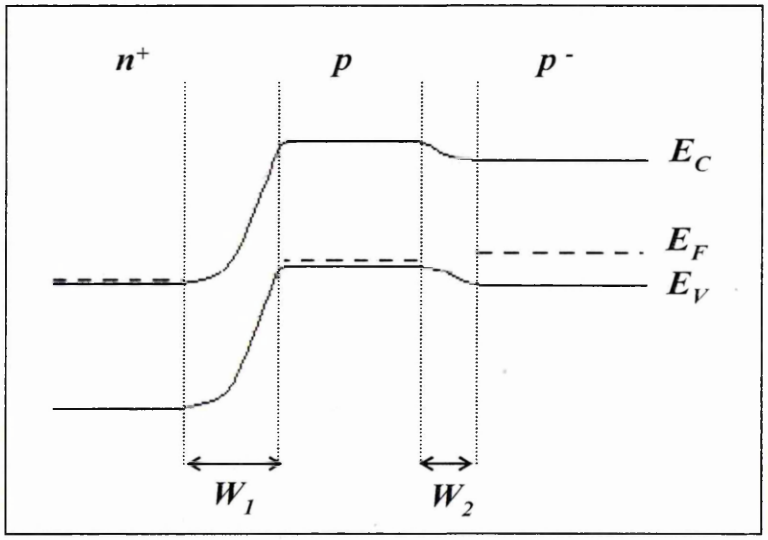

Fig. 7.24: Calculated energy band diagram of S7 with normal polarity, showing the relative positions of the conduction and valence bands in all three regions

In this normal polarity configuration the n^+p depletion region is reverse biased, which means that its width has increased and the $p\text{-}p^-$ depletion region is forward biased and hence W_2 is now smaller than in equilibrium. It is best to examine the diode under a small reverse bias with normal polarity in order to investigate the influence of both depletion regions on the diode characteristics, before the $p\text{-}p^-$ depletion region becomes flat under a large forward bias. The built-in voltage V_{bi1} of junction 1 was found to be 1.07V and V_{bi2} was 0.788V. The sudden capacitance decrease of the CV characteristics at a bias of about 0.7V can be attributed to the fact that the barrier at the $p\text{-}p^-$ junction is becoming flat at this bias, since the forward bias is comparable to V_{bi2}. As the temperature reduces, the built-in voltage, which is strongly dependent on the intrinsic carrier concentration, increases slightly and this is the reason the $p\text{-}p^-$ depletion region does not disappear until slightly higher bias.

As the reverse bias increases further than 1V, there is another increase in capacitance although the only depletion region in the diode now should be at the n^+p interface. An increase in capacitance entails a decrease in depletion region width which in turn would involve a sudden increase in the carrier concentration. The N-x profile suggests that this is taking place at about 0.1μm from the n^+p interface with the value of this depth decreasing with temperature. The SIMS profile for this diode in Fig. 5.3 shows that at the n^+p junction, the B concentration is not flat but exhibits a valley-like characteristic for about 100nm and then the concentration increases slightly again. Hence the strange N-x profile that exhibits a sudden increase at the end of the measured depletion region may reflect this change in carrier concentration.

CV and N-x characteristics were also measured with opposite polarity. These are displayed in Fig. 7.25. The CV plots with opposite polarity also indicate the presence of two depletion capacitances in series although the CV profiles appear less complicated. Once again the capacitance at zero bias increases as the temperature decreases which is the opposite from what is expected from a typical diode. As the temperature reduces below 200K however, the capacitance reduces with bias in a more diode-like fashion. This can also be observed from the N-x characteristics where from 300-200K the carrier concentration of the profiled volume appears to decrease very abruptly with bias, while below 200K the carrier concentration is stable $\sim 2*10^{18}cm^{-3}$. In addition this value is much closer to that of the SIMS profile ($\sim 5*10^{18}cm^{-3}$). The depth profiled according to

the N-x profiles is comparable to that with normal polarity at ~0.1μm from the interface and reducing with temperature, although the width of the depletion region is narrower with opposite polarity. With the latter configuration the CV and N-x characteristics appear more reasonable especially as the temperature reduces below 200K. Again however, the contribution of both depletion regions is obvious and carrier concentration values closer to the doping content of the SIMS profile would be more accurate for calculation of depletion region widths and potential barrier heights at the two depletion regions.

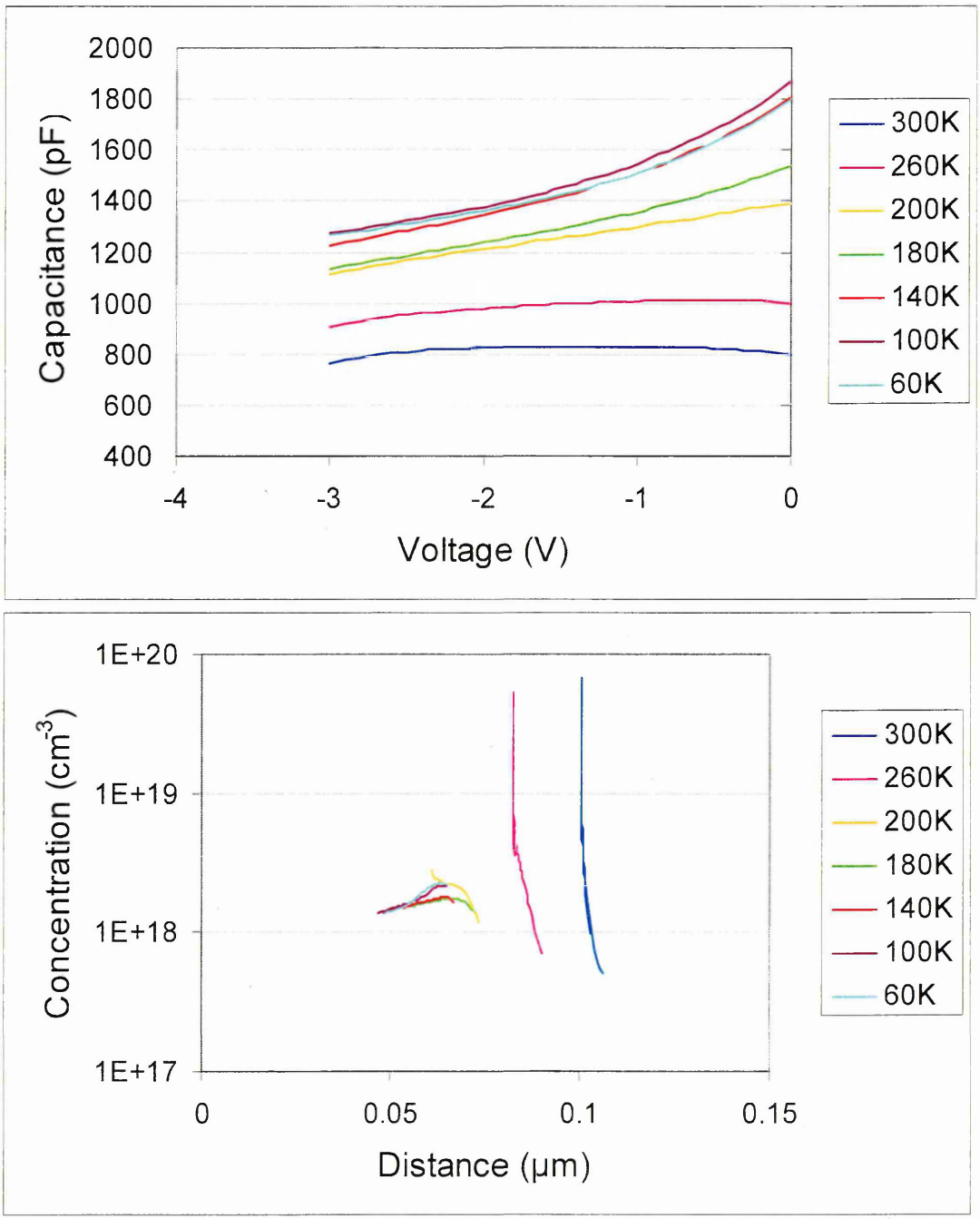

Fig. 7.25: CV and N-x profiles for diode S7 at different temperatures with opposite polarity

The band diagram of diode S7 with opposite polarity is shown in Fig, 7.26 for a small forward bias applied to the diode.

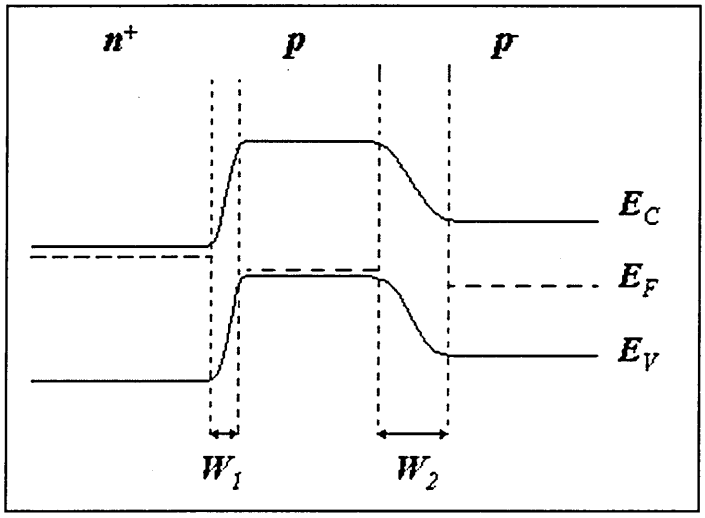

Fig. 7.26: Energy band diagram of S7 with opposite polarity under a small forward bias

With opposite polarity the n^+p depletion region is forward biased and therefore W_1 will be smaller than in equilibrium. In contrast, the $p\text{-}p^-$ depletion region is now reverse biased and its depletion width has increased even more. Before the applied bias reaches the V_{bi} value of 1.07V, a combination of the capacitance of both depletion regions is being measured. However, when the n^+p barrier becomes very small, under a large forward bias, there may be electron injection over the barrier into the p-side as the Fermi level on the n-side is slightly within the conduction band. Moreover since the width of the n^+p depletion region is extremely small it is possible that electrons can tunnel towards the valence band on the p-side or to energy levels in the bandgap. Table 7.1 shows the results of calculated depletion region widths at different voltages for normal and opposite polarity measurements at room temperature.

Normal Polarity		
Bias (V)	**W_1 (nm)**	**W_2 (μm)**
0	17	1.1
-0.5	20	0.668
-0.78	22	0.11
-1.0	23	
-3	33	
Opposite Polarity		
Bias (V)	**W_1 (nm)**	**W_2 (μm)**
0.5	12	1.4
1.0	4	1.66
3		2.4

Table 7.1: Calculated depletion region widths for n^+p and $p\text{-}p^-$ depletion regions with normal and opposite polarity

From the above results it can be seen that there is a large difference in the depletion region widths of the two space charge regions. Only in the case of normal polarity and just before the potential barrier at the p-p⁻ junction becomes flat it can be seen that W_2 is five times bigger than W_1. As this takes place at a reverse bias of around 0.7V, the change of the CV characteristics at this bias can now be attributed to the fact that the two capacitances are of comparable magnitude only when the bias reaches -0.7V.

Fig. 7.27 shows the IV characteristics for diode S7 with an expanded view of the reverse current as the inset as selected temperatures and the breakdown voltage with temperature at 10μA.

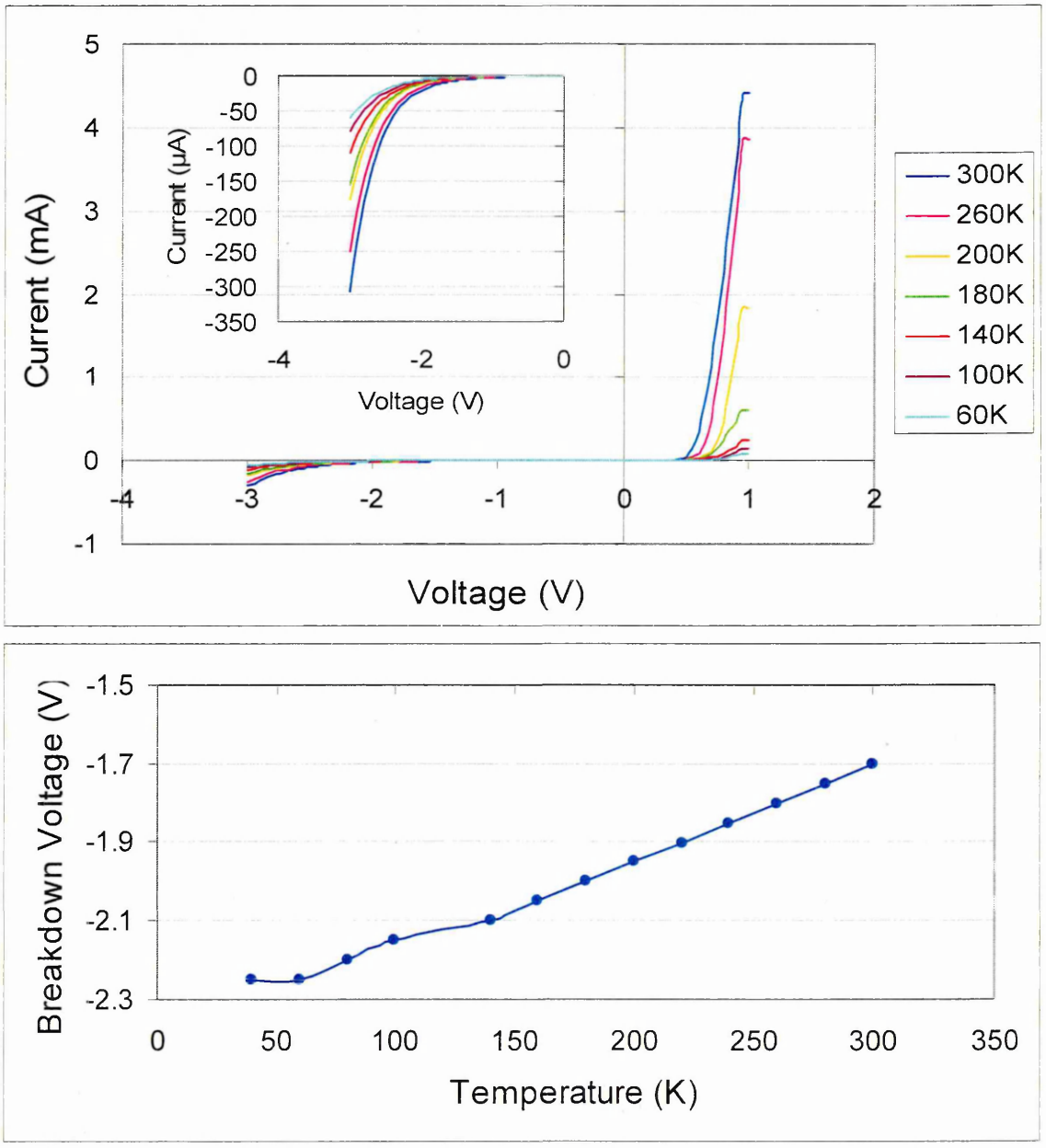

Fig. 7.27: IV characteristics of diode S7 and breakdown voltage at 10μA. The inset shows the reverse current

In Fig. 7.27 the forward current is steadily decreasing as the temperature reduces. The reverse current characteristics display a lot of leakage current which is large at room temperature but once again steadily decreases as the temperature reduces. However it can be seen that even at the lowest temperature of 60K there still is 60μA leakage current at -3V. This suggests that there is tunneling which can be confirmed by inspection of Fig. 7.24 where it can be seen that the top of the valence band on the p-side is in fact at a higher potential than the conduction band bottom on the n^+-side. In addition, since the n^+p depletion region is reverse biased and the bandgap has narrowed there may be tunnelling of electrons towards the top of the valence band on the p-side. The breakdown voltage increases in value as the temperature reduces which also confirms that tunnelling is taking place and results in a high leakage current.

DLTS measurements were performed on diode S7 with both normal and opposite polarity. With normal polarity and a positive fill pulse, majority carrier traps were revealed. This is because a positive fill pulse lowers the diode bias and injects majority carriers (holes) in the reverse biased depletion region. When the n^+p depletion region is forward biased, electrons are injected into the p-side, driven by the field, and they can be captured by an electron trap. This can either be achieved under normal polarity conditions by keeping the diode under small reverse bias and applying a large forward fill pulse, or in these diodes where two depletion regions are present, by using opposite polarity and applying a positive fill pulse. Fig. 7.28 shows the DLTS spectra obtained with reverse bias -2V and 2V fill pulse.

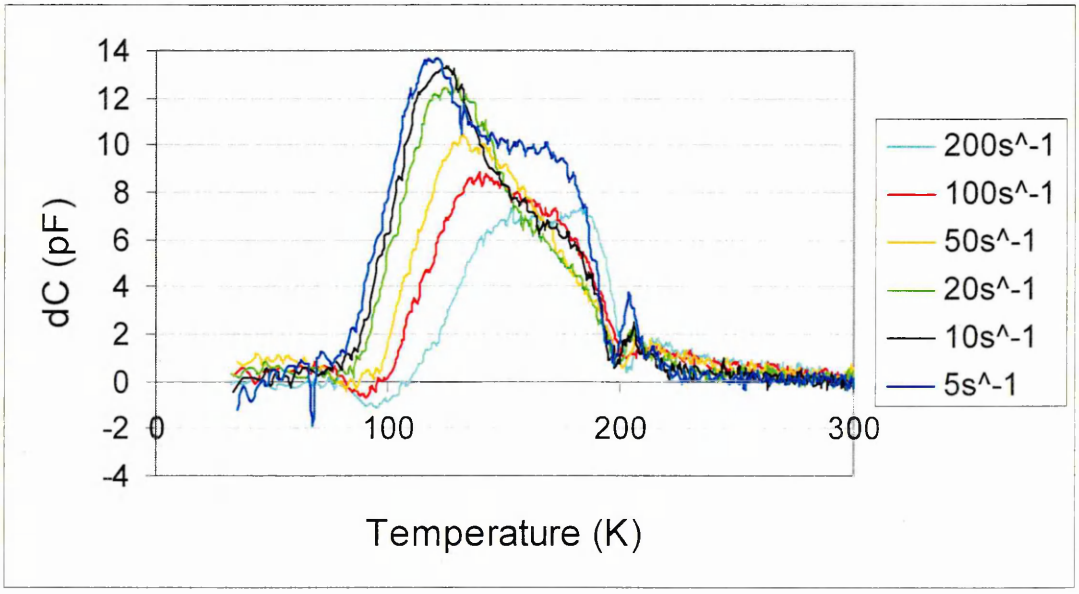

Fig. 7.28: DLTS spectra for S7 with normal polarity-2V reverse bias and 2V fill pulse

The DLTS spectra with normal polarity reveal a multitude of defects within the temperature range from 230K to 70K. It's worth noticing that this temperature range coincides with the large increase in capacitance observed by the C-T measurements. However, the defects appear very closely spaced and DLTS cannot resolve their peak emission with temperature consistently at all rate windows. It can also be observed that as the rate window reduces the magnitude of the peaks increases. There are two relatively more distinct peaks below 200K. The peak of these levels appears at lower temperatures for reduced rate windows and hence their activation energy can be found. The Arrhenius plots of these two peaks are shown in Fig. 7.29.

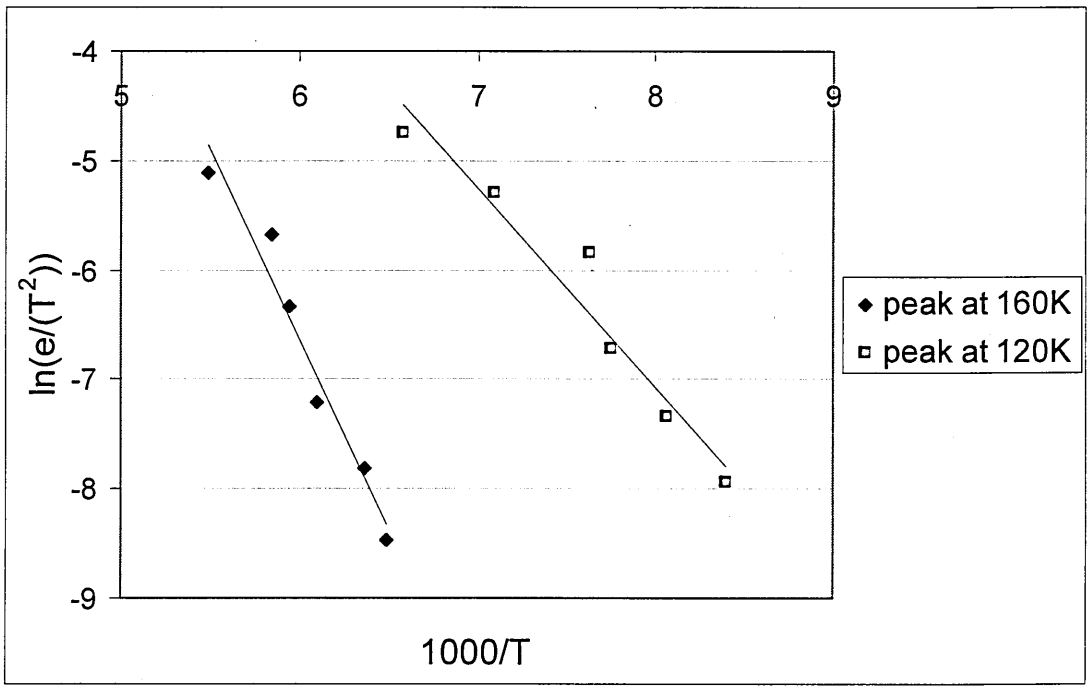

Fig. 7.29: Arrhenius plots of the two peaks revealed by DLTS with reverse bias -2V and fill pulse 2V

The activation energy of the peak at 120K was found to be 0.16eV while that of the peak at 160K is 0.3eV. DLTS was also performed with different positive fill pulse biases between 0.5-2V in an effort to separate these two peaks but this was not possible and especially not for enough rate windows in order to allow construction of a more accurate Arrhenius plot. However, some of these scans revealed three peaks at rate windows of $50s^{-1}$ or lower. This is a reasonable result as the temperature range of 230-70K is very broad and in particular in p-type Si is known to contain several defect levels [1, 4, 5]. As the peaks of some of these levels may be overlapping, the activation energies of Fig. 7.29 may be due to a combination of emission from these defects. For instance the activation energy of 0.3eV for the peak at 160K is most likely due to a defect containing carbon, as it is located between the energy range of the carbon-oxygen

and the boron interstitial-carbon substitutional complexes above the valence band [1]. Therefore higher resolution measurements may yield more accurate results about this level.

DLTS was also performed with opposite polarity, as already mentioned, in order to provide information on any electron traps present. The DLTS spectra obtained with opposite polarity, reverse bias -2V and fill pulse 1V are shown in Fig. 7.30 for different rate windows.

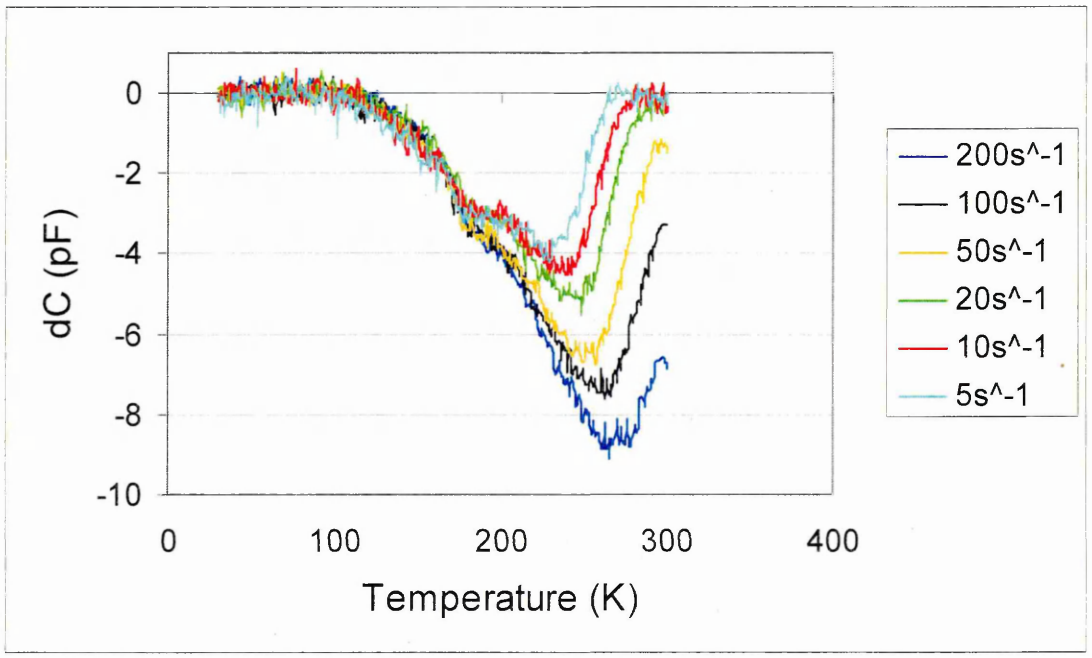

Fig. 7.30: DLTS spectra of diode S7 with opposite polarity, reverse bias -2V and fill pulse 1V

Opposite polarity measurements revealed minority carrier traps resulting from a minority capacitance transient as expected. A broad temperature range from 150-300K is covered by this peak which is possibly indicative of the presence of more than one defects. In addition, the peak of the main trap reduces in temperature for lower rate windows although only the high temperature side of the trap shifts to lower temperatures. The main peak at 260K is more prominent, while the peak at around 170K is more discernible at low rate windows and hence its activation energy could not be accurately determined. Fig. 7.31 shows the Arrhenius plot of the peak at 260K. The Arrhenius plot for this minority peak yielded an activation energy of 0.48eV. As the depletion region width at the n^+p junction is very small with opposite polarity, even before the potential barrier at the n^+p junction collapses, and only 1/11 part lies in the n^+-side, this minority trap cannot be a hole trap on the n^+-side. Hence it is an electron

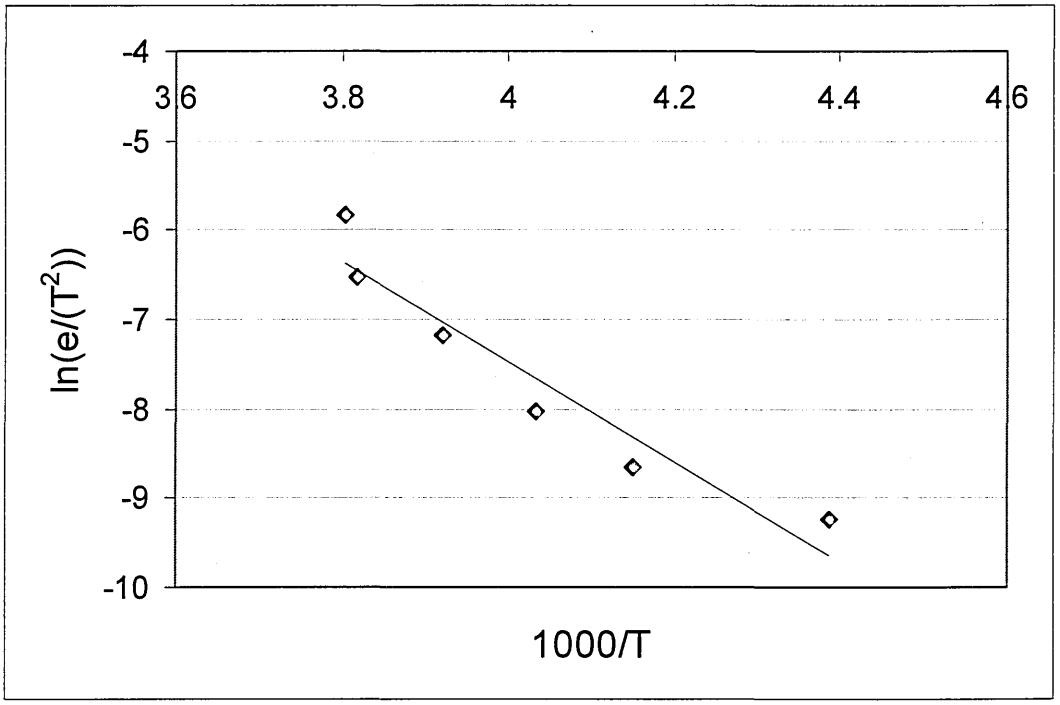

Fig. 7.31: Arrhenius plot of minority trap at 260K detected by DLTS with opposite polarity for diode S7

trap on the p-side and if the depth indicated by the N-x profile with opposite polarity is considered, the volume scanned is within 100nm from the n^+p interface since at a fill pulse of 1V the n^+p depletion barrier is most likely not entirely flat. Therefore this electron trap might arise from As implantation damage. It is therefore attributed to the vacancy-arsenic level (V-As) which is known to have an almost identical activation energy [6, 7]. Hence it is concluded that in S7, opposite polarity measurements revealed As-related implantation damage since the As E-centre was detected.

LDLTS was performed with the same biasing conditions as LDTS both with normal and opposite polarity. For the majority carrier traps detected with normal polarity, reverse bias -2V and fill pulse 2V, LDLTS was performed at temperatures around the main peaks of the DLTS spectrum. Fig. 7.32 shows the LDLTS of the hole trap around 160K in 3-D view. As expected many emission rates are detected by LDLTS for the broad peak that was obtained with normal polarity from DLTS. The high emission rate peak does not particularly change in emission as the temperature reduces, which indicated emission from an extended defect. There are also two more emission rate peaks present at each temperature at lower emission. These reduce in emission as the temperature reduces. Hence the construction of Arrhenius plots for these peaks was attempted but the emission rate-temperature points did not lie on a straight line despite the fact that

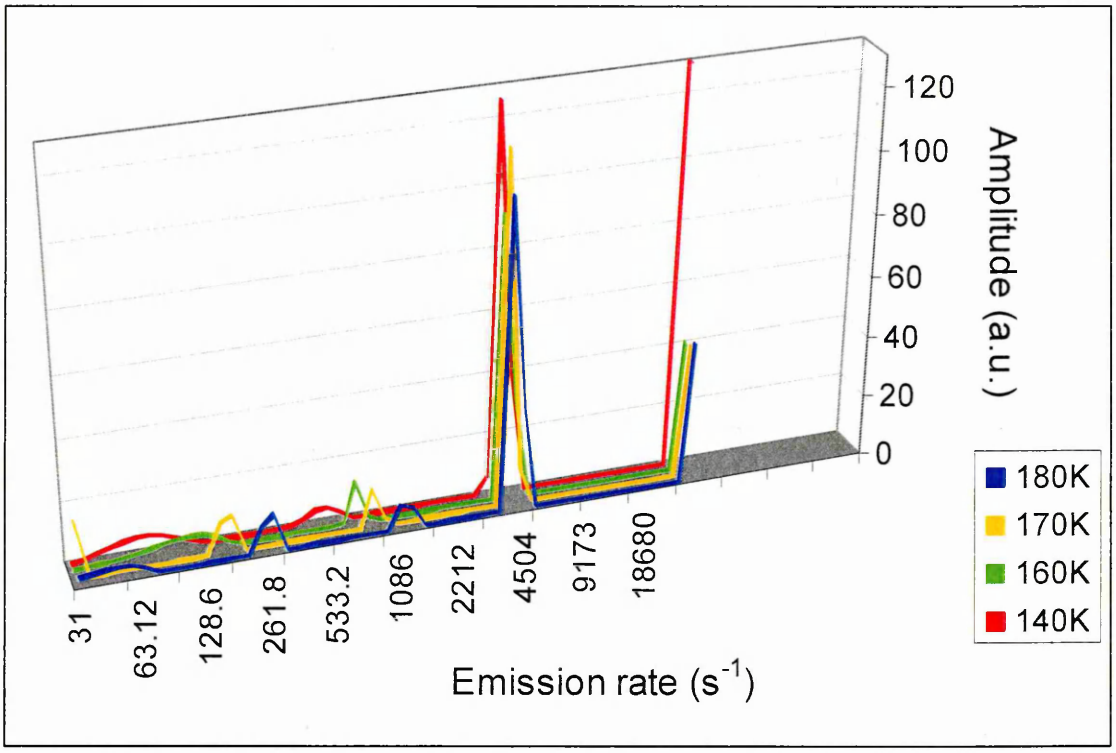

Fig. 7.32: LDLTS spectra for the hole trap detected at 160K with normal polarity from DLTS

emission reduces for reduced temperature. As the two majority carrier traps detected by DLTS were overlapping, it is perhaps necessary to examine the emission of the LDLTS peaks at even lower temperatures below 140K. Fig. 7.33 show the Laplace spectra obtained for the low temperature peak detected by DLTS at 120K.

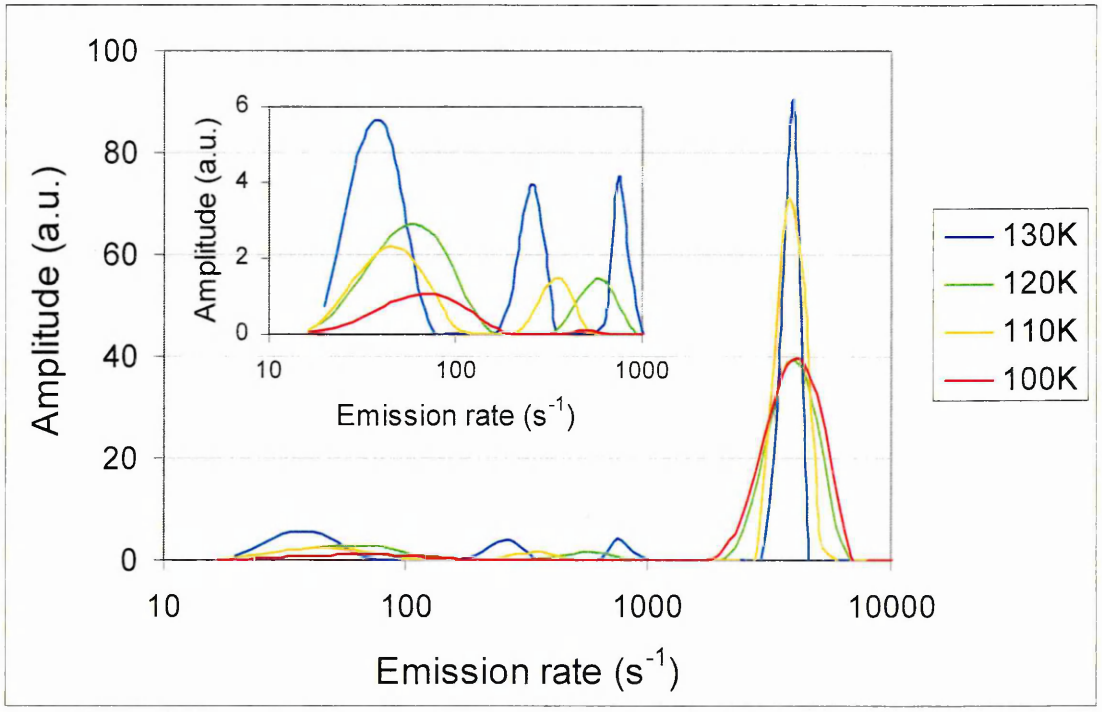

Fig. 7.33: LDLTS spectra of the low temperature peak detected by DLTS at 120K with normal polarity. The inset shows an expanded view of the emission rates below 1000s^{-1}.

The inset of Fig. 7.33 shows the emission rates below 1000s^{-1} as their amplitude was too small when all the peaks are on the same spectrum. Three or four emission rates are again detected for the DLTS peak at 120K as seen in Fig. 7.33. This indicates that emission is continued for these levels throughout the temperature range of 180-100K and the evolution of these with temperature should be examined. Hence Arrhenius plots were again constructed following the emission of these peaks from 180-100K. However, once again, the emission rate-temperature points did not allow calculation of activation energy as they did not fall on a straight line, despite the fact that their emission reduced with decreased temperature. Therefore it is concluded that these emissions are not due to point defects but most likely to complex defects that contain many levels. This result is in agreement with the proposed emission from carbon complexes, with non-point defect behaviour. This because the carbon-oxygen interstitial complex has been reported to exhibit time-dependent capture kinetics and with similar activation energy as detected for the high temperature trap by DLTS [4, 8].

The LDLTS of the minority trap obtained with opposite polarity by DLTS at about 270K is shown in Fig. 7.34 in 3-D view to facilitate observation of the emission rates.

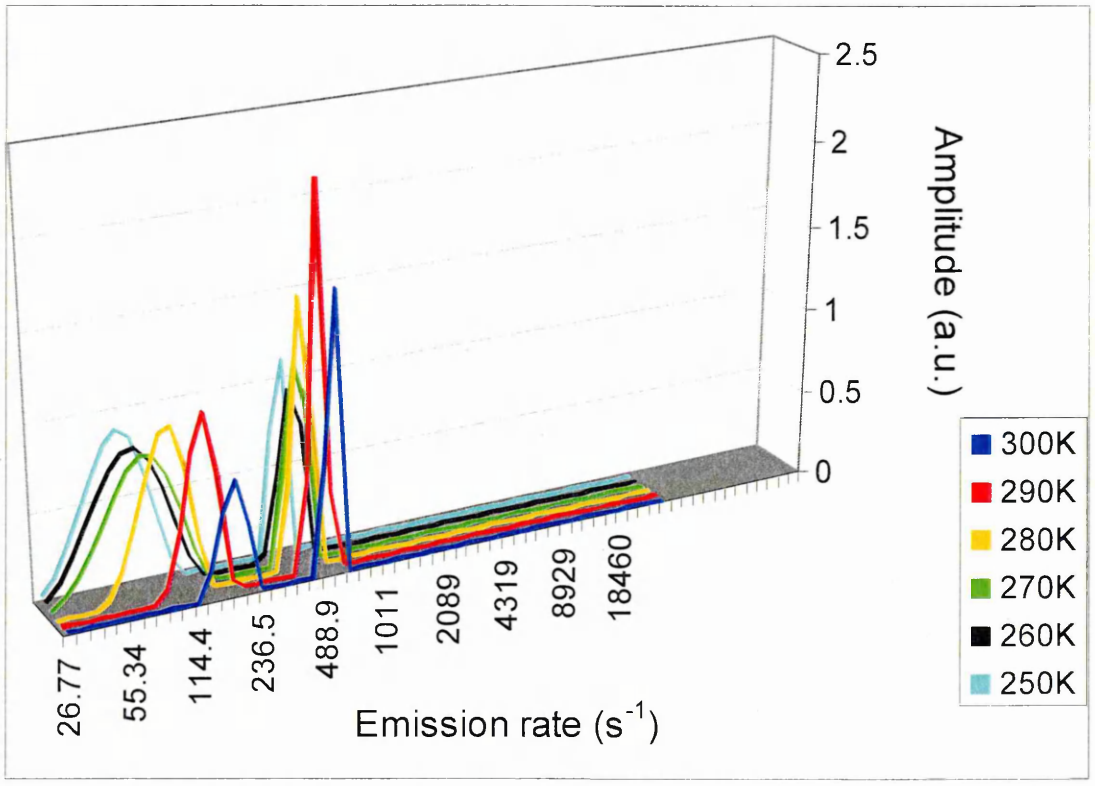

Fig. 7.34: LDLTS spectra of minority trap obtained with opposite polarity from DLTS at 270K

Two emission rates are detected from the LDLTS scans at each temperature. The low emission peak more consistently reduces in emission as the temperature is lowered, than the high emission peak. The latter only reduces as the temperature drops from 300K to 280K and then remains almost invariable with temperature. Therefore its activation energy cannot be determined. The Arrhenius plot of the low emission peak is shown in Fig. 7.35.

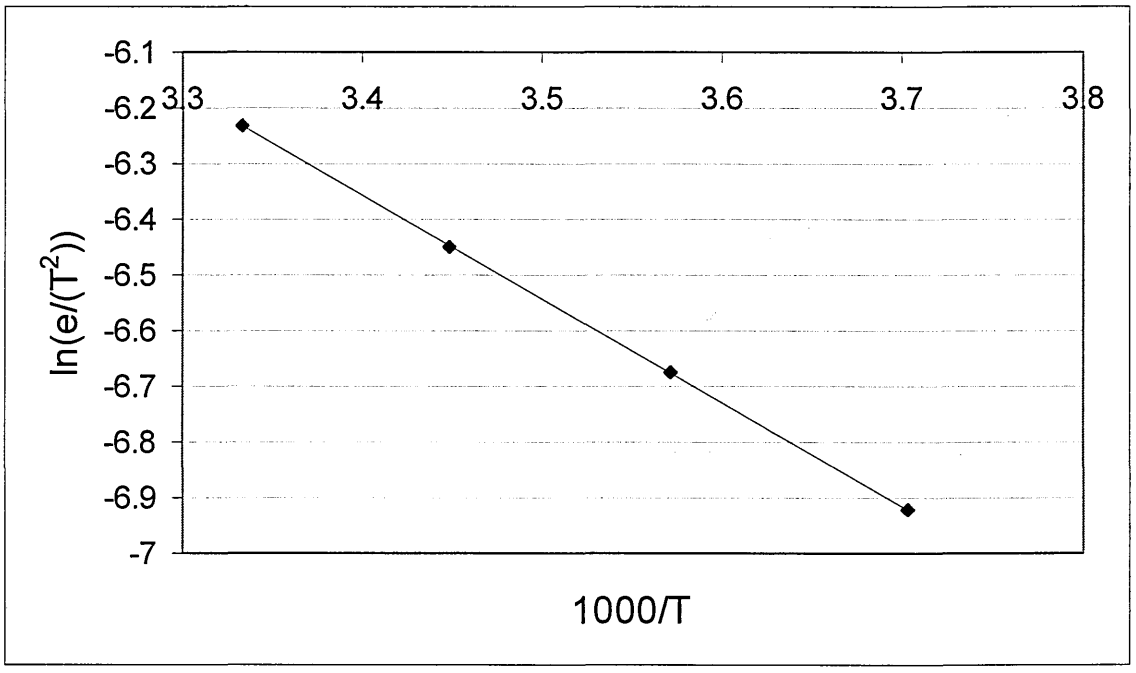

Fig. 7.35: Arrhenius plot of the low emission peak of LDLTS, obtained with opposite polarity for the minority peak at 270K of the DLTS spectrum

The activation energy found from LDLTS for the low emission rate was 0.16eV which is very much lower to the 0.48eV obtained by from the DLTS peak. However, this is due to the fact that the DLTS spectra cover both defects and are more likely to be measuring the emission of the high emission rate level. The activation energy obtained from LDLTS is due to the defect with the low emission rate and this explains the difference in activation energy between the DLTS and LDLTS measurements. The activation energy of 0.16eV resulting from LDLTS is closer to that of the positive divacancy level above the valence band.

7.5 Conclusion

This chapter focused on the characterisation of ultra-shallow n^+p diodes in Si. It was observed that an increase in the p-side B implantation dose by a factor of 2 in diode S7 compared to S8, resulted in a more complicated structure. The presence of two

depletion region capacitances in diode S7 dominated the CV characteristics and required the implementation of both normal and opposite polarity biasing conditions, during DLTS. In addition considerably more leakage current is observed in this diode compared to S8 which possibly originates from the presence of a multitude of defects. However, it should be mentioned that some of the detected defects in both these highly doped n^+p diodes, were of complex nature and not point-defect like. The majority of these originated from interstitial or substitutional defects involving carbon, as revealed by the combination of the DLTS and LDLTS techniques. Minority carrier emission was also obtained from both diodes S8 and S7 with normal and opposite polarity respectively. In the case of S8 this was attributed to an extended defect, while two vacancy-related levels were distinguished by the combined application of DLTS and LDLTS in S7. In the latter case opposite polarity measurements revealed end-of range As-implantation damage attributed to the vacancy-arsenic level.

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Chapter 8: Deep Level Transient Spectroscopy of p-type diamond on silicon

8.1 Introduction

This chapter presents results from the electrical characterisation of p-type CVD diamond thin films on silicon measured by CV, IV, DLTS and LDLTS. As mentioned earlier two different diode structures were investigated. The first section shows the results obtained from p-type diamond on p-type Si Schottky diodes while the second section deals with the characterisation of p-type diamond on n-type Si p-n diodes that were fabricated according to the process previously described in chapter 5. The use of these two diode structures enabled examination of defects that may be present at different depths of the diamond layer. Investigation of the Schottky diodes allowed profiling of the area near the surface of the diamond while the p-n diodes allowed analysis of the depletion region near the interface of diamond with Si. Consequently useful conclusions were drawn about the nature of defects throughout the diamond film and their capture kinetics, while significant information is extracted about the dopant behaviour at different depths.

CV and IV measurements were initially performed at room temperature on all the diodes of each sample for selection of diodes with the best characteristics. The CV data was analysed to yield concentration-depth (N-x) profiles while the reverse and forward current of the diodes was examined by IV measurements. Only the diodes with the least leakage current, good capacitance-bias dependence and carrier concentration profiles were chosen for further CV and IV analysis at different temperatures. DLTS was then performed over a broad temperature range, usually from 100K to 690K, with different rate windows and the spectra were analysed to determine the number of defects present and the temperature range they covered. Subsequently the activation energy and trap concentration was found for different defects. LDLTS was then performed to find the exact emission rates of the defects or to separate closely space defects across the entire defect temperature range, which also allowed a more accurate activation energy calculation in certain cases. Finally capture cross-section measurements were performed

at the most appropriate biasing conditions to investigate the capture behaviour of the defects, where possible. The obtained results are discussed in each section and are compared with the literature. The last section provides a comparison between the examined Schottky and p-n diodes and emphasises the importance of the different diode structures which enabled depth profiling of the diamond films.

8.2 Diamond on p-type silicon

Four p-type diamond on p-type Si samples were examined where the B doping in the diamond ranged from $1.9*10^{20}cm^{-3}$ to $7.6*10^{20}cm^{-3}$. Commercial p-type Si was used with resistivity 1-20Ωcm, yielding a carrier concentration of about $7*10^{16}cm^{-3}$. Table 8.1 shows the B concentration of the grown diamond films of the examined Schottky diodes.

Schottky diodes	B concentration (cm^{-3})
JEF6	$1.9*10^{20}$
JEF7	$2.1*10^{20}$
JEF8	$5.8*10^{20}$
JEF9	$7.6*10^{20}$

Table 8.1: B concentration of diamond films for Schottky diodes

As can be seen from table 8.1 the B concentration of the last two diodes JEF8 and JEF9 is well within the range for metallic conduction as has been previously discussed in chapter 3 [1]. Therefore it is expected that for these two diodes IV measurements will reveal more linear characteristics with high leakage current which may render them unsuitable for DLTS measurements. However, it should be once again mentioned that the B concentration of $3*10^{20}cm^{-3}$ is considered to be the beginning of metallic conduction, in single crystal diamond and hence there may be a difference with the polycrystalline diamond films used for the Schottky diodes examined here [1]. Another issue to be addressed at this point is that the IV and CV measurements were performed at a wide temperature range from 100K to 690K and as the temperature increases the leakage current of the diodes may rapidly increase. For the very highly doped JEF8 and JEF9 samples, measurements may not be possible at high temperatures due to high currents. Beginning the analysis of the diodes, Fig. 8.1 shows the IV measurements of JEF6 at different temperatures.

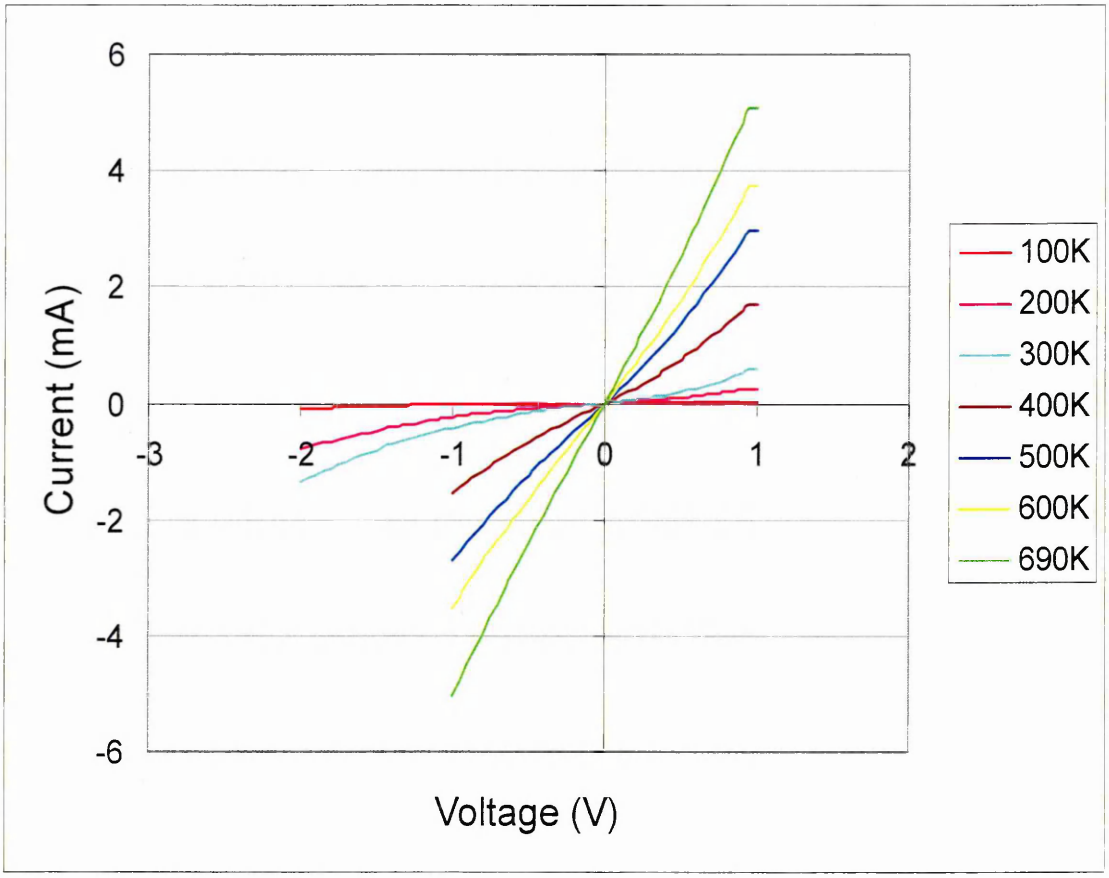

Fig. 8.1: IV measurements of diode JEF6 at different temperatures

Fig. 8.1 reveals reasonable diode characteristics for a diamond diode in particular between 100K and room temperature (300K) at -2V. At 100K the reverse current is 0.1mA at -2V and the forward current is 0.02mA at 1V. However, as the temperature rises above 300K both the reverse and forward current continue to quickly increase and above 600K the IV characteristic becomes virtually linear. Consequently the high leakage current at these temperatures is directly proportional to the applied bias and in order to avoid irreversible diode breakdown the maximum applied bias was set to -1V. However, the IV characteristics are diode-like for the majority of the temperature range making the diode suitable for further analysis and DLTS application.

Fig. 8.2 shows the IV data obtained for JEF7 for a range of temperatures. The IV characteristics are similar to the ones of JEF6 with the reverse and forward currents increasing as the temperature increases but not as rapidly as in JEF6. At 100K the reverse current is 0.6mA at -2V and the forward current 0.2mA, which is higher than JEF6 but they increase slower with increasing temperature. In fact even at 600K and 690K the IV curves remain diode-like although the applied bias was reduced to -1V

above 350K to ensure breakdown would not occur. Therefore once again this diode is suitable for DLTS measurements, which will be presented shortly.

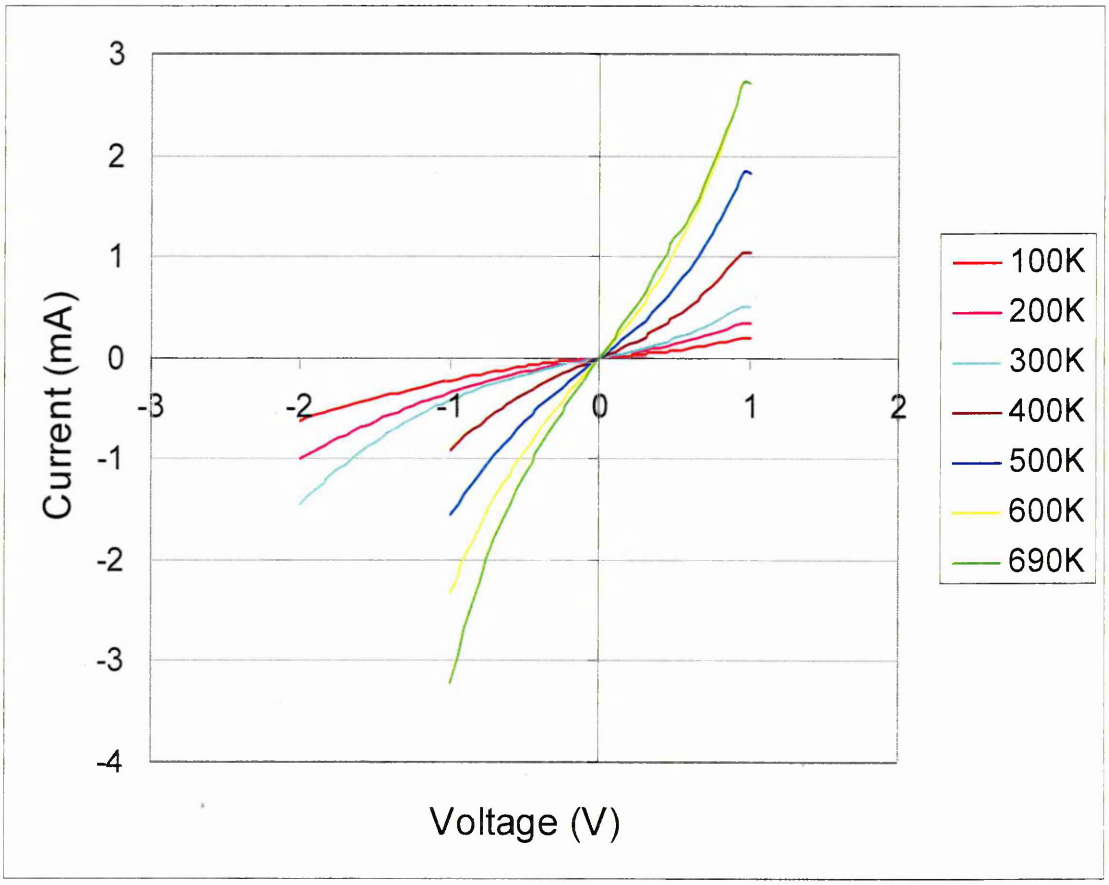

Fig. 8.2: IV characteristics of diode JEF7 at different temperatures

The IV results for JEF8 are shown in Fig. 8.3 where it can be seen that despite the fact that the B content of the diode is high enough for metallic conduction, the IV characteristics are not yet entirely linear. The IV curves reveal that the forward and reverse currents are high but they still exhibit very small rectification. Due to their high values the maximum applied bias was limited to -1V at all temperatures to prevent diode breakdown. For the same reason the IV measurements were only performed up to 450K, which however is a broad enough temperature range. This suggests that metallic conduction has not yet commenced despite the high B doping of JEF8 since the diode does not show resistive behaviour. Therefore the diode may still be used for DLTS and valuable data may be obtained. In addition, this result constitutes significant evidence that metallic conduction in polycrystalline diamond films requires higher B concentration compared to single-crystal diamond. By examination of the IV results of Fig. 8.3 it can be seen that both the forward and reverse currents rapidly increase with increasing temperature until 300K while as the temperature rises above 300K they start

to decrease. This is a different result compared with JEF6 and JEF7 where the current was continuously increasing as the temperature increased. A possible explanation for this phenomenon is that when the B concentration is very high, near the limit for metallic conduction, the carrier concentration appears to be independent of temperature and mobility decreases at temperatures higher than 300K due to phonon scattering [2, 3]. Consequently conductivity is also slightly reduced at this temperature resulting in a small decrease in current. However, the IV characteristics may still possess sufficient rectifying properties to perform DLTS.

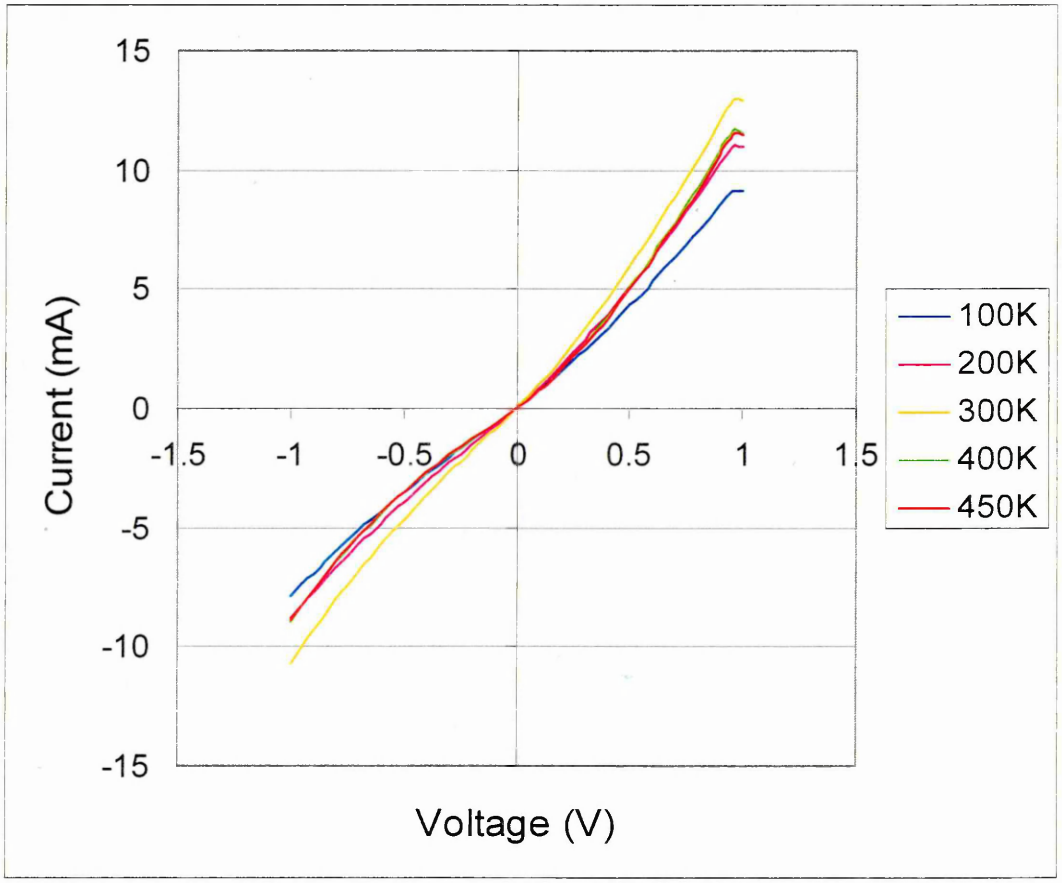

Fig. 8.3: IV characteristics of diode JEF8 at different temperatures

In contrast, the IV data of JEF9 revealed a completely linear characteristic (not shown) due to the combination of low mobility and very high B doping in this film, which resulted to the current being only proportional to the applied bias. This is an expected result for this very highly doped sample, which exhibits metallic conduction [3]. For instance, the forward current at room temperature in this diode reached 20mA while the reverse current was 15mA. These values of current are very high and further analysis at different temperatures, DLTS and LDLTS experiments, were not possible for this sample.

CV measurements were performed on the same diodes and the acquired data was analysed to yield the carrier concentrations for each sample. Fig. 8.4 shows the CV and carrier concentration-depth (N-x) profiles obtained at different temperatures for JEF6.

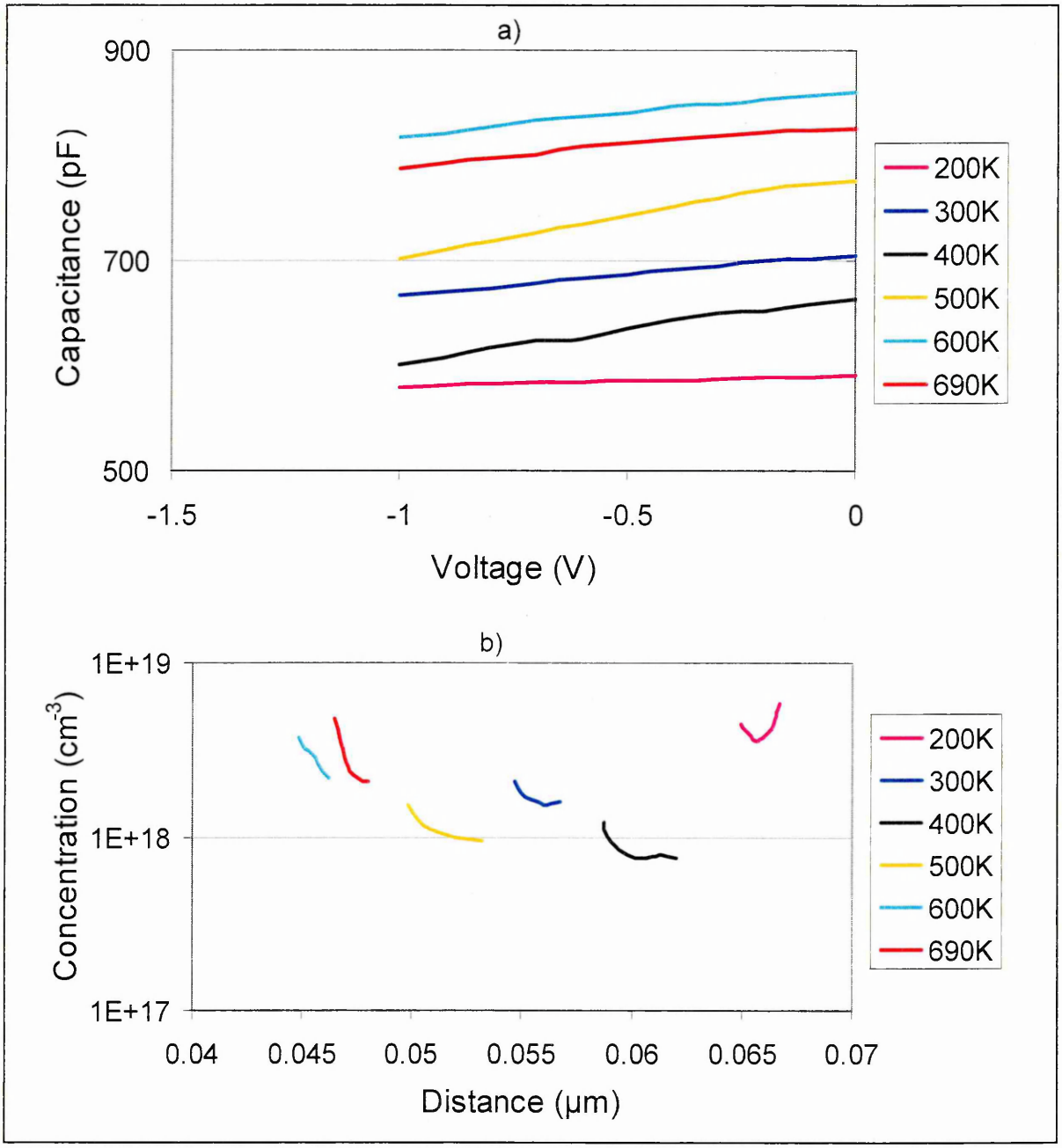

Fig. 8.4: a) CV and b) N-x profiles of diode JEF6 at different temperatures

The CV measurements were performed with the same bias as the IV measurements to ensure there was no large current passing through the diode. The capacitance of JEF6 at zero bias is quite large and it largely increases with temperature. This indicates that the depletion region width is narrow, as can be verified from the N-x profiles, which is expected since the carrier concentration is high. In addition, from 100K to about 300K the capacitance is not very bias dependent but as the temperature rises beyond this point

the capacitance changes more rapidly. Fig. 8.4b) shows that the depletion region lies at a depth of about 50-60nm from the surface, at temperatures of 200K and above, and the carrier concentration changes only slightly with temperature but is generally centred around $1.5*10^{18}cm^{-3}$. It has to be noted here that the concentration axis is set at the logarithmic scale. The obtained carrier concentration value is therefore about two orders of magnitude smaller than the doping concentration indicating that only about 0.8% of the initial B concentration has been activated.

Fig. 8.5 shows the CV and carrier concentration profiles obtained for JEF7 at different temperatures.

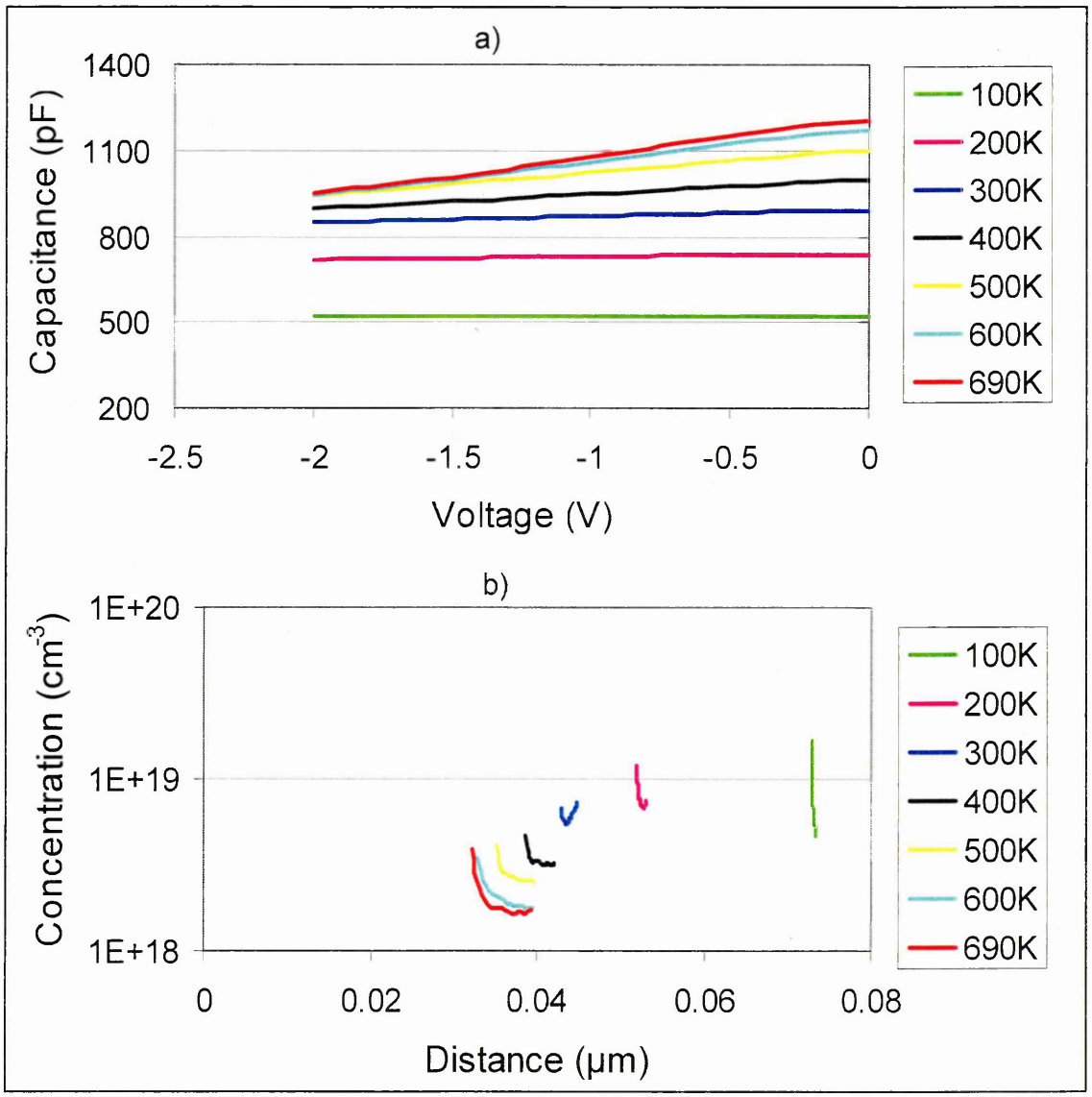

Fig. 8.5: a) CV and b) N-x profiles of diode JEF7 at different temperatures

Fig 8.5a) shows that the capacitance of JEF7 is even higher than that of JEF6 as the B doping for this sample is higher. Consequently the carrier concentration is larger and the depletion region width is even narrower in this case as it can be verified from Fig. 8.5b). The capacitance is increasing much more but in a continuous manner with temperature. It can be observed that the capacitance is more bias dependent above room temperature as was the case for JEF6. The carrier concentration correspondingly is decreasing as the temperature increases from about $1*10^{19}cm^{-3}$ at 100K to $2*10^{18}cm^{-3}$ at 690K but is around $6*10^{18}cm^{-3}$ at room temperature and the depletion region lies around 40nm from the surface. Therefore in JEF7 the B ionisation percentage is 2.8% which is larger than JEF6 but still a small fraction compared to the B doping for this sample.

Fig. 8.6 shows the CV and N-x profile for diode JEF8 at the same temperature range as the IV measurements, from 100K to 450K.

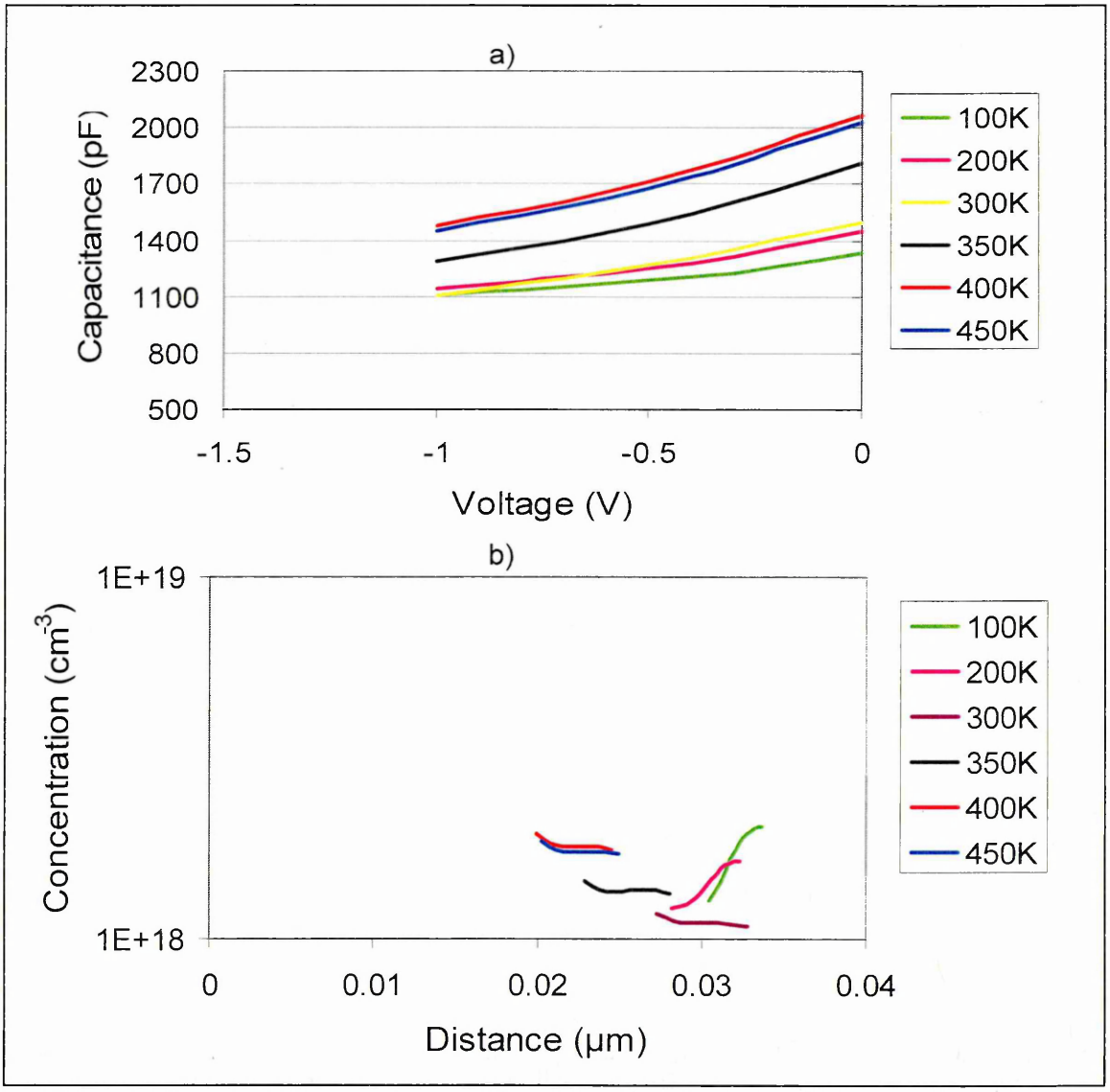

Fig. 8.6: a) CV and b) N-x profiles of diode JEF8 at different temperatures

The CV characteristics of JEF8 show that the capacitance of this diode is very high at zero bias and it greatly increases with temperature. The depletion region is now narrower and around 30nm from the surface. In addition for every temperature the capacitance is much more bias dependent than the previous two examined diodes. The CV measurements were performed with a maximum of 1V reverse bias similarly to the IV characteristics to avoid large currents passing through the device. Despite the large capacitance values which are due to the high B content, the measured carrier concentration of JEF8 is around $2*10^{18}cm^{-3}$ which is much lower than that of JEF7 showing a B ionisation percentage of 0.34% for this diode.

CV measurements for diode JEF9 were only performed at selected temperatures because as mentioned earlier the diode exhibited very high leakage currents and linear IV characteristics. Fig. 8.7 illustrates the obtained CV and corresponding N-x results for this very highly doped diode.

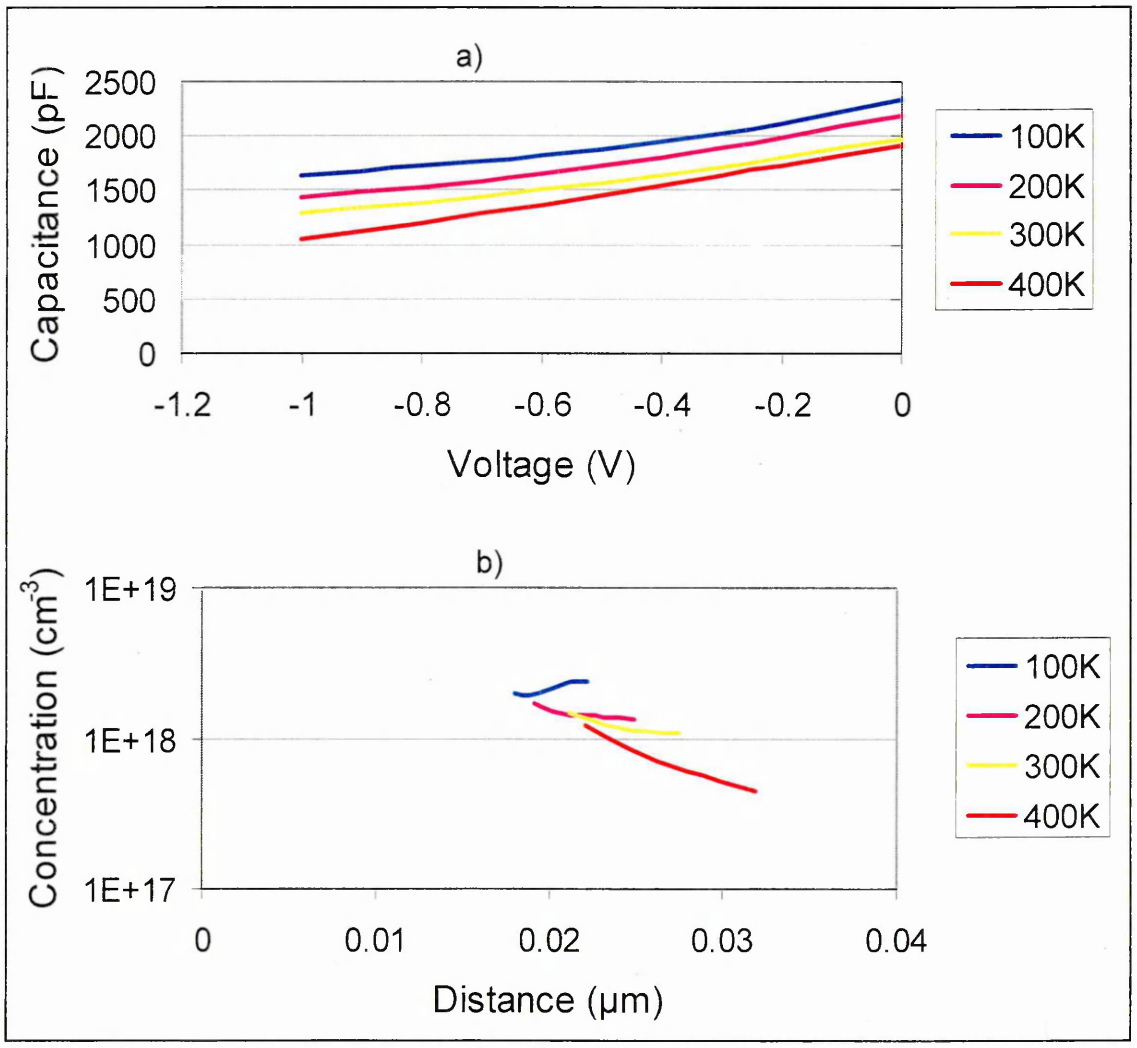

Fig. 8.7: a) CV and b) N-x profiles of diode JEF9 at different temperatures

From Fig. 8.7 it is obvious that the capacitance of diode JEF9 is very high. However, it decreases as the temperature increases which is the opposite of what is expected for a normal diode. Furthermore the CV characteristics as the temperature increases are no longer diode-like. For instance at 400K, the capacitance is changing with bias almost linearly. Fig. 8.7b) shows that the carrier concentration is actually decreasing steadily with increasing temperature. To explain this it is worth noting that the diamond is very highly doped in this diode and metallic conduction is taking place. Therefore the B acceptor level may be overlapping with the valence band [1]. Consequently it was not possible to conduct any further measurements on this diode such as DLTS or LDLTS.

The following section presents the DLTS results that were obtained for diodes JEF6-JEF8 by using different rate windows and biasing conditions. Starting with JEF6, Fig. 8.8 shows the DLTS spectra acquired with six different rate windows, reverse bias (RB) -2V, fill pulse (FP) 1V and for a temperature range of 100-690K. The fill pulse length is 1ms for all these measurements unless stated otherwise.

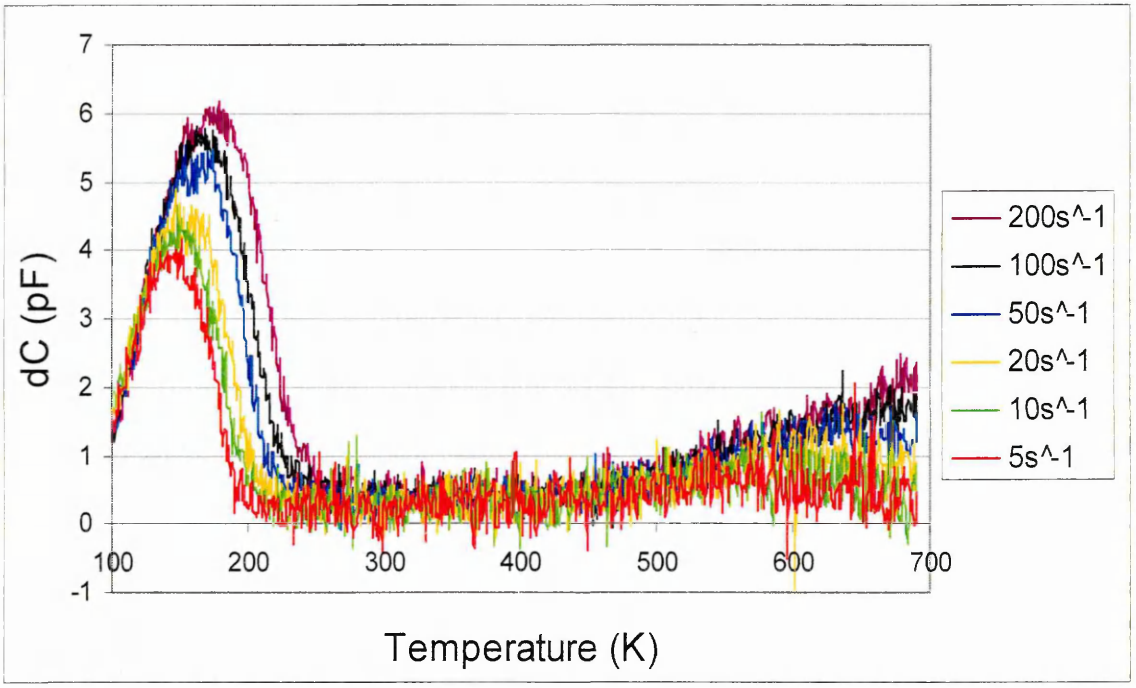

Fig. 8.8: DLTS spectra of JEF6 from 100-690K with RB=-2V and FP=1V

The DLTS spectra for this diode reveal a defect level emitting between 100-200K and a broad spectrum starting from 400K. The latter does not appear to peak within the measured temperature range although for lower rate windows below $50s^{-1}$ the peak can be distinguished. These peaks are positive for this p-type material therefore they are hole traps. The low temperature peak appears to be symmetrical. However, its height

reduces for lower rate windows and it is only the high temperature side of the defect that shifts to the left for lower rate windows, while the low temperature side remains fixed. For a Si diode this may have been an indication that this is not a point defect and it is possible that this may also be applicable to diamond [4]. As it is a narrow level, it does not appear to consist of many closely spaced defects, however in order to verify this result higher resolution measurements are required that will be provided by LDLTS. By measuring the peak temperature (T_{max}), of each defect on the DLTS spectrum for a particular rate window (e) and collecting these temperature-rate window pairs (T_{max}, e) the activation energy of the defect can be found. For the broad defect above 400K, only the lower four rate windows were used where the DLTS shows a maximum. The slope of the Arrhenius plot of the logarithm of the rate window against temperature will allow the calculation of the activation energy as explained in chapter 4. Fig. 8.9 and 8.10 show the Arrhenius plots for the low temperature defect and the high temperature broad spectrum respectively for JEF6.

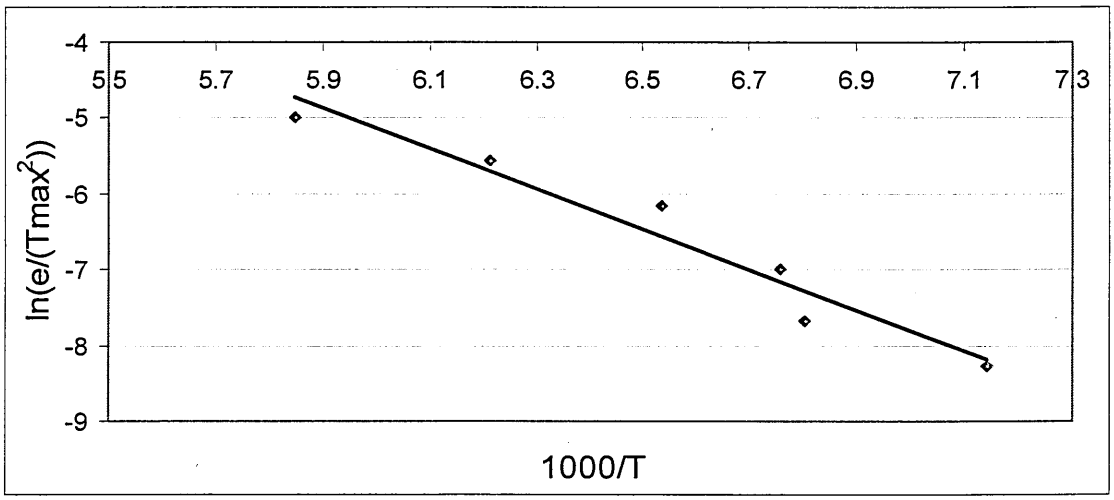

Fig. 8.9: Arrhenius plot of the low temperature defect of JEF6

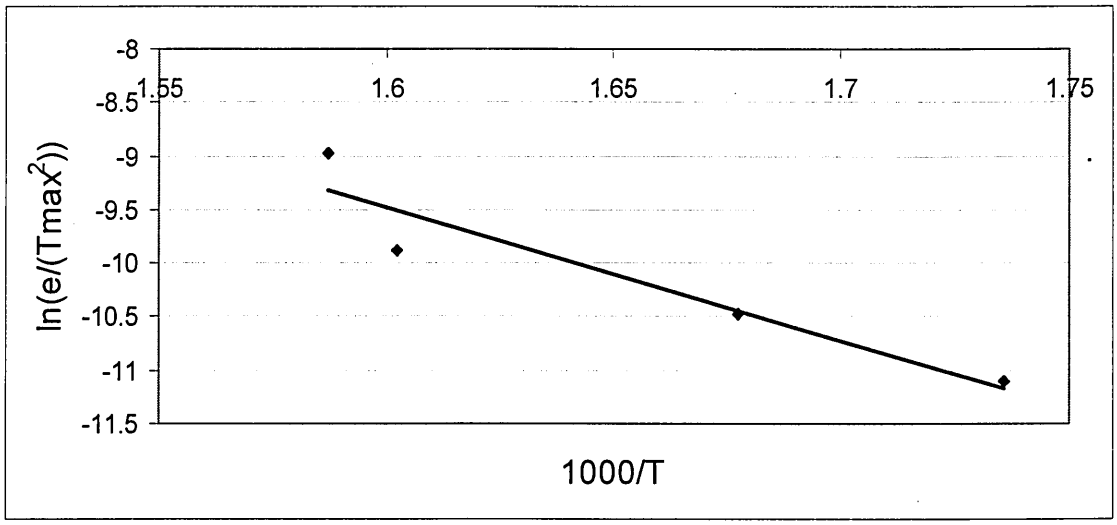

Fig. 8.10: Arrhenius plot of the broad spectrum above 400K in JEF6

From graphs 8.9 and 8.10 it can be seen that the slope of the maximum temperature-emission rate points fit well on a straight line. Using the slope of this plot the activation energy of the low temperature defect was found to be 0.25eV while that of the high temperature broad spectrum was 1.06eV which is reasonable since this defect is located at such high temperature and can be compared to the literature [6-8]. The defect at 0.25eV above the valence band is probably a different level than the B acceptor level which is usually measured as 0.38eV. The latter has not been detected in these samples. A comparable spectrum of a low temperature level and a broad spectrum have been observed in the literature for similar p-type diamond/p-type Si diodes thus verifying the DLTS results presented here, although in that work the activation energy of the broad spectrum was not reported [5]. The same two defect levels were obtained under different biasing conditions of -2V reverse bias and zero volts fill pulse which was enough to fill the hole traps in the depletion region.

A similar result was obtained for diode JEF7 which is slightly more highly doped than JEF6. The DLTS measurement was performed with the same biasing conditions of reverse bias -2V and fill pulse 1V and for the same temperature range. The DLTS spectra for JEF7 using the same rate windows as previously are shown in Fig. 8.11.

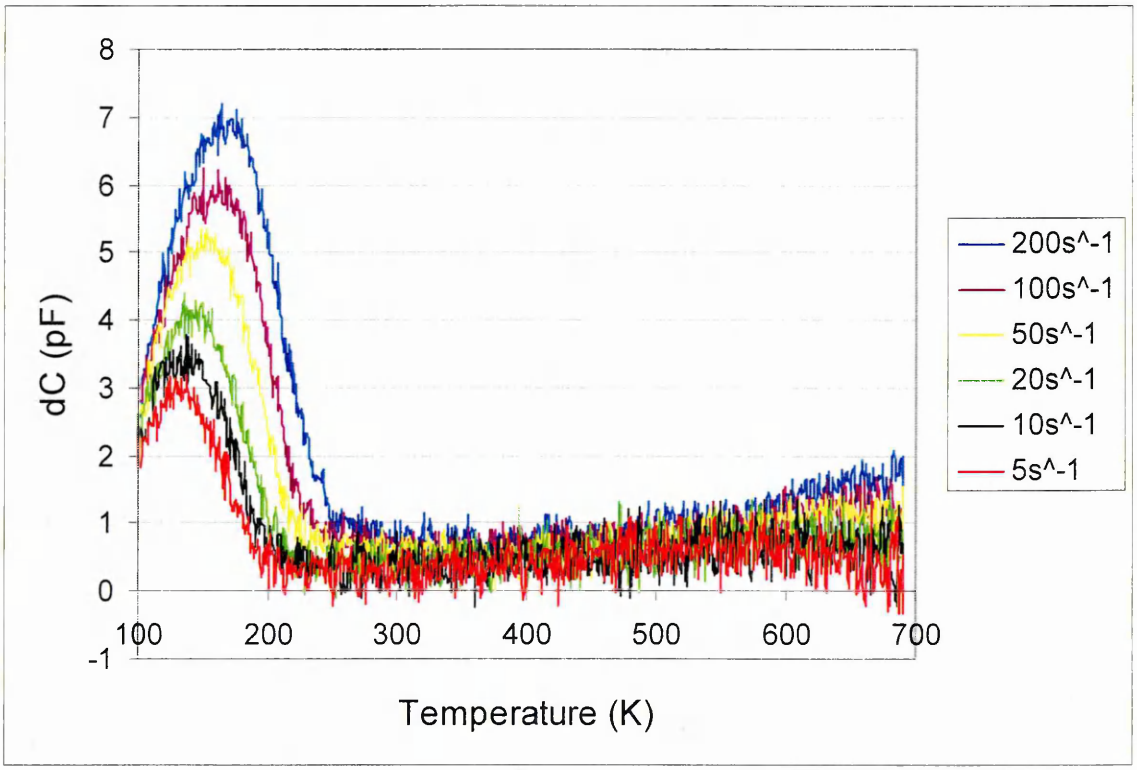

Fig. 8.11: DLTS spectra of JEF7 from 100-690K with RB=-2V and FP=1V

The peak at low temperature is slightly wider in this sample and the high temperature broad spectrum is located at lower temperatures. It was possible to distinguish the peak of the latter for the lower five rate windows, therefore making the calculation of its activation energy more accurate. The peak at 170K once again reduces for lower rate windows while the low temperature side of this peak appears fixed compared to the high temperature side as the rate window reduces. The activation energy plots for the low and high temperature defects of JEF7 are shown in Fig. 8.12 and 8.13 respectively.

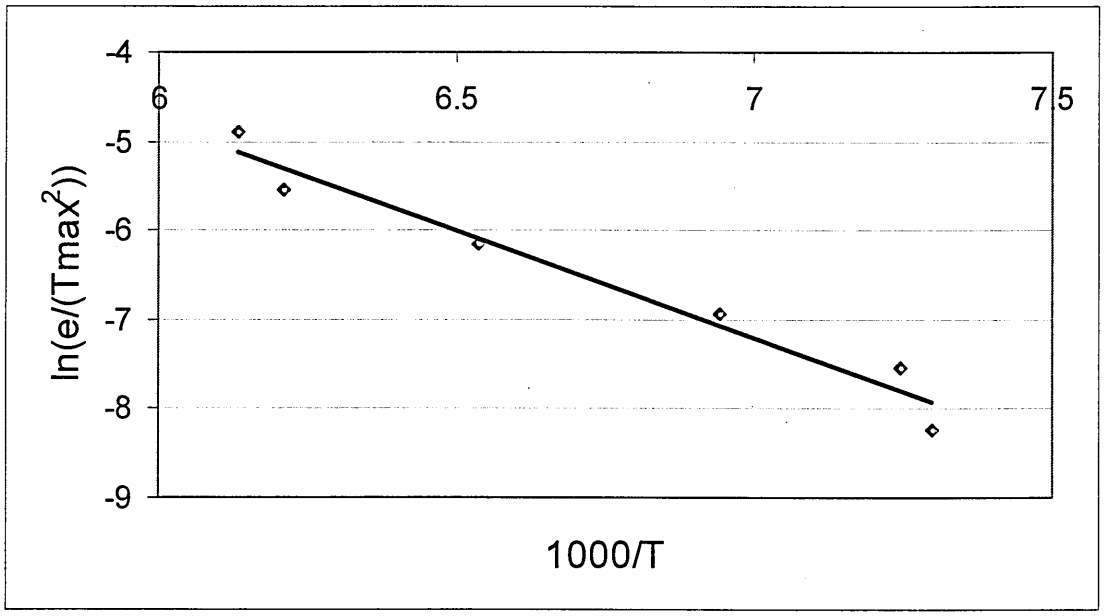

Fig. 8.12: Arrhenius plot of the low temperature defect in JEF7

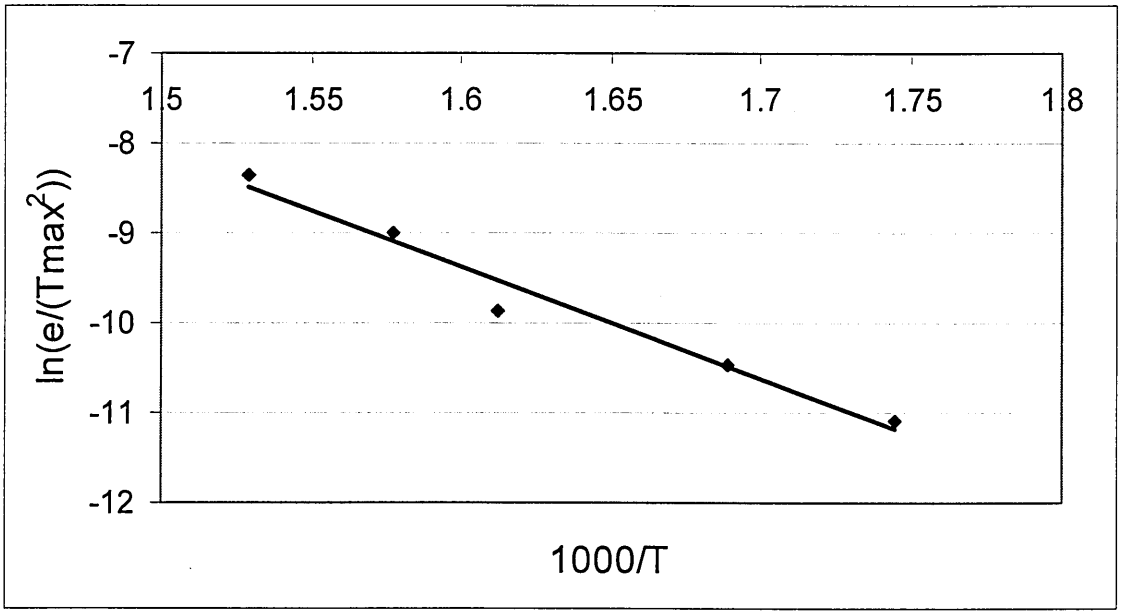

Fig. 8.13: Arrhenius plot of the high temperature level in JEF7

The activation energy of the peak at 170K was found from its Arrhenius plot to be 0.21eV above the valence band while that of the high temperature broad spectrum was 1.07eV [6]. The activation energy plots show that the peak temperature-emission rate points for JEF7 have a better linear fit for this diode.

DLTS measurements of JEF8 were difficult due to the high leakage current of the diode. However in DLTS the reverse bias is lowered after the application of the fill pulse therefore diode breakdown was avoided. No DLTS signal was expected to be observed since the diode is very highly doped and in the range for metallic conduction. The measurements were performed once more with reverse bias of -2V and fill pulse 1V and for each rate window individually in this case. The results obtained are presented in Fig. 8.14.

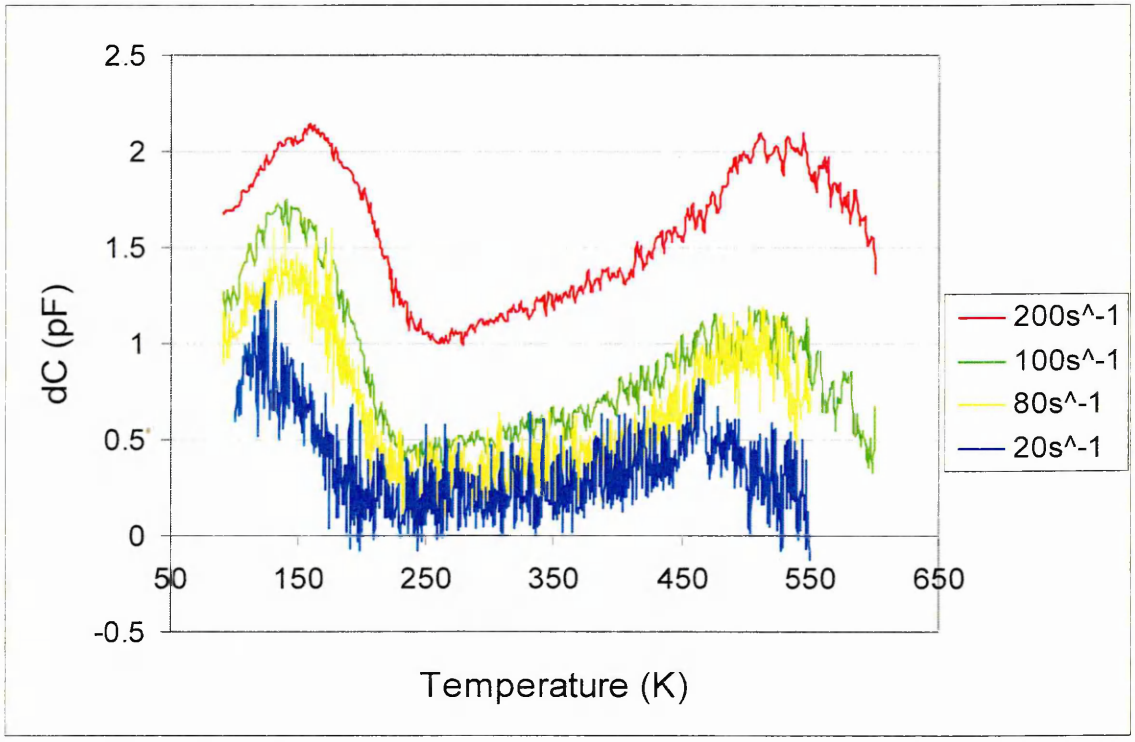

Fig. 8.14: DLTS spectra of JEF8 from 80-600K with RB=-2V and FP=1V

It can be seen from Fig. 8.14 that even though this diode is very highly doped it was possible to observe similar DLTS spectrum as the previous two diodes. The signal is much smaller and therefore is noisy, especially for the lower rate windows, but the low temperature peak and broad spectrum at high temperatures are still clearly observed. The peak of the low temperature defect is now located around 150K but the peak of the broad spectrum can now be distinguished even for the high emission rate of $200s^{-1}$.

DLTS with lower rate windows did not yield any results as the signal was obscured by noise. Fig. 8.15 and 8.16 show the activation energy plots for these two levels.

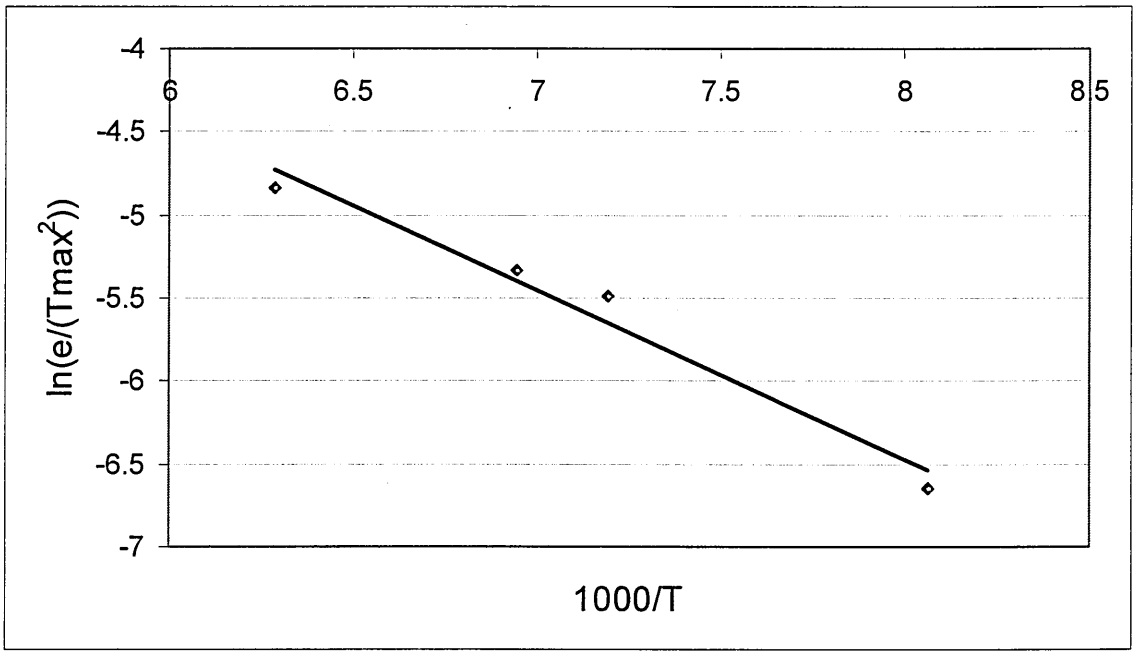

Fig. 8.15: Arrhenius plot of the low temperature level of JEF8

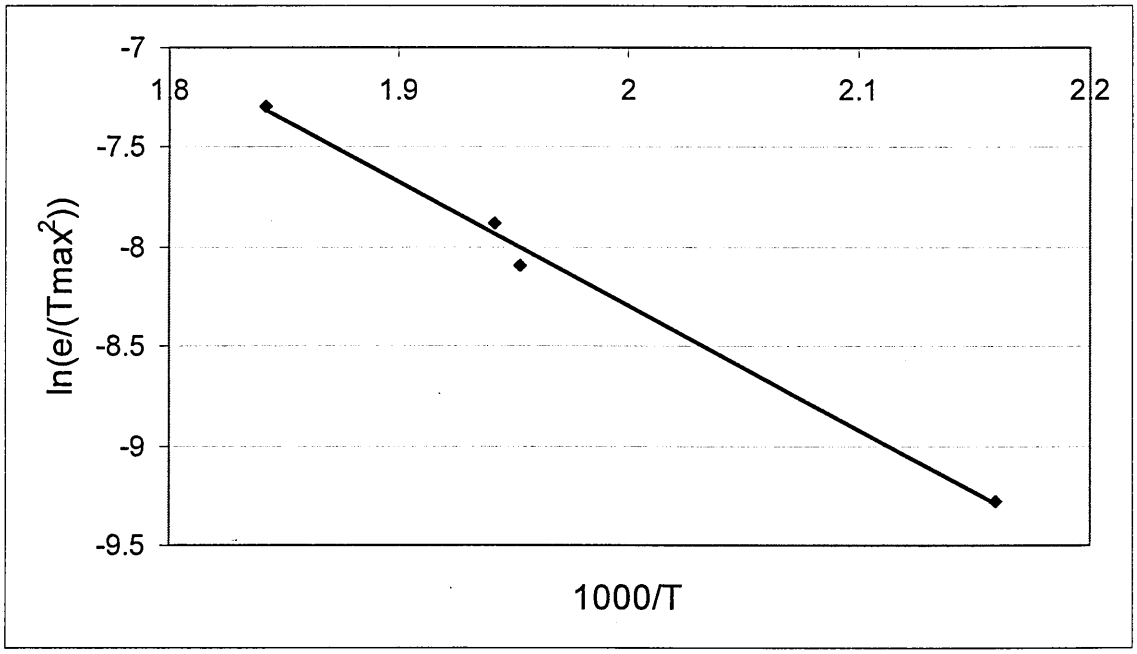

Fig. 8.16: Arrhenius plot of the high temperature level in JEF8

The fact that DLTS was possible with four rate windows for this diode entails that only four peak temperature-emission rate points were available for the calculation of the activation energy. These are normally sufficient for activation energy calculations. DLTS ideally yields satisfactory results with an accuracy of ± 50meV where the

obtained signal is clear and the peaks easily identified. In the case of JEF8 calculation of the activation energy was found to be 0.1eV for the low temperature and 0.53eV for the high temperature level respectively. However it has to be noted that due to the noisy signal and the possible presence of metallic conduction these values may not be within the usual accuracy of DLTS, in particular for the low temperature peak which might be overlapping with the valence band.

DLTS measurements were also performed for JEF9 keeping the reverse bias very low in order not to break the diode down but the obtained spectra did not yield any meaningful results as only noise was observed.

LDLTS was performed on diodes JEF6-JEF8 under the exact same biasing conditions as the DLTS measurements in order to provide more information about the nature of the defects and their emission rates. In addition the measurement was not only carried out at the peak of the DLTS spectrum, but also in steps, across the entire temperature range that each defect covered. The most representative of the results will be presented here. Fig. 8.17 and 8.18 show the LDLTS spectra for JEF6 around the peak of the low temperature and the high temperature defect respectively. These are shown in 3-D view to facilitate comparison.

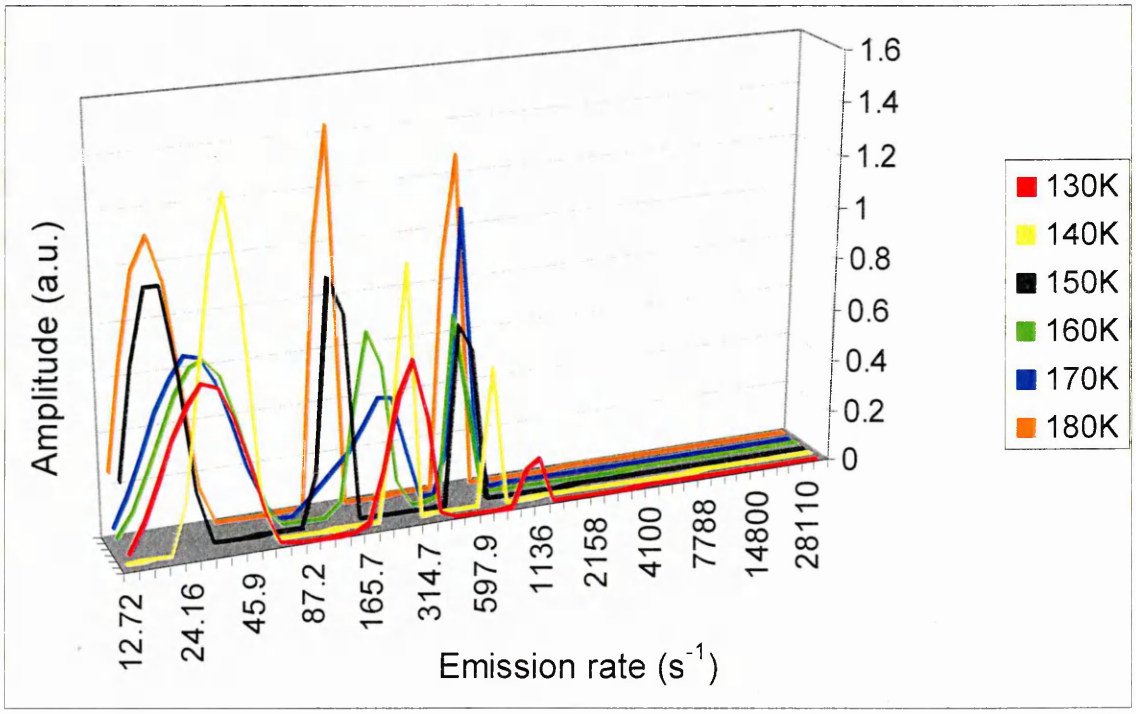

Fig. 8.17: LDLTS of defect at 170K in JEF6 with RB=-2V and FP=1V

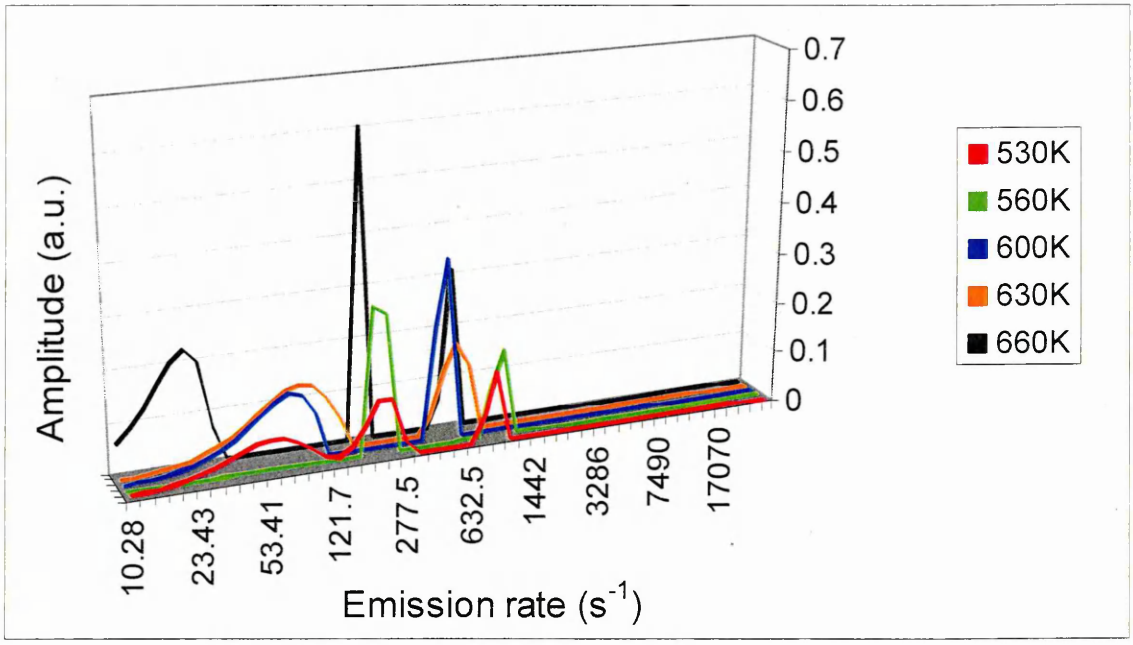

Fig. 8.18: LDLTS of high temperature defect in JEF6 with RB=-2V and FP=1V

Fig. 8.17 reveals three different emission rate components at each of the measured temperatures for the DLTS peak at around 170K for JEF6. The emission rates of these are around $30s^{-1}$, $200s^{-1}$ and $500s^{-1}$ respectively and they appear at all the measured temperatures. This result entails that either there are three closely spaced point defects that DLTS could not separate, or possibly extended defects. In the case of point defects, an increase of emission rate when the temperature increases would be expected. The LDLTS peaks should be shifting towards higher emission rates at every temperature increment in a consistent manner. However, careful examination of the LDLTS spectra shows that this is not the case. The peaks of the emission rates are either moving in a random fashion when the temperature increases or they seem almost unaffected by the temperature change. In fact efforts to calculate the activation energy of the defects by plotting the LDLTS pairs of peak emission rate against temperature does not yield a straight line as the emission rates increase with reducing temperature (not shown). The points for each of the emission rates would be quite scattered as can be easily observed from Fig. 8.17. Most importantly the slope of reducing emission with increasing temperature would indicate that when the temperature increases, the logarithm of the emission rate divided by the square of the temperature (y-axis) would also increase. However, this is the opposite of what is expected to occur, since when the temperature increases the emission rate should increase since the traps have more energy at higher temperatures to emit faster. As this is not the case in diode JEF6 the activation energy from LDLTS will not provide reasonable results and certainly not in any way

comparable with the DLTS activation energy of 0.25eV. The LDLTS of the high temperature broad spectrum is even more complicated since there are a different number of emission components at every temperature. In addition, once more the peak emission rates do not steadily increase with temperature making it impossible to calculate the activation energy. In fact most of the points of each component would fall on a straight line parallel to the 1000/T axis of the activation energy plot, indicating that even though the temperature increased, the emission rate slightly decreased. Therefore the traps observed in this diode are quite possibly not point defects, although capture cross-section measurements, which will be shown later may offer more information about their nature.

LDLTS measurements of JEF7 produced similar results to those of JEF6. The biasing conditions were the same as the DLTS for this diode with reverse bias -2V and fill pulse 1V and the measurements covered the entire temperature range of both the low and high temperature defects for comparison. The LDLTS spectra obtained for the defect at 170K are shown in Fig. 8.19 while that of the high temperature broad spectrum are shown in Fig. 8.20. The low temperature defect appears to consist of two components at most temperatures. The high emission component remains the same for most of the temperatures in Fig. 8.19 while the low emission component peak varies but once again not steadily with temperature.

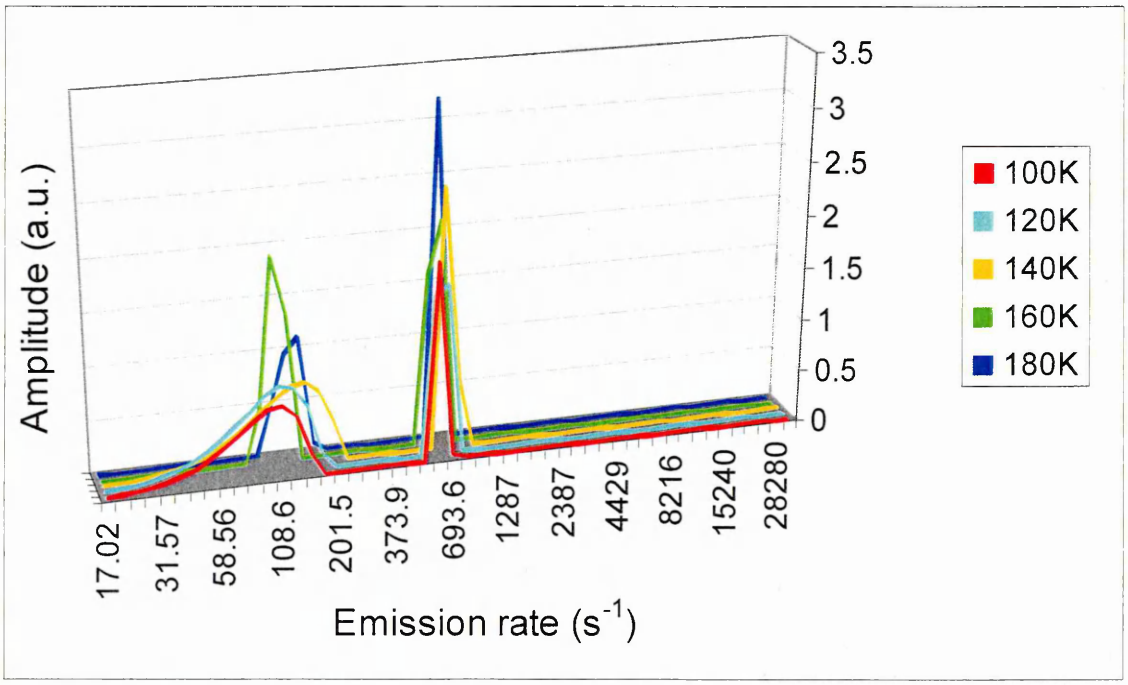

Fig. 8.19: LDLTS spectra of low temperature defect in JEF7

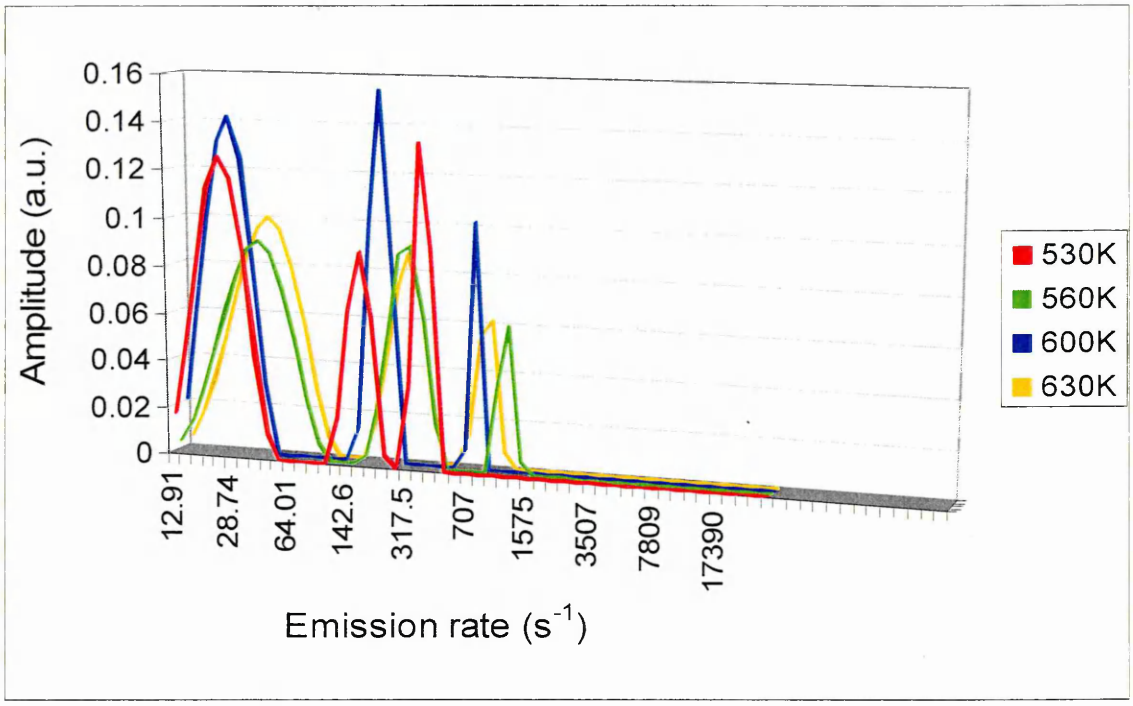

Fig. 8.20: LDLTS spectra of high temperature defect in JEF7

Fig. 8.20 shows that the high temperature defect consists of three emission rates. These however, do not steadily increase in emission with temperature as would be expected for a point defect. Since the emission rates of both defects of JEF7 either do not change with temperature or change in a random manner, it can be suggested that these are not point defects and further analysis is necessary to identify their nature. The Arrhenius plots constructed from the LDLTS spectra of the low temperature defect for both its emission components are shown in Fig. 8.21. These plots illustrate that as the temperature increases, the logarithm of emission over the square of temperature decreases, because the emission rate remains constant or reduces. Hence it is not possible to calculate an activation energy and these plots are merely shown to support this conclusion.

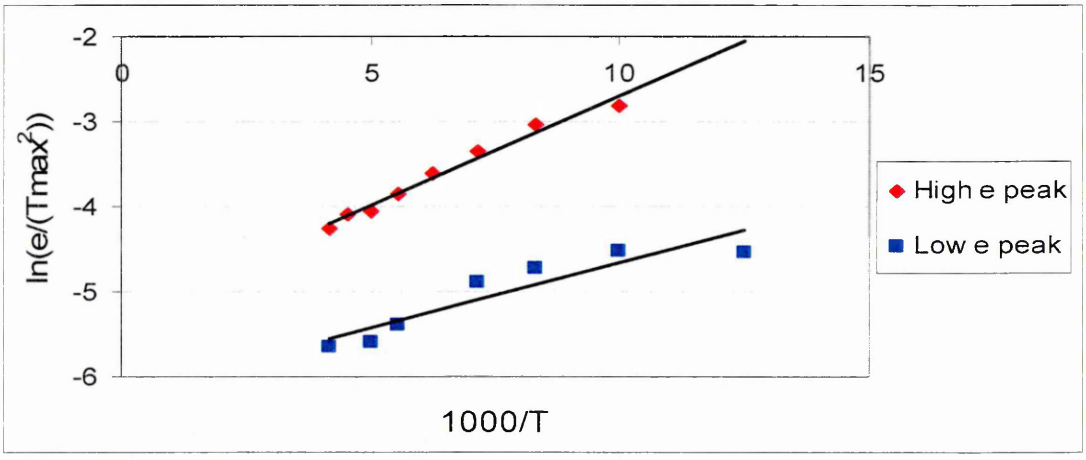

Fig. 8.21: Arrhenius plot from LDLTS for the 170K peak in JEF7

Fig. 8.22 and 8.23 show the LDLTS spectra for the low and high temperature defects of JEF8 respectively, corresponding to the DLTS results of Fig. 8.14 and obtained with the same biasing conditions of -2V reverse bias and 1V fill pulse.

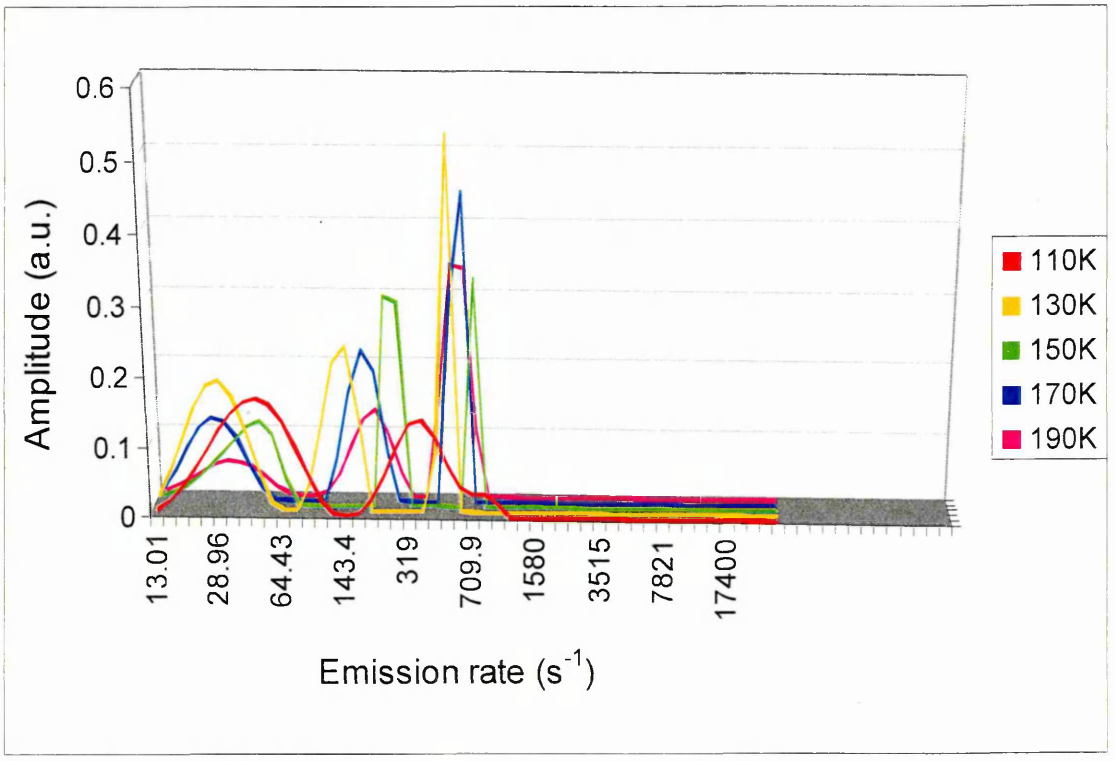

Fig. 8.22: LDLTS results for the low temperature defect in JEF8

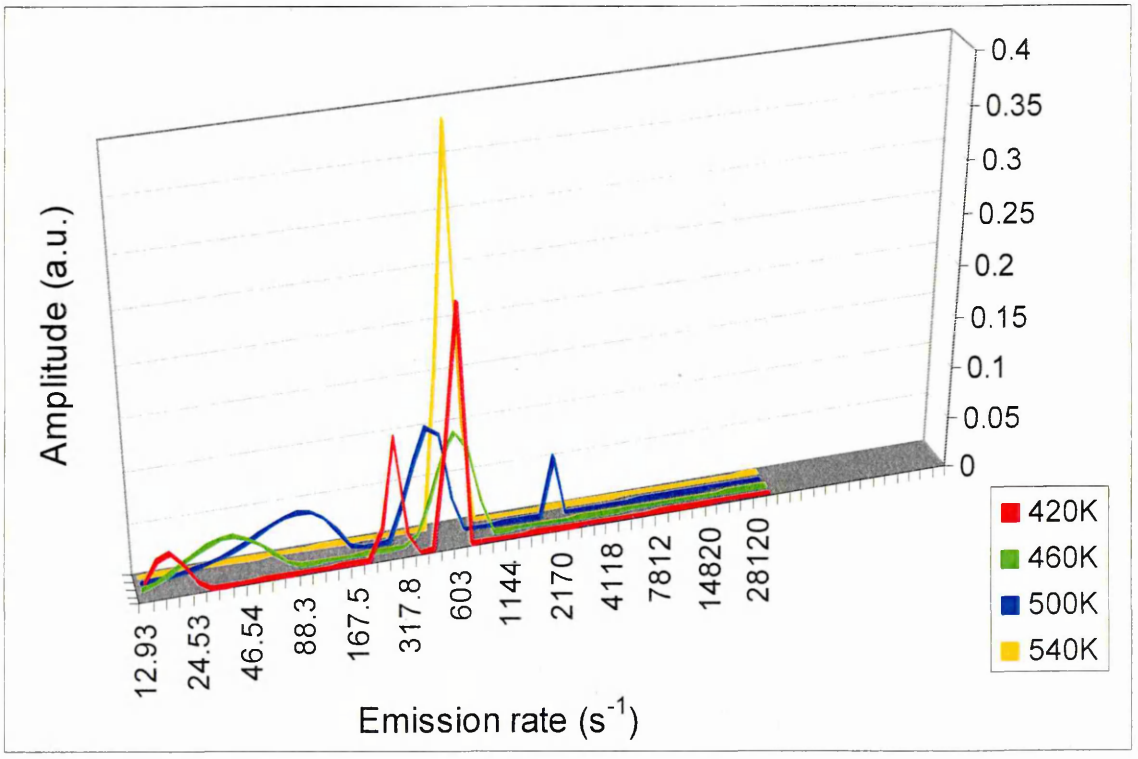

Fig. 8.23: LDLTS results for the high temperature defect in JEF8

For the low temperature defect in JEF8, LDLTS reveals that there are three emission rates at each temperature. The emission rate of these components however, does not constantly increase as was the case for the same defect in the diodes studied previously. The high temperature broad spectrum of JEF8 either has two or three components at each temperature with the high emission component remaining almost unaffected by the increase in temperature. In addition the lower emission components increase or decrease randomly with increasing temperature. To verify these observations it was attempted to calculate the activation energy of these components for the low temperature defect of JEF8 from the LDLTS data and this is shown in Fig. 8.24.

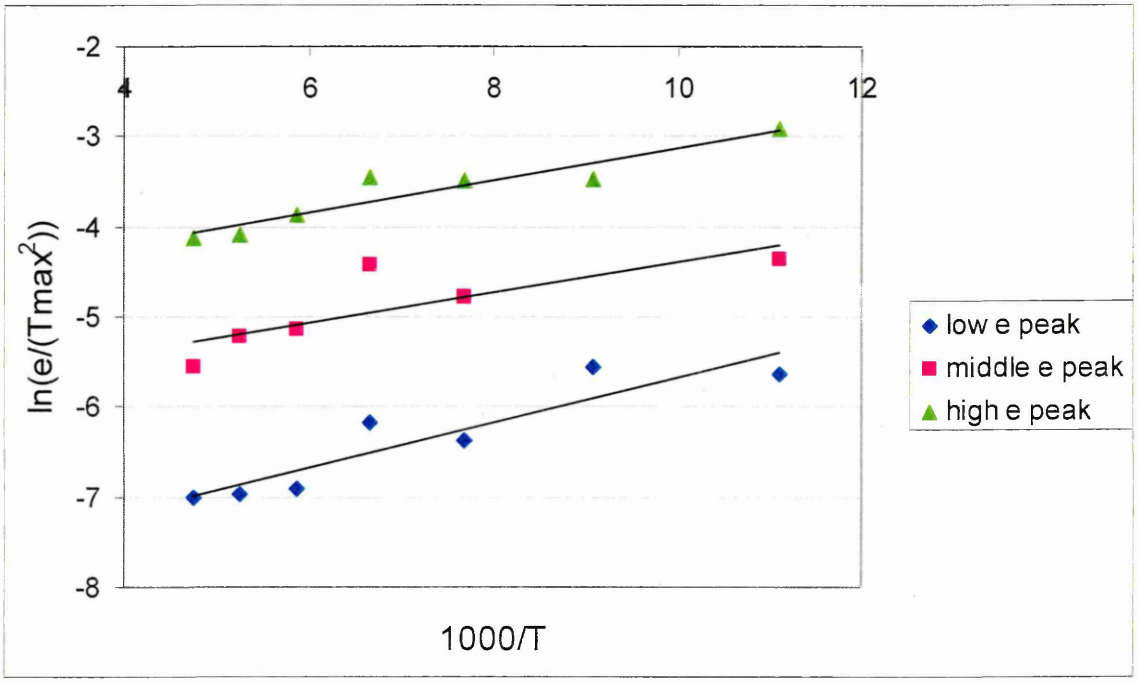

Fig. 8.24: Arrhenius plot of the emission rates of the low temperature defect in JEF8

The above graph shows that as the temperature increases, the y-axis value also increases, which suggests that the emission rate either decreases or remains unchanged. This result is once again the opposite of what should be taking place for the case of a point defect. It is therefore concluded that the many emission components appearing on the LDLTS spectra do not correspond to closely spaced point defects. Moreover this conclusion also applies to diodes JEF6 and JEF7, as the LDLTS spectra yielded similar results and further discussion and comparison among these diodes and between these and the p-n diodes will be presented in the last section of this chapter. Finally, LDLTS data indicate the presence of extended defects and this will be further investigated by the capture cross-section measurements that follow.

Using the data from the CV and DLTS measurements it was possible to calculate the concentrations of the traps that were observed in diodes JEF6-JEF8. The parameters used, were the capacitance in the absence of bias (C), the difference in capacitance (dC) from the peak of the DLTS spectrum and the carrier concentration (N_A) from the analysis of the CV results and these were inserted into Eq. (4.16). Table 8.2 shows the trap concentrations of both the low temperature and high temperature traps for these diodes.

Schottky diodes	Low Temp. peak (cm^{-3})	High Temp. peak (cm^{-3})
JEF6	$8.1 * 10^{16}$	$1.2 * 10^{16}$
JEF7	$1.8 * 10^{17}$	$5.8 * 10^{15}$
JEF8	$4.8 * 10^{15}$	$3.6 * 10^{15}$

Table 8.2: Trap concentrations of defects in diodes JEF6-JEF8

Table 8.2 shows that the trap concentration of the low temperature level is higher for JEF7 even though JEF8 has the highest B doping among these diodes. However, JEF7 has the highest B ionisation percentage. This result can be explained by the fact that the measured carrier concentration is used for the calculation of the trap concentration, as opposed to the doping concentration. Hence it is the B ionisation that determines the occupied trap concentration in diamond samples. On the contrary, the high temperature peak concentration is highest for JEF6 and decreases as the doping concentration increases. Due to the fact that this level appears at very high temperatures it can be suggested that the decrease of the trap concentration is due to the onset of metallic conduction which becomes more prominent for the more highly doped samples.

In order to further characterise the nature of the defects present in these samples, capture cross-section measurements were performed on the low temperature peak of diodes JEF6 and JEF7. These are plotted according to Eq. (4.18) in order to investigate the evolution of the capture kinetics with time. Fig. 8.25 and 8.26 show the results obtained for diodes JEF6 and JEF7 respectively. These measurements were performed with the same biasing conditions as DLTS while reducing the fill pulse length (t), for each temperature scan, from 5ms to 5μs and with a temperature range in the vicinity of the maximum of the DLTS peak.

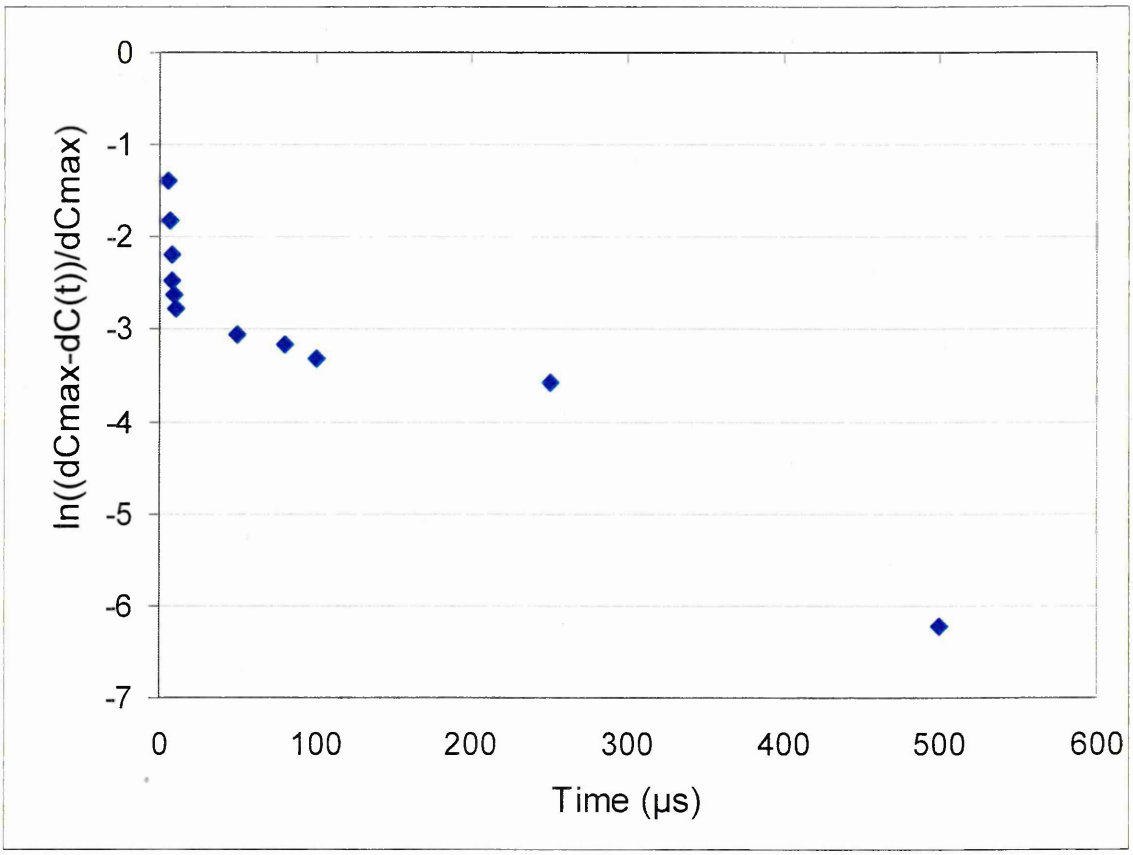

Fig. 8.25: Capture cross-section measurements for trap at 170K in JEF6

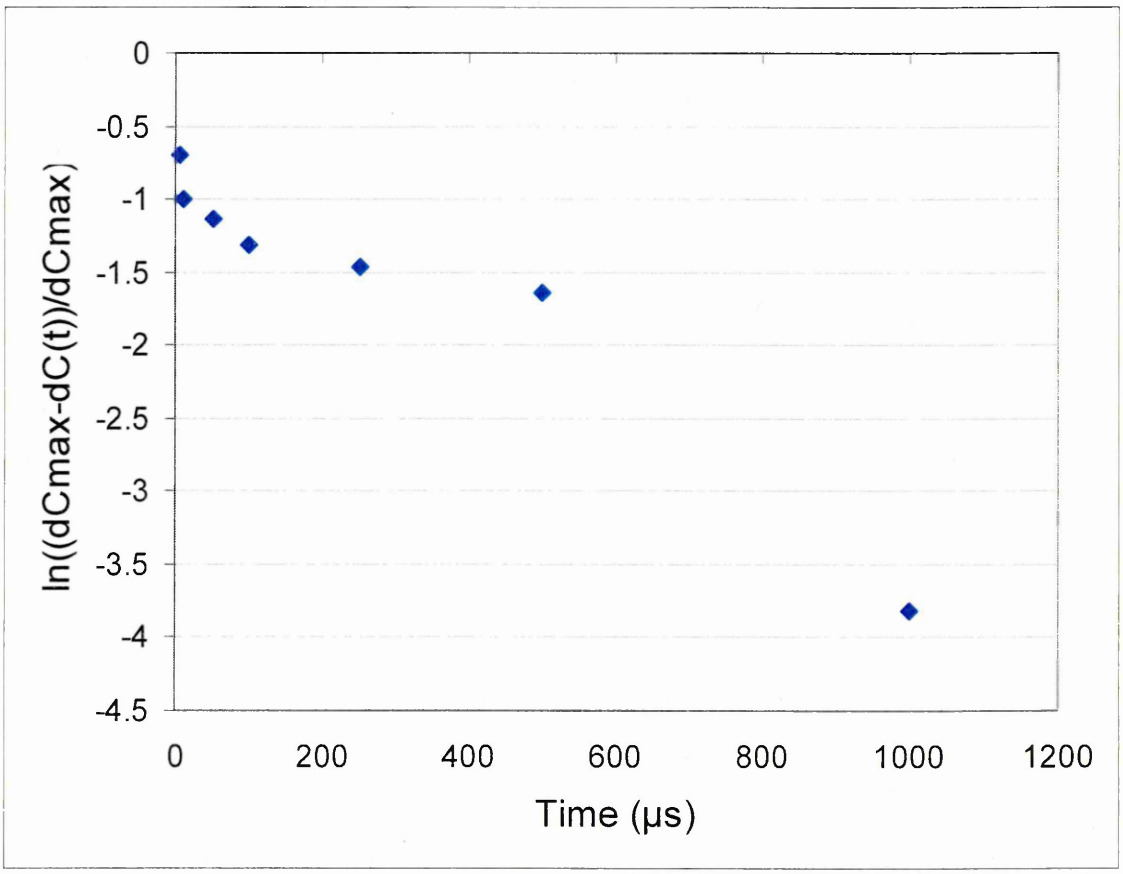

Fig. 8.26: Capture cross-section measurements for trap at 170K in JEF7

As can be seen from Fig. 8.25 and 8.26 the capture cross section cannot be calculated from the slope of the graphs as the points do not lie on a straight line. In particular for JEF7 it appears that the defect has a capture rate that changes exponentially with time which suggests that this is more likely an extended defect. The capture rate for JEF6 in Fig. 8.25 appears to have a combination of linear and exponential dependency with time. It is hence proposed that this capture behaviour is due to the presence of extended defects, where a Coulomb potential has been built-up because the initially trapped carriers repel any further charges, resulting in a diminished carrier capture probability with time. The LDLTS measurements are in accordance with this conclusion where it was seen that the capture rate was also not temperature dependent. It was observed that the capture rate was either unaffected by the change in temperature or even reduced for increased temperatures. Consequently, it is most likely that the profiled volume of these Schottky diodes, near the surface of the diamond films, contain extended defects.

8.3 Diamond on n-type silicon

This section presents the experimental results obtained from IV, CV, DLTS and LDLTS measurements of p-type diamond, grown on n-type Si, which therefore forms p-n diodes. The background doping concentration of the Si was $3*10^{15}cm^{-3}$ while the B doping of the HFCVD grown diamond films ranged from $7*10^{18}cm^{-3}$ to $7*10^{21}cm^{-3}$. The diamond in one of the samples was kept nominally undoped for reference purposes. Table 8.3 shows the doping concentrations of these four p-n diode structures.

p-n diodes	B concentration in diamond (cm^{-3})
JEF1	$7*10^{18}$
JEF2	$6*10^{20}$
JEF3	$7*10^{21}$
JEF4	Background doping only

Table 8.3: B concentration of diamond films for p-diamond/n-Si diodes

As already mentioned the purpose of investigating these p-n diodes is to depth-profile the diamond film near the interface with the Si. This is expected to be more easily achieved for the lightly doped samples as the depletion region may lie both on the p-diamond and n-Si sides of the junction. However, diodes JEF2 and JEF3 are very heavily doped with B and it is expected that only a small part of the depletion region

will be in the diamond. Comparison of the defects found in both the lightly and heavily doped diodes though, should provide a clear description of their location. Commencing with the undoped diamond diode, Fig. 8.27 shows the IV results obtained from JEF4 at different temperatures.

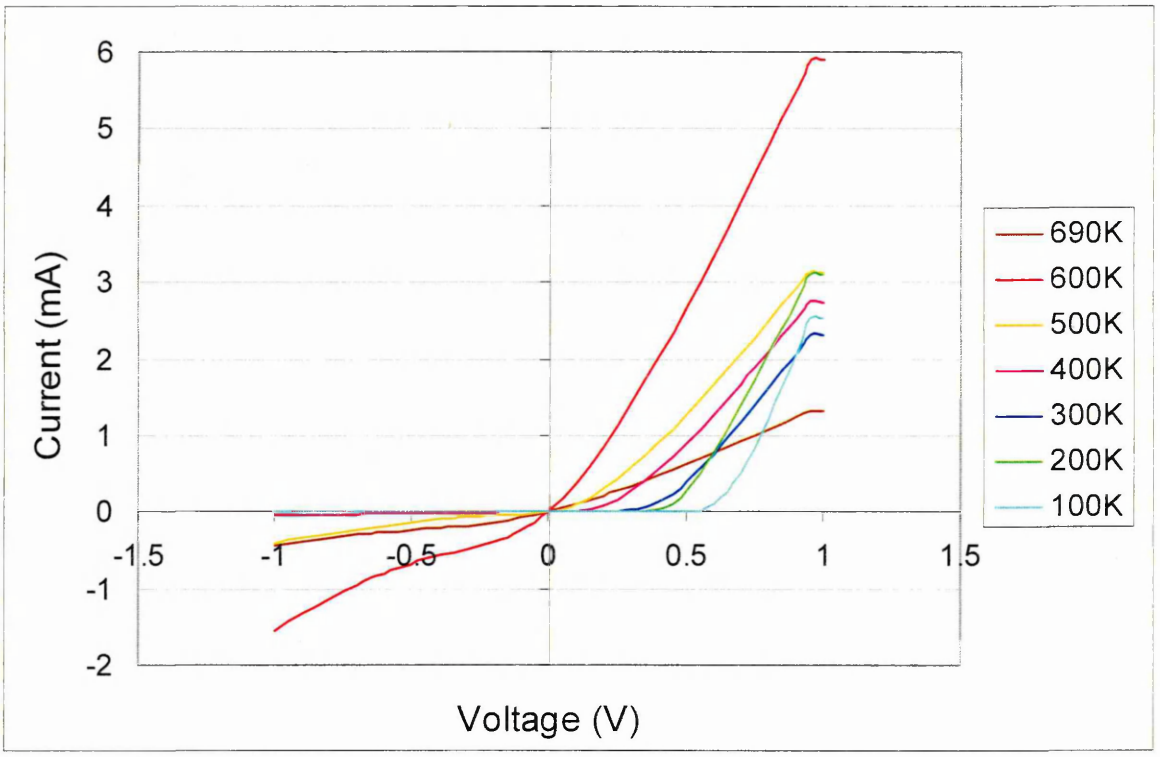

Fig. 8.27: IV measurements of JEF4 at different temperatures

The IV characteristics of JEF4 exhibit small forward and reverse current at most temperatures and increase rapidly above 500K. The reverse current at -1V and at 100K is 0.07μA, while at 300K and 600K it is 0.86μA and 1.55mA respectively. At the highest measured temperature of 690K both the forward and reverse current are seen to decrease again and the characteristic becomes more linear as opposed to diode-like. These results indicate that further measurements and analysis may be successfully performed on this diode.

Fig. 8.28 shows the IV data obtained for the low doped diode JEF1 at different temperatures. Some of the high temperature measurements for this diode have been performed with maximum reverse bias of 1V in order to prevent diode breakdown as the reverse current rises rapidly above 500K. In general the characteristics of this diode exhibit a less exponential behaviour when it is forward biased although the reverse current is relatively small until about 500K. At -1V reverse bias the current is 12μA at 100K, 56μA at 300K and 1.82mA at 600K. The forward current appears somewhat

reduced compared to that of the undoped JEF4 and this can be attributed to the B doping. Finally unlike JEF4, the current continues to increase at very high temperatures above 500K and the characteristic becomes more linear.

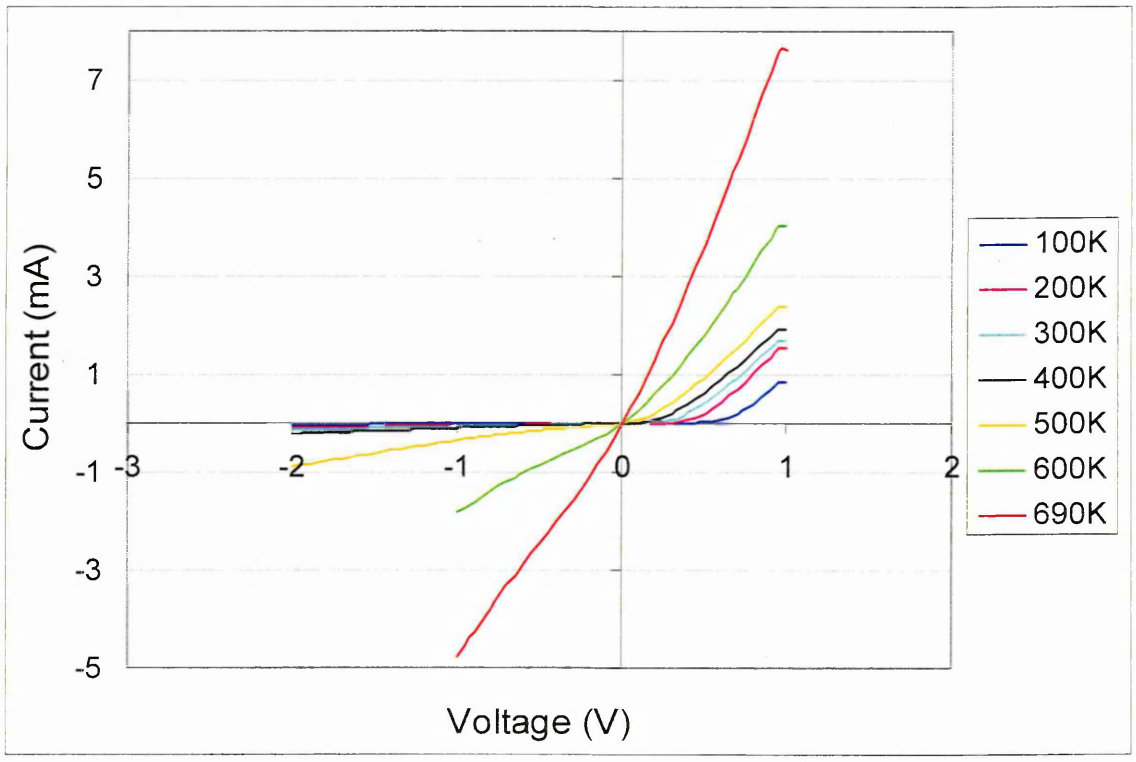

Fig. 8.28: IV measurements of JEF1 at different temperatures

The IV results for the highly doped diode JEF2 at different temperatures are shown in Fig. 8.29.

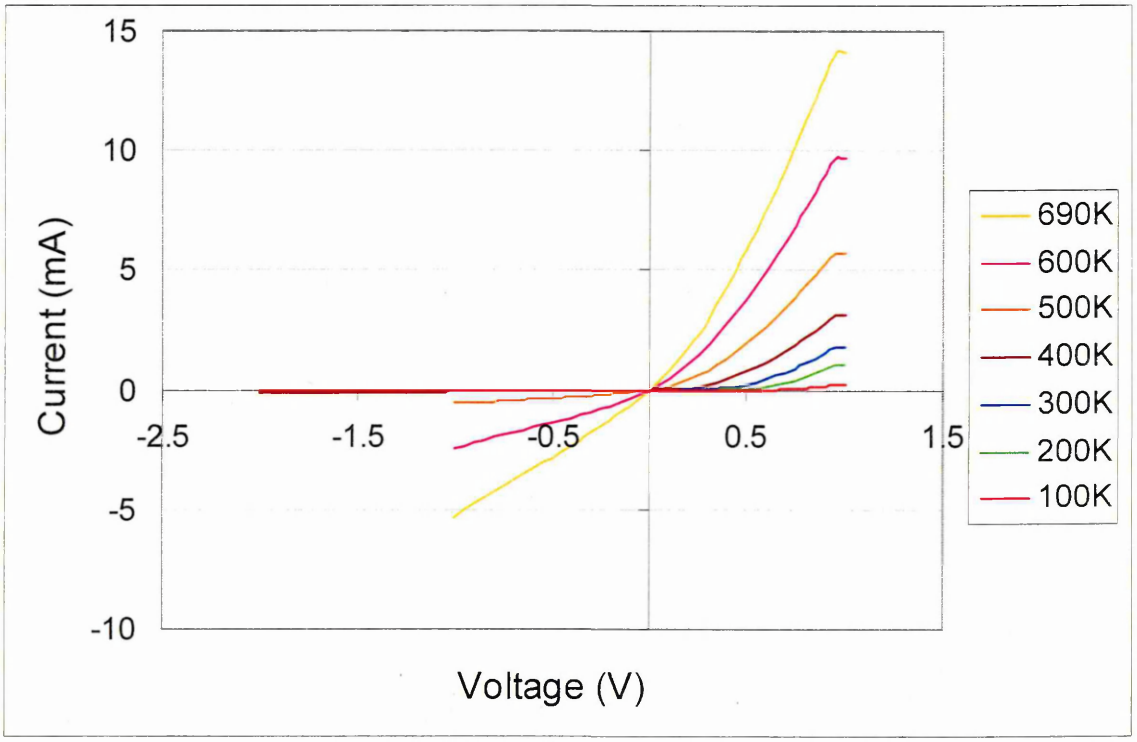

Fig. 8.29: IV measurements of JEF2 at different temperatures

The IV characteristics for JEF2 exhibit much higher forward current but smaller reverse current at most temperatures than JEF1. In addition the leakage current is increasing less rapidly with temperature until about 550K above which it increases much faster. This was the reason measurements at high temperatures were performed with a maximum reverse bias of 1V. At a bias of -1V the current is just 1.73μA at 100K, 20μA at 300K and 2.45mA at 600K. Therefore at relatively low temperatures the reverse current of JEF2 is lower than that of JEF1 even though JEF2 is more highly doped. The temperature of this transition, where the reverse current of JEF1 starts being lower than the corresponding leakage current of JEF2, is at around 400K. The forward current shows a slower exponential rise but more bias and temperature dependent. Despite the high forward current and slightly high reverse current at very high temperatures in diode JEF2, it is still possible to conduct further experiments as will be shown shortly.

Fig. 8.30 presents the IV measurements obtained from the most heavily B doped diode JEF3 at different temperatures.

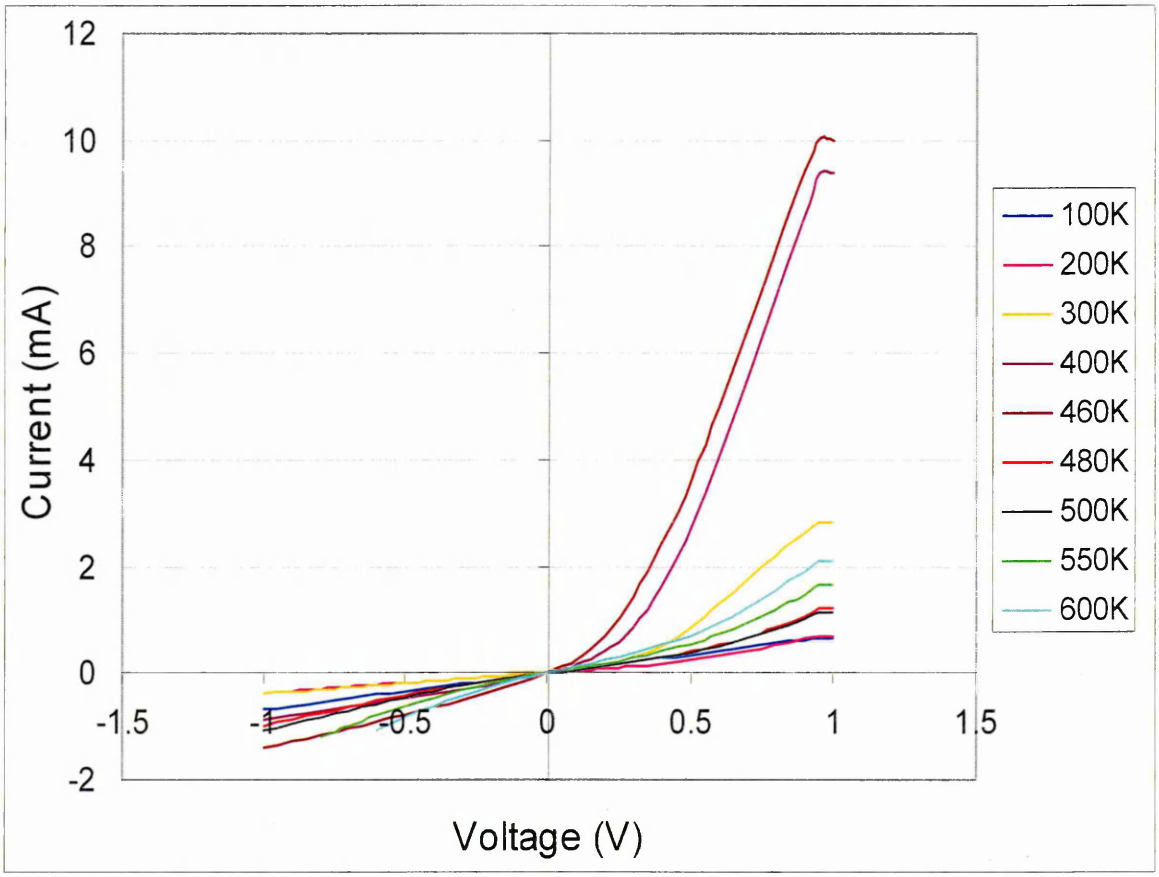

Fig. 8.30: IV measurements of JEF3 at different temperatures

The forward current in the above IV characteristics shows a peculiar development. It has its lowest value at 100K and as the temperature increases it rapidly increases until the temperature reaches 460K. Then it abruptly decreases to a value close to that at 200K and starts to slowly increase again until the highest temperature, however maintaining a value smaller than that of room temperature. The reverse current is lower than 2mA at all temperatures at -1V reverse bias and hence it is larger than in the undoped JEF4 but lower than that of JEF2. Its value at the maximum reverse bias of 1V is 0.68mA at 100K then it decreases to 0.38mA at 300K and has its maximum value of 1.41mA at 460K. Although the forward current is comparable to that of JEF2 in magnitude the overall diode characteristics of JEF3 are more linear than in any of the other p-n diodes and DLTS measurements are expected to be difficult or may not yield any results. In addition, as it was seen in Table 8.3, the B doping in JEF3 is very high which suggests that the depletion region lies in Si and hence DLTS should not yield any defects originating from the diamond. To illustrate the peculiar behaviour of the current in JEF3, the reverse and forward currents have been plotted against temperature in Fig. 8.31 at -0.5V and 1V respectively.

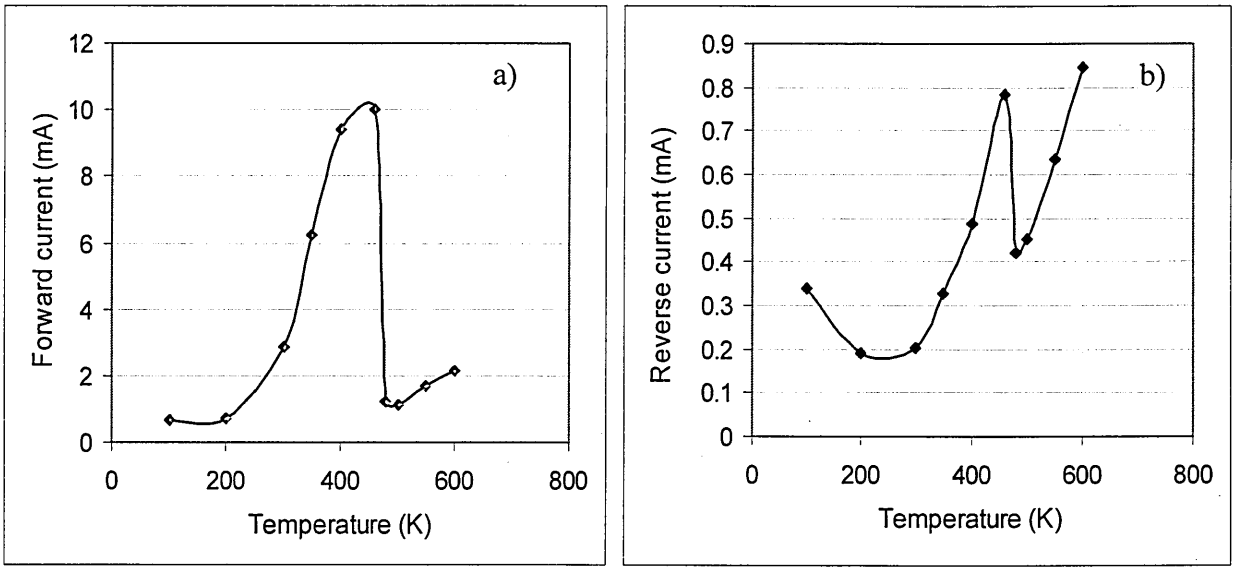

Fig. 8.31: a) Forward current in JEF3 at 1V against temperature and b) Reverse current in JEF3 at -0.5V against temperature

The forward current has a very sudden drop at 460K as can be observed in Fig. 8.31a), while at the same temperature the reverse current in Fig. 8.31b) attains almost its maximum value. This should perhaps be examined together with the CV results that will be shown shortly for this diode. However, it should be noted here that this behaviour could

perhaps be attributed to the fact that due to the high B doping the measured IV represents conduction in Si rather than in the diamond at this high temperature of 460K.

The following part presents the CV data obtained for these p-diamond/n-Si diodes as well as the analysis of the results in the form of carrier concentration-distance (N-x) profiles. Fig. 8.32 shows the CV and N-x profiles for diode JEF4.

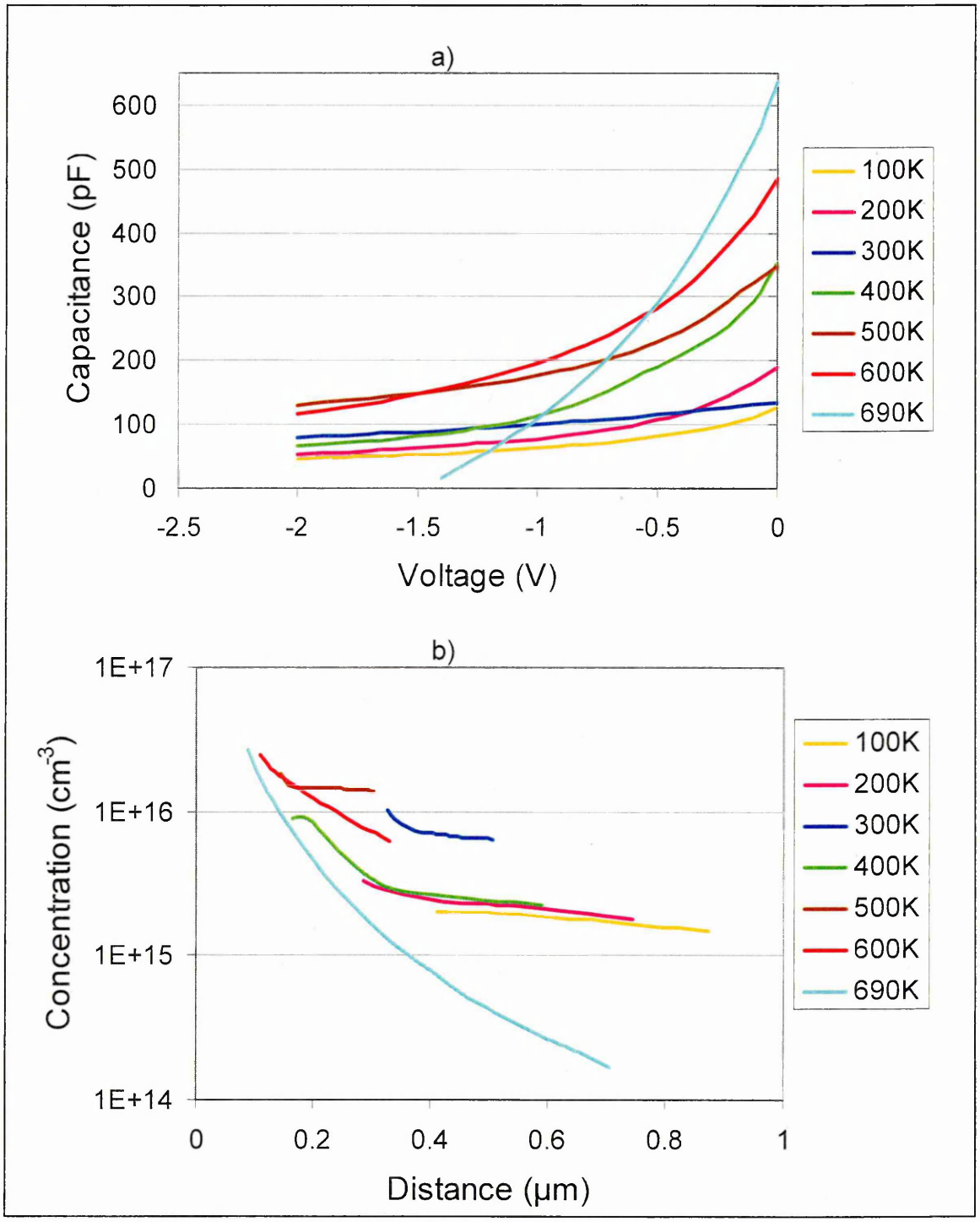

Fig. 8.32:a) CV and b) N-x profiles of JEF4 at different temperatures

The CV plots of JEF4 show that the capacitance is very bias dependent. The capacitance both at zero bias and -2V, consistently increases with increasing temperature except at room temperature where it appears slightly smaller. At the highest temperature of 690K however, the slope of the capacitance is much more abrupt and the maximum applicable bias was -1.4V before the capacitance became zero. This rapid change in capacitance indicates a large change in carrier concentration as it can be verified from the N-x plot at 690K. As the diamond in this diode is undoped the depletion region exists both in the diamond and Si. Compared to the Schottky diodes this means that the depletion region is larger as can be confirmed from the N-x profiles. The carrier concentration is around $5*10^{15}cm^{-3}$ and it slightly increases for higher temperatures.

Fig. 8.33 illustrates the CV and N-x results for diode JEF1 at different temperatures.

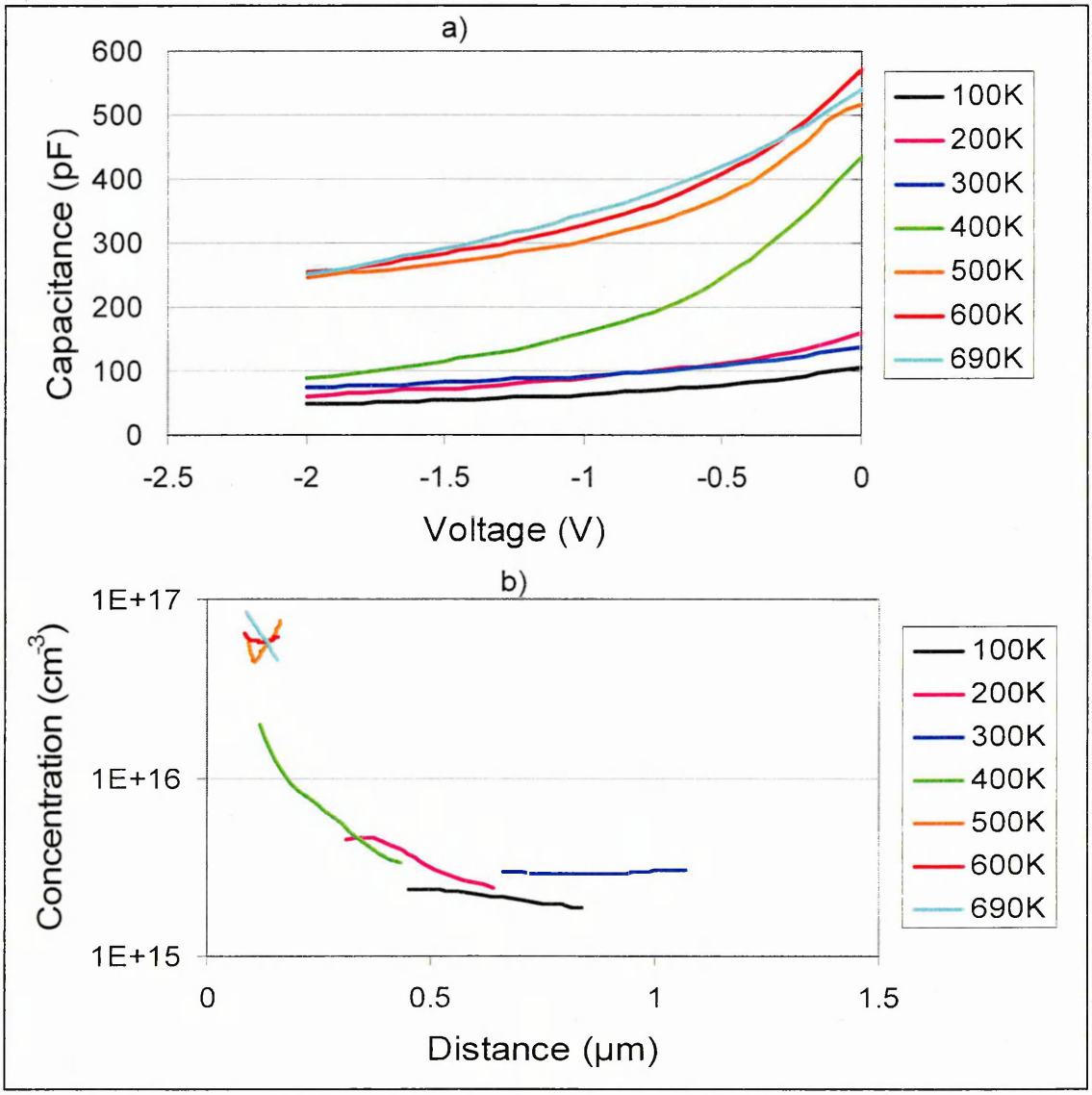

Fig. 8.33: a) CV and b) N-x profiles of JEF1 at different temperatures

As seen from the CV plots the capacitance increases with increasing temperature in this diode, and above room temperature it becomes more bias dependent. In addition, above 300K the capacitance increases more rapidly. This is reflected in the carrier concentration profiles where the concentration at temperatures above 400K in particular, is around $1*10^{16}cm^{-3}$ while below this temperature the concentration is lower at around $6*10^{15}cm^{-3}$. This result suggests a very temperature dependent carrier concentration. Indeed from the IV characteristics of Fig. 8.28 for this diode, it is obvious that both the forward and reverse current rise swiftly above the temperature of 400K. From Table 8.3 for this diode the B ionisation percentage is 0.08% which is much lower compared to that of the Schottky diodes of the previous section.

The CV and N-x results for diode JEF2 are shown in Fig. 8.34 at different temperatures.

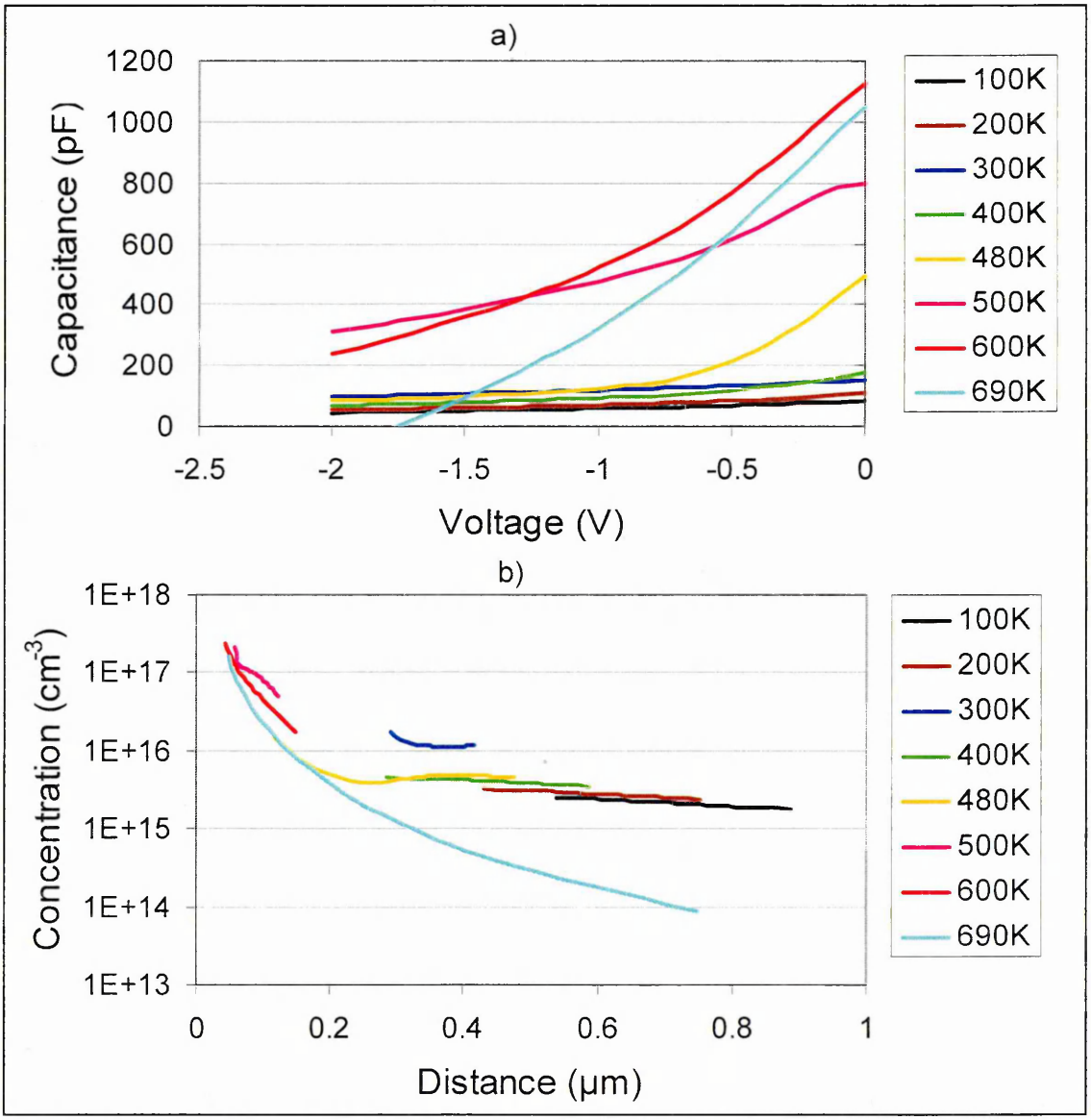

Fig. 8.34: a) CV and b) N-x profiles of JEF2 at different temperatures

From the CV results of Fig. 8.34 it can be seen that the capacitance is low until the temperature of 400K is reached and then it increases very rapidly with temperature and also with increasing reverse bias. In particular the capacitance at the highest temperature of 690K decreases almost linearly to zero and hence the maximum possible applied bias was -1.7V. Once again this rapid capacitance decrease is depicted by a large decrease in the carrier concentration with applied bias. The carrier concentration is slightly higher in this sample with a value of $1*10^{16}cm^{-3}$ at room temperature. Above 480K the measured carrier concentration is much higher at about $8*10^{16}cm^{-3}$. Compared with the B doping of Table 8.3 for this diode, the B ionisation percentage is 0.001% which is on average 3 orders of magnitude lower than that of the Schottky diodes.

The CV and N-x results obtained from diode JEF3 are shown in Fig. 8.35 for different temperatures.

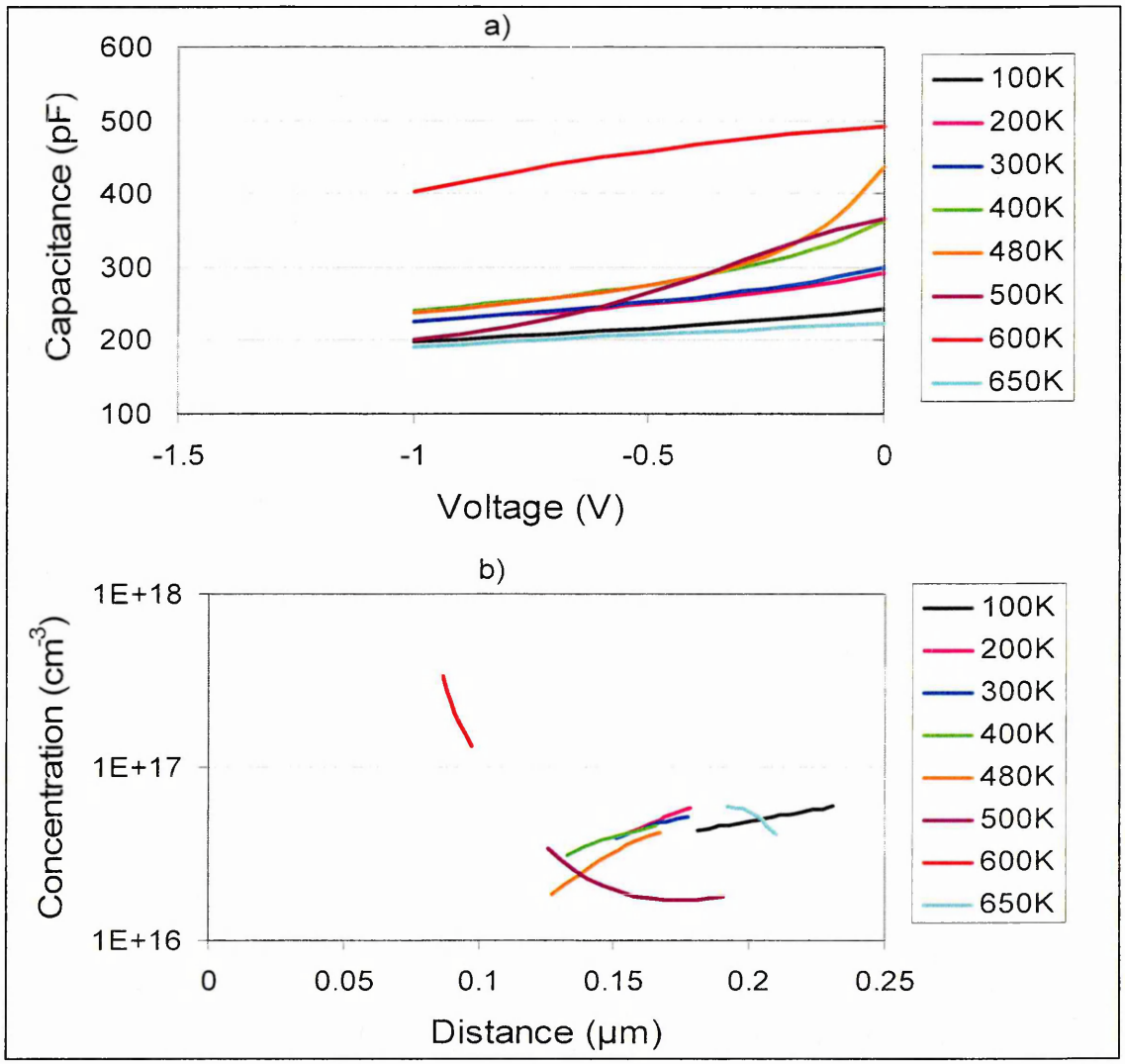

Fig. 8.35:a) CV and b) N-x profiles of JEF3 at different temperatures

The CV results of JEF3 show that the capacitance increases normally with temperature until 480K but above that temperature there are some peculiar characteristics. From 500-600K the CV results are not diode-like as the capacitance decreases rapidly with increased bias. In addition, at the highest temperature of 650K, the capacitance has dramatically decreased to values even below those at 100K. The carrier concentration recorded from the N-x profiles at room temperature is $5*10^{16}cm^{-3}$ which yields a B ionisation percentage of 0.0007%. Between 500 and 600K the concentration appears increased and shows a more exponential dependence with bias. This coincides with the fact that the IV characteristics of Fig. 8.30 for this diode exhibit a sudden decrease above 480K. The very high B doping would mean that the diode should exhibit metallic conduction if the depletion region lied on the diamond side. However, it is suggested that since this is a p-n diode, the entire depletion region lies in Si. This explains the low measured carrier concentration, since at very high temperatures scattering mechanisms may limit conduction, in a material such as Si with a small bandgap even when the doping is low. Both the IV measurements of Fig. 8.30 and the CV data of Fig. 8.35 seem to indicate a sudden change in carrier concentration at elevated temperatures, therefore supporting the aforementioned suggestion. Hence DLTS and LDLTS measurements are not expected to reveal any traps since the Si is of very high quality.

DLTS was performed with different biasing conditions for all the diodes in order to reveal all existing traps. Although JEF4 contains the undoped diamond film and was intended as a reference sample it is more advisable to first examine diode JEF3. This is because the diamond in JEF3 is very highly doped with B and therefore the depletion region entirely lies on the Si side of the junction. By investigating diode JEF3 any potential defects in Si will be revealed, which will be used as a guide to distinguish between defects in diamond and Si in the remaining diodes, where part of the depletion region is located in diamond. However, it should be mentioned that the quality of Si used for these samples is excellent as it is commercially available Si. DLTS was performed with reverse bias -1V and fill pulse 0.5V from 100K-550K, with different rate windows and fill pulse length of 1ms. The resulting spectra are shown in Fig. 8.36 for the rate window $200s^{-1}$. Different biasing conditions and rate windows were also used in order to ensure that the obtained spectra reflect the entire range of defects and the same result was obtained.

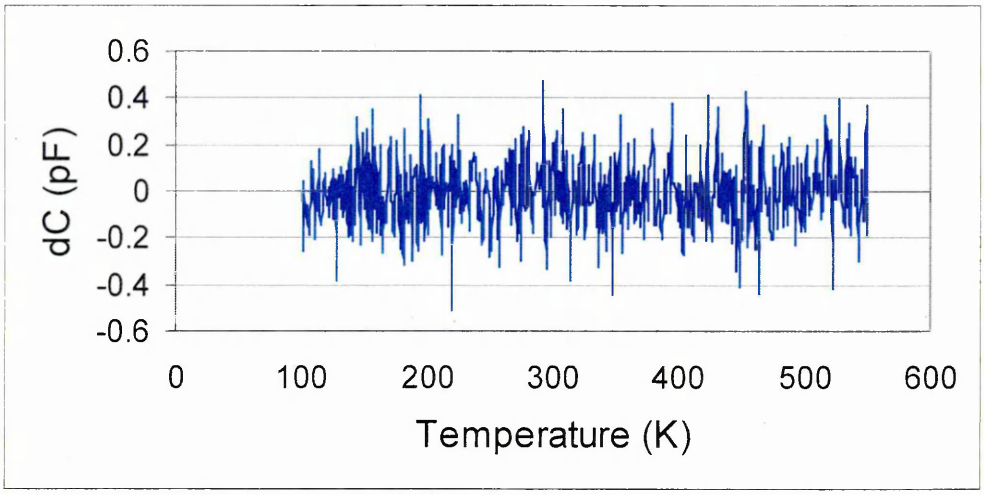

Fig. 8.36: DLTS spectra of JEF3 with reverse bias -1V, fill pulse 0.5V and rate window 200s^{-1}

From the above spectra it can be seen that no defect levels were detected in JEF3 and this applied to all the different biasing conditions that were implemented for this sample as well as to all rate windows used. Consequently no LDLTS or other measurements were performed on this diode. However, this is a very important result since it confirms that there are no defects in Si and any defects observed in the other diodes will be situated in the diamond side of the p-diamond/n-Si junction.

The DLTS results for diode JEF4 are shown in Fig. 8.37 from 90K to 690K and with reverse bias -2V, fill pulse 1V and fill pulse length 1ms.

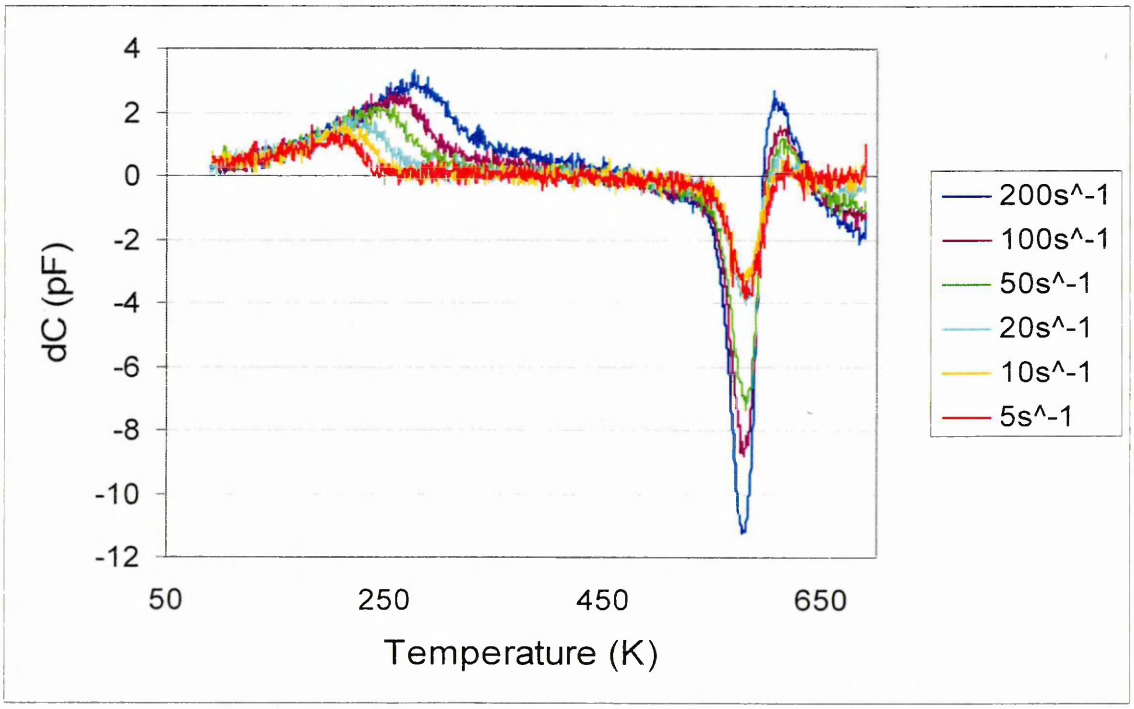

Fig. 8.37: DLTS spectra of JEF4 with different rate windows, reverse bias -2V and 1V fill pulse

The DLTS spectra of JEF4 reveal a very broad trap level, covering a wide temperature range from 100K to 400K. This appears as a single trap in this spectrum, although due to the wide temperature range it covers and the broad shoulder extending above 300K, which results in an asymmetric characteristic, it is possibly due to more than one defect. As expected the peak of the trap shifts towards lower temperatures as the rate window reduces indicating the activation energy of this trap can be calculated. At very high temperatures, around 570K, there is a reversal of capacitance which results in a peak that could be due to minority carrier emission. However, the peak of this spectrum increases for increasing rate windows and hence it does not result in a meaningful activation energy. Therefore this peak will not be discussed further as it may be due to a system error or a result of heating up Si at very high temperatures. An Arrhenius plot was constructed in order to find the activation energy of this defect and this is shown in Fig. 8.38.

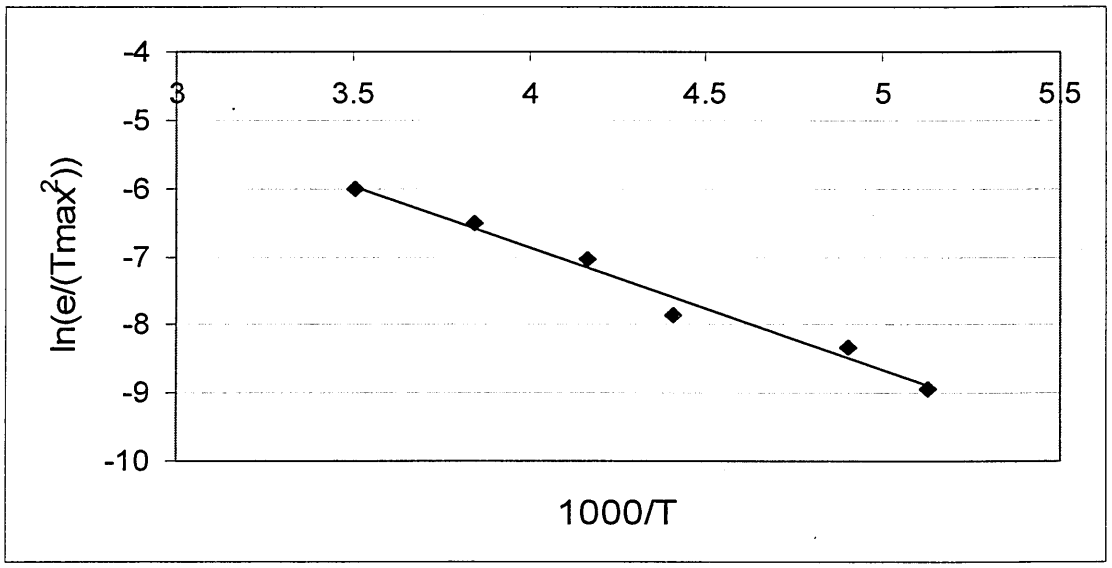

Fig. 8.38: Arrhenius plot of JEF4 with RB=-2V, FP=1V

As can be seen from Fig. 8.38 the points of emission rate-peak maximum temperature from the DLTS spectra are virtually on a straight line and hence the activation energy of the trap can be calculated. This was found to be 0.15eV. Since no such defect was observed in the previous diode JEF3, this level is located in the diamond and it is a hole trap, since it has a positive capacitance transient. Therefore this trap is located at 0.15eV above the valence band. Different biasing conditions that cause saturation of the hole trap detected at 270K were applied, in an attempt to separate any closely spaced levels within the temperature range of 90-400K. Fig. 8.39 shows the DLTS spectra

obtained with reverse bias -2V and fill pulse 2V that injects more majority carriers in the depletion region.

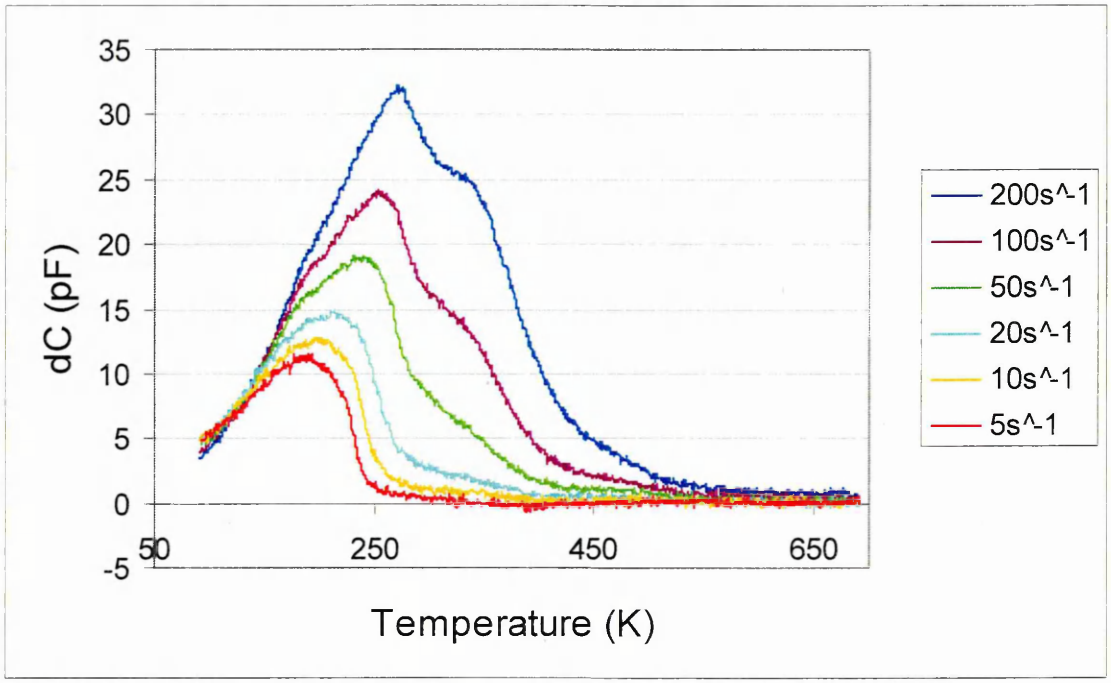

Fig. 8.39: DLTS spectra of JEF4 with different rate windows, reverse bias -2V and 2V fill pulse

From Fig. 8.39 it is clear that there are at least two closely spaced defects from 90-400K when the fill pulse is increased. The peak of the low temperature defect is clear at all rate windows used while that of the high temperature level is only apparent with some of the rate windows which make the activation energy calculations more difficult. However, an Arrhenius plot was constructed for these two peaks with all the available points for each defect and this is shown in Fig. 8.40.

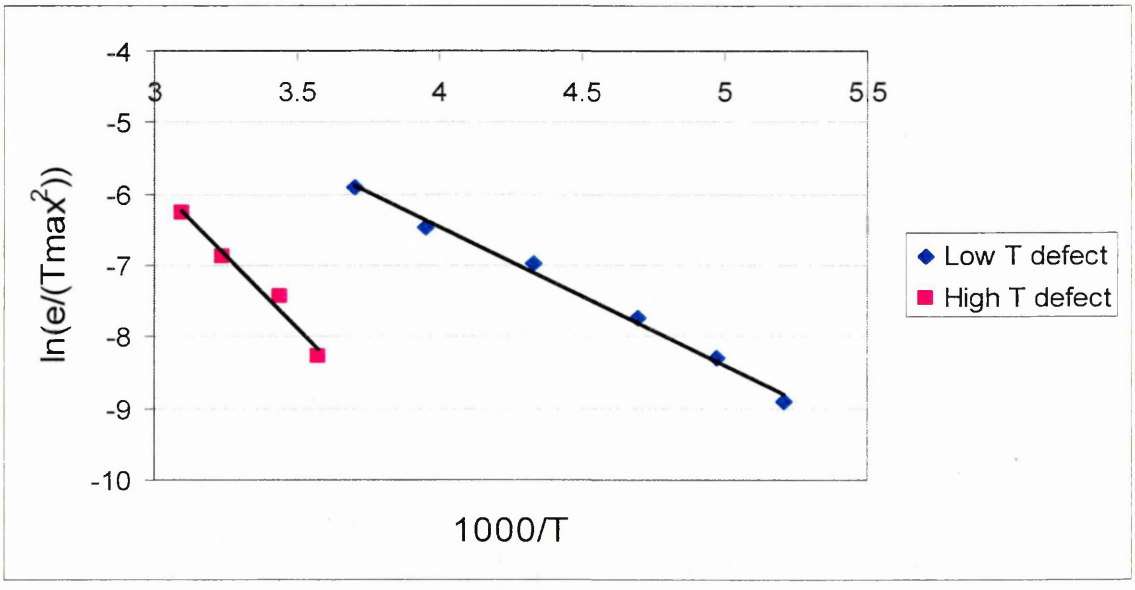

Fig. 8.40: Arrhenius plot of low and high temperature defect of JEF4 with RB=-2V FP=1V

The activation energy of the low temperature level was found to be 0.16eV and that of the high temperature level is 0.35eV. The activation energy value of the high temperature level is very close to that of the B acceptor level (0.38eV) but higher resolution measurements provided by LDLTS may be able to determine this value more accurately or provide more information on whether there are more defects within the temperature range of 100-400K.

The DLTS spectra of diode JEF1 with reverse bias -2V, fill pulse 1V and different rate windows are shown in Fig. 8.41.

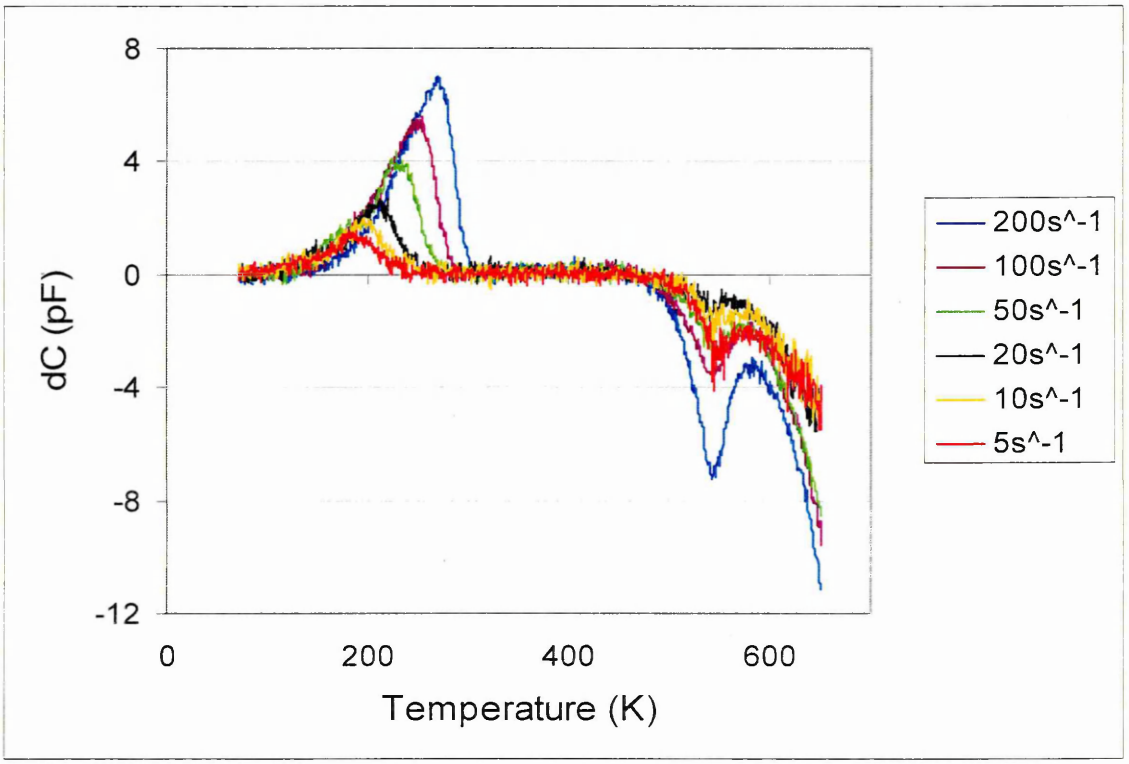

Fig. 8.41: DLTS spectra of JEF1 with different rate windows, reverse bias -2V and 1V fill pulse

Fig. 8.41 reveals a broad peak at about 260K which is similar to that observed in JEF4. This is somewhat narrower in this diode covering a temperature range from 100-290K and it contains a shoulder that extends mostly towards lower temperatures. The peak of the defect is shifted to lower temperatures for lower rate windows indicating that it is possible to calculate its activation energy. Due to its asymmetric shape and broad temperature range of about 200K it probably consists of other closely spaced defects although efforts to separate these by using different biasing conditions did not yield any other levels. Application of larger positive fill pulse was performed in order to saturate the defects, as in the case of JEF4, but this did not reveal any other levels. The

capacitance reversal at high temperatures is again present, similarly to JEF4, although it does not correspond to any defects. The Arrhenius plot for the defect at 260K is shown in Fig. 8.42.

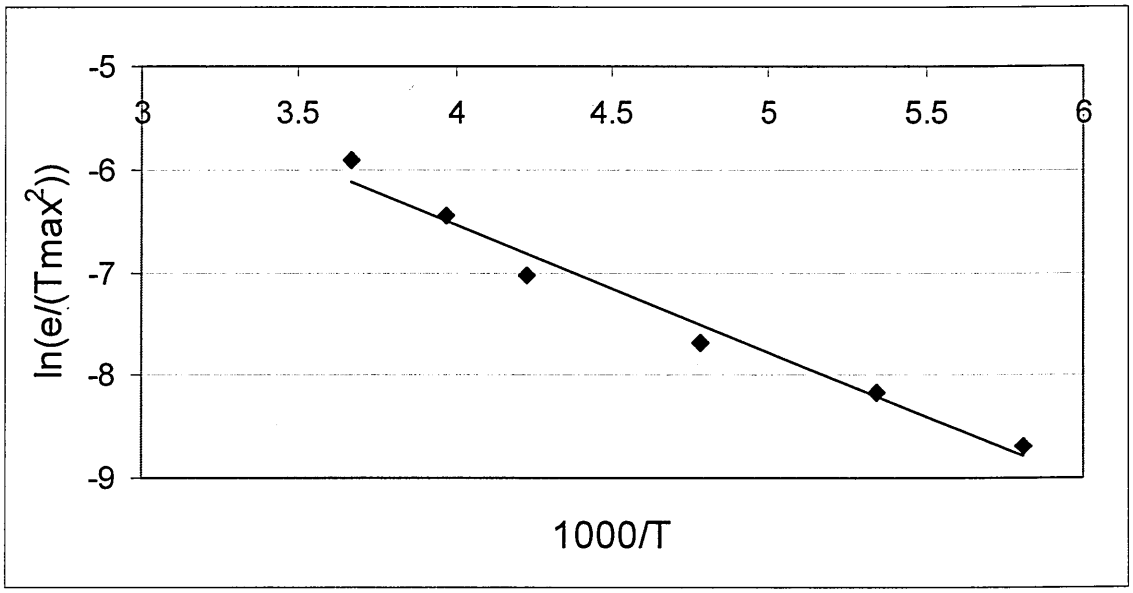

Fig. 8.42: Arrhenius plot of defect at 260K of JEF1with, reverse bias -2V and 1V fill pulse

From Fig. 8.42 it was possible to calculate the activation energy that corresponds to the DLTS peak at 260K for JEF1 since the emission rate-peak maximum temperature pairs lay on a straight line. This was found to be (0.11 ± 0.05) eV above the valence band and it is slightly lower than that found for JEF4 in Fig. 8.38. This DLTS peak may contain more defects similarly to JEF4 and one of them may be the B acceptor level which reduces in activation energy for higher doped diodes, such as JEF1. It may be the reason the activation energy of the observed defect in JEF1 is lower than that of JEF4. LDLTS measurements that may provide more information about the nature of this defect will be presented in the following section.

The last p-diamond/n-Si diode examined was the highly doped JEF2. However as it was seen earlier, the B ionisation in the diamond film of this diode was lower than JEF1. Therefore in order to fill any majority traps in the depletion region, a higher forward fill pulse will need to be applied since there are fewer carriers. DLTS measurements were performed with different biasing conditions and the most relevant results are shown here. Fig. 8.43 shows the DLTS spectra obtained with reverse bias -2V and fill pulse-2V at different rate windows. A high temperature minority carrier trap was revealed at around 480K that has not been observed in the other diodes. In addition, the low temperature peak at around 200K that was observed in the previous diodes is still

present but is now smaller in magnitude and its signal appears noisier because the high temperature peak is larger. The insert shows the majority trap at 200K separately for clarity, as it is hard to distinguish due to the magnitude of the minority trap.

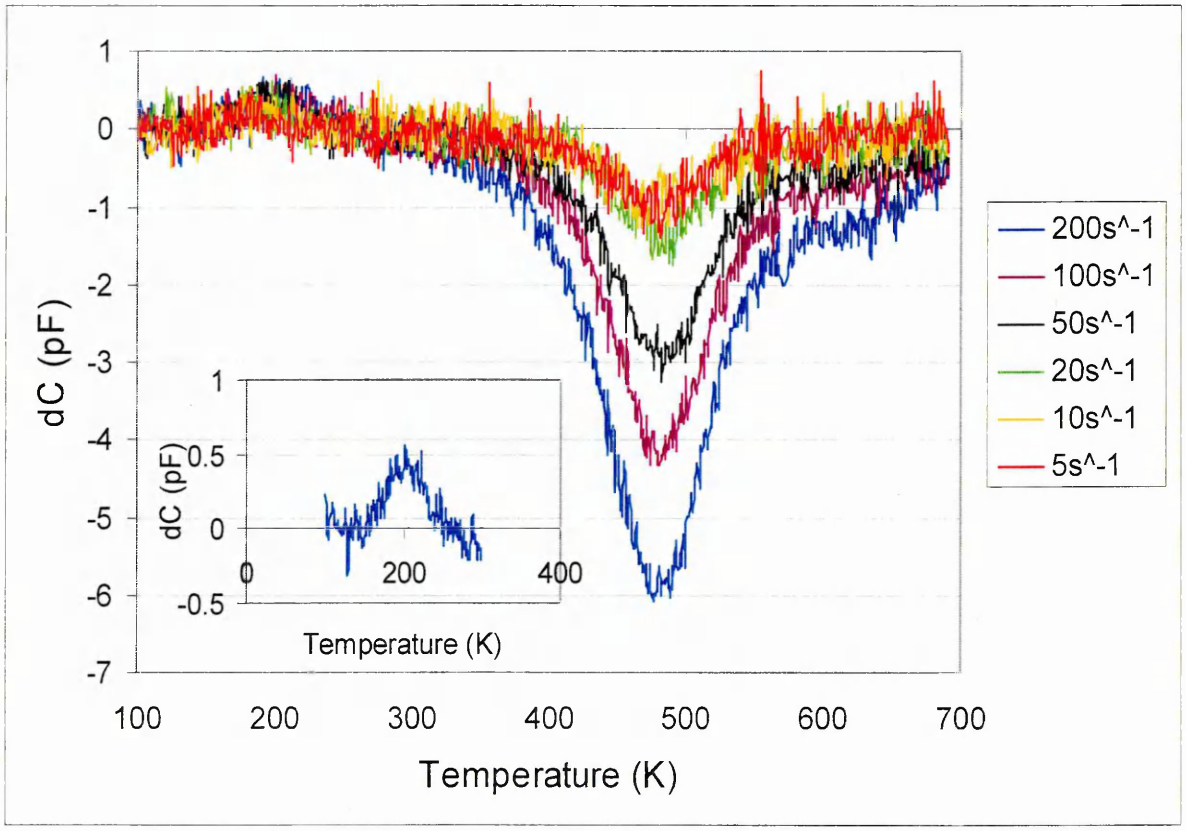

Fig. 8.43: DLTS spectra of JEF2 with different rate windows, reverse bias -2V and 2V fill pulse. The insert shows the majority trap at 200K plotted separately for clarity for the rate window 200s^{-1}.

It is important that even in such a highly doped diode the low temperature level is still present due to the low ionisation percentage of B, as this entails that DLTS can be applied to very highly doped samples. The peak of the minority carrier trap reduces with temperature slightly but it is sufficient for the calculation of its activation energy. Varying of the biasing conditions did not yield any other closely spaced defects. The Arrhenius plots of the two defects for this diode are shown in Fig. 8.44 and 8.45. For the low temperature peak it is seen from Fig. 8.44 that the points fit well on a straight line and the activation energy of this hole trap was found to be 0.37eV above the valence band. Compared to the literature this is remarkably similar to the activation energy of the B acceptor level. A less ideal straight line fit of the peak temperature-emission rate points developed for the high temperature defect, however its activation energy was found to be 2.3eV which is expected since it is located at such high temperature.

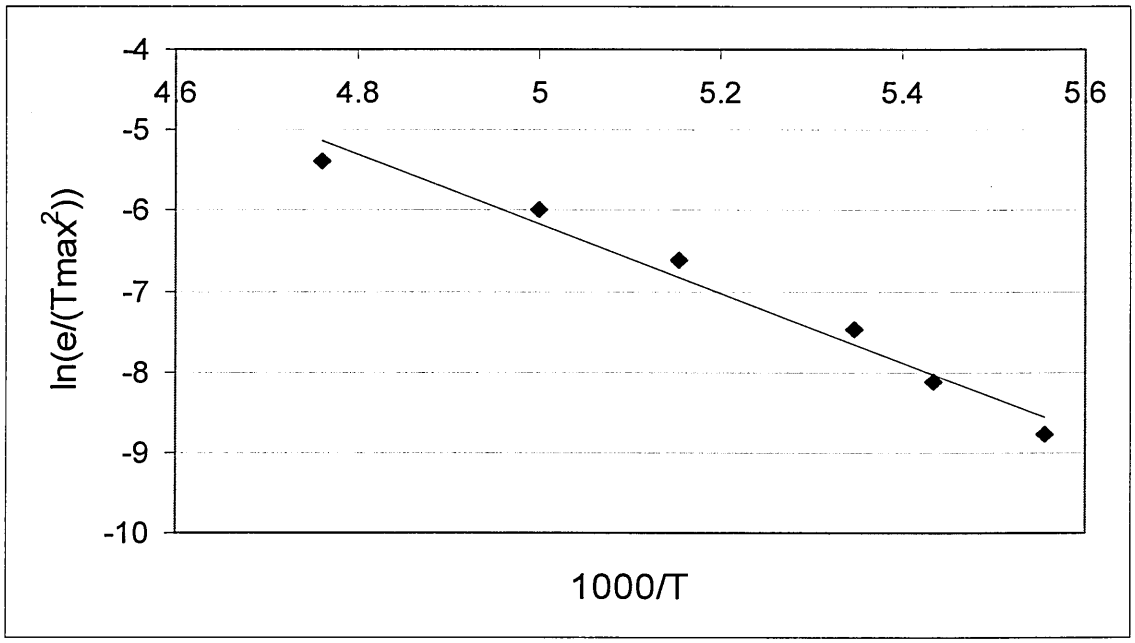

Fig. 8.44: Arrhenius plot of the low temperature 200K defect of JEF2

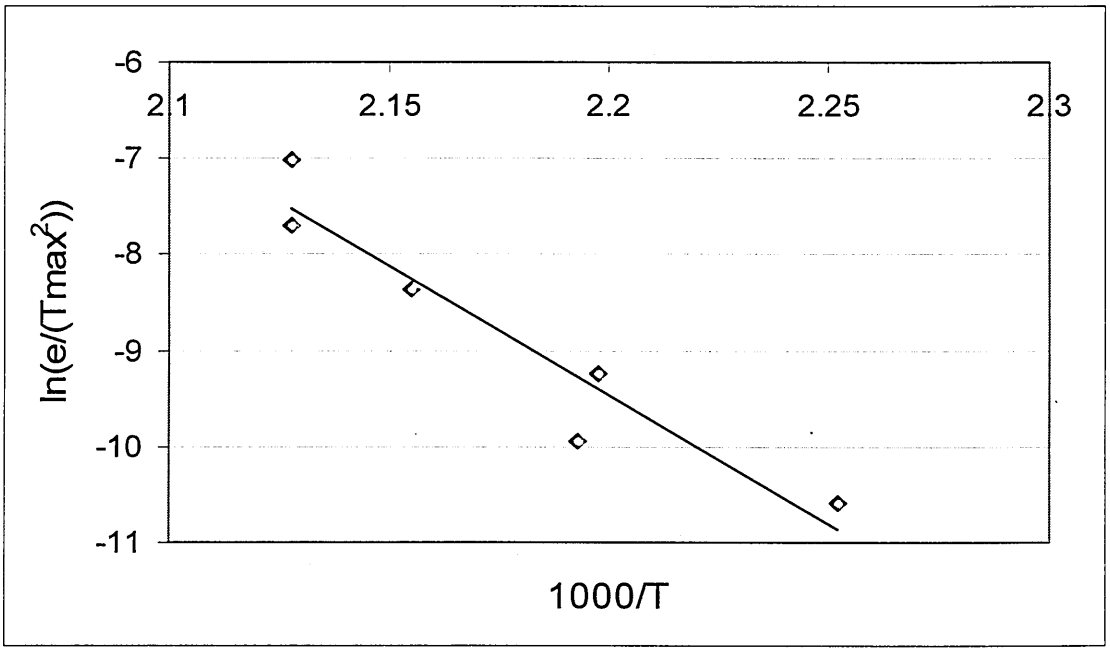

Fig. 8.45: Arrhenius plot of the minority carrier trap at 480K of JEF2

Due to the fact that this is a minority (electron) trap, it is therefore located at 2.3eV below the conduction band which makes it a deep level trap in the diamond bandgap. The low temperature trap was detected in the previous diodes that had lower carrier concentrations and it was identified as a defect on the diamond side of the p-n junction. JEF2 has slightly higher carrier concentration, as was seen from the CV measurements, and about one sixth of the depletion region lies in the diamond. However, the low temperature peak corresponding to a hole trap in the diamond side of the junction is still present. Consequently it is suggested that the high temperature minority trap of JEF2,

that appears on the same spectrum as the peak at 200K, must also be located in diamond and this explains the reason it was determined to be an electron trap. The fact that the activation energy of the 200K level is so similar to the B acceptor level and is so clearly identified in this diode, indicates that the carrier concentration is not very high, irrespective of the B doping. This was verified from the CV measurements that showed very low B ionisation percentage. The fact that the previous p-n diodes exhibited this level much closer to the valence band, compared to JEF2, can perhaps be attributed to the presence of more than one level. If indeed more than one level were encompassed by the low temperature peak of the previous diodes and DLTS was not able to distinguish all of them, then the activation energy from the spectra would correspond to the dominant level with the highest emission rate. This level was perhaps other than the B acceptor level and hence the activation energy of the ensemble was lower, than the one clear defect observed at 200K in JEF2.

LDLTS was performed at the same biasing conditions as DLTS for these p-n diodes. The broad peak that was detected in JEF4 was further analysed with LDLTS. Because of the multitude of LDLTS peaks that were acquired at this broad temperature range a few results will be shown here initially in the form of LDLTS spectra and the rest of the results will be illustrated in the form of peak emission rate against temperature to aid further analysis. Fig. 8.46 shows the LDLTS spectra obtained at 180K, 280K and 380K as an example to illustrate the number of emission rate components that are present.

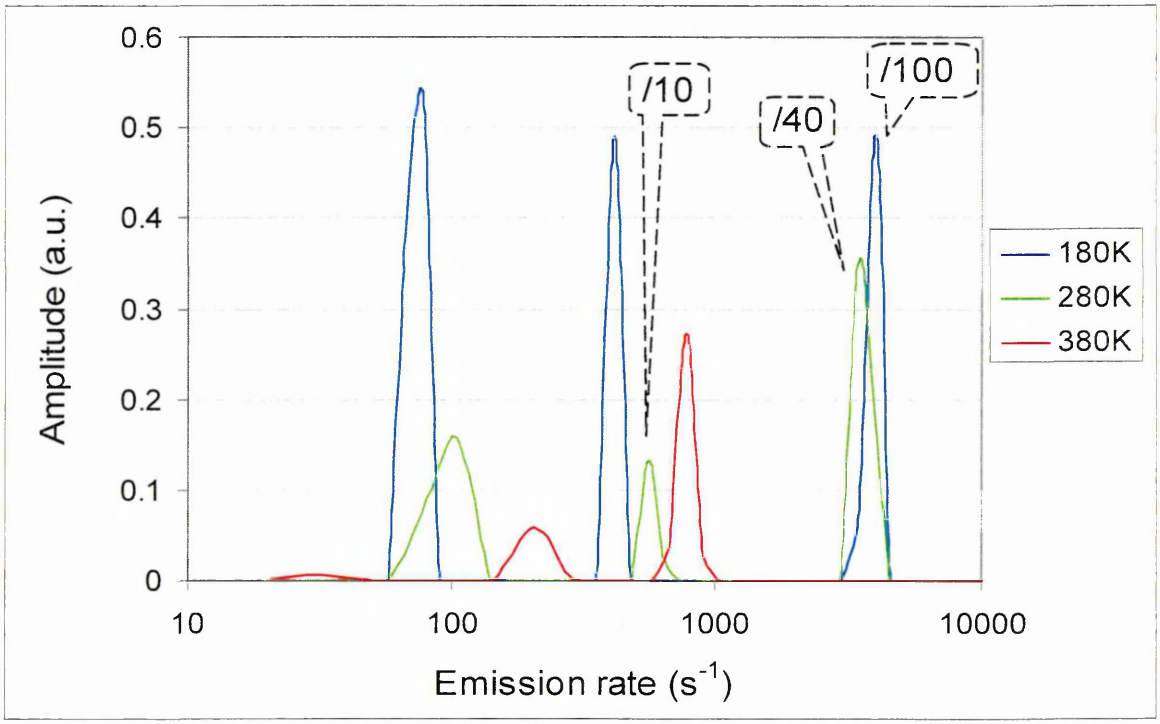

Fig. 8.46: LDLTS spectra of JEF4 at 180K, 280K and 380K

The LDLTS spectra of Fig. 8.46 reveal three separate emission rates at each temperature. Such a result is expected since the DLTS spectrum of JEF4 covered a very broad temperature range and it is bound to be consisted of more than one defect. From the experimental data it was observed that the high emission rate was much larger at lower temperatures from 140K to 300K. To assist the comparison of these LDLTS peaks the high emission rate shown at 180K had to be scaled down by 100 times while the high and middle peaks at 280K had to be scaled down 40 and 10 times respectively as shown in Figure 8.46. As the temperature increased in the interval from 140-300K the high emission rate slowly reduced in amplitude and continued to do so as the temperature increased further. At 380K it is of comparable amplitude with the rest of the emission rates. The emission of all three peaks is very scattered with temperature and reduces as the temperature increases which is the opposite from what should be expected from point defects. LDLTS was performed at the entire temperature range 100-400K of the DLTS spectra for these defects but the emission of the three observed levels did not allow meaningful activation energy calculations since they increased with reducing temperature. However the fact that three emission rates are consistently observed at all temperatures clearly demonstrates the presence of three levels and shows improvement over the DLTS technique. Fig. 8.47 shows the peak emission of the high emission rate of Fig. 8.46 to demonstrate its evolution with temperature.

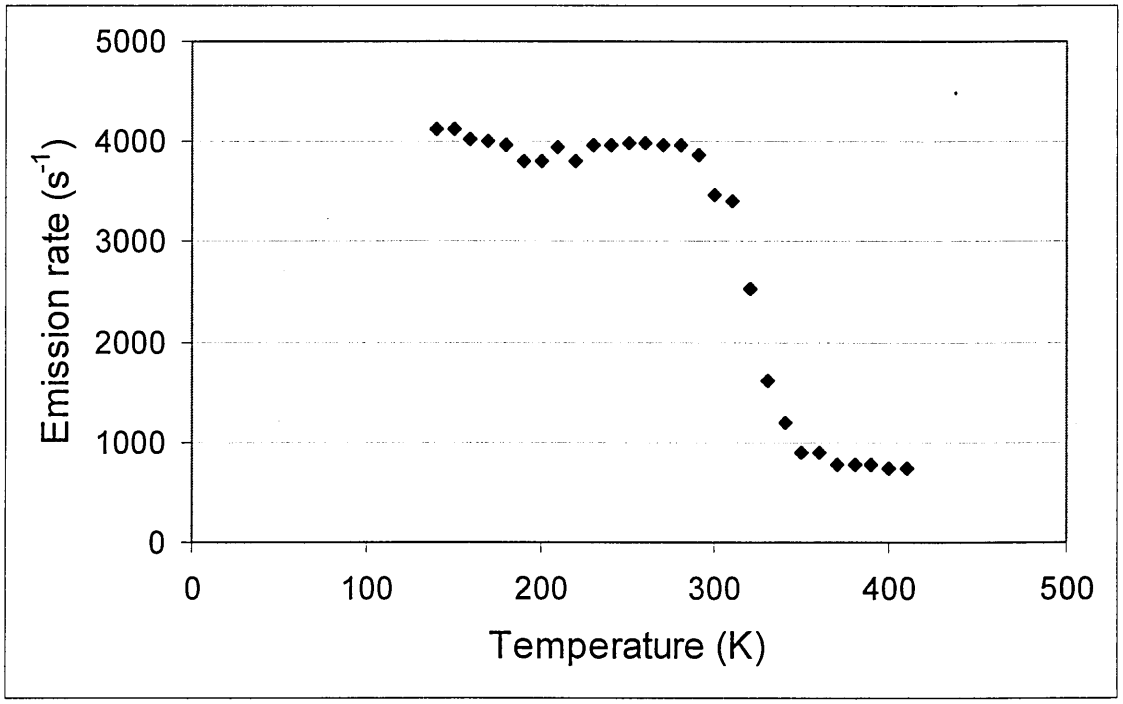

Fig. 8.47: Peak emission as a function of temperature for the high emission rate of JEF4

From Fig. 8.47 three distinct regions are obvious. From 100-280K the peak emission of this high emission rate is almost constant and then follows a linear decrease until the temperature reaches about 350K. Above this temperature only a small decrease in emission is detected. Although this could signify that three separate levels could be present, Fig. 8.47 clearly shows that no activation energy can be extracted and that these levels are neither due to point defects nor possibly to extended defects as the emission behaviour with temperature is very peculiar. A possible explanation for this phenomenon could be that these levels are due to grain boundaries in the diamond where B is trapped at non-substitutional sites. The nature of polycrystalline diamond makes the identification of defects at grain boundaries very difficult as their concentration is high and normal point defect capture and emission characteristics are not be applicable. It can also be suggested that the very broad DLTS defect spectrum that covered a wide temperature range of more than 300K, must entail the presence of multiple defects. As the temperature increases the emission of some defects reduces but new levels gradually appear thus making impossible not only the identification of defects and their nature but even a precise estimate of their number. Therefore in the case of diode JEF4 due to the broad defect spectrum, LDLTS can not yield more information other than the fact that a multitude of closely spaced defects exist, which are possibly not point defects but possess more complicated capture or emission characteristics.

Fig. 8.48 shows the LDLTS spectra obtained for JEF1 with the same biasing conditions as DLTS of reverse bias -2V and fill pulse 1V at selected temperatures.

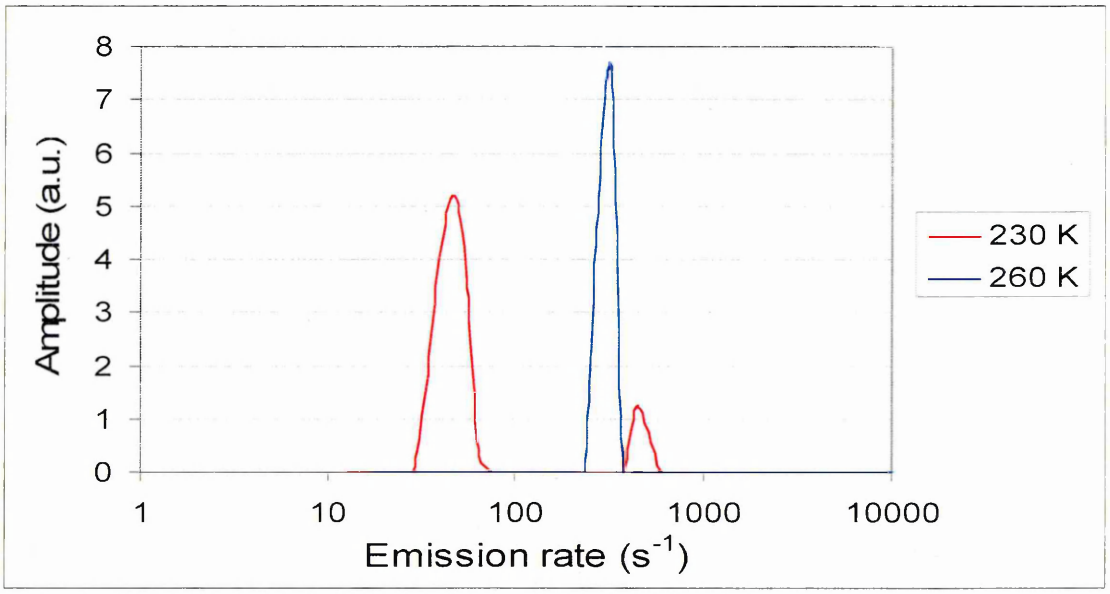

Fig. 8.48: LDLTS spectra of JEF1 at 230K and 260K

Although LDLTS was performed throughout the range 200-300K only the measurements at 230K and 260K are shown for clarity. In this case of diode JEF1, only two emission rates are present which facilitates the observation of their evolution with temperature. The high emission rate is present at all temperatures while the low emission rate is only appears from 200K to 240K. In addition both these emission rates consistently reduce in emission with decreasing temperature. Since the high emission rate gradually reduces in emission with reducing temperature, it could be confused with the low emission rate appearing at 240K at higher initial emission. This could have been the case with the previously examined JEF4, where many levels were present yielding a very complicated LDLTS spectrum that could not be resolved. Consistent decrease in emission rate with lowered temperature is expected for point defects, therefore the levels resolved by LDLTS in JEF1 could be due to point defects. However, capture cross-section measurements should be able to provide a better understanding of the nature of these defects. Because of the reducing emission with temperature of these defects their activation energy could be determined from the LDLTS data and this is shown in Fig. 8.49.

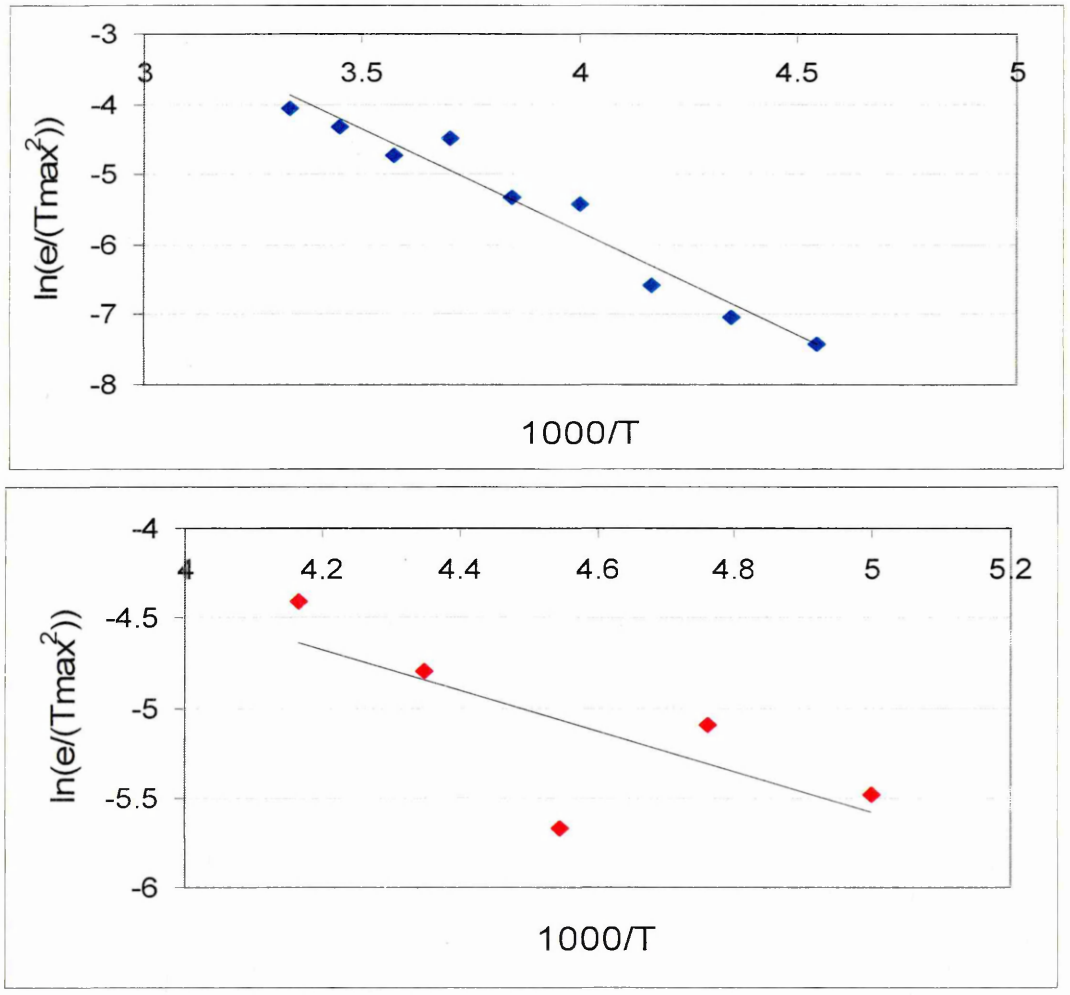

Fig. 8.49: Arrhenius plots of high (top) and low (bottom) emission components of JEF1

The activation energy found from the Arrhenius plot of the high emission rate was 0.21eV and that of the low emission crate was 0.1eV. DLTS indicated a level at 0.11eV which almost coincides with that of the low emission rate and may be related to hydrogen involved in the diamond deposition [9]. Moreover it appears that DLTS in this case detected more easily a trap that emits slowly. Since LDLTS of JEF1 yielded fewer defects than the nominally undoped JEF4 perhaps it can be suggested that higher B doping has an effect on lowering the number of defects in the depletion region.

In diode JEF2 there were two defects present in DLTS. The low temperature defect at 200K and a high temperature electron trap at 470K. The low temperature defect had a very low concentration in the DLTS spectrum and several biasing conditions had to be tried before it was clearly observed. Therefore LDLTS was not performed on this level. Its activation energy value of 0.37eV indicates that it may once again be the B acceptor level. The LDLTS spectra obtained for the high temperature electron trap of JEF2 are shown in Fig. 8.50 in 3-D view for some of the temperatures of the measured range 360-600K.

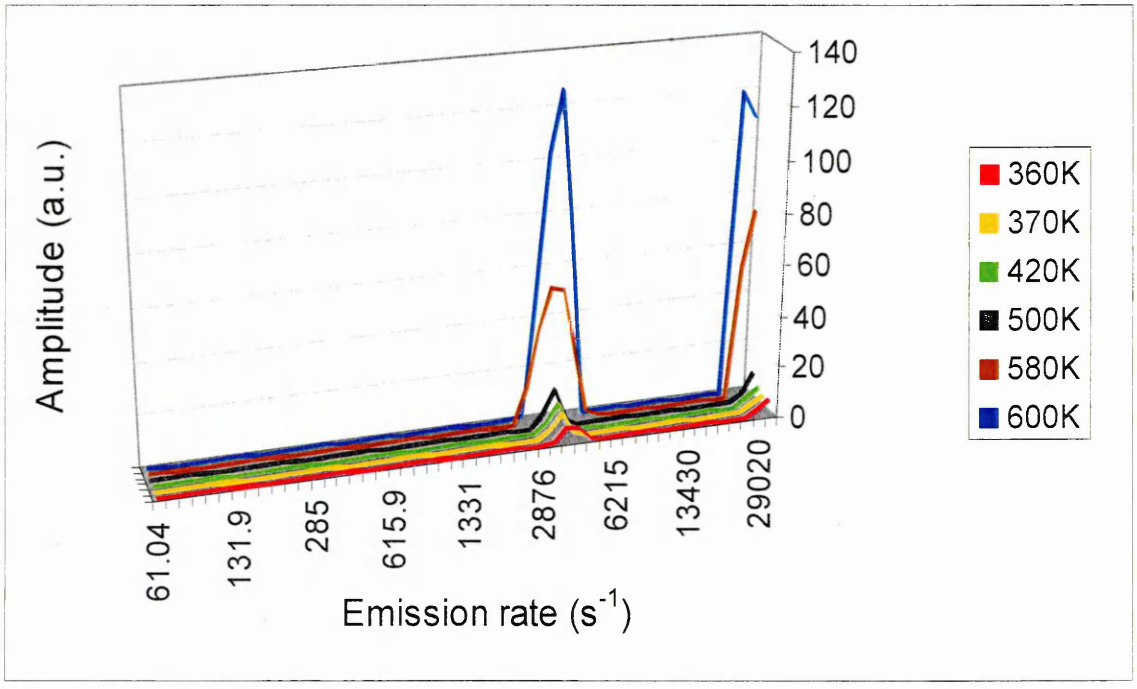

Fig. 8.50: LDLTS spectra obtained for diode JEF2

As can be seen from Fig.8.50 the LDLTS spectra of JEF2 appear to exhibit only one emission rate throughout the entire temperature range that the measurements were taken. For a defect with a large concentration such as the electron trap detected by DLTS for JEF2, a number of defects should have been resolved in LDLTS as the DLTS

covered a very wide temperature range. In addition the peak emission of these peaks is almost identical at most temperatures and hence it is not possible to calculate an activation energy. The amplitude of the peak increases with increasing temperature, though for the calculation of the activation energy it is important that the emission rate increases with increasing temperature. In addition, the peak emission is centred around the high value of $4300s^{-1}$. As the emission rate of the defect is unaffected by temperature it is concluded that the emission detected in DLTS is either an extended defect or due to grain boundaries in diamond, exhibiting very complex emission characteristics. The combination of several characterisation techniques would be necessary to investigate such a defect.

Finally the trap concentration was determined for the p-n diodes under investigation using the same equations as for the Schottky diodes earlier. These are shown in Table 8.4 for diodes JEF1, JEF2 and JEF4 as JEF3 did not produce any traps on the DLTS spectrum.

p-n diodes	Trap Concentration of Low Temp. peak (cm^{-3})	Trap Concentration of High Temp. peak (cm^{-3})
JEF1	$3 * 10^{14}$	-
JEF2	$8.3 * 10^{13}$	$9.7 * 10^{13}$
JEF4	$3.1 * 10^{14}$	-

Table 8.4: Trap concentrations for p-diamond / n-Si diodes

From the trap densities of the p-n diodes it can be observed that the most highly doped JEF2, out of the diodes that exhibited traps in DLTS, has the lowest trap density. This diode has the highest B doping and the highest carrier concentration after CV investigation, although it had the lowest B ionisation percentage. A comparison between the Schottky and p-n diodes will be provided later on in this chapter.

Capture cross-section measurements were performed on p-n diode JEF1. This diode was chosen as it exhibited the lowest concentration of defects that were more easily resolved when examined by DLTS and LDLTS. Therefore the capture cross-section result is expected to be less complicated and easier to analyse, while at the same time providing useful information about the nature of the defects involved and their capture

kinetics. Fig. 8.51 presents the capture cross-section data of the peak capacitance acquired form DLTS measurements with reducing fill pulse length from 5ms to 5μs and under the same biasing conditions as the original DLTS presented earlier. The logarithm of the capacitance components is plotted against time and for clarity the scale of the latter has been set to logarithmic.

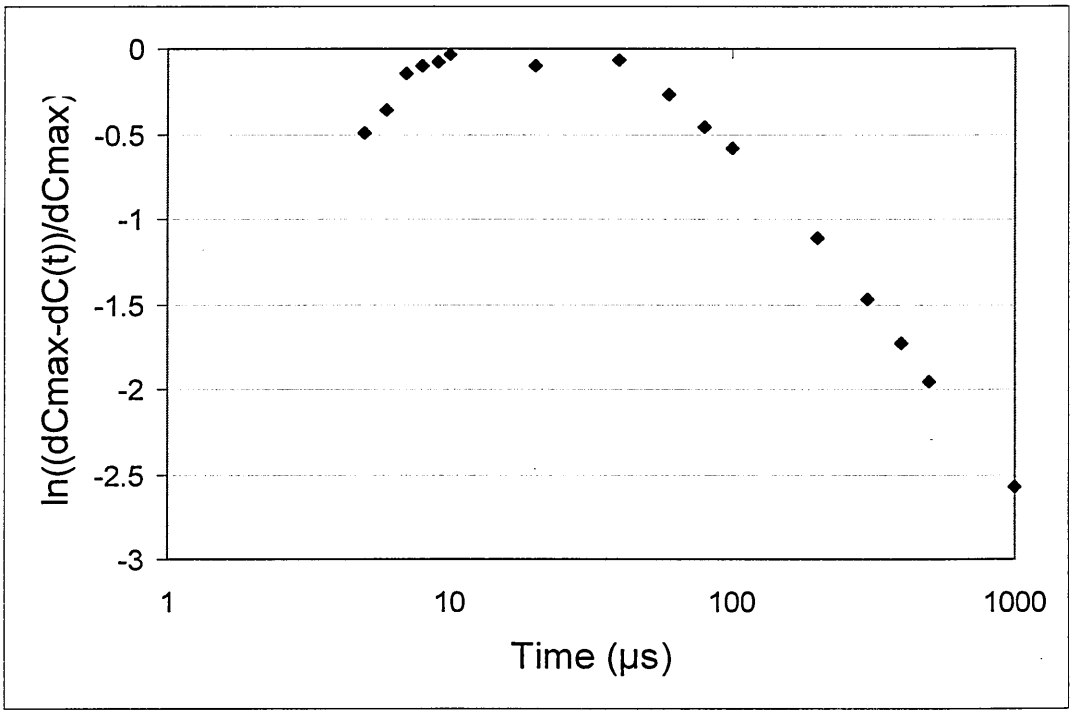

Fig. 8.51: Capture cross-section results of JEF1 with reducing fill pulse length from 5ms to 5μs

From Fig. 8.51 it can be seen that the logarithm of the capacitance values does not exhibit linear dependence with fill pulse length which suggests that the observed traps are not due to point defects. However, the capacitance points in Fig. 8.51 also suggest that there may be two capture cross-sections detected since two distinct regions can be observed. LDLTS results have already demonstrated the presence of two defects, whose combination of capture cross sections may be the result of the data obtained in Fig. 8.51. The logarithm of the capacitance points down to a fill pulse of 40μs, follow a slightly more linear decrease, but as the fill pulse is further reduced the combination of capacitances starts to reduce. To explain these results it is necessary to analyse the logarithmic part of the plot on the y-axis.

The combination of capacitances should remain below unity as *Cmax* is the maximum of the DLTS peak for the highest fill pulse length. The observed increase in the capacitance terms with reduced fill pulse length signifies that the term *dC(t)* becomes smaller which means that the peak of the DLTS spectrum for reduced fill pulse reduces.

This conclusion is expected for point defect behaviour. However, when the fill pulse reaches 40μs, the decrease of the combination of capacitances signifies that the peak of the DLTS spectrum starts to increase even if the fill pulse length gradually reduces. These conclusions indicate either that there may be two separate defects, one of which has a more point defect-like capture behaviour while the other is an extended defect, or that the entire capture process is governed by one extended defect. In this latter case of the extended defect, the Coulomb potential that has developed after the initial capture may be of opposing strength to the electric field existing in the depletion region during bias application and is hence momentarily reduced enough by the long fill pulses, to result in point defect-like capture or emission. When however the length of the applied fill pulse is very short, there is not enough time to reduce the Coulomb potential around the extended defect sufficiently for carrier capture, thus the behaviour of emission deviates from that of a point defect. In fact emission is seen to increase as the DLTS peak maximum *dC(t)* increases which is not typical behaviour even for extended defects. Therefore the case of emission from grain boundaries has to be considered as the capture process is even more complicated. The LDLTS results, shown in Fig. 8.48, support the suggestion of two separate defects whose capture cross section combination may be the result of the data obtained in Fig. 8.51.

8.4 Discussion and comparison

As mentioned earlier the objective of measuring both Schottky and p-n diode diamond films, was to investigate the depth profile of defects in the diamond film. Therefore it is constructive to compare the results obtained for both sets of diodes. The main difference between these diodes was the B ionisation percentage which was higher for the Schottky than the p-n diodes by at least three orders of magnitude even though some of the p-n diodes had higher B doping than the Schottky diodes. As the Schottky diodes assisted profiling of the volume near the surface of the diamond film, the obtained results may suggest that B ionises more easily near the surface than at a great depth where the depletion region at the interface with Si was situated. Since these samples were grown with Hot-filament chemical vapour deposition (*HFCVD*), the difference in B ionisation suggests that there are certain factors that deter B ionisation more at the beginning of deposition rather than at the end. This can be attributed to the nature of the polycrystalline diamond since at the beginning of deposition the density of grain boundaries is higher than near the surface. This means that more B is trapped at

grain boundaries and hence is inactive at the beginning of growth which is represented by the volume near the diamond/Si interface.

The measurements presented in this chapter showed that there is a larger number of defects at the depletion region with Si than near the surface of the diamond and in some of these diodes the B acceptor level was detected while it was not observed near the surface. Also higher carrier concentration and consequently capacitance was detected in the Schottky diodes than in the p-n diodes, including the p-n diode JEF3 which had the highest B doping than all the other diodes. Another outcome was the higher forward and reverse current observed in Schottky diodes that caused the IV characteristic to be more linear than diode-like. Capture cross-section measurements indicated that the defects observed in Schottky diodes had a more clear exponential dependence with time as far as their emission was concerned. These could be attributed to the presence of extended defects entirely. However in the p-n diodes both discrete levels, such as the B acceptor level and extended defects were recorded and even the capture cross-section measurements could not accurately identify them, as even higher resolution is required. In support of this argument LDLTS could not offer any further information about the activation energy of the defects that were resolved in the Schottky diodes, apart from the fact that emission was probably due to extended defects. However, it was a powerful tool in the investigation of the p-n diodes, by resolving the closely spaced defects and providing information about the activation energy of these and the potential nature of their kinetics, through investigation of their emission rates with temperature.

8.5 Conclusion

This chapter presented the results obtained by IV, CV, DLTS, LDLTS and capture cross-section measurements on p-diamond/p-Si Schottky diodes and p-diamond/n-Si p-n diodes. Investigation and analysis of these results offered information not only about their individual structures and the defects that are present but also an in-depth profiling of the diamond films. Fewer defects were observed near the surface of the diamond film although they were determined to be mostly extended defects. At the interface with the Si a larger number of defects are present however some of them are most likely to be point defects. Finally it was observed that B ionises in diamond more readily near the surface than at a great depth due to the lower density of grain boundaries near the surface.

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Chapter 9: Conclusions and future work

9.1 Conclusions from Ultra-shallow junction diodes

The electrical characterisation performed on the p^+n and n^+p ultra-shallow junction diodes was of great importance as it allowed investigation of structures that are currently necessary in CMOS technology. In particular, it was shown through basic CV and IV measurements that in such highly doped diodes, where even the lower doped side of the shallow junction has a high doping concentration, two depletion regions are formed which give rise to two capacitances. Due to the fact that these capacitances are in series it was possible to apply different biasing conditions that normally would not be allowed for diode investigation. Consequently it was shown that different depths, near the shallow junction or closer to the substrate were profiled for defects, despite the complicated CV and IV measurements. Finally, it was demonstrated, that characterisation techniques such as DLTS and LDLTS can be a very useful tool for the detection of defects even in such complex structures.

As the examined diodes contained multiple implants, it is possible to compare the effects of different dopant species relative to the production of defects that were observed. It was shown that as the dose increased the number of observed defects also increased. In particular, minority carrier traps were detected for all p^+n diodes at activation energies similar to those of interstitial complexes of either carbon or boron. LDLTS confirmed that these levels are not point defects but most likely complexes of defects or extended defects. According to literature, time dependent capture kinetics for some of these interstitial complexes have been observed and the LDLTS analysis performed in this work verified this result. The highly P-doped p^+n diode revealed a divacancy related defect even under the normal polarity configuration which was confirmed by LDLTS, while the highly As-doped p^+n diode revealed no such point defect with normal polarity. However, both these diodes exhibited divacancy-related defects with opposite polarity when the end-of range of P and As regions respectively, were profiled. The general conclusion that can be extracted from these p^+n diodes however is that, the defects observed in these complicated structures were mostly due to interstitial complexes rather than vacancy-related. This appears to be a reasonable

result as some transient-enhanced diffusion was observed, apparent even in some of the SIMS profiles. In addition the depth sampled by these electrical measurements was mostly within the interstitial-rich region of the doping well or even in the substrate.

The n^+p ultra-shallow junction diodes exhibited a dose dependence of defect production. For a doubling of the implantation dose, more traps were detected which were closely spaced in emission indicating clusters or complexes of defects. Furthermore in these diodes the normal polarity configuration yielded a multitude of hole traps while the opposite polarity revealed electron traps. Finally, there was indication that the n^+p diodes contained more carbon-related defects rather than vacancies, while few defects were detected due to the dopant species.

9.2 Conclusions from diamond on Si diodes

Two types of diodes were examined based on diamond thin films. The Schottky diodes were formed by p-type diamond grown on p-type Si. The p-type diamond grown on n-type Si substrate formed p-n diodes. This intentional arrangement offered the opportunity to examine diamond films grown by the same HFCVD technique within a volume that encompassed the end and beginning of growth of the films. It is well known that CVD polycrystalline diamond films contain grain boundaries. However, successful characterisation of these diodes was achieved by careful contact deposition and choice of biasing conditions.

The Schottky p-diamond/p-Si diodes revealed a relatively shallow hole trap and a broad spectrum belonging to a deeper hole trap within the diamond even at the highly doped diode containing $5.8*10^{20}cm^{-3}$ of B. The location of these levels was ~0.22eV and ~1.06eV above the valence band although extensive LDLTS analysis showed that these are not point defects. Given the presence of grain boundaries and the high doping of these films the presence of extended defects or emission of carriers trapped at grain boundaries are suitable explanation for the observed levels. Capture cross-section measurements are in support of this conclusion since time-dependent capture and emission was observed. Finally it was noticed that the actual carrier concentration was lower than the B doping which is in agreement with literature and clearly suggests low B ionisation in diamond, probably due to segregation at grain boundaries.

The presence of more defects was observed near the interface with Si in the p-diamond/n-Si diodes. Hence more defects are present at the beginning of the deposition of diamond. However, some of these levels were due to point defects as revealed by LDLTS measurements and the presence of some extended defects was also verified. The presence of hydrogen-related levels was suggested from defects located very close to the valence band in addition to activation energies arising from the B acceptor level. Nonetheless the polycrystalline nature of the films once again revealed complex emission characteristics which were confirmed both by LDLTS and capture-cross section measurements. Finally lower B ionisation was observed in these diodes compared to the Schottky diodes, indicating that B may be less trapped at large defects as growth proceeds.

9.3 Future Work

Due to the multitude of implants in the Ultra-shallow junctions a number of defects were present and their characterisation with DLTS or even with the high resolution LDLTS was difficult. Therefore further work on such technologically important structures could involve lower dose implants or implants of slowly increasing doses. This would facilitate the formation and evolution of defects. Additionally the characterisation of such structures would benefit from a parallel study with different techniques such as Transmission Electron Microscopy which would be able to detect extended defects at the implantation damaged end-of range regions. However, such work should ensure the concentration of these defects is sufficient for detection. Alternatively USJ research could be performed in diodes before and after annealing in order to provide comparison between the TED driven interstitial evolution of complexes and preliminary defects.

For the diamond diodes on Si substrates the major disadvantage was the polycrystalline nature of the synthetic diamond which meant a large concentration of grain boundaries. These in turn trapped acceptor atoms, mainly B, rendering them inactive and hence resulting in a low carrier concentration despite the high doping levels. Future work implementing the powerful techniques of DLTS and LDLTS could be very advantageous if performed on single-crystal diamond films where electrical characterisation would not be hindered by the presence of grain boundaries.