ORGANIC/INORGANIC HYBRID SOLAR CELLS BASED ON ELECTROPLATED CDTE

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Organic/Inorganic Hybrid Solar Cells Based on Electroplated CdTe

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Declaration

I hereby declare that the work described in this thesis is my own work, done by me and has not been submitted for any other degree anywhere.

Abstract

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The purpose of this work is to develop organic/inorganic hybrid solar cells based on electroplated CdTe. The materials used in this research are CdS, CdTe and PAni. These materials have been characterised by XRD, Raman spectroscopy, EDX, SEM, AFM, UV-Vis spectroscopy, PEC, C-V and DC measurements, UPS and PL for their structural, compositional, morphological, optical, electrical and defect properties. CdS has electrodeposited from the electrolyte using $(NH_4)_2S_2O_3$ as the sulphur source. The optimum growth voltage (V_g) and temperature (T_g) are obtained at 1455 mV and 85°C, respectively. The best annealing condition is found to be at 400°C for 20 minutes in the presence of $CdCl_2$+CdF_2. CdTe thin films were electrodeposited from $CdCl_2$ precursor and a comprehensive study was carried out for the first time. The work has demonstrated a better understanding of material issues and some clues on the effect of $CdCl_2$ treatment. The optimum V_g and annealing condition were obtained at 698 mV with respect to the calomel electrode and 420°C for 20 minutes in the presence of $CdCl_2$+CdF_2 or $CdCl_2$+CdF_2+$GaCl_3$. The development of PAni thin films has been established using anodic and cathodic deposition. The pernigraniline salt PAni grown from anodic has an amorphous structure, large bandgap and cementing growth effect while leucoemeraldine salt PAni grown from cathodic deposition shows the best crystallinity at V_g=1654 mV with respect to carbon anode, smaller grain size, higher resistivity and lower bandgap. The CdS, CdTe and PAni thin films have been studied in device structures, assessing their solar cell device performance. The best of CdS/CdTe solar cell was observed with efficiency of 5.8% when using CdS thin film treated with $CdCl_2$+CdF_2 at 400°C. The best solar cell from CdTe study shows the efficiency of 6.8% when using CdTe thin films treated with $CdCl_2$+CdF_2 at 420°C. Further study demonstrates that a device with g/FTO/n-CdS(~200 nm)/n-CdTe(~1200 nm)/p-CdTe(~300 nm)/Au shows high J_{sc} and highest efficiency (7.7%) due to the formation of n-n heterojunction, p-n homojuction and ohmic contact within the structure. The efficiency of the solar cell increased from ~2.4% to ~4.2% when incorporating ~81 nm thick PAni layer grown from anodic deposition. The devices incorporating ZnS, ZnTe and CdSe layers show the prospect of graded bandgap solar cell, but proper optimisation on each material should be carried out before using in multi-layer device structures. The study on the lifetime of solar cells show slow degradation and it maintained more than 83% of its initial efficiency after 9,000 hours.

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List of Publications

Journal publications

1. **N. A. Abdul-Manaf**, O.K. Echendu, F. Fauzi L. Bowen and I. M. Dharmadasa, Development of Polyaniline Using Electrochemical Technique for Plugging Pinholes in Cadmium Sulfide/Cadmium Telluride Solar Cells. *Journal of Electronic Materials*, 43:11 (2014) 4003–4010.

2. **N. A. Abdul-Manaf**, R. Weerasinghe, O.K. Echendu and I. M. Dharmadasa, Electro-plating and characterisation of Cadmium Sulphide thin films using Ammonium Thiosulphate as the sulphur source, *Journal of Materials Science: Materials in Electronics*, 26: 4 (2015) 2418-2429.

3. **N. A. Abdul-Manaf**, H. I. Salim, M. L. Madugu, O. I. Olusola and I. M. Dharmadasa, Electro-plating and characterisation of CdTe thin films using $CdCl_2$ as the cadmium source, *Energies*, 8:10 (2015) 10883-10903.

4. I. M. Dharmadasa, O.K. Echendu, F. Fauzi, **N. A. Abdul-Manaf** and H.I. Salim, Effects of $CdCl_2$ treatment on deep levels in CdTe and their implications on thin film solar cells; A comprehensive photoluminescence study, *Journal of Materials Science: Materials in Electronic*, 26 (2015) 4571-4583.

5. O. I. Olusola, M. L. Madugu, **N. A. Abdul-Manaf** and I. M. Dharmadasa, Growth and characterisation of n- and p- type ZnTe thin films for applications in electronic devices, *Current Applied Physics*, 16 (2016) 120-130.

6. I. M. Dharmadasa, O.K. Echendu, **N. A. Abdul-Manaf**, H. I. Salim, M. L. Madugu, O. I. Olusola and A. Ojo, Improvement of composition of CdTe thin films during heat treatment in the presence of CdCl2, (submitted to *Solar Energy Materials & Solar Cells* in September 2015, status: under review).

7. I. M. Dharmadasa, O. K. Echendu, F. Fauzi, H. I. Salim and **N. A. Abdul-Manaf**, Study of Fermi level movement during $CdCl_2$ treatment of CdTe thin films using ultra-violet photoemission spectroscopy, (submitted to Journal of Materials Science: Materials in Electronics in September 2015, status: under review).

Conference proceedings

1. I. M. Dharmadasa, D. G. Diso, O. K. Echendu, H. I. Salim, **N. A. Abdul-Manaf**, M. B. Dergacheva, K. A. Mit and K. A. Urazov, Thin film photovoltaic solar cells with nano- and micro-rod type II-VI semiconducting materials grown by electroplating, *Proceedings of the 9th Photovoltaic Science, Applications and Technology Conference C95,* Swansea, United Kingdom, 10-12 April 2013, pp 79-82.
2. **N. A. Abdul-Manaf**, O. K. Echendu, H. I. Salim, L. Bowen and I. M. Dharmadasa, Electrodeposition and characterization of polyaniline for development of organic/inorganic hybrid solar cells, *Solar Asia 2013*, CIUM, University of Malaya, Kuala Lumpur, Malaysia, 22-24 August 2013, pp. 105-110.
3. F. Fauzi, **N. A. Abdul-Manaf**, O. K. Echendu and I. M. Dharmadasa, Electrochemical deposition of organic and inorganic pin-hole plugging layers for CdS/CdTe solar cells, *Solar Asia 2013*, CIUM, University of Malaya, Kuala Lumpur, Malaysia, 22-24 August 2013, pp. 47-54.
4. I. M. Dharmadasa, O. K. Echendu, **N. A. Abdul Manaf**, M. B. Dergacheva, K. A. Mit and K. A. Urazov, Next generation solar cells using graded bandgap structures utilising nano- and micro- rod type semiconductors, *Solar Asia 2013*, CIUM, University of Malaya, Kuala Lumpur, Malaysia, 22-24 August 2013, pp. 17-22.
5. **N. A. Abdul-Manaf, O. K.** Echendu, F. Fauzi, L. Bowen and I. M. Dharmadasa, Electrodeposition and characterization of polyaniline to develop organic/inorganic hybrid solar cells based on cadmium telluride, *Proceedings of the 28th European Photovoltaic Solar Energy Conference and Exhibition,* Paris, France, 1-3 October 2013 pp. 2327 - 2332.
6. **N. A. Abdul-Manaf**, H. I. Salim, M. L. Madugu and I. M. Dharmadasa, Electrodeposition of CdTe thin films using chloride precursor for the application in solar cells, *Photovoltaic Science Application and Technology Proceeding*, PVSAT 11, University of Leeds, Leeds, 15-17 April 2015, pp. 137-140.
7. **N. A. Abdul-Manaf** and I. M. Dharmadasa, Fabrication of CdS, CdTe, and PAni Thin Films For Solar Cell Application Based on Electrodeposition Technique, *UK Semiconductors & UK Nitrides Consortium Summer Meeting,* 1-2 July, 2015, Sheffield, United Kingdom, pp. 132.

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Chapter 1 - Introduction

1.1 Current issue on energy

Global demand for energy has risen inevitably in the last few decades, in line with industrial development and population growth. The various usages of energy became more important due to the technological inventions created by scientists. According to the International Energy Agency, (IEA) technological development in electronic utensils and appliances has increased the demand for residential energy over the past 10 years [1]. As the world today moves towards high-technology lifestyles and industrialisation, more energy resources are needed to cover people's needs.

Today, world energy consumption is highly dependent on fossil fuel-based sources, such as petroleum, natural gas and coal. They provide 84% of the primary energy used worldwide [2]. In spite of this, these sources have presented several drawbacks to the environment, human health and society in general. Petroleum is a carbon-based fuel and the combustion of petroleum produces carbon dioxide, which contributes to the greenhouse effect [3]. Coal provides around 28% of our energy. However, burning coal produces sulphur dioxide, an acidic gas that contributes to the formation of acid rain [2,4]. Although natural gas is cleaner than petroleum and coal, the huge quantity of methane is much more dangerous, since it can cause an enormous explosion due to any leakage of the gas. Fossil fuels are not renewable, since they cannot be replenished when they are used. It is estimated that the resources of petroleum and natural gas will run out within 50 and 30 years, respectively, while coal can endure for the next 90 years [2].

Therefore, it is vital for us to find an alternative renewable energy to ensure long-term security of energy supplies. Renewable energy is a natural form of energy that is much cleaner and sustainable, and has a low impact on the environment. Possible alternative renewable kinds of energy include hydropower, wind, biofuel, geothermal, wave and solar [5]. A brief discussion on this area follows in section 1.2.

1.2 Renewable energy

The demand on renewable energy sources has become more crucial these days, due to environmental and economical sustainable issues. Renewable energy comes from resources such as water, wind, biomass, geothermal heat, ocean and sunlight that are

constantly replenished. It will not deplete our natural resources, is clean and has a very low impact on the environment or greenhouse effect.

Hydropower is power gained from the energy of falling or flowing water. The kinetic energy produced from the gravitational force or movement of water converts into mechanical energy through the spinning of turbines. The generator uses a magnetic field to convert this mechanical energy into electrical energy. Hydro-electric power stations can produce a great deal of power at a very low cost. It is much more reliable than other renewable energies, since electricity can be generated constantly. In fact, the water can be stored in the reservoir and ready to cope with peaks in demand. In spite of this, building a large reservoir is very expensive and will flood a very large area upstream, which causes problems for the residents and animals living there. Water quality of downstream can also be affected, which can have an impact on the health of the community and the environment [6].

Wind energy generated by the wind flows through a wind turbine that converts the kinetic energy into mechanical power [7]. This mechanical power can be used for specific tasks, such as grinding grain or pumping water. In the case of electricity, the generator is needed to convert the mechanical energy into electricity for various uses. Wind energy is a free, non-polluting and clean energy source. However, the cost of wind power technology requires a high initial investment for the machinery, site preparation and installation. In addition, some concern over the noise produced by the rotor blades and threat to the birds and bats turns out to be due to issues regarding this energy source. In fact, the major challenge of using wind as a source power is that it is intermittent. Although the generated electricity can be stored, not all winds can be harnessed to meet the timing of electricity demands.

Biofuel is an energy obtained from biomass materials through a process that converts carbon compounds into useful fuel. Biomass is a wide range of materials such as wood, agricultural residues, food and industrial waste. As there is a wide range of materials, the conversion technology of biomass into energy can be achieved by various methods, subject to the application. For example, the burning of biomass for direct usage, such as cooking, to produce heat and steam turbines has been extensively practised since ancient times. Moreover, the biomass is converted into liquid or gas, known as biodiesel, and this has been used widely for transportation [8]. In many ways, biodiesel works better than diesel, due to less polluting and the high quality of lubricating, which is good for engines. However, it has lower energy output than traditional fuels, and therefore requires greater quantities to be consumed, in order to

produce the same energy level. In fact, the requirement of large cropland to grow fuel crops could have an impact on the cost of food and could possibly lead to food shortages.

Geothermal is an energy obtained from the Earth, in particular from the hot rocks present inside the Earth. The energy is produced by the fission of radioactive materials in the Earth core and causes water deep inside the Earth to form steam. The steam becomes compressed at high pressure and comes out in the form of hot springs, which produces geothermal power [9]. Geothermal energy can be used directly, is non-polluting, does not generate by products, such as biofuels, and requires less maintenance cost. In fact, in ancient times, people used this source of energy for heating homes and other purposes. However, due to the small generation potential, there is no guarantee that the amount of energy produced will justify the capital expenditure and operation costs. Moreover, the safety issue regarding the poisonous gases and the eruption of volcano also becomes one of the disadvantages of this renewable energy source.

Wave energy is the energy generated from the interminable march of waves of the oceans. The kinetic energy formed by the continuous oscillating water is converted to the mechanical energy through the turbine rotation. Then, a generator converts this mechanical energy into useful electricity. Also, tidal energy is a hydropower that converts the energy of the tides into electricity. The tides are created by the gravitational effect of the sun and the moon on the earth due to the orbital characteristics of the Earth-Moon system and bring about cyclical movement of the seas. Both wave and tidal energies have unlimited supply. They can produce significant amount of energies with low running costs and no waste products. Nevertheless, these renewable energies are suitable only for certain locations. The wave energy has low performances in rough weather. Moreover, both of these energies also create hazards for some of the creatures near it. Large machines have to be placed nearby and in the water to gather energy from the waves and tides. These machines disturb the seafloor, change the habitat of near-shore populations and create noise that disturbs the sea life around them.

Solar energy is produced from the radiant energy emitted by the Sun. There are two types of solar energy; solar thermal and solar photovoltaic (PV). Solar thermal absorbs energy from sunlight to a heat receiver, which transforms energy from heat into solar thermal electricity for hot water heating and a variety of purposes. Solar PV panels convert the solar energy into electricity directly through photovoltaic conversion, using a PV cell [10]. Solar energy makes absolutely no noise at all, is clean, non-polluting and will last forever. It is reliable because electricity is actively created in just a few

millimetres thickness. Additionally, it requires only a low cost of maintenance, since there are no moving parts such as turbines in a solar panel, and this makes it impossible to really damage them. Although solar panel installation requires an expensive initial cost, once a solar panel is installed, solar energy can be produced free of charge. In the long term, there can be a high return on investment due to the amount of free energy a solar panel can produce. The fact that solar energy can only be harnessed in daytime and in sunny conditions has become a disadvantage of this energy. However, the use of batteries can be exploited to charge the solar power to be used at any time.

In general, each source of renewable energy has unique benefits and cost, but the positive and negative effects of these energies should be considered before developing them to create power. After all, replacing fossil fuels with renewable energy has been found to reduce premature mortality and overall damage, including public health and global warming emissions. Among all, solar energy is the most diversified form of renewable energy. It is a long-lasting source of energy, which can be used almost anywhere, even where there is no national grid such as at remote site areas or in space.

1.3 Solar energy

1.3.1 Solar radiation

The Sun produces about 386 billion billion Megawatts (386×10^{24} W) of energy by the nuclear fusion of hydrogen into helium in its core [11]. This energy is then radiated out from the core and moves across the solar system. The Earth then receives 174 petawatts (174×10^{15} W) of solar energy at the upper atmosphere [12]. Some of this energy has been bounced off to space and about 89 petawatts has passed through the atmosphere and reached the Earth's surface. Worldwide energy consumption, reported by IEA was about ~15 terawatts (15×10^{12} W) in 2012 [12]. This figure is only 1/5900 of the total energy received from the sun. Therefore, the main challenge facing us is to capture that energy. A lot of study and research should be done to harness the Sun, and transform its energy to meet our needs.

The Sun radiates light across a broad range of the electromagnetic spectrum from the ultraviolet, (UV) through the visible to the far infrared, (IR). Thus, the solar spectrum can be divided into three main regions as shown in Figure 1.1. UV in the wavelength range from 100 to 400 nm contains ~5% of irradiance, visible light with the wavelength range from 400 to 700 nm containing ~43% of the irradiance and IR with the wavelength range from 700 nm to ~1 mm, consisting of almost ~52% of irradiance.

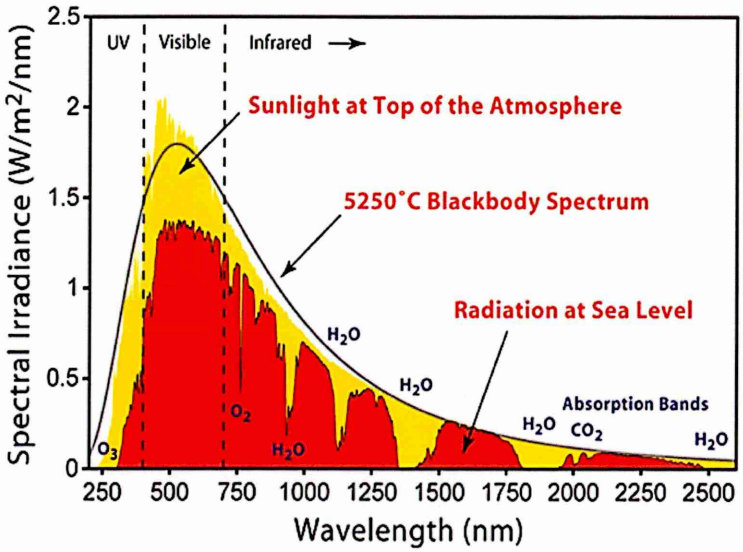

Figure 1.1: The shape of the solar spectrum at different condition.

The intensity and the spectral distribution of the radiation received on the Earth's surface are subject to the optical path length between the Earth and the Sun, the angle of incident radiation and the atmospheric conditions. The path length through the atmosphere is characterised by the term air-mass (AM). It is defined as the thickness of the air layer around the Earth through which sunlight passes. The spectrum, as detected from a satellite at outer space, is referred to as AM0, where there is no absorption of the radiation. The power density of AM0 is about 1360 Wm^{-2}. The solar spectrum that has travelled through the atmosphere with normal incidence above the point on the Earth is AM1. AM1 can be used for characterising solar cells in tropical region of the Earth. AM 1.5 is the air mass when the sun is at an angle of 48.2° above the horizon. It is used in a mid-lattitudes and adopted by the global solar energy industry as a standard for the solar cells characterisation. The power density of AM1.5 is 1000 Wm^{-2} [13]. The path length of sunlight through the atmosphere down to the Earth's surface is shown in Figure 1.2 [13].

$$AM = \frac{1}{\cos \Theta_z} = \sec \Theta_z \qquad 1.1)$$

where θ_z is the angle made between the Sun and the zenith.

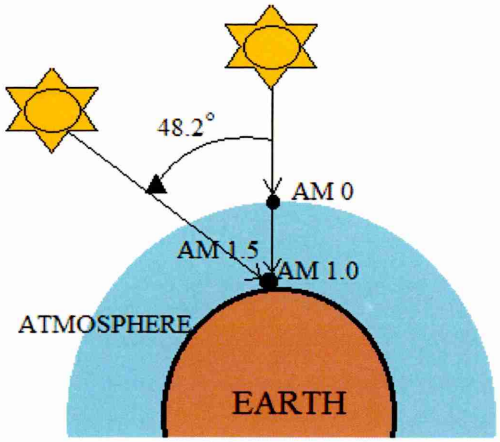

Figure 1.2: Path length of the Sun's illumination through the atmosphere.

Several conditions within the atmosphere can have an adverse effect on the intensity of solar radiation. The atmosphere contains 78% nitrogen, 21% oxygen, 0.9% argon, and 0.03% carbon dioxide with very small percentages of other elements. Our atmosphere also contains water vapour and traces of dust particles, pollen, plant grains and other solid particles. Apart from that, latitude, terrain, season, weather and clouds can also affect the amount of radiation that reaches the surface at any given location.

As mentioned in the previous section, there are two techniques to harvest solar radiance. These are solar thermal and solar PV. Solar thermal technology absorbs solar radiance from the Sun, using appropriate equipment, and converts into heat or electrical energy through solar thermal conversion, while solar PV converts light energy (photons) into electricity through the PV cell. In this conversion, specific materials, typically semiconductor materials are used to absorb the photons and release electrons. The free electrons are collected through the external circuit and then produce electricity. Further explanations on PV conversion are given in section 1.3.2.

1.3.2 Photovoltaic technology

PV technology is a method of generating electricity by converting solar radiation into direct current electricity through a semiconductor device, known as a solar cell, that exhibits the PV effect.

PV conversion requires three principal processes starting from the absorption of photons, which creates electron-hole pairs, separation of these photo-generated charge carriers pair of opposite types (free electron and free hole), and, finally, extraction of these separated carriers to an external circuit [14,15].

The energy supply for a solar cell is from photons, which comes from the Sun. These photons contain various amounts of energy corresponding to the different wavelengths of the solar spectrum. When photons strike the solar cell, some of them will be reflected, some will be absorbed, while others are transmitted. The absorbed photons generate electricity by transferring their energy to electrons in the bonded state (in the valence band). With its newfound energy, the electron leaves a hole behind and excites to a higher energy state corresponding to the energy of the incident photon. A variety of materials and processes can potentially satisfy the requirements for photovoltaic energy conversion, but in practice, nearly all photovoltaic energy conversion systems use semiconductor materials in the form of a p-n junction. Further explaination on p-n junction is discussed in Section 2.2.2. This p-n junction creates an internal electric field in solar cell devices and thus drives the holes to the p- side and electrons to the n- side. The electrons then dissipate their energy in the external circuit and return to the solar cell. The PV conversion in solar cell devices and the band diagram of the p-n junction can be seen in Figure 1.3.

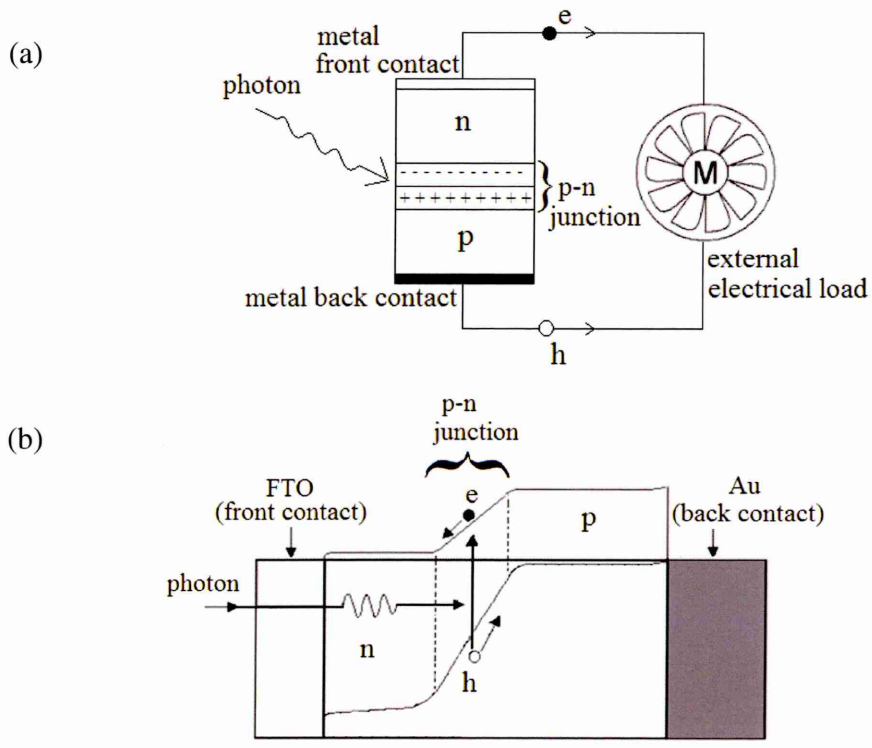

Figure 1.3: Schematic of (a) PV conversion in p-n junction solar cell and (b) Energy band diagram of a p-n junction solar cell.

1.3.3 Brief history of solar cells

A solar cell is an electronic device that converts the energy of light to electrical energy through the photovoltaic effect. Solar to electricity conversion was first invented by a French physicist, Edmond Becquerel in 1839. Becquerel was observing the photovoltaic effect while experimenting with a solid electrode in an electrolyte solution, when he saw voltage being generated when light fell upon the electrode. Several inventions were made afterwards, contributing to the evolution of solar energy use. In 1891, the first solar heater was created, and in 1893, the first solar cell was introduced. Solar power equipment started becoming popular and commercialised in the 1950s [16]. Now, it has been used to power space exploration equipment and the research and developments are in progress to establish solar power in transportation systems. At each phase of development, advanced large-scale solar energy plants are produced. In June 2015, the largest photovoltaic power plant was completed in Antelope Valley, Carlifonia and currently it is operating with 579 Megawatts [17].

Solar cells can be categorised into three generations, based on the order of their prominence. The first generation contains solar cells that are relatively expensive to produce. They are based on silicon (Si) or germanium (Ge) that are doped with phosphorus, P and boron, B to form p-n junctions. This generation is dominating the commercial solar cell market. Silicon cells have high efficiency, but particularly only pure silicon is needed, and due to the required complex process, the price is still high compared to the power output. Second generation solar cells are usually called thin-film solar cells, because they are made from layers of semiconductor materials only a few micrometres thick. The most common light absorbing materials used in thin film solar cells are cadmium telluride, (CdTe), copper indium gallium diselenide, (CIGS) and amorphous silicon, (a-Si). The biggest advantage of this technology is that it has a lower price than crystalline silicon solar cells, since it uses less material and lower cost manufacturing processes. This is the generation that we focus on in the following section of this research work. The third generation solar cells are being made from a variety of new materials, including nanotubes, quantum dots, silicon wires, solar inks using conventional printing press technologies, organic dyes, and conductive plastics. However, these solar cells need cutting edge technology and, currently, they produce low efficiency along with serious lifetime issues.

1.3.4 A range of next generation solar cells

The ideas on next generation of solar cells have been proposed for the development of solar cell devices. The next generation of solar cells should be cheaper, more efficient

and much more environmentally friendlier than current versions. There could be future design improvements or a potential to exceed the Shockley-Queisser limit of power conversion for a single junction or multi-junction solar cells. Following sections highlight some of the next generation solar cells.

1.3.4.1 Hot carrier solar cells

The main purpose of the hot carrier solar cell is to tackle the carrier thermalisation loss after the absorption of high energy photons with energy greater than the bandgap. In conventional solar cells, the photo-generated electrons usually lose their energy by cooling down from their initial energetic position to the band edges through optical phonon emission [18]. Hot carrier solar cells attempt to minimise this loss by extracting the generated carriers at higher energies. This process involves slowing the rate of carrier cooling in the absorber from picoseconds (ps) to nanoseconds (ns) and the extraction of energy selective carrier through energy selective contacts. In general, the three common approaches of hot carrier solar cells are such as by direct extraction of hot carriers through energy selective contacts, by application of an intermediate band assisted absorber and by using the multiple exciton generation. Hot carrier solar cells are an attractive alternative to the multilayer approach and offer simplicity of design with greater conversion efficiencies. The maximum achievable efficiency has been predicted to be 66%, but the practical realisation of actual hot carrier solar cells has never been successful [19]. The thermalisation in the absorber layer leading to insufficient collection of hot carrier at the electrical contact and the heat production in the environment could be harmful to the output of the solar cells [20, 21].

1.3.4.2 Plasmonic solar cells

The plasmonic solar cell is among the third generation solar cells that convert light into electricity by improved light absorption using quantum of plasma oscillation known as plasmons. Plasmons are free-electron oscillations in a conductor that allow light to be manipulated at the nanoscale. The ability of plasmons is to guide and confine the light on sub-wavelength scales [22]. The designs for plasmonic solar cells vary depending on the method being used to trap and scatter light across the surface and through the material. The nanopartical cell is one of the common designs by deposit metal nanoparticles on the upper surface of the thin film semiconductor as shown in Figure 1.4 [23]. The basic principles for the functioning of plasmonic solar cells are such as scattering and absorption of light due to the deposition of metal nanoparticles. When

light hits these metal nanoparticles at their surface plasmon resonances, the light is scattered in many different directions. This allows light to travel along the semiconductor and bounce between the substrate and the nanoparticles, enabling the semiconductor to absorb more light. According to the proposers, the plasmonic solar cell is cheaper, more practical and the design offers a promising way to increase the efficiency of the solar cell. However, in addition to plasmonic effects, other effects such as doping effects of nanoparticles can have detrimental result for the solar cell. Practical devices with improved efficiencies are yet to come.

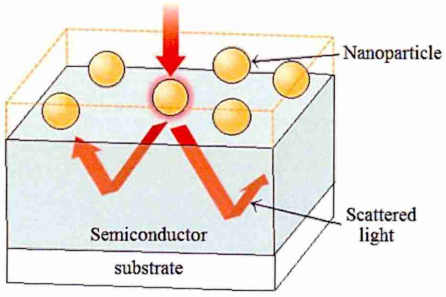

Figure 1.4: Example of a nanoparticle cell of the plasmonic solar cell.

1.3.4.3 Organic solar cells

An organic solar cell is a type of solar cell that uses an organic compound, commonly a polymer, to absorb light and produces electricity through the photovoltaic effect [24, 25]. The conversion process is made by the combination of several types of materials, all having distinct optical and electrical properties. Although the photovoltaic concepts of the organic solar cell are quite similar to inorganic solar cells, certain mechanisms somehow differ from inorganic solar cells. For instance, the separation of electrons and holes in organic solar cells is caused by the electric field at the organic-metal interface created by the differences in electron affinity and ionisation potential between these two materials and the electric field is not associated with any band-bending, unlike in the inorganic solar cells. Organic solar cells can be formed in a single layer, bilayer, bulk heterojunction and graded heterojunction. The single layer organic solar cell is the simplest form. This cell is made by sandwiching a layer of organic electronic material between the two metallic conductors. The organic solar cell has low production costs in high volumes since the modification in molecular engineering and device architecture can be done by changing the chain length and functional group of polymers, which consequently forming variation of HUMO-LUMO gaps [24]. The optical absorption coefficient of organic molecules is high, so a large amount of light can be absorbed with

a small amount of materials. In spite of this, the major drawbacks associated with organic photovoltaic cells are the lifetime issue, low stability, low efficiency and low strength compared to inorganic photovoltaic cells.

1.3.4.4 Quantum dot and nano solar cells

The quantum dot solar cell has secured its place as another promising next generation solar cells due to its operational feasibility, durability and ease of maintenance. This particular solar cell uses quantum dot as the absorbing material. As the bandgap in bulk material is fixed by the choice of the material, quantum dot can adjust its own bandgap by changing the size of the dots. This makes quantum dots attractive for multi-junction solar cells where a variety of materials are used to improve efficiency by harvesting multiple portions of the solar spectrum [26].

Another promising solar cell is the type with the attachment of semiconductor nanostructures such as nano-wires, nano-tubes and nano-rods in the device structure. In recent years it has been observed and experimentally verified that many nanostructures as such can improve solar cell efficiency by modifying the properties of previously used materials and can reduce cost due to their self-assemble property [27]. For instance, single-wall carbon nanotube polymer solar cells are able to produce cheaper, light and flexible devices for space power applications.

1.3.4.5 Up conversion and down conversion for solar cells

Up and down conversion is a strategy to improve the efficiency of the solar cell. In practice, a photon with a lower energy than the bandgap will be lost in a solar cell and a photon with very high energy will also lose the energy above the bandgap limit due to thermalisation [28]. So, this solar cell uses up conversion technology to convert two or more of the lower energy photons into a photon with energy above the band gap energy. Meanwhile, the down conversion technology converts the excessive high-energy photon into several lower energy photons but the energy is still above the bandgap of the absorber used [28, 29]. Therefore, all the photons now have sufficient energy to be absorbed by the photovoltaic cell. The optimised down-conversion and up-conversion theoretical efficiency limits are 40% and 48%, respectively [30].

Up and down conversion material is a thin film of material, which is fabricated separately from the solar cell device. The up conversion layer usually lies between the solar cell material and the back reflector while the down conversion layer lies on the

front of the solar cell material. This is illustrated in Figure 1.5. The research is in progress to enhance the up and down conversion layers in solar devices.

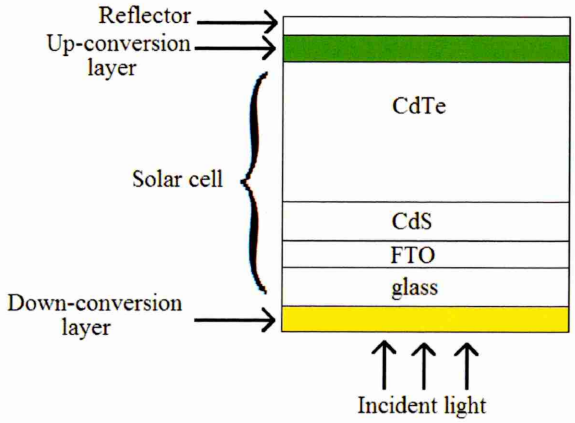

Figure 1.5: Schematic diagram of the device with up and down conversion layers.

1.3.4.6 Perovskite solar cell

Perovskite solar cells hold an advantage over other typical solar cells in the simplicity of their processing. This infact the extension of the dye sensitized solar cells (DSSCs). Perovskite solar cell is a type of cell containing a perovskite structure compound with the ABX_3 crystal structure of the absorber material [31]. Perovskite materials with an ABX_3 formula as illustrated in Figure 1.6 with A and B are the cations of different size and X is anion. Most of the perovskite solar cells are based on organic-inorganic halide perovskite where A, the larger cation is organic material, B, the smaller cation is inorganic material such as Pb or Sn and X, anion is a halogen such as F, Cl, Br or I [32].

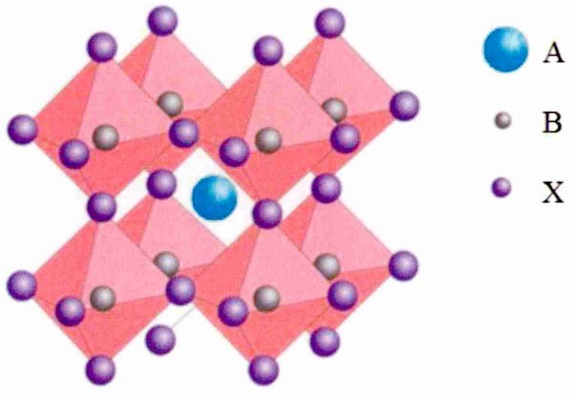

Figure 1.6: Typical Perovskite crystal structure of the form ABX_3.

Some key attributes of this type of solar cell include strong solar absorption, flexibility and low non-radiative carrier recombination rates. Perovskites are easily synthesised, and their distinctive crystalline structure makes them a perfect match for the

development of efficient solar cells. The efficiency limit of perovskite solar cells is about 31%, which approaches the Shockley-Queisser limit of gallium arsenide (33%). The past three years have seen the extraordinary rapid development of perovskite solar cells and brought them to the attention of the academic community, researchers and industry. The highest conversion efficiency in perovskite solar cell has been reported up to 20.1% by S. Seok from Korea Research Institute of Chemical technology (KRICT) [33]. The current issues are mainly on stability and lifetime of the devices. Once these issues are solved, these materials show high potential in the PV field.

1.4 CdS/CdTe thin film solar cell

Among the different photovoltaic device structures under development, the CdS/CdTe thin film solar cell has attracted considerable attention. The CdS/CdTe solar cell device was first reported in 1963 by Cusano [34]. It was a two-layers solar cell, where the p-type material was Cu_2Te and the n-type material was CdTe. Cusano reported that this solar cell was a p-n hetero-junction device with efficiency of 6.0%. Typically, CdS/CdTe solar cells have a superstrate structure where the light incident passes through the CdS layer. Therefore, it needs a transparent substrate such as glass. The glass substrate was deposited with a transparent conducting oxide (TCO) layer to serve as a front contact. Glass panels coated with fluorine-doped tin oxide (FTO) or indium-doped tin oxide (ITO) are commercially available. Both coatings provide transparency of the glass/TCO substrate above 85% in the spectral range of interest and low sheet resistance.

The use of CdS as a window layer is ideal, since it has a direct wide bandgap of 2.42 eV, which absorbs only the photons with energy greater than 2.42 eV and transmits almost all other photons to the absorber layer, CdTe. CdS is a binary compound of the group II-VI semiconductor family and generally has a cubic or hexagonal crystal structure with lattice constant of cubic ~5.82 Å and hexagonal (a=4.14 Å, c=6.71 Å) [35, 36]. CdS films are always n-type with a typical carrier concentration in a range of ~10^{16} cm^{-3} to 10^{18} cm^{-3} due to the presence of excess cadmium or sulphur vacancies [37]. It also has an electron affinity of 4.50 eV [38], which is similar to that of CdTe and enables the conduction bands of CdS and CdTe to join smoothly at the interface.

CdTe is one of the most attractive semiconductor materials, which is widely used in infrared optical windows and solar cell absorber materials. It commonly has a cubic crystal structure with lattice constant ~6.48 Å, as well as a direct bandgap of 1.45 eV for maximum photovoltaic conversion efficiency [36, 39]. CdTe has a high chemical

stability as well as a high optical absorption coefficient of more than 5×10^{-4} cm^{-1} [38]. The theoretical efficiency of CdTe p-n junction thin film solar cell is expected to be around 28 – 30% [40]. Only about ~2 μm thickness of CdTe is sufficient to absorb a major part of the solar radiation with energy greater than the energy bandgap.

A final step in the solar cell fabrication is the application of back electrical contact to the CdTe layer. One of the most important potential issues of instability in CdTe/CdS solar cells is related to the back contact degradation due to the use of copper as a dopant in Au/Cu contact. Therefore, in this research only, Au contact is used to prevent the degradation issue in solar cell devices.

The work on CdS/CdTe thin film solar cell started in the 1970s, but progress in research and development gained real impetus in the 1980s with the development of various techniques and efficiencies exceeding 10% for CdTe/CdS hetro-junction solar cells [41, 42, 43]. The work from different groups in the 1990s pushed the efficiency to ~15-16% [43]. The commercialisation of the CdTe photovoltaic technology began in the late 1990s and CdTe photovoltaic modules were available in the market with efficiency at about 10% and the output power ranging from 45-55 W at the size scale of 60x120 cm^2. Over a period of 20 years, the efficiency of CdS/CdTe was not increasing mainly due to the lack of understanding of the material issues and the physics behind the device. There are now two different structures, a simple p-n junction assessed from early 1980s and a combination of n-n heterojunction with a large Schottky barrier at the back contact [44, 45]. It is interesting to observe the efficiency increase from ~16% to 21.5% as reported by the First Solar company during the past few years (2011-2015). Although the reason for this rapid increase is not available to the PV community, this must be related to improve understanding of material issues and device architectures.

Fabrication methods for CdS/CdTe layers have a significant impact on solar cell efficiency and cost. Samples have been developed successfully by several common techniques, such as electrodeposition (ED) [46], close spaced sublimation (CSS) [47], chemical bath deposition (CBD) [48], radio frequency (RF) sputtering [49] and physical vapour deposition (PVD) [50]. The deposition methods should be carefully chosen with the consideration of cost of manufacturing, high quality thin-film structure for high efficiency, proper pollution control and commercial production prospects. Although RF sputtering is a fast method of deposition, the film has a poor quality that reduces the cell efficiency. CBD could provide a dense and smooth CdS layer but the chemical solution waste recycling and management have cause extra cost in manufacturing. Among these techniques, ED has demonstrated numerous advantages due to its simplicity, low-cost

and suitability for the production of macro-scale devices such as solar panels. The highest efficiency in CdTe photovoltaic devices prepared by the ED technique was ~18%, as reported in 2003 [45].

1.5 Current issues in CdS/CdTe solar cell fabrication

A typical CdS/CdTe solar cell consists of glass/FTO/CdS/CdTe/Au structure. During the fabrication process of thin film solar cell devices, pinholes are formed for various reasons. Pinholes are small areas with a missing layer of the semiconducting CdS or CdTe layers. These pinholes are entropy driven and are formed randomly. The pinholes can arise from incomplete coalescence of the CdTe grains during deposition, or due to defects in the underlying surface, and are a continuing concern in thin film polycrystalline devices. If these pinholes are left untreated, they will lead to short-circuit in photovoltaic devices after deposition of a metal contact. In order to prevent this, insulating layers can be introduced to fill these pinholes. PAni is a semi-insulating polymer, with tuneable bandgap, high chemical stability and has been widely used in various fields. A very thin layer of PAni film has been proposed to plug these pinholes in order to cover the leakage part, forming an MIS type structure, increasing the barrier's height and consequently improving the efficiency of solar cells.

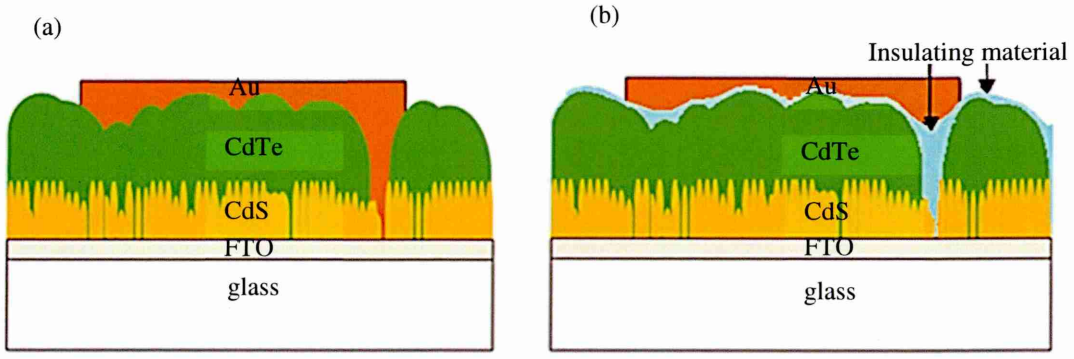

Figure 1.7: Schematic diagram of (a) conventional CdS/CdTe thin film solar cell and (b) proposed CdS/CdTe thin film solar cell with a pinhole plugging layer.

During fabrication of CdTe/CdS thin film solar cells, a $CdCl_2$ treatment is essential after the deposition of a CdTe layer. The use of $CdCl_2$ treatment has been practised extensively since the 1979 to improve the material properties, in particular enhancement of the grain size and, consequently, an increase in solar cell efficiency. However, the $CdCl_2$ solution should be prepared with very high concentration in order to see a clear outcome [51, 52]. Somehow, the highly saturated $CdCl_2$ does not only

promote the larger grain growth, but also generates larger voids or pinholes between the grains. The combination of other halogen elements is proposed to enhance the reaction of the $CdCl_2$ and treatment process. Halogen elements are those such as bromine, iodine and fluorine. Among these, fluorine has been chosen since it has small atomic radii, which make it easy to diffuse into the grain boundaries and perform better treatment. In fact, Echendu and Mazzamoto have reported the advantage of using $CdCl_2$ in the presence of fluorine in improvement of material properties and solar cell device performance [53, 54]. Apart from that, the Ga-doped in CdTe has been reported by Fernández as able to dissolve the Te precipitates and enhance the electrical property of CdTe. Therefore, in this research, a variety of chemical treatments on CdS and CdTe films has been proposed to effectively improve the efficiency of CdS/CdTe solar cells.

Another challenge is how to improve the entire device parameters, including short-circuit current density (J_{sc}), open circuit voltage (V_{oc}) and fill factor. The theoretical maximum of efficiency, J_{sc} and V_{oc} base on Shockley-Queisser limit are ~31%, ~30.5 $mA{\cdot}cm^{-2}$ and ~1200 mV [55, 56]. Several factors that hindered from reaching these theoretical maximum limits are including the defects, oxidation, losses, impurities, poor crystallinity, low carrier density and mobility. The strategies for improving the solar cell parameters can be done by using high purity chemical in order to reduce the impurity. The annealing process and chemical treatments are helpful to reduce the defects and improve the crystalinity of the materials. In fact, many parameters in all features, including material properties, device architectures and device fabrication should be optimised properly before fabricating the solar cell. For that reason, the proper optimisation of each layer including CdS and CdTe films will be characterised properly before using them in device fabrication. In addition, the fabrication process, in particular the etching process and variety of device structures, including the incorporation of a buffer layer and capping layer obtained from other researchers within the SHU solar energy group will be explored in this research work.

1.6 Research objectives

Based on the introduction and current issues discussed above, the research objectives of this programme are formulated as follows:

1. Optimise the growth parameter of CdS electrodeposition from an aqueous electrolyte containing $CdCl_2$ and ammonium thiosulphate ($(NH_4)_2S_2O_3$). Full characterisation of CdS thin films, using a wide range of analytical techniques, such as XRD, Raman spectroscopy, UV-Vis spectrometer, optical profilometer,

DC conductivity measurement, PEC cell characterisation, SEM, AFM and EDX. Fabrication of solar cell device by using CdS thin film as a window layer.

2. Preparation of CdTe thin films, electrodeposited from an aqueous solution containing $CdCl_2$ as the Cd source instead of typical $CdSO_4$. Optimise the growth parameter of CdTe electrodeposition through the variety of analytical techniques, such as XRD, Raman spectroscopy, UV-Vis spectrometer, optical profilometer, DC conductivity measurement, PEC cell characterisation, CV measurement, SEM and AFM. Fabrication of solar cells by using n- and p-CdTe thin films as absorber layer.
3. Establish the growth of PAni thin films, using electrodeposition technique. Full characterisation of PAni thin films, using a wide range of analytical techniques such as XRD, UV-Vis spectrometer, optical profilometer, DC conductivity measurement and SEM. Fabrication of solar cells by incorporating PAni as a pinhole plugging layer.
4. Development of low-cost solar cell devices, fabricated using the three materials characterised above. The general main structure of the device is glass/FTO/CdS/CdTe/back contact, and an attempt to use PAni for pinhole plugging layers will be made to study the effect of this layer on the device performances.
5. Development of solar cells with other device structures involving zinc sulphide (ZnS), cadmium selenide (CdSe) and zinc telluride (ZnTe) for buffer or capping layers to achieve highest possible efficiency.

1.7 Organisation of chapters

This thesis is organised into eight chapters, as illustrated in Figure 1.8. The introduction and the research background of this work are presented in the first two chapters. This is then followed by the explanation on experimental work including material growth and characterisation techniques as well as solar cell fabrication procedure and assesments. Chapters 4 to 6 are presented on electrodepositions and characterisations of the main three materials used in this work. These are such as CdS, CdTe and PAni thin films. The device assessments are presented at Chapter 7 and finally the conclusion and suggestion for future work are presented in chapter 8. The summary of each chapter is as follows:

Chapter 1 discusses the current issue on energy, a brief review on other renewable energy sources and further in-depth discussion on solar energy, including solar

radiation, photovoltaic technology, solar cells, brief history of solar cells and CdS/CdTe thin film solar cell. Research objectives have been proposed after a broad discussion on current issues in CdS/CdTe solar cell fabrication.

Chapter 2 reviews the literature of solar cells. The review on p-n junction, Schottky barrier, ohmic contact, thin film deposition, as well as material background including CdS, CdTe and PAni has been discussed intensively in this chapter.

The experimental methods of this research are discussed in Chapter 3. The research work has been divided into five main parts, which are sample preparation, electrodeposition of thin films, characterisation of thin films, development of solar cell devices and characterisation of solar cell devices.

The materials growth and characterisations The characterisation of CdS thin films under various conditions, such as growth parameters, annealing conditions, chemical treatments and sulphur concentrations in CdS precursor has been presented in Chapter 4.

Chapter 5 presents the growth and material characterisation of CdTe thin films. The effects of growth voltage, annealing conditions and chemical treatments have been studied systematically through various characterisation techniques.

The effort to establish PAni thin films from electrodeposition has been presented in Chapter 6. PAni thin films have been studied with various growth conditions, annealing temperatures and pH concentrations.

Chapter 7 presents the characterisation of solar cell devices, mainly from the CdS and CdTe thin films. The attempt to use PAni for pinhole plugging layers, buffer layers, capping layers, intermediate layers and graded bandgap solar cells has also been shown in this chapter. The effect of etching conditions in device fabrication and analysis on device lifetime is discussed in the final part of this chapter.

Final conclusion, future work and the thoughts on the next generation solar cells have been presented in Chapter 8. This discussion includes the challenges encountered in this work and suggestions for future work.

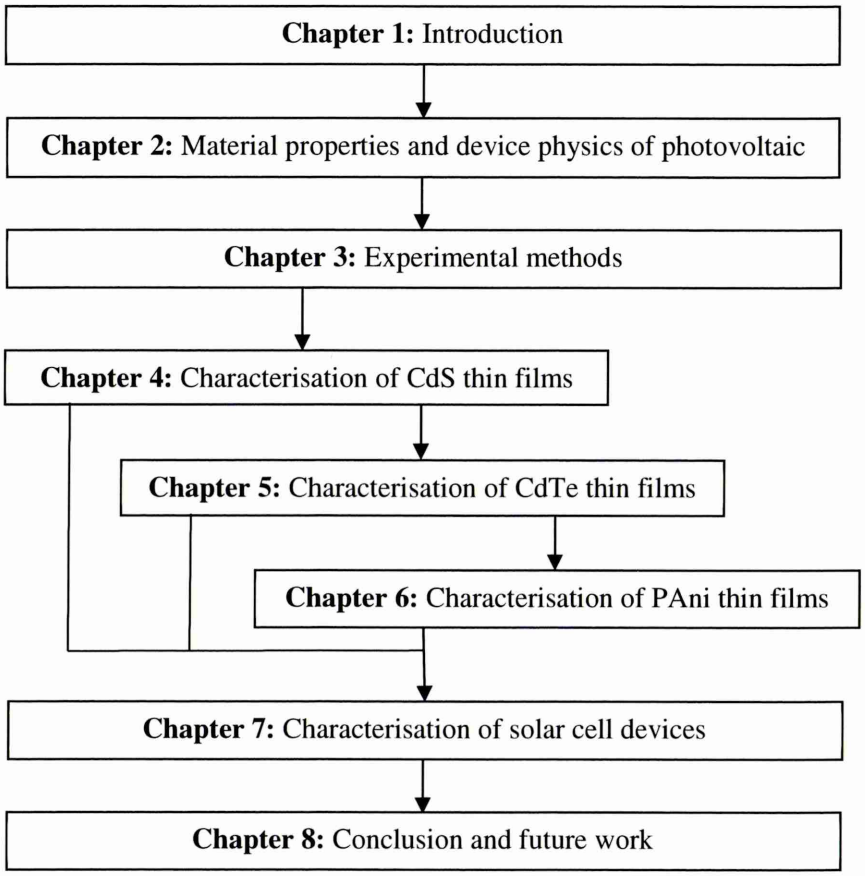

Figure 1.8: Outline of chapters.

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Chapter 2 - Material properties and device physics of photovoltaic

2.0 Introduction

This chapter presents the literature review on the science background of the research area including the solar energy materials used in this work, the physics of junctions and interfaces in solar devices as well as a view of various deposition techniques for solar cell fabrication.

2.1 Solar energy materials

Materials can be categorised into three main groups; which are metals, semiconductors and insulators corresponding to their electrical conductivities or energy bandgaps. Metal has the highest conductivity and the narrowest bandgap (≤0.3 eV). The electrons in metal only partially fill the valence band, therefore the electrons can move freely without gaining extra energy. A semiconductor has a filled valence band and empty conduction band with the bandgap between 0.3 eV to 4.5 eV. However, some of the electrons in the valence band can be excited to the conduction band by thermal or optical excitation [1, 2]. Hence, the electrical conductivity of a semiconductor lies between metal and insulator. An insulator has a similar band structure to a semiconductor but the bandgap is much wider (≥10.0 eV). It is quite impossible for the electrons to jump from the valence band to the conduction band. Therefore most of the electrons in insulators only fill all the available states in the valence band, thus they have high resistance. The summary of these can be seen in Table 2.1.

Table 2.1: Electrical conductivity and bandgap of three categories of materials.

Materials	Electrical conductivities $(\Omega cm)^{-1}$	Bandgap , E_g (eV)
Metals	$\sim 10^{0}$-10^{8}	≤0.3
Semiconductors	$\sim 10^{-8}$-10^{0}	~0.3-4.5
Insulators	$\sim 10^{-20}$-10^{-8}	≥4.5

In most cases, solar energy materials are based on semiconductors. These material must have certain characteristics depending on the purpose of that material used in the solar cell structure which aims to absorb the sunlight and convert them to generate and collect electron hole pairs [1]. For instance, the high optical absorption, direct bandgap, low density of recombination centres and high crystallinity are some of the desired

properties for the absorber layer, whereas high transmittance, wider bandgap, good adhesion and high conductivity are some of the sought after properties for the window layer and in particular the solar cell device.

Semiconductors have been widely used in electronic devices. They can be pure materials such as germanium [3], silicon [3-4], selenium [5] or binary compounds such as gallium arsenide (GaAs) [6], indium phosphide (InP) [7], cadmium telluride (CdTe) [8-10] or ternary compounds such as aluminium gallium arsenide (AlGaAs), cadmium zinc sulphide (CdZnS) or quaternary compounds such as copper indium gallium diselenide (CIGS) or gallium indium nitrogen arsenide (GaInNAs) [11-12]. The compound semiconductors can be grouped according to their respective valences such as III-V and II-VI semiconductors. Semiconductors can have either direct or indirect bandgaps depending on the positions of the maximum point of the valence band, E_v or the minimum point of the conduction band, E_c. A direct bandgap semiconductor can absorb light more easily because an electron in the E_v can be promoted directly to the E_c without a change in momentum. For instance, in the case of the photovoltaic behaviour in the solar cell device, the absorption of the photon energy occurs without any involvement of lattice vibrations. But in an indirect bandgap semiconductor, the E_c and E_v occur at different momenta. Therefore the electron needs to move from the E_v to E_c involving phonon interactions. CdS and CdTe have direct bandgaps and they both belong to II-VI semiconductor group [13].

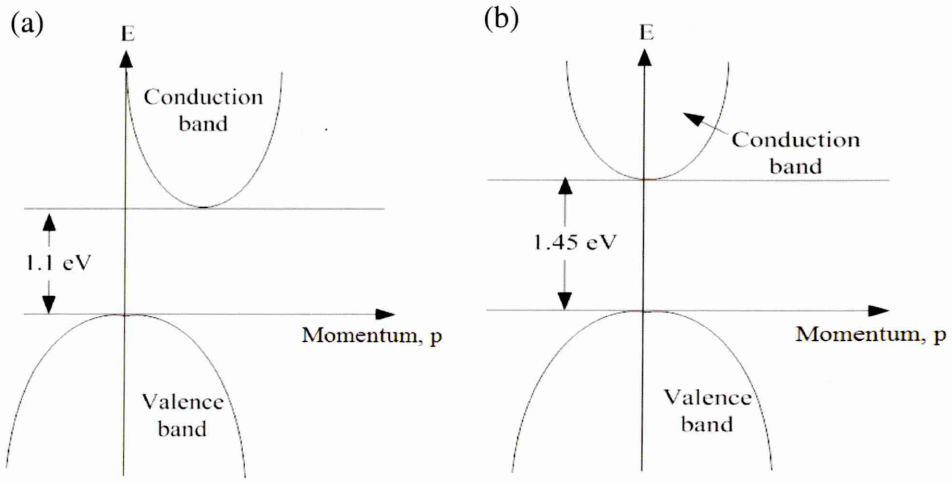

Figure 2.1: The examples of energy band diagram for (a) indirect (Si) and (b) direct (CdTe) bandgaps.

2.1.1 Intrinsic and extrinsic materials

An intrinsic semiconductor is a pure semiconductor without any significant dopant species present. The atoms of intrinsic semiconductor bond with each other with covalent bonding [2]. If one of the valence electrons receives sufficient energy it can release itself from the covalent bond and move inside the crystal. This unbound electron can now contribute to the flow of electrical current. By having more free electrons, the magnitude of electrical current can be increased. Therefore, impurities (dopant) added in small quantities such as parts per million (ppm) can increase the electrical conductivity [11,14]. By controlling the concentration in ppm of dopant, the characteristic of the device can be modified to obtain the desired material properties.

The doped intrinsic material is known as an extrinsic semiconductor. Doping atom can be either donor or acceptor. Donor atom has an extra electron while acceptor atom has an electron less. The intrinsic material doped with donor atoms becomes n-type material and the intrinsic material doped with acceptor atoms becomes p-type material. For instance the intrinsic silicon, Si material has four valence electrons. If this material is doped with arsenic, As atom with five valence electron, the As atom forms covalent bonds with its four neighbouring Si atoms, the fifth electron becomes a conduction electron that is donated to the conduction band [2]. The Si now becomes an n-type material with the Fermi level shifting towards the conduction band as shown in Figure 2.2 (b). On the other hand, if the intrinsic Si is doped with boron, the B atoms which has three valence electrons and an additional electron of Si is accepted to form four covalent bonds around the boron, and a hole is created in the valence band. The Si has now become p-type material with the Fermi level shifting towards the valence band as shown in Figure 2.2 (c).

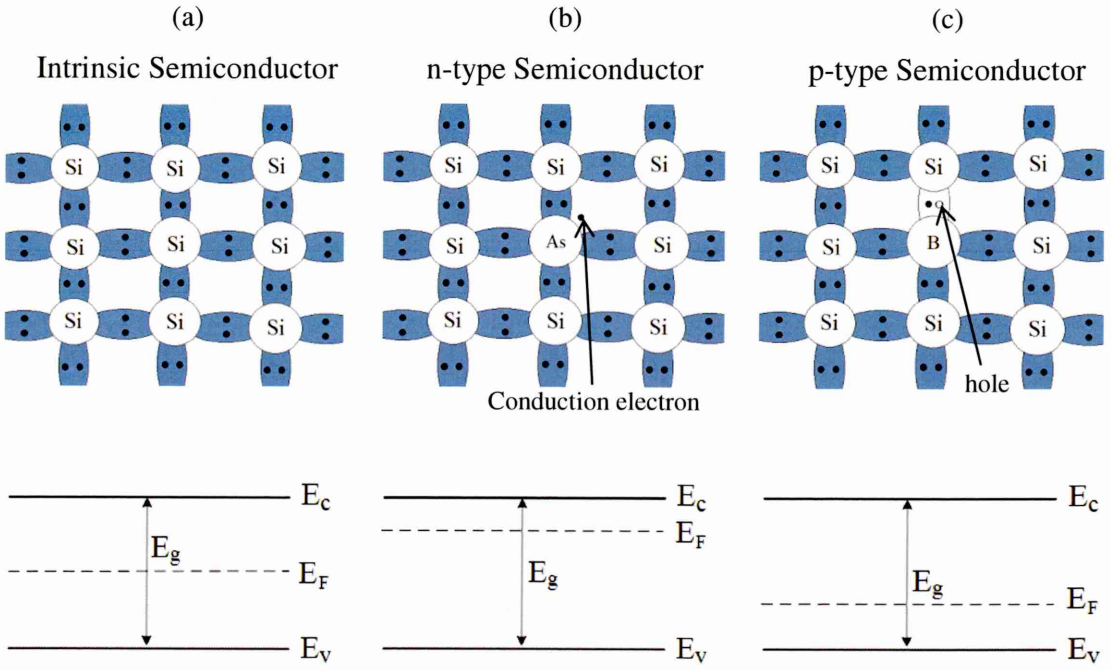

Figure 2.2: Schematic diagrams of covalent bonding in intrinsic Si crystal lattice, and covalent bonding between Si atoms and doping atoms. Also the schematic of energy band diagrams for intrinsic, n-type and p-type semiconductors.

2.1.2 Structure of materials

Structure of solid materials can be classified as crystalline, polycrystalline and amorphous. Crystalline is a single-crystal material where the crystal lattice of the entire solid is continuous and free of any grain boundaries. It can be prepared intrinsically by containing only the pure semiconductor, or extrinsically containing a very small quantity of other elements to change its semiconducting properties. Polycrystalline is a material with many crystallites of varying size and orientations. This crystallite is also knowns as grains and they are separated by disordered regions of grain boundaries. Polycrystalline solar cell is the most common type in the fast-growing PV market. Amorphous refers to materials that are without clear definition of shape or form and completely lack long-range order.

Crystalline structures have a unique and fixed arrangement of atoms or molecules with respect to the point of the lattice [15]. Ideally, there are only fourteen crystal lattices possible in a three-dimensional space [14,16]. They are actually formed by seven crystal families with different Bravais lattices as shown in Figure 2.3. A Bravais lattice is the different lattice crystal arrangement formed in a crystal family. In two dimensions there are five different Bravais lattices, while in three dimensions there are fourteen. These fourteen lattices are further classified as shown in Table 2.2 which

define that a_1, a_2 and a_3 are the magnitudes of the unit vectors and α, β and γ are the angles between the unit vectors.

Table 2.2: The summary of the crystal shapes, number of Bravais lattices and conditions.

Crystal shape	Number of Bravais lattices	Conditions
Cubic	3	$a_1 = a_2 = a_3$ $\alpha = \beta = \gamma = 90^o$
Tetragonal	2	$a_1 = a_2 \neq a_3$ $\alpha = \beta = \gamma = 90^o$
Hexagonal	1	$a_1 = a_2 \neq a_3$ $\alpha = \beta = 90^o, \gamma = 120^o$
Orthorhombic	4	$a_1 \neq a_2 \neq a_3$ $\alpha = \beta = \gamma = 90^o$
Rhombohedral	1	$a_1 = a_2 = a_3$ $\alpha = \beta = \gamma < 120^o \neq 90^o$
Monoclinic	2	$a_1 \neq a_2 \neq a_3$ $\alpha = \beta = 90^o \neq \gamma$
Triclinic	1	$a_1 \neq a_2 \neq a_3$ $\alpha \neq \beta \neq \gamma$
Total crystal lattice	14	

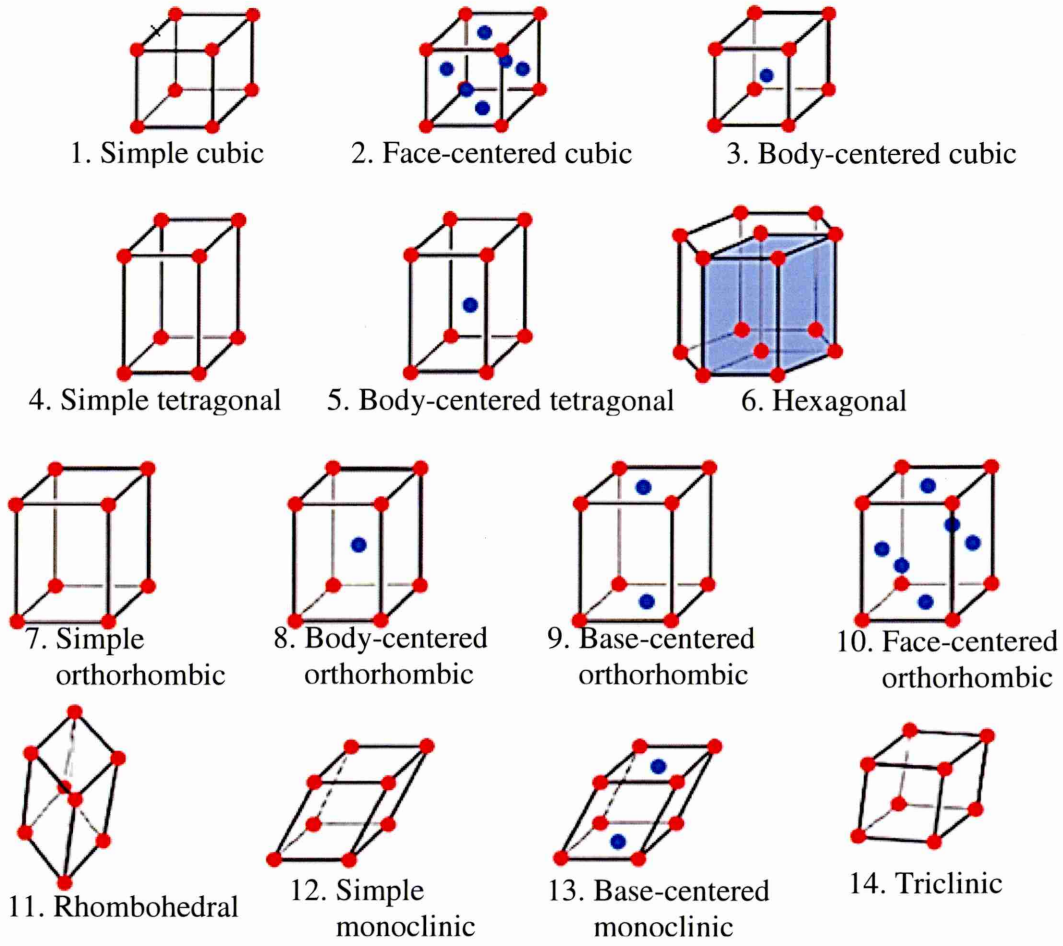

Figure 2.3: The 14 different crystal lattices of materials.

Compound semiconductors such as CdTe typically have a structure based on cubic crystal systems with a zinc-blended lattice as shown in Figure 2.4 (a). The lattice comprises two different types of atoms which are Cd and Te with ionic radius of 1.55 Å and 1.42 Å, respectively [17]. Each Cd atom in the zinc-blend lattice has four covalent bonds with Te atoms at the corner of the tetrahedron. CdS can be either cubic or hexagonal in structure. The hexagonal structure can be shown in Figure 2.4 (b). CdS crystallised in wurtzite lattice inside a hexagonal unit cell which has lattice points at the corners defining each hexagonal face and at the centre of the two faces [16]. The hexagonal structure contains of Cd and S atoms with atomic radius 1.55 Å and 1.00 Å, respectively [17]. Similar to the zinc blend structure, each of the Cd atoms has four covalent bonds with S at the corner of a tetrahedron and each of S similarly surrounded by four Cd atoms. The Cd and S bonds parallel to the *c*-axis all point in the same direction contrasting with the zinc-blend structure, forming a unique and symmetrical axis as shown in Figure 2.4 (b). When CdS/CdTe interface is formed, the lattice parameter of CdS is reduced or the lattice mismatch transit gradually from CdS to CdTe

with fewer interface states. The lattice mismatch between hexagonal CdS and cubic CdTe is ~9.7%. This can be calculated using equation 2.1.

$$\text{Lattice mismatch} = \frac{Lattice\ constant\ material\ A - Lattice\ constant\ material\ B}{Lattice\ constant\ material\ B} \times 100\% \qquad (2.1)$$

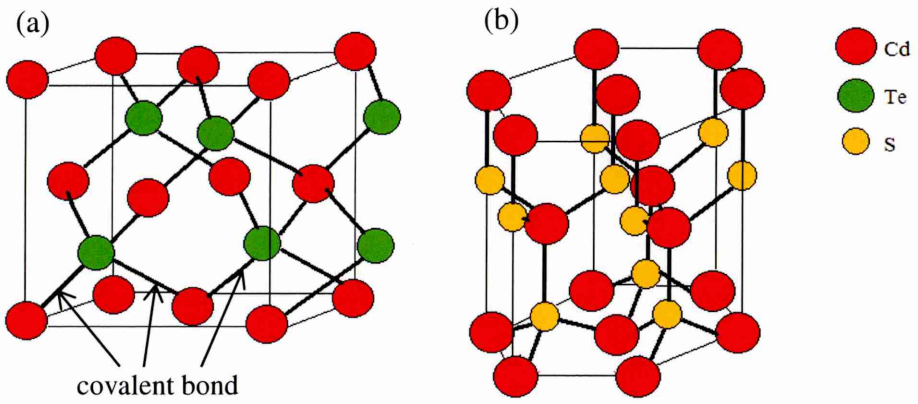

Figure 2.4: The crystal structure diagram of (a) zinc blend of CdTe and (b) wurtzite or hexagonal structure of CdS [18].

2.1.3 Polymer

Apart from that, a study on a polymer material is also covered in this thesis. Polymer is the material with very large molecules that are made up of small molecular units or "mers" that link together into chainlike or network structures [17]. Polymer can be organic or inorganic. Organic polymer is a polymer with the backbone chain made from carbon-carbon linkage. Most organic polymers are lightweight, tough and easy to fabricate, however they have some limitations at higher temperatures. An inorganic polymer is a polymer with a skeletal structure that does not include carbon atoms. These are such as polyphosphazenes, polydimethylsiloxane and polythiazyl. Although some polymers could be considered as insulators, a few polymers are also considered to be electrical conductors and a number of them possess semiconductor properties [13]. The simplest polymer is known as polyethylene.

Some of the polymers are crystalline but they possess none of the classic structural perfection of metal or semiconductor crystal whose atoms have a fixed arrangement order. The polymer molecules fold into a parallel length of 5-50 nm to form crystalline platelets and the fraction of the polymer molecule remains disordered to facilitate incomplete crystallisation [17].

Polymers can be synthesised by a chemical reaction that binds the "mers" together into a macromolecule. For this reason, the starting material must be chemically reactive. For instance, in a simplest polymer such as polyethylene; the reactivity is provided by the double bond between the two carbon atoms in the ethylene molecule. This double bond can be opened, making the bonding to other ethylene molecules, forming polyethylene. This type of reaction leads to addition polymerisation or chain polymerisation. On the other hand, the synthesis reaction also can occur between an organic acid, amine or an alcohol. This can be shown in Figure 2.5.

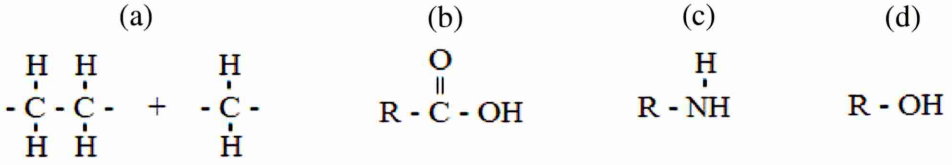

Figure 2.5: The chain polymerisation (a) with the same molecule in polyethylene, (b) with an organic acid, (c) with an amine and (d) with an alcohol. Note that R denotes an organic radical.

Polymerisation requires the radical ions to initiate free radical and/or ionic polymerisation. Radical initiation works best on the carbon-carbon double bond and the carbon-oxygen double bond. The examples of initiation for the polymerisation are such as thermal decomposition, photolysis, persulfates, ioning radiation and electrochemical reaction. Electrochemical is an initiation in electrolysis of a solution which contains monomer and electrolyte. For instance which related to this work, in cathodic electrodeposition, a monomer molecule will receive an electron at the cathode and becomes a negative radical ion known as radical anion, whereas in anodic electrodeposition a monomer molecule will donate an electron at the anode to form a positive radical ion or what is known as radical cation [18]. This can be illustrated in Figure 2.6. The free radicals are transferred from the initiator molecules to the monomer to form a bond with another free radical to produce a chain growth polymerisation.

(a)

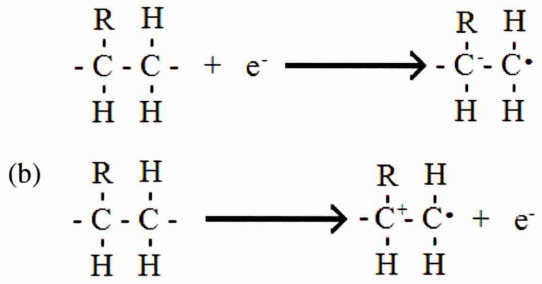

Figure 2.6: Formation of (a) radical anion at the cathode and (b) radical cation at the anode in electrochemical deposition.

The electron energy levels in polymers can be labelled as highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) and the energy difference between these two is HOMO-LUMO gap. The concept of these terms is similar to the conduction band minimum, valence band maximum and the energy bandgap in inorganic semiconductors. LUMO is equivalent to the conduction band minimum, HOMO is equivalent to the valence band maximum and HOMO-LUMO gap is the energy bandgap.

The polymer which will be used in this research is polyaniline. Polyaniline is a kind of organic polymer which has a unique property since it can be converted to conductive, semi conductive and resistive polymers by appropriate oxidation or doping [4]. Polyaniline can be prepared by electrochemical polymerisation of aniline monomer [19, 20]. Many derivatives of polyaniline were also synthesised by polymerising ring- or nitrogen-substituted aniline monomers and by copolymerisation. There has been much progress in improving the synthetic methodology and elucidating the mechanism of polymerisation. Polyaniline in the base form consists of two main structural units which are benzenoid diimine and quinoid diamine [20]. It can be represented schematically by the following formula in Figure 2.7:

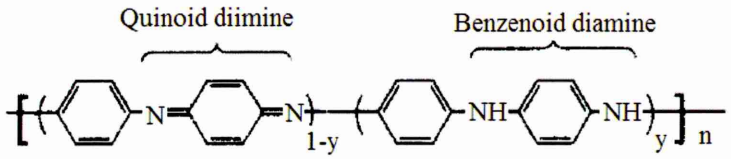

Figure 2.7: The chain structure of polyaniline.

The oxidation state of polyaniline is determined by the y values. Pernigraniline is the completely oxidized form with y = 0, whereas leucoemeraldine is the fully reduced form y = 1 [21, 22]. Emeraldine contains an equal fraction of both reduced and oxidised

forms (y=0.5). This work will focus on leucoemeraldine and pernigraniline based on polyaniline. This behaviour will be discussed more in Section 2.1.4.3.

2.1.4 Materials used in this work

2.1.4.1 Cadmium Sulphide

In recent years, the CdS thin film has become increasingly important due to its applications in many industrial fields. CdS is an n-type semiconductor with a wide direct band gap of 2.42 eV for bulk material at room temperature [21]. This layer demonstrates a good conversion efficiency (above 21%) when employed as a window layer in combination with absorber materials such as CdTe [22, 23] and CIGS ($CuInGaSe_2$) [21]. Therefore, CdS thin films have been used widely as window layers in solar cells. CdS thin films have been deposited by various methods such as dip coating [24], chemical bath deposition (CBD) [25, 26], spray pyrolysis [23, 27], vapour deposition [26] and electrodeposition [26, 29]. Electrodeposition is an attractive technique for the preparation of CdS because it uses relatively inexpensive instruments, enables deposition of large area films and provides easier control of growth parameters.

A highly crystalline structure, higher optical transmission in wavelength >512 nm, wide optical band gap with n-type electrical conductivity, films with minimum defects, lower thickness (<200 nm) and highly uniform layers are the fundamental requirements for solar cell window layers [26]. In order to meet these requirements, CdS thin films should be grown in desired environments without harmful impurities. In the case of electroplating, $Na_2S_2O_3$ is normally used as a sulphur source [22, 26, and 29]. Although sodium (Na) ions are not electrodeposited at low cathodic voltages, Na can be incorporated in CdS films via absorption or adsorption and chemical reactions as Na accumulates in the bath where $Na_2S_2O_3$ is gradually added to the electrolyte. Na is a p-type dopant in CdS [21], and it can increase the electrical resistivity of n-CdS layers introducing detrimental effects for solar cell application. In order to avoid this situation, $(NH_4)_2S_2O_3$ has been used as the sulphur source in this research. With this precursor, CdS layers can be grown continuously with a long bath lifetime, avoiding accumulation of harmful elements such as Na. The study on the growth and characterisation of CdS layers by electrodeposition using $(NH_4)_2S_2O_3$ as sulphur precursor will be present in Chapter 4.

2.1.4.2 Cadmium Telluride

CdTe is one of the most promising photovoltaic (PV) thin film materials for solar cell applications with the conversion efficiency of 21.5%, reported by the First Solar in February 2015 [29]. CdTe has high optical absorption coefficient with a direct bandgap of 1.45 eV at room temperature (300 K), which is close to the ideal bandgap for absorbing the maximum amount of the solar spectrum using one bandgap p-n junction.

Various techniques have been reported for preparation of CdTe thin films such as physical vapour deposition (PVD) [30], RF sputtering [31], spray pyrolysis [32], close-space sublimation (CSS) [33,34] and electrodeposition (ED) [35-40]. Electrodeposition is an attractive technique for the preparation of CdTe because of its affordability, simplicity, scalability, manufacturability and ability to obtain p-, i- or n-type materials by controlling the cathodic voltage during electrodeposition [40-42]. Cathodic electrodeposition of CdTe was first reported by Mathers and Turner in 1928 using an aqueous solution of $CdSO_4$ and TeO_2 [35]. The work on this electrodeposition remained silent for 50 years until Panicker et al. reported their study on CdTe electrodeposition in 1978 [36]. Afterwards, the electrodeposition technique has been widely used and later modified to anodic and non-aqueous deposition [43-45].

In electrodeposition, the Cd source of CdTe was conventionally from $CdSO_4$ precursor [36-39]. Then, the deposited CdTe layer should undergo $CdCl_2$ treatment to activate the properties of CdTe for a better performance in CdS/CdTe solar cells. $CdCl_2$ treatment is well-known since 1979 [46] as an activation step of CdTe solar cells and the efficiency of solar cells is always improved by an order of magnitude with this so-called 'magic step' [47,48]. The $CdCl_2$ treatment is believed to promote the grain growth, improve recrystallisation and lifetime of charge carriers, change the doping concentration, and remove defects and Te precipitations in the CdTe thin films [49,50]. With regards to these advantages, a systematic study on CdTe electrodeposition from an aqueous solution containing chloride precursor was carried out in this work by using $CdCl_2$ as the Cd source instead of $CdSO_4$. Although Bonilla and Dalchiele [51] have reported their initial efforts on this, no systematic study has been made so far. The study on the growth and characterisation of CdTe thin films grown by the three-electrode system using $CdCl_2$ as the Cd source is presented in Chapter 5.

2.1.4.3 Polyaniline

PAni has been studied extensively and is finding increasing uses in various fields of technology such as in anti-corrosion coatings, gas sensors, actuators and light emitting displays (LEDs) [52-53]. PAni is known as a unique polymer, with highly tuneable bandgap, high chemical stability and processability with a potential application in various fields. As mentioned briefly in Section 2.1.3, PAni comes in three oxidation states, known as leucoemeraldine (fully reduced), emeraldine (half reduced, half oxidised) and pernigraniline (fully oxidised). This can be seen in Figure 2.8. The oxidation state of PAni can be represented by the distinctive colour appearance of the layer. For instance, the fully oxidised pernigraniline base is violet but the protonate pernigraniline salt is blue, the emeraldine base is light green but protonate emeraldine salt form is dark green and the fully leucoemeraldine base is colourless, but protonate leucoemeraldine salt is pale yellow [54,55]. The chemical properties, conductivity and colour of the PAni also vary with the degree of protonation, electrode potential and/or concentration of the acid or base used [56].

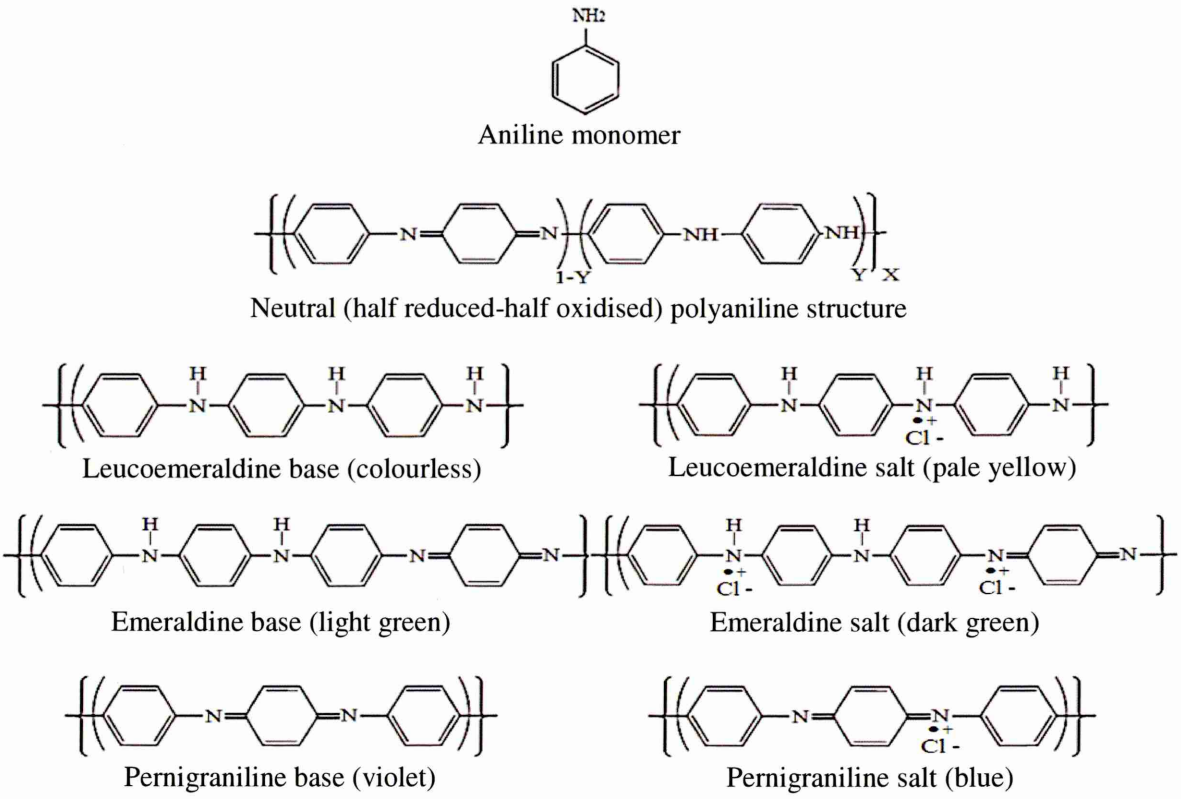

Figure 2.8: The aniline monomer, its neutral polymerised form and possible states of oxidised polyaniline and colour appearance.

All three PAni bases are generally non-conducting. However, the conductivity of base polyaniline can be modified by doping with protonic acid. For instance, the doped emeraldine base can turn into semiconducting or conducting polymer depending on the doping concentration and this material is then called emeraldine salt. During the doping process, the protonic acid allocates the coordination of protons with amine nitrogen of emeraldine base and consequently leads to a change in the delocalisation in conjugate backbone and improves the DC conductivity [53,57]. The emeraldine salt has a conductivity in the range of ~0.01 to 100 $(\Omega\ cm)^{-1}$, which in many orders of magnitude is higher than a common polymer ($<10^{-9}(\Omega\ cm)^{-1}$) and lower than the typical metal ($>10^{5}\ (\Omega\ cm)^{-1}$) [54, 58]. The same goes for the leucoemeraldine and pernigraniline bases. Doping these two bases can change their colour and conductivity to form leucoemeraldine salt and pernigraniline salt [59]. The doping is usually by the strong acids. Acid was introduced to ammonia and amine in the PAni chain. The protonation of amines by acids binds a non-oxidised nitrogen atom with protons, and forms ammonium cation and is stabilised by acid anion. The interaction between acid and oxidised nitrogen atom changes between acid and neutral nitrogen. PAni polarons are stabilised rather by acid anion than by proton. At the same time, the proton remains relatively free thus providing high proton conductivity of PAni which is absent in ammonia salts and protonated amines [60].

The electrochemical polymerisation of aniline typically performed in strongly acidic aqueous electrolytes through several chemical chain reaction such as formation of anilinium radical cation, radical coupling, increasing of chains and organisation into complex super-molecule structures [61]. The electrochemical polymerisation of aniline is always carried out in anodic deposition, although polymerisation in cathodic electrode was also reported [62, 63]. The study on the growth and characterisation of PAni thin films grown from anodic and cathodic deposition is presented in Chapter 6.

2.2 Junctions and interfaces in solar cell devices

Solar cell converts photon energy into electricity through photovoltaic effect. When photons are absorbed, they transfer their energy to release electrons and generate electron-hole pairs. These charges must be separated immediately before the recombination occurs. In inorganic based semiconductor solar cells, the separation of generated charges is formed by a built in electric field within the device. This field is usually produced by the fabrication of various junctions between several types of

materials which can be semiconductors, metals and insulators. The sort of junctions used or available in solar cells will be discussed in this section.

2.2.1 Homojunction and heterojunction

Homojunction is a junction made from one type of material through different doping while heterojunction consists of two different materials with different bandgaps [2, 10,12]. Homojunction can be p-n, n^+-n or p^+-p junctions. In the case of p-n homojunction, the material can be doped with n-type and p-type material without altering the bandgap. This is such as n-Si and p-Si joining together to form p-n homojunction. The highest potential step can be produced using the p-n junction. As for p^+-p or n^+-n homojunction, doping level has been varied in the material. For instance, Si which has been heavily doped with boron, B and another Si which has been lightly doped with B form p^+- and p- type Si. If these two materials are joined together, they will form p^+-p junction. This is similar to n^+-n homojunction condition. The band diagrams for these are illustrated in Figure 2.9.

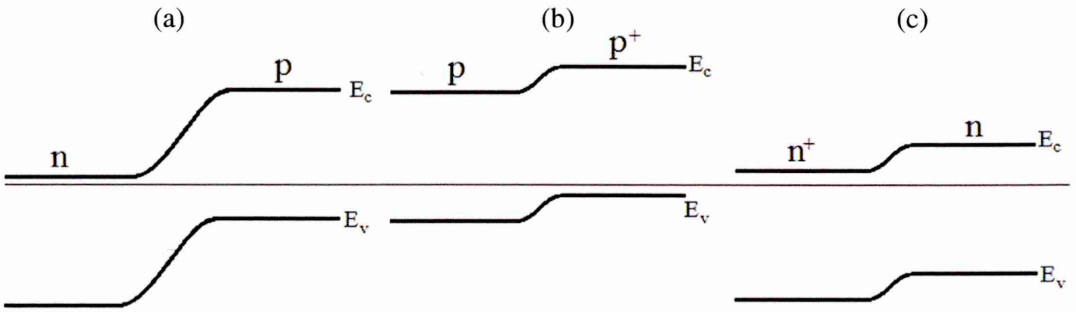

Figure 2.9: The band diagram of (a) p-n homojunction (b) p^+-p homojunction and (c) n^+-n homojunction.

Heterojunction can be formed when two semiconductor materials with different bandgaps form an intimate contact. Similar to homojunction, heterojunction also can be p-n, n^+-n and p^+-p junctions. The p-n heterojunction can be formed by joining two different materials with different electrical conductivity type. These are such as n-CdS/p-CdTe, n-ZnS/p-ZnTe, n-ZnO/p-SiC, etc. The n^+-n and p^+-p heterojunctions can be formed by joining two different materials with the same electrical conductivity type but with different level of doping. The examples of n^+-n heterojunctions are such as n-ZnS/n-CdS, n-CdS/n-CdTe, etc. while the examples of and p^+-p heterojunctions are such as p-ZnTe/p-CdTe, p-GaAs/p-GaN, etc. A good heterojunction should have ideal lattice matching to prevent the strain and stress at the junction and interface since it can

lead to dislocation and charge carrier trap centres. The band diagram for p-n, n-n and p-p heterojunction can be seen in Figure 2.10.

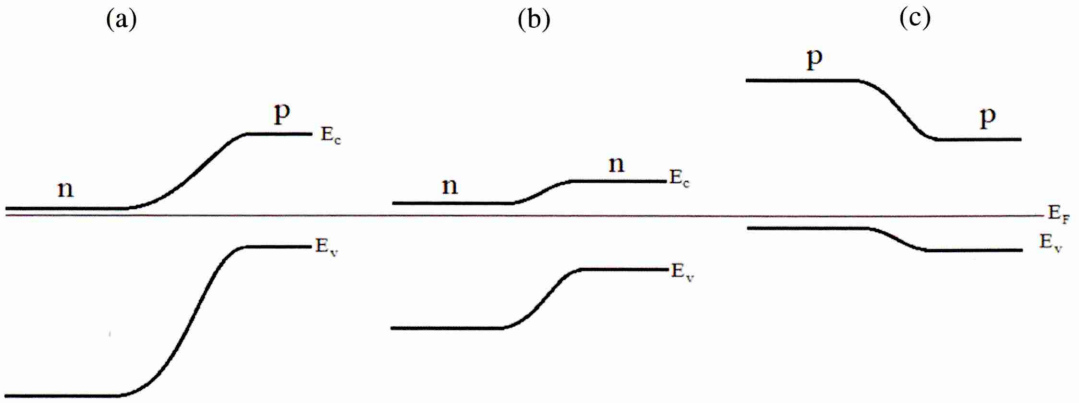

Figure 2.10: The band diagram of (a) p-n heterojunction (b) n-n heterojunction and p-p heterojunction.

2.2.2 p-n and p-i-n junctions

The p-n junction is one of the common junctions used in solar cells. The concept of p-n junction has been discovered by Russell Oh from Bell Telephone Labs in Holmdel and this concept has been applied by Bardeen, Schockley and Brattain for their transistor effect which led to a Nobel Prize in 1956 [64]. p-n junction can be a homojunction or a heterojunction as described earlier in Figure 2.9 (a) and 2.10 (a) respectively.

The p-n junction can be formed either by doping the particular material with n- and p-type dopants, or by joining the two different semiconductors with different bandgaps and conductivity types together. The p-type semiconductor has majority positive charge carriers (holes) while the n-type semiconductor has majority negative charge carriers (electrons) in the materials. During the formation of the p-n junction, the electrons from the n-type semiconductor diffuse into the p-type semiconductor and holes from the p-type semiconductor diffuse into the n-type semiconductor. This forms a space charge region at the junction which is known as a depletion region. An electric field is created within the junction due to the concentration of ionised donors and acceptors on the opposite sides of this junction. In the case of band diagram description, when p-type and n-type semiconductors are in contact, the Fermi level will align, thus developing potential barrier, ϕ_b and internal electric field, E_i between these two charged layers. At the junction, electrons start to recombine with holes and form a depletion

region. The diffusion of electrons leave positively charged ionised donors on the n-side and the diffusion of holes leave negatively charged ionised acceptors on the p-side [65]. This behaviour can be illustrated in Figure 2.11.

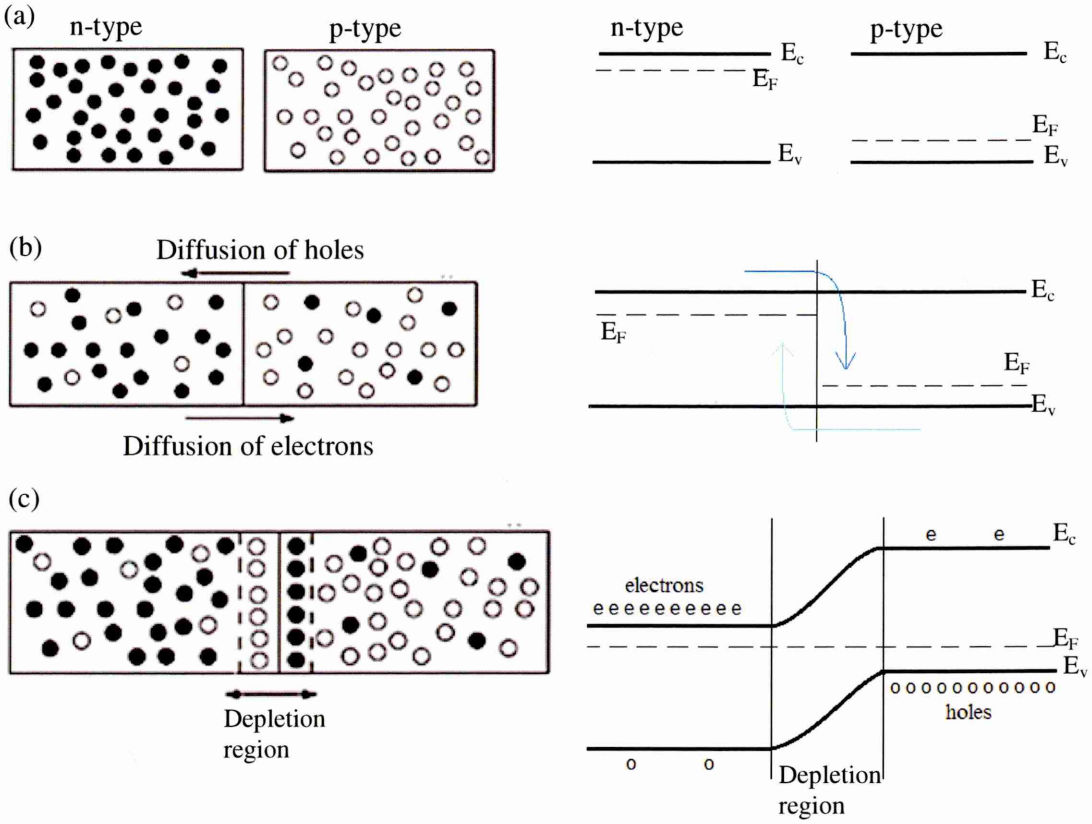

Figure 2.11: Schematic diagrams and energy band diagrams of a p-n junction (a) before intimate contact (b) during intimate contact and (c) after intimate contact.

The p-i-n junction is an advanced stage of the p-n junction. In the same way as p-n junction, p-i-n junction can be formed by a homojunction or a heterojunction depending on the desired materials used. The band diagram of p-i-n homojunction and p-i-n heterojunction can be seen in Figure 2.12. The p-i-n junctions can be formed by incorporating an intrinsic (i-type) semiconductor in between p-type and n-type semiconducting layers. This arrangement aligns the Fermi level of two semiconductors through i-type material. In this case, all the photo-generated charge carriers happen within the intrinsic material. Therefore the material should be carefully selected and fabricated to avoid the impurities and high resistance.

The advantage of the junction having p-i-n junction is the controllability of the width of the space charge region. The high open circuit voltage, V_{oc} also can be obtained due to the presence of high potential barrier, ϕ_b. The example of p-i-n junction in solar

cell devices are such as amorphous silicon solar cell, and CdTe solar cell which comprise of p-ZnTe, i-CdTe and n-CdS or p-i-n CdTe thin films [66-68].

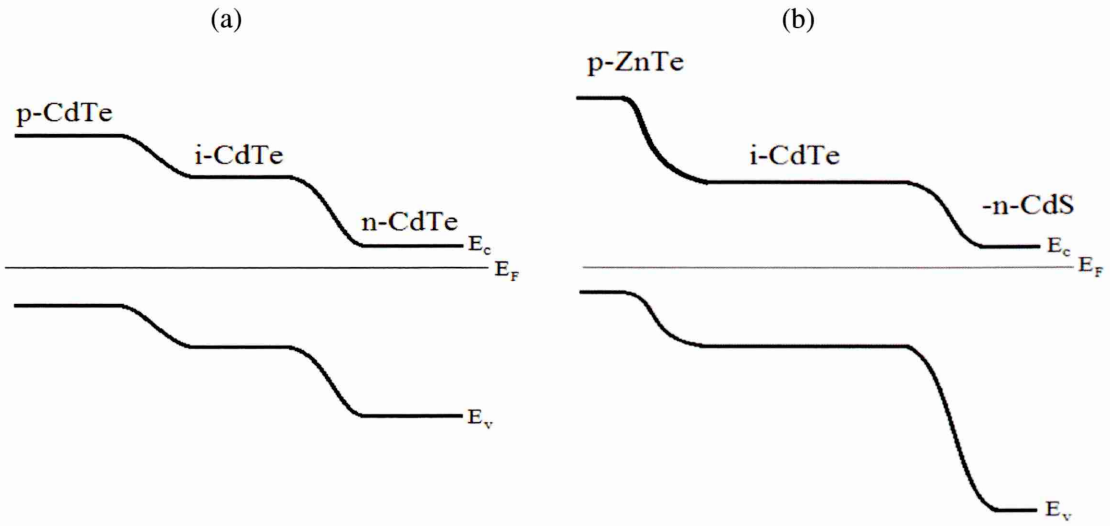

Figure 2.12: The schematic diagram of (a) a p-i-n homojunction formed by p-CdTe/i-CdTe/n-CdTe and (b) a p-i-n heterojunction formed by p-ZnTe/i-CdTe/ n-CdS in solar cell device.

2.2.3 Metal-Semiconductor interfaces: Schottky diodes and Ohmic contacts

Metal-semiconductor junctions are important components in solar cell devices since these are responsible for collecting the photo-generating charge carriers and transporting them to an external circuit. They can be classified into two which are Ohmic junction and Schottky diodes dependent on the characteristics of the interface, in particular the work function of the metal, ϕ_m and electron affinity of the semiconductor, χ_{sc} [69]. When a metal with ϕ_m forms an intimate contact with an n-type semiconductor with χ_{sc}, if ϕ_m value is less than χ_{sc} value ($\phi_m < \chi_{sc}$), the Ohmic contact is formed; however if ϕ_m value is higher than χ_{sc} value ($\phi_m > \chi_{sc}$), the rectifying Schottky diode is formed. On the other hand, when metal with ϕ_m forms an intimate contact with p-type semiconductor with χ_{sc}, if ϕ_m value is less than χ_{sc} value ($\phi_m < \chi_{sc}$), the rectifying Schottky diode is formed; but if ϕ_m value is higher than χ_{sc} value ($\phi_m > \chi_{sc}$), the Ohmic contact is formed. The list of ϕ_m of common metal contacts and χ_{sc} of common semiconductors used in solar cells are listed in Table 2.3.

Table 2.3: Metal work functions of some metals, and electron affinities of some semiconductors.

Metal contact	Metal work function, ϕ_m (eV)	Semiconductor material	Electron affinity, χ_{sc} (eV)
Al	4.08	Si	4.01
Au	5.10	CdS	4.80
Pt	6.35	CdTe	4.40
Hg	4.50	ZnS	3.90
Ag	4.26-4.73	ZnTe	3.54
Cu	4.70	CdSe	4.58

Metal/Semiconductor contact has a significant effect on the performance and behaviour of solar cell devices. The formation of rectifiying contact arises from the separation of charges at the metal-semiconductor interface. The energy band diagrams in Figure 2.13 illustrate the process of Schottky barrier formation. Figure 2.13 (a) shows the electron energy band diagram of a metal having a work function, ϕ_m and an n-type semiconductor of work function ϕ_s with electron affinity χ_{sc}. When these two materials are brought into intimate contact, electrons from the conduction band of the semiconductor, which have higher energy than the metal electrons, flow into the metal until the Fermi levels on the two sides, are brought into coincidence. As the electrons move out of the semiconductor into the metal, the free electron concentration in the semiconductor region near the boundary decreases. Since the separation between the conduction band edge E_c and the Fermi level E_f of the semiconductor increases with decreasing electron concentration, the conduction band edge near the interface bends up as shown in Figure 2.13 (b) [70].

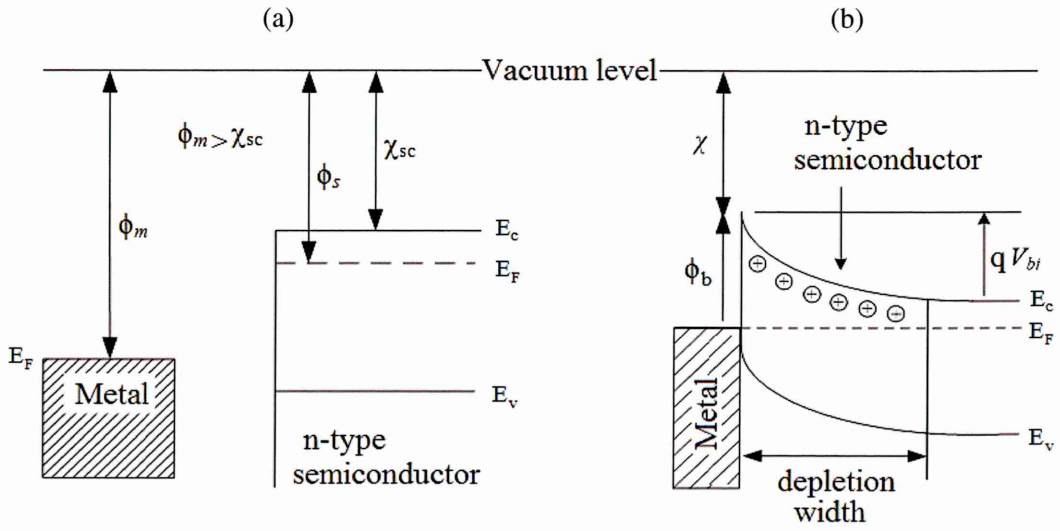

Figure 2.13: The formation of a Schottky barrier between a metal and an n-type semiconductor (a) before contact and (b) after contact [71].

The conduction band electrons which cross over into the metal leave a positive charge of ionised donors behind, so the semiconductor region near the metal gets depleted of mobile electrons. Thus a positively charge layer is established on the semiconductor side of the interface and the electrons which cross over into the metal form a thin sheet of negative charges. As a result, an electric field is established from the semiconductor to the metal. The amount of band bending is equal to the difference between the two vacuum levels:

$$qV_{bi} = \phi_m - \phi_s \qquad (2.2)$$

where V_{bi} is the built-in potential of the junction and qV_{bi} is the potential barrier seen by electrons moving from the semiconductor to metal. The formation of potential barrier, ϕ_b is given by:

$$\phi_b = \phi_m - \chi_{sc} \qquad (2.3)$$

The rectifying electrical property of the device is given by the equation (2.4):

$$J_D = A^* T^2 e^{\left(\frac{-q\phi_b}{kT}\right)} \cdot \left[e^{\left(\frac{qV}{nkT}\right)} - 1\right] \qquad (2.4)$$

Where J_D is the dark current density (Acm^{-2}), A^* is the effective Richardson constant for thermionic emission ($Acm^{-2}K^{-2}$), n is the ideality factor of the diode and V is the external applied voltage.

Ohmic contacts are relatively simpler to make, by ensuring direct contact between the metals without intervening layers of insulating contamination or oxidation. It is a non-rectifying junction which has a linear current-voltage (I-V) curve as with Ohm's law. Low resistance Ohmic contacts are used to allow charge to flow easily in both directions between the two conductors, without blocking due to rectification or excess power dissipation due to voltage thresholds.

2.2.4 Metal-Insulator-Semiconductor junctions

The potential barrier, ϕ_b formed in Schottky diodes are generally lower than the potential barrier of p-n junction. Therefore the open circuit voltage, V_{oc} of the Schottky barrier solar cell is usually low due to the low potential barrier. Therefore the incorporating of a very thin insulating layer in between metal and the semiconductor is able to increase the ϕ_b and as a result the V_{oc} can be improved. This is shown in Figure 2.14. The insulating layer could be polymer materials such as PAni. Therefore the use of polyaniline (PAni) in reality can provide two purposes, one is as a pinholes plugging layer and another one can increase the barrier height due to the MIS structure. However the thickness of the insulating layer should not be too thick. The incorporation of an insulator layer in between metal and semiconductor contact also can minimises the interaction between metal and semiconductor due to the in and out diffusion of semiconductor and metal elements and improves the stability and lifetime of photovoltaic devices.

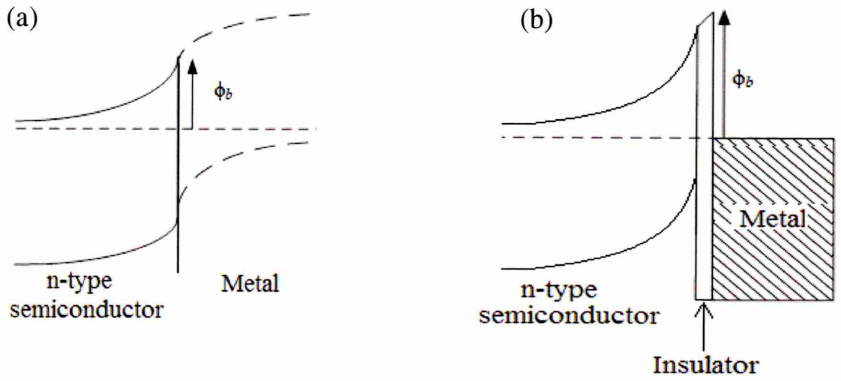

Figure 2.14: Band diagram showing (a) the potential barrier of typical metal-semiconductor interface and (b) the increment of the potential barrier after incorporating an insulating layer between metal and the semiconductor.

2.3 Thin film deposition

Thin film is a material with thickness ranging from several nanometers (nm) to micrometers (μm). Thin films were first obtained by Robert Boyle and Robert Hooke as interference patterns in 1650. The development of the first thin film deposition and method of thickness measurement by Faradays and co-workers in 1850 has brought about commercialisation of this method for gold plating of uniform accessories at the beginning. Now, thin film is widely used in semiconductor electronic technology, the manufacturing processes, optical and mechanical applications, protective coatings and tribology industry. There are a wide variety of techniques of thin film depositions. In general, these can be classified into two main categories, namely the physical deposition and chemical deposition.

Physical deposition refers to a wide range of technologies where a material is released from a source and deposited on a substrate using mechanical, electromechanical or thermodynamic process. These are such as magnetron sputtering, radio frequency (RF) sputtering, molecular beam epitaxy (MBE), closed space sublimation (CSS), etc. [72]. Chemical deposition used a volatile fluid precursor or gases to produce a chemical reaction on the surface and leaves behind a chemically depositing coatings of a thin film on the surface. These are such as chemical bath deposition (CBD), electrodeposition, chemical reduction plating, spin coating, chemical vapour deposition, (CVD) including metal organic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), etc. The variety of methods of thin film deposition can be summarised in Table 2.4.

Table 2.4: The classification of thin film deposition techniques.

Physical		Chemical	
Sputtering	Evaporation	Gas environment	Liquid environment
▪ Radio frequency (RF) sputtering ▪ Magnetron sputtering ▪ A.C. sputtering ▪ D.C. sputtering ▪ Ion beam sputtering ▪ Triode sputtering	▪ Vacuum evaporation ▪ Close space sublimation (CSS) ▪ Molecular beam epitaxy (MBE) ▪ Ion beam deposition ▪ Laser evaporation ▪ Flash evaporation ▪ Electron beam evaporation	▪ Chemical vapour deposition (CVD) ▪ Metal organic chemical vapour deposition (MOCVD) ▪ Photo-chemical vapour deposition ▪ Plasma enhance chemical vapour deposition (PECVD)	▪ Electrodeposition ▪ Chemical bath deposition (CBD) ▪ Spin coating ▪ Polymer assisted deposition (PAD) ▪ Spray pyrolysis ▪ Liquid phase epitaxial

2.3.1 Various deposition techniques in thin film solar cells

Thin film solar cells can be prepared by several techniques depending on the materials used and type of solar cells. For instance, Si based solar cells can be fabricated using PECVD or RF sputtering while CIGS solar cells can be fabricated using CBD, RF sputtering, CSS, CVD or PECVD. GaAs based solar cells can be grown by MBE or MOCVD and CdTe based solar cells can be fabricated using CBD, CSS, RF sputtering or electrodeposition techniques [32-77].

MBE is one of the physical vapour deposition techniques which able to produce a single crystal of epitaxial layer in ultra-high vacuum [78]. This deposition technique initiates by giving heat onto the ultra-pure solid element sources to sublime and condense on the substrate. The evaporated atoms do not interact with each other in the vacuum chamber until they reach the substrate. The timing and flux of beams can be controlled by shutters which separate the sources from the substrate. The composition and the thickness of the layers can be precisely controlled by a computer down to a single layer of atoms. MBE produces the uniform layer with low defect concentration and provide the facility for developing thin film architectures. However, this equipment is extremely expensive, requires high maintenance and provides a slow deposition ratio.

RF sputtering is also a physical deposition technique which involves emission of material from the source on to the substrate using radio frequency (RF) power supply [79]. The sputtered atoms emitted from the source have a wide energy distribution. RF

requires more power input to achieve the same effect as an electron current, therefore the inert gas plasma in RF system can be maintained at a much lower pressure and this makes RF sputtering ideal for target materials that have insulating qualities. The main drawback with RF sputtering is the uniformity of deposition and difficulty to produce high quality thick coatings due to high internal residual stress levels [79].

CSS is one of the physical deposition techniques perform in vacuum or in inert gas environment at high temperature [80]. In this equipment, the substrate is placed close to the source. The deposition initiated by giving thermal heating to the source vessel to sublime the coating material. The film growth occurs close to the equilibrium condition with a small difference in temperature which limits the deposition rate. Although CSS deposition is simple, low cost and ability to offer the deposition at high transport efficiency, it only offers a limited number of material depositions because of limited heating capacity to heat source material and there is no thickness monitoring system to check the growth rate or thickness of the film during deposition.

CVD is a chemical vapour deposition technique with extremely complex processes and involves a series of gas-phase and surface reactions. CVD relies on reactive carrier gases to transport the precursors of the desired material to the substrate surface. The material then reacts with other gases or decomposes to produce stable reaction products and deposit on the substrate. This action is performed in a rough vacuum chamber using a thermal heating or plasma energy source to provide energy for the chemical reaction [81]. CVD is among the most versatile deposition techniques because it provides a wide range of chemical reactants and reactions and able to produce a variety of films for a wide range of applications. It also can be divided into several subcategories such as PECVD, MOCVD, etc.

PECVD is a chemical deposition based on gas or vapour to form solid films on the substrate. The deposition process starts with the creation of plasma of the reacting gas by RF or direct current discharge between two electrodes. This is then followed by the chemical reactions on the surface to create the solid thin film [81]. PECVD is one of the fastest deposition techniques with a low temperature which produces a good film quality compared to sputtering or MBE depositions. However, the high cost of the equipment and the toxic by-product become a drawback of using this technique.

MOCVD is one of the chemical vapour depositions which is able to produce either single or polycrystalline thin films. The crystal layer is grown by injecting ultra-pure gases to a reactor followed by a gas phase reaction to produce a very thin layer of atoms onto a surface of substrate. Ideally MOCVD can deposit faster than MBE but the

issues are the use of toxic gases, production of toxic by-products, community safety and environmental impact which become the main drawbacks of this technique.

CBD is a deposition of thin film started by the nucleation within the chemical bath followed by particle growth on the substrate based on the formation of a solid phase from a solution. It can be employed for large-area batch processing or continuous deposition. The growth of thin films strongly depends on growth conditions, such as duration of deposition, composition of the bath, temperature of the solution, and topographical and chemical nature of the substrate. Although CBD technique is a simple method, it produces stable and uniform thin films, but there is wastage of solution after every deposition [72]. This is an expensive step, especially when element like toxic Cd is involved in the case of depositing CdS.

Electrodeposition is a chemical deposition in the presence of electricity, electrolyte, cathode and anode. The deposition is initiated by the applied electric field through the cathode and anode. When the electrons flow from the power supply to the cathode, the positively charged cations are attracted to the cathode, reduced and neutralised electrically by receiving electrons and getting deposited on the cathode [81]. The deposition is controlled by monitoring the amount and the rate of charge passing through the electrolyte. The electrodeposition method is simple, low cost, enables deposition of large area films and provides easier control of growth parameters. It also offers a continuous industrial process drastically reducing toxic waste generation compared to batch process of CBD since the electrolyte can be used over a long period of time [7].

Due to the excellent advantages of electrodeposition along with the aim to produce low cost solar cell devices, all the materials used in this research work are prepared by electrodeposition technique. This technique has been discussed further in Section 2.3.2.

2.3.2 Electrodeposition

Electrodeposition is the process that uses electric current to form electrochemical reaction at the electrolyte/electrode interface to create the solid materials on the conducting substrate. As mentioned previously, this technique requires simple and basic apparatus such as power supply, anode, cathode and electrolyte. The illustration of electrodeposition set-up can be seen in Figure 2.15. The electrode connected to the positive terminal is known as anode while the electrode connected to the negative terminal is known as cathode. Electrodeposition can be formed either in anodic or

cathodic. In cathodic deposition, positively charged ions are attracted, form reduction by accepting one or more electrons and attach themselves to the conductive substrate to form a solid thin film while in anodic deposition, the negatively charged ions are attracted, form oxidation by donating one or more electrons and deposited onto conductive substrate attached to the anode electrode. Cathodic deposition is more commonly used in inorganic electrodeposition since it provides less defective layers with better stoichiometry and adhesion [82]. However, anodic deposition is also common in polymer material growth since it offers better polymerisation and excellent quality of layers [83].

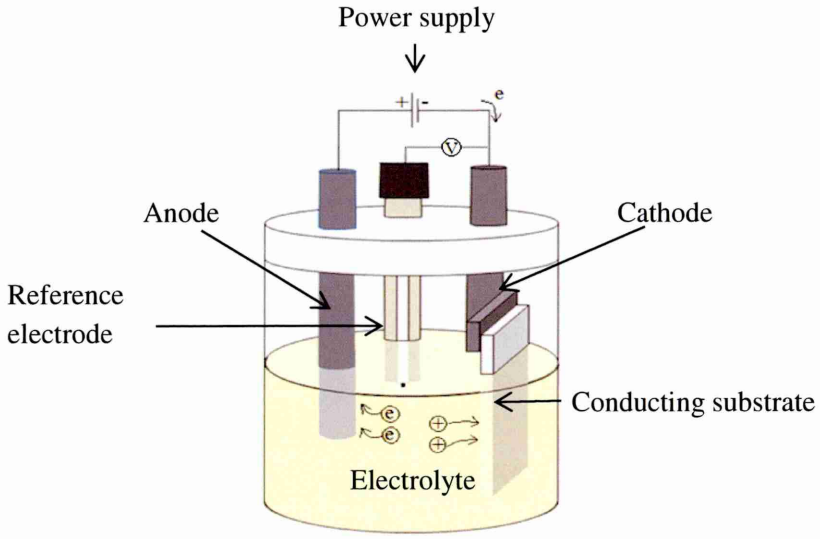

Figure 2.15: The electrodeposition experiment set-up of cathodic deposition.

The morphology and composition of the electrodeposited thin film is dependent on the current density, presence of the impurities, the nature of anions or cations in the solution, potential supply which associated to the growth voltage, V_g, physical and chemical nature of the conductive substrate, electrolyte temperature, pH, stirring rate and electrolyte concentrations [81]. The relationship between the weight of the deposited material and the various electrodeposition parameters can be governed by Faraday's Law of Electrolysis. These laws were discovered in 1843 by Michael Faraday which states that the weight of a substance formed at an electrode is proportional to the amount of charge passed through the cell [71]. This can be summarised as:

$$m = \left(\frac{Q}{F}\right)\left(\frac{M}{z}\right) \qquad (2.5)$$

where m is the mass of a substance formed on an electrode, Q is the total electric charge passed through the cell, F *is* the Faraday constant (F= 96,485 $Cmol^{-1}$), M is the molar mass of the substance and z is the valence number of ions.

The theoretical thickness of the deposited films can also be calculated by Faraday's equation which is:

$$T = \frac{1}{nFA}\left(\frac{itM}{\rho}\right) \tag{2.6}$$

where T is the thickness, F *is* the Faraday constant (F= 96,485 $Cmol^{-1}$), A is the area, i is the average current, t is the time, M is the molar mass of the substance and ρ is the density of the deposited material. This relation can only be used for specific compound such as CdS and CdTe with known n value.

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Chapter 3 - Experimental methods

3.0 Introduction

This chapter discusses the fundamental of the instruments and experimental approach in the research programme. The work has been divided into five main parts, which are substrate preparation, electrodeposition (ED) of thin films, characterisation of thin films, fabrication and development of solar cell devices and characterisation of solar cell devices. The summary of this is illustrated in the flowchart in Figure 3.1.

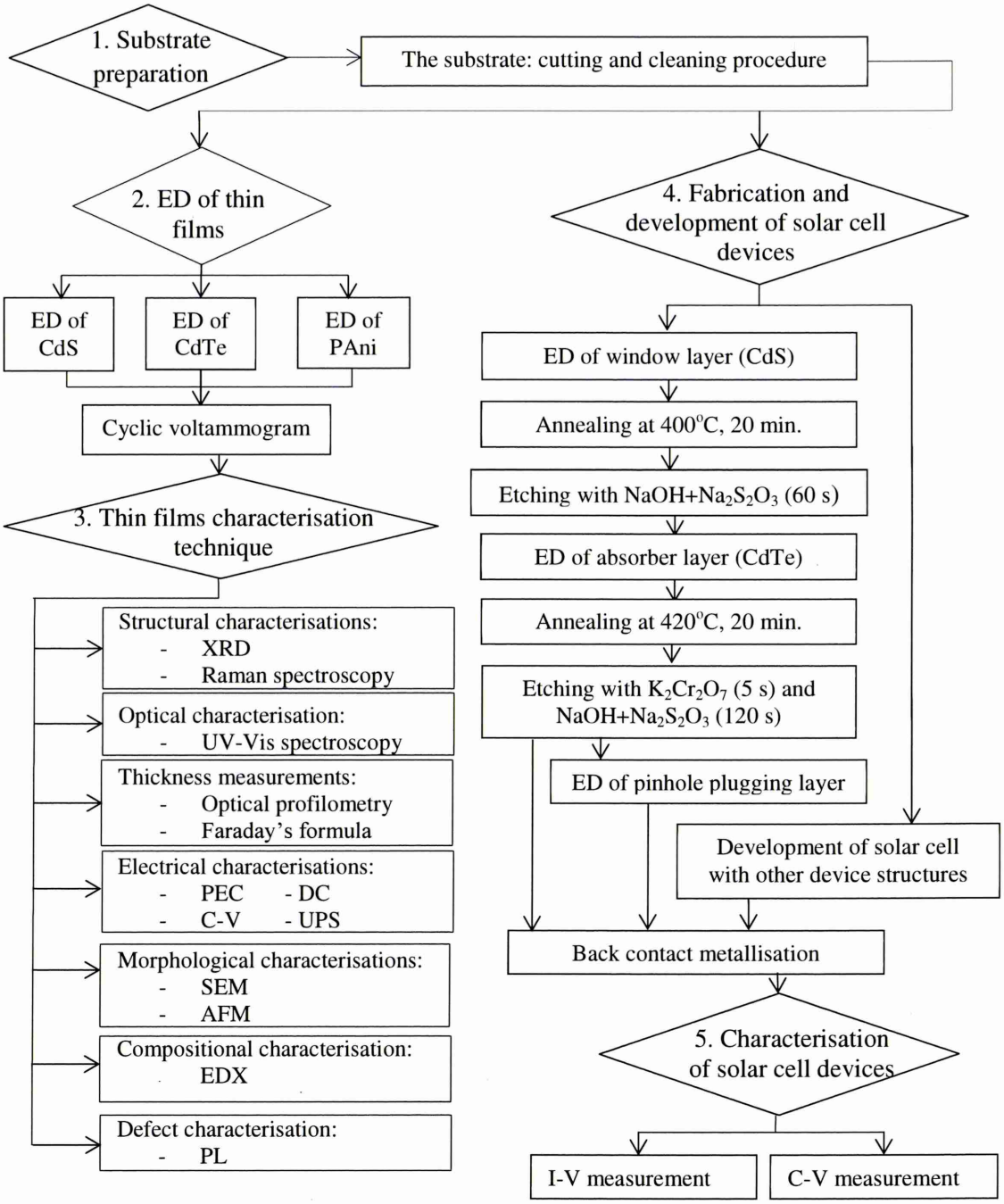

Figure 3.1: Flow chart of the experimental work in the research project.

3.1 Substrate preparation

Substrate preparation is a typical procedure for any device fabrication. This process should not be ignored since it also affects solar cell performance. The preparation processes include substrate selecting, substrate cutting and cleaning. These substrates should be prepared appropriately before any experiment in order to obtain a good thin film layer formation.

3.1.1 The substrate: Cutting and cleaning procedure

The substrate is a one of the important components of a solar cell device. It should withstand high temperature, transparent, and have high optical transmittance and low resistivity. Transparent conductive oxide (TCO) coated glass is the best choice to fit this requirement since it is an n^+ conductive oxide with a very high bandgap (>3.80 eV) [1]. Fluorine-doped tin oxide (FTO) and indium-doped tin oxide (ITO) are the most widely used materials for TCO coating on glass. FTO has a slightly misty-blue appearance, while ITO has a good transparency and transmits light better. However, the cost of ITO-coated glass is extremely high, even for the high sheet resistance substrate [2]. Therefore, in this work we chose FTO-coated glass as the substrate, since it has lower resistivity, is cheaper and stable under high temperatures. FTO-coated glass with a sheet resistance of 7 Ω/□ was purchased from Sigma-Aldrich.

The substrate was cut to a desired dimension with a diamond glass cutter. The cleaning procedure started with arranging the FTO-coated glass substrates face up inside a beaker that contains a soap and water. The beaker was then placed in the ultrasonic bath and agitated for 10 minutes. Then the substrates were rinsed with deionised water before being immersed in acetone solution to remove grease and organic residues. These substrates were then rinsed again in deionised water and dipped in methanol solution to eliminate the tough grease. Some of the researchers further washed the substrate in solvents such as isopropanol to remove residues, but these cleaning methods are optional [3]. The substrates were finally rinsed in deionised water and dried with a nitrogen gas flow before electrodeposition.

3.2 Electrochemical deposition (ED) of thin films

All of the thin films in this work have been produced using the electrochemical deposition technique. The theoretical background on electrodeposition has been mentioned in Section 2.3.2. A typical electrodeposition setup requires an electrolyte

containing appropriate ions, electrodes, a beaker, a hot plate with magnetic stirrer, a magnetic stirrer bar and a computerised potentiometer. This section describes the electrodeposition process of the three main materials used in this research, which are cadmium sulphide (CdS), cadmium telluride (CdTe) and polyaniline (PAni).

3.2.1 Electrodeposition of cadmium sulphide (CdS)

The electrolyte for the CdS electrodeposition was prepared with 0.30M of hydrated cadmium chloride ($CdCl_2 \cdot xH_2O$) and 0.03M ammonium thiosulphate $(NH_4)_2S_2O_3$ (analytical reagent grade), both with a purity of 98% in 500 ml of deionised water. The $CdCl_2$ aqueous solution was electropurified for 100 hours before the experiment started to eliminate any metallic ions present in the chemical precursor, since $CdCl_2 \cdot xH_2O$ has a low purity (~98%). In this work, $(NH_4)_2S_2O_3$ was used as the sulphur precursor instead of the typical sodium thiosulphate, $Na_2S_2O_3$, for the reason which has been discussed in Section 2.1.4.1. The $(NH_4)_2S_2O_3$ required stirring for 2 hours before it fully dissolved in the water.

The pH of the electrolyte should be in acidic region (usually pH<2.50) for better conductivity and quality of adhesion. However the too high acidic electrolyte can caused a dissolution of the previous or buffer layer and result in poor quality of electrodeposited layer while the too low acidic caused poor conductivity and slow deposition rate. Therefore in this work the pH measured at room temperature and maintained at 2.00±0.02, and diluted solutions of hydrochloric acid (HCl) and ammonium hydroxide (NH_4OH) were used to adjust the pH at the start of the deposition. The ED of the CdS thin film was done at a temperature of 85±2°C using a hot water bath technique. A hot water bath is a heating technique in which a plastic beaker of electrolyte is placed in a glass beaker of hot deionised water. The glass beaker is placed on a hot plate and the deionised water surrounds the electrolyte with uniform heating [4].

A simple two-electrode system with a high-purity graphite rod as an anode and FTO-coated glass substrate as a working electrode (cathode) was used for this study. Before the addition of $(NH_4)_2S_2O_3$, cyclic voltammogram was carried out on the aqueous solution containing only $CdCl_2$ and the aqueous solution containing only $(NH_4)_2S_2O_3$, at a pH of 2.00±0.02 and a temperature of 85±2°C for both. Cyclic voltammogram was also carried out on a mixture of $CdCl_2$ and $(NH_4)_2S_2O_3$ at a pH of 2.00±0.02 and a temperature of 85±2°C. The purpose of cyclic voltammogram study is to estimate the approximate voltage range for film deposition. Using the voltage range

estimated, CdS thin films were grown at different growth voltages (V_g), and the growth conditions were optimised after thin film characterisations. The overall reaction for the formation of the CdS thin film at the cathode can be described as follows [5, 6]:

$$\text{Overall reaction: } 2Cd^{2+} + S_2O_3^{2-} + 6H^+ + 8e^- \rightarrow 2CdS + 3H_2O \qquad (3.1)$$

During deposition, a deficiency of $(NH_4)_2S_2O_3$ in the CdS electrolyte may produce a cadmium-rich deposited film, while an excess of it may slow down the deposition rate [7]. Therefore, it is suggested to add the $(NH_4)_2S_2O_3$ continuously in appropriate concentrations to produce good quality thin films.

3.2.2 Electrodeposition of cadmium telluride (CdTe)

A three-electrode system with high-purity graphite rod as anode, saturated calomel electrode (SCE) as reference electrode and FTO coated glass substrate as working electrode were used for this study. The deposition temperature of 65±2°C was used to avoid detrimental effects on the SCE reference electrode due to its 70°C upper temperature limit.

A conventional Cd source in the CdTe deposition electrolyte is prepared from $CdSO_4$. However, in this work, the Cd source was prepared from $CdCl_2$ for many reasons, which have been discussed in Section 2.1.4.2. Initially, 1.00M of hydrated cadmium chloride ($CdCl_2 \cdot H_2O$) with a purity of 99.99% was dissolved in 800 ml deionised water. The solution was electropurified by applying a cathodic potential just below the required potential for reducing Cd^{2+} for ~100 hours, before any cyclic voltammetric study. Cyclic voltammogram was then recorded on the aqueous solution containing only $CdCl_2$ at the pH of 2.00±0.02 and temperature of 65±2°C.

The initial Te precursor was prepared by adding 1 g of 99.999% (5N) TeO_2 powder to concentrated hydrochloric acid (HCl) and continuously stirred for 24 hours. The TeO_2 acidic solution was then diluted with deionised water and pH value was adjusted to 2.00±0.02 using either HCl or NH_4OH, and again the cyclic voltammogram for the aqueous solution containing only TeO_2 was recorded at temperature of 65±2°C.

About 1 ml of the prepared TeO_2 solution was then added to 800 ml aqueous solution containing purified 1.00M $CdCl_2 \cdot H_2O$. The pH of the resulting deposition electrolyte was adjusted to 2.00±0.02. Finally the cyclic voltammogram of aqueous solution containing $CdCl_2$ and TeO_2 was carried out at a pH of 2.00±0.02 and

temperature of 65±2°C to identify the approximate range of deposition potentials for CdTe at ~65°C. The electrodeposition of CdTe in the acidic bath involved the reduction of $HTeO_2^+$ to Te, which in turn reacted with Cd^{2+} to produce CdTe. The reactions for the CdTe thin film formation at the cathode are described in equation (3.2) to (3.4) [7, 8]:

$$1^{st} \text{ reaction: } HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \quad (3.2)$$

$$2^{nd} \text{ reaction: } Cd^{2+} + Te + 2e^- \rightarrow CdTe \quad (3.3)$$

$$\text{Overall reaction: } HTeO_2^+ + Cd^{2+} + 3H^+ + 6e^- \rightarrow CdTe + 2H_2O \quad (3.4)$$

3.2.3 Electrodeposition of polyaniline (PAni)

A fresh aniline solution was prepared with a 0.10M concentration by dissolving aniline in deionised water. The solution was stirred for 15 minutes and the pH value was adjusted to ~2.20±0.02 using H_2SO_4 and NH_4OH. The attempt on deposition of polyaniline thin films in this work was carried out by cathodic and anodic depositions. As for anodic deposition, the working electrode (glass/FTO) was connected to anode and a high-purity graphite rod was connected to cathode whereas in the cathodic deposition, a working electrode (glass/FTO) was connected to the cathode and a high-purity graphite rod was functioning as an anode [9,10]. The cyclic voltammogram for each cathodic and anodic deposition study was carried out at potential between −100 mV and 2000 mV using a computerised Gill AC potentiostat (ACM instruments).

3.2.4 Cyclic voltammogram

Cyclic voltammogram is a technique used to study the electrochemical reaction of the electrodeposition process by monitoring the electric current through the electrolyte as a function of potential sweep. It is a practical method for providing qualitative information about electrode reactions and determining quantitative properties of the charge transfer reaction [11].

Cyclic voltammogram is performed by scanning the potential of a working electrode in forward and reverse direction and measuring the resulting current. The experimental setup requires a potentiostat and a data recorder system. Initially the generator modulates the output of the potentiometer in order to apply a cyclic linear ramp with desirable slope and modulate the working electrode potential between two voltage limits. A potentiometer generally has two outputs proportional to the working

electrode potential and cell current that are fed to the X and Y inputs of the data recorder system.

In this work, cyclic voltammogram is used to identify the regions where the deposition of thin film material takes place. Using the voltage range estimated, thin films were grown at different growth voltages and the growth conditions were optimised after characterisation. The forward scan gradually increases the cathodic potential while the reverse scan starts in opposite direction. It is important to note that some analyses undergo oxidation first, in which case the potential would first scan positively. The cycle can be repeated and the scan rate can be varied.

3.3 Thin films characterisation techniques

The properties of the electrodeposited materials should be studied systematically through several characterisation techniques in order to understand the structural, optical, electrical, morphological, compositional and thickness properties of these materials. This section, therefore, comprehensively discusses the characterisation techniques used in this research work.

3.3.1 Structural characterisation

The structural properties of electrodeposited thin films have been analysed by two different instruments which are X-ray diffraction (XRD) and Raman spectroscopy. This section clarifies in detail the functional principles and basics of operation of both these instruments.

3.3.1.1 X-ray diffraction (XRD)

X-ray diffraction (XRD) is a technique used to identify the crystalline phases present in materials and to measure the structural properties, including grain size, lattice parameters, atomic spacing, phase composition and preferred orientation of these phases. It is a non-contact and non-destructive characterisation method [12]. XRD was first observed in practice by Max Von Laue in 1912; he won the Nobel Prize in Physics in 1914 [13].

The principle of XRD is based on constructive interference from X-rays scattered by the atomic planes in a crystal. The condition for constructive interference from planes with inter-atomic distance d is given by Bragg's law in equation (3.5).

$$n\lambda = 2d \sin\theta \qquad (3.5)$$

A crystal lattice is a three-dimensional distribution of atoms, which are arranged to form a series of parallel planes separated from one another by a distance, *d*. When a monochromatic X-ray beam with wavelength λ is projected onto a crystalline material at an angle θ, diffraction occurs as beams are reflected from successive planes which differ by a whole number *n* of wavelengths. For diffraction to be observed, the detector must be positioned accordingly, the crystal must be oriented and the angle between the diffracting plane and the incident X-ray must be equal to Bragg's angle. The conditions for maximum intensity contained in Bragg's law allow us to calculate details about the crystalline structure.

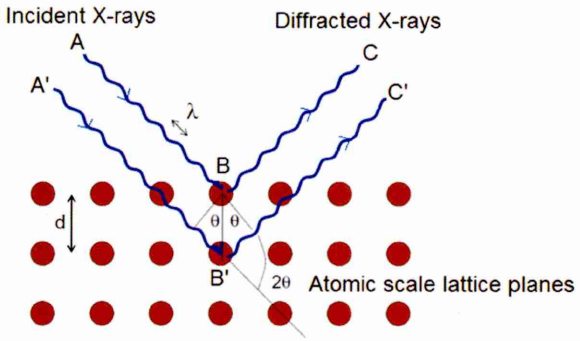

Figure 3.2: Schematic of Bragg's law reflection. The diffracted X-rays exhibit constructive interference when the path difference between the two rays differs by an integer number of wavelengths.

The basic XRD setup is outlined in Figure 3.3. It consists of three main parts, which are X-ray source, sample holder and X-ray detector. X-rays are produced by converting electrical energy into an electromagnetic waves. This is done in a cathode-ray tube by accelerating electrons from an electrically negative cathode towards a positive target anode. When electrons have sufficient energy to displace inner shell electrons of the target material, characteristic X-ray spectra are produced. X-ray spectra consist of several components, subject to different kinds of transition energies, commonly labelled as K_α and K_β. The specific wavelengths are characteristic of the target material such as Cu, Fe, Mo or Cr. X-rays are collimated and directed onto the sample. As the detector is rotated, the intensity of the reflected X-rays is recorded. When the geometry of the incident X-rays impinging on the sample satisfies the Bragg equation, constructive interference occurs and a peak in intensity occurs. A detector

records and processes this X-ray signal and converts the signal to a count rate, which is then output to a device such as a printer or computer monitor.

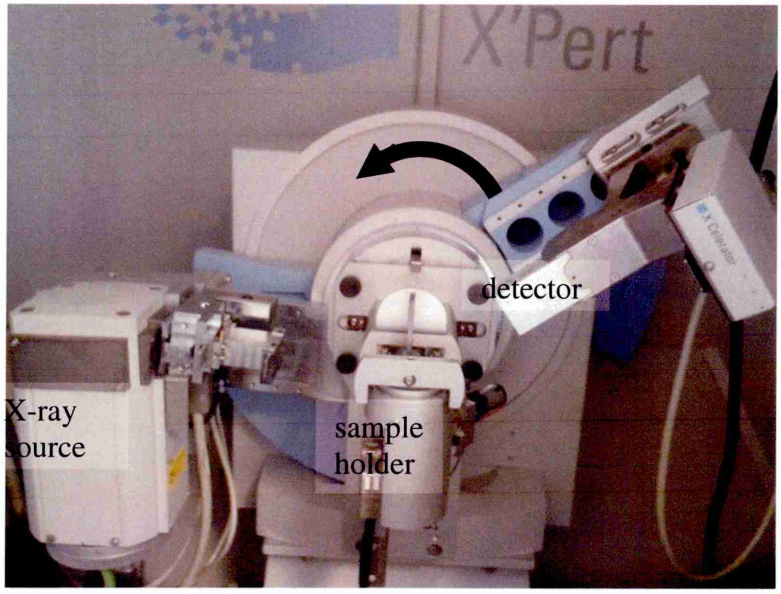

Figure 3.3: XRD instrument used in this study (Panalytical X'Pert) showing the three main components.

In this measurement, the range of angles is 2θ=20-70^{o} and and type of sample is thin film. The XRD pattern is produced by plotting the intensity as a function of angular positions. The crystallite size, D, can be calculated using Scherer's formula:

$$D = \frac{0.94\,\lambda}{\beta \cos\theta} \qquad (3.6)$$

where λ is the wavelength of the X-ray used (1.541 Å), β is the full width at half maximum (FWHM) of the diffraction peak in radians, and θ is the Bragg angle. Conversion of the diffraction peaks to d-spacing allows identification of the materials because each material has a set of unique d-spacings. Typically, this is achieved by comparing d-spacing with standard reference patterns.

3.3.1.2 Raman spectroscopy

Raman spectroscopy is a very convenient technique to observe vibration, rotation and other low-frequency modes in materials and hence identifying elements and compounds. This technique is based on inelastic scattering of monochromatic radiation. Elastic light scattering has been observed since the 19th century by famous physicists such as Albert Einstein and Lord Rayleigh. However, no inelastic scattering had been

observed experimentally, even though the effect had been predicted theoretically by A. Smekal in 1923 [14]. The first experimental observation of inelastic light scattering by molecules in liquid phase was discovered by the Indian scientist Sir Chandrasekhara Venkata Raman and his student Kariamanickam Srinivasa Krishnan in 1928 [15]. Two years later, Sir Chandrasekhara Venkata Raman received the Nobel Prize in Physics and the Raman Effect carries his name ever since.

Raman spectroscopy relies on the inelastic scattering of photons from matter. This inelastic scattering is observed as a shift in the frequency of the scattered light relative to the excitation wavelength. When the excitation laser beam is directed onto the sample, the electric field of the laser distorts the electron clouds that make up the chemical bonds in the sample and store some energy. As soon as the electric field reverses, distorted electron clouds relax and stored energy is reradiated. The scattered beam reradiates in all directions. Most of the stored energy reradiates at the same frequency as the excitation laser beam, which means that the excited photon returns to the same energy state (Illustrated in Figure 3.4). This is known as Rayleigh scattering. However, a small portion of the stored energy is transferred to the sample itself, exciting the vibrational energy. This is an inelastic scattering event, where the energy of the scattered photon is different from the incident photon by one vibration unit. The vibrational energy that is deducted from incident photon energy is called Raman scattering. Fundamentally, only one in 10^6 to 10^8 photons scattered undergo Raman scattering. The reverse process also occurs, where existing vibration is annihilated by a thermal process and the photon energy is enhanced. The vibrational energy that is enlarged from the incident photon energy is called anti-Stokes scattering. The diagram of the Rayleigh, Raman and anti-Stokes scattering is shown in Figure 3. 4.

The schematic diagram of the Raman spectroscopy system is shown in Figure 3.5. The four main components of the system are the laser source, optical components such as lens and mirrors, a spectrometry and detector. The excitation laser is directed into the sample by an array of mirrors. The power of the excitation laser is controlled by a set of neutral density filters. Scattered light is collected and fed back into the spectrometry and passed through a notch filter to remove the intense Rayleigh-scattered radiation, allow the weaker Raman-scattered light. The Raman-scattered light is focused by a set of focusing optics before diffraction grating separates the different wavelengths. The different wavelengths are finally detected by a charged-coupled device (CCD) camera, which is connected to a PC running Raman software.

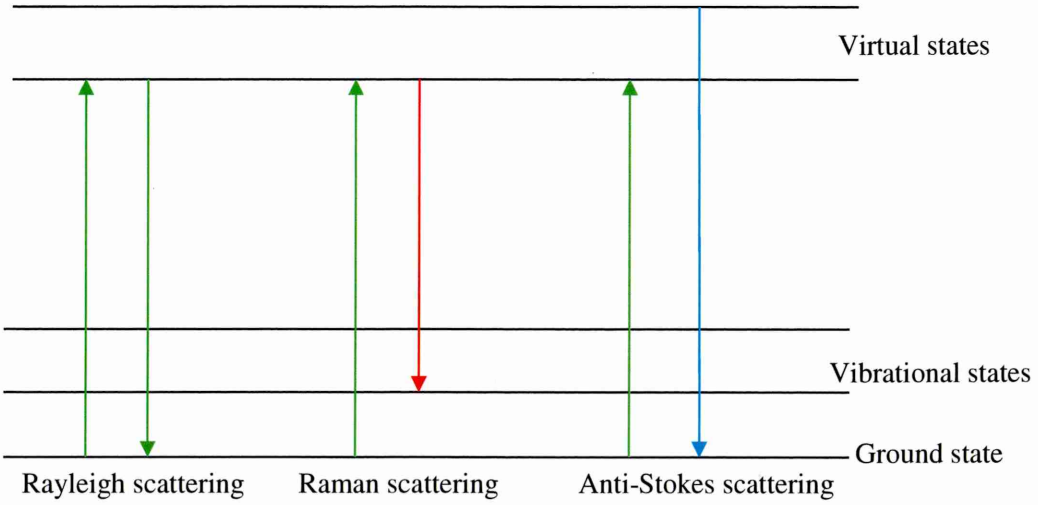

Figure 3.4: Diagram of the Rayleigh and Raman scattering processes. Note that both the low energy (upward arrows) and the scattered energy (downward arrows) have much larger energies than the energy of a vibration does.

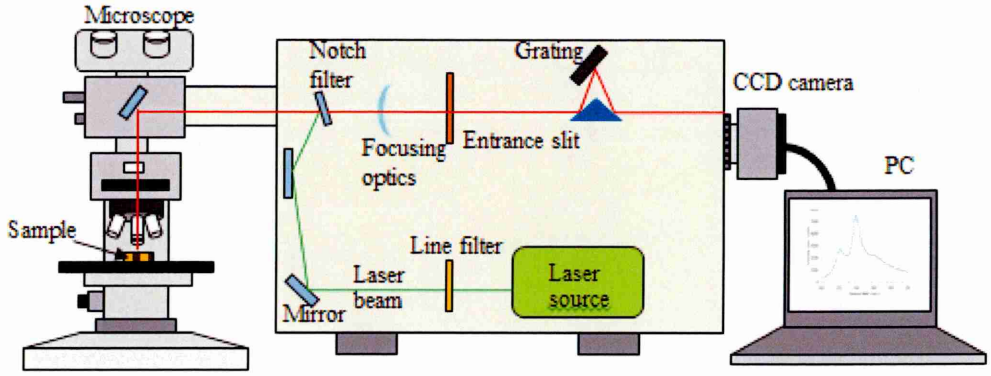

Figure 3.5: Schematic diagram of the Raman spectrometry.

The Raman spectrometry setup used in this work is Renishaw's Raman microscope. The excitation laser used is an Argon ion laser with 514.0 nm wavelength. The Raman spectrum provides good information and can be used as a fingerprint for the identification of unknown materials by directly comparing the spectrum with the spectra in a reference library.

3.3.2 Optical characterisation

Optical properties are one of the important parameters in developing a solar cell device. The role of electrodeposited CdS as a window layer demands high transmittance, low absorbance and low reflectance in order to transmit photons through the active junction region and absorber layer. Unlike CdS, CdTe required a higher absorbance to fully

absorb the light. The optical characterisation of each electrodeposited material is studied under UV-visible spectroscopy. This includes the absorbance, transmittance and reflectance properties. The details of instrument, concept, operation and analysis in this research work are described below in details.

3.3.2.1 UV-Vis spectroscopy

When light is directed at a material, some of it will be absorbed and reflected and the remaining part will be transmitted through the material. UV-visible spectroscopy is an instrument used to study optical properties, which includes the absorption, reflectance and transmittance of the material at electromagnetic spectrum range from UV (~200–400 nm) to visible light (~400–700 nm).

UV-visible spectroscopy consists of six main parts, which are a light source, collimator, monochromator, slit, sample holder and detector. The basic setup of this instrument is illustrated in Figure 3.6. The scan rate, slit width and resolution are 10 $nm \cdot s^{-1}$, 1.5 nm and <1.5 nm, respectively. Initially, the emitted white light is produced from a light source and directed through the collimator lens and monochromator. The output wavelength of the monochromator can be tuned by rotating the prism. The slit then transmits a desired wavelength directed onto the sample. The light that passes through the sample is then detected by the photocell in the detector before passing the signal to the software for analysis. Absorbance, transmittance and reflectance mode can be selected through the software.

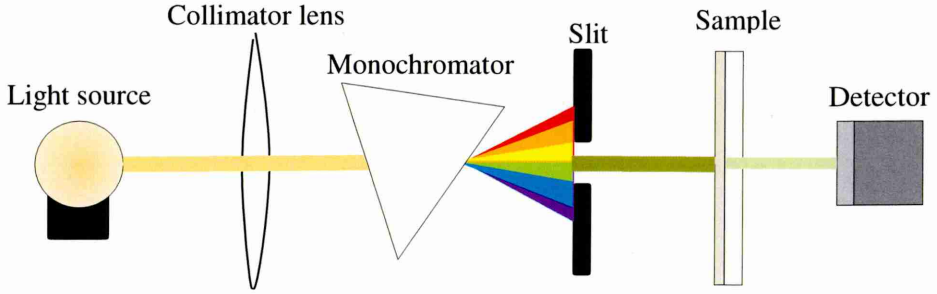

Figure 3.6: Schematic diagram showing main components of UV-Vis spectrometry.

All optical measurements reported in this thesis were carried out using the Cary 50 Scan UV-Vis Spectrophotometer. The optical absorption measurement is carried out to estimate the energy bandgap, E_g, of the electrodeposited materials. The E_g value can be derived from a mathematical treatment of data obtained from this measurement with the Stern relation for near-edge absorption data:

$$\alpha = \frac{C(hv - E_g)^{\frac{n}{2}}}{hv} \tag{3.7}$$

Where α is the absorption coefficient, C is a constant of proportionality, which depends on the material, h is Planck's constant, E_g is the energy bandgap and v is the frequency of light. In this work, the graph of $(\alpha hv)^2$ versus hv is used to obtain E_g by extrapolating the straight line portion of the graph to the hv axis. In the above equation, n=1 for direct bandgap materials.

The absorption coefficient is also related to the transmittance of the material and thickness according to equation 3.8

$$\alpha = \frac{\ln T}{d} \tag{3.8}$$

Where T is transmittance and d is thickness. Transmittance is the ratio of the intensity of the light transmitted from the sample, I, to the intensity of the incident light on the sample, I_o. This can be expressed as:

$$T = \frac{I}{I_o} \tag{3.9}$$

The transmittance value can be analysed directly from a graph of transmittance versus wavelength.

3.3.3 Thickness measurements

Thin film is a sheet of material with thicknesses ranging from a few nanometres up to several micrometres. This extremely thin layer requires a powerful instrument to measure it accurately. In this work, the thickness of electrodeposited thin film has been measured using an optical profilometer. A theoretical calculation using the Faraday's law equation has also been used to compare the results obtained from the optical profilometry measurement. This section will discuss this instrument and calculation further.

3.3.3.1 Optical profilometry

Optical profilometry is the most common method used to characterise the surface features and thin film thickness without contact. In this work, optical profilometry has been used to determine the thickness of the thin films by measuring the difference in surface height between the substrate and the coated thin film on the substrate. Since it is a non-contact method, the surface of the sample cannot be damaged during the measurement.

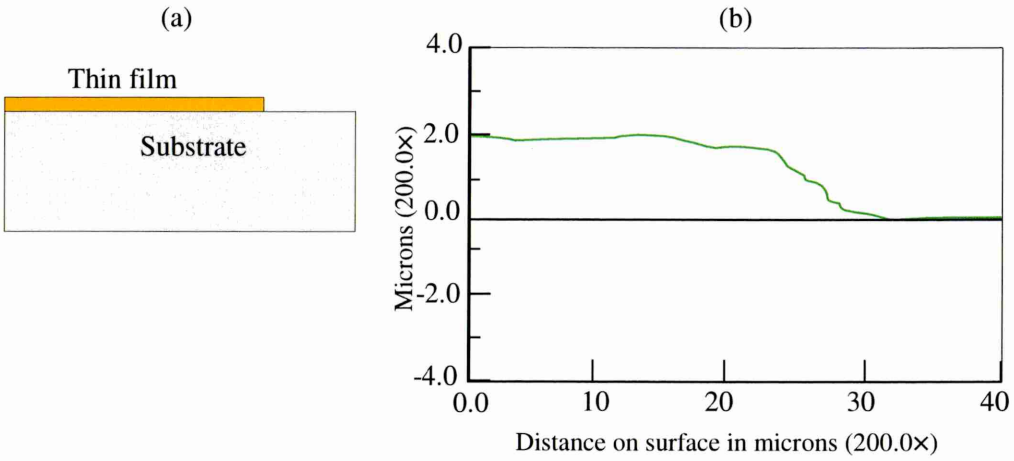

Figure 3.7: The schematic diagrams of (a) a layer of thin film coated on substrate and (b) the optical profilometry trace of a region on the thin film and substrate.

The process of optical profilometry involves scanning the surface with an optical probe, which transmit the light interference signal back to the profilometry detector through an optical fibre [16]. The optical profilometer used in this research is a UBM optical profilometer. In this method, light reflected from the surface of interest interferes with the light from an optically flat reference surface. The variation in fringe shape that is produced by the interference is related to the difference in surface height. This variation can be measured by moving the interferometer probe over the area of interest on the sample. A tracing of the surface is typically digitised and stored in a computer for display. Figure 3.7 shows a typical optical profiler trace of a region on a thin film edge. It displays the result for the thin film thickness, which is about 2.0 μm. In standard measurements, the surface has a variation of about 0.2 μm, but in some cases the difference can exceed 1 μm. Therefore, due to the lack of precision, this measurement should be done several times in order to get the average value for the final data.

3.3.3.2 Faraday's law equation

Faraday's law equation is another technique to estimate the thickness of electrodeposited thin films. This calculation is more accurate than the optical profilometry measurement in estimating the thickness, since it regards every aspect in the thin film ED process by relating all the parameters between current, time and the mass of electroplated material. Michael Faraday was an English scientist who conducted research in the areas of chemistry, electricity and magnetism. He published the electrochemical principles that refer to Faraday's laws of electrolysis in 1834 [17].

One of the Faraday's law states that the mass of material change at an electrode is directly proportional to the quantity of electrical charge that transfers to the electrode and the element's equivalent weight of the material (molar mass), divided by the change in oxidation state it goes through during the ED [18]. Mathematically, Faraday's law can be expressed as:

$$\text{Thickness} = \frac{1}{n\,F\,A} \times \frac{i\,t\,M}{\rho} \qquad (3.10)$$

Where n is the number of electrons in the chemical reaction of the electrolyte, F is a Faraday's constant, A is the electrodeposited area of the thin film, i is the average electrical current during growth, t is the deposition time, M is molar mass of the material and ρ is the density of electrodeposited film.

The thickness of almost all of the thin film prepared by the ED can be calculated with Faraday's law equation. The one weakness of this calculation is that it is only valid for as-deposited thin film. Once the film has been annealed or treated with other chemicals, the quantity of the material is altered and consequently the thickness is also changed. Therefore, this calculation is not valid for annealed and treated samples.

3.3.4 Electrical characterisation

Electrical properties of semiconductors play an important role in solar cell fabrication because the performance of the devices relies on the conduction mechanism. Information on conductivity type of semiconductor, electrical conductivity and doping concentration are essential in deciding on the type of junction and designing the device structure. This section therefore presents the conventional instruments used in measuring the electrical properties. These are photoelectrochemical (PEC) cell measurement, direct current (DC) conductivity measurement and capacitance-voltage

(C-V) measurement. The principles and procedures of these measurements are discussed in detail below.

3.3.4.1 Photoelectrochemical (PEC) cell characterisation

PEC cell measurement is a simple technique for determining the electrical conductivity type of a semiconductor. It is based on the effect of semiconductor-electrolyte interfaces under illumination and dark conditions.

In general, the Fermi level of a semiconductor and the electrolyte energy level are different. When a semiconductor is immersed in the electrolyte, electronic charge initially flows across the junction until electronic equilibrium is reached and Fermi level of the electrons in the solid is equal to the redox potential of the electrolyte, as shown in the Figure 3.8. On the semiconductor side near the interface, the energy band, bend either upwards or downwards, depending on the position of the Fermi level in the solid [19]. Upon illumination, the shift occurs generally towards the initial value, thus the band bending decreases. The potential change is equivalent to the shift of the bulk Fermi level ${}^{*}E_F$ with respect to the E_F. This can be simply represented as [20]:

$$\Delta E = \frac{1}{e}\left|{}^{*}E_F - E_F\right| = E_{illumination} - E_{dark} \qquad (3.11)$$

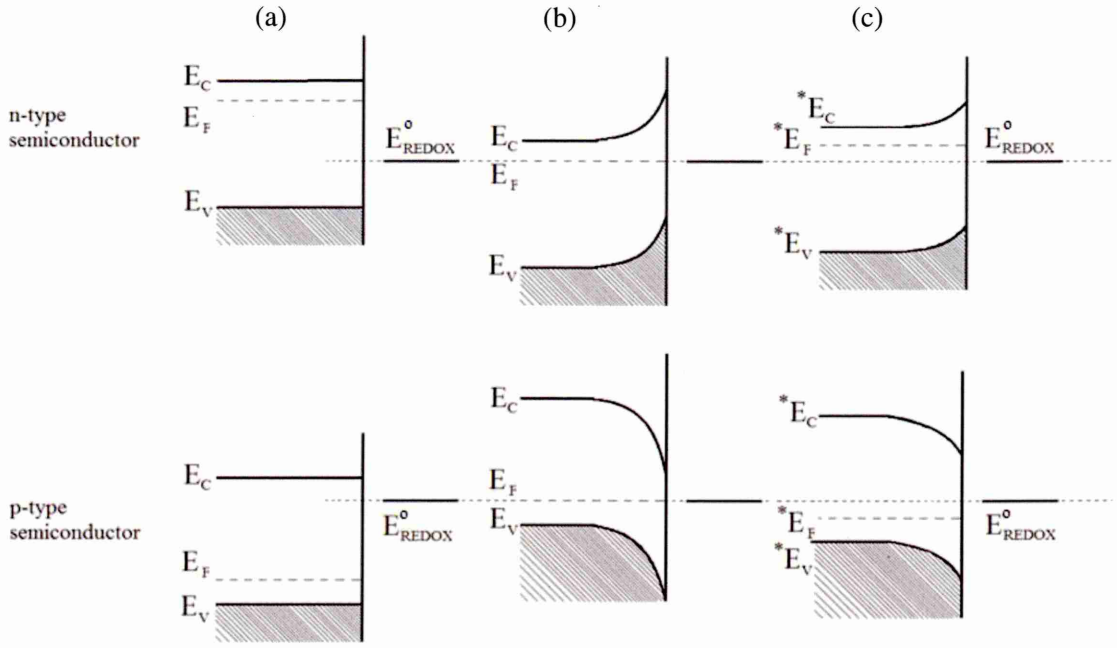

Figure 3.8: The interface between bulk semiconductor and electrolyte (a) before equilibrium with the electrolyte, (b) after equilibrium with the electrolyte in the dark, and (c) after illumination.

In this work, PEC cell characterisation has been measured in electrolyte of 0.1M $Na_2S_2O_3$. The experimental setup of the PEC cell measurement is shown in Figure 3.9. Working and counter electrodes are connected to a digital voltmeter, DVM, and placed in a suitable electrolyte to form a solid/liquid junction. Once connected, the voltages between the two electrodes are measured under both dark and illuminated conditions. The difference between these two voltage values gives the open circuit voltage of the liquid/solid junction or the PEC signal. The sign of the PEC signal determines the conductivity type of the semiconducting layer, and the magnitude of the signal indicates the level of doping concentration. A zero PEC signal is produced for metallic and insulating layers.

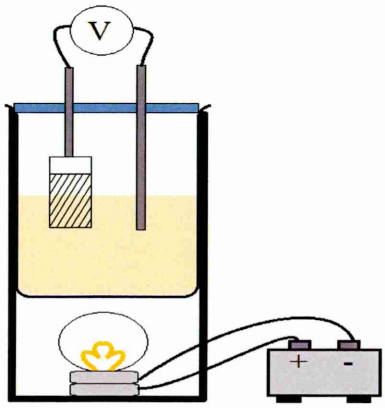

Figure 3.9: The schematic diagram of the PEC measurement system.

3.3.4.2 Direct current (DC) conductivity measurement

The DC conductivity measurement is a typical measurement for the study of electrical conductivity (σ) and resistivity (ρ) in semiconductor materials. The principle of this measurement is based on Ohm's law, which relates to voltage and current in an ideal state.

The DC conductivity measurements in this work have been carried out using a Keithley 619 Multimeter. Before the measurement, a semiconductor sample should be prepared with appropriate metal contacts depending on the conductivity type of the sample to form ohmic contacts. The measurement procedure is quite simple by varying DC voltages that are connected to the two contacts across the sample and recording the DC current flowing through the material. The circuit diagram for this measurement is shown in Figure 3.10.

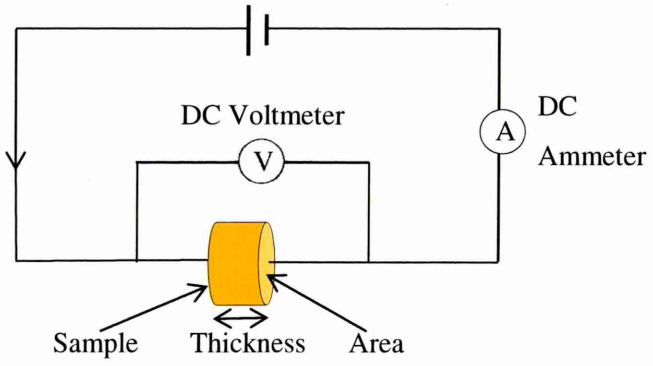

Figure 3.10: Schematic of circuit used in DC conductivity measurement.

The value of resistance, R, of the semiconductor material between the two electrodes can be determined directly from the slope of the current versus voltage graph.

The resistivity and conductivity of the semiconductor can be calculated by using equation (3.13) and (3.14), respectively.

$$R = \frac{\Delta V}{\Delta i} = \rho \frac{L}{A} \tag{3.12}$$

Where, in this case, L is a thickness of the semiconductor thin film and A is the area. Therefore,

$$\rho = \frac{RA}{L} \tag{3.13}$$

and

$$\sigma = \frac{1}{\rho} \tag{3.14}$$

3.3.4.3 Capacitance-Voltage (C-V) measurement

C-V measurement is a typical technique for measuring a variety of electrical properties of semiconductor materials and semiconductor devices. In semiconductor material characterisation, it can be used to determine the conductivity type, doping concentration and indirect estimation of mobility of charge carriers, whereas in solar cell device characterisation, this measurement is used to determine the depletion width, diffusion voltage and Fermi level in the bandgap. Further details on solar device measurement will be discussed in section 3.5.2.

Capacitance of a junction can be determined from the variables in the following equation:

$$C = \frac{A\kappa}{d} = \sqrt{\frac{q\varepsilon_s N_D}{2}}\,(V + V_d) \tag{3.15}$$

where A is the area of the capacitor, κ is the dielectric constant of the semiconductor sample, d is the thickness, q is a charge carrier, ε_s is a semiconductor permittivity and N_D is doping concentration. Also, the equation (3.16) can be derived from the above equation.

$$\frac{1}{C^2} = \frac{2}{\varepsilon_s q A^2 N_D}(V + V_d) \quad (3.16)$$

The procedure for taking C-V measurements involves the application of DC bias voltages across the capacitor (junction) while making the measurements with an AC signal [21]. The bias is applied as a DC voltage sweep. As bias voltage is decreased, majority carriers get pushed away from the oxide interface, and the depletion region forms. When the bias voltage is reversed, charge carriers move the greatest distance from the oxide layer, and capacitance is at a minimum. From this inversion region capacitance, the number of majority carriers can be derived.

A Schottky contact is compulsory for sample preparation. In material analysis, a graph of $1/C^2$ versus V is plotted from the measurement. It is also known as a Mott–Schottky plot. The conductivity type of the semiconductor sample can be obtained from the slope of the $1/C^2$ versus V graph. A positive slope indicates p-type conductivity while a negative slope indicates n-type conductivity as shown in Figure 3.11.

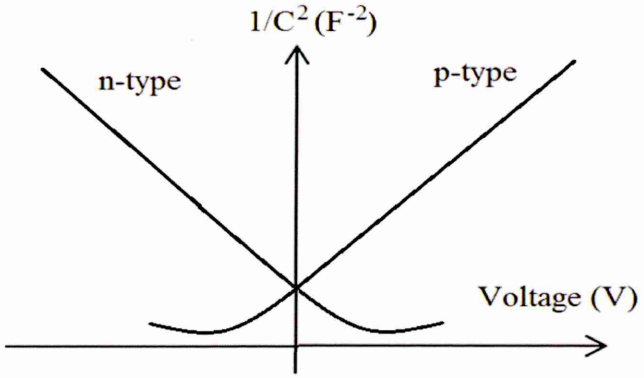

Figure 3.11: A plotted graph of $1/C^2$ versus V. The slope of the graph represents the conductivity type of the semiconductor.

The doping concentration of electrodeposited material can be determined from equation (3.19) and data from an $1/C^2$ versus V graph. The slope of the graph of $1/C^2$ versus V can be represented as in equation (3.18):

$$y = m\,(x + c), \text{is equivalent to } \frac{1}{C^2} = \frac{2}{\varepsilon_s e A^2 N_D}(\mathrm{V} + V_d) \quad (3.17)$$

Therefore, the slope of the graph, m, can be derived as:

$$m = \frac{2}{\varepsilon_s e A^2 N_D} \tag{3.18}$$

Thus,

$$N_D = \frac{2}{m\, \varepsilon_s e A^2} \tag{3.19}$$

with the known doping concentration value obtained from this measurement and the conductivity value from DC conductivity measurement, as discussed in section 3.3.3.2, the mobility of the charge carriers in the semiconductor can be calculated with equation (3.21) [22].

Thus,

$$\sigma = q\,(\mu_n N + \mu_P P) \tag{3.20}$$

where μ_n and μ_P refers to the mobility of the electrons and holes, and N and P refer to the density of free electrons and holes, respectively. Since in a doped semiconductor, majority carriers greatly outnumber minority carriers, equation (3.20) can be reduced to a single term involving the majority carrier [22]. Therefore,

$$\mu = \frac{\sigma}{q\, N_d} \tag{3.21}$$

3.3.4.4 Ultra-violet photoemission spectroscopy (UPS)

UPS measures the kinetic energy of photoelectrons produced by molecules which have absorbed UV photons. It is used to determine the position of the valence band maximum (E_v) and the Fermi level (E_F) and to study the E_F movement across the forbidden bandgap [21].

The UPS measurements in this work has been carried out using VG Scientific MultiLab 3000 ultra-high vacuum surface analysis system, equipped with a CLAM4 hemispherical electron energy analyser and a differentially-pumped He cold cathode capillary discharge UV lamp. Initially, the samples were excited with a resonance line He-I with the base chamber pressure in the 10^{-9} Torr range and the *hv* value of 21.22 eV to shift the spectra out of nonlinear region of the analyzer and to avoid instrumental distortions/cutoffs in the lens system at low kinetic energy. All the measurements were performed under the same negative bias of 18 eV in order to shift the spectra out of the

non-linear region of the analyser and to avoid instrumental distortions or cut-offs in the lens system at low kinetic energy levels. The position of the E_F is then measured from the He-I Fermi edge of gold films deposited on a half of each sample.

UPS measurement required simple sample preparation. Before the experiment, each sample was covered partially with a glass slide and a thin gold layer was sputtered on to the exposed region. A silver paste was used to connect the sputtered gold film with the sample stage to enable its effective electrical biasing.

3.3.5 Morphological characterisation

This section presents the instrument setups used for morphological characterisation of thin films in this work. These include scanning electron microscopy (SEM) and atomic force microscopy (AFM) instruments. Information on instruments, procedure and basic principles are also discussed.

3.3.5.1 Scanning electron microscopy (SEM)

SEM is a type of electron microscope that produces images of a sample by scanning it with a focused beam of electrons. Magnifications of up to 1,000,000x with an ultimate resolution of 1 nm can be achieved [23]. SEM can provide information on surface topography, grain structure, grain size, composition and electrical behaviour of the top few microns of the sample. This instrument was first invented by Manfred von Ardenne in 1937, who utilised the transmitted current to obtain images [24].

The schematic diagram of the SEM instrument is shown in Figure 3.12. The SEM instrument consists of four main components, which are electron source, the series of magnetic focusing lenses, the sample vacuum chamber with a sample stage region and the electronic console containing control panel, monitor and the scanning module. The electrons source of this instrument is the electron gun. There are three types of electron gun, which are tungsten filament, lanthanum hexaboride (LaB_6) and field emission gun. The electron beams typically have high energies up to 40 keV. Three electromagnetic condenser lenses are used to demagnify the electron beam into a fine probe that is scanned across the selected area of the sample. Each lens has an associated defining aperture that limits the divergence of the electron beam. The incident electrons penetrate the sample in a teardrop-shaped volume whose overall dimension depends on the energy beam and the atomic masses of elements of the sample [25]. The interaction of the electron beam with the sample produces secondary electrons, backscattered electrons, Auger electrons and X-rays, which are collected by various detectors. The

image produced by the secondary electrons demonstrates surface inclination contrast, where the image inclined towards the detector appears brighter than that turned away from the detector, whereas in the backscattering the brightness of the image corresponds to the element masses. In this case, the heavier elements appear brighter in the image than the lighter elements [25,26]. The signal from each detector is then rastered, synchronised with the electron beam and sent to a monitor.

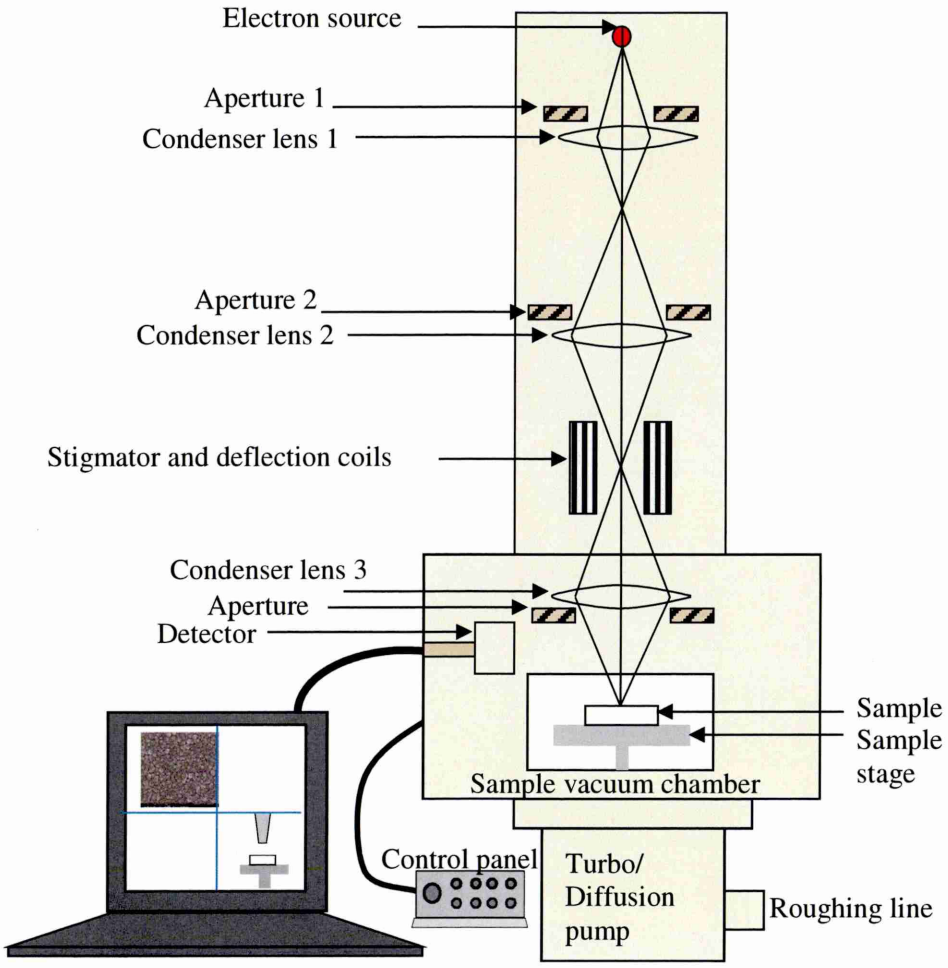

Figure 3.12: Schematic diagram of a SEM instrument showing the location of a sample stage and the series of lenses.

The SEM setup in this work is the FEI Nova NanoSEM 200. This system offers high resolutions of up to 1 nm in high vacuum mode with an accelerating voltage of up to 30 kV. SEM does not need special sample preparation, except for biological or non-conductive samples. This is because biological and non-conductive samples tend to

charge when scanned by the electrons in vacuum condition and cause scanning faults or other image artefacts. Therefore, it is necessary to coat a non-conductive sample with a thin layer (~10 nm) of gold in order to prevent the charging effect, thermal damage, thus improving the imaging of the sample.

3.3.5.2 Atomic force microscopy (AFM)

AFM uses a scanning probe microscope that is used to measure surface roughness, change in friction and local elasticity over a sample surface. It is a practical instrument, since the sample can be imaged in situ condition. AFM has a vertical resolution up to 1 Å but the lateral resolution is low (~30 nm) due to the convolution.

In AFM, a fine tip is scanned across the surface of the sample to measure surface morphology and construct a 3D image of the surface [27]. The concept of this operation is illustrated in Figure 3.13. To obtain an image, the tip attached to the cantilever is scanned over the sample surface. A laser beam is reflected off the back of the cantilever. The changes between the tip and the surface of the sample deflect the cantilever and are detected by a position-sensitive photodiode detector. This deflection is processed by the system electronics to determine topological height changes on the sample surface.

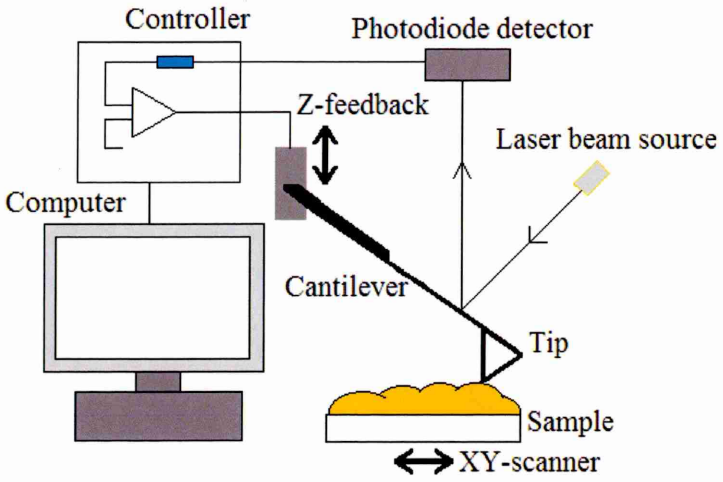

Figure 3.13: Schematic diagram of the setup operation in AFM measurement system.

The imaging process of AFM can be accomplished in either contact mode or tapping mode [28]. In contact mode the tip is in constantly in contact with the sample surface, whereas in tapping mode the cantilever is oscillated at its resonant frequency and the tip is gently tapped on the surface of the sample and consequently reduces sample damage. The tapping mode, therefore, is more commonly used when imaging very soft or very thin layers of material.

In this work, AFM is used to determine the surface morphology, topology and roughness of electrodeposited thin films. It does not require any sample preparation and it can image both conductive and non-conductive samples. AFM image analysis is important to provide some understanding of the surface of the electrodeposited materials before using them in fabrication of solar cell devices. A smooth and less rough thin film is sought after in order to promote good adhesion, better contact and reduce voids between layers.

3.3.6 Compositional characterisation

Composition of the electrodeposited materials was another essential parameter to investigate before these materials were used in the fabrication of solar cell devices. It is very important to get the right composition of each thin film in order to produce high-efficiency solar cell devices. Several techniques can be used to study atomic composition such as energy dispersive X-ray (EDX) spectroscopy, X-ray fluorescence (XRF) spectroscopy, mass spectroscopy (MS) and secondary ion mass spectrometry (SIMS). However, in this work we used EDX for compositional characterisation of electrodeposited thin films. The principles and basic operations of EDX spectroscopy is discussed further in this section.

3.3.6.1 Energy dispersive X-ray (EDX) spectroscopy

EDX spectroscopy is a qualitative and quantitative analysis that can provide information on the chemical composition of all elements in the periodic table from beryllium to uranium. The detection limit of EDX depends on the element's atomic mass. If the sample consists of elements that are lighter than aluminium, the detection limit is up to 0.5%, while if it consists of elements that are heavier than aluminium, the detection limit is about 0.2 to 0.3% [29]. Moreover, the lateral resolution of EDX is about 1 μm and this system is usually attached to the SEM instrument.

The principle of EDX is based on the X-ray spectrum that is emitted from the sample due to the ionisation of an atom when it is bombarded by a focused beam of

electrons [26, 29]. The illustration of this process for one atom is shown in Figure 3.14. During the bombardment, the incident electron ionises the atom by ejecting an inner-shell electron. In order to stabilise this atom, the electron from the outer shell makes a transition into the vacant inner shell. This transition produces a photon with energy equivalent to the energy potential difference between the two shells, which is emitted as an X-ray. The energy generated from this transition is unique for every atom. It carries the element of the parent atom and the characteristic of the transition. The cascade of this transition will continue until the last shell is reached. Therefore, many emissions can be produced if the sample has atoms with several shells.

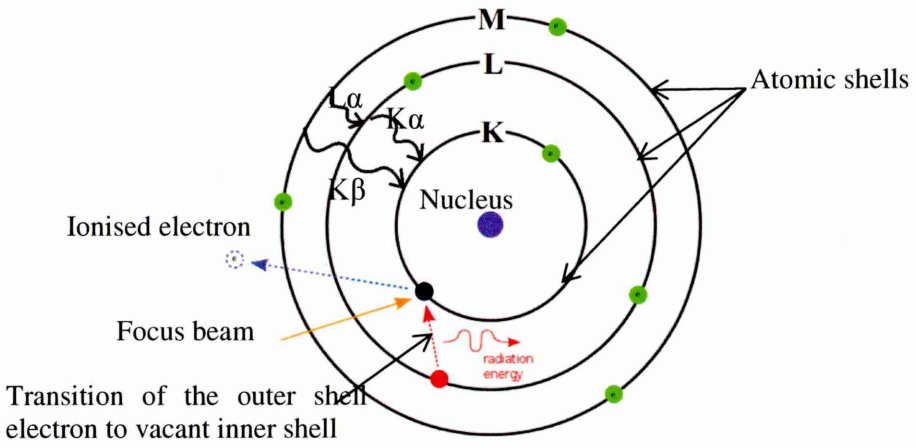

Figure 3.14: An illustration of atomic shells when the atom of the sample is bombarded with the high-energy focus beam electron.

The schematic of an EDX system is shown in Figure 3.15. The most important part in this system is the PIN-diode which is made from a silicon (Si) crystal with diffused lithium (Li) atoms. This diode is functional as a detector. After the incident electrons interact with the sample with the emission of X-rays, these rays pass through the window protecting Si(Li) diode and are absorbed by the detector crystal. The X-ray energy is then transferred to the Si(Li), processed into a digital signal that is displayed on a cathode ray tube (CRT) as a histogram number of photons versus energy.

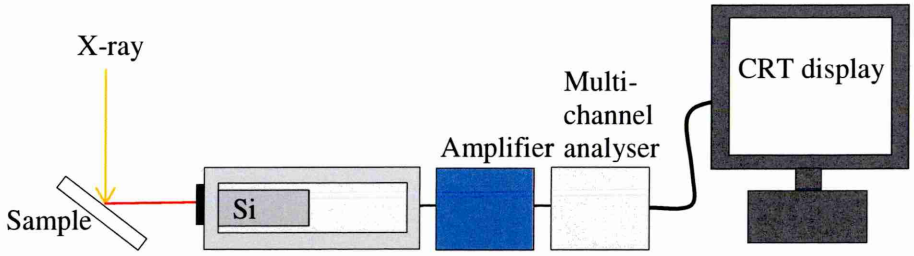

Figure 3.15: Schematic diagram of the instruments setup in EDX spectroscopy.

EDX used in this work is carried out using an EDX detector from Oxford Instruments attached to a FEI Nova NanoSEM 200. The software used in the mode mapping is INCA mode selector. EDX does not require any sample preparation except carbon coating, since most of the samples in this work are non-conductive thin films.

3.3.7 Defects characterisation

A defect is a distortion that changes the ideal crystal structure of semiconductor material. Defects in semiconductors are usually created by impurities, treatment with other materials and the annealing process. It can also come from the material structure itself, such as through a dislocation, stacking faults, interstitial defects and vacancies. The presence of defects in the semiconductor materials created energy states in the forbidden gap. This can cause a great effect on the electrical and optical properties of the semiconductor material. Many techniques have been used to investigate these defects. These include deep level transient spectroscopy (DLTS), photoluminescence (PL) and cathodoluminescence (CL). In this work, we used PL to study the defects in solar cell materials. Further details on this instrument is described in this section.

3.3.7.1 Photoluminescence (PL)

PL is the emission of photons with characteristic wavelengths from a semiconductor material (sample) after it is bombarded by a beam of high-energy photons. It is an important technique for measuring the purity and the crystalline quality of semiconductor materials. Defects arising from surface damage, dopants and impurities can be detected with this measurement [30]. The PL measurement in this work has been carried out using Renishaw inVia Raman Microscope with the PL wavelength excitation 632 nm at (~196 eV) with He-Ne laser as excitation source.

In PL, a sample gains energy by absorbing photons from the light source. This energy then promotes electrons from valence to the conduction band state. Due to instability, the electrons are then move to more stable excited levels such as the lowest level of the conduction band before they return back directly to the valence band or are trapped at any defect levels at the forbidden gap. The electrons then release their energy in the form of a photon. These photons are detected as photoluminescence. The spectrum of the PL intensity provides information about the properties of the sample. The illustration of this process is shown in Figure 3.16. Analyses of the PL peak

positions and intensities in the PL spectrum reveal density of traps and their location that represents the defect levels in the semiconductor material.

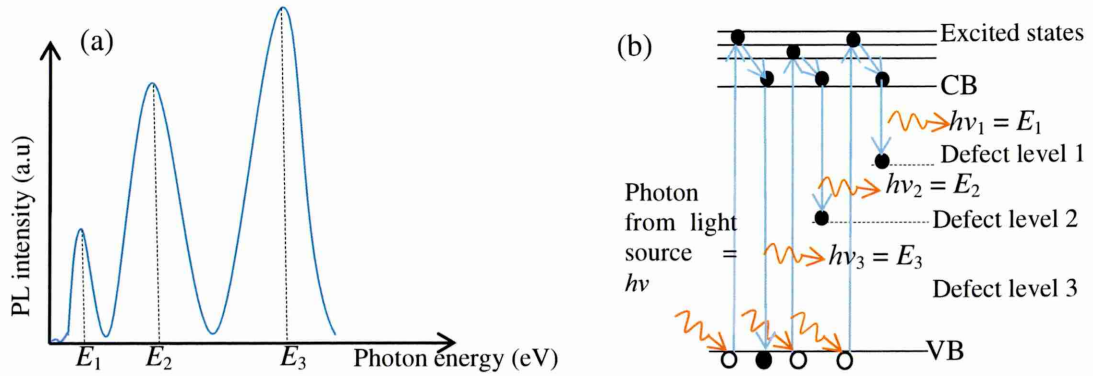

Figure 3.16: Schematic of (a) an energy band diagram showing electron excitation and defect levels in a semiconductor and (b) a PL spectrum which presents the peaks E_1, E_2 and E_3 due to electron transition in a semiconductor material.

3.4 Fabrication and development of solar cell devices

Typical CdTe solar cell structure consists of glass/FTO/CdS/CdTe/electrical contact. In this work, solar cell devices have been fabricated with different structures and conditions using three main electrodeposited materials, which are CdS, CdTe and PAni. In the final stage of the experimental work, graded bandgap of solar cells have also been studied with other semiconductor materials such as PAni, ZnS, CdSe and ZnTe. The development of solar cell devices in this work has been shown in the flow chart in Figure 3.1. The details of this fabrication and the processing steps, including the heat treatment, chemical etching and back contact metallisation will be discussed in details in this section.

3.4.1 Fabrication of the glass/FTO/CdS/CdTe solar cells

Initially the glass/FTO substrates were cleaned thoroughly before the electrodeposition of CdS thin films. About 200 nm of CdS films were electrodeposited on the substrate. The thickness of the CdS film should be appropriate in order to cover the rough surface of FTO uniformly. The thickness should not be too thin due to the the reduction of the thickness after being annealed. At the same time the too thick of CdS layer can caused high series resistance and low short current density in device performance. The CdS layers were heat-treated at 400°C for 20 minutes with or without chemical treatment. The treated CdS layer required basic etching to clean the unwanted substances or

chemical residues left on the surface of the CdS layer. About 1500 nm of CdTe layers were deposited as an absorber layer followed by the chemical treatments and annealing in air at 400°C for 20 minutes. The treated glass/FTO/CdS/CdTe solar cells were then required both acidic and basic etchant to polish the top surface of CdTe layer. These devices were then rinsed with deionised water and dried under a stream of nitrogen gas before the deposition of back electric contact (~100 nm Au contact). The sample with pinhole may need a thin layer of PAni as pinhole plugging layer before metal back contact deposition. The flowchart of the main step of fabrication of devices can be refer in Figure 3.1.

3.4.2 The etching process

Etching process is the last treatment stage before completion of the device with metal contact. The purpose of etching is to remove the unwanted substances and to provide a clean surface prior to metal contact deposition. There are two types of etchants used in this processing which are acidic etchant and basic etchant. An acid etchant was prepared by dissolving 1 gram of potassium dichromate ($K_2Cr_2O_7$) in 20 ml of deionised water followed by addition of ~0.1 ml of concentrated sulphuric acid (H_2SO_4) into the solution. As for basic etchant, 0.5 g of sodium hydroxide (NaOH) and 0.5 g of sodium thiosulphate ($Na_2S_2O_3$) was dissolved in 50 ml of deionised water and heated to about 50°C using a hot plate. The etching process starts by immersing the device structure into acidic solution for 5 seconds and rinse with deionised water. Then, the device should be etched in the basic solution for 2 minutes, rinse with deionised water and purge with nitrogen gas to dry up the surface. Once the etching process is complete, it should be transfered quickly onto the mask and proceed to metalliser since the etched layer will easily get oxidised in air. However, if the device has pinholes, it may require a thin layer of PAni before deposition of back metal contact.

3.4.3 Back metal contact deposition

Back metal contact deposition is the final stage of solar cell fabrication. The metal depositions were carried out by Edwards Auto 306 vacuum metalliser. A spiral shape of ~5 cm of gold wire was placed in the tungsten filament target. The chamber dome was properly positioned in order to avoid the leakage during pumping. The chamber was pumped and the pressure was brought down to 10^{-6} Torr. After the pressure in the chamber is below 10^{-6} Torr, the filament was slowly heated by applied

~2 A of direct current in low tension condition. The melted gold will evaporate and about 100 nm of Au thin film was deposited on the CdTe surface through the mask with circular shape of 2.0 mm diameter. Each circular gold contact on the device is a solar cell and at this point, it is ready for assessment.

3.5 Characterisation of solar cell devices

Solar cell device characterisation in this work is carried out by two different techniques, which are current-voltage (I-V) measurement and capacitance-voltage (C-V) measurement. The solar cell can be represented by the equivalent circuit model as shown in Figure 3.17. It consists of a light induced current source (I_L), a depletion capacitance (C_D), a diode, series resistance (R_s) and shunt resistance (R_{sh}). The effect of R_s and R_{sh} are observed in I-V characteristics while the effect of C_D can be observed in C-V measurements. This section, therefore, discusses the I-V and C-V measurements in detail.

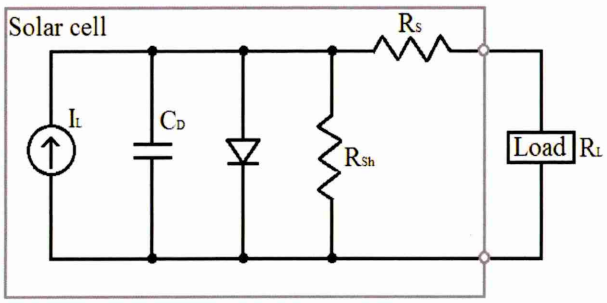

Figure 3.17: Equivalent circuit model of a solar cell showing the presence of C_D, R_{sh} and R_s.

3.5.1 Current-Voltage (I-V) characterisation

The current-voltage (I-V) characteristics of solar cells can be obtained under two different conditions. The first condition is without any illumination, or under dark conditions, while the second condition is under illumination. The I-V characterisation under dark conditions can determine the device parameters such as rectification factor (RF), ideality factor (n), saturation current (I_o), potential barrier height (ϕ_b), dark series resistance (R_s) and dark shunt resistance (R_{sh}), whereas I-V characterisation under illumination can derive the solar cell parameters such as open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF), conversion efficiency (η), series resistance (R_s) and shunt resistance (R_{sh}). The value of R_s and R_{sh} under dark and illuminated conditions can vary according to the photo-conductivity of materials and effect of

defects. I-V characterisation is carried out using a Keithley 614 digital electrometer and DC voltage source, which can source and measure both current and voltage under a solar spectrum simulator with AM 1.5 illuminations. The analyses of I-V characteristics for solar cell devices operating in the dark and under illumination are discussed below in details.

3.5.1.1 I-V characterisation under dark condition

A solar cell under dark conditions behaves like a rectifying diode. When an external voltage is applied across the diode, it will experience a high current only in forward bias. Ideally, there is no current at all when it is in reversed bias. In dark conditions, this behaviour can be represented by equation (3.22):

$$I_D = SA^*T^2 \exp\left(\frac{-e\phi_b}{kT}\right)\left[exp\left(\frac{eV}{nkT}\right) - 1\right] \tag{3.22}$$

where, S represents the area of the contact, A^* is Richardson constant for thermionic emission, T is temperature, e is electronic charge, ϕ_b is potential barrier height, k is Boltzmann constant and n is the ideality factor of the diode [31,32].

I-V characterisation under dark conditions can be present in log-linear form or in linear-linear form. In the log-linear form, the applied bias voltage is plotted in a linear scale on the x-axis and the current measured through the device is plotted in logarithmic scale on the y-axis. The graph of Log I versus V is shown in Figure 3.18. The parameters that can be derived from this graph are RF, n, I_o and ϕ_b.

RF is a ratio of forward current, I_F, to reverse current, I_R at given voltage. It represents the rectification quality of the diode. From this graph, RF can be obtained from the saturation current of logarithm I_F and the I_R, and the calculation is shown in equation (3.23). A higher value of RF is required for better solar cell efficiency, but then the RF with three orders of magnitude (~10^3) is adequate to produce a good solar cell with high efficiency [32].

$$RF = \left(\frac{I_F}{I_R}\right)_{V=1.0\,V} \tag{3.23}$$

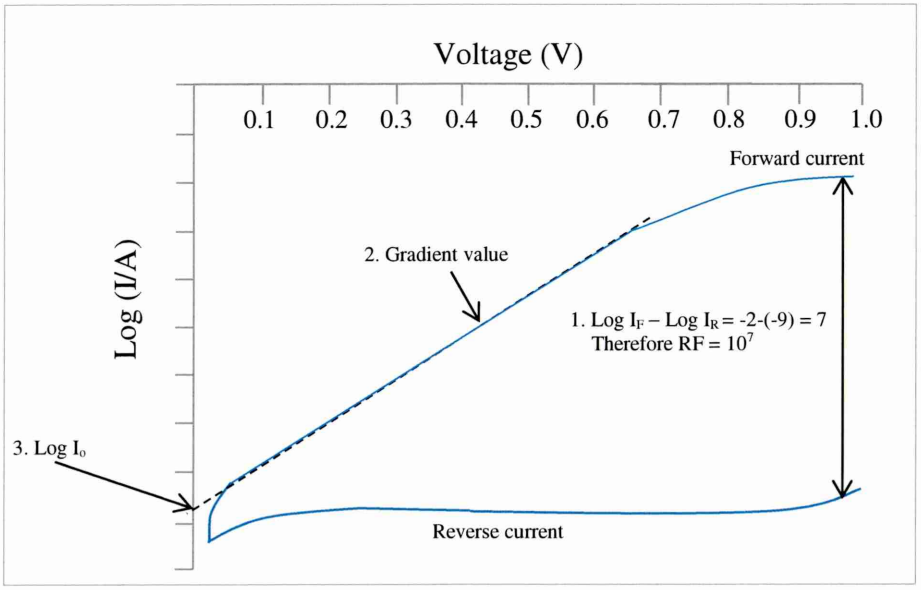

Figure 3.18: A typical graph of log- linear I-V characteristics of a diode under dark condition.

The n value provides a general idea about the current transport through the potential barrier [31]. It can be calculated using equation (3.24) and the slope, m of the straight line portion of the forward current in the graph. For an ideal diode, n should be in between of 1.00 and 2.00 [31, 32, 33]. If the current transport through potential barrier is only dominated by thermionic emission, the value of n is 1.00. If the metal-semiconductor interface is full of recombination and generation centres, and the current transport is only by recombination and generation process, the value of n becomes 2.00 [34]. In practical devices, both mechanism taken place and therefore n value is between 1.00 and 2.00.

$$n = \left(\frac{q}{(2.303)(gradient)kT}\right) \qquad (3.24)$$

where q is is the electron charge, 2.303 is the conversion from ln 10 to log, k is the Boltzmann constant (1.3806×10^{-25} JK^{-1}) and T is temperature.

The I_o represents the degree of rectification of the diode. If the diode rectification is high, I_o is low. I_o can be obtained from the Y-intercept of the straight line portion of the forward current in the graph as shown in Figure 3.18. With this known I_o value, the ϕ_b of the diode can be calculated using equation (3.25).

$$\phi_b = \frac{kT}{q} \ln\left(\frac{SA^*T^2}{I_o}\right) \quad (3.25)$$

where k is the Boltzmann constant (1.3806×10^{-25} JK^{-1}), T is temperature, q is is the electron charge, S is the cell area and A^* is the effective Richardson constant.

In the linear-linear form, the applied bias voltage is plotted on the x-axis and the current measured through the device is plotted on the y-axis. A typical graph of I versus V is shown in Figure 3.19. The parameters that can be derived from this graph are R_s and R_{sh} [31]. The R_s is due to the resistance of the metal contact, interface within the device, defects and junction depth. A good solar cell requires a low value of R_s, while an ideal diode has zero R_s (R_s=0). R_s can be determined from the slope of the straight line portion at the high forward end of the dark I-V curve.

The value of R_{sh} denotes the presence of a current leakage path in the solar cell, and an ideal diode has infinite R_{sh} (R_{sh}=∞). Therefore, a high value of R_{sh} is desirable for a good solar cell. R_{sh} can be obtained from the slope of the straight line portion in the reverse current as shown in Figure 3.19.

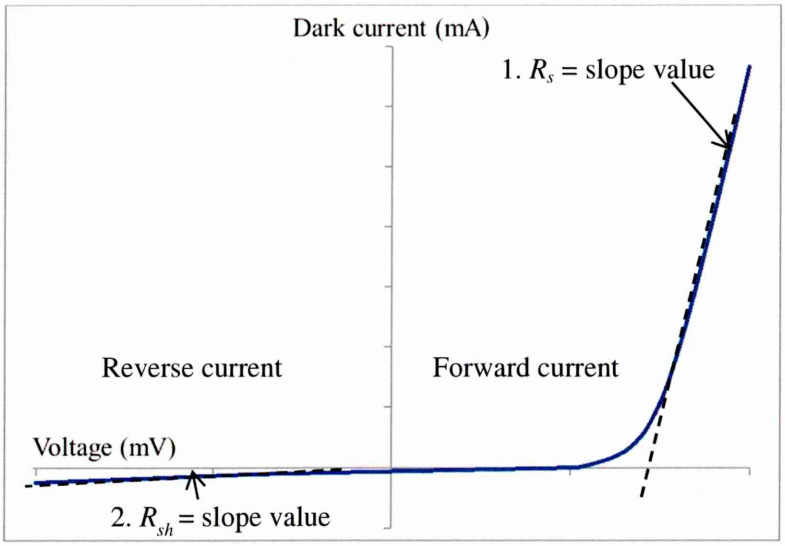

Figure 3.19: A graph of linear-linear I-V characteristics of a diode under dark conditions.

3.5.1.2 I-V characterisation under illumination

The I-V characteristics under illumination can be plotted in a linear-linear graph as shown in Figure 3.20. The parameters that can be derived from this graph are V_{oc}, J_{sc}, FF, η, R_s and R_{sh}. The V_{oc} and J_{sc} (or I_{sc}) can be derived directly from the graph. The FF

can be obtained by drawing the largest possible rectangle through the maximum power point voltage, V_m, and current, I_m, as shown in Figure 3.20 followed by the calculation in equation (3.27). The η can be calculated by using equation (3.28). The R_s and R_{sh} can be derived in the same way as in the dark I-V graph, which has been described previously.

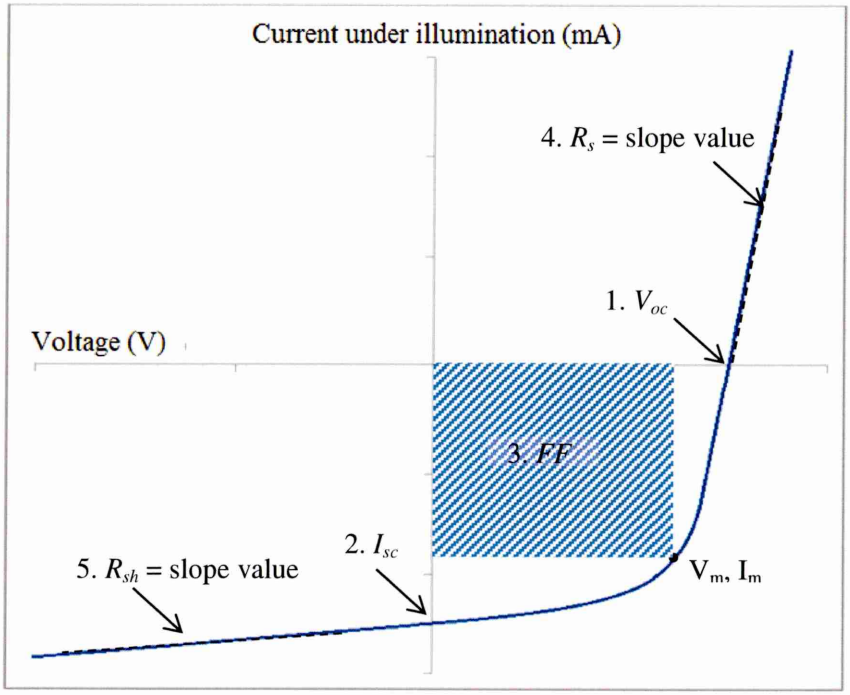

Figure 3.20: A graph of I-V characteristics of a solar cell under illumination.

The V_{oc} is the output voltage of the device under illumination when the current flowing through the junction is zero or the load resistance is much greater than the device resistance. V_{oc} can be obtained from the X-intercept when the illumination current density = 0 in the I-V graph as shown in Figure 3.20. The value of J_{sc} represents the photocurrent flowing through a cell junction when the device is short circuited. The short circuit current density depends on the intensity of the light source and the spectral response of the device. Short circuit current, I_{sc} can be derived from the Y-intercept when the voltage is zero in the I-V graph as shown in Figure 3.20. The J_{sc} can be calculated from equation (3.26), where S represents cell area in cm^2.

$$J_{SC} = \frac{I_{SC}}{S} \qquad (3.26)$$

The *FF* is the ratio of the maximum electrical power output, P_m, to the product of V_{oc} and I_{sc}. It can be represented as equation (3.27). *FF* is affected by the value of the ideality factor n, R_s and R_{sh} of the cell. Low values of n and R_s, and a large value of R_{sh} are required for a high *FF*.

$$FF = \frac{P_m}{V_{oc}I_{sc}} = \frac{V_m I_m}{V_{oc}I_{sc}} \tag{3.27}$$

The conversion efficiency of the solar cell, η, is the parameter that describes the overall performance and is expressed in terms of I_{sc}, V_{oc}, *FF* and the input power, P_{in} as shown in equation (3.28) and (3.29) [33].

$$\text{Efficiency } (\eta) = \frac{Power\ output}{Power\ input} = \frac{V_m I_m}{P_{in}} \tag{3.28}$$

$$\eta = \frac{I_{sc} \times V_{oc} \times FF}{P_{in}} \tag{3.29}$$

where P_{in} is the solar power of the incident light. The P_{in} value in this measurement is 100 mW·cm^{-2}, since it used standard AM 1.5 illumination.

3.5.2 Capacitance-Voltage (C-V) characterisation

The information and basics of C-V measurement for thin film characterisation has been discussed in Section 3.3.4.3. The purpose of a C-V measurement conducted on a solar cell device is to determine the width of the depletion region, w. The depletion region in a solar cell can be estimated from the depletion capacitance, C_D. The value of C_D can be considered as the parallel plate capacitor separated by a distance, w between the two opposite charged plates [35,36]. The graph of C versus V can be illustrated in Figure 3.21.

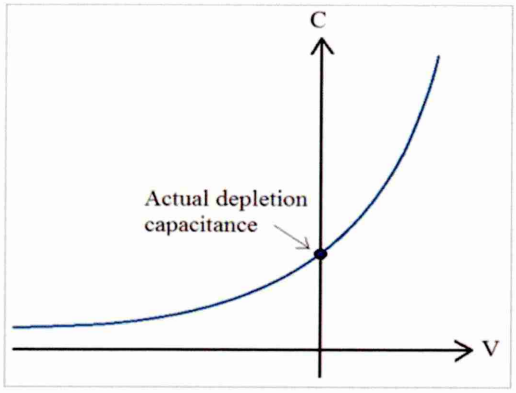

Figure 3.21: A typical graph of depletion layer capacitance versus V of a solar cell.

From this graph, the actual depletion capacitance of the junction can be obtained from the curve at zero bias (V=0), known as C_o or C_D. The width of the depletion region can be determined using equation (3.30):

$$C_o = \frac{A\,\varepsilon_o\,\varepsilon_r}{W} \qquad (3.30)$$

where ε_o is the permittivity of free space, ε_r is the relative permittivity or dielectric constant of the semiconductor and A is the contact area.

Similar to thin film characterisation, the doping concentration, N_D, of a solar cell diode can be determined from equation (3.31) and data from a $1/C^2$ versus V graph.

$$\frac{1}{C^2} = \frac{2}{\varepsilon_s q A^2 N_D}(V + V_d) \qquad (3.31)$$

where ε_s is the semiconductor permittivity, q is the charge carrier, A is the area of the capacitor and N_D is the doping concentration.

The gradient, $m = \frac{2}{\varepsilon_s q A^2 N_D}$ provides the doping concentration, N_D of the semiconductor.

$$N_D = \frac{2}{m\,\varepsilon_s e A^2} \qquad (3.32)$$

With a known N_D value obtained from this measurement (equation 3.32) and effective density of states at conduction band edge, N_C given by equation (3.36) and (3.37), the Fermi level position in the bandgap can be estimated by using equation (3.34) and (3.35).

$$N_D = N_c \, exp\left(\frac{-q\Delta E}{kT}\right) \tag{3.33}$$

N_D is known as N_A for p-type semiconductor. Therefore,

Bandgap for n-type semiconductor:

$$E_c - E_f = \frac{kT}{q}\ln(\frac{N_C}{N_D}) \tag{3.34}$$

Bandgap for p-type semiconductor:

$$E_v - E_f = \frac{kT}{q}\ln(\frac{N_C}{N_A}) \tag{3.35}$$

and N_C can be calculated from equation (3.35) and (3.36),

For n-type semiconductor:

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}} \tag{3.36}$$

For p-type semiconductor:

$$N_c = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{\frac{3}{2}} \tag{3.37}$$

where m_e^* is the effective electron mass for the semiconductor ($m_{e\,(CdTe)}^*$=0.11m_o), m_p^* is hole effective mass of the semiconductor ($m_{p\,(CdTe)}^*$=0.4m_o) [37], m_o is the free electron mass (9.1×10^{-31}) kg, k is the Boltzmann constant (1.3806×10^{-23} $m^2kgs^{-2}K^{-1}$), T is temperature and h is the Planck constant (6.626×10^{-34} m^2kgs^{-1}) [37].

3.6 Overall conclusions

The summary of experimental methods in this work is presented as a flowchart in Figure 3.1. The detailed explanations of the sample preparation which includes the substrate, cutting and cleaning procedure are presented in Section 3.1 followed by the

description of the ED process of CdS, CdTe and PAni in Section 3.2. The various thin film characterisation techniques, which include the cyclic voltammogram, structural, optical, electrical, morphological, compositional, thickness and defect characterisation are presented and discussed in Section 3.3. Each technique is distinctive and important to understand thin film behaviour before the device fabrication. The details of device fabrication processes are presented in section 3.4. The last part of this chapter (Section 3.5) discussed device characterisation techniques such as I-V measurements under dark and illuminated conditions, C-V measurements and the parameters of the solar cells obtained from these measurements.

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Chapter 4 - Characterisation of CdS thin films

4.0 Introduction

This chapter presents systematic studies on the window layer used in solar cell device, CdS thin films. The effect of growth parameters, annealing conditions, chemical treatments and sulphur concentrations in CdS electrolyte have been studied with various thin film characterisation techniques such as XRD, Raman spectroscopy, UV-Vis spectroscopy, optical profilometry, PEC measurement, DC conductivity measurement, C-V measurement, SEM, AFM and EDX. The objective of this work is to understand the properties of CdS thin films under various conditions before employing them as a window layer in the solar cell device structure. This chapter has been divided into five main parts and the summary of this is illustrated in the flowchart in Figure 4.1.

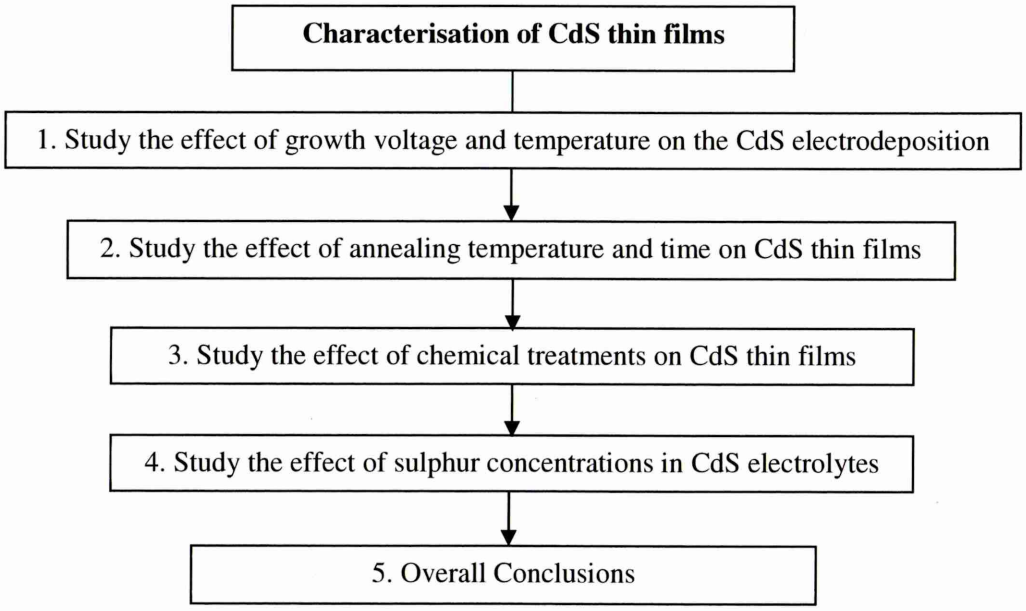


Figure 4.1: Flow chart of the characterisation of CdS thin films.

4.1 Study the effect of growth voltage and temperature on the CdS electrodeposition

This section presents the research on growth parameters, which include the growth voltage, V_g and growth temperature, T_g on CdS electrodeposition. Initially, the cyclic voltammogram experiment was carried out to study the CdS behaviour (deposition and dissolution) during the voltage scan. By referring to the suitable voltage range in the voltammogram result, the samples were grown at different V_g and characterised for their

properties. CdS thin films have also been grown at three different temperatures at 25, 50 and 85°C in order to optimise the best T_g. The electrodepositions were carried out potentiostatically in a two-electrode system and the deposition time was kept constant for 60 minutes.

4.1.1 Voltammogram

A cyclic voltammogram was obtained in order to estimate the approximate voltage range for film deposition. Using the voltage range estimated, CdS thin films were grown at different V_g and the growth conditions were optimised after characterisation. Figure 4.2 shows a typical cyclic voltammogram of aqueous solutions of (a) 0.3M $CdCl_2$, (b) 0.06M $(NH_4)_2S_2O_3$ and (c) mixture of 0.3M $CdCl_2$ and 0.06M $(NH_4)_2S_2O_3$ during the forward and reverse cycles between 0 and 2500 mV at the scanning rate of 3 mVs^{-1}. The pH and bath temperature was maintained at 2.00±0.02 and 85°C, respectively.

From Figure 4.2(a), it is noted that Cd from the $CdCl_2$ source started to deposit in the forward cycle at a cathodic voltage of around 1049 mV. Cd has a reduction potential of E^o=-400 mV [1]. As the cathodic voltage increases, the current density increases and thus more Cd is deposited. In Figure 4.2(b), the deposition of sulphur is observed at ~438 mV, thus suggesting that sulphur is being deposited at a lower V_g compared to Cd. Sulphur has a reduction potential of E^o=+449 mV [1].

From the voltammogram of a mixture of 0.3M $CdCl_2$ and 0.06M $(NH_4)_2S_2O_3$ shown in Figure 4.2(c), it is observed that CdS starts to deposit at ~718 mV in the forward cycle and starts to dissolve after 1397 mV. At point ~1397 mV in the reverse cycle the deposition rate of CdS is equal to dissolution rate; therefore, the current density growth, J_g is zero. It is also observed a clear hump in the forward scan starting at the V_g~875 mV to ~1450 mV. This is associated with the co-deposition of Cd and S atoms to form a mixture of sulphur and cadmium sulphide. The film colour starts changing to transparent yellow at $V_g \geq 500$ mV, which suggests a sulphur-rich region. These films start turning to transparent greenish-yellow at V_g~1100 mV and above, thus suggesting the presence of stoichiometric CdS. As the growth potential increased to ≥1600 mV, the film colour becomes dark green in appearance, which suggests that the $V_g \geq 1600$ mV are in the Cd-rich region. CdS thin films with a good dark yellow appearance can be grown at the V_g from 1100 mV to 1500 mV. Changing the applied potential can vary the composition of the formed CdS compound [2]. Therefore, the

stoichiometry of CdS thin film is predictable, showing sulphur-rich materials at lower V_g and cadmium-rich films at higher V_g. The detailed study on the cathodic potential from 1400 to 1500 mV was carried out to obtain the best V_g to grow CdS thin films. After growing at fixed cathodic voltages and characterisation with XRD, this voltage region was narrowed down to 1440-1460 mV.

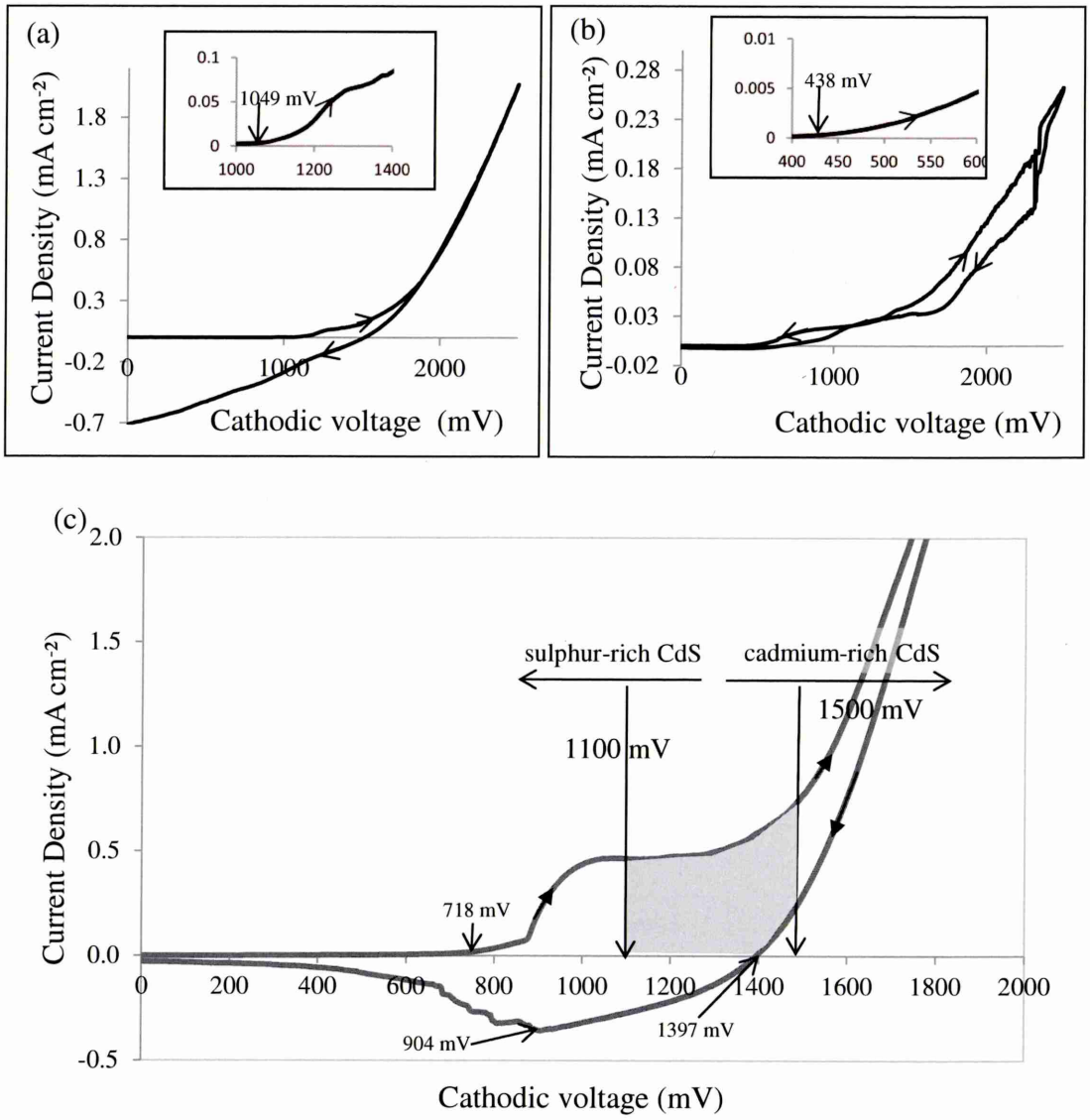


Figure 4.2: Cyclic voltammograms for aqueous solutions of (a) 0.3M $CdCl_2$, (b) 0.03M $(NH_4)_2S_2O_3$ and (c) mixture of 0.3M $CdCl_2$ and 0.03M $(NH_4)_2S_2O_3$ using glass/FTO as the cathode and a graphite rod as the anode. The arrows indicate the directions of the cycles.

4.1.2 Structural characterisation

Structural study for CdS thin films in this work have been carried out by XRD measurement. For V_g study, CdS thin films were grown at different cathodic potentials from 1440 mV to 1460 mV. The study on V_g was done by referring to the best crystallinity as observed in XRD for as-deposited and annealed CdS layers. The XRD patterns of the as-deposited and annealed CdS layers are shown in Figures 4.3(a) and (b), respectively. An intense hexagonal CdS peak (002) overlaps with FTO peak at 2θ = 26.67°. The appearance of (002) peak has been reported in the hexagonal phase for CdS thin film produced from spray pyrolysis [3, 4, 5], vapour deposition [6, 7] and chemical bath deposition [8, 9, 7]. This is due to the nature preferred growth direction of CdS, which is along the c-axis normal to the substrate. According to the as-deposited samples in Figure 4.3(a), the appearance of small crystalline peaks of CdS are observed at 2θ = 24.93° and 28.46°, corresponding to the (100) and (101) hexagonal planes. Also a small crystalline peak of sulphur (S) at 2θ = 32.22° and cubic CdS at 2θ = 30.81° and 43.91° were observed, corresponding to diffraction of (200) and (220) planes respectively. Thus, this verifies that as-deposited CdS thin films are polycrystalline in nature with mixed phases. The annealing process typically reduces the excess sulphur and causes phase transition from the mixture of a cubic and hexagonal phase to a single hexagonal phase. It is well known that CdS can grow in two crystalline structures that are cubic (zinc blende) and hexagonal (wurtzite) [10]. Between these two crystalline structures, the hexagonal structure is the thermodynamically more stable while cubic CdS with zinc blende structure is a metastable phase [10]. The formation of a particular CdS thin film structure is dependent on the preparation conditions [11, 12, 13]. Kaur et al. [14] reported that the CdS films exhibit hexagonal and cubic structures due to vigorous stirring during the electrodeposition [12]. From this work, it is observed that CdS grown at V_g=1455 mV shows the highest crystallinity films in both as-deposited and after annealing; therefore, it suggests that the film has the highest order of atomic arrangement, which is homogenous and more stoichiometric.

Figure 4.4 shows the XRD spectra plotted in log-scale in order to identify all peaks. These spectra are for as-deposited and heat-treated CdS layers grown at V_g=1455 mV. The three peaks of hexagonal CdS show an obvious enhancement in crystallinity after heat treatment. This is probably because of the reduction of strain in the film due to some degree of reorientation of the particles during the heat treatment process [14].

The summary of XRD data and the obtained structural parameters of CdS thin films grown at V_g=1455 mV are shown in Table 4.1. The crystallite size, D was calculated using Scherrer's formula:

$$D = \frac{0.94\,\lambda}{\beta \cos\theta} \tag{4.1}$$

where λ is the wavelength of the X-rays used (1.541 Å), β is the full width at half maximum (FWHM) of the diffraction peak in radian and θ is the Bragg angle.

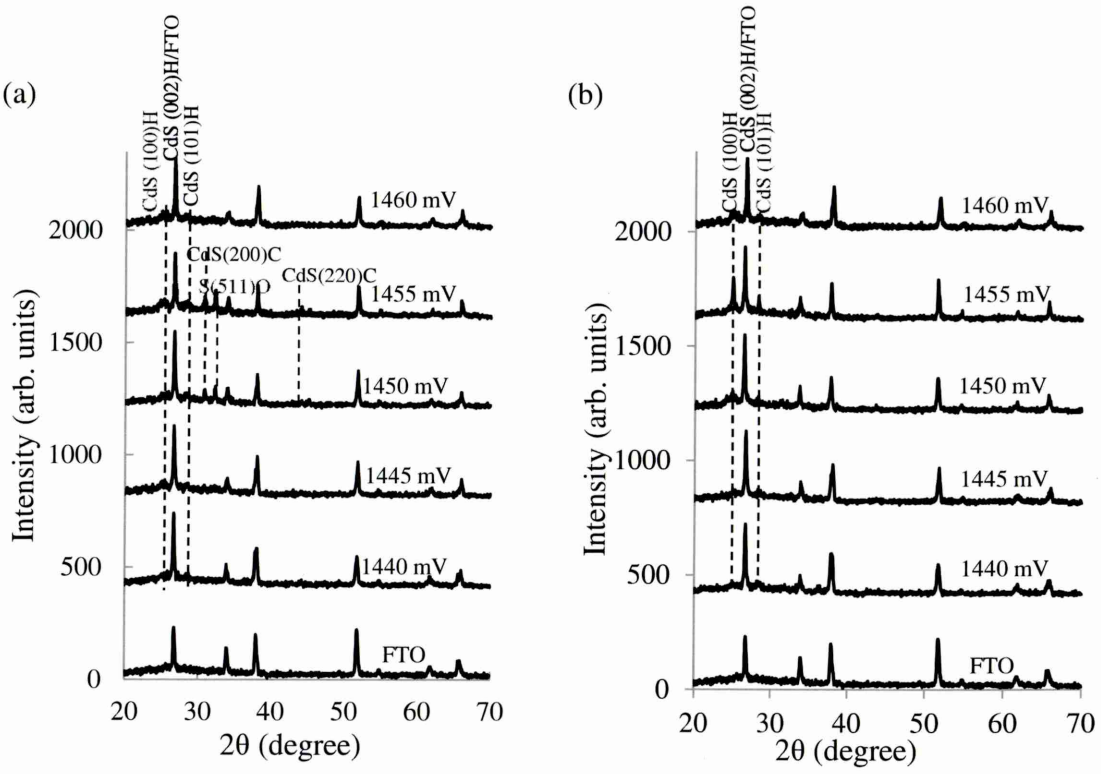


Figure 4.3: XRD patterns of CdS thin films grown at V_g range from 1440-1460 mV (a) for as-deposited and (b) after heat treated in air.

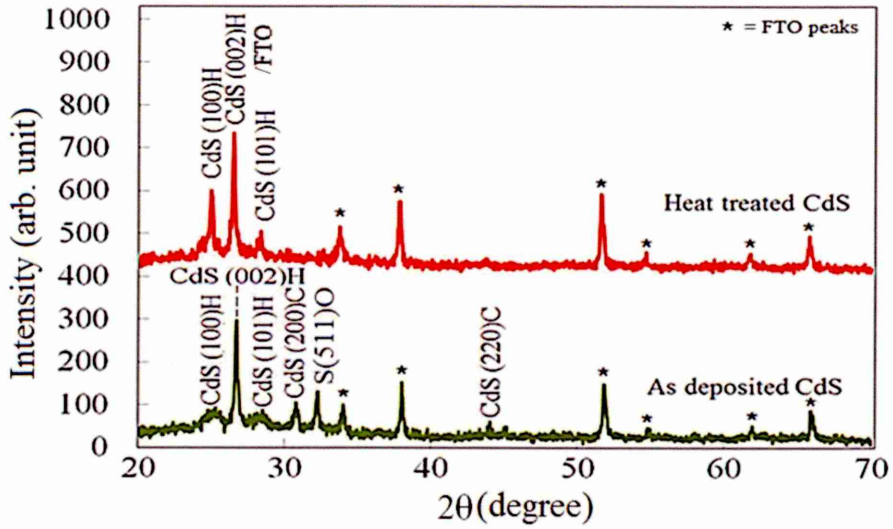


Figure 4.4: XRD patterns of CdS layer grown at 1455 mV plotted in log-scale.

Table 4.1: Summary of XRD data for as-deposited and heat treated CdS. Both samples were grown at 1455 mV.

Sample	Angle (2θ)	Intensity relative to the peak at ~26° (%)	FWHM (Degrees)	Plane of orientation (h k l)	Crystallite size, D (nm)	d-spacing (Å)	Assignments
AD CdS (V_g = 1455 mV)	24.93	8.9	0.779	(1 0 0)	11.7	3.56	Hex CdS
	26.67	100.0	0.197	(0 0 2)	47.0	3.34	Hex CdS/FTO
	28.46	7.8	0.322	(1 0 1)	29.3	3.11	Hex CdS
	30.81	19.2	0.325	(2 0 0)	29.7	2.90	Cubic CdS
	32.22	33.7	0.213	(5 1 1)	45.9	2.78	Orthorhombic S
	43.91	5.1	0.325	(2 2 0)	35.5	2.32	Cubic CdS
HT CdS (V_g = 1455 mV)	24.86	48.5	0.279	(1 0 0)	32.7	3.58	Hex CdS
	26.46	100.0	0.162	(0 0 2)	57.1	3.37	Hex CdS/FTO
	28.15	27.9	0.265	(1 0 1)	35.6	3.17	Hex CdS

In order to study the effect of deposition temperature for electrodeposition of CdS, three different CdS layers were grown at V_g of 1455 mV for 1 hour at three different temperatures of 25°C, 55°C and 85°C. The XRD spectra of these samples are shown in Figure 4.5. It is observed that samples grown at 25°C and 55°C having only one noticeable peak of hexagonal CdS overlaps with FTO peak at 2θ = 26.72°. The sample grown at 85°C shows a rising of another two peaks at 2θ = 25.32° and 28.16°

corresponding to the (100) and (101) hexagonal planes, respectively. Also, a small peak of cubic CdS at 2θ = 30.81° corresponding to diffraction of (220) plane was observed for CdS grown at 85°C. The arising of several peaks for sample grown at 85°C indicates that the crystallinity of CdS increased as the growth temperature increased. This is also possibly due to the increase in films thickness since a higher temperature bath usually enhances the deposition rate of the chemicals in electrodeposition.

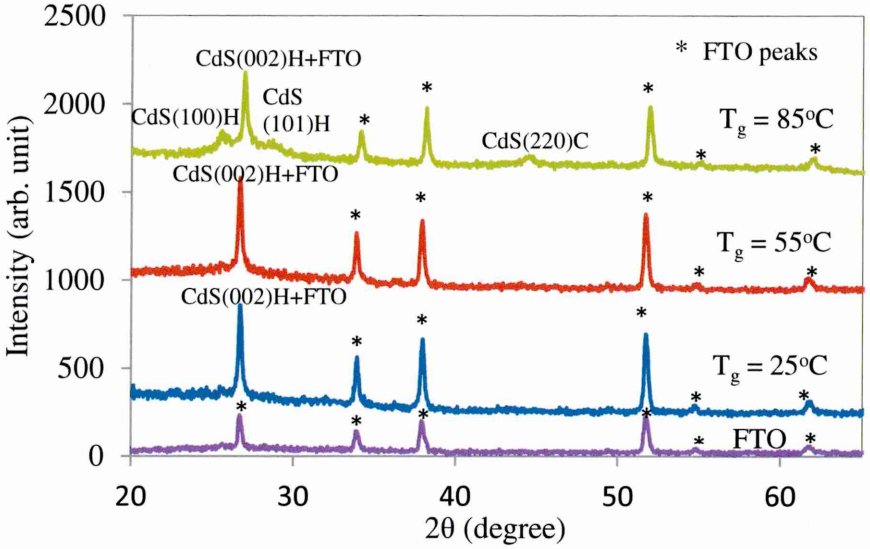


Figure 4.5: The XRD spectra of as-deposited CdS thin films deposited at 25°C, 55°C and 85°C. Note that these layers were grown at 1455 mV for 60 minutes.

4.1.3 Optical characterisations

Optical properties of CdS layers were studied at room temperature by using a UV-Vis spectrophotometry in the wavelength range 200 nm - 1000 nm. Measurements were carried out to study the optical absorbance and transmittance behaviour of CdS layers. Figure 4.6 shows the optical absorbance spectra for CdS thin films grown at different voltages for as-deposited and annealed samples. The square of absorbance (A^2) has been plotted as a function of photon energy, and the energy bandgap was estimated by extrapolating the straight-line portion of the graph to the photon energy axis. The energy bandgap of as-deposited CdS films was found to be scattered from 2.30 to 2.50 eV. It is observed that the energy bandgap gradually reduces with an increase in V_g. It is understood that deposition at higher potential enhances the deposition rate of cadmium, resulting in lower bandgap [15]. This bandgap shift is also clearly consistent with the

change of the colour of the CdS thin films, as shown in Figure 4.7. CdS layers grown at lower growth potentials ($V_g \leq 1445$ mV) show transparent yellow films and, as the V_g increases, the film colour becomes slightly dark green in appearance, which demonstrates the effect of Cd-richness. After the heat treatment of the samples at 400°C for 20 minutes, most of the bandgap energies shifted to 2.42 eV, which is equal to the bulk (standard) value for hexagonal CdS.

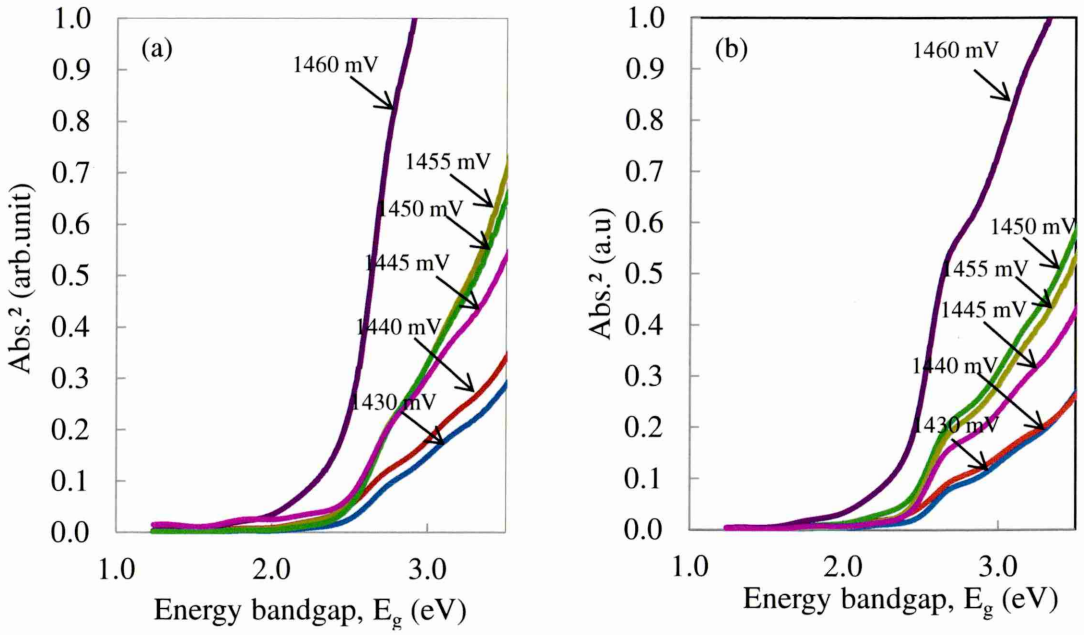


Figure 4.6: Optical absorption of CdS thin films grown at different V_g for (a) as-deposited and (b) heat treated samples at 400°C for 20 minutes in air.

Table 4.2: Energy bandgap of CdS films grown at different growth potentials.

	Energy bandgap, E_g (eV)					
V_g (mV)	1430	1440	1445	1450	1455	1460
As-deposited	2.50	2.45	2.41	2.38	2.32	2.30
Heat Treated	2.42	2.42	2.42	2.42	2.40	2.40

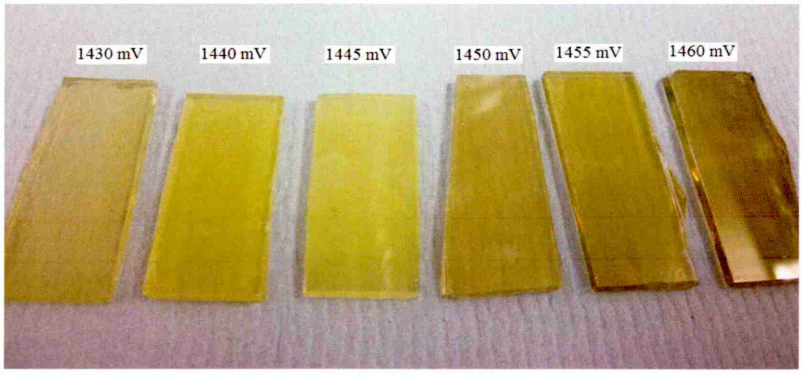


Figure 4.7: The physical image of CdS layers grown at different V_g.

4.1.4 Thickness measurements

The thickness of CdS thin films with different growth temperature were measured using an optical profilometer and calculated by using Faraday's laws of electrolysis equation. The growth temperature was carried out systematically from room temperature (25 ± 2°C) up to 85±2°C deposited at V_g = 1455 mV for 60 minutes. It was observed that the thickness of the films showed an increment with higher growth temperature. Increasing growth temperature resulted in higher deposition rates and consequently thicker films are produced for the same deposition time.

Table 4.3: The summary of CdS thin film thickness as a function of growth temperature at V_g=1455 mV.

Growth Temperature, T_g (°C)	Average current density during growth, J_g ± 1 (μA cm^2)	Film thickness		Deposition rate ± 0.1 (nm min^{-1})
		Faraday's law equation ± 1 (nm)	Optical profilometry ± 50 (nm)	
25	43	232	167	3.8
55	107	595	533	10.1
85	134	745	750	12.4

4.1.5 Electrical characterisation

The electrical characterisation of CdS gown with different V_g has been studied using PEC cell measurement to determine the conductivity type of films. Figure 4.8 shows the trend of PEC signal for as-deposited and heat-treated CdS thin films. It is observed that

all CdS thin films have n-type conductivity for as-deposited and heat-treated samples. The natural n-type conductivity of CdS films is due to the intrinsic donor defect caused by S vacancies and Cd interstitials in the crystal lattice [16]. About 67% of the PEC signals move towards the –n side after annealing, especially for CdS grown at higher cathodic potentials V_g > 1300 mV. This is attributed to the sulphur (S) evaporation during the heat treatment.

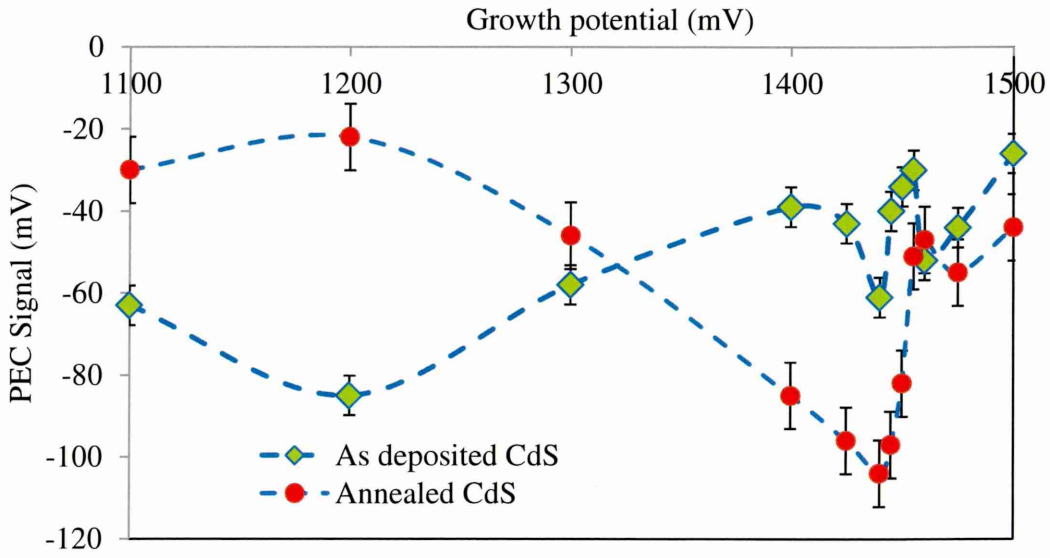


Figure 4.8: PEC signals of CdS layers grown at cathodic potential from 1100 mV to 1500 mV, indicating n-type electrical conduction for all layers.

4.1.6 Morphological characterisation

Microstructure and morphological study of CdS with different growth temperature were carried out using SEM measurement. The growth temperature was carried out from 25°C, 55°C and 85°C. All of the samples were deposited at V_g = 1455 mV for 60 minutes. The thickness measurement in the previous section shows that increasing the growth temperature resulted in thicker film. The microstructures from the SEM images in Figure 4.9 show a similar trend. The packing of grains of CdS grown at 25°C is not as dense as the CdS grown at 55°C and 85°C. It is demonstrated that the substrate is not completely covered and pinholes are observed. A similar image is seen for a sample grown at 55°C but the grain sizes are larger. CdS thin film grown at 85°C has completely covered the FTO surface without any pin-hole appearance. The grain sizes are also bigger than those deposited at 55°C and 25°C. This is due to the higher

crystallinity of CdS thin film grown at 85°C, which enhanced the agglomeration size of CdS. This result established that growth temperature can contribute to the grain formation. Varying film thickness also improves the coverage and removal of pinholes. According to the results summarised in Table 4.3, the film thickness grown at 25, 55 and 85°C are approximately 180, 550 and 750 nm, respectively. Therefore, full coverage and pinhole removal can be fully explained. In thicker layers grown at 85°C, large agglomerations can be observed consisting smaller crystallites of CdS.

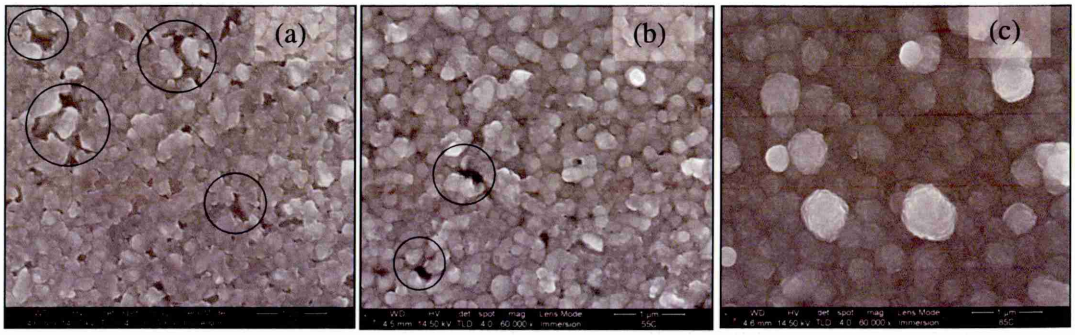


Figure 4.9: SEM images of CdS thin films grown at (a) 25°C, (b) 55°C and (c) 85°C. All of these films were grown at 1455 mV.

4.1.7 Composition characterisation

The composition of electroplated CdS layers have been characterised using EDX to study the percentage of Cd and S atoms presents in the layers. Figure 4.10 (a) and (b) show the EDX spectra of as-deposited CdS layers grown at 1200 mV (S rich region) and 1500 mV (Cd rich region). As shown in Figure 4.10 (a), the composition of Cd:S atoms at V_g=1200 mV is 45.2:54.8 which demonstrates that as-deposited CdS layer is more rich in S than in Cd whereas in Figure 4.10 (b), the atomic percentage of Cd:S at V_g=1500 mV is found to be 61.3:38.7 showing that the CdS layer is more rich in Cd than in S. This EDX analysis further confirmed the earlier statement in Section 4.1.1 that S-rich region was achieved at low V_g while while Cd-rich region was achieved at high V_g. It should also be considered that EDX analysis typically carries uncertainty of the order of 1-3% depending on the accuracy of calibration.

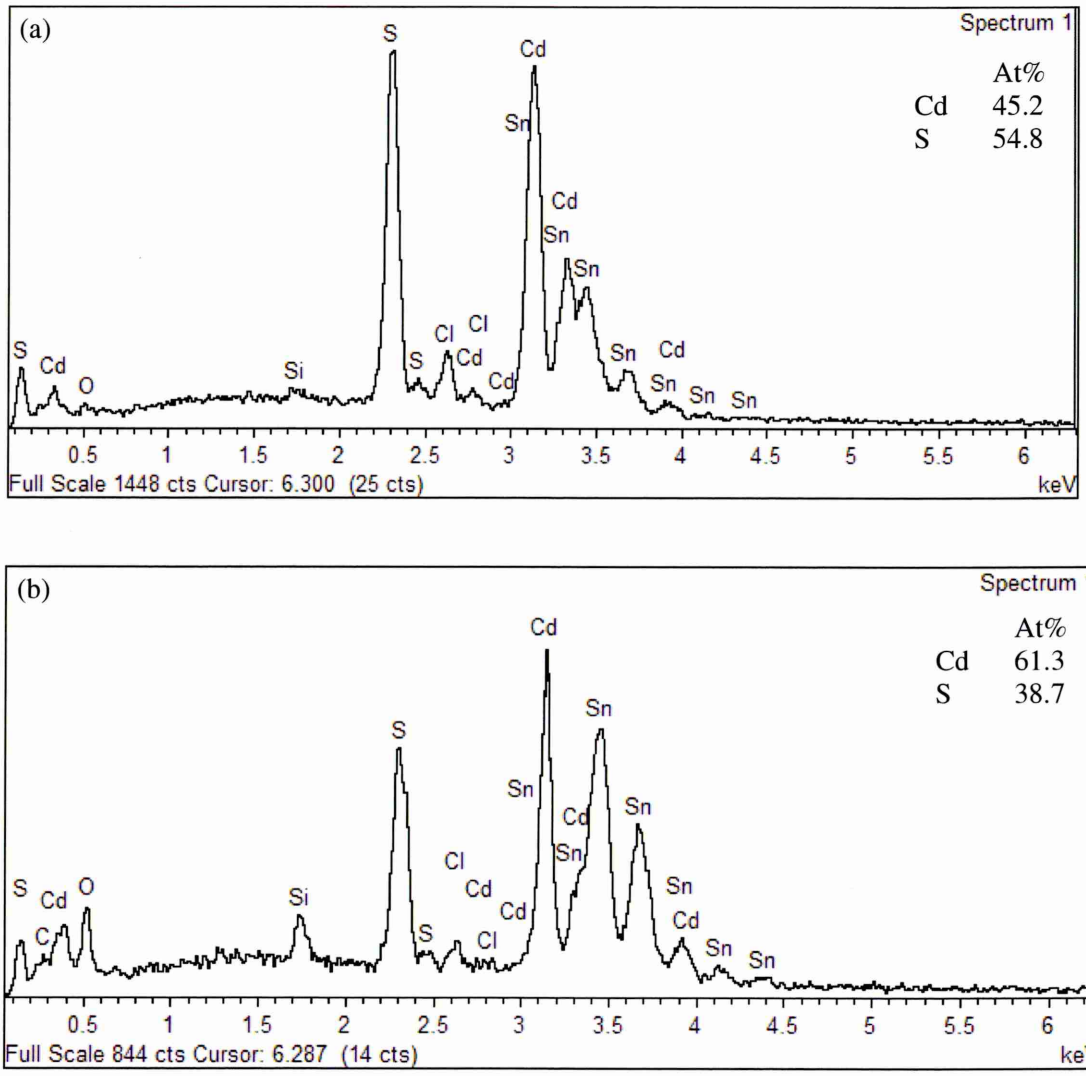


Figure 4.10: EDX spectra of the as-deposited CdS thin films grown at V_g (a) 1200 mV and (b) 1500 mV.

4.1.8 Conclusion

The growth voltage and growth temperature for electrodeposition of CdS thin films have been studied. The voltage range for deposition has been estimated by a cyclic voltammogram scanning from 0 to 2000 mV. The study on the growth voltage has been narrowed down to 1440-1460 mV and the deposition temperature varied from 25 to 85°C. The optimum V_g and temperature were obtained at 1455 mV and 85°C, respectively.

4.2 Study the effect of annealing temperature and time on CdS thin films

This section discusses the study on annealing conditions and includes annealing temperature and time for CdS thin films. In this experiment, one large substrate (6.0×3.0 cm^2) of glass/FTO was electrodeposited at V_g and T_g of 1455 mV and 85°C, respectively. This layer was grown for longer time (30 min.) to achieve thicker layer. This substrate was cut into six pieces. One of the pieces is set aside as a reference sample (as-deposited) while the others were annealed in air at temperatures of 250, 350, 400, 450 and 550°C. In the second part of this section, the best annealing temperature was chosen to study the effect of annealing time from 10, 20, 30 and 60 minutes. The purpose of this work is to optimise the annealing temperature and time for CdS thin films. All of the samples were characterised for their structural, optical, thickness, electrical, morphological and compositional properties using XRD, UV-Vis spectroscopy, optical profilometry, DC conductivity measurement, SEM and EDX.

4.2.1 Structural characterisation

Figure 4.11 shows the XRD spectra of CdS layers for as-deposited and annealed at 250, 350, 400, 450 and 550°C. The XRD spectra show a noticeable peak of (002) hexagonal peak, which overlaps with FTO peak at 2θ=26.72°, which in turn increased with higher temperature, but deteriorates after annealing at 550°C. Also, the two peaks of (100) and (101) hexagonal CdS at 2θ = 25.15° and 28.53° became more pronounced as annealing temperature increased but diminished after being annealed at 550°C. The annealing process usually improved the crystallinity due to the well-organised atomic arrangement and enlargement of the crystallite size [9]. However, the too high annealing temperature may cause oxidation, cracks formation, deterioration and sublimation of the material. Also the (220) cubic CdS peak at 2θ=45.15° started to disappear at temperature ≥400°C. Therefore it is suggested that the phase transition from the mixture of cubic and hexagonal phase to a single hexagonal phase appeared at a temperature in between of 350-400°C.

The XRD spectra for CdS thin films annealed at 400 and 450°C with different time duration are shown in Figures 4.12(a) and (b) respectively. The annealing time varied from 10, 20, 30 and 60 minutes. It shows that the three peaks of (100), (002) and (101) hexagonal CdS in both graphs increased as the annealing time increased from 10 to 20 minutes and deteriorated with further annealing time (≥30 minutes). The

deterioration of the crystallinity peak is so obvious for CdS films annealed at 450°C. This work suggests that the annealing time of CdS also has a limitation up to 20 minutes. Further annealing time (≥30 minutes) may cause a material deterioration and thus reduce the crystallinity peak in the XRD pattern.

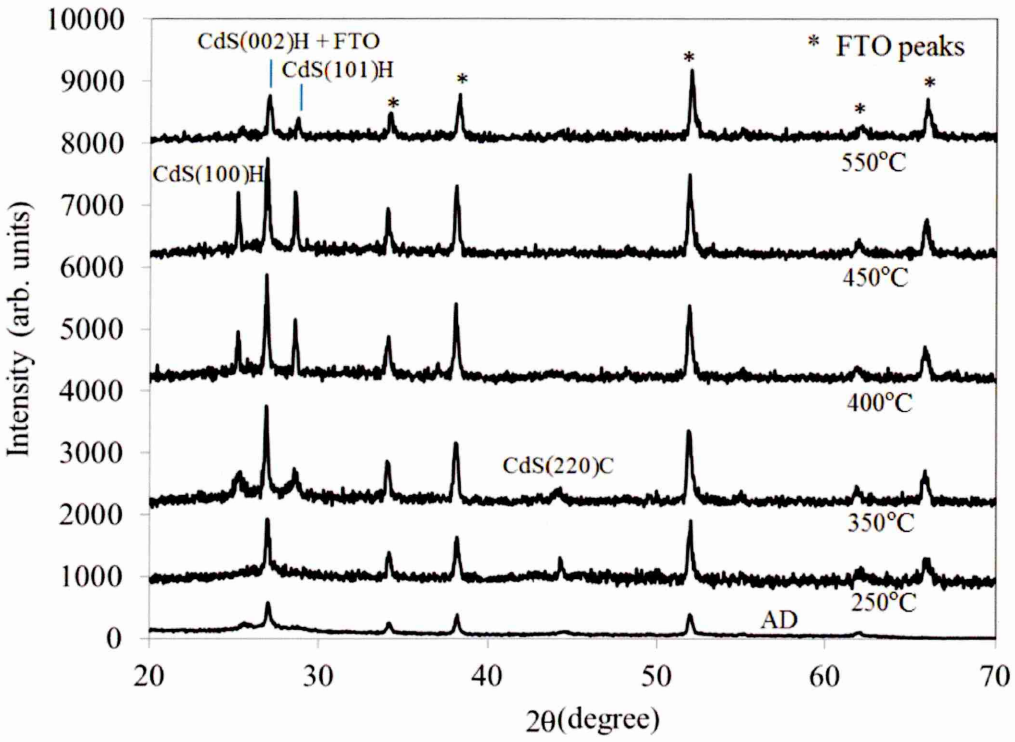


Figure 4.11: XRD spectra of CdS thin films with different annealing temperature.

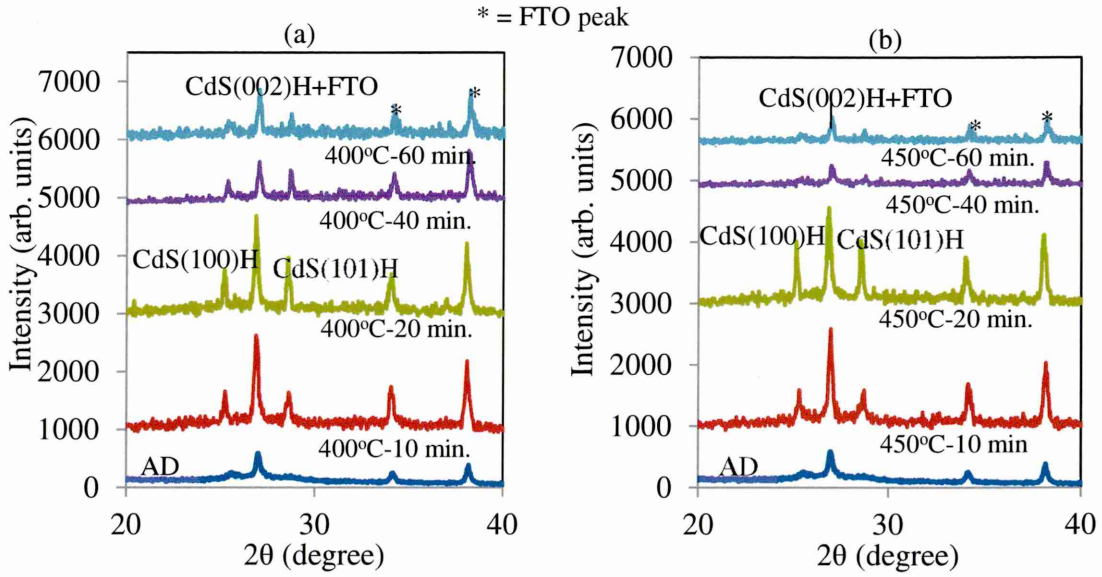


Figure 4.12: XRD spectra of CdS thin films annealed at (a) 400°C and (b) 450°C with different annealing durations.

4.2.2 Optical characterisation

The optical absorption and transmittance spectra of CdS thin films as a function of annealing temperatures are shown in Figure 4.13 while the summary of these measurements are shown in Table 4.4. The physical appearance of CdS with different annealing temperature is displayed in Figure 4.14. As mention earlier, the CdS layers were purposely grown for longer time. Therefore it shows a dark green appearance with a lower bandgap and transmittance due to the high absorbance and thicker layer. The darker layer in appearance also could be attributable to the incorporation of elemental Cd. Annealing process forms CdS by combining elemental Cd and S and CdO with bandgap of 2.20 eV. However, XRD data in this experiment only shows peaks of CdS instead of CdO. The increasing in annealing temperatures reduced the absorbance and the gradient of the absorbance curves in optical spectra. It is also observed that the energy bandgap and transmittance increased as the thickness of the layer reduced caused by an increment in annealing temperature. Also the transmittance is strongly affected by the quality of absorption and reflection loss associated with the FTO surface. This can be seen in Figure 4.13 (c) and (d). The FTO interface between of CdS layer and glass reduced light transmittance because of reflection loss in the range of ~0.8%. If the reflectivity loss is reduced completely, the transmittance of CdS can be improved.

A low absorbance, high transmittance and larger bandgap are the suitable criteria for high-quality window layers in solar cells [15, 17]. The reduced in absorbance with annealing temperature in this study could be due to the grain growth which forming larger unfilled inter-granular volume and reduced the absorption per unit thickness [2]. However, the loss of material through sublimation, thinning down the layer and, as such at too high annealing temperature also can result in more transparent properties as shown in Figure 4.14 [18]. Therefore annealing process of CdS layers should be limited up to 400°C in order to avoid the deterioration or sublimation of the materials.

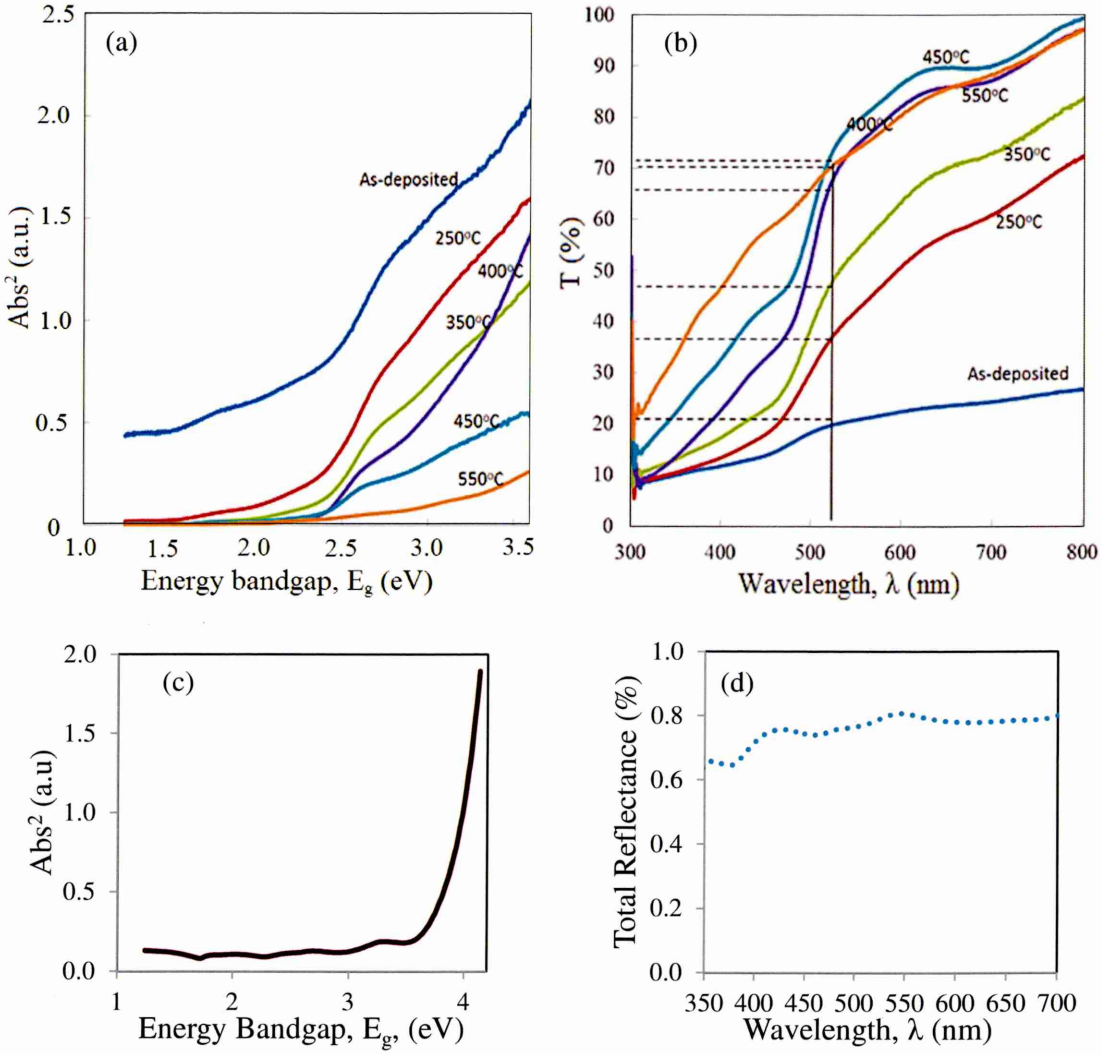


Figure 4.13: The variation of (a) Optical absorbance and (b) Optical transmittance of CdS layers with different annealing temperatures and (c) and (d) are the optical absorption and total reflectance of the glass/FTO substrate.

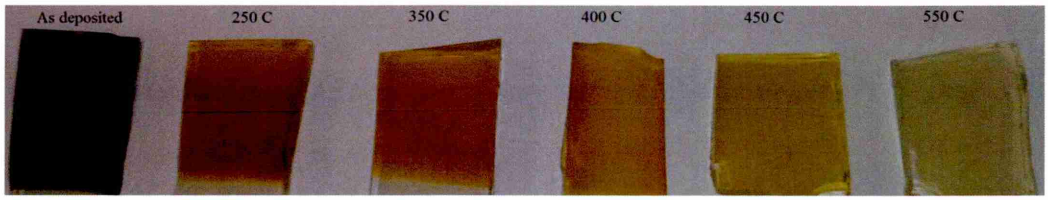


Figure 4.14: The physical appearance of the CdS thin films for as-deposited and after annealed at different temperatures.

Table 4.4: The optical properties of CdS layers annealed at different temperatures.

Annealing Temp (°C)	E_g (eV)	T (%)
As-deposited	2.03	19
250	2.25	35
350	2.33	46
400	2.42	66
450	2.42	70
550	2.45	73

4.2.3 Thickness measurement

The thicknesses of CdS layers after annealed at different temperatures were measured using an optical profilometer since the calculation of Faraday's formula is invalid once the electrodeposited film has annealed or been treated with other chemicals. The measurement of each sample was carried out three times at different film areas in order to get an accurate average thickness. Figure 4.15 shows the graph of the average thickness measurements versus annealing temperatures. It shows that the thickness has reduced slightly from 400 nm (as-deposited) to ~350 nm when it was annealed at 350°C. The thickness shows rapid decline to ~200 nm at a temperature range of 450-550°C, which is due to the sublimation of material at too high temperatures [18]. Therefore the annealing of CdS layers in air should be limited to a temperature of 400°C, in order to avoid loss of the material.

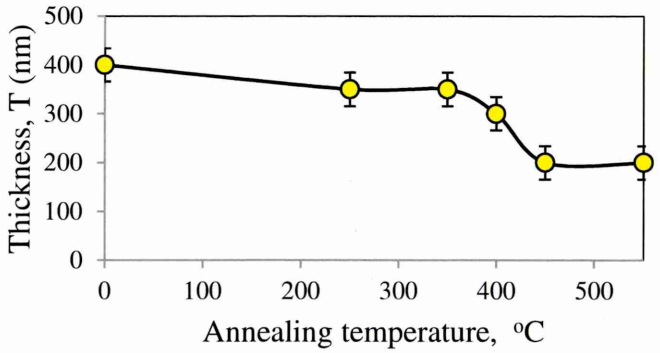


Figure 4.15: Thickness of CdS layers as a function of annealing temperatures.

4.2.4 Electrical characterisation

DC conductivity measurements were carried out to study the effect of annealing on the electrical conductivity of CdS layers. 2 mm diameter and circular ohmic contacts were made by evaporating Al through a metallic mask. The resistance of FTO/CdS/Al structures were measured using I-V characteristics. The electrical conductivity (σ) and resistivity (ρ) were calculated with known thicknesses of the CdS layer.

Table 4.5 summarises the measurements of average resistance, electrical resistivity and conductivity of CdS layers as a function of the annealing temperature. It shows that the value of conductivity decreases as the CdS films were annealed at higher temperatures. Many researchers, however, reported the increasing in conductivity of CdS after annealing [9,10,19]. This behaviour is expected in polycrystalline semiconductors due to the improvement of crystallinity. However, Preusser and Cocivera have reported the decreases in conductivity of CdS after annealing [20]. The decrease in conductivity of CdS thin films with higher annealing temperatures in Figure 4.16 (b) is probably due to the oxidation, loss of material and diffusion of Na from glass to CdS layer. As shown in Figure 4.15, the thickness of CdS decreases after ~400°C due to the loss of material, therefore reducing the electrical conductivity. Many researchers report that the diffusion coefficient of Na depends on several factors such as glass composition, dopant, annealing temperature, time and environment [21-23]. Tian et al. reported in their paper that the diffusion of Na in glass occurred in the temperature range between 250 and 1000°C [21] while Smedskjaer et al. observed the Na inward diffusion at 575°C [22]. Earlier, Osaka et al. reported a drastic increment of the electrical resistance when the Na ions start diffusion from the substrate to the films [23]. If we observe the data in Table 4.5 and the graph shown in Figure 4.16(a), the electrical resistance of CdS increased exponentially with an annealing temperature. With this

observation we believed that heat treatment temperature above 450°C is closed to the activation enthalpy point for sodium out-diffusion. Therefore we suggest that 400-450°C is an optimal processing temperature for CdS thin films. It should be noted that the impurity distribution in CdS layers are also different for different growth methods. Therefore, the final electrical conductivity will also depend on the impurities present in those material layers.

Table 4.5: The summary of electrical properties of CdS thin films annealed at different temperatures.

Annealing temperatures (°C)	Average Resistance (Ω)	Resistivity, ρ x 10^5 (Ωcm)	Conductivity, σ x 10^{-6} $(\Omega cm)^{-1}$
As deposited	34.4	0.30	33.33
250	115.3	1.03	9.67
350	188.5	1.69	5.19
400	212.0	2.22	4.51
450	256.4	2.46	4.07
550	396.1	6.25	1.61

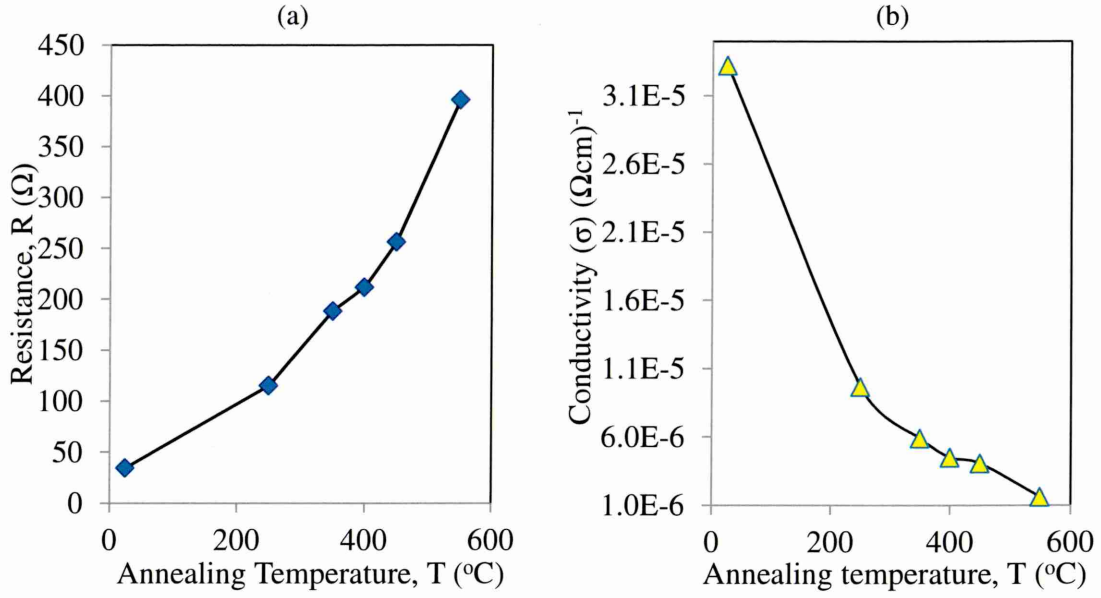


Figure 4.16: The (a) average resistance and (b) electrical conductivity of CdS layers as a function of annealing temperature.

4.2.5 Morphological characterisation

Figure 4.17 shows the SEM images of CdS thin films for as-deposited and annealed at 400 and 450°C for 10, 20 and 30 minutes. As can be seen from Figure 4.17(a), the average grain size of as-deposited CdS thin film is around 200-300 nm with a clear appearance of small crystallites coalesced inside a grain. CdS thin film annealed at 400 and 450°C for 10 minutes does not show any obvious increments of the grain sizes, but CdS film annealed at 400°C for 10 minutes shows a compact grain growth with less gaps as compared to CdS annealed at 450°C for 10 minutes. CdS thin films annealed for 20 minutes at both temperatures show slight enlargement of the grain sizes in a range of 300-400 nm. This is due to the coalescence of smaller nano-crystallites into larger clusters. The change in microstructure has been attributed to the transformation of a mixed hexagonal and cubic phase into a single hexagonal phase (from XRD) after heat treatment as well as re-crystallisation [9,13]. However, prolong annealing is not helpful since it may introduce cracks, voids or disintegration of the material layer. This has been verified by the SEM images of CdS layers in Figures 4.17 (d) and (g). The CdS layers annealed for 30 minutes demonstrate the presence of voids in between grains. Also, large grain sizes but with the existence of cracks are observed for CdS film annealed at 450°C for 30 minutes. Larger grain size is good for electron mobility in a solar cell, however the presence of voids and cracks in the CdS is unhealthy since these will create leakage paths to the FTO layer. Therefore, the conclusion is that the annealing time of CdS should not be more than 20 minutes in order to avoid cracks and material disintegration.

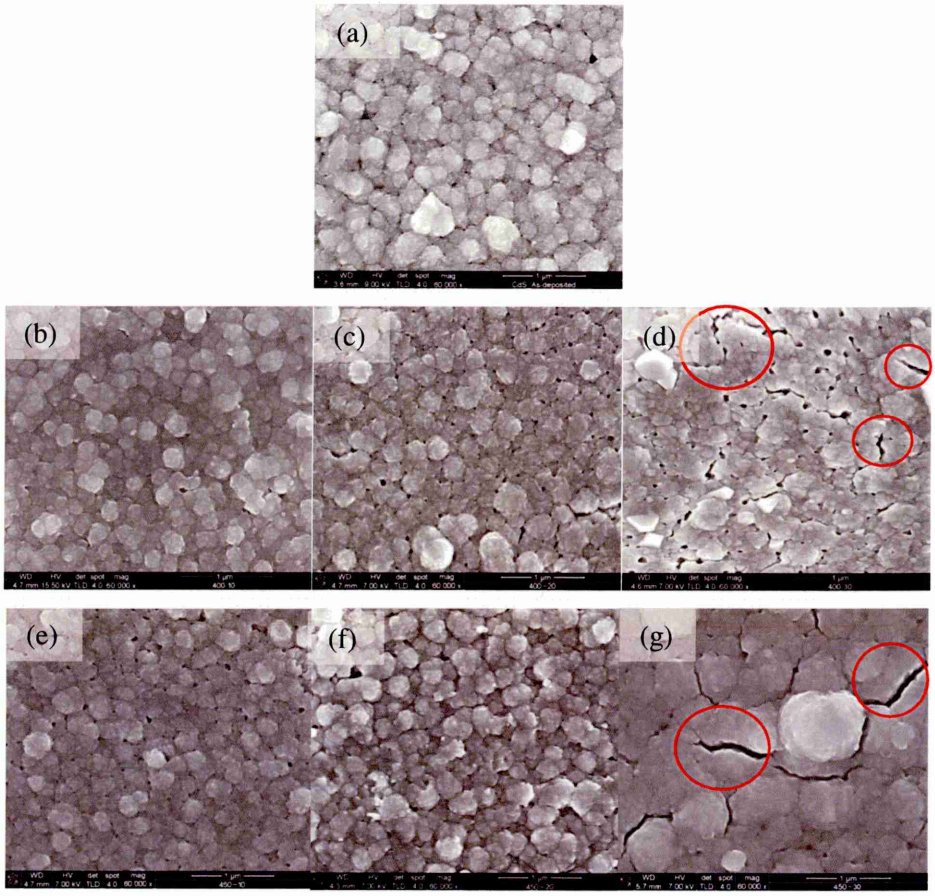


Figure 4.17: The SEM images of CdS thin films for (a) as-deposited and annealed at temperature of 400°C for (b) 10, (c) 20 and (d) 30 minutes and temperature of 450°C for (e) 10, (f) 20 and (g) 30 minutes.

4.2.6 Compositional characterisation

The EDX measurement has been used to confirm the composition or the atomic percentage of CdS thin films. Figure 4.18 shows the EDX spectra of CdS thin films for as-deposited and annealed CdS at 400°C for 20 minutes. The spectra indicate the presence of both Cd and S atoms as expected. The peaks also show the presence of O, Si and Sn, which come from the underlying substrate (glass) and conducting layer (FTO) on which these CdS layers were grown. The percentage atomic concentrations of Cd and S in these samples are presented in Table 3. It is observed that the as-deposited CdS is Cd-rich. This trend is associated with the previous observation in optical characterisation and physical appearance of the as-deposited CdS. The annealed CdS shows almost balance concentration of Cd and S in the layer, which revealed that the un-reacted cadmium has diffused during the annealing process and created more stoichiometric material after annealing.

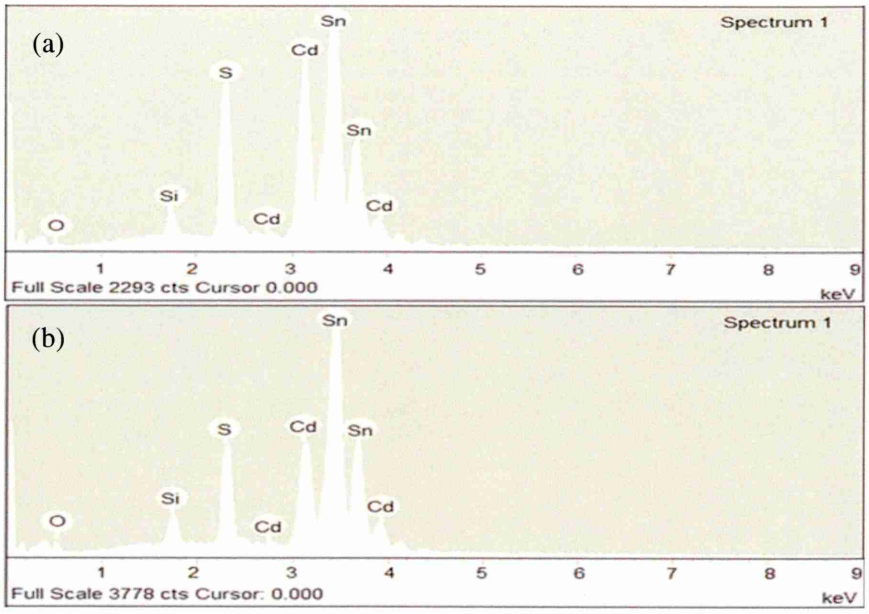


Figure 4.18: EDX spectra for (a) as-deposited and (b) annealed of CdS thin films.

Table 4.6: Composition percentage of Cd and S in CdS thin films for as-deposited and after annealing at 400°C for 20 minutes.

Sample	Atomic composition %		Cd/S ratio
	Cd	S	
As-deposited	53.6	46.4	1.16
Annealed at 400°C for 20 minutes	50.7	49.3	1.03

The binary phase diagram of the CdS system, adapted from references [23,24], is shown in Figure 4.19. In this diagram, solid and liquid phases are described. The melting point of pure intrinsic CdS is ~1405°C. The melting point of Cd-rich CdS is ~321°C, so all Cd-rich CdS compounds will exhibit some level of liquid phase above ~321°C. Likewise, S-rich CdS shows 2 solid phases, α- and β-. The melting point for α- is at ~95°C and melting point for β- phase is ~115°C. The liquidus temperature of S-rich CdS is observed at 1000°C. In this work, the CdS thin films have been annealed at different temperatures from 250 °C to 550°C in order to provide different crystal growth rates and better stoichiometric phase of CdS. EDX analysis suggests that the as-deposited CdS thin films are slightly enriched in Cd which would support the presence of some liquid and solid phases at temperatures above 321°C. But, there is no direct evidence supporting the involvement of some level of liquid-solid phase sintering

during annealing off-stoichiometric CdS ratio, therefore it cannot be discounted. Previous study also showed the dark physical appearance of CdS film due to the Cd-richness. Annealing process must be helping to produce stoichiometric CdS from un-reacted elements and also forming CdO.

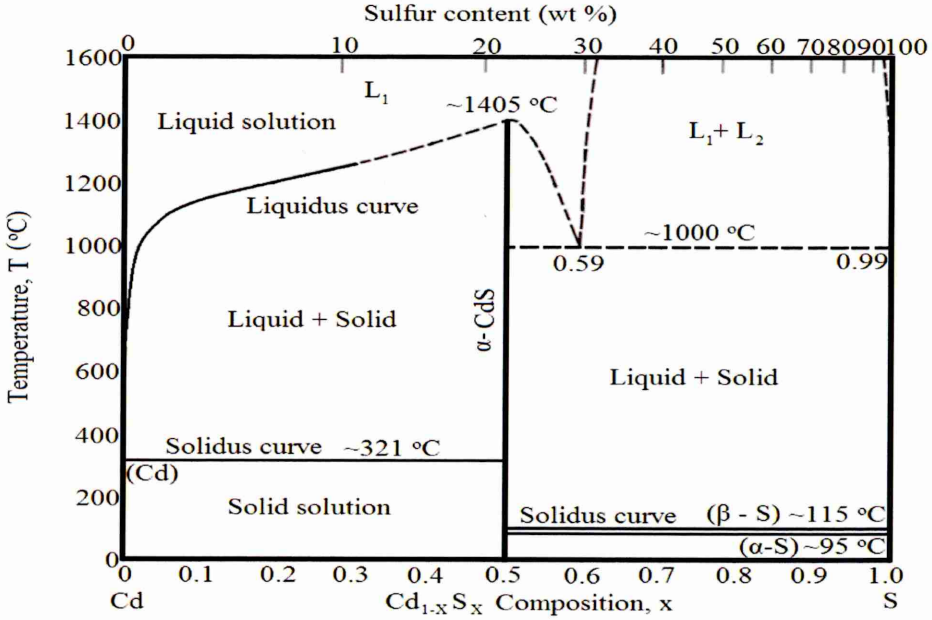


Figure 4.19: The phase diagram of CdS [23,24].

4.2.7 Conclusion

The annealing temperature and time for CdS thin films have been studied at 250, 350, 400, 450 and 550°C and at 10, 20, 30 and 60 minutes respectively. XRD studies show an improvement of crystallinity with annealing temperature and time but these two parameters have their limitations. The too-high annealing temperature and too-long annealing time deteriorate the crystallinity of the CdS films. The highest crystallinity is observed for a sample annealed at 450°C for 20 minutes. The bandgap energies reach that of bulk standard value (2.42 eV) after CdS thin films were annealed. CdS thin film shows improved transmission with higher annealing temperature. Thickness measurement shows rapid decline to ~200 nm at a temperature range of 450-550°C, which was due to loss of material through sublimation. The electrical conductivity measurement demonstrates a reduction with higher annealing temperature, which is caused by a thickness reduction, oxidation, loss of material and diffusion of Na from the substrate at higher temperature. The morphological study from SEM shows an improvement of grain size with higher annealing time, however cracks and voids form

if the layers were annealed at 400 or 450°C for prolonged periods greater than 30 minutes. EDX study demonstrated that the sample became more stoichiometric after annealing. From this work, it suggests that the good annealing temperatures and time for decent CdS layers are those annealed at 400 and 450°C for 20 minutes. Further than this, the CdS will experience deterioration due to cracks, voids, loss of material and oxidation.

4.3 Study the effect of chemical treatments on CdS thin films

In this particular work, two kinds of chemicals were prepared for the surface treatment on the electrodeposited layer. These are saturated $CdCl_2$ and a mixture of $CdCl_2$+CdF_2. Initially the CdS layer was electrodeposited on a glass/FTO sample with the area size of 4.0×3.0 cm^2. The CdS sample was cut into four pieces. One of the pieces was kept as a reference sample (as-deposited) while the others were annealed in air without chemical treatment, annealed with $CdCl_2$ and $CdCl_2$+CdF_2 treatment. The details of the samples are shown in Table 4.7. The annealing process was carried out at 400°C for 20 minutes. The purpose of this work was to study the effect of chemical treatments on CdS thin films and to get some idea of which treatment is better for developing CdS for solar cell fabrication. A comparative study was carried out on these samples by characterising their structural, optical, thickness, electrical and morphological properties by using XRD, Raman spectroscopy, UV-Vis spectroscopy, optical profilometry, DC conductivity measurement and SEM.

Table 4.7: The descriptions of CdS thin films with different condition of treatments.

Sample identifier	Sample detail
AD	As-deposited CdS thin film
HT	CdS thin film annealed in air at 400°C for 20 minutes
CC	CdS thin film annealed with $CdCl_2$ treatment at 400°C for 20 minutes
CF	CdS thin film annealed with $CdCl_2$+CdF_2 treatment at 400°C for 20 minutes

4.3.1 Structural characterisation

Structural characterisation in this work was carried out by XRD and Raman spectroscopy. Figure 4.20 shows the XRD spectra for samples AD, HT, CC and CF.

The as-deposited CdS film shows a small peak of (100) and (101) hexagonal CdS at 2θ=25.15° and 28.53° and the highest peak of (002) hexagonal, which overlaps with FTO at 2θ=26.72°. Also there is a very small peak corresponding to (220) cubic CdS. This shows the poor crystallinity of AD CdS layers. This includes elemental Cd and S, in addition to CdS. All the (100), (101) hexagonal peaks and the (220) cubic peaks increased after annealing without any chemical treatment. This could be due to the formation of the CdS by reacting elemental Cd and S which result in the change of colour in physical appearance observed in Figure 4.14.

CdS film annealed with $CdCl_2$ shows an increment of both the (100) and (101) peaks, but a peak corresponding to (220) cubic CdS disappeared. The presence of $CdCl_2$ has improved in crystallinity and induced the phase transformation from the mixture of cubic and hexagonal phases to the single hexagonal phase [26].

When the CdS film was annealed with $CdCl_2$+CdF_2 the new peak appeared at 2θ=47.85°, which corresponds to the (103) hexagonal peak. At the same time the intensity of (100), (002) and (101) peaks decreased but the FWHM decreased for (002) peak. This suggests that the presence of a small amount of fluorine in $CdCl_2$+CdF_2 treatment has improved crystalline nature in the material and the preferential orientation was reduced as the hexagonal structure content increased [27].

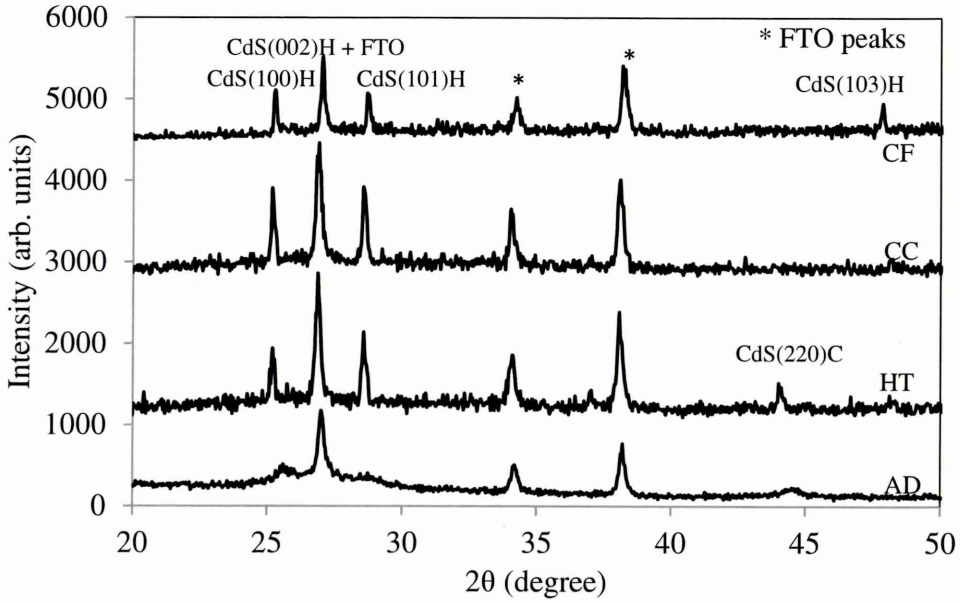


Figure 4.20: XRD spectra of CdS with different chemical treatments followed by annealing at 400°C for 20 minutes.

Raman spectroscopy is an alternative method that can identify material phases and determine the degree of crystallinity of the thin films. Figure 4.21 shows the Raman spectra for as-deposited, annealed without any chemical treatment, annealed with $CdCl_2$ and annealed with $CdCl_2$+CdF_2 after normalising. The dominant peaks in the spectra are the longitudinal optical (LO) vibration mode at wave numbers ~305 cm^{-1} for 1LO and ~605 cm^{-1} for 2LO. It is observed that all the samples show clear peaks at 1LO with a slight blue shift in peak positions after annealed with and without chemical treatment. $CdCl_2$+CdF_2 treated CdS shows the highest blue shift on both 1LO and 2LO peaks. Raman blue shift correspond s to the increasing of energy of scattered photons from the materials due to changing in material structure, and the peak will be shifted to higher wavenumber. [28]. Ichimura et al. reported that the increase of Raman shift is due to enlargement in crystallite size [29]. The FWHM of Raman spectra is also used to qualitatively evaluate the crystallinity of CdS. The sample annealed with $CdCl_2$ shows a decrease in the FWHM of 1LO and 2LO peaks, which also proves that the enhancement of crystallinity appeared after it was annealed with the presence of $CdCl_2$ [30].

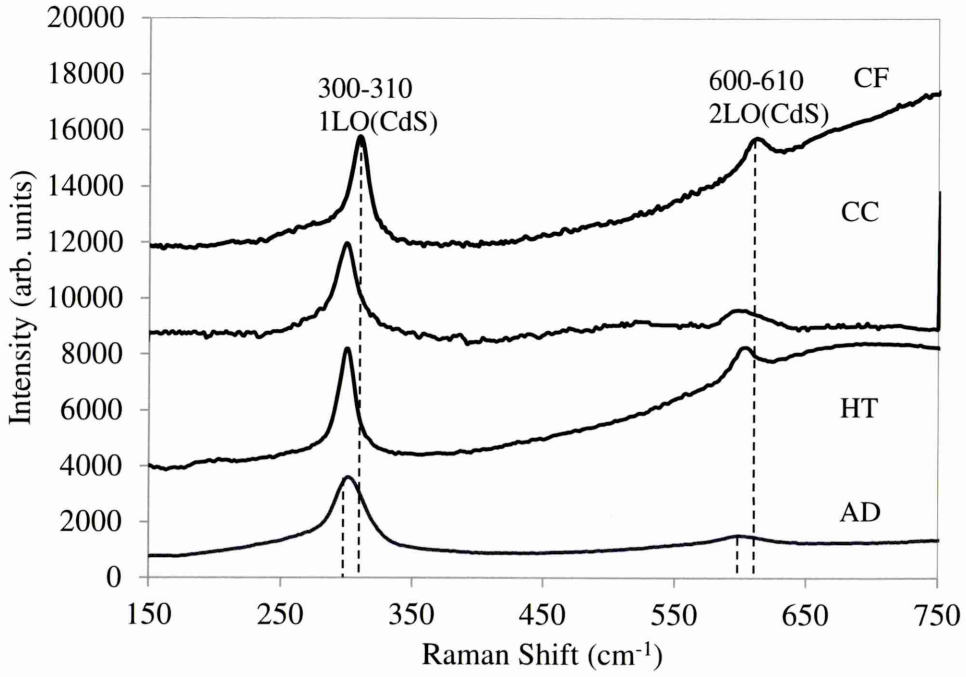


Figure 4.21: Raman spectra of CdS for as-deposited and with different chemical treatments followed by annealing at 400°C for 20 minutes.

4.3.2 Thickness measurement

Figure 4.22 shows the average thicknesses of CdS layers measured by an optical profilometer. These measurements were carried out three times in order to get the accurate value. As we discussed in Section 4.2.3, the thickness of CdS decreased with increasing annealing temperature in the air due to the sublimation of the materials [18]. Similarly from this result, it is observed that CdS annealed in air without any chemical treatment caused more material loss than those annealed with chemical treatments. It could be due that the presence of chemical treatment such as $CdCl_2$ and/or CdF_2 on the top of CdS surface protect the layer during annealing process.

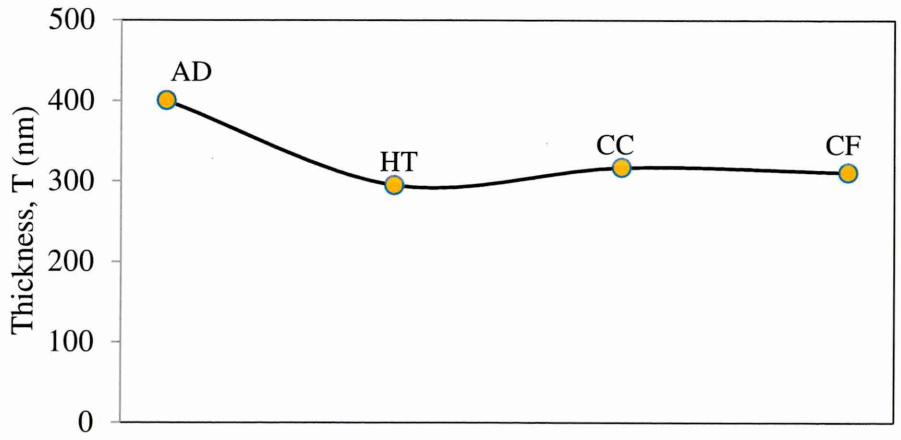


Figure 4.22: The thickness measurement of CdS thin films for as-deposited and annealed with different chemical treatments at 400°C for 20 minutes.

4.3.3 Electrical characterisation

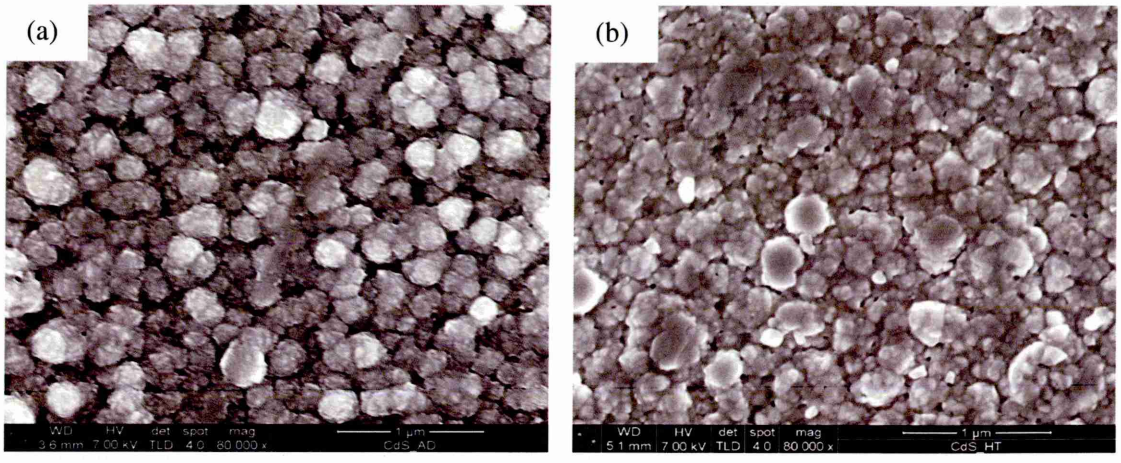
The electrical properties of these samples are characterised using D.C. conductivity measurements and are shown in Table 4.8. The conductivity of as-deposited CdS is 33.33 $\Omega^{-1}cm^{-1}$. The value is reduced dramatically from 33.33 to 4.51 $\Omega^{-1}cm^{-1}$ after it was annealed in air. The reason for this occurrence has been discussed in section 4.2.4. CdS annealed with $CdCl_2$ treatment and $CdCl_2$+CdF_2 treatment also shows a reduction of conductivity compared to as-deposited CdS. However, the reductions are much smaller than those of annealed without any chemical treatment. It is understood from the EDX characterisation in section 4.2.6 that the sulphur in CdS film has diffused after being annealed without any chemical treatment in air. The sulphur vacancies and Cd interstitials are typically known as intrinsic donor defects [30]. During the annealing process, the oxygen from the surroundings absorbed and filled the sulphur vacancy and thus removed the donor site and this resulted in a drastic reduction in conductivity since the carrier concentrations are reduced [31]. With the presence of $CdCl_2$ or $CdCl_2$+CdF_2 treatment during the annealing process the absorbed oxygen is equalised by the excess carriers provided by the chemical treatment; therefore, the decrease in conductivity are fewer. CdS film annealed with $CdCl_2$ shows slightly better conductivity than CdS film annealed with $CdCl_2$+CdF_2.

Table 4.8: The summary of electrical properties of CdS thin films annealed with different chemical treatments.

Sample	Average Resistance (Ω)	Resistivity, ρ x 10^5 (Ωcm)	Conductivity, σ x 10^{-6} $(\Omega cm)^{-1}$
AD	34.4	0.30	33.33
HT	212.0	2.22	4.51
CC	42.8	0.41	24.57
CF	58.1	0.61	16.45

4.3.4 Morphological characterisation

CdS thin films for AD, HT, CC and CF are shown in Figure 4.23. The as-deposited CdS shows the appearance of small crystallites coalesced together, which form grains with size in the range 200-300 nm. The CdS annealed in air also shows a clear crystallite inside the grains but the crystallite size is slightly larger. CdS annealed with $CdCl_2$ treatment also shows a larger crystallite size and still coalesces together, forming larger grains. During $CdCl_2$ treatment, it was reported that chlorine diffuse into grain boundaries and create recrystallisation and larger crystallites [32,33]. CdS thin film annealed with $CdCl_2$+CdF_2 treatment shows solid grains without an appearance of crystallites. These grains originate from small crystallites and enlarge during $CdCl_2$+CdF_2 treatment. The grain size observed in this material is quite smaller and different to others. The presence of a small quantity of fluorine during heat treatment has performed exclusive treatment since fluorine has a smaller atomic radius than chloride; thus, it can diffuse more easily through grain boundaries than chloride and perform better treatment [34,35]. This clearly shows the effect of fluorine in improving the crystallinity of CdS layers. As demonstrated later in this thesis, the effect of fluorin is clearly shown in enhancing the performance of CdS/CdTe solar cells.



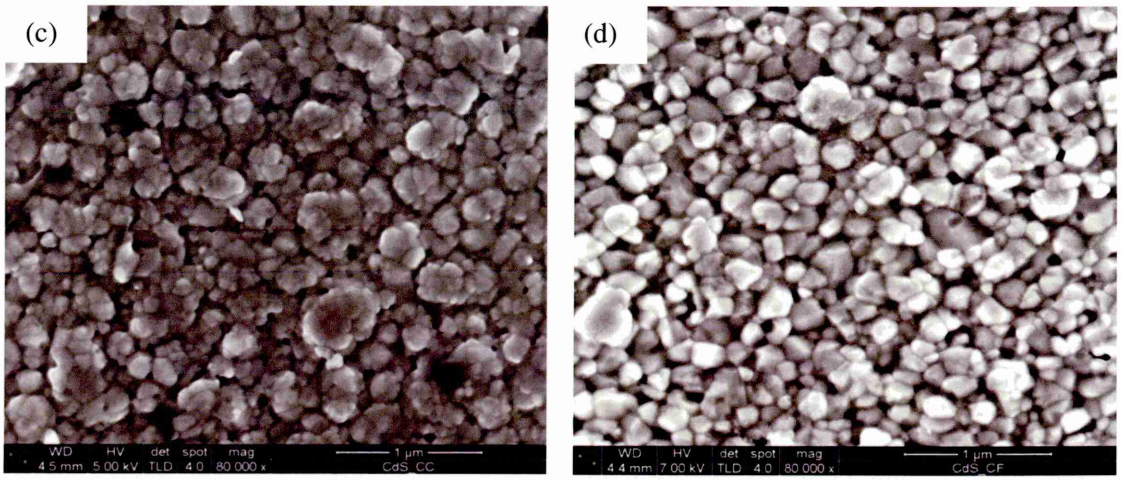


Figure 4.23: The SEM images of CdS thin films for (a) as-deposited, (b) annealed in air without any chemical treatment, (c) annealed with $CdCl_2$ and (d) annealed with $CdCl_2$+CdF_2.

4.3.5 Conclusion

CdS thin films have been studied with different chemical treatments prior to annealing process. XRD studies show an enhancement of crystallinity after being annealed with $CdCl_2$ treatment. The phase transformation from mixture of hexagonal and cubic (in as-deposited) to only hexagonal was also observed after the CdS annealed with $CdCl_2$ treatment and $CdCl_2$+CdF_2 treatment. $CdCl_2$+CdF_2 treated CdS shows the appearance of additional (103) hexagonal peak and elimination of (002) peak, indicating improved crystallinity. The highest crystallinity is observed for sample annealed with $CdCl_2$. Raman spectroscopy studies demonstrated a blue shift on the 1LO peak, which suggests an enlargement in crystallite size and this result is in good agreement with the SEM result. The presence of a small amount of fluorine in $CdCl_2$+CdF_2 treatment enhances the recrystallisation and crystallite growth since fluorine has a smaller atomic size and a higher diffusivity than chlorine. Electrical measurements show a drastic reduction in conductivity for CdS annealed in air most probably due to formation of CdO on the sample. Both CdS annealed with $CdCl_2$ and $CdCl_2$+CdF_2 treatments also show reduction in conductivity, but the reductions are slightly smaller than those annealed in air. From this work, it suggests that the CdS layers annealed with the chemical treatments created better properties than CdS annealed without any chemical treatment. Further studies on this have been expanded in solar cell fabrication and characterisation and are presented in section 7.1.1 in Chapter 7.

4.4 Study the effect of sulphur concentrations in the CdS electrolyte

This section presents a brief study on sulphur concentrations in the CdS electrolyte. Four different CdS electrolyte containing sulphur to cadmium (S/Cd) ratio of 0.1, 0.2, 0.5 and 1.0 were prepared in this study. $(NH_4)_2S_2O_3$ concentrations ranged from 0.03 M to 0.30 M were added to 0.30 M $CdCl_2$ in 300 ml of deionised water. The pH and bath temperature was maintained at 2.00±0.02 and 85°C, respectively. The details of these solutions are shown in Table 4.9. The CdS thin films produced from each electrolyte were studied for their structural, optical, thickness and morphological properties using XRD, UV-Vis spectroscopy, optical profilometry and SEM measurements.

Table 4.9: The summary of various concentrations used in CdS precursors.

Samples	$CdCl_2$ concentration (M)	$(NH_4)_2S_2O_3$ concentration (M)	S/Cd Ratio
R0.1	0.30	0.03	0.1
R0.2	0.30	0.06	0.2
R0.5	0.30	0.15	0.5
R1.0	0.30	0.30	1.0

4.4.1 Structural characterisation

Figure 4.24 shows the XRD measurement of the as-deposited CdS thin films with variation of sulphur concentration. Although all of these samples were grown at the same deposition time, but the thickness of each layers are different since the growth rate for each electrolyte is different. The dominant peak of hexagonal CdS overlaps with FTO is observed in all spectra and the peak intensities increased slightly with higher S/Cd ratio up to 0.5. This is due to the thicker layer since the growth rates of CdS are increased as the S/Cd ratio increased. The small peaks of (100) and (101) hexagonal CdS peaks also observed on samples R0.2, R0.5 and R1.0 together with a small hump of (220) cubic CdS peak on samples R0.5 and R1.0.

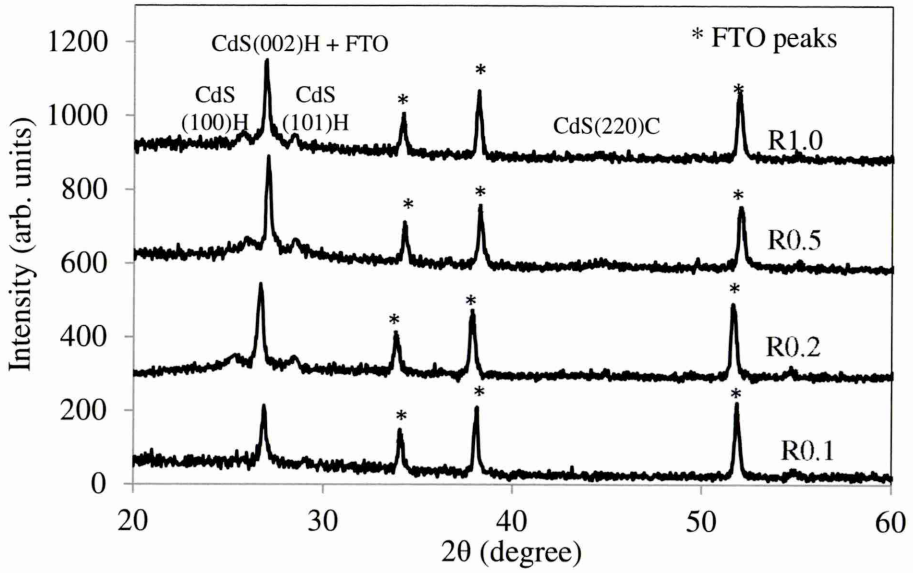


Figure 4.24: The XRD spectra of CdS thin films grown with different S concentrations in a CdS bath at 1455 mV, 85°C for 60 minutes.

4.4.2 Optical characterisation

The optical absorption and transmittance of CdS films with different S/Cd ratios are shown in Figures 4.25 (a) and (b) respectively. The bandgap value and transmittance at wavelength ≥520 nm obtained from these graphs are shown in Table 4.10. These results show that the bandgap of CdS are reduced from 2.50 to 2.43 eV with an increasing S/Cd ratio. Sample grown from higher sulphur (R1.0) shows the lowest transmittance due to the high thickness and a formation of cloudy layer. From the observation during the experiment, too much sulphur in the electrolyte created sulphur precipitation with the yellowish particle inside the solution. This can be seen in Figure 4.26. It is assumed that the formation of cloudy surface might be due to this fact. Therefore, the electrolyte with too much sulphur is not recommended in order to produce a healthy window layer for a solar cell device.

Table 4.10: The bandgap and transmittance values of CdS films grown from electrolytes with different S:Cd ratios.

Samples	Energy bandgap, E_g (eV)	Transmittance, T (%)
R0.1	2.50	97
R0.2	2.45	78

R0.5	2.42	62
R1.0	2.43	53

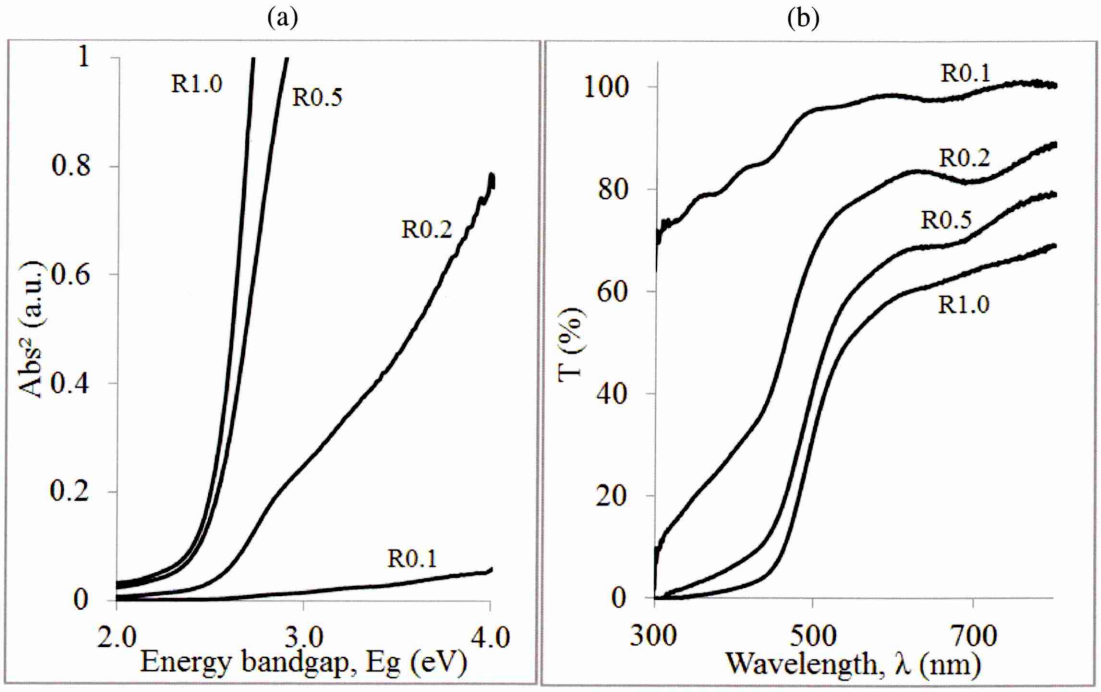


Figure 4.25: Optical (a) absorption and (b) transmittance spectra of CdS thin films grown with a variation of S/Cd ratio.

(a) (b)

Figure 4.26: Images of (a) CdS electrolytes with S/Cd ratio of 0.1, 0.2, 0.5 and 1.0 and (b) an image of sulphur precipitation in an R1.0 bath.

4.4.3 Thickness measurement

The thickness of CdS grown in this work has been calculated from Faraday's equation and measured by optical profilometry. Both figures from calculations and measurements show a similar trend. It is expected that the thickness of CdS should be increased with the increasing of the S/Cd ratio. However, the CdS layer R1.0 shows lesser thickness than the thickness of sample R0.5. The current density growth also shows the reduction of deposition rate in the electrolyte R1.0. This is because of too much sulphur in the CdS electrolyte, which may produce a resistive bath due to sulphur precipitates. From the observation in this research, an ideal deposition rate for a good quality and uniform CdS layer is about 150-200 mA cm^2. Therefore, it suggests that electrolyte R0.2, which contained 0.3M $CdCl_2$ and 0.06M $(NH_4)_2S_2O_3$, is more suitable to grow CdS thin films for solar cell devices.

Table 4.11: The comparison of CdS films thickness from calculation and measurements.

Samples	Average current density growth, J_g ± 1 (μA cm^2)	Film thickness	
		Faradays law equation ± 1 (nm)	Optical profilometry ± 100 (nm)
R0.1	70	380	400
R0.2	128	532	600
R0.5	760	4244	3800
R1.0	333	1860	1900

4.4.4 Morphological characterisation

SEM images of CdS thin films grown with different S/Cd ratios are shown in Figure 4.27. It is observed that the grain sizes increased as the ratio of S/Cd was increased. The higher concentration of sulphur introduced more ions in the electrolyte to form sufficient nucleation centres on the surface and more scope for grains to expand their volume [36]. Ramaiah et al. and Saxena et al. also observed the same trend [36,37]. This suggests that the grain sizes can be controlled by the concentration of Cd and S in the electrolyte. The CdS films deposited with an S/Cd ratio of 1.0 shows established round shaped grains.

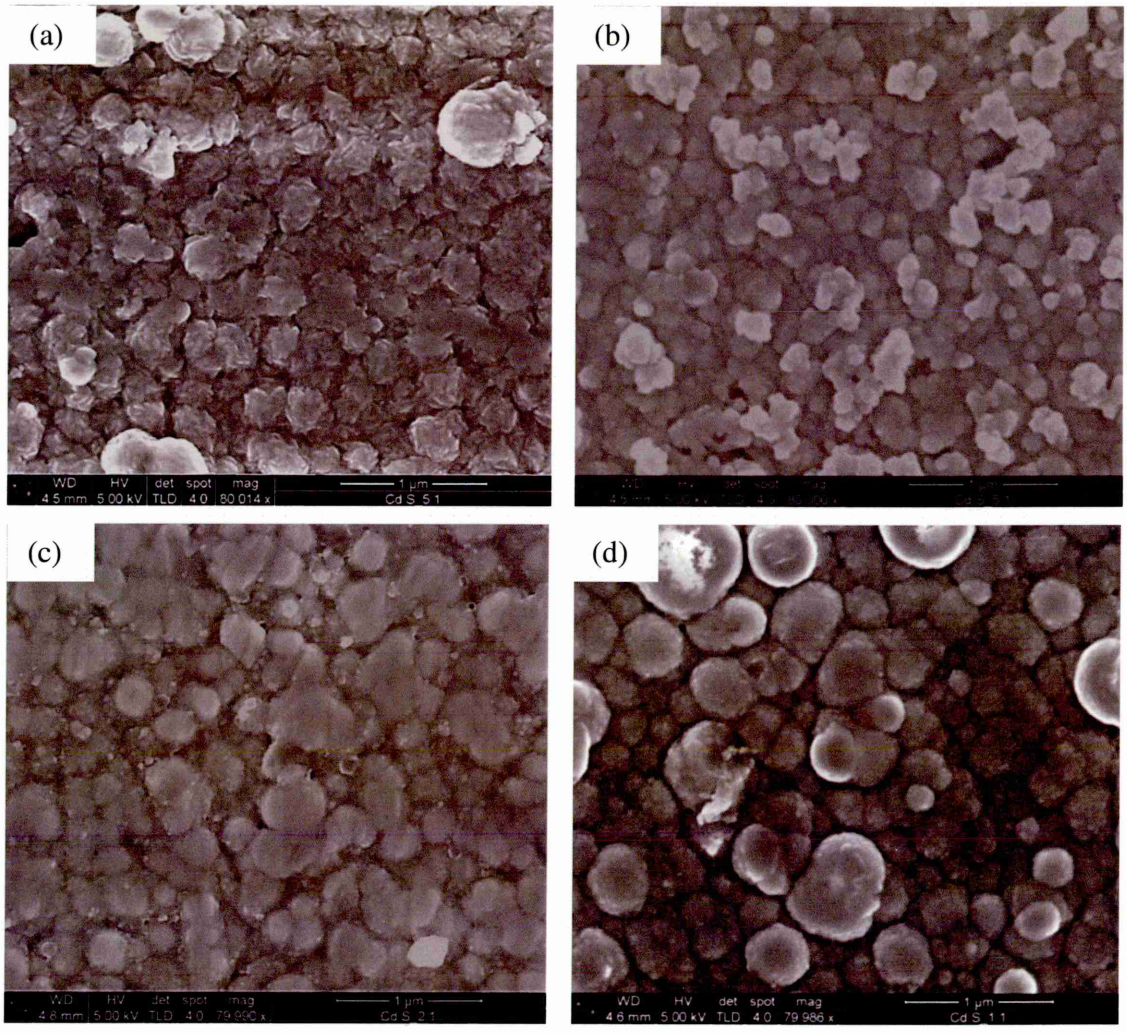


Figure 4.27: The SEM images of CdS thin films with S/Cd ratio of (a) 0.1, (b) 0.2, (c) 0.5 and (d) 1.0.

4.4.5 Conclusion

CdS thin films have been prepared from four different electrolytes containing S/Cd ratios of 0.1, 0.2, 0.5 and 1.0. The XRD measurement shows an increase of crystallinity as the ratio of S/Cd in the electrolyte is increased, which is due to the increase in thickness. Optical characterisation shows the decrement of energy bandgap and transmittance as the sulphur concentration increased. Sample grown from S/Cd ratio of 1.0 shows a cloudy surface due to the precipitation of the yellowish CdS particle in the electrolyte. The thickness measurement shows that the deposition rate of the CdS increased as the S/Cd concentration ratio increased up to 0.5 but then reduced with the further addition of sulphur. SEM images show that the grain sizes enlarge as the S/Cd ratio increased. The addition of sulphur did enhance the crystallinity and deposition rate of CdS films but it has a limitation since too much sulphur generated a precipitation in the electrolyte, thus the solution became more resistive. From this experiment it is suggested that the suitable range of S/Cd concentration ratio is in between 0.2 to 0.5 in order to produce a good quality of CdS.

4.5 Overall Conclusions

CdS thin films have successfully grown via electrodeposition from an aqueous electrolyte containing $CdCl_2$ and ammonium thiosulphate ($(NH_4)_2S_2O_3$). Thin films of CdS showed good adhesion to the FTO/glass substrate. From the study on the growth voltage and temperature for electrodeposition of CdS thin films, the optimum V_g and T_g were obtained as 1455 mV and 85°C, respectively. The annealing temperature and time have also been studied systematically. The best annealing temperature and time for the CdS films observed in this work are 400°C and 20 minutes, respectively. Further than this, the CdS will experience cracks, voids, loss of material and lower in electrical conductivity. The effects of chemical treatments on CdS during annealing have also been studied and it shows that the CdS thin films annealed with the chemical treatment ($CdCl_2$+CdF_2) have produced better properties. Four different electrolytes containing S/Cd ratio of 0.1, 0.2, 0.5 and 1.0 have been prepared to study the effects of sulphur concentration in the CdS electrolyte. From this experiment, it suggests that the suitable S/Cd concentration ratio is between 0.2 and 0.5. The application of CdS as a window layer will be further studied in the form of solar cell device performance.

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Chapter 5 - Characterisation of CdTe thin films

5.0 Introduction

This chapter presents a material study on the main absorber layer in our solar cell device, CdTe layers. The CdTe layers in this work were prepared by an electrodeposition technique from an aqueous solution containing $CdCl_2$ as the Cd source instead of typical $CdSO_4$ [1-3] and $Cd(NO_3)_2$ [4] in the previous work. The reason why we grow CdTe from chloride precursor has been discussed in Section 2.1.4.2. The effect of growth voltages, annealing conditions and chemical treatments on CdTe thin films have been studied with various characterisation techniques such as XRD, UV-Vis spectroscopy, optical profilometry, PEC measurement, DC conductivity measurement, C-V measurement, SEM and AFM. The aim of this work is to study the electrodeposition of CdTe thin film grown from chloride precursor and to understand the properties of electrodeposited CdTe layers under various conditions before using them as an absorber layer in the solar cell device. The chapter has been divided into four sections as shown in the flowchart in Figure 5.1.

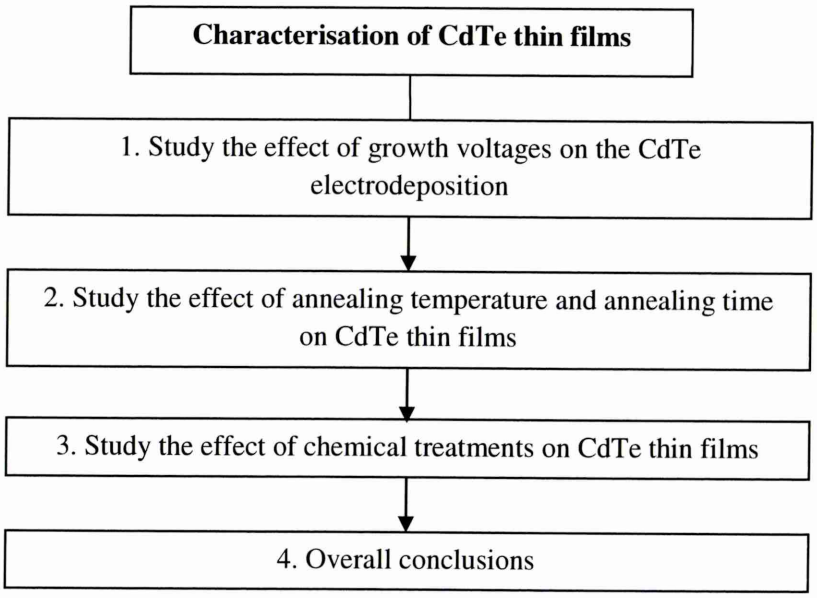

Figure 5.1: Flow chart of a study on CdTe thin films reported in this chapter.

5.1 Study the effect of growth voltages on the CdTe electrodeposition

The optimisation of growth voltages on CdTe deposition is compulsory before electroplating the layer. Cyclic voltammetry was obtained to estimate the approximate voltage range for film deposition. Using the approximate growth voltage range, CdTe thin films were grown at different $V_{g.}$ values. The electrodeposition was carried out

potentiostatically in a three-electrode system and the deposition time was kept constant for 90 minutes. The growth conditions were optimised by characterising the electrodeposited films through XRD, UV-Vis spectroscopy, PEC measurement, DC conductivity measurement, C-V measurement, SEM and AFM.

5.1.1 Voltammogram

Cyclic voltammetry provides the information on the electric current flow in the electrolyte and it is obtained by measuring the current passing through the working electrode during the potential scans. Figure 5.2 shows a typical cyclic voltammogram of aqueous solutions of (a) 1.00 M $CdCl_2$, (b) 1 mM TeO_2 and (c) mixture of 1.00 M $CdCl_2$ and 1 ml of prepared 1 mM TeO_2 during the forward and reverse cycles between 0 and 2000 mV. The scanning rate and the solution temperature were maintained at 3 mVs^{-1} and 65±2°C, respectively.

The cyclic voltammogram of 1.00 M $CdCl_2$ aqueous solution is shown in Figure 5.2(a). Cd from $CdCl_2$ source started to deposit at a cathodic voltage of ~673 mV with respect to SCE in the forward cycle. Cd has a reduction potential of E^o=-403 mV with respect to H_2 reference electrode [5]. As the voltage increases, the current density increases after ~673 mV and thus more Cd is deposited. The noise in the cyclic voltammogram at high cathodic voltages could be due to H_2 gas evolution. During the reverse cycle, the current becomes negative after 670 mV due to the dissolution of Cd from the cathode surface.

From the cyclic voltammogram for aqueous solutions of 1 mM TeO_2 in Figure 5.2(b), it is observed that Te deposition starts at ~343 mV with respect to the saturate calomel reference electrode in the forward cycle and is dissolved at ~764 mV in the reverse cycle. Also, the deposition rate of Te is equal to the dissolution rate at points a, b, and c, therefore the resultant current density is zero. Te has a reduction potential of E^o=+593 mV with respect to the H_2 electrode [5]. Therefore, Te is depositing at lower cathodic potentials compared to Cd.

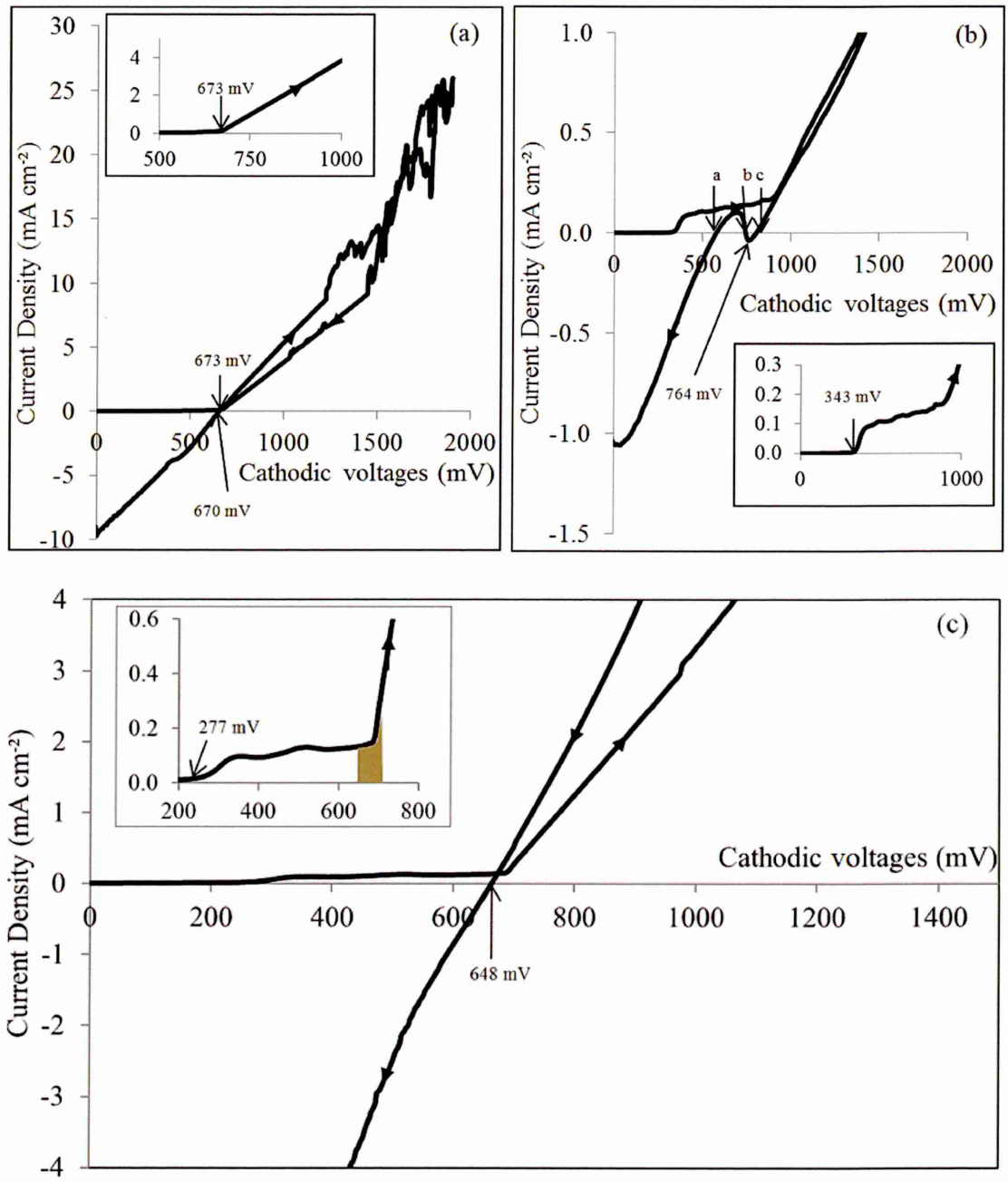

Figure 5.2: Cyclic voltammograms for aqueous solutions of (a) 1.00 M $CdCl_2$ (b) 1 mM TeO_2 and (c) mixture of 1.00 M $CdCl_2$ and 1ml of 1 mM TeO_2 using glass/FTO as the cathode, a graphite rod as the anode and SCE as the reference electrode. The arrows indicate the directions of the cycle.

From the cyclic voltammogram of a mixed solution of 1.00 M $CdCl_2$ and 1 ml of prepared 1 mM TeO_2 shown in Figure 5.2(c), CdTe mixed phase deposition starts from ~277 mV. As the cathodic voltage is gradually increased, it is observed that the film colour starts changing into a dark appearance at $V_g \geq 300$ mV due to the Te-rich CdTe region. This film starts turning to a honey-black colour at a cathodic voltage of around

650-700 mV, thus suggesting the deposition of stoichiometric CdTe. As the cathodic potential increases to ≥730 mV, the layer becomes silvery bluish metallic which suggests that the cathodic voltages above 730 mV produce Cd-rich CdTe. Changing the applied potential can vary the composition of the CdTe layer. The deposition rate of CdTe is equal to the dissolution rate of CdTe at V_g=648 mV and therefore the current density is zero at this voltage during the reverse cycle. Therefore, from the voltammogram observed in this work, the suitable V_g range for the stoichiometric CdTe layer is observed from 660 to 710 mV. The detailed study on the V_g was carried within this range in order to obtain the optimum V_g to grow CdTe thin films, via relevant material characterisations.

5.1.2 Structural characterisation

The X-ray diffraction studies were carried out on as-deposited and $CdCl_2$ heat-treated CdTe layers and typical results are shown in Figure 5.3 (a) and (b) respectively. In this study, CdTe thin films were electrodeposited at different cathodic voltages from 680 to 709 mV. The $CdCl_2$ heat treatment was performed at 400°C for 20 minutes in air. According to Figure 5.3, both graphs show the presence of the noticeable peak of CdTe at 2θ=24.15° corresponding to the (111) cubic phase. The highest crystallinity peak was observed at the cathodic potential of 698 mV for both as-deposited and $CdCl_2$ heat-treated CdTe layers. In Figure 5.3 (b), most of the $CdCl_2$ treated samples show a reduction of (111) CdTe peak as a general trend. Also the other peaks of cubic CdTe at 2θ=39.46° and 46.58° were observed, corresponding to a diffraction of (220) and (311) planes, respectively after the $CdCl_2$ treatment. This suggests that the reduction in (111) XRD peak is due to the loss of preferred orientation and grains becoming randomly orientated after $CdCl_2$ heat treatment.

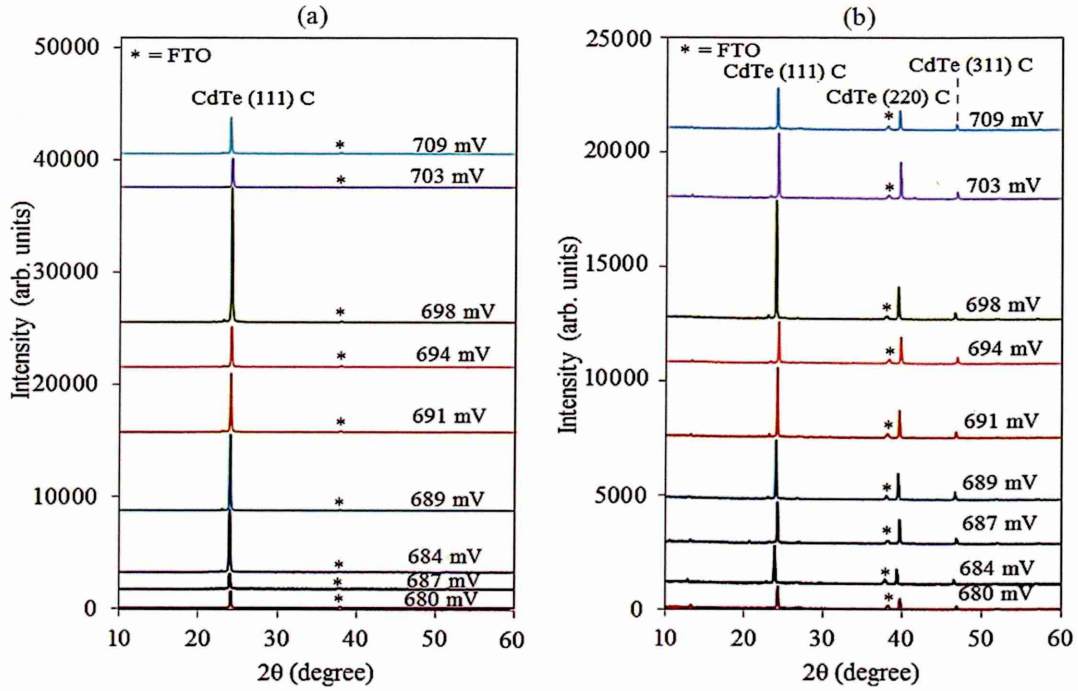

Figure 5.3: XRD patterns of CdTe thin films grown at a cathodic voltage range of 680 to 709 mV for (a) as-deposited and (b) $CdCl_2$ treated samples at 400°C for 20 minutes in air.

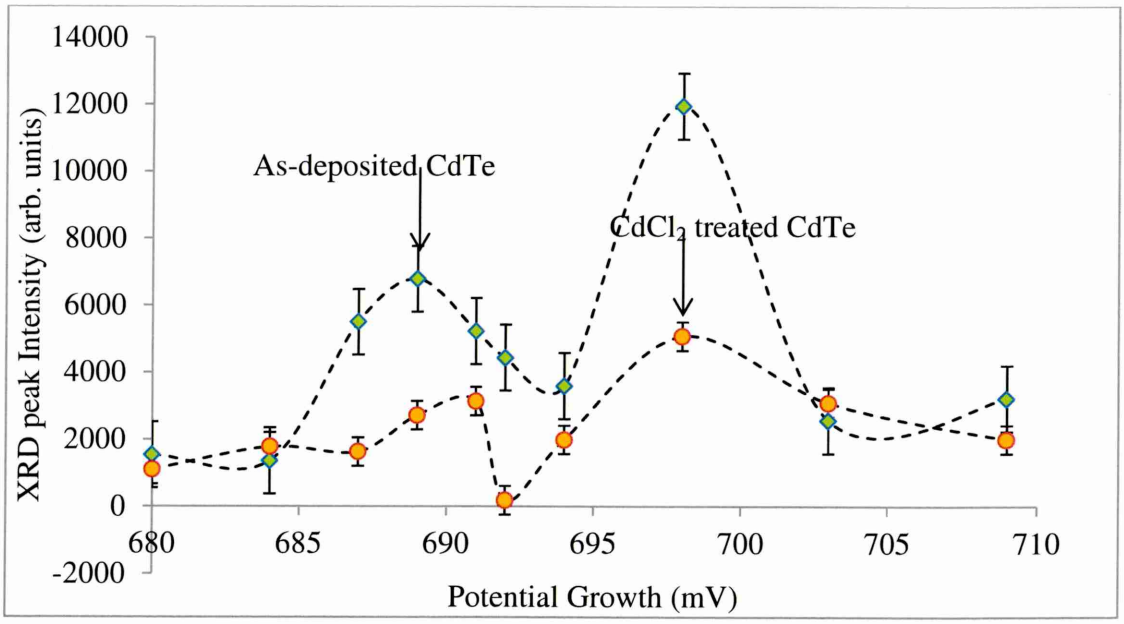

Figure 5.4: The intensity of (111) peak for as-deposited and $CdCl_2$ treated CdTe layers.

Figure 5.4 shows the graph of intensity of (111) peak on as-deposited and after $CdCl_2$ treated CdTe. It is observed that the most intense XRD peak is at V_g=698 mV for both as-deposited and $CdCl_2$ treated material. The high intensity of (111) peak indicates high crystallinity related to a stoichiometric material. The deviation from the

stoichiometric point reduced the crystallinity due to the Cd-rich or Te-rich CdTe. In a recent publication [6], a sudden phase transition was identified when CdTe layer is heat-treated at 385±5°C in air, in the presence of $CdCl_2$. At this temperature, liquid phases occur at the grain boundaries, and the grains lose their preferred orientation of (111) and show random orientations. From the phase diagram in Figure 5.5, it is suggested that a liquid phase occurs at the grain boundaries, since the melting point of Cd-rich CdTe is ~321°C. Therefore, all the Cd-rich CdTe will exhibit some level of liquid phase above ~321°C. Also the EDX spectrum for Te-rich CdTe film in Figure 5.6 shows Cl peak which indicates the presence of Te-Cl phase ($TeCl_2$ melts at ~208°C and $TeCl_4$ melts at ~224°C) at the grain boundary. As a result, (111) peak collapse and the other two peaks (220) and (311) appear in the XRD spectra. In our heat treatment at 400°C, this transition has just occurred and therefore intensity decreased in (111) peak and the appearance of the other two peaks has been observed.

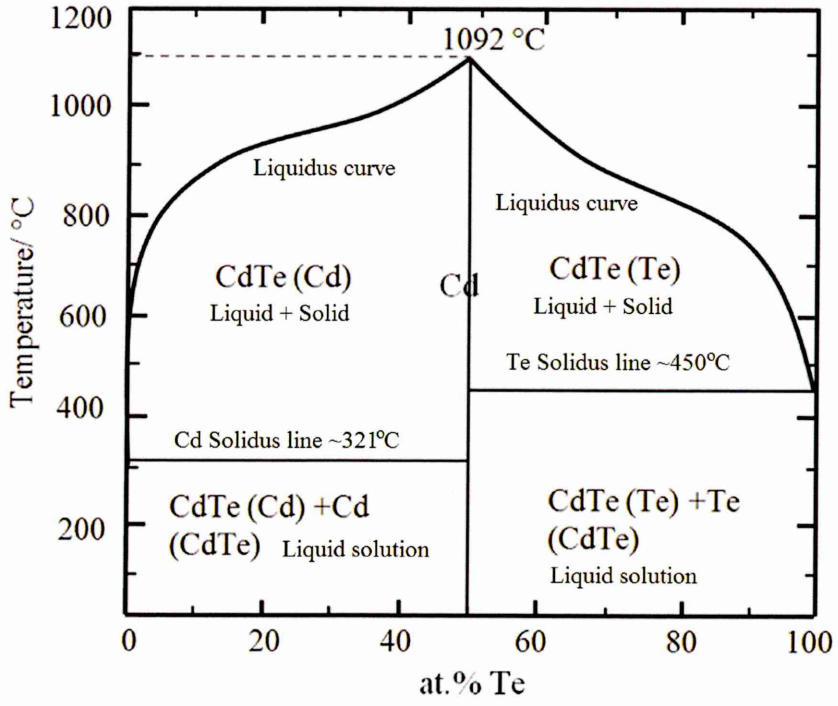

Figure 5.5: Schemetic diagram of a phase diagram of CdTe.

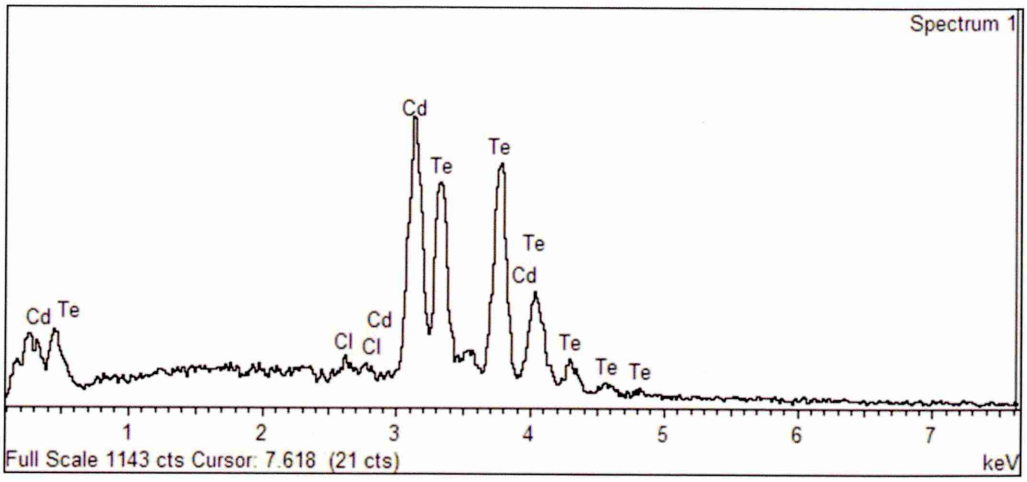

Figure 5.6: Schemetic diagram of the EDX spectrum on Te-rich CdTe thin film.

Figure 5.7 shows the XRD spectra plotted on a log-scale in order to identify all peaks. These spectra are for as-deposited and $CdCl_2$ treated CdTe layers grown at V_g=698 mV. The as-deposited sample shows the appearance of small crystalline peaks of TeO_2 and Cd_xTeO_y at 2θ=21.94° and 23.11° corresponding to the (011) orthorhombic and (111) monoclinic planes, respectively. These compounds incorporating oxygen are expected on the surface or in the material, since the layers are grown in atmospheric conditions in an aqueous solution. Also the prominent peak of (111) cubic CdTe is observed in the as-deposited sample. The TeO_2 peak disappeared while both (111) Cd_xTeO_y and (111) CdTe peaks slightly reduced after $CdCl_2$ treatment at 400°C for 20 minutes. Also, after $CdCl_2$ heat treatment, extra peaks were observed at 2θ=39.46° and 46.58° which represent the cubic CdTe with (220) and (311) planes respectively. It is well known that $CdCl_2$ treatment usually improves the crystallinity of CdTe up to a certain temperature [6-8]. However, after this temperature, a rapid reduction of (111) CdTe peak and the appearance of (220) and (311) peaks have been observed [4,9,10]. In a recent publication, this transition temperature has been identified as 385±5°C [6]. The XRD peak intensities, angles and occurrence of new peaks can be attributed to the random orientation of the grains in CdTe layers after the melting of the grain boundaries at ~385°C. The summary of XRD data and obtained structural parameters of CdTe thin films grown at V_g=698 mV are shown in Table 5.1. The crystallite size, D was calculated using Scherrer's formula as mentioned in equation (4.1) in the previous chapter.

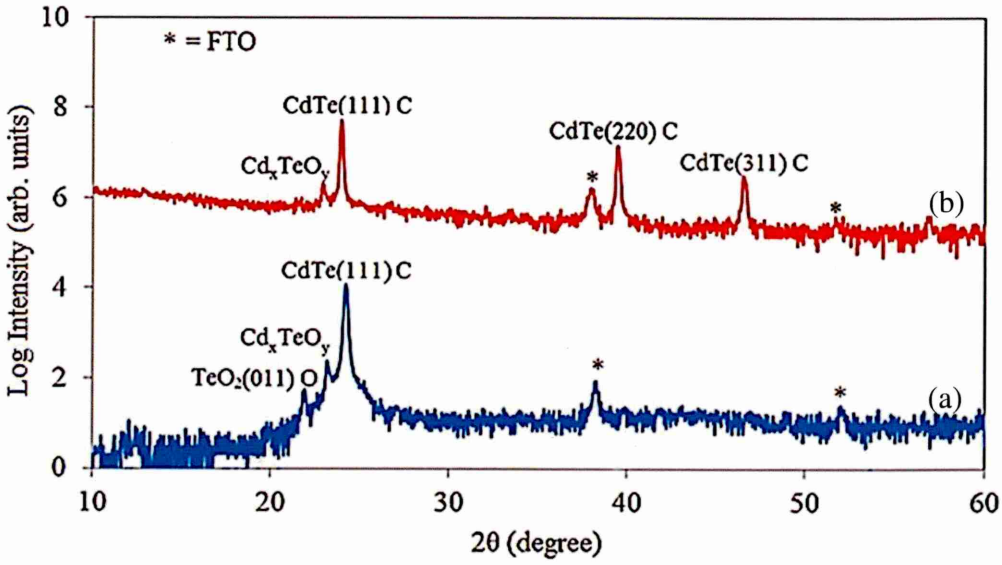

Figure 5.7: XRD patterns of (a) as-deposited and (b) $CdCl_2$ treated CdTe layers grown at a cathodic potential of 698 mV plotted on a log-scale.

Table 5.1: Summary of XRD data for as-deposited and after $CdCl_2$ treated CdTe layers grown at a cathodic potential of 698 mV.

Sample	Angle $2\theta^o$	Lattice spacing d (Å)	Intensity (a.u)	FWHM (Degree)	Crystallite size D (nm)	Plane of orientation ($h\ k\ l$)	Assignments
As-deposited CdTe	21.94	4.00	56	0.173	51.7	(0 1 1)	TeO_2 / Orthorhombic
	23.11	3.88	239	0.134	63.2	-	Cd_xTeO_y
	24.05	3.71	12325	0.134	63.3	(1 1 1)	CdTe / Cubic
$CdCl_2$ HT CdTe	23.04	3.91	129	0.134	63.2	(1 1 1)	$CdTeO_3$ / Monoclinic
	24.15	3.70	4102	0.134	63.3	(1 1 1)	CdTe / Cubic
	39.46	2.28	1367	0.167	64.3	(2 2 0)	CdTe / Cubic
	46.58	1.93	238	0.233	51.8	(3 1 1)	CdTe / Cubic

5.1.3 Optical characterisations

The optical absorption measurements of the CdTe layers were carried out using a UV-Vis spectrophotometry in the wavelength range 600–1000 nm. The square of absorbance (A^2) has been plotted as a function of photon energy, and the energy bandgap was estimated by extrapolating the straight-line segment of the graph to the photon energy axis. Figure 5.6 shows optical absorption of the as-deposited CdTe thin films grown at different cathodic voltages from 680 to 709 mV. It is observed that the energy bandgap of the as-deposited CdTe films was in the range of 1.48 to 1.51 eV. The

average error of these measurements is ±0.02 eV. The graphs in Figure 5.8 and Figure 5.9 show that the trend of energy bandgap is increased with V_g up to 694 mV and gradually reduces with further increments of V_g. The reduction of the bandgap with the higher V_g is due to the deposition of metallic Cd with a zero bandgap. Also the slope of the band edge is much sharper at V_g=698 mV which suggests that there are less shallow donors and acceptors exist in these stoichiometric layers. The summary of the slope of the band edge with different V_g is shown in Table 5.2.

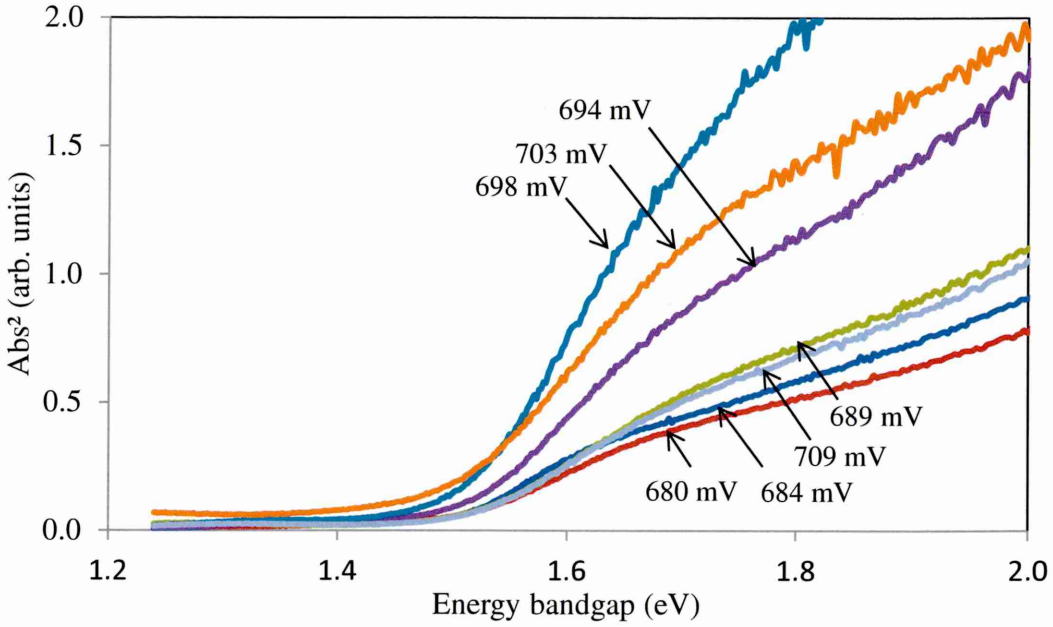

Figure 5.8: Optical absorption curves of as-deposited CdTe thin films grown at different V_g values.

Table 5.2: The optical bandgap and slope of band edge of CdTe layers at different V_g values. Note that asterisk (*) indicates the maximum slope.

Cathodic Voltage, V_g (mV)	Energy bandgap, E_g (eV)	Slope of absorption band edge (eV^{-1})
680	1.48	1.86
684	1.49	3.08
689	1.51	2.73
694	1.51	4.54
698	1.49	7.80*
703	1.48	5.29
709	1.49	2.50

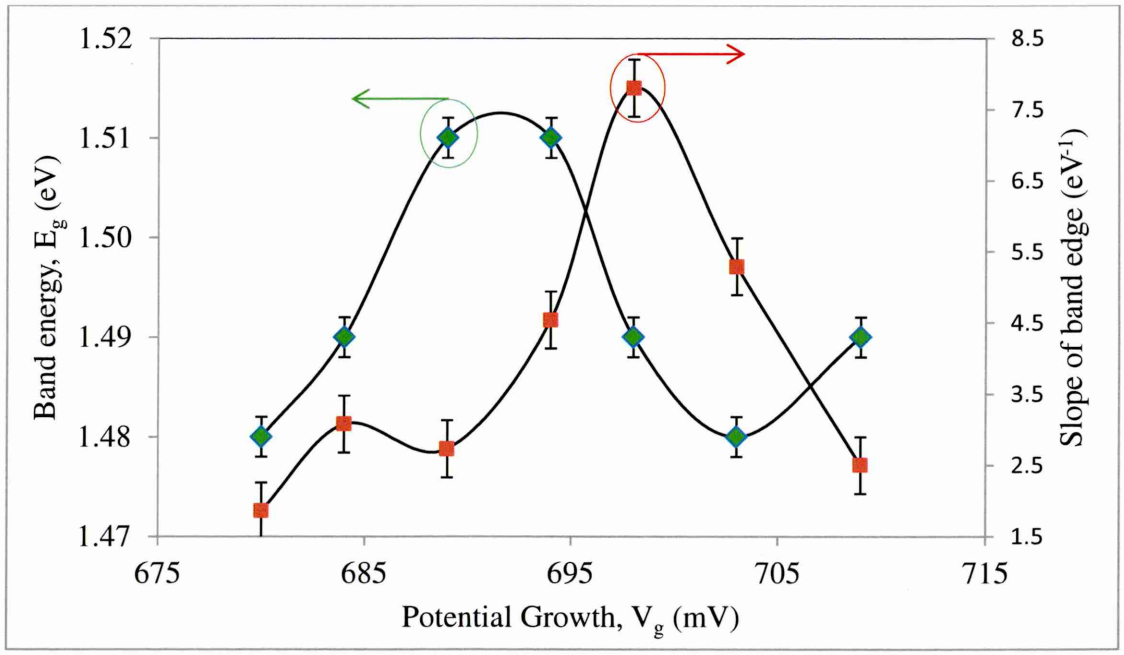

Figure 5.9: Energy bandgap and the slope of band edge versus V_g for as-deposited CdTe thin films.

5.1.4 Thickness measurement

The thicknesses of electrodeposited CdTe layers at different V_g were calculated theoretically by Faraday's law equation and experimentally using an optical profilometry. As shown in Figure 5.10, the thicknesses obtained from the theoretical and experimental methods are similar. This indicates that the loss of electronic charges for the electrolysis of water is minimal under these growth conditions. It is observed

that the deposition rate of CdTe thin film calculated from both theoretical and experimental methods are 6 nm per minute. From this result, it is estimated that the thickness of CdTe deposition is ~360 nm per hour. Therefore, it requires at least four hours deposition to fabricate solar cells with 1.44 μm thick CdTe absorber layer.

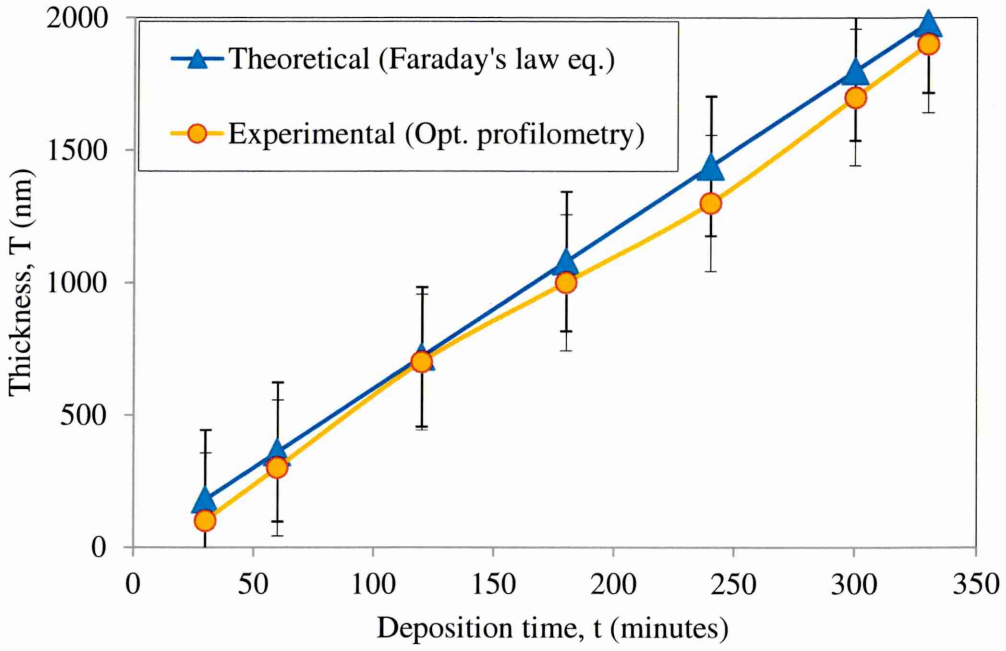

Figure 5.10: Thickness of CdTe thin films obtained from theoretical and experimental methods as a function of different deposition times (V_g was kept at 698 mV, optimum value).

5.1.5 Electrical characterisation

The PEC measurements were carried out in order to test the electrical conductivity type of CdTe layers. Glass/FTO/CdTe layers were immersed in 0.1M $Na_2S_2O_3$ aqueous solution to form a solid/liquid junction at the CdTe/electrolyte interface. The voltage produced at the junction was measured with respect to a carbon counter electrode under dark and illuminated conditions. The difference in voltages provides the open circuit voltage of the solid/liquid junction, or the PEC signal. The system was first calibrated with a known material like n-CdS, and the sign of the PEC signal shows the electrical conductivity type of the CdTe layers. Figure 5.11 shows the trend of the PEC signal for as-deposited and $CdCl_2$ treated CdTe thin films as the function of growth voltage, V_g. It is observed that the as-deposited CdTe samples grown at lower voltages (V_g<700 mV) are n-type and those which are grown at higher voltages ($V_g \geq 700$ mV) are p-type.

These results show complete contrast to the CdTe grown by $CdSO_4$ [3,6] and $Cd(NO_3)_2$ [4] precursors. Figure 5.12 shows PEC results obtained from CdTe layers grown using sulphate and nitrate precursors without the presence of Cl^- in the bath. These results behave according to electrodeposition principles. According to the E^o values of Te (+0.593 V) and Cd (-0.403 V) with respect to standard hydrogen electrode, CdTe electrodeposited below the stoichiometric point (V_i) shows a p-type electrical conductivity due to Te-richness, while CdTe layers grown above V_i show an n-type electrical conductivity due to Cd-richness. This has been reported earlier from our previous work using sulphate and nitrate precursors [4,6,11]. The completely opposite results observed for CdTe layers grown from chloride precursor are therefore due to the "built-in $CdCl_2$ treatment" during this growth.

After heat treatment at 400°C for 20 minutes, in the presence of $CdCl_2$, all samples become p-type in electrical conductivity. This provides a clue for CdTe becoming p-type in electrical conductivity when a high concentration of Cl is present in the material. There are many reasons why the conductivity type of CdTe changes with annealing or treatment. One is due to the generation of Cd vacancies due to the Cd sublimation during treatment. In fact, the diffusion of excess Te from the grain boundaries into the CdTe crystallites or film surface and the doping effect due to impurities also can contribute to the type conversion [12]. Annealing certain dopants can also drastically affect the electrical properties [13]. In this case, the doping effects seem to be drastic depending on the initial composition of the CdTe layer and the concentration of Cl present for doping the material.

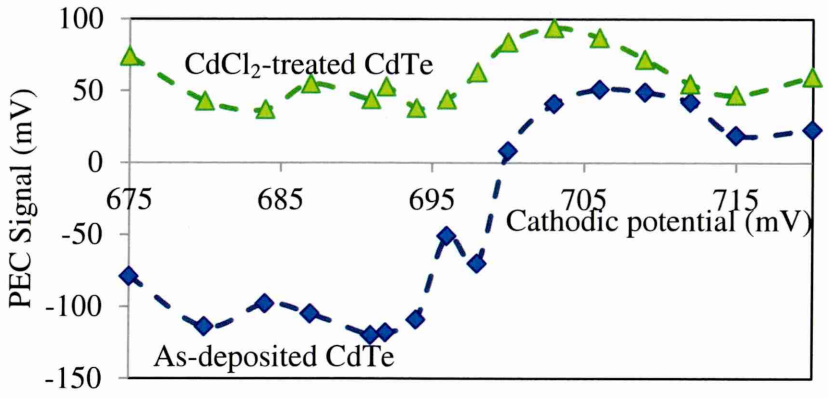

Figure 5.11: PEC signals as a function of growth voltage, for as-deposited and $CdCl_2$ treated CdTe layers grown from chloride precursors.

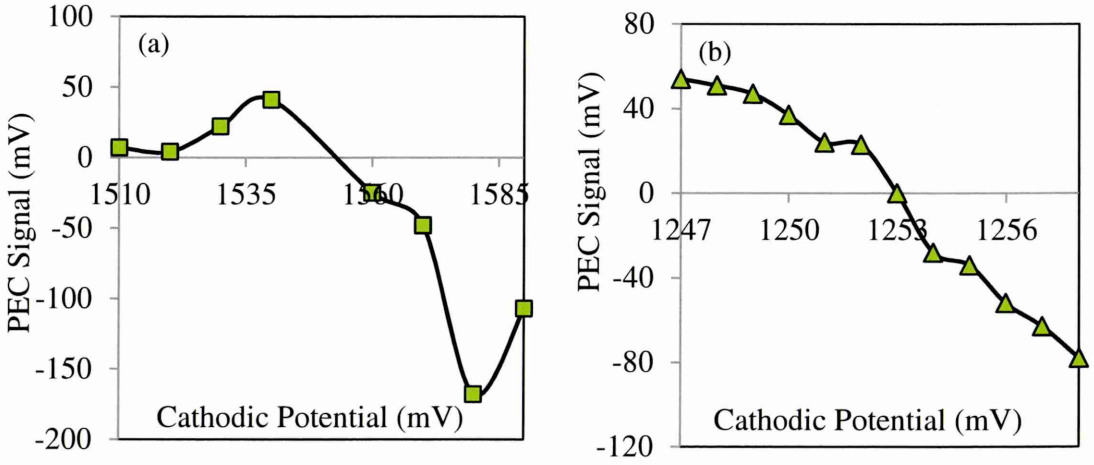

Figure 5.12: PEC signals for as-deposited CdTe layers grown from (a) sulphate [3] and (c) nitrate precursors [4].

Further investigation on the effect of the conductivity type of CdTe layers over the electrical properties is presented in this section. Four samples with size 2.0×2.0 cm^2 were electrodeposited at V_g 690, 698, 700 and 705 mV in order to get a variation of conductivity types. These samples were deposited for three hours to get the thicker layer ~1 μm. PEC measurement has been carried out to confirm the conductivity type of these materials. Samples grown at 690 and 698 mV have been identified as n-type CdTe layers while the other two samples grown at 700 and 705 mV were confirmed as p-type CdTe layers. These samples were then cut into two pieces with the size of 1.0×2.0 cm^2 each. Half of these samples were used for DC conductivity measurements and the other half of the pieces was used for C-V measurements.

As for DC conductivity measurement, 2 mm diameter and circular ohmic contacts were made by evaporating the Au layer for p-type CdTe samples and Al layer for n-type CdTe samples through a metallic mask. The resistance of the CdTe layers was carried out through I-V measurements at several points of contact. The average resistance of each sample was measured and the electrical conductivity was calculated using equations 3.12 and 3.13 as stated in Chapter 3. Table 5.3 and Figure 5.13 show the electrical conductivity trend of n-type (grown at 690 and 698 mV) and p-type (grown at 700 and 705 mV) CdTe layers. It is observed that n-type CdTe films have higher conductivities than p-type CdTe films by one order of magnitude. Higher conductivity in n-type CdTe is due to the higher mobility in the n-type semiconductor than the p-type semiconductor since the drift velocity of an electron is faster than the drift velocity of a hole. In addition, the electron effective mass is smaller than the hole's

effective mass therefore the electron mobility is greater than the hole's mobility [14]. The relation between drift velocity, mobility and conductivity is shown in equation 5.1 and 5.3 below and equation 3.19.

$$\sigma = ne\mu \tag{5.1}$$

$$\mu = \frac{\sigma}{qN_d} \tag{5.2}$$

$$\mu = \frac{V_d}{E} \tag{5.3}$$

where σ is electrical conductivity, μ refers to the mobility of the electrons or holes, and n is free carrier concentration at room temperature (n can be N_A or N_D), V_d is a drift velocity and E is the electric field.

For C-V measurements, the circular Schottky contacts with a diameter of 2 mm were made by evaporating an Al layer for p-type CdTe samples and Au layer for n-type CdTe. The C-V measurements were carried out at several points of contact under dark conditions. The Mott-Schottky graph was plotted and the doping density was calculated using the equation 3.15 to 3.18. The summary of C-V measurements is shown in Table 5.3 and Figure 5.13. It is observed that the doping concentration of CdTe is reduced from 2.17×10^{17} to 5.70×10^{13} cm^{-3} as the V_g increases from 690 to 698 mV but then the doping concentration increases exponentially as the V_g increases to 700 and 705 mV. This result indicates that the doping concentration of the stoichiometric region of CdTe grown from cadmium chloride precursor is in the range of 5.70×10^{13} to 9.59×10^{14} cm^{-3}. This is good since many results in the literature report that the best solar cell efficiency for CdTe is produced when the doping concentration is in the magnitude order of 10^{14} cm^{-3} [6,15,16]. The mobility of these layers was then calculated using equation 5.2 and presented in Table 5.3. The result demonstrated that the increase in mobility is mainly due to the doping concentration. The CdTe layer grown at 698 mV shows the highest mobility which is associated with the optimum V_g value in the previous experiment. However, it should be noted that the chemical treatment and annealing process also affect these parameters, thus further experiments on this work will be discussed more in section 5.3.3.

Table 5.3: Summary of conductivity, doping concentration and mobility values calculated from I-V and C-V measurements.

V_g (mV)	Conductivity Type	I-V Measurement		C-V Measurement		Mobility, μ ($cm^2V^{-1}s^{-1}$)
		Structure	Conductivity $\times10^{-5}$ $(\Omega cm)^{-1}$	Structure	Carrier concentration, n (cm^{-3})	
690	n	g/FTO/CdTe/Al	1.30	g/FTO/CdTe/Au	2.17×10^{17}	0.0004
698	n	g/FTO/CdTe/Al	2.62	g/FTO/CdTe/Au	5.70×10^{13}	2.8713
700	p	g/FTO/CdTe/Au	0.26	g/FTO/CdTe/Al	9.59×10^{14}	0.0170
705	p	g/FTO/CdTe/Au	0.83	g/FTO/CdTe/Al	4.35×10^{17}	0.0001

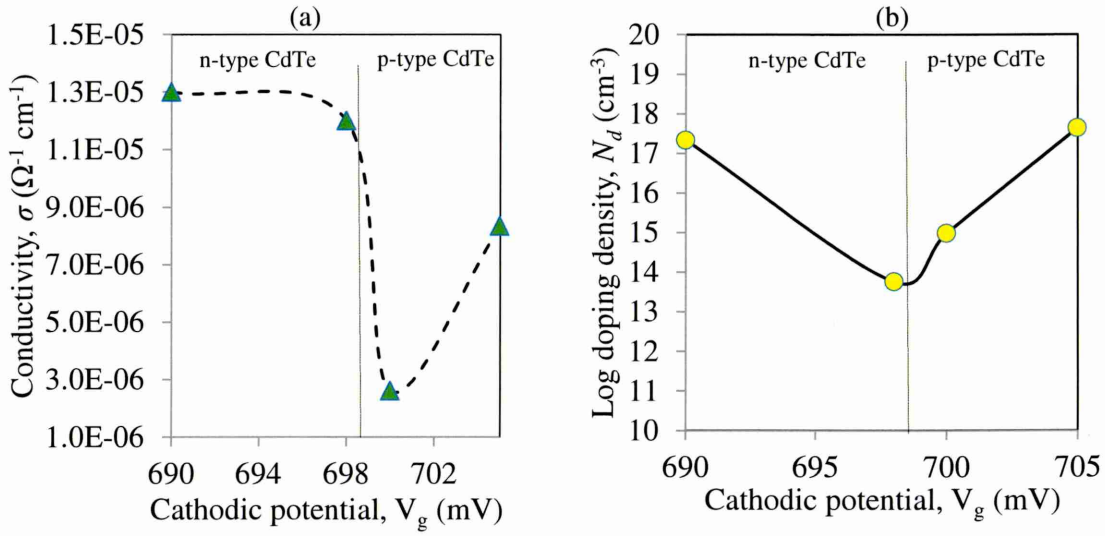

Figure 5.13: The trends of (a) conductivity and (b) doping concentration of CdTe thin films electrodeposited at 690, 698, 700 and 705 mV.

5.1.6 Conclusion

CdTe thin films have been successfully grown by electrodeposition using cadmium chloride precursors. The voltage range for the stoichiometric CdTe layer has been estimated by a cyclic voltammogram from 660 to 710 mV. XRD results show the presence of the prominent peak of (111) cubic CdTe and this peak shows the highest intensity for CdTe grown at V_g=698 mV for both as-deposited and after $CdCl_2$ treatment CdTe. Optical characterisation obtained showed that the energy bandgap of as-deposited CdTe films was in the range of 1.48 to 1.51 eV. Thickness measurements derived that the deposition rate of CdTe thin film calculated from both theoretical and experimental is ~360 nm per hour. PEC cell measurement shows a possibility to grow p-, i- and n-

type CdTe layers by tuning the V_g during electrodeposition. This result shows complete contrast to the CdTe grown by $CdSO_4$ and $Cd(NO_3)_2$ precursors due to the "built-in $CdCl_2$ treatment" during the growth. The I-V measurement shows that the n-type CdTe layers have higher conductivities than p-type CdTe due to the higher drift velocity and lower effective mass of electrons. The C-V measurement obtained showed an ideal doping concentration of 10^{13} to 10^{14} cm^{-3} at the stoichiometric region and n-type CdTe grown at 698 mV shows the highest mobility than other CdTe layers. From this study, the optimum V_g is suggested at 698 mV. The summarised result on this section is presented in Figure 5.14.

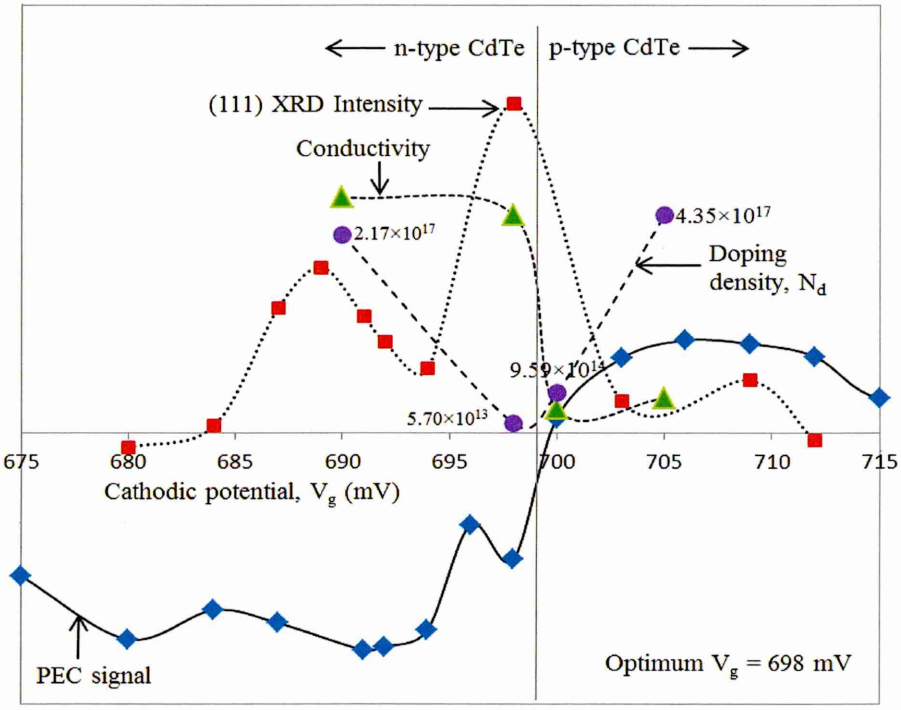

Figure 5.14: Graphical presentation of the summary of results for the electrodeposition of CdTe at various V_g values. The best V_g is obtained at 698 mV.

5.2 Study the effect of annealing temperature and annealing time on CdTe thin films

This section presents the study on annealing temperature and time for CdTe thin films. The work on the annealing process has been carried out in the presence of $CdCl_2$ treatment in air. Hence, it will be referred to as 'annealing' in this section. In the first part of the study, one substrate of glass/FTO with the area size of 7.0×2.0 cm^2 was electrodeposited with CdTe at 698 mV for two hours. This substrate was cut into seven

pieces to the size of about 1.0×2.0 cm^2 each. One of the pieces was set aside as a reference sample (as-deposited) while the other six pieces were annealed at different temperatures from 350 to 550°C. These samples were then characterised by XRD, UV-Vis spectroscopy, optical profilometry, PEC cell measurement, DC conductivity, SEM and AFM for their structural, optical, thickness, electrical and morphological properties. The best two temperatures were chosen for the following experiment.

In the following experiment, one medium size substrate with a size of 4.0×3.0 cm^2 was prepared and electrodeposited at 698 mV for about two hours. This sample was then cut into eight pieces to a size of about 1.0×1.5 cm^2 each and divided into two sets. The first set was annealed with the best temperature obtained from the previous work for 10, 15, 20 and 30 minutes. The second set of CdTe layers was annealed with the second best temperature obtained from the previous studies for 10, 15, 20 and 30 minutes. All the samples were characterised for their structural, electrical, and morphological properties using XRD, PEC cell measurement and SEM.

5.2.1 Structural characterisation

The XRD spectra of CdTe layers after being annealed at different temperatures up to 500°C are shown in Figure 5.15. It seems that the natural growth trend of CdTe on FTO is along a (111) preferred orientation. The results in Figure 5.15 and Table 5.4 show that the intensity of (111) peak increases up to a temperature between 385°C and 420°C in the beginning. At this temperature, the grain boundaries melt and the CdTe grains become randomly orientated [6]. After the melting of the grain boundaries, the grains become randomly oriented and start to coalesce and form larger grains. The limitation of the Scherer equation and XRD instrumentation prevent the determination of the size of these large grains, but SEM in Figure 5.21 (d) clearly shows the formation of larger grains in the few μm sizes. CdTe film annealed at 420°C shows the clear enhancement of the other two peaks (220) and (311) while film annealed at ≥450°C demonstrates the collapse of (111) peak. Annealing at 500°C leads to reduction of all three peaks due to the loss of material via deterioration and sublimation. Besides, the CdTe layer annealed at 550°C did not survive at all. Therefore, the optimum temperature for annealing is suggested between 420 and 450°C for electrodeposited CdTe layers grown from a $CdCl_2$ precursor.

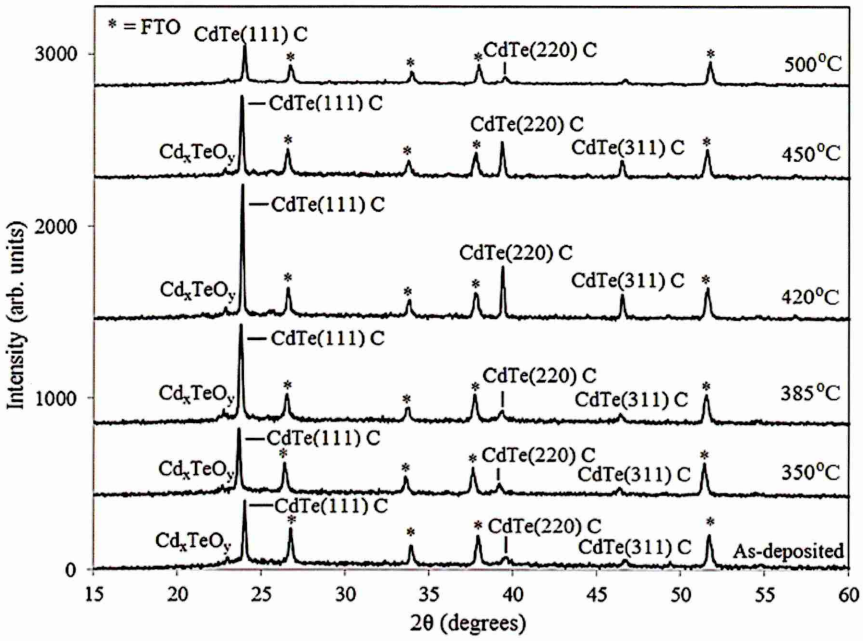

Figure 5.15: The XRD spectra for as-deposited CdTe and after annealing at 350, 385, 420, 450 and 500°C for 20 minutes in the presence of $CdCl_2$.

Table 5.4: Analysis of the XRD peaks for as-deposited CdTe and annealed at different temperatures from 350 to 500°C for 20 minutes in the presence of $CdCl_2$.

Annealing Temperature, T (°C)	Peak intensity			% peak relative to 111 peak			Crystallite size calculated from (111) peak, D (nm
	(111)	(220)	(311)	(111)	(220)	(311)	
As-deposited	373	15	9	100	4	2	63.3
350	383	26	12	100	7	3	63.3
385	501	38	10	100	8	2	63.3
420	730	241	109	100	33	15	65.8
450	433	176	66	100	41	15	63.3
500	235	32	11	100	14	5	63.3
550	The layer did not survive						

Figure 5.16 shows the XRD graphs of CdTe annealed at 420 and 450°C for 10, 15, 20 and 30 minutes. Both graphs show the presence of a prominent peak of (111) cubic CdTe and other two peaks (211) and (311). From Figure 5.16 (a), it is clear that the intensity of (111) peak start to increase as the annealing time increases up to 20 minutes and then deteriorates slightly with further annealing time. It is also observed that the presence of (220) and (311) peaks after the deposited sample is annealed at 420°C. The recrystallisation process during annealing has two stages which are through the recrystallisation by the random orientation of the grains followed by the orientation of the crystallites in a particular direction [6,17]. From Figure 5.16 (b), it is observed that the best annealing time was 15 minutes by referring to the intensities of (111) and (220) peaks. Similar to CdTe annealed at 420, CdTe annealed at 450°C also demonstrates the reduction of all three peaks after it is annealed for 30 minutes due to the loss of material by deterioration and sublimation. Based on XRD measurements it is suggested that a good annealing temperature and time is either at 420°C, 20 minutes or at 450°C, 15-20 minutes.

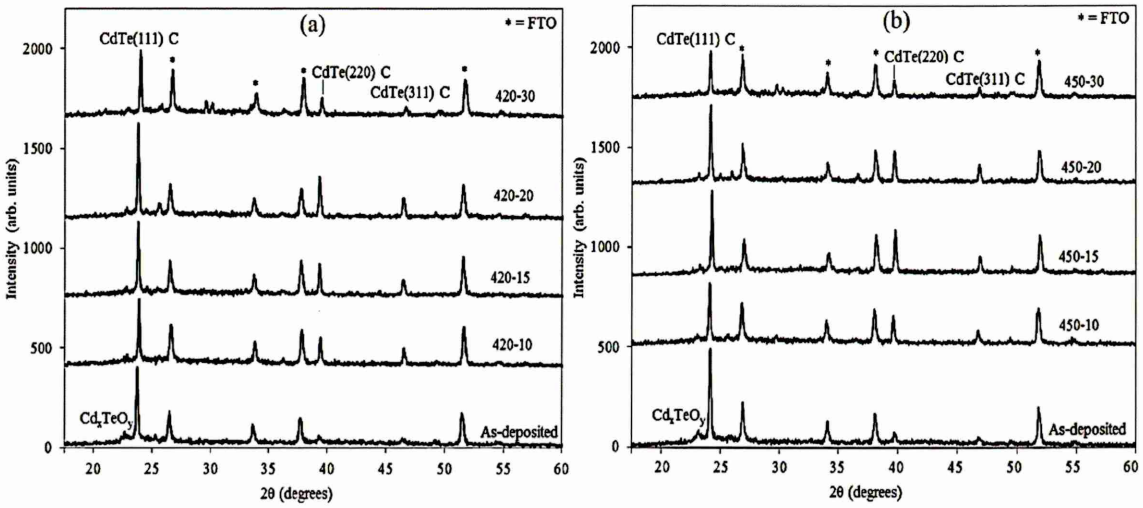

Figure 5.16: The XRD spectra for CdTe thin films annealed at (a) 420°C for 10, 15, 20 and 30 min and (b) 450°C for 10, 15, 20 and 30 min.

5.2.2 Optical characterisation

Figure 5.17 shows the optical absorption spectra of CdTe thin films annealed at temperatures from 350 to 500°C in the presence of $CdCl_2$. The bandgap of CdTe layers are decreased with higher annealing temperatures. The decrease in the energy bandgap after annealing temperature >385°C can be due to the recrystallisation, increase in grain size and lower defects [18]. The elimination of pinholes due to the grain growth also can prevent the photons passing through the pinholes. The close value of the bulk CdTe can be obtained if the atoms are better arranged in the crystal lattice. The presence of defects or impurities in as-deposited CdTe disturbs the lattice and leads to low light absorbance. The appropriate annealing temperature and time helps the atom to form better crystalline lattices. CdTe annealed at 500°C shows a drastic increment of bandgap which could be due to the sublimation of the material at a too-high annealing temperature. Overall, the variation of the bandgap with annealing temperature is relatively small. The range observed from 1.45-1.49 eV is considered nearly the same within the experimental error (±0.02 eV) of this measurement. This must be due to the quality of material which the bandgap does not affect too much during annealing; hence there is no significant difference for bangap energies with increasing annealing temperature. The summary of the optical energy bandgap with different annealing temperatures of $CdCl_2$ treatment is shown in Table 5.5.

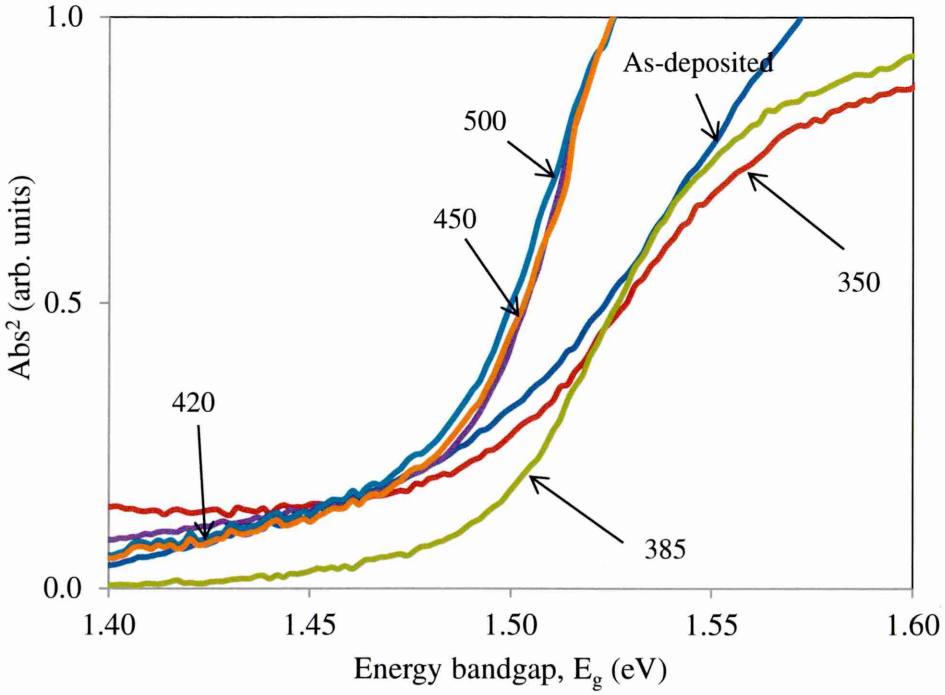

Figure 5.17: Optical absorption of CdTe thin films for as-deposited and annealed at temperatures from 385 to 500°C.

Table 5.5: The energy bandgap of CdTe layers at annealed temperatures.

$CdCl_2$ Treated Temperatures, T (°C)	Energy bandgap, E_g ±0.02 (eV)
65	1.49
350	1.48
385	1.49
420	1.46
450	1.45
500	1.47

5.2.3 Thickness measurement

The thicknesses of CdTe thin films as a function of annealing temperatures from 350 to 500°C were measured using optical profilometry and shown in Figure 5.18. From these measurements, it is observed that the thickness of the films decreased from 800 nm (as-deposited) to ~500 nm when the samples were annealed at temperature up to 450°C. The thickness shows a rapid decline to 200 nm at temperature 500°C which is due to the rapid loss of the material through sublimation. Therefore the annealing of CdTe thin

films should stick to a temperature range of 420-450°C to avoid the loss of material and to get all the benefits of the annealing process.

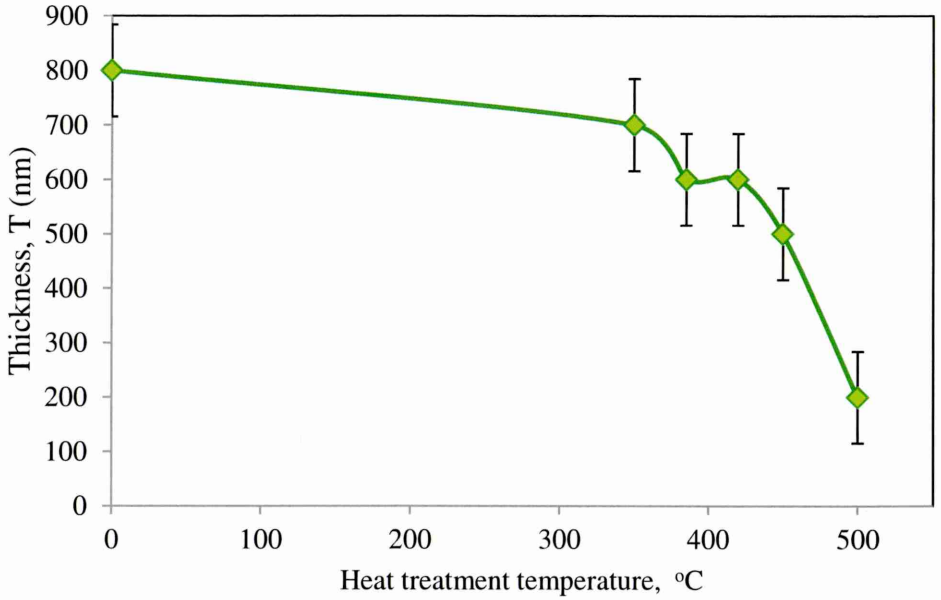

Figure 5.18: Thickness of CdTe thin films as a function of different annealing temperatures with the presence of $CdCl_2$.

5.2.4 Electrical characterisation

PEC cell measurements for as-deposited and annealed CdTe at different temperatures are shown in Table 5.6. The as-deposited CdTe thin film electrodeposited at 698 mV is n-type. However the electrical conductivity type of these samples has changed to p-type after annealing at 350, 385 and 420°C. As shown in Figure 5.19, Cd has a higher vapour pressure than Te [19]. Therefore, Cd tends to evaporate easier during annealing since the material with a higher vapour pressure tends to evaporate earlier than those with a lower vapour pressure. Krishnamurthy also has reported that the Cd sublimation energy to terminate the surface of the CdTe layer is much smaller than Te [20]. Therefore, Cd atom should be much easier to remove than Te. Therefore, the as-deposited CdTe with an n-type conductivity changed to p-type after annealing at 350 to 420°C. However, those samples annealed at 450°C and above have demonstrated n-type electrical conductivities. The high annealing temperature (T≥450°C) has initiated the deterioration of the layer through oxidation and sublimation. Also CdTe annealed at 550°C did not show any PEC signal since the layer did not survive. These results agree with the XRD data and SEM image presented in Table 5.4 and Figure 5.21.

Table 5.6: The PEC signal of CdTe grown at 698 mV with variations of annealing temperatures from 350°C to 550°C.

Annealing Temperature, T (°C)	$V_{Illumination}$ (mV)	V_{dark} (mV)	PEC Signal (V_{ill}-V_{dark}) (mV)	Average PEC signal (mV)	Conductivity type	Comments
	-113	-39	-74			
	-104	-36	-68			-
As-deposited	-103	-35	-68	-70.0	n	
	-38	-101	63			
	-45	-103	58			-
350	-43	-107	64	61.7	p	
	-50	-95	45			
	-50	-95	45			-
385	50	-95	145	78.3	p	
	-86	-147	61			
	-85	-140	55			-
420	-80	-129	49	55.0	p	
	-113	-53	-60			
	-117	-53	-64			material
450	-118	-50	-68	-64.0	n	degradation
	-138	-133	-5			
	-127	-119	-8			material
500	-112	-98	-14	-9.0	n	degradation
	-443	-443	0			
	-427	-427	0	no	the layer did	completed
550	-405	-405	0	signal	not survive	sublimation

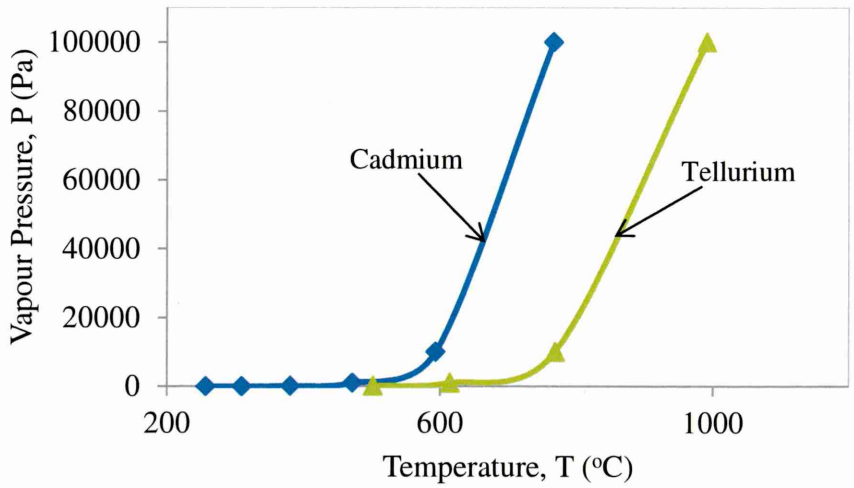

Figure 5.19: The vapour pressure of cadmium and tellurium as a function of temperatures [20].

Table 5.7 shows the PEC signal of CdTe thin films annealed at 420 and 450°C for 10, 15, 20 and 30 minutes. The as-deposited CdTe for this set of experiments is n-type with the PEC signal of -70 mV. Similarly, like previous results, the CdTe films have changed to p-type after being annealed at 420°C. The value of conductivity still remains p-type after 30 minutes annealing time. This result confirms that CdTe film is always p-type after being annealed at 420°C up to 30 minutes. Strangely, CdTe films annealed at 450°C are p-type in the first 10 to 15 minutes, and change to n-type conductivity after being annealed ≥20 minutes at 450°C. From previous work, we understand that the conversion of conductivity type of CdTe from p- to n-type occurs at a temperature of 450°C. But in this work we realise that the conversion of the conductivity type actually happens at a particular annealing temperature and annealing time. A longer annealing time causes material deterioration, oxidation, breakdown of bonds and sublimation. Under the appropriate conditions of annealing temperatures and time (420°C for ~20 min.), the material shows the optimum performance that we sought for the application in solar cell devices.

Table 5.7: The PEC signal of CdTe thin films for as-deposited and annealed CdTe at 420 and 450°C for 10, 15, 20 and 30 minutes.

Annealing Temperature, T (°C)	Annealing Time, t (min.)	$V_{Illumination}$ (mV)	V_{dark} (mV)	PEC Signal (V_{ill}-V_{dark}) (mV)	Average PEC signal (mV)	Conductivity type	Comments
As-deposited	-	-103	-35	-68	-68.0	n	-
		-104	-36	-68			
420	10	-14	-101	87	86.5	p	-
		-13	-99	86			
	15	-40	-103	63	65.0	p	-
		-34	-101	67			
	20	-19	-89	70	70.5	p	-
		-17	-88	71			
	30	-70	-91	21	22.0	p	material degradation
		-65	-88	23			
450	10	32	-30	62	62.5	p	-
		30	-33	63			
	15	-5	-17	12	14.0	p	-
		-4	-20	16			
	20	-10	3	-13	-14.0	n	material degradation
		-10	5	-15			
	30	71	140	-69	-62.5	n	material degradation
		80	136	-56			

DC conductivity measurements were carried out in order to determine the electrical conductivity of as-deposited and annealed CdTe layers. For these experiments, thicker layers were used in order to avoid leakage through pinholes. 2 mm diameter and circular ohmic contacts were made by evaporating Al layers for n-type samples and Au layers for p-type samples through a metallic mask. The resistance of CdTe layers was measured using I–V characteristics. The average resistance of each sample was measured and the conductivity was calculated with known thicknesses and areas of FTO/CdTe/Al or Au structures. Table 5.8 summarises the measurements of the average resistances, resistivity and electrical conductivity of as-deposited and annealed CdTe layers at different temperatures. Figure 5.20 shows that the value of electrical conductivity has increased from 6.97×10^{5} to 17.19×10^{5} $(\Omega cm)^{-1}$ after being annealed at temperatures of 420°C. The conductivity enhancement is due to the improvement of crystallinity, the enlargement of the grain size and the reduction of defects [21,22] which promote the higher mobility of electrons. However, a decrease in conductivity was observed for the $CdCl_2$ treated samples at annealing temperatures ≥450°C. This

could be due to the material breakdown, oxidation and sublimation of the layer at higher annealing temperatures and this trend is also consistent with the material deterioration observed in both the XRD and PEC analyses in previous sections.

Table 5.8: The summary of electrical properties of CdTe thin films annealed at different temperatures in the presence of $CdCl_2$. Note that these samples were grown at V_g=698 mV.

Annealing Temperature, T (°C)	Average Resistance (Ω)	Resistivity, ρ x 10^4 (Ωcm)	Conductivity, σ x 10^{-5} ($\Omega^{-1}cm^{-1}$)
As deposited	31.1	1.43	6.97
350	26.0	1.09	9.19
385	12.3	0.64	15.53
420	11.1	0.58	17.19
450	14.0	0.88	11.42
500	17.6	2.67	3.75

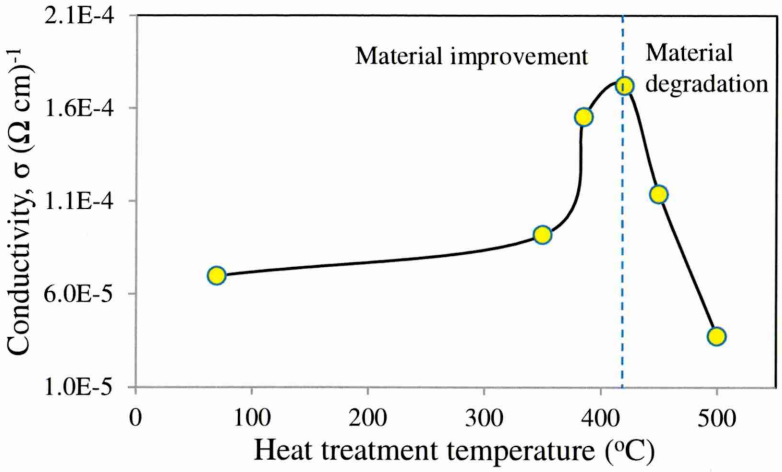

Figure 5.20: The electrical conductivity of CdTe at different annealing temperatures.

5.2.5 Morphological characterisation

Figure 5.21 shows the SEM images of CdTe thin films for as-deposited and annealed CdTe at 350, 385, 420, 450, 500 and 550°C in the presence of $CdCl_2$. The as-deposited CdTe shows the agglomeration size in a range of 150 to 200 nm. As the annealing temperatures were increased, the crystallites and agglomerations started to coalesce together forming larger grains. CdTe layers annealed at 350 to 450°C show a compact

grain growth without any gaps appearing. CdTe annealed at 420 and 450°C shows grain sizes in (700-900) nm and (1000-4000) nm ranges, respectively. It is an important point to note that the electrodeposition CdTe layers grown at low temperature (~65°) attained comparable grain sizes to CSS-CdTe after $CdCl_2$ treatment. However, annealing at 500°C and above seems to open up gaps between the grains. The formation of wide gaps, oxidation and material loss through sublimation also could form at too-high annealing process [23]. Figure 5.21 (g) shows the SEM image for CdTe annealed at 550°C. It exposes the FTO surface since CdTe layers sublime at very high annealing temperature. These observations confirm the results observed from the XRD, PEC and DC conductivity measurements in this work. The optimum annealing seems to be in between 420 and 450°C and this could be finalised during device fabrication.

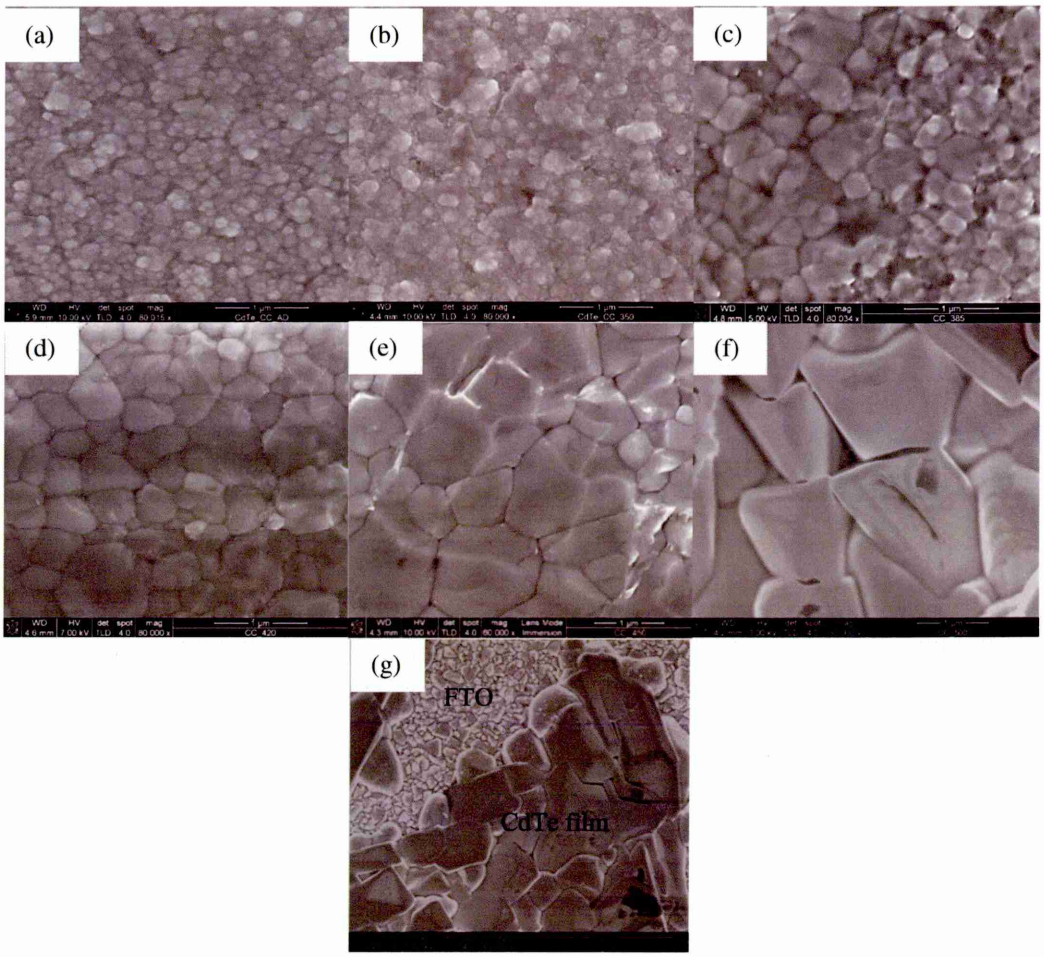

Figure 5.21: SEM images of CdTe grown at 698 mV for (a) as-deposited and annealed at (b) 350, (c) 385, (d) 420, (e) 450, (f) 500 and (g) 550°C for 20 minutes.

Figure 5.22 shows the SEM images for CdTe annealed at 420 and 450°C for 10, 15, 20 and 30 minutes. CdTe thin films treated at 420°C show an increasing of the grain size up to ~1000 nm as the annealing time increased to 30 minutes. Similarly, CdTe layers annealed at 450°C also demonstrated the grain growth with a longer annealing time. However, CdTe annealed at 450°C for 30 minutes showed a clear appearance of pinholes and gaps forming in between the grain boundaries. The existence of gaps in the CdTe layers is not a good sign since it will cause a catastrophic impact on the performance of solar cells due to short circuiting devices. Higher annealing temperatures like 450°C speed up the recrystallisation and grain growth, therefore it requires a short time for annealing. A longer time of annealing may set off over-treatment and destroy the properties of the layer. Therefore, from this work it is suggested that the annealing time for 420°C is up to 30 minutes while for temperatures of 450°C it is only up to 15 minutes.

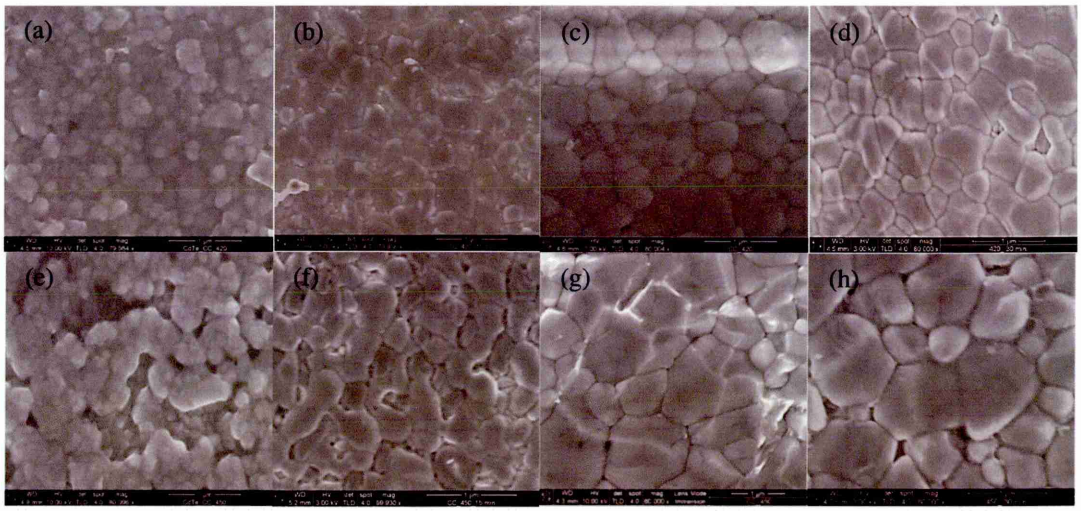

Figure 5.22: The SEM image of CdTe annealed at temperatures of 420°C for (a) 10, (b) 15, (c) 20 and (d) 30 minutes and 450°C for (e) 10, (f) 15, (g) 20 and (h) 30 minutes.

AFM is a convenient technique to study the morphology and surface roughness of thin films. Figure 5.23 shows the typical 1.0×1.0 μm 2D and 5.0×5.0 μm 3D AFM micrographs of (a) as-deposited and annealed CdTe films at temperatures (b) 385 (c) 420 and (d) 450°C. The brightness of these micrographs indicates the variation of depth of the surface morphology. It is observed that the as-deposited CdTe shows a surface with homogeneous brightness which suggest that the layer is uniform due to the formation of smaller grains. The annealed samples show a variation of brightness which

represents the formation of valleys and peaks on the surface. The roughness of the films increased as the annealing temperature increased due to the enlargement of the grain size especially forming columnar type grains, growing upwards. The average surface roughness for the as-deposited CdTe and $CdCl_2$ treated CdTe are shown in Table 5.9.

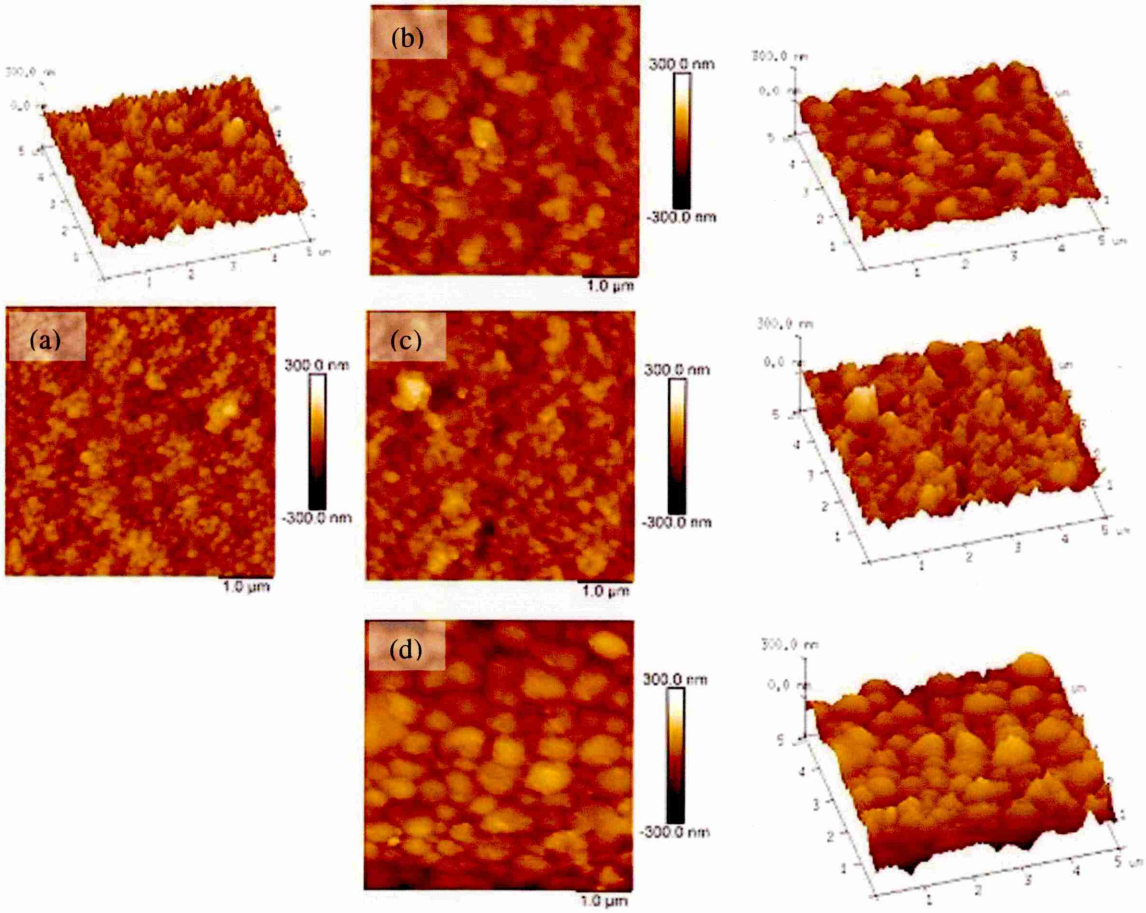

Figure 5.23: The AFM images of (a) as-deposited and annealed at (b) 385, (c) 420 and (d) 450°C for 20 minutes.

Table 5.9: The AFM data on surface roughness of CdTe thin films, as a function of annealing temperatures.

Sample	R_{ms} (nm)
As-deposited	25.7
$CdCl_2$ heat-treated at 385°C	38.0
$CdCl_2$ heat-treated at 420°C	54.3
$CdCl_2$ heat-treated at 450°C	68.7

5.2.6 Conclusion

The annealing temperature and annealing time of CdTe has been successfully studied from 350 to 550°C and from 10 to 30 minutes, respectively. All the samples survived except the sample treated at 550°C. The XRD characterisation demonstrated that the optimum temperature for annealing lies in between 420 °C, 20 minutes and 450°C, 10 minutes by referring to the (111), (220) and (311) peaks. The optical measurement characterisation demonstrates a reduction of bandgap with annealing which is due to the recrystallisation and increments in grain size and reduced stress. CdTe annealed at 500°C, however shows a larger bandgap due to the sublimation of the material at a too-high annealing temperature. This is associated with the reduction of thickness with a higher annealing time. CdTe layers demonstrated the conversion of the conductivity type n- to p- after being annealed above 350°C and below of 450°C, 10 minutes. The conversion of CdTe changed back to the n-type at 450°C, 20 minutes, and this is due to change of properties due to material degradation. The DC conductivity measurement shows that the conductivity increased as the annealing temperature increased due to the improvement of crystallinity and enlargement of the grain size which promotes the higher mobility of charge carriers. From SEM and AFM, the grain growth is observed with a higher annealing temperature but a too-high temperature and/or a too-long duration time in annealing deteriorates the CdTe films due to the gaps and pinholes formation. From this work, it is suggested that the best annealing temperature and time is either 420°C, 20 minutes or 450°C, 15 minutes. The summary of the characterisation in this section is shown in Figure 5.24.

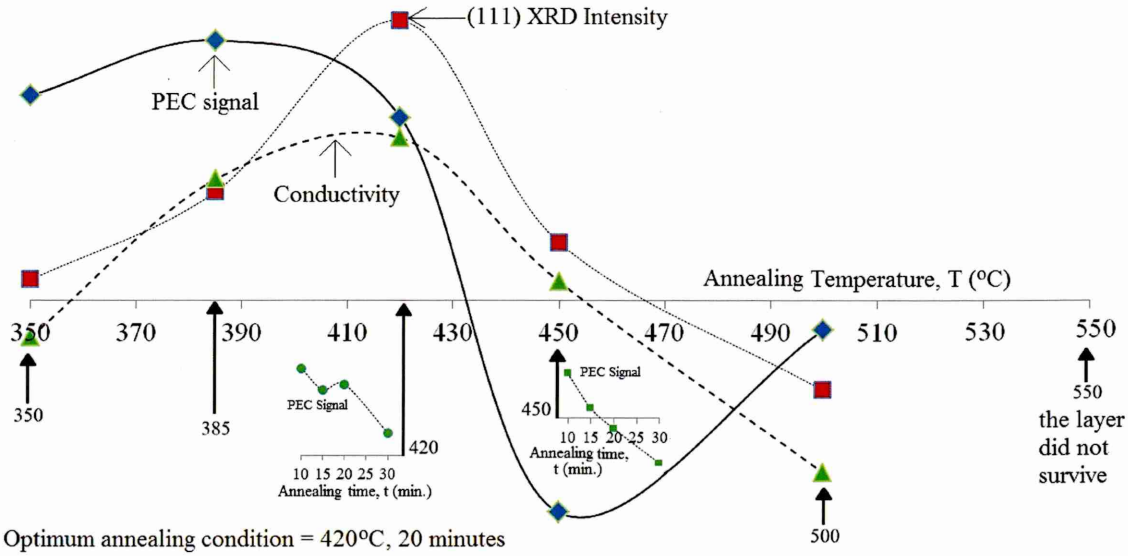

Figure 5.24: Graphical presentation of the summary of characterisation for annealing condition studies on CdTe thin films. The best annealing condition is observed at 420°C, 20 minutes.

5.3 Study the effect of chemical treatments on CdTe thin films

This section presents the work on the effect of chemical treatment on CdTe thin films. Three chemical treatments were used in this study. These are saturated $CdCl_2$ solution in deionised water, saturated $CdCl_2$+CdF_2 solution in deionised water and saturated $CdCl_2$+CdF_2+$GaCl_3$ in deionised water. All $CdCl_2$, CdF_2 and $GaCl_2$ have purities of 99.999%. To prepare the sample for this experiment, a glass/FTO with dimensions of 5.0×2.0cm^2 was cleaned, immersed into CdTe precursor and electrodeposited at 698 mV for ~3 hours. This sample was then cut into five pieces. One of the pieces was kept as a reference (as-deposited) sample. One of the pieces was annealed without any chemical treatment while the other three samples were annealed with $CdCl_2$ treatment, $CdCl_2$+CdF_2 treatment and $CdCl_2$+CdF_2+$GaCl_3$ treatment. The treatments were done by dipping the samples in the prepared chemical and allowing them to dry before the annealing process. The annealing was done at 420°C for 20 minutes in air. The details of the samples are shown in Table 5.10. These samples were then characterised via XRD, Raman spectroscopy, UV-Vis spectroscopy, optical profilometry, PEC cell measurement, DC conductivity measurement, C-V measurement, SEM and AFM for their structural, optical, thickness, electrical and morphological properties.

Table 5.10: The details of CdTe thin films with different chemical treatments.

Samples (identifier)	Sample details	Annealing Temp. and Time (°C, minutes)
AD	As-deposited	-
HT	Annealed in air	400°C, 20 minutes
CC	Annealed with $CdCl_2$ treatment	
CF	Annealed with $CdCl_2$+CdF_2 treatment	
GC	Annealed with $CdCl_2$+CdF_2+$GaCl_3$ treatment	

5.3.1 Structural characterisation

Figure 5.25 shows the XRD spectra of CdTe thin films for as-deposited, annealed CdTe without any chemical treatment and annealed with $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$ treatments. The results show the prominent peak of (111) together with other two crystallite peaks of (220) and (311) in the cubic crystal plane in all five conditions. In addition, a peak at 22.54° is attributed to the Cd_xTeO_y peak. However this peak did not show any clear change after annealing with various chemical treatments. Table 5.11 shows the intensities of (111), (220) and (311) peaks and the calculated intensity ratios of (220) and (311) peaks referring to (111) peak. It is observed that the CdTe annealed with chemical treatment improved (111) preferred orientation peak greater than those annealed without any chemical treatment. Similarly (220) and (311) peaks also improved when annealed with these three chemical treatments compared to annealing without chemical treatment. CdTe film annealed with $CdCl_2$ treatment shows the highest (111) peak while CdTe film annealed with $CdCl_2$+CdF_2 treatment shows the highest (220) and (311) peaks. This indicates the change in the preferred orientation of grains in the sample after treatment. Chemical treatment with the presence of $CdCl_2$ is well known to perform better structurally due to recrystallisation [4,6,17,21,24,25]. The presence of fluoride in ppm in the treatment demonstrated a rearrangement in the orientation of the crystallite due to the reduction of (111) peak and increase in the other two peaks of (220) and (311). Nicola and Echendu also observed a similar trend when treating CdTe films in the presence of fluoride [26,27]. Based on these peak intensities, it is suggested that treatment with $CdCl_2$+CdF_2 shows good polycrystalline properties.

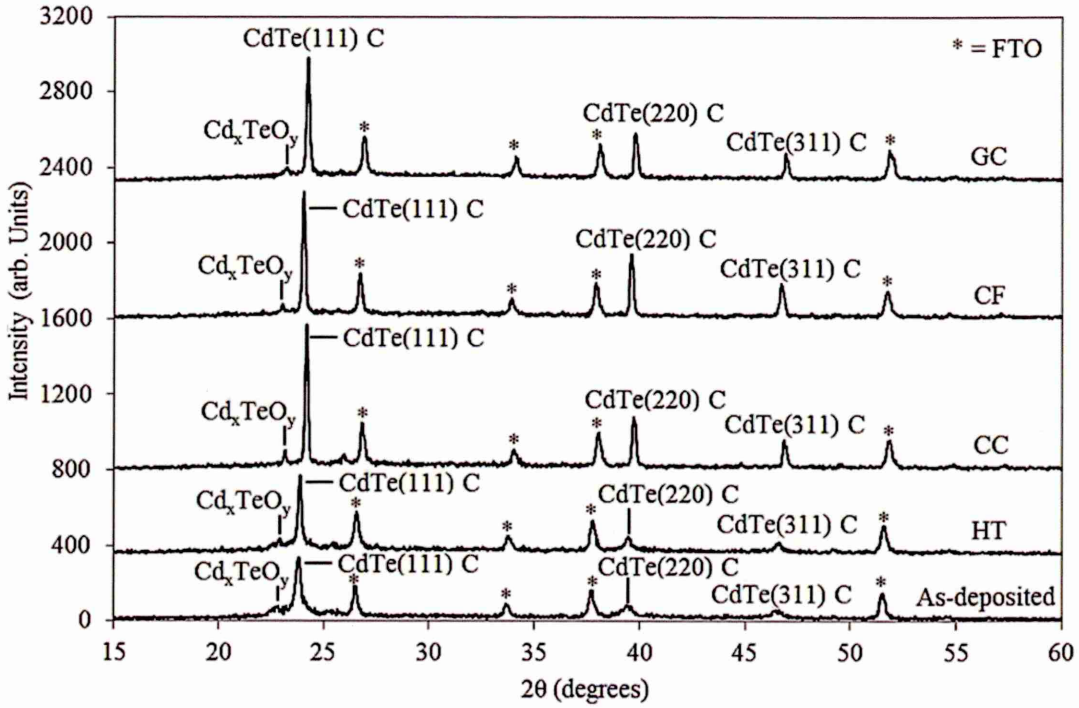

Figure 5.25: XRD peaks of CdTe thin films for as-deposited, annealed without any chemical treatment and annealed with $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$ treatments at 420°C for 20 minutes.

Table 5.11: Analysis of XRD peaks of CdTe for as-deposited, annealed in air and annealed with different chemical treatments at 420°C for 20 min.

CdTe Sample annealed with different treatments	Peak intensity			% peak relative to 111 peak		
	(111)	(220)	(311)	(111)	(220)	(311)
As-deposited	289	43	17	100	15	6
HT	407	44	27	100	11	7
CC	750	229	132	100	31	18
CF	694	321	174	100	46	25
GC	663	215	98	100	32	15

The Raman spectroscopy is an alternative and convenient method to identify material phases and determine the degree of crystallinity of the thin films. In this technique, vibrational, rotational and other low-frequency modes in materials are observed based on inelastic scattering of monochromatic radiation. The excitation source used in this work was a 514 nm argon ion laser. The spectra of Raman spectroscopy for as-deposited and $CdCl_2$ treated CdTe are shown in Figure 5.26. All the samples show the prominent peak of transverse optical (TO) of CdTe together with the elemental Te at wave numbers of ~142 cm^{-1}. This peak shifted from 139.2 to 139.0 cm^{-1} after annealing

without any chemical treatment. However, the Raman shift increased to 140.4, 141.8 and 140.8 cm^{-1} after annealing with $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$, respectively. Similarly, this trend was also observed for longitudinal optical (LO) CdTe at ~164 cm^{-1}. The trend of these blue shifts is due to the energy gained by the photon by increasing the vibration mode and the lattice strain. The increase in the Raman shift is usually observed together with the increment in the FWHM peak. Also noticed is that the FWHM of these peaks increased after annealing with chemical treatments. There are two possible effects influencing the FWHM of the Raman peak which are size effect and the lattice dislocation effect [28]. In this case, the size effect is more pronounced since we observed the enlargement in a crystallite size after annealing with chemical treatments as shown in Figure 5.31. This trend is similar to the previous XRD results. The summary of the Raman analysis is presented in Table 5.12.

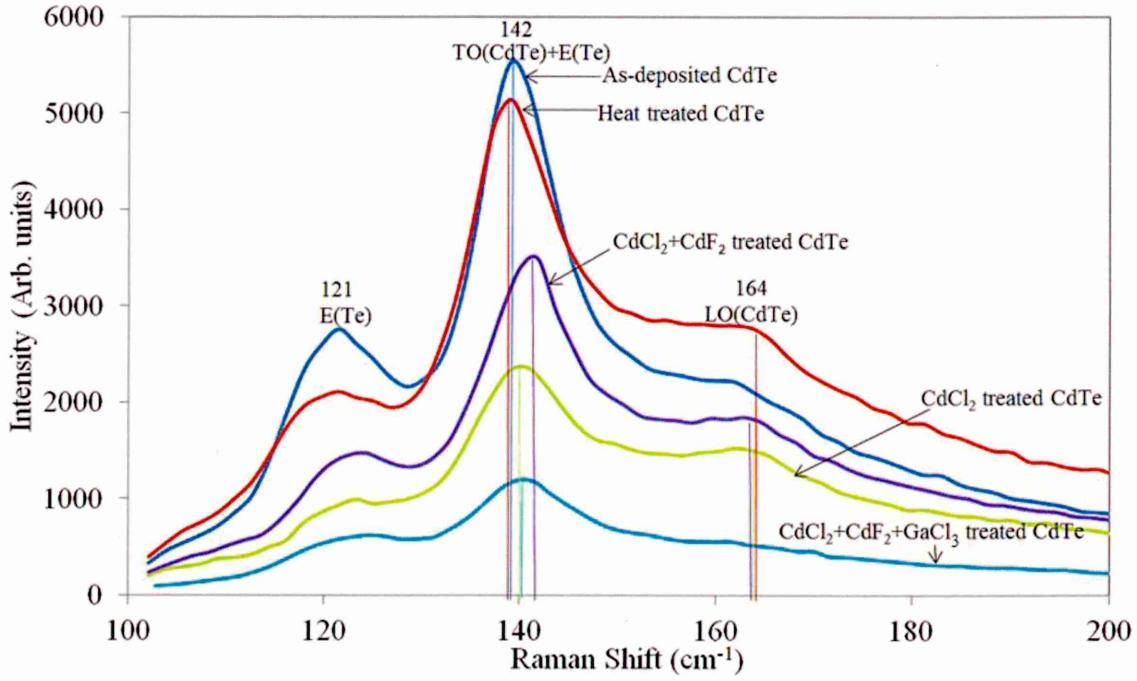

Figure 5.26: Typical Raman spectra of CdTe thin films for as-deposited, annealed without any chemical treatment and annealed in a presence of $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$.

Table 5.12: Summary of Raman peaks observed in Figure 5.24 for as-deposited, annealed CdTe films without any chemical treatment and annealed with $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$.

	Peak 1:	Peak 2:	Peak 3:

	Elemental Te			Transverse optical CdTe + Elemental Te			Longitudinal Optical CdTe		
Samples	Peak Position (cm^{-1})	Intensity (a.u)	FWHM (cm^{-1})	Peak Position (cm^{-1})	Intensity (a.u)	FWHM (cm^{-1})	Peak Position (cm^{-1})	Intensity (a.u)	FWHM (cm^{-1})
AD	121.5	2759	5.29	139.2	5538	7.0	161.9	2212	3.52
HT	121.4	2055	5.36	139.0	5138	7.2	163.7	2766	5.32
CC	122.5	930	5.56	140.4	3306	8.4	163.2	1503	5.32
CF	123.2	1410	5.39	141.8	2359	8.8	162.9	1845	3.52
GC	123.0	604	6.73	140.8	1192	8.8	-	-	-

5.3.2 Optical characterisation

Figure 5.27 and Table 5.13 show the graph of square of absorbance versus photon energy and the energy bandgap values of CdTe films for as-deposited and annealed without and with different chemical treatments. These results demonstrated the increase in the energy gap from 1.43 eV in the as-deposited CdTe film to ~1.46 eV after annealing without any chemical treatment in air. Annealing with the presence of $CdCl_2$+CdF_2 treatment increased the energy gap up to ~1.47 eV. However, CdTe annealed with $CdCl_2$ and $CdCl_2$+CdF_2+$GaCl_3$ shows a lower increment in energy bandgaps. The gradual bandgap increment is could be due to the sublimation of the material, reduced in film thickness and oxidation. Also, it is observed that both of the samples have higher absorbance spectra compared to others. The absorption edges also are improved after being annealed with chemical treatments. This could be due to the removal of the defects during these chemical treatments improving the material properties.

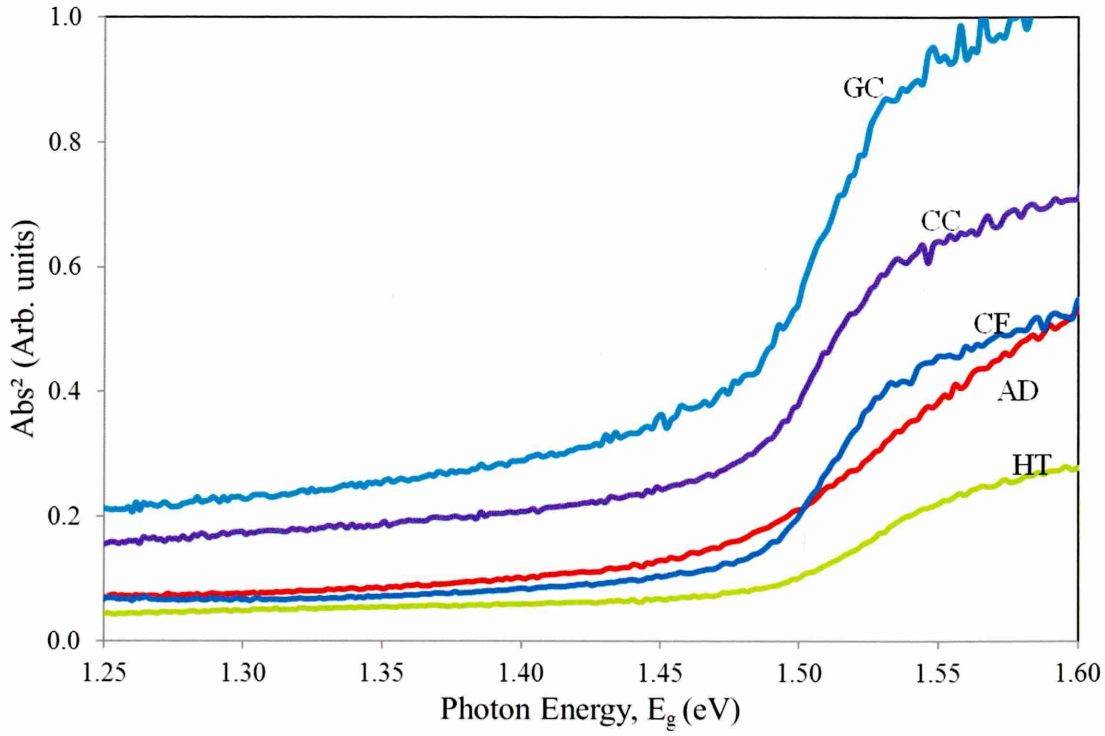

Figure 5.27: Optical absorption of as-deposited, annealed without any chemical treatment and annealed with $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$ CdTe samples.

Table 5.13: The energy bandgap of CdTe layers for as deposited, annealed without any chemical treatment and annealed with $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$.

Samples	Energy bandgap, E_g (eV)
AD	1.43
HT	1.46
CC	1.45
CF	1.47
GC	1.44

5.3.3 Electrical characterisation

Figure 5.28 shows the PEC measurements of CdTe as a function of growth voltage for as-deposited and annealed without and with three different chemical treatments. As discussed in section 5.1.5., the conductivity of as-deposited CdTe thin films electrodeposited from chloride precursor are n-type at $V_g \leq 698$ mV and p-type at $V_g \geq 700$ mV. After annealing without any chemical treatment, the majority of the samples move towards p-type conductivity. Samples grown at $V_g \leq 694$ mV are still n-type but the PEC signals have reduced and showing the movement towards p-type.

It was also observed that when CdTe films are annealed in the presence of $CdCl_2$ and $CdCl_2$+CdF_2, all samples become p-type in electrical conductivity. The $CdCl_2$ treatment could change the doping concentration when it makes complexes with currently unknown native defects in CdTe and produce p-type CdTe after $CdCl_2$ treatment. Due to the high diffusivity, the presence of fluoride enhanced the treatment and made it become more p-type. This experiment provides a clue for CdTe becoming p-type in electrical conductivity when high concentrations of Cl or both Cl and F are present in the materials.

CdTe thin films annealed with $CdCl_2$+CdF_2+$GaCl_3$ treatment have changed the as-deposited p-CdTe at $V_g \geq 706$ mV into n-type. This could be due to the effect of the Ga melt dissolving the Te precipitations which migrate to the top of the surface films during annealing in the presence of Ga. Fernández also has observed that Ga-inclusion in CdTe dissolved the Te precipitates in CdTe and doped CdTe with n-type [29]. The effect of Ga seems to be two fold; making the CdTe material more stoichiometric by removing excess Te, and doping CdTe layer to make it n-type in electrical conduction.

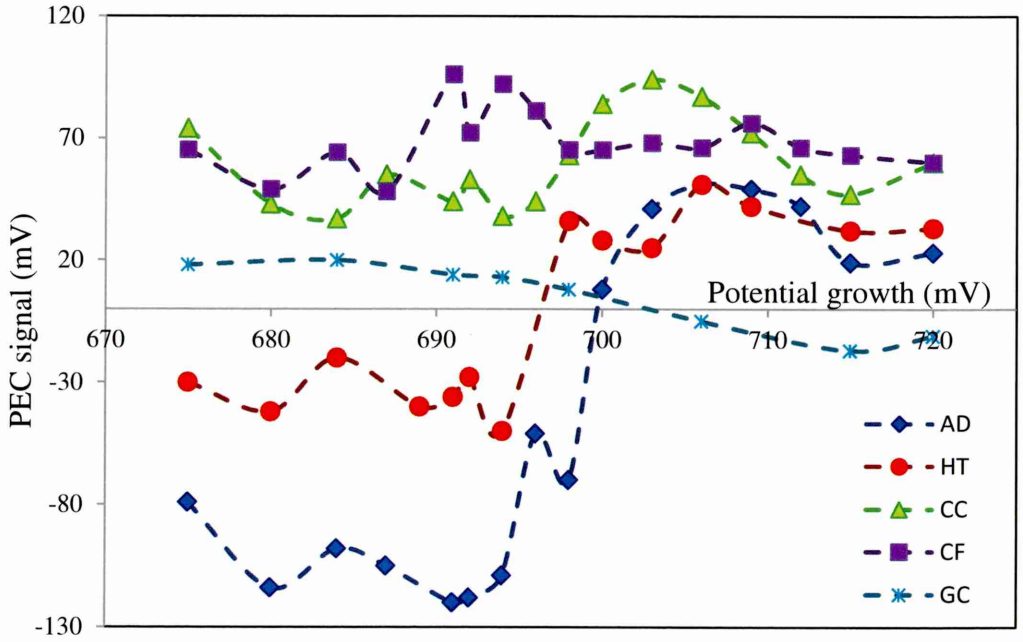

Figure 5.28: PEC signal of CdTe thin films for as-deposited, annealed without any chemical treatment and annealed with the presence of $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$.

Based on these results, samples of AD, HT, CC, CF and GC grown at V_g=698 mV were used with DC conductivity measurements and C-V measurements. These samples were cut in to two pieces and half of each sample was used for the DC conductivity measurement while another half was used for the C-V measurement.

In the DC conductivity measurement, a 2 mm diameter of circular ohmic contacts were created on the p-type CdTe by sputtering Au layers while the Al layers were sputtered onto n-type CdTe. The resistance of the CdTe layers was estimated through I-V measurements at several points of contact. The average resistance of each sample was measured and the electrical conductivity was calculated and shown in Table 5.14. Similar to the previous CdTe set, the as-deposited CdTe film in this batch has conductivity in the order of 2.63×10^{-5} $\Omega^{-1}cm^{-1}$. CdTe layers annealed without any chemical treatment show the lowest conductivity value of 5.87×10^{-6} $\Omega^{-1}cm^{-1}$ compared to those samples annealed with $CdCl_2$, $CdCl_2$+CdF_2, and $CdCl_2$+CdF_2+$GaCl_3$ treatments. This result is quite expected since CdTe films annealed with chemical treatments always have better electrical properties due to the removal of defects, enlargement of grains size and improvement in material properties. Annealing without any chemical treatment is not enough to remove the defects and improve the movement of the free electrons to the conduction band. Among all three chemical treatments, CdTe annealed with $CdCl_2$+CdF_2 shows better conductivity compared to other chemical treatments.

Table 5.14: The conductivity type (from PEC measurements) and electrical conductivity value (from DC conductivity measurements) of CdTe thin films as-deposited and annealed without any chemical treatment, annealed with $CdCl_2$, $CdCl_2$+CdF_2, and $CdCl_2$+CdF_2+$GaCl_3$ treatments.

Sample	Conductivity type/ contact	Average resistance, R (Ω)	Thickness (μm)	Resistivity, ρ x 10^4 (Ωcm)	Conductivity, σ x 10^{-5} ($\Omega^{-1}cm^{-1}$)
AD	n-type / Al	181.8	1.5	3.81	2.63
HT	p-type / Au	651.0	1.2	17.04	0.59
CC	p-type / Au	29.7	1.2	0.77	12.91
CF	p-type / Au	157.1	1.2	4.11	2.43
GC	p-type / Au	47.5	1.2	1.24	8.05

As for C-V measurement, Schottky contacts with 2mm diameter circles were created by evaporating the Al layer to the p-type CdTe. The p-type CdTe in this particular set is that annealed without any chemical treatment and annealed with $CdCl_2$, $CdCl_2$+CdF_2, and $CdCl_2$+CdF_2+$GaCl_3$ treatments. The as-deposited sample with the n-type conductivity was evaporated with Au to form the Schottky contact. The Mott-Schottky graph was plotted and a linear dependence has been obtained. From the slope of such a curve, the doping density was calculated using equations 3.15 to 3.18 disclosed in Chapter 3. The results of the C-V measurements are summarised in Table 5.15. It shows that the doping concentration of CdTe is reduced after annealing, both without any chemical treatments and with all the chemical treatments. CdTe annealed with $CdCl_2$+CdF_2+$GaCl_3$ shows the lowest doping concentration compared to other samples. Ideally, a healthy depletion region can be achieved with the doping concentration lower than ~1.0×10^{14} cm^{-3} [30]. From these experiment results, it is observed that all the layers are good since the stoichiometric layer of CdTe grown at V_g=698 mV has a doping density of ~10^{13} cm^{-3}. CdTe annealed in the presence of $CdCl_2$+CdF_2+$GaCl_3$ is suggested for solar cell fabrication since it shows the lowest carrier concentration (n=7.86×10^{11} cm^{-3}) and is expected to produce wider depleted device of PV active. However, the Mott-Schottky graph in in Figure 5.29 is not linear as expected due to the voltage distribution at the CdTe surface, band bending and defects. The C-V and $1/C^2$ versus V plots observed for CdTe treated with $CdCl_2$+CdF_2+$GaCl_3$ are shown in Figure 5.29 below.

Table 5.15: The summary of material parameters calculated from the C-V measurements and the mobility of electrons of as-deposited CdTe films and the mobility of holes of CdTe films annealed without and with $CdCl_2$, $CdCl_2$+CdF_2, and $CdCl_2$+CdF_2+$GaCl_3$ treatments.

Sample	Schottky contact	Sample	Slope of graph $\frac{1}{C^2}$ versus V	Carrier concentration, n (cm^{-3})	Mobility, μ ($cm^2V^{-1}s^{-1}$)
AD	n-CdTe / Au	AD	$2.28x10^{20}$	5.70×10^{13}	2.88
HT	p-CdTe / Al	HT	$4.75 x10^{20}$	2.73×10^{14}	0.13
CC	p-CdTe / Al	CC	$1.71 x10^{20}$	7.60×10^{13}	10.57
CF	p-CdTe / Al	CF	$4.93 x10^{20}$	2.63×10^{13}	5.77
GC	p-CdTe / Al	GC	$1.66 x10^{22}$	7.86×10^{11}	638.87

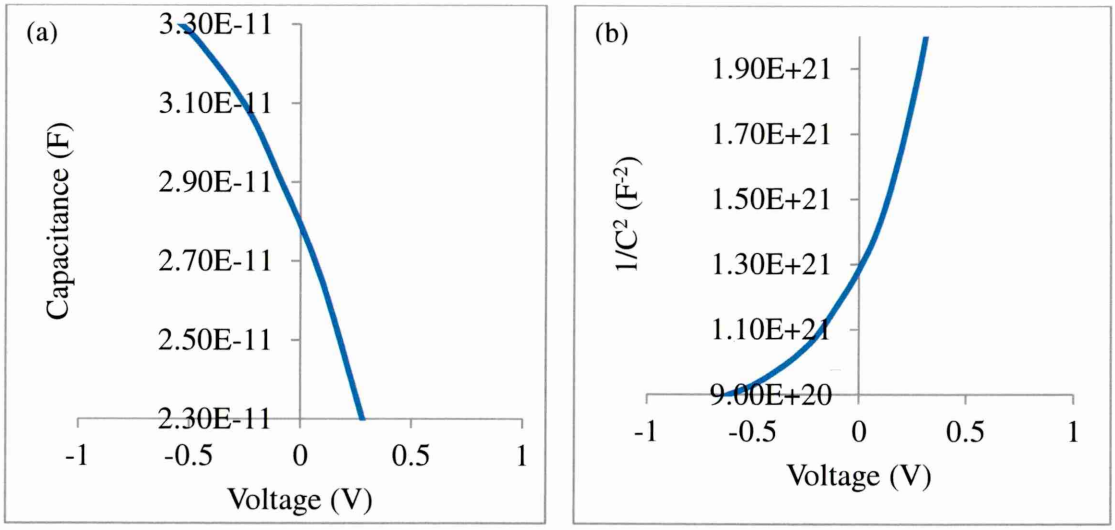

Figure 5.29: The graphs of (a) C-V and (b) $1/C^2$ versus V for CdTe film treated with $CdCl_2$+CdF_2 +$GaCl_3$ treatment.

Using the electrical conductivity and doping density values calculated from the DC conductivity measurements and the CV measurements respectively, the mobility of these layers was calculated using equation 5.2 and presented in Table 5.15. These values represent the mobility of charge carriers normal to the FTO substrates ($\mu_\perp$) rather than mobility values reported in the literature by measuring Hall Effect ($\mu_\parallel$), which is the mobility of charge carriers parallel to the FTO substrate. The

illustration on mobility values observed in this work ($\mu_{\perp}$) can be represent in Figure 5.30 below.

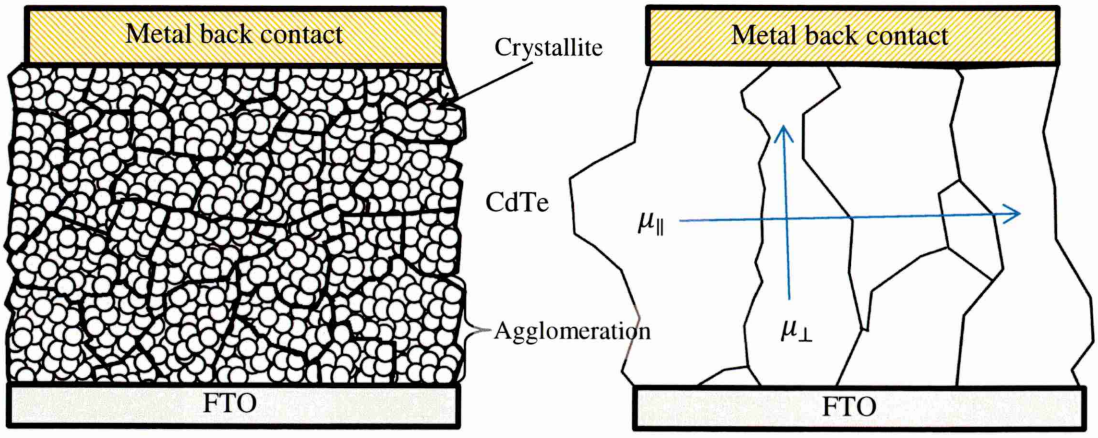

Figure 5.30: The schematic diagram of (a) as-deposited CdTe material with agglomeration consisting of ~50 nm size crystallites and (b) heat treated materials with larger grain size of few microns across the layer.

As-deposited CdTe consists of large agglomerations with smaller crystallites (~50 nm). Therefore in n-type as-deposited CdTe ,the electrons suffer grain boundary scattering when traveling in both direction, parallel to FTO and normal to the substrate. Therefore, the measured electron mobility is fairly low (2.88 $cm^2V^{-1}s^{-1}$).

When heat treated with chemical treatments, these agglomerations and smaller crystallites form larger grains with size in few microns across the layer as shown in Figure 5.30. This is clearly shown by the SEM work presented in the next section (Figure 5.31). From PEC measurements, all the annealed CdTe layers become p-type in electrical conduction (see Table 5.14) and therefore the estimated mobilities are holes mobilities. The highest mobility observed is 638.87 $cm^2V^{-1}s^{-1}$ for CdTe annealed in the presence of $CdCl_2$+CdF_2+$GaCl_3$,. In this case, the holes move along the fully crystalline grains from the FTO to Au contacts and there are no grain boundaries to hinder the charge carrier movements. Because of this reason, the experimentally observed hole mobility is $\mu_{\perp}$and the electron mobility could be one or two orders of magnitude higher. This shows the benefits of having micro-size columnar type grains in solar cell. In addition to this high mobility, the larger grains material introduce active PV junction along the grain boundaries due to melting and diffusion of doped into CdTe grains. The combination of these vertical junctions at grain-boundaries together with the main rectifying junction of the CdS/CdTe solar cell leads to transfer of electrons and holes in

different paths and minimise the recombination [6]. This will provide the future research direction for producing high efficiency solar cells.

5.3.4 Morphological characterisation

The effect of chemical treatment on the morphology of CdTe thin films was investigated through SEM and AFM. Figure 5.31 shows the SEM images of CdTe films for (a) as-deposited, (b) annealed without any chemical treatment and annealed with the presence of (c) $CdCl_2$, (d) $CdCl_2$+CdF_2 and (e) $CdCl_2$+CdF_2+$GaCl_3$ treatments at 420°C for 20 minutes. It is observed that the grain sizes increased tremendously after being annealed with all three types of chemical treatments. It is well known that the presence of $CdCl_2$ in the heat treatment has enhanced the coalescence of smaller nano-crystallites into larger crystals to improve material layers. The presence of fluoride in the chemical treatment shows a higher improvement in the grain growth than chemical treatment with only $CdCl_2$ since fluoride atoms are easier to diffuse into the grain boundaries due to their smaller atomic radii than chloride atoms [31]. Mazzamuto also reported an advantage of annealing CdTe films in the presence of CHF_2Cl_2 in CSS-CdTe [32]. For these reasons the results show that CdTe annealed with $CdCl_2$+CdF_2 demonstrated the largest grain size compared to other chemical treatments.

Many researchers observed the grain growth appearance together with gaps in between grain boundaries after $CdCl_2$ treatment. However, CdTe layers grown in this work show a compact grain growth without any gaps appearing after being annealed with both $CdCl_2$ and $CdCl_2$+CdF_2 treatments. This suggests that the CdTe produced from chloride precursor has a better quality for solar cell devices since it has no obvious gaps and has larger grain sizes for less scattering at the grain boundaries and with high charge carrier mobility. However, the sample annealed with the presence of $CdCl_2$+CdF_2+$GaCl_3$ shows the presence of small voids and gaps in between the grain boundaries as shown in Figure 5.31 (e). As observed before, this can be avoid by reduced the annealing temperature and/or annealing period.

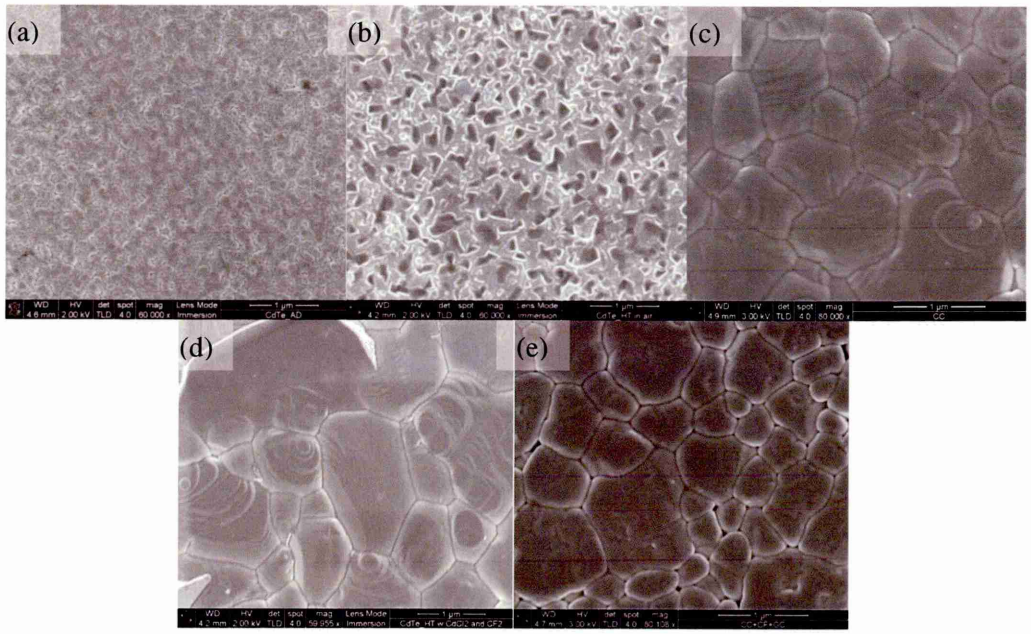

Figure 5.31: SEM images of the CdTe thin films for (a) as-deposited, (b) annealed without any chemical treatment, and annealed with (c) $CdCl_2$, (d) $CdCl_2$+CdF_2 and (e) $CdCl_2$+CdF_2+$GaCl_3$ treatments.

Figure 5.32 shows 1.0 μm scale of 2-D images and 5 μm scale of 3-D images of AFM micrografts of CdTe films used in this experiment. Many researchers report that the surface roughness increases after $CdCl_2$ treatment [33,34]. This observation is in agreement with the results in Figure 5.30. This is due to the formation of larger grains forming the variation of surface roughness in thin films. Thin film with a higher surface roughness is unhealthy for devices since it may create discontinuities in the back metal contact if the contacting metal layer thickness is less than the surface roughness of the CdTe film. However the issue on this can be solved by using thicker back electrical contacts in device fabrication.

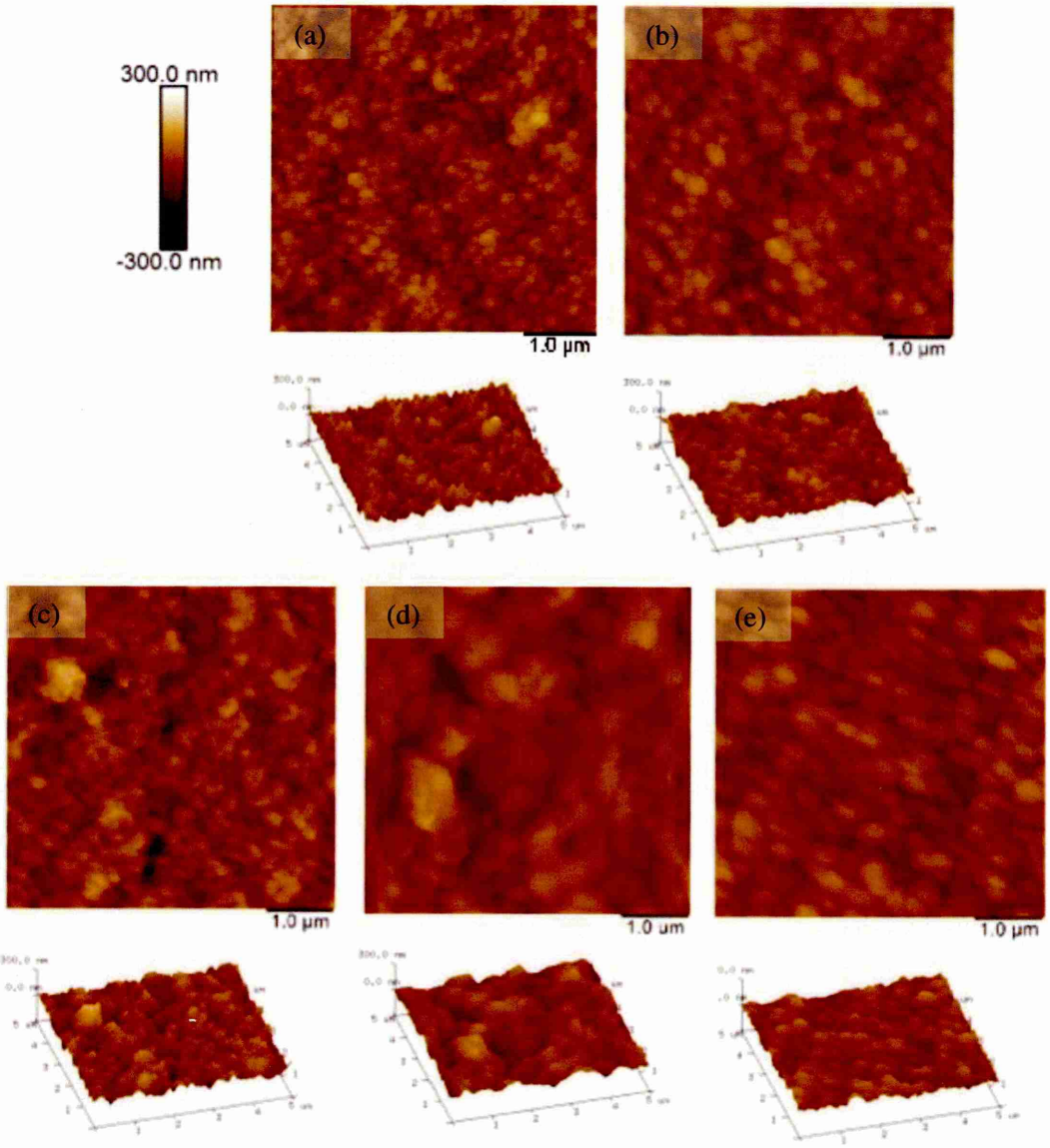

Figure 5.32: The AFM images of CdTe films for (a) as-deposited, (b) annealed without any chemical treatment, and annealed with (c) $CdCl_2$, (d) $CdCl_2$+CdF_2 and (e) $CdCl_2$+CdF_2+$GaCl_3$ treatments at 420°C for 20 minutes.

5.3.5 Conclusion

The effect of the chemical treatments of CdTe thin films has been studied with three different chemical treatments which are $CdCl_2$, $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$. The samples were treated with these chemicals and annealed at 420°C for 20 minutes. The as-deposited and annealed CdTe without any chemical treatment at 420°C have also been prepared for reference samples. The XRD characterisation demonstrated that the presence of fluoride in ppm in the treatment demonstrated a rearrangement in the orientation of the crystallite and increased the (220) and (311) peaks to form a

polycrystalline structure. The FWHM of TO-CdTe and LO-CdTe in the Raman peaks are slightly increased after being annealed with chemical treatments which is suggested due to the size effect. The optical absorption shows a high absorption for the materials treated with $CdCl_2$ and $CdCl_2$+CdF_2+$GaCl_3$. PEC measurements demonstrated that no matter the electrical conductivity of the as-deposited CdTe, all of them become p-type after being treated with $CdCl_2$ and $CdCl_2$+CdF_2. Contrary, CdTe treated with $CdCl_2$+CdF_2+$GaCl_3$ changes the as-deposited p-CdTe at $V_g \geq 706$ mV into n-type due to the effect of Ga which dissolved the Te precipitations to the surface. The DC conductivity and C-V measurements demonstrated the remarkable value of holes mobility on samples treated with $CdCl_2$+CdF_2+$GaCl_3$. This suggested that this treatment may provide high device parameters if applied in solar cell fabrication. SEM and AFM measurements demonstrated the tremendous grain growth if these samples were annealed with chemical treatments but treatment under $CdCl_2$+CdF_2+$GaCl_3$ shows small voids and gaps in between grain boundaries. This may need re-adjustment of the annealing temperature and duration of the heat treatment in $CdCl_2$+CdF_2+$GaCl_3$ condition. This work provides more understanding of the importance of the chemical treatment especially the presence of $CdCl_2$ for better material properties for solar cells. Annealing with chemical treatment shows better properties. During the annealing, the halogen atoms, such as chloride and fluoride diffuse at the grain boundaries and changed the doping concentration at the skin of grain. A small crystallite merged into a larger grain by 'Ostwald ripening' where small grains coalesce together to form larger grains. The presence of $CdCl_2$ is well known to be able to enhance recrystallisation and grain growth, change the electrical conductivity type and doping concentration, reduce the defect and remove the Te precipitates [6,24,30]. Many researchers also found out that $CdCl_2$ treatment can work well if it is used mixed with a gas containing fluorine [27,32,35]. Based on the peak intensities, it is suggested that treatment with $CdCl_2$+CdF_2 appears to produce better polycrystalline properties than those chemically treated with only $CdCl_2$ or in the presence of $GaCl_3$.

5.4 Overall conclusions

CdTe thin films have successfully grown by electrodeposition from an aqueous electrolyte bath containing $CdCl_2 \cdot H_2O$ and TeO_2. These layers demonstrated good adhesion to the FTO/glass substrate. From the study on the growth voltages of CdTe deposition in the first section, the best V_g was obtained at 698 mV with respect to

calomel electrode for both as-deposited and after $CdCl_2$ treatment. Electrodeposition technique shows the possibility of growing p-, i- and n-type CdTe layers by tuning the V_g during electrodeposition. From the observation, the n-type layers have better conductivities than p-type CdTe layers and the layers grown in the n- stoichiometric region show the highest mobility than others. The annealing temperature and time have also been studied systematically from 350 to 550°C and from 10 to 30 minutes, respectively. The best annealing temperature and time for the CdTe films in this work lies in between 420 °C, 20 minutes and 450°C, 15 minutes. More harsh condition than this, the CdTe thin film will be oxidised, deteriorated, sublimed, lose material and formed pinholes. The effects of chemical treatments on CdTe during annealing have also been studied and they show that the CdTe thin films annealed in the presence of fluoride and galium in ppm demonstrated better properties. The application of CdTe as an absorber layer will be further studied in the form of solar cell device performance.

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Chapter 6 - Characterisation of PAni thin films

6.0 Introduction

This chapter presents research work on the pinhole plugging layer used in solar cell devices, polyaniline (PAni). PAni thin films have been grown by the electrodeposition technique. The study on the growth conditions, annealing temperatures and pH have been carried out with various characterisation techniques, such as XRD, UV-Vis spectroscopy, optical profilometry, DC conductivity measurements and SEM. The aim of this work is to establish the growth of PAni thin films, using the electrodeposition technique, and to understand the properties of PAni thin films under numerous conditions before using them for plugging pinholes or as buffer layers in the solar cell device structure. The chapter has been divided into three main sections, which have been summarised in the flowchart in Figure 6.1.

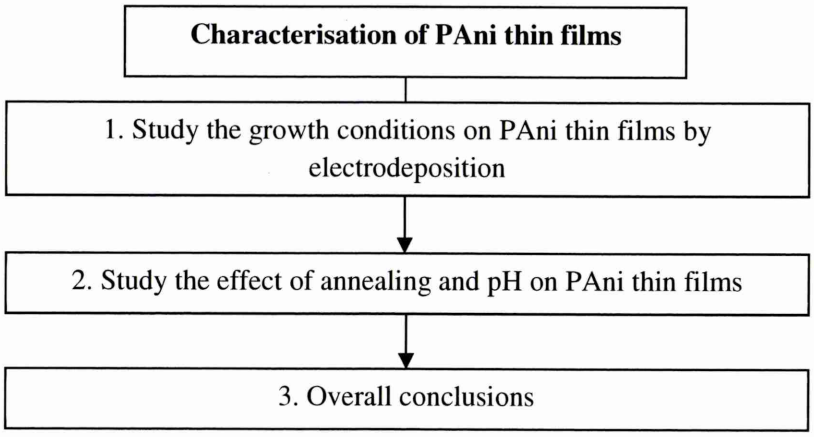


Figure 6.1: Flow chart of the growth and characterisation of PAni thin films.

6.1 Study the growth conditions of the PAni thin films by electrodeposition

This section presents the study on the growth conditions of PAni thin films by electrodeposition technique. Chemical oxidative polymerisation of PAni thin films from anodic deposition has been reported by many researchers [1-4]. However, Shao and Xhuzheel'skii also reported the possible growth of PAni thin films using cathodic deposition [5-6]. PAni can be formed in three phases; leucoemeraldine, emeraldine and pernigraniline. The anodic deposition forms the oxidation base of PAni, called pernigraniline, whereas the cathodic deposition produces a reduction base of PAni, leucoemeraldine. In this work, the attempt to grow PAni from both anodic and cathodic deposition has been made, and the deposited layers have been characterised and

compared. In the beginning, cyclic voltammograms for anodic and cathodic depositions were carried out in order to estimate the suitable voltage for the film deposition. Using the estimated voltage range, PAni thin films were grown at different growth voltages and the growth conditions were optimised after characterisation. The effect of deposition times in both deposition techniques will also be presented in this section. The electrodeposited films were studied for their structural, optical, thickness and morphological properties by XRD, UV-Vis spectroscopy, optical profilometer and SEM.

6.1.1 Voltammogram

The 0.10 M electrolyte was prepared by dissolving aniline in 300 ml of deionised water. The synthesis was based on mixing an aqueous solution of aniline in deionised water with 0.01 M sulphuric acid, H_2SO_4 and ammonium hydroxide, NH_4OH function as dopant and oxidising agent respectively, and as reagents to adjust pH to 2.20±0.02. Figure 6.2 shows the cyclic voltammogram of the electrolyte during the anodic scan from -100 to 2000 mV. The voltammogram provides information on the passage of electric current through the electrolyte and hence the materials deposition details. This has been used to study electropolymerisation of PAni and to estimate the suitable voltage range for PAni electrodeposition. The arrows indicate the forward and reverse cycles. It is shown that the PAni starts to electrodeposit at ~111 mV while in the reverse sweep the layer starts to dissolve at ~405 mV. A single hump, which indicates the peak of oxidation was also observed at the voltage range of ~750 to ~850 mV. Also, the nucleation loop is observed at ~450 mV in Figure 6.2 due to the homogeneous follow-up reaction of soluble oligomers on the layer and the coupling steps between "dimers" and the subsequent. The polymerisation of aniline involves the formation of anilinium radical cation by aniline either by oxidation or reduction, radical coupling, increasing of chains and organisation into complex super-molecule structure to form solid PAni layer on the electrode [7,8]. In anodic deposition, the oxidation of the monomer at anode leads to formation of soluble oligomers. The detailed study on the anodic deposition at the growth potential around 750 to 850 mV was carried out to optimise the V_g for PAni.

Figure 6.3 shows the cyclic voltammogram of aqueous solution of the same solution through cathodic scan during the forward and reverse cycles between -100 to 2000 mV. The graph shows that electrodeposition of PAni starts at ~845 mV, while in a reverse sweep the layer starts to dissolve at ~1100 mV. In the cathodic voltammogram,

there are two humps, which indicate the reduction peak at the voltage range of ~1120 to ~1200 mV and ~1600 to ~1700 mV. The further rise in the voltage beyond 1800 mV can be assigned to complete reduction of PAni to the leucoemeraldine base. The detailed study on the growth potential of 1600-1700 mV (second peak) was carried out to optimise the V_g for PAni.

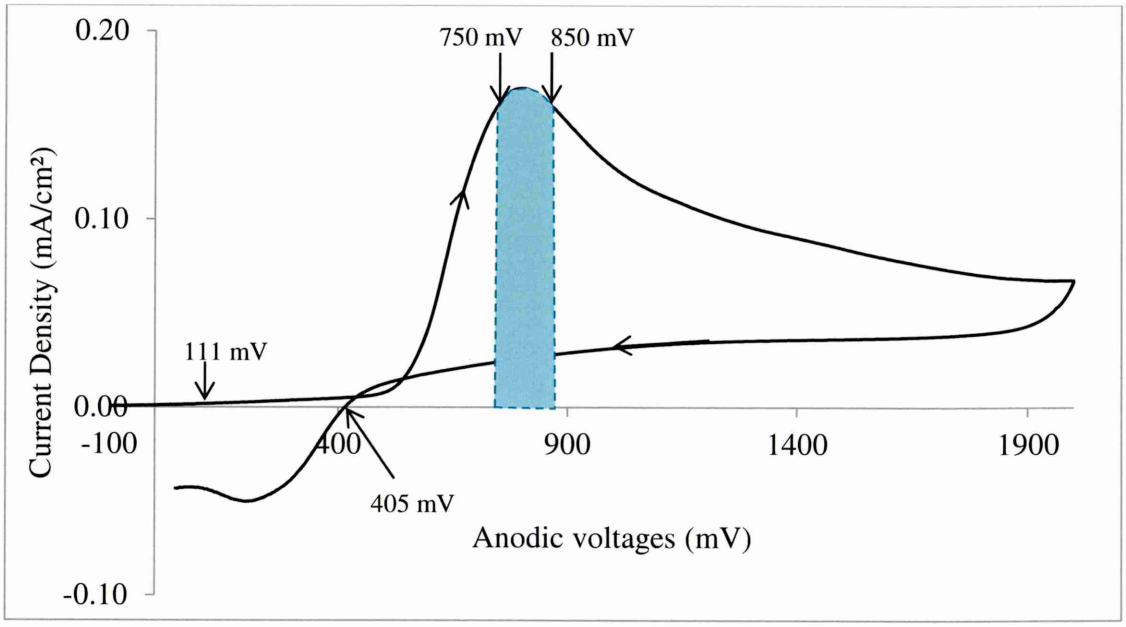


Figure 6.2: Cyclic voltamogram of anodic electrodeposition of PAni in aqueous aniline solution with glass/FTO as the anode and carbon rod as the cathode.

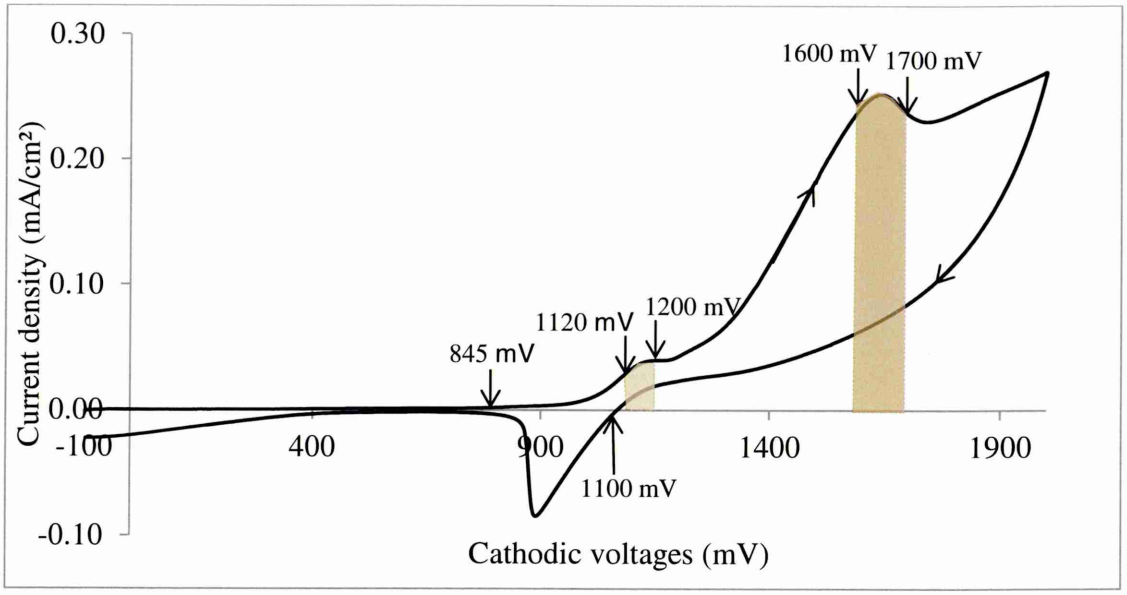


Figure 6.3: Cyclic voltamogram of cathodic deposition of PAni in aqueous aniline solution with glass/FTO as the cathode and carbon rod as the anode.

6.1.2 Structural characterisation

Figure 6.4 shows the XRD spectra of PAni layers, grown from anodic deposition at voltages in the range of 750 and 850 mV. Figure 6.4 demonstrated the absence of any sharp diffraction line except the FTO peaks. Additionally, a very small hump at 2θ=44.0° is observed for samples grown at 750 and 780 mV. This suggests that pernigraniline base of PAni films are amorphous in nature, similar to the results reported by other researchers [1,9,10]. The lack of amorphous hump in XRD spectra is could be due to the very thin layer of electrodeposited PAni (~200 nm).

Figure 6.5 shows the XRD spectra of PAni thin films grown at different cathodic voltages between 1600 and 1700 mV. By referring to the XRD spectra of FTO substrate, it is possible to identify four peaks arising from PAni thin films. The two strongest peaks of PAni are observed at 2θ = 30.7° and 32.1°, which indicate the crystallinity of PAni [11, 12]. The intensity of these peaks increased as the V_g increased from 1600 to 1654 mV, which may be caused by the benzene rings settling down on top of another, creating a crystalline nature in PAni. The highest peak of this XRD intensity was obtained at V_g = 1654 mV. There are also two weak peaks appearing at 2θ = 44.0° and 44.9°, arising from PAni film, which could be due to the quinoid-ring introduced during the acid-treatment [13,14]. Therefore, in this work, V_g = 1654 mV has been chosen as the optimum potential for electrodeposition of PAni.

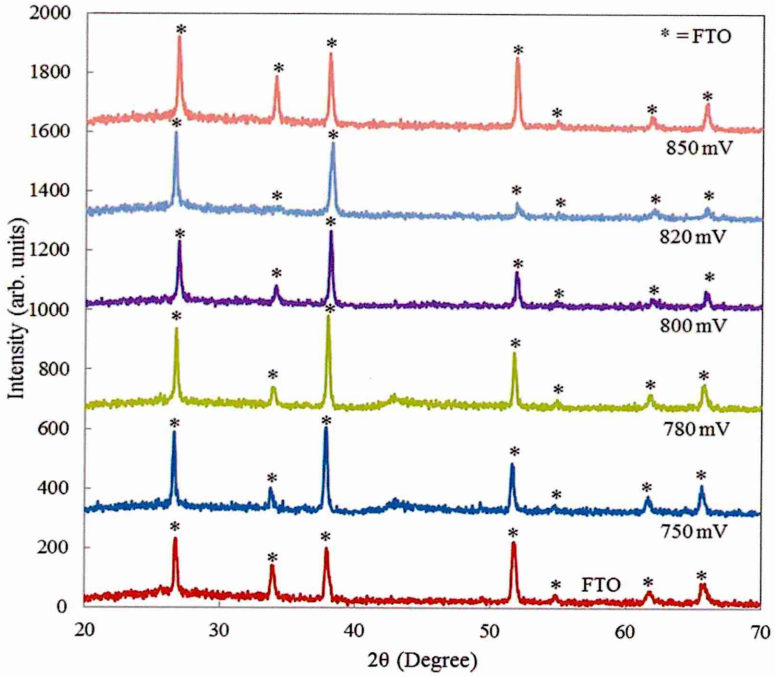


Figure 6.4: XRD spectra of PAni thin films grown on glass/FTO substrates at different anodic voltages from 750 to 850 mV.

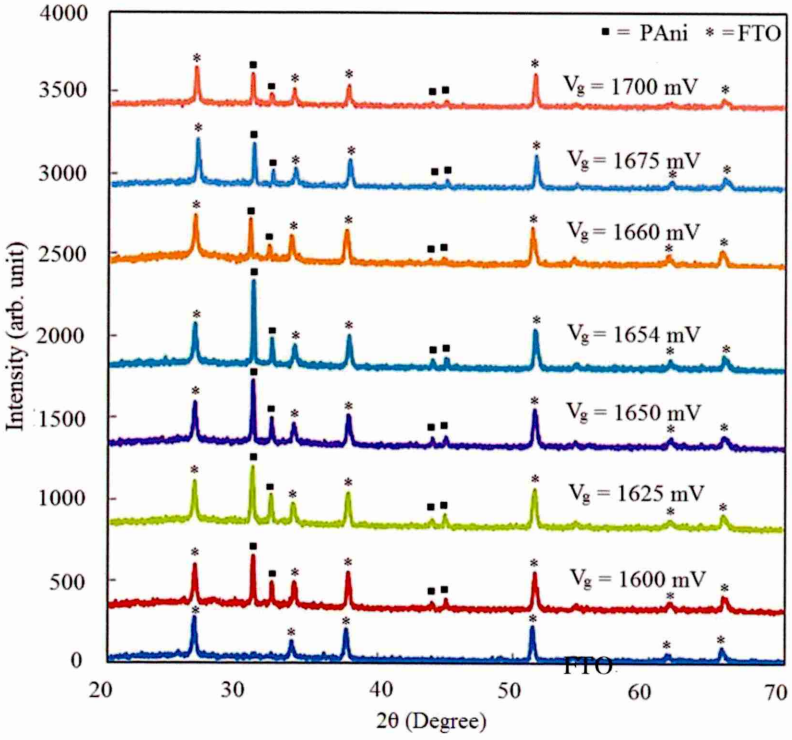


Figure 6.5: XRD patterns of polyaniline grown on glass/FTO substrates at different cathodic voltages from 1600 to 1700 mV. Note the best crystallisation taking place at 1654 mV.

6.1.3 Optical characterisations

The optical absorption measurements were carried out in order to estimate the energy bandgap of the PAni layers. Figure 6.6 and Figure 6.7 show the optical absorption spectra and the trend of energy bandgap of the as-deposited PAni layers grown from anodic and cathodic depositions at different growth voltages from 750-850 mV and 1600-1675 mV, respectively.

Figure 6.6 (a) shows the bandgap of the PAni layers grown from anodic in the range of 3.90-4.08 eV. The formation of the energy bandgap is associated with the π-π^* transition of the conjugated ring system in PAni film [15,16]. Although pernigraniline is an amorphous material, optical absorption is due to the transition of charge carriers through the forbidden gap [12]. The slight decrease in the bandgap was also observed at the high V_g. This trend could be due to the excitation transition of the polaron band and change in oxidation state, associated with transformation of colour on PAni thin films, as shown in Figure 6.8 (a). In Figure 6.6 (b) and 6.7 (b), it is observed that the PAni layers grown from cathodic deposition have bandgaps in a range from 1.05 to 1.20 eV. The slope of the absorption edge increased up to 1654 mV and slightly reduced with higher V_g. The highest in the slope of the absorption indicates the fewer defects in the materials. The bandgaps are reduced with the increment in the growth voltage. This trend could be due to the thicker layer forming at higher V_g since the deposition rate of PAni increased with the growth voltage.

The appearance of the PAni thin films grown from anodic and cathodic depositions is shown in Figure 6.8. PAni films grown from anodic deposition shows blue colour, which indicates the pernigraniline (fully oxidised state) of polyaniline [10,17], while those grown from cathodic show a dark pale yellow appearance, indicated as leucoemeraldine (fully reduced state) of polyaniline [17]. The appearance is concomitant with observations of other researchers.

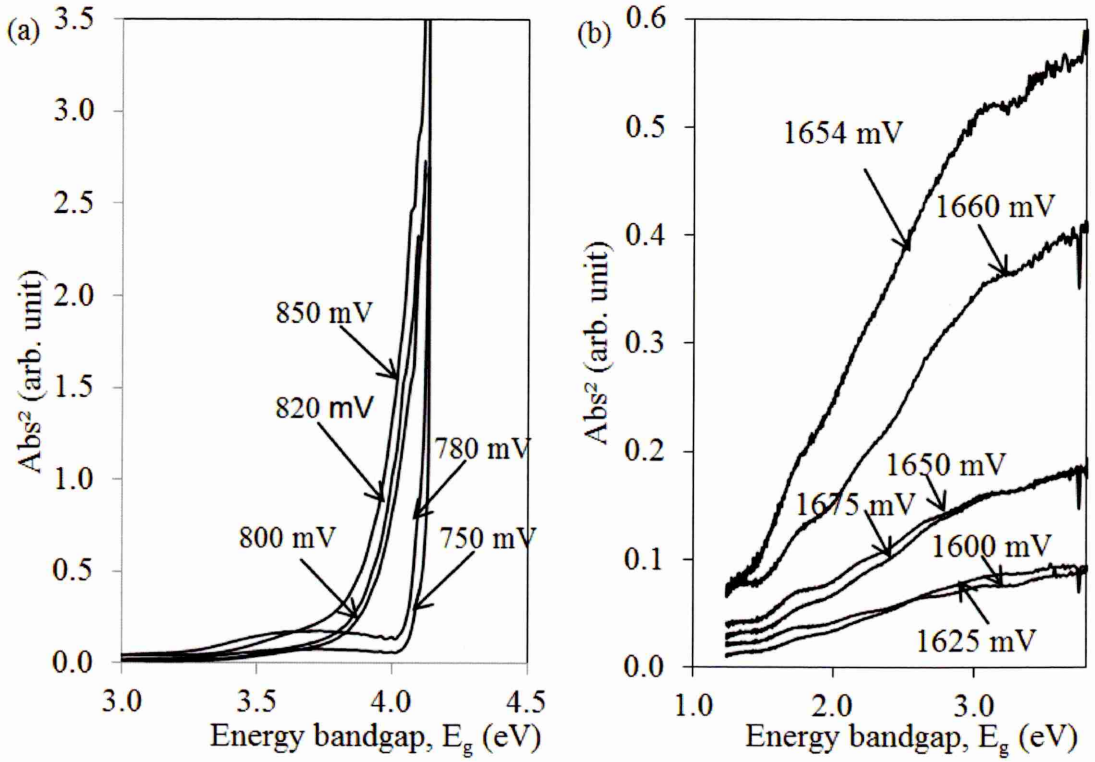


Figure 6.6: The optical absorption spectra of PAni thin films electrodeposited from (a) anodic deposition and (b) cathodic deposion at V_g of 750-850 mV and 1600-1675 mV, respectively.

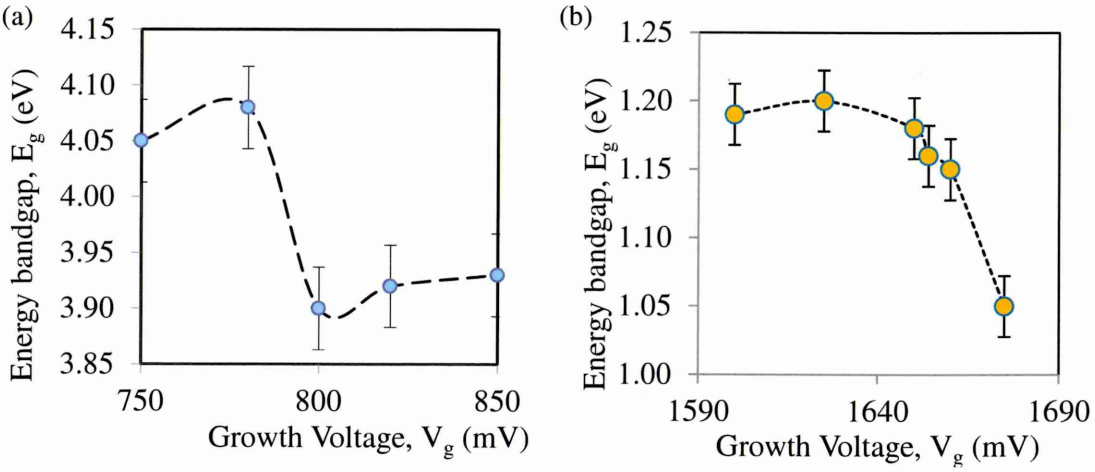


Figure 6.7: The trend of energy bandgap as function of the growth voltage of PAni thin films grown from (a) anodic and (b) cathodic depositions.

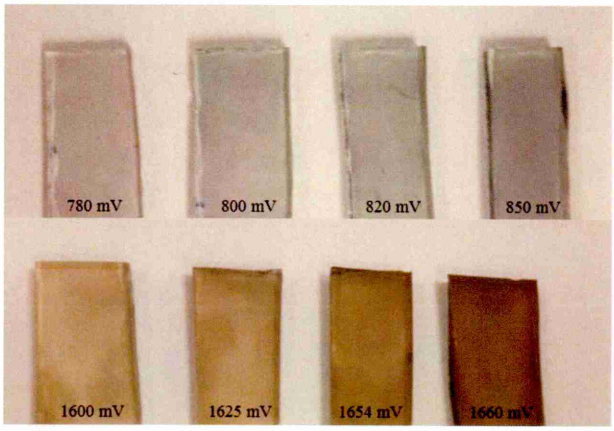


Figure 6.8: The physical appearance of PAni thin films grown from (a) anodic and (b) cathodic depositions.

6.1.4 Thickness measurement

The thicknesses of these layers were measured by two different methods, using an optical profilometer and the average measurement in SEM cross-section images. The purpose of this measurement is to estimate the deposition rate for PAni thin films grown from anodic and cathodic depositions. As for PAni layers grown using anodic deposition, five samples were deposited at different deposition times from 10, 15, 20, 40 and 60 minutes at V_g=780 mV, whereas from cathodic deposition, six samples were grown at different deposition times from 5, 10, 15, 20, 40 and 60 minutes at V_g=1654 mV.

Table 6.1 shows the data for thickness of PAni thin films obtained from the optical profilometer. The measurements were carried out three times, and the average value was calculated and presented. Although the thickness of both deposited forms of PAni films increased as the deposition time increased, the deposition rate was reduced with the longer deposition time. The higher deposition rate in the beginning of the electrodeposition is due to the high electric field between the electrolyte and conductive FTO surface. As the deposition time increased, the conductive surface was slowly covered with the growth material, which reduces the electric field and growth current density, J_g and therefore slows the deposition rate. PAni thin films electrodeposited using cathodic deposition show a higher deposition rate than those grown from anodic deposition. This means that cathodic deposition formed a thicker layer than the anodic deposition. This trend can be seen in Figure 6.9(a).

Table 6.1: The summary of the thickness value of PAni films grown from anodic and cathodic depositions are measured by an optical profilometer.

Deposition Time, t (minute)	Anodic deposition		Cathodic deposition	
	Average thickness, *t* ±50 (nm)	Deposition rate (nm minute^{-1})	Average thickness, *t* ±50 (nm)	Deposition rate (nm minute^{-1})
5	-	-	133	26.6
10	100	10.0	267	26.7
15	133	8.9	300	20.0
20	167	8.4	367	18.4
40	233	5.8	633	15.8
60	267	4.5	867	14.5
Average deposition rate		7.5		20.3

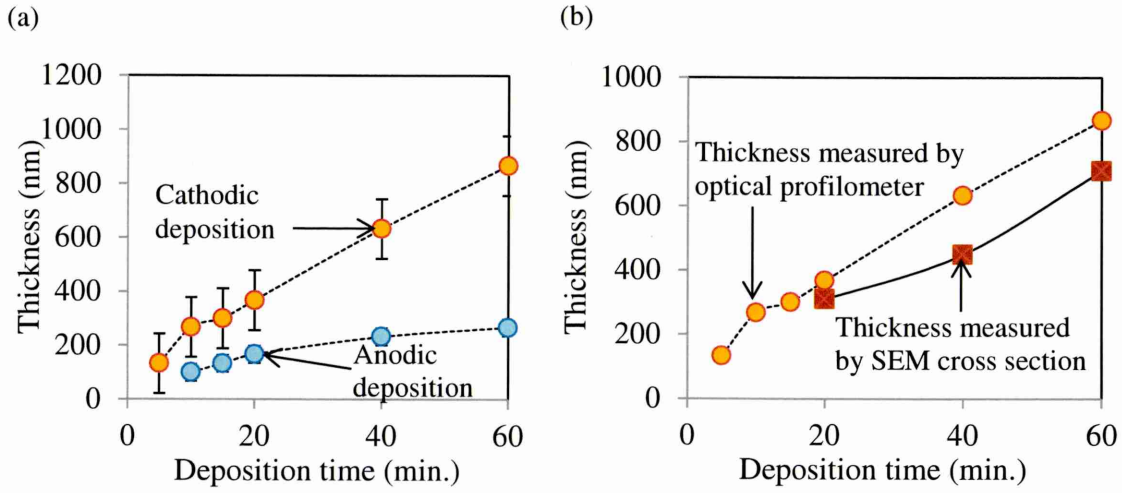


Figure 6.9: The schematic diagram of graphs comparing the thickness of PAni (a) grown from anodic and cathodic depositions and (b) measured by optical profilometry, and SEM cross section for PAni grown by cathodic deposition.

Figure 6.10 shows the SEM cross sections of PAni films deposited for 20, 40 and 60 minutes, using cathodic depositions and 40 minute using anodic deposition. As expected, the thickness increases with longer deposition. Also observed is a formation of separated grains on the top of the layer for PAni film grown from anodic deposition for 40 minutes. Although the average deposition rate estimated from the SEM is slightly lower than those derived from optical profilometer, nevertheless the trend is the same. The SEM cross-section measurements are consistent with the results from the optical profilometer. The summary of the thicknesses estimated from these cross sections is shown in Table 6.2. The comparison of thicknesses measured from the optical

profilometer and the SEM cross section for samples grown from cathodic deposition is shown in Figure 6.9 (b).

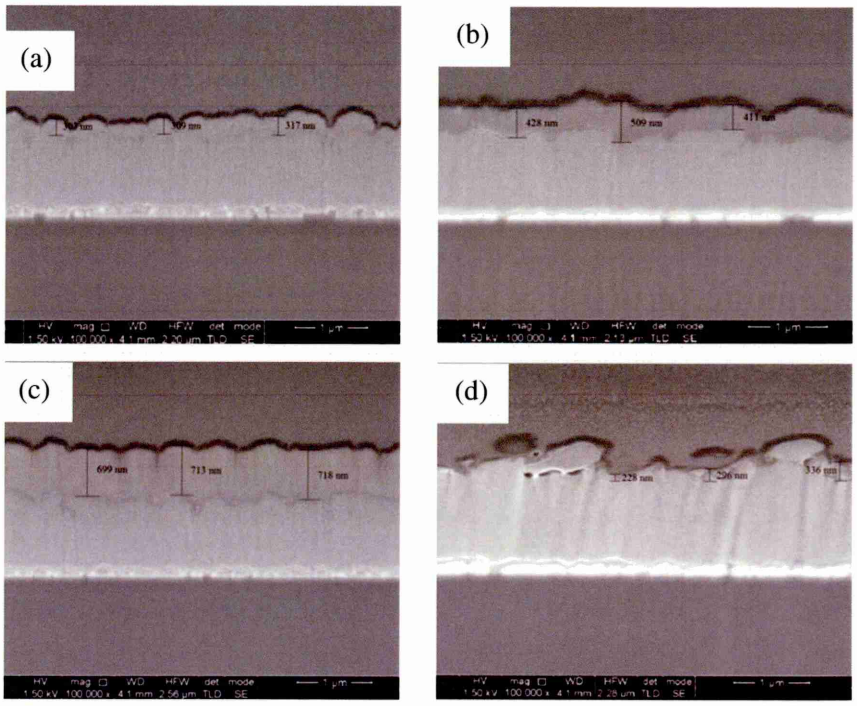


Figure 6.10: The SEM cross section of glass/FTO/PAni thin films grown from cathodic deposition for (a) 20, (b) 40, (c) 60 minutes and (d) glass/FTO/PAni thin films grown from anodic deposition for 40 minutes.

Table 6.2: The summary of the thickness estimated from the SEM cross section for PAni layers grown from cathodic deposition at 10, 20, 40 and 60 minutes.

Deposition time, t (min.)	Anodic deposition (Pernigraniline base PAni)		Cathodic deposition (Leucoemeraldine base PAni)	
	Average thickness, *t* ±5 (nm)	Deposition rate (nm min.$^{-1}$)	Average thickness, *t* ±5 (nm)	Deposition rate (nm min.$^{-1}$)
20	-	-	310	15.5
40	287	7.2	449	11.3
60	-	-	710	11.8
Average deposition rate		7.2		12.9

6.1.5 Morphological characterisation

Scanning electron microscopy was employed to study the surface morphology and grain size of PAni layers grown on FTO substrates. Figure 6.11 presents the SEM morphology of the (a) FTO substrate and PAni thin films grown from anodic deposition

for (b) 10, (c) 20, (d) 40 and (e) 60 minutes, as well as PAni layers grown from cathodic deposition for (f) 10, (g) 20, (h) 40 and (i) 60 minutes.

The morphology of PAni layers shows a strong dependence on the deposition method. As shown by the SEM in Figure 6.11 (b) and (c), PAni grown from anodic deposition seem to grow with the cementing effect at the first 20 minutes of the deposition. However, the formation of larger separated grains starts to appear at further deposition time. Hong-zhi and Guo also observed the cementing effect on their first 20 minutes' deposition of PAni layers from anodic deposition and explained it as a "gel effect" [18,19]. At the beginning of the deposition, PAni and other molecular complexes that consist of a few monomer that are called oligomers are deposited simultaneously on the FTO surface. Some of the oligomers were further oxidised and the others interacted with dopant and aniline monomer to form the gel coating the smaller grains. This decreased the amount of nucleation sites to favour the one dimensional growth [20]. As the deposition time increased, the whole base was covered by polyaniline. It was more inclined to polymerise on the membrane surface. These promoted the formation of larger and isolated grains on the top of the matrix after $\geq$40 minutes deposition.

SEM images of PAni layers grown from cathodic deposition show a random distribution of smaller grains in the range 50-90 nm covering the top and the grain boundaries of the FTO surface at the beginning of the deposition. PAni film grown from cathodic deposition formed thicker layers after being deposited for $\geq$40 minutes. It is also clearly seen that the grain size is not affected by the deposition time.

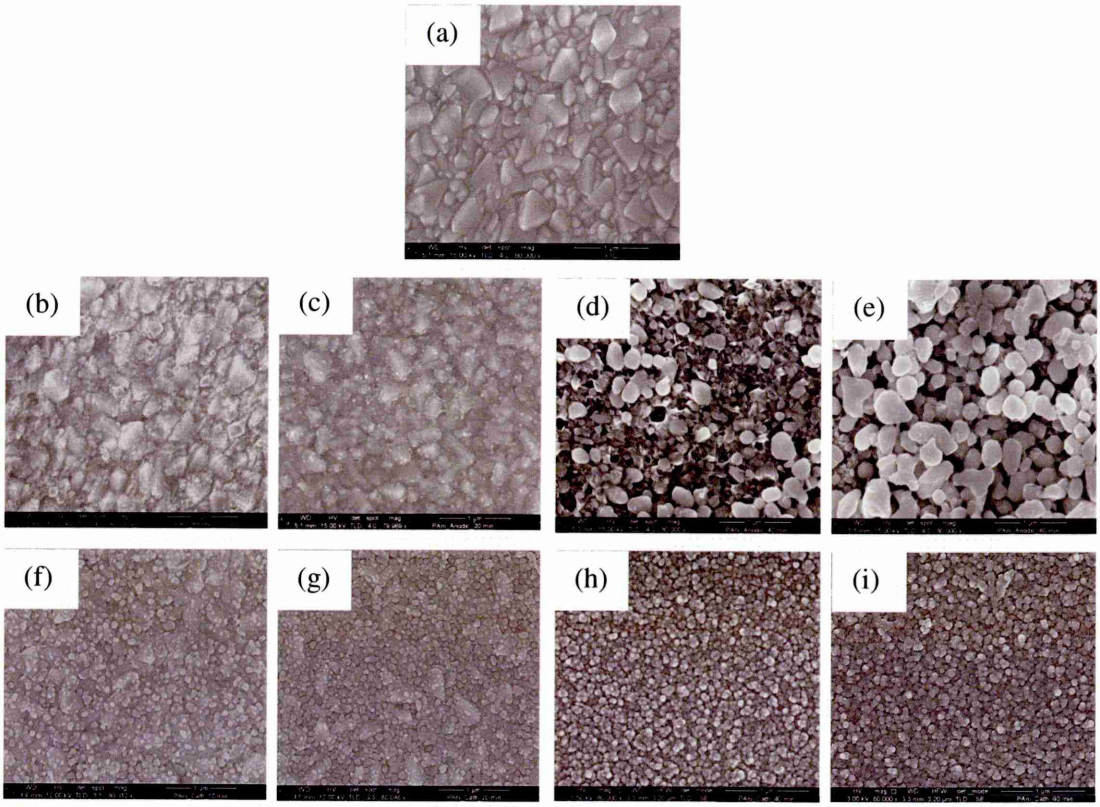


Figure 6.11: The SEM surface morphology images of (a) FTO substrate and PAni layers grown from anodic deposition for (b) 10, (c) 20, (d) 40 and (e) 60 minutes as well as grown from cathodic deposition for (f) 10, (g) 20, (h) 40 and (i) 60 minutes.

6.1.6 Conclusion

The electrodeposition of PAni thin films has been successfully established. PAni thin films formed well on glass/FTO substrates using anodic and cathodic deposition. PAni thin films grown from anodic deposition show blue-violet colour, which denotes as pernigraniline (fully oxidised state) of PAni. XRD spectra do not show any clear crystalline peak, and it is suggested that PAni thin films grown from anodic deposition are amorphous. The bandgap of these layers is in the range of 3.90 to 4.08 eV. SEM images show the cementing effect at the beginning of deposition. However, the larger isolated grains are formed on the surface at longer deposition time.

On the other hand, PAni thin films grown using cathodic deposition show pale yellow colour, which indicates as leucoemeraldine (fully reduced state) of PAni. PAni thin films grown from cathodic deposition show the best crystallinity at V_g of 1654 mV, with the band gap range in between of 1.05 to 1.20 eV. The measurements from optical profilometry and SEM cross section demonstrate that PAni layers deposited using cathode deposition are much thicker than those grown from anodic deposition. They

also show random distribution of smaller grains in the beginning of the deposition and these grains have fully covered the FTO surface after being deposited ≥40 minutes.

From this work, it is suggested that a thin layer of PAni grown from anodic deposition is suitable to be used as a buffer or window layer in solar cell fabrication. This is because it has a wide bandgap. The cementing effect in the first 20 minutes of deposition while PAni is grown using cathodic deposition is suitable for plugging the pin hole layer, since it has a narrow bandgap and smaller grain size. The effect of the PAni films in solar cell devices will be discussed further in section 7.2.

6.2 Study the effect of annealing and pH on PAni thin films

The first part of this section presents the study on the effect of annealing temperature on PAni thin films grown from anodic and cathodic deposition. The annealing temperature has been varied from 150, 250, 350 and 450°C. The purpose of this work is to optimise the suitable annealing temperature of PAni grown from anodic and cathodic deposition. All the samples in this work were characterised for their structural, optical, thickness, electrical and morphological properties using XRD, UV-Vis spectroscopy, DC conductivity measurements, optical profilometry and SEM. The second part of this work is to study the effect of pH in the aqueous solution on PAni thin films on the bandgap and electrical conductivity of PAni thin films. This work has been done only for samples grown from cathodic deposition, because PAni layers grown from anodic deposition usually form a very thin layer, which is not suitable for DC measurements. The pH in the aqueous solution has been varied from 1.00 to 6.50 ± 0.02. The V_g and deposition time are maintained at 1654 mV and 60 minutes, respectively. These samples were then characterised using UV-Vis spectroscopy and DC conductivity measurements for their optical and electrical properties.

6.2.1 Structural characterisation

Figure 6.12 shows the effect of annealing temperature on the crystalline structure of PAni thin films grown from (a) anodic deposition and (b) cathodic deposition. Four different annealing temperatures varied from 150 to 450°C for ~10 minutes. From Figure 6.12(a), it is observed that the as-deposited PAni layer from anodic deposition shows a small hump at $2\theta=42.8^{\circ}$. But this hump disappeared after annealing. These films do not show any new crystalline peaks appearance even after being annealed up to

450°C. This work again confirms that the pernigraniline base of PAni grown from anodic deposition is an amorphous layer.

Figure 6.12(b), shows the XRD spectra of PAni thin films grown from cathodic deposition. It is observed that the intensity of prominent peaks at $2\theta=30.7^{o}$ and 32.1^{o} reduced with annealing temperature. The decrease in the crystallinity with annealing temperature could be due to the heat effect or loss of materials [12]. The sample annealed at 350°C, indicate the appearance of a new peak of PAni related at $2\theta = 30.1^{o}$. This might be due to the improvement of re-orientation of benzene rings removing any strain created during deposition. Further annealing causes the deterioration of crystallinity, reducing XRD peak intensity, which might be due to the change in molecular structure arising from the chain breaking and cross-linking reaction [8,13,14,21]. Heat treatment of an aromatic hydrocarbon at a temperature of 350°C in atmospheric conditions could easily break the bonding in this material, forming H_2O and CO_2, and reducing the crystalline nature of the PAni layer [14].

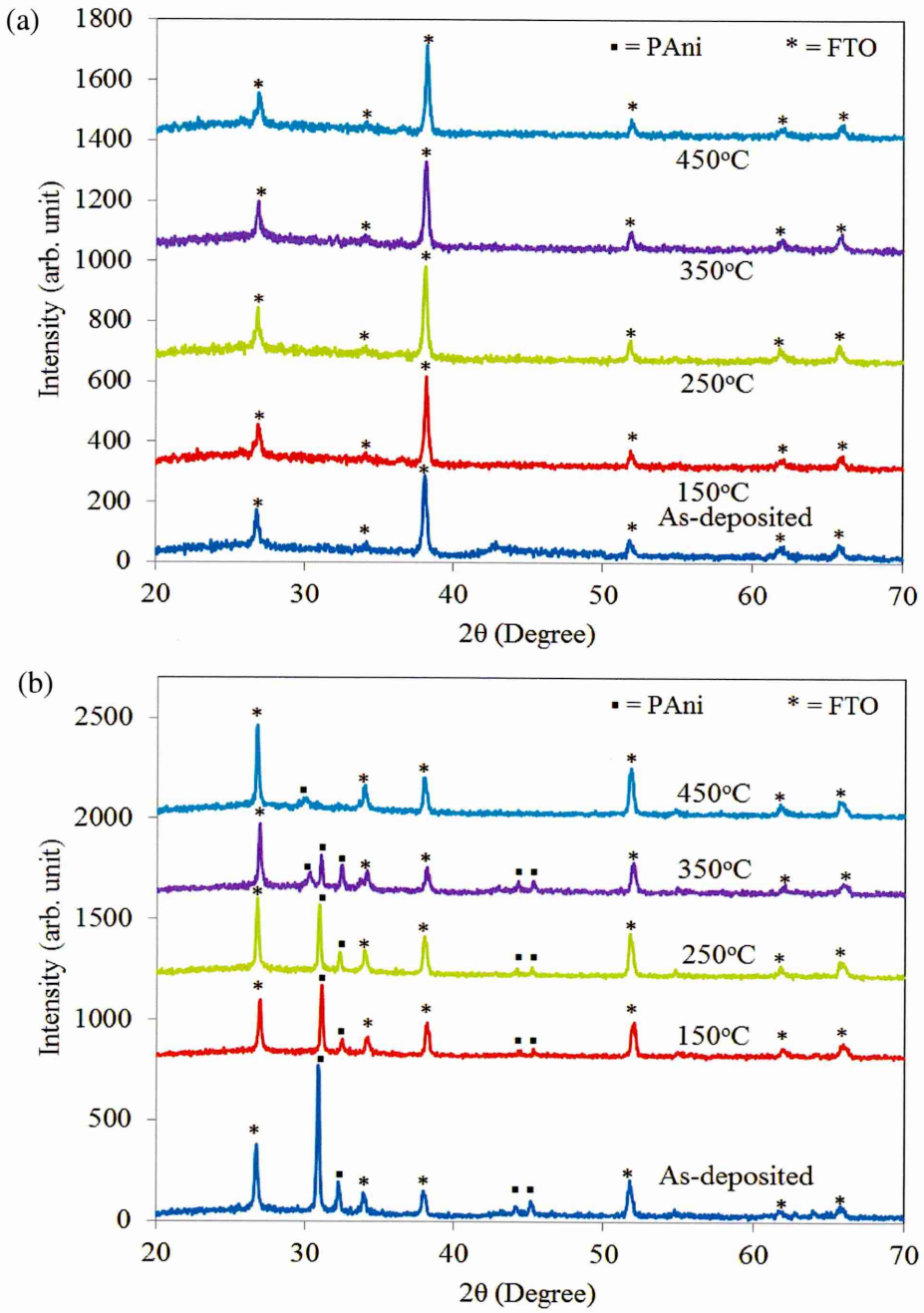


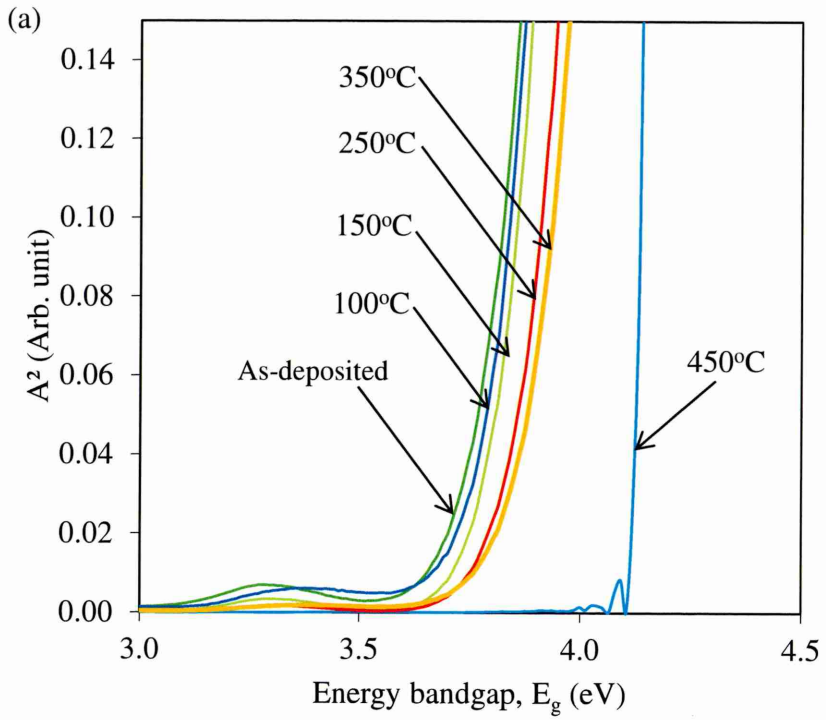
Figure 6.12: The XRD spectra of PAni thin films electrodeposited from (a) anodic and (b) cathodic deposition for as-deposited and annealed at temperatures from 150 to 450 °C, in air.

6.2.2 Optical characterisation

Figure 6.13 shows the absorption spectra of PAni thin films grown from anodic and cathodic depositions annealed at different temperatures from 100 to 450°C. The summary of these graphs is presented in Figure 6.14 and the physical appearances of the

films are shown in Figure 6.15. As shown in Figure 6.13(a) and 6.14, the bandgap of PAni thin films grown from anodic increased from ~3.65 to ~4.11 eV after being annealed from 150 to 450°C. The samples annealed at 450°C show an almost transparent light blue layer, due to the sublimation of the material. This indicates that PAni grown from anodic deposition is not suitable to be annealed at high temperatures, due to the molecular deterioration as a result of overheating. In fact, the breakage of the chemical bonds, cross linking, quinoid to benzenoid ring conversion and vice versa along with the doping and dedoping process is sensitive to high annealing temperature [12].

Likewise, the bandgap of PAni thin films grown from cathodic deposition also increased from ~1.28 to ~2.20 eV with corresponding colour changes when annealed at high temperature. Kang et. al [14] described the behaviour of increment in energy bandgap upon annealing as arising from the escape of hydrogen atom/molecules, which are absorbed and bonded loosely to the PAni layers. At the cathodic voltage of 1654 mV, water splitting takes place in an aqueous solution, and therefore hydrogen molecules have evolved at the cathode while the polymerisation of aniline has taken place. Therefore, loosely bound hydrogen atoms could be formed in as-deposited PAni layers. The percentage of unbound hydrogen, water and unbound H_2SO_4 loss with respect to PANI film decreases as the annealing temperature is increased.



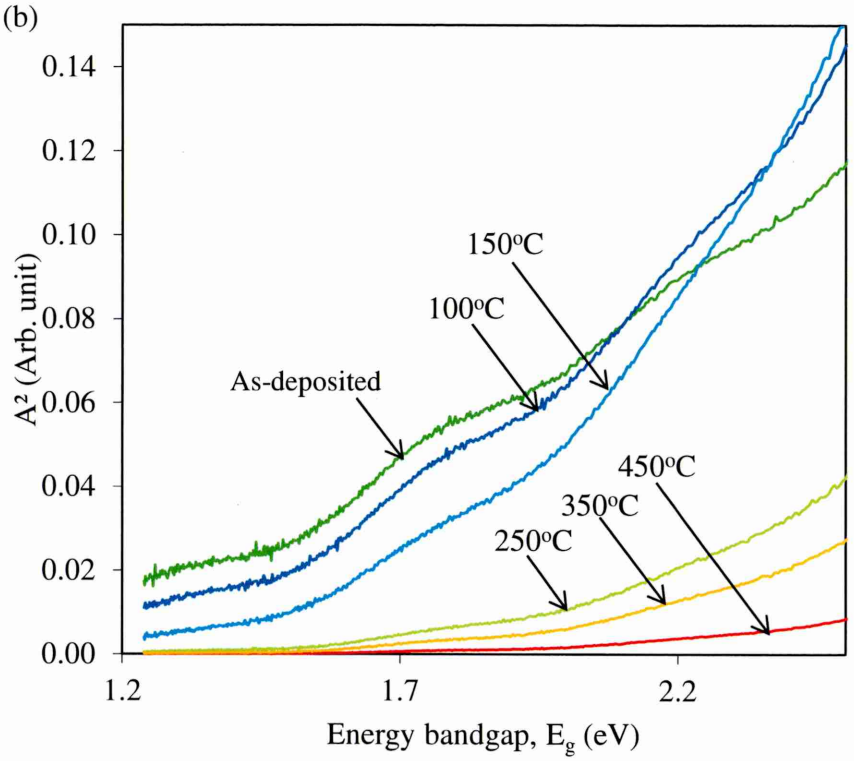


Figure 6.13: The optical absorbtion spectra of PAni electrodeposited from (a) anodic and (b) cathodic deposition for as-deposited and annealed at 100, 150, 250, 350 and 450°C.

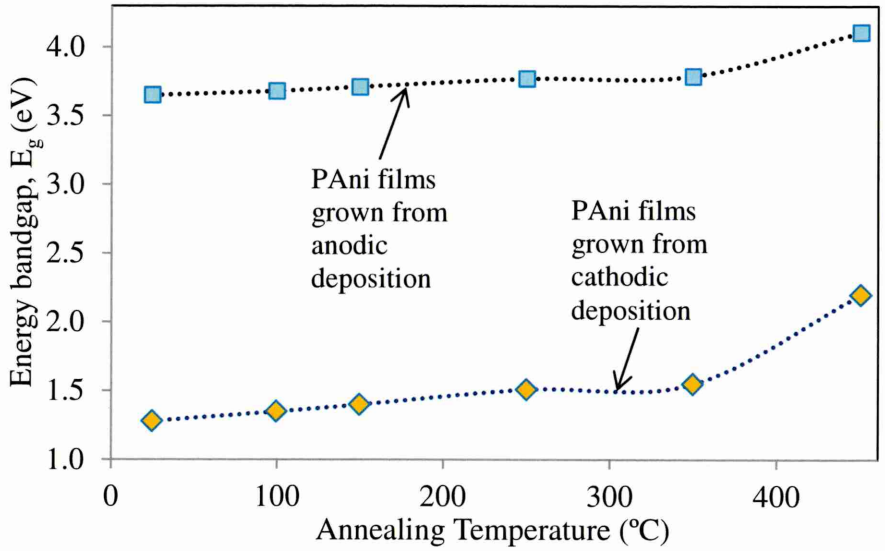


Figure 6.14: A typical variation of energy bandgap of PAni layers, as a function of annealing temperature. Duration of annealing at 300°C was kept constant at five minutes.

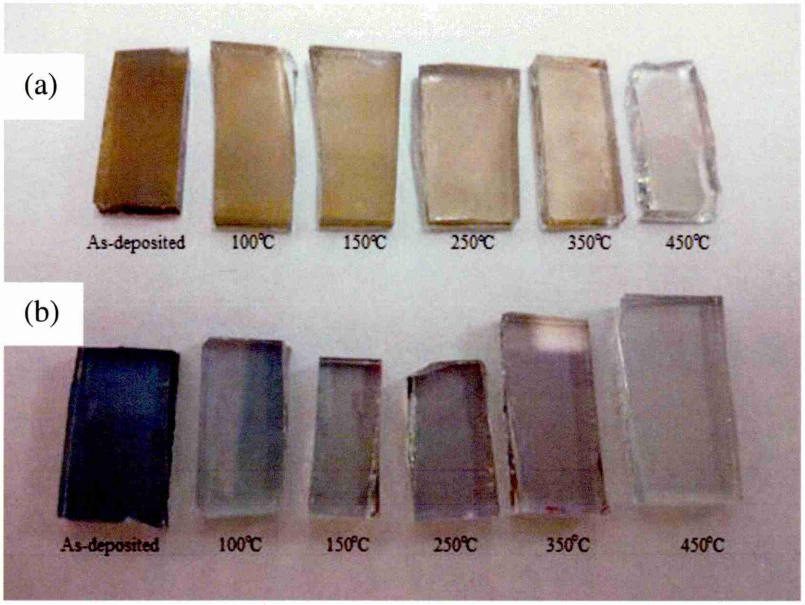


Figure 6.15: The colour appearance of PAni thin films grown from (a) cathodic and (b) anodic depositions with different annealing temperatures from 100 to 450°C.

6.2.3 Electrical characterisation

In order to estimate the electrical conductivity of electrodeposited PAni layers, glass/FTO/PAni/Au structures were fabricated with thick (~950 nm) PAni layers. Two mm diameter and circular ohmic contacts were made by evaporating Au on the top of PAni layers. I-V measurements were carried out at several point contacts to observe their ohmic behaviour. The resistances of PAni layers were measured and the electrical conductivity was calculated, using equations 3.12 and 3.13 as stated in Chapter 3.

The summary of the DC conductivity measurements with different annealing temperatures is shown in Table 6.3. The DC conductivity does not show any relevant result for samples with thickness lower than 200 nm. Therefore, this work has only presented the electrical conductivity of PAni films with thickness > 200 nm. It is shown that conductivity of PAni grown from both depositions is reduced after being annealed. PAni layers grown from anodic deposition seem to have higher conductivity than those grown from cathodic deposition. This could be associated with the stability of the pernigraniline base and the degree of protonation and chain structure of the pernigraniline PAni films deposited from doped electrolyte, or they might experience some reduction and rest between the pernigraniline-emeraldine based transitions [8]. Also observed in Table 6.3, the thickness decreases rapidly at the temperature >250°C. Lodha et. al also observed a loss of material and degradation of PAni films at a

temperature of 300°C [22]. PAni layers electrodeposited from cathodic deposition show very low conductivities due to the nature of the leucoemeraldine base. In the same way as the film is grown from anodic deposition, the conductivities also reduce with the annealing process. The annealing of PAni at different temperatures causes extrinsic structural changes such as the removal of dopant, and intrinsic changes like oxidation, chain scission or cross linking, and other chemical reactions and all these thermo-chemical changes do affect its conductivity [1,22]. In this case, both states of PAni thin films become more resistant after the annealing process.

Table 6.3: The summary of thickness and electrical conductivity measurements of PAni grown from anodic and cathodic deposition for as-deposited and after annealed at 100 to 450°C.

Samples	Annealing Temperature	Average Thickness (nm)	Average Resistance (Ω)	Conductivity x 10^{-5} $(\Omega\ cm)^{-1}$
PAni films grown from anodic deposition	As-deposited	316	0.58	164.7
	100	233	0.82	90.5
	150	203	-	-
	250	133	-	-
	350	116	-	-
	450	the layer did not survive		
PAni films grown from cathodic deposition	As-deposited	800	31.70	7.8
	100	433	43.61	2.2
	150	300	120.10	1.1
	250	216	-	-
	350	133	-	-
	450	the layer did not survive		

Further investigations on the effect of pH in the aqueous solution on electrical and optical properties of PAni thin films have been explored and presented in this section. Nine samples with size 2×2 cm^2 were electrodeposited at various pH values of 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5 and 6.5. The pH was monitored and the deposition was done for 90 minutes to grow the thicker layers. These samples were characterised by DC conductivity measurement and UV-Vis spectrometer for their electrical conductivities and bandgap properties.

Table 6.4 summarises the measurements of average resistance, electrical conductivity and bandgap of PAni layers as a function of the pH values. Figure 6.16

graphically shows the calculated electrical conductivity as a function of pH values. It is observed that the electrical conductivity reduced from (26.81 to 2.56) x 10^{-6} $(\Omega cm)^{-1}$ as the pH values increased from 2.00 to 6.50 during the deposition. The fact that the electrical conductivity of the PAni layers is higher for samples grown under more acidic conditions has been observed by many researchers [22, 23]. At low pH, H^+ concentration increases, and therefore, there are more protonated states in electrolytes. As the pH increases, the electrolyte has low H^+ concentration, so there is less protonate state at high pH. Protonation is the addition of proton (H^+) to the molecule to form a conjugate base. The protonation is also accompanied by drastic changes in the electrical structure of the polyaniline [23, 24]. Initial protonation at low pH leads to the formation of radical cations, which act as charge carriers. The protonation of aniline reduces with the increase of the pH [9,11]. As a consequence, the free charge carriers are getting lower at the higher pH, thus reducing the electrical conductivity of PAni films [13]. However, the value of electrical conductivity of PAni thin films in this work is considered lower than that of the CdS layer and CdTe layer in the previous study. This is due to the nature of the formation of the PAni in the leucoemeraldine base, which is highly resistive. However, the presence of a very thin layer of a highly resistive layer as a plugging pinhole is somehow helpful in the solar cell structure to form the MIS structure, which can increase the potential barrier, hence improving the V_{oc} in the solar device performance [21].

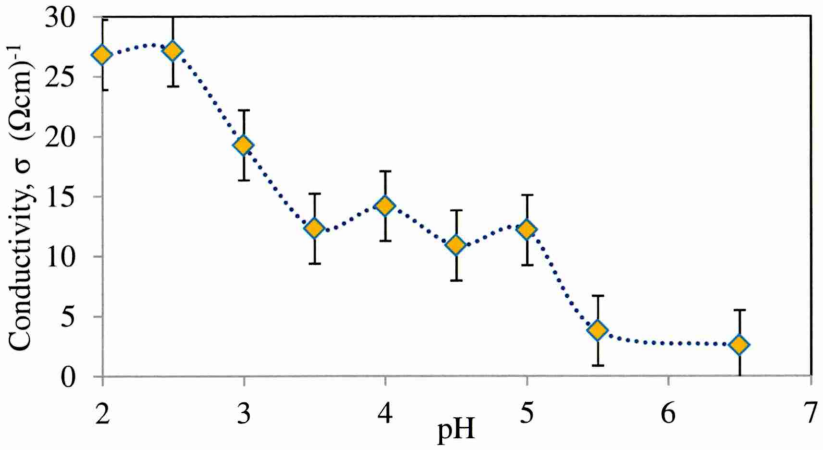


Figure 6.16: Electrical conductivity of PAni layers grown as a function of pH value of the electrolyte.

Table 6.4: The summary of electrical and optical properties of PAni thin films grown at different pH.

pH concentration	Average resistance (Ω)	Conductivity x 10^{-6} $(\Omega\ cm)^{-1}$	Energy bandgap (eV)
2.0	20.2	26.81	0.98
2.5	12.9	27.12	1.30
3.0	14.9	19.25	1.56
3.5	12.9	12.30	1.77
4.0	13.5	14.16	1.80
4.5	14.6	10.89	1.83
5.0	15.7	12.17	1.90
5.5	16.8	3.78	1.95
6.5	24.9	2.56	2.32

6.2.4 Morphological characterisation

Figure 6.17 shows the SEM images of PAni grown from cathodic deposition at pH of 2.0, 3.5 and 5.0. It is observed that the grain of PAni formed uniformly and homogeneously in all samples. The change in pH in electrolytes seems not to affect the formation of the grains' shape. However, the grain size seems to reduce slightly with the increasing of the pH. The grain size of PAni at pH=2.00 is in a range of ~80-120 nm, while those grown at pH 3.5 and 5.0 have grain sizes in the range of 60-70 nm and ~40 nm, respectively. The slight reduction in grain size could be due to the lack of H^+ to initiate the reaction [25]. At high pH, polymerisation of aniline results in shorter PAni polymer chains that stick more tightly while producing a smaller grain size [26]. When the pH reduced to 2.00, polymerisation of aniline resulted in PAni polymers that were loosely attached due to the small number of those negatively charged, and results in larger grains of PAni. The PAni film in these particles has longer chains and higher conductivity, as presented in the results of electrical conductivities. This work gives an idea that the grain size of PAni grown from cathodic deposition can be controlled by the acidity of precursor solutions.

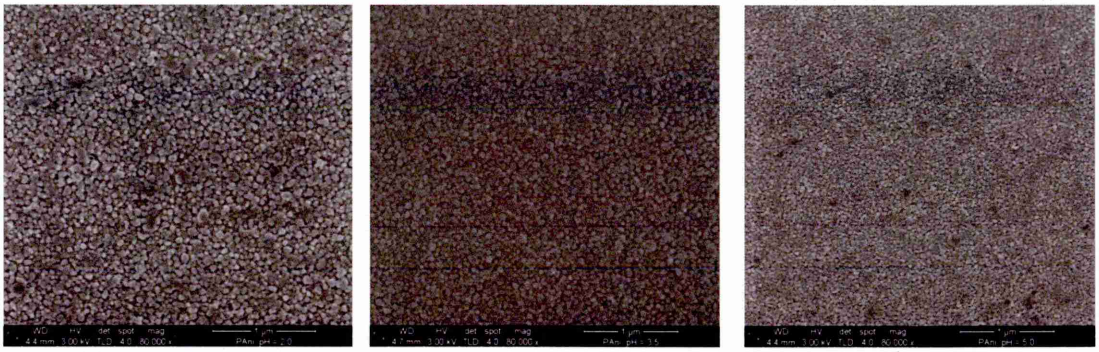


Figure 6.17: The SEM images of PAni thin films grown from cathodic depositions at different pH values of 2.0, 3.5 and 5.0.

6.2.5 Conclusion

The effect of annealing temperature on the crystal structure, bandgap and electrical conductivity has been studied for PAni thin films grown from anodic and cathodic depositions. The XRD results of PAni grown from anodic do not show any appearance of XRD peaks for even after the annealing process. PAni grown from cathodic deposition, however, showed crystalline nature for as-deposited layers and the deterioration of the prominent peak, together with the appearance of another new related peak of PAni after being treated at 350°C. Optical and electrical measurements demonstrate an increase in bandgap and reduction in conductivity for both PAni layers, due to the sublimation and degradation of the materials. Therefore, from this work, it can be suggested that the annealing process is not so helpful in enhancing the properties of PAni thin films. The effect of pH in aqueous solution demonstrated a reduction in conductivity, increment in energy bandgap and lessening in grain size with higher pH values. Therefore, with the knowledge acquired by this work, it is suggested that an ultra-thin layer of PAni layer grown from cathodic deposition at pH~5.00 is suitable to be used as a pinhole plugging layer, due to its high resistivity to forming a MIS structure in back contact, and its smaller grain size to fill the possible pinholes in the absorber layer, in order to improve solar cell parameteres.

6.3 Overall Conclusions

The electrochemical synthesis of PAni thin films in acidic and aqueous solution has been successfully established. PAni thin films can be grown from anodic and cathodic deposition. PAni layers grown from anodic deposition in this work have been identified as pernigraniline base, while the layers grown from cathodic are suggested as

leucoemeraldine base on the films appearance and the nature of oxidation and reduction layers obtained through anodic and cathodic depositions, respectively. The PAni layers polymerise well on glass/FTO substrates at anodic growth voltages ~800 mV. The optimum V_g of anodic cannot be estimated, due to the amorphous nature of these layers in as-deposited and even after annealing. However, pernigraniline base PAni layers grown from anodic deposition have large bandgaps and cementing growth effect and are suitable to be used as buffer layers in solar cell devices. The best V_g for PAni grown from cathodic deposition is 1654 mV, based on the highest crystallinity peak obtained from XRD and the maximum band edge slope in optical absorption. The annealing process does not demonstrate any improvement in the crystallinity of PAni grown from anodic. In fact, a high annealing temperature deteriorates the crystallinity and conductivity of PAni grown from cathodic depositions. A PANI layer grown from cathodic deposition at pH of ~5.00 is suggested to be applied in pinhole plugging layers, due to the nature of the smaller grain size and the higher resistivity of this layer to fill the gaps and create the MIS type electrical contacts. The study of the use of PAni as a buffer and a pinhole plugging layer in n-CdS/n-CdTe solar cells will be discussed further in the next chapter.

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Chapter 7 - Characterisation of solar cells

7.0 Introduction

This chapter presents the characterisation of solar cell devices fabricated using the three materials characterised in the previous chapters (Chapter 4–6). In general, the solar cell devices in this research are based on CdTe. A CdS window layer has been the best partner for CdTe in forming a heterojunction structure, thus making the main structure of the solar cell a CdS/CdTe structure. The first section of this chapter presents the effect of various conditions of CdS and CdTe thin films on CdS/CdTe solar cells. The effect of using n-type and p-type CdTe in CdS/CdTe solar cells is also discussed here. A test using a PAni thin film in a CdS/CdTe solar cell was done to study the effect of this layer on device performance. Other device structures incorporating zinc sulphide (ZnS), cadmium selenide (CdSe) and zinc telluride (ZnTe) were also studied in this chapter. In the final section of this chapter, an experiment on the etching process and analysis of device lifetime are presented briefly. The summary of this chapter is illustrated in the flowchart below:

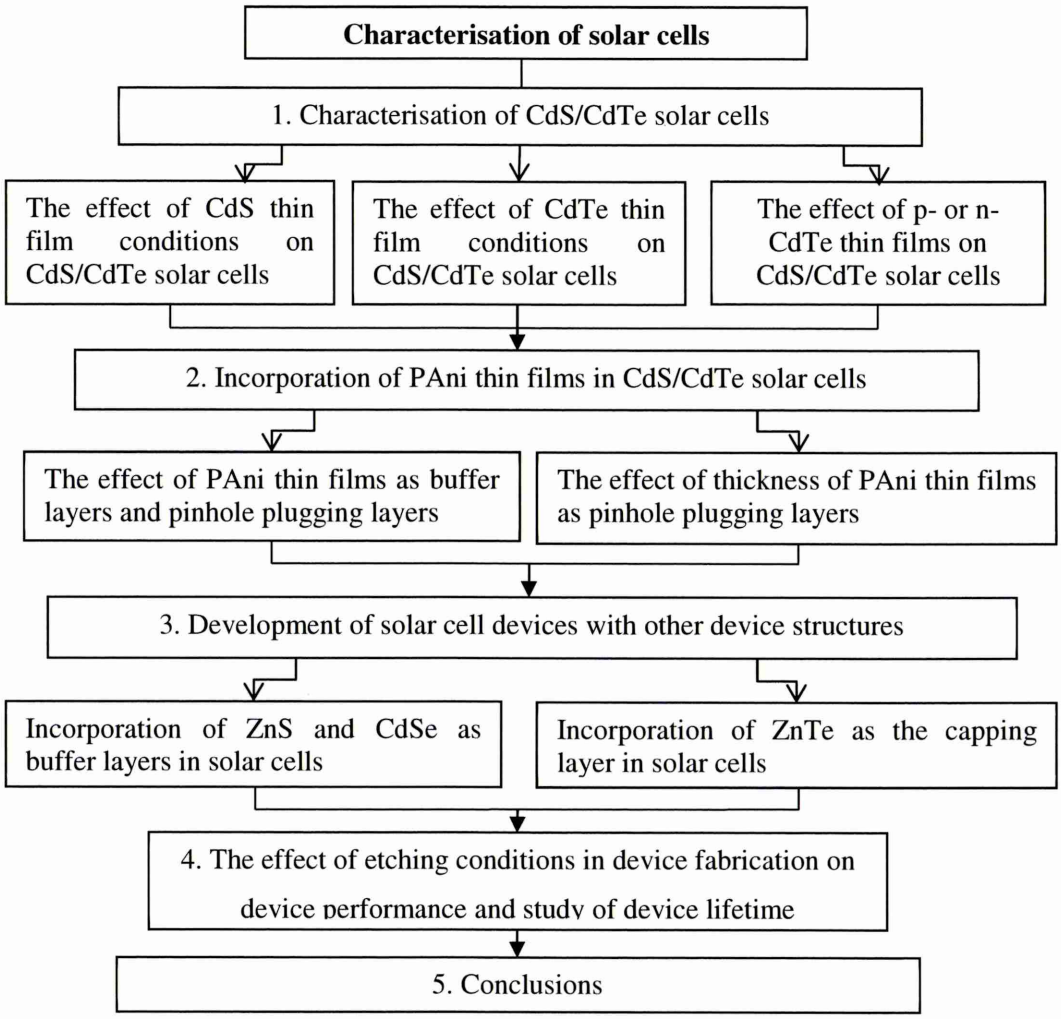


Figure 7.1: Summary of characterisation of solar cells reported in this chapter.

7.1 Characterisation of CdS/CdTe solar cells

In this section, solar cell devices were fabricated with the structure of glass/FTO/CdS/CdTe/Au. In the first part of this section, CdS layers were prepared with a variety of annealing temperatures and chemical treatments to study the effect of these annealing temperatures and chemical treatment on solar cell device performance. The second part of this section presents the development of CdS/CdTe solar cells using CdTe layers with different annealing temperatures and chemical treatments. The effect of $CdCl_2$ treatment on defect and Fermi-level movement is also discussed in the second section. Both p- and n-type CdTe was used to study the effect of conductivity type of CdTe film on solar cell performance.

7.1.1 The effect of CdS thin film conditions on CdS/CdTe solar cells

Many devices have been fabricated with a variety of CdS thin film conditions, but in this particular work, seven sets of CdS/CdTe solar cells were fabricated using various CdS layers. Initially, the glass/FTO was cut into 7.0×1.5 cm^2 and put through a standard cleaning process. The CdS layers were grown at V_g=1455 mV for about 30 minutes to obtain the thickness of 300–400 nm. Then the glass/FTO/CdS sample was cut into seven to produce seven samples of glass/FTO/CdS. One of them was set aside as a reference sample (as-deposited) while the other six samples underwent different annealing temperatures, with and without chemical treatments as described in Table 7.1. All these samples were then coated with CdTe layers with the same growth condition, thickness, annealing and treatment. All these devices were then put through an etching and metallising process. The same processing conditions were maintained for all the devices for comparison.

Table 7.1: The details of CdS thin films on CdS/CdTe solar cells.

Annealing temperature, T (°C)	CdS Conditions			
	As-deposited	Annealing without any chemical treatment	Annealing with $CdCl_2$ treatment	Annealing with $CdCl_2$+CdF_2 treatment
As-deposited	CS_AD	-	-	-
400°C	-	CS_HT_400	CS_CC_400	CS_CF_400
450°C	-	CS_HT_450	CS_CC_450	CS_CF_450

The solar cells' measurements under AM 1.5 illumination are presented in Table 7.2, and the trend observed is presented in the bar charts in Figure 7.2. From these measurements, it is found that the open circuit voltage, V_{oc}, of the solar cells is greater if the CdS layers were annealed either with or without any chemical treatments. The devices using CdS layers that were annealed at 450°C, however, demonstrated lower V_{oc} than those using CdS film annealed at 400°C. The short circuit current density, J_{sc}, of devices is improved slightly when CdS layers were annealed with or without chemical treatment, since the annealing process tends to improve the crystallisation, grain size and optical transmittance [1, 2]. The highest J_{sc} is observed for devices treated with CdS treated with $CdCl_2$+CdF_2, since the presence of fluorine performed an exclusive treatment to encourage recrystallisation and to produce solid grains for better electron mobility. The fill factor, *FF*, for this particular set of devices is generally low with a range of 0.25 to 0.46. However, the *FF* is improved for the CdS layers treated with

either $CdCl_2$ at 400°C or $CdCl_2$+CdF_2 at both 400°C and 450°C. This may be due to the elimination of the small grains and grain boundaries in the window layer.

Figure 7.2 (d) shows that the efficiency, η, of solar cell devices increases gradually from AD, HT, CC and CF. Overall, the best η of the solar cell devices is obtained with device CS_CF_400 with 5.8%. The devices with annealed CdS layers are clearly better than those with as-deposited CdS layers, since they have better crystallinity, are more stoichiometric, and have good transmission and a larger grain size. Although both annealing temperatures and chemical treatments are important for CdS layers, from this set of experiments it is observed that the device performances are affected by the annealing temperatures more strongly than by the chemical treatments. However, annealing at 450°C seems too high and it is believed that it deteriorates the layer, subsequently reducing the solar cell performance due to the presence of voids, cracks, sublimation or reduction of the CdS thickness at higher annealing temperatures, as discussed in section 4.2.

Table 7.2: The measurements of solar cell device performance with a variety of conditions of CdS thin films. Note that the asterisk denotes the highest-efficiency cell.

Sample ID	Measurement					Average			
	No.	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
CS_AD	1*	222	16.9	0.26	1.0	151	13.2	0.25	0.5
	2	95	12.5	0.25	0.3				
	3	135	10.2	0.24	0.3				
CS_HT_400	1	602	17.1	0.38	3.9	586	17.8	0.38	4.0
	2*	604	18.5	0.38	4.3				
	3	552	17.9	0.38	3.8				
CS_HT_450	1*	374	17.7	0.29	1.9	367	17.1	0.29	1.8
	2	361	17.0	0.30	1.8				
	3	366	16.5	0.29	1.8				
CS_CC_400	1	592	18.2	0.46	5.0	593	18.0	0.46	5.0
	2*	607	18.4	0.48	5.4				
	3	581	17.5	0.45	4.6				
CS_CC_450	1*	400	19.2	0.30	2.3	399	19.1	0.29	2.2
	2	398	18.9	0.28	2.1				
	3	400	19.1	0.29	2.2				
CS_CF_400	1	611	20.7	0.47	6.0	609	20.4	0.46	5.8
	2*	614	20.7	0.47	6.0				
	3	603	19.9	0.45	5.4				
CS_CF_	1*	554	18.9	0.45	4.7	532	18.3	0.44	4.3

450	2	537	17.3	0.44	4.1				
	3	504	18.6	0.44	4.1				

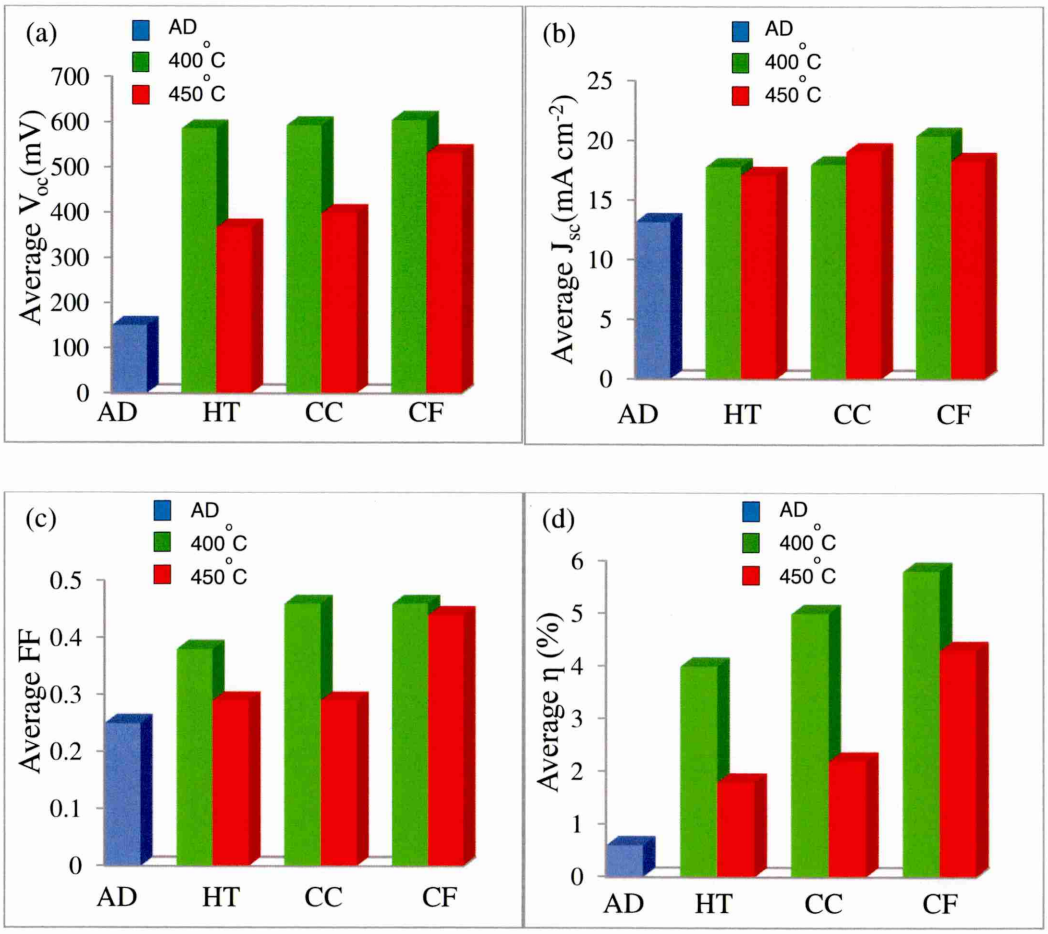


Figure 7.2: The comparison of the device parameters of (a) V_{oc}, (b) J_{sc}, (c) *FF* and (d) efficiency of CdS/CdTe solar cells with various CdS layers.

The best cells measured (marked by an asterisk) for each CdS condition in Table 7.2 are shown in Figure 7.3. The summary of the device parameters in Figure 7.3 and under dark conditions are presented in Table 7.3. The best device efficiency observed in this experiment is for films treated at 400°C. From the dark measurements, it is observed that the device fabricated with the as-deposited CdS layer has a large ideality factor, n, compared to other devices. In practical devices, n should be between 1.00 and 2.00. In this case, the high ideality factor is mainly due to the formation of a poor rectifiying junction within the device. Smaller grains of CdS layer provides large surface area for CdTe to deposit and interact. This behaviour allows a mixed compound, $CdS_{(1-x)}Te_{(x)}$, to form at the junction of CdS to CdTe. This will also provide a poor

substrate for CdTe to grow producing low electronic quality CdTe and that will cause the photovoltage and photocurrent performance in a typical heterojunction to deteriorate, which results in a low saturated current and low barrier height together with low V_{oc} and FF [3, 12]. The annealed or treated CdS layer formed a good morphology and compactness of film, which did not allow the compound to mix to a larger extent, hence favouring the formation of a high quality CdTe and better devices. Therefore, devices produce better performance. Thus, it is vital that the CdS is annealed for optimum solar cell device performance, especially for CdS thin films grown at low temperature, such as through electrodeposition. The series resistance, R_s, of the dark measurement is also high without any chemical treatment. This could be due to the formation of CdO_2 on top of the CdS surface when this layer was annealed without chemical treatment in air, thus lowering the conductivity of the CdS. The low conductivity of the window layer and the recombination of the carrier into the bulk materials eventually raise the R_s and degrade the efficiency of the solar cells [4]. This again shows a drawback of using as-deposited CdS film in the device performance.

Solar cell device with $CdCl_2$ treated CdS at 400°C demonstrated a V_{oc} slightly lower than the device with $CdCl_2$+CdF_2 treated CdS, but the increased FF overcame the loss of V_{oc} due to this treatment. This work shows that the processing step of CS_CF_400 produce the best device parameters, the lowest n (2.90) indicating minimum defect, the highest potential barrier (>0.77 eV), the highest V_{oc} and J_{sc}, the lowest R_s, the highest R_{sh} and consequently producing the highest efficiency of 6.0%. Apart of this result, it is important to mention that this batch of solar cells are apart of the high efficiency set of data. A significant number of CdS/CdTe solar cells with efficiencies equal to or greater than 6.0% demonstrate good stability and reproducibility of the devices. This can be seen in Figure 7.4.

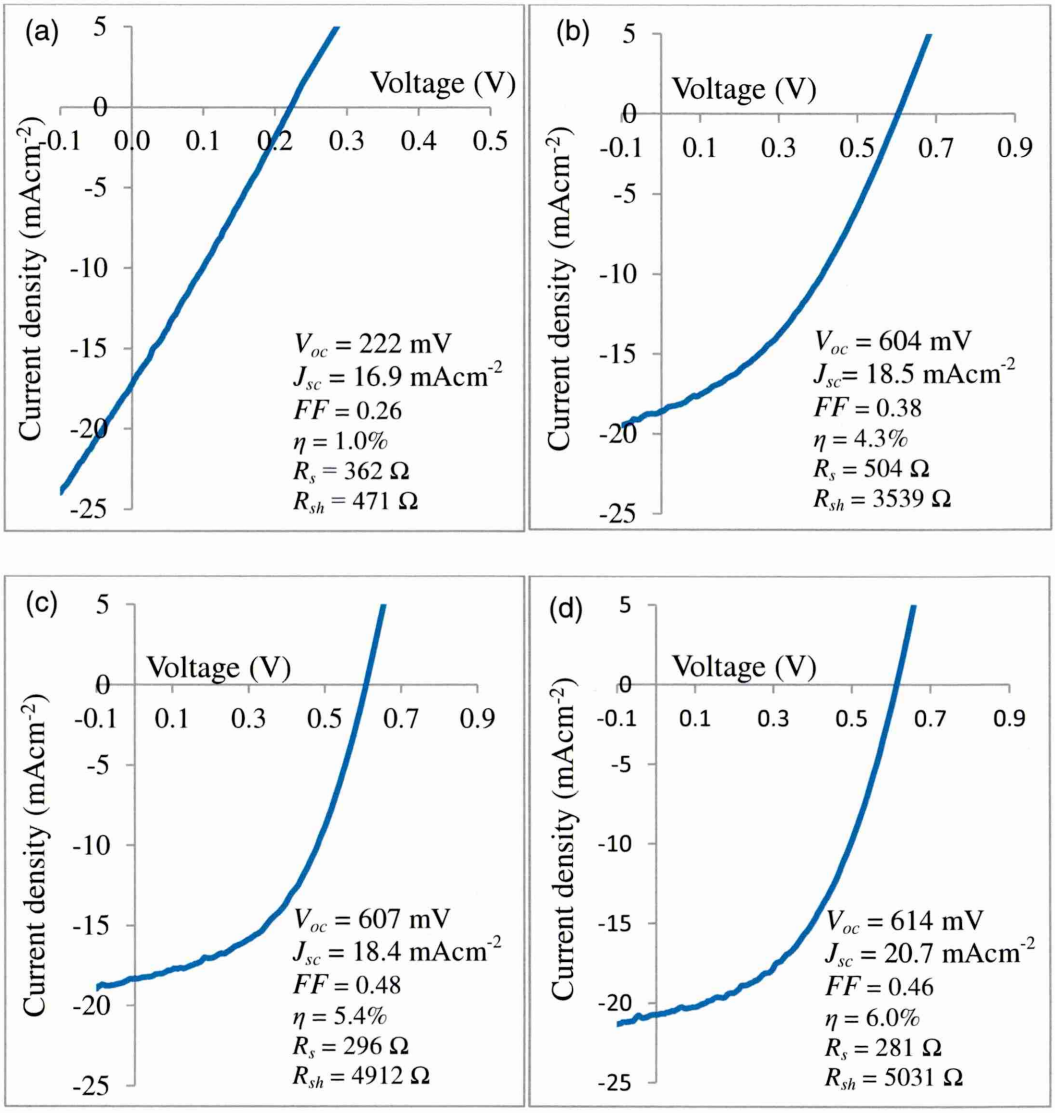


Figure 7.3: The J-V curves obtained from the highest-efficiency solar cells from (a) CS_AD, (b) CS_HT_400, (c) CS_CC_400 and (d) CS_CF_400.

Table 7.3: The details of solar cell parameters derived from J-V measurements under dark and light conditions.

Sample ID	Device Parameters								
	Dark I-V			Light I-V					
	n	I_O (mA)	ϕ_b (eV)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	R_s	R_{sh}
CS_AD	6.19	1.59×10^{-4}	>0.49	222	16.9	0.26	1.0	362	471
CS_HT_400	4.61	1.99×10^{-7}	>0.67	604	18.5	0.38	4.3	504	3539
CS_CC_400	4.24	6.31×10^{-8}	>0.69	607	18.4	0.48	5.4	296	4912
CS_CF_400	2.90	3.98×10^{-9}	>0.77	614	20.7	0.46	6.0	281	5031

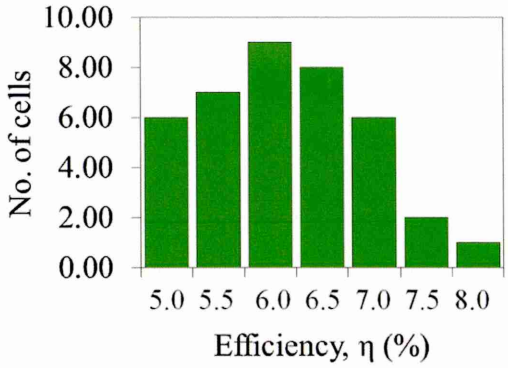


Figure 7.4: The efficiency baseline statistic of CdS/CdTe solar cells.

7.1.2 The effect of CdTe thin film conditions on CdS/CdTe solar cells

There were plenty of CdTe solar cell fabricated in this research, but in this particular experiment, CdS/CdTe solar cell devices were fabricated using various CdTe layers to get a clear trend of the effect of annealing temperatures and chemical treatments on CdTe layers. In order to maintain the same conditions for all samples in this study, in the beginning, a large glass/FTO substrate with an area 7.0×3.0 cm^2 was cleaned thoroughly, deposited with CdS layers and annealed with $CdCl_2$+CdF_2 at 400°C for 20 minutes. The above conditions were the best condition for CdS layer, as confirmed in Section 7.1.1. The sample was cooled down before the deposition of ~1500 nm of CdTe at V_g=698 mV. The glass/FTO/CdS/CdTe sample was then cut into thirteen pieces and one of these was put aside as a reference sample (as-deposited CdTe). The other twelve samples were subjected to twelve different conditions (with/without annealing, with/without chemical treatment), as described in Table 7.4. All the fabricated devices then went through the same etching and metallising process for comparison.

Table 7.4: The details of CdTe thin film conditions in the fabrication of solar cell devices.

	Conditions				
Temperature	As-deposited	Annealing without any chemical treatment	Annealing with $CdCl_2$ treatment	Annealing with $CdCl_2$+CdF_2 treatment	Annealing with $CdCl_2$+CdF_2+ $GaCl_3$ treatment
No annealing	CT_AD	-	-	-	-
385°C, 25 min	-	CT_HT_385	CT_CC_385	CT_CF_385	CT_GC_385
420°C, 20 min	-	CT_HT_420	CT_CC_420	CT_CF_420	CT_GC_420
450°C, 15 min	-	CT_HT_450	CT_CC_450	CT_CF_450	CT_GC_450

The J-V measurements under AM 1.5 illumination are shown in Table 7.5, and the trends of the average device parameters from these measurements are presented in the bar chart in Figure 7.5. The results here reported the consequence of two important factors, which are the effect of the annealing temperature on and the role of the chemical treatment of the CdTe layers in solar cell devices. From these experiments, it is observed that solar cells fabricated with as-deposited layers generally measure low on all device parameters [1, 4–5]. The as-deposited CdTe is a highly defective material. The electrical property of as-deposited CdTe is dominated by residual impurities, Cd interstitials or Te vacancies and numerous grain boundaries [6, 7]. Therefore, it needs an appropriate annealing process to enhance its properties for higher device performance. The annealing process can remove the recombination centres in the CdTe and the interface for better carrier collection [8–11]. As the CdTe layers were annealed (even without any chemical treatments), all the device parameters improved. However, it is also spotted that one of the solar device (sample CT_HT_385) still has a low J_{sc}, even after annealing without any chemical treatment at 385°C. This could be due to the low annealing temperature. In this case, the annealed process without any chemical treatment may require higher temperatures than 385°C to improve the crystallisation, grain size and conductivity of the film. As the annealing temperatures increased, the average V_{oc} and FF and the efficiency improved. In particular, device annealed in air at 450°C, demonstrates the best performance compared to the other two devices annealed without chemical treatment at 385°C and 420°C.

The positive effects of the chemical treatments on CdTe films for solar cell devices are well known in terms of grain growth, recrystallisation, lifetime of charge carriers, CdS/CdTe junction improvement and defect states reduction within the CdS/CdTe device [12–16, 18]. It is observed that the efficiency of the devices treated with $CdCl_2$ improved compared to those annealed without any chemical treatment. This improvement is mainly in the V_{oc} and the *FF*. The J_{sc} increased as the $CdCl_2$ treatment temperature increased to 450°C because of enlarged CdTe grain size, eliminating the defects and reduced recombination centres in the junction, which enhances the carrier collection of the device, thus it delivered high efficiency with 6.6%.

The V_{oc} of the devices treated with $CdCl_2$+CdF_2 at 385°C and 420°C are generally high compared to the devices with other chemical treatments. In fact the device parameters, including V_{oc}, J_{sc}, *FF*, and efficiency, are improved as the $CdCl_2$+CdF_2 treatment temperature increased from 385°C to 420°C. Fluorine has higher vapour pressure and a lower atomic radius and density than chlorine. The presence of fluorine should be more pronounced and showed drastic improvement in the overall solar cell device [17, 18]. Therefore, it required low activation energy and annealing temperature to diffuse through the CdTe grain boundary compared to chlorine. The V_{oc} together with the *FF* and efficiency, however, start to reduce as the CdTe is treated at more than 420°C, although J_{sc} is still increased. The increment in the J_{sc} and reduction in the V_{oc} and the *FF* at high annealing temperatures is due to the enlargement of the grain size together with the formation of gaps between grain boundaries and the degradation of crystallinity, conductivity and loss of material, as discussed in Chapter 5. The too-high $CdCl_2$+CdF_2 treatment temperature (> 420°C) may cause the CdTe layer and device performance to deteriorate. In this set of experiments, the best photovoltaic property is achieved in the device with $CdCl_2$+CdF_2 treated CdTe at 420°C with 6.8% of efficiency.

In Table 7.5, it can be observed that the solar cells fabricated using $CdCl_2$+CdF_2+$GaCl_3$ treated CdTe films generally have a high J_{sc}. The presence of the Ga in the chemical treatment removes Te precipitates in the CdTe layer, thus making it more stoichiometric. It also reduce the diffusion of CdTe and CdS layers at the interface, thus eliminating the alloy interface of $CdS_{(y)}Te_{(1-y)}$ and improving the device performance, especially carrier collection. This result is associated with the large grain size, low doping density and highest mobility observed in Section 5.3, which increased

carrier transport and current collection at the CdTe grain boundaries. Also, the presence of small voids and gaps between the grain boundaries, in the SEM images in the previous chapter, are the main reasons why the V_{oc} and the *FF* are lower for these devices than devices with other chemical treatments.

From this batch under investigation, it can be concluded that both annealing and chemical treatments affect the device performance. Too much annealing in the presence of chemical treatment may cause the CdTe films to deteriorate and may consequently lower the device efficiency. The device with a CdTe layer treated with $CdCl_2$+CdF_2 at 420°C obviously shows a better efficiency than others since it has better crystallinity, higher conductivity, mobility and a larger grain size without gaps or voids.

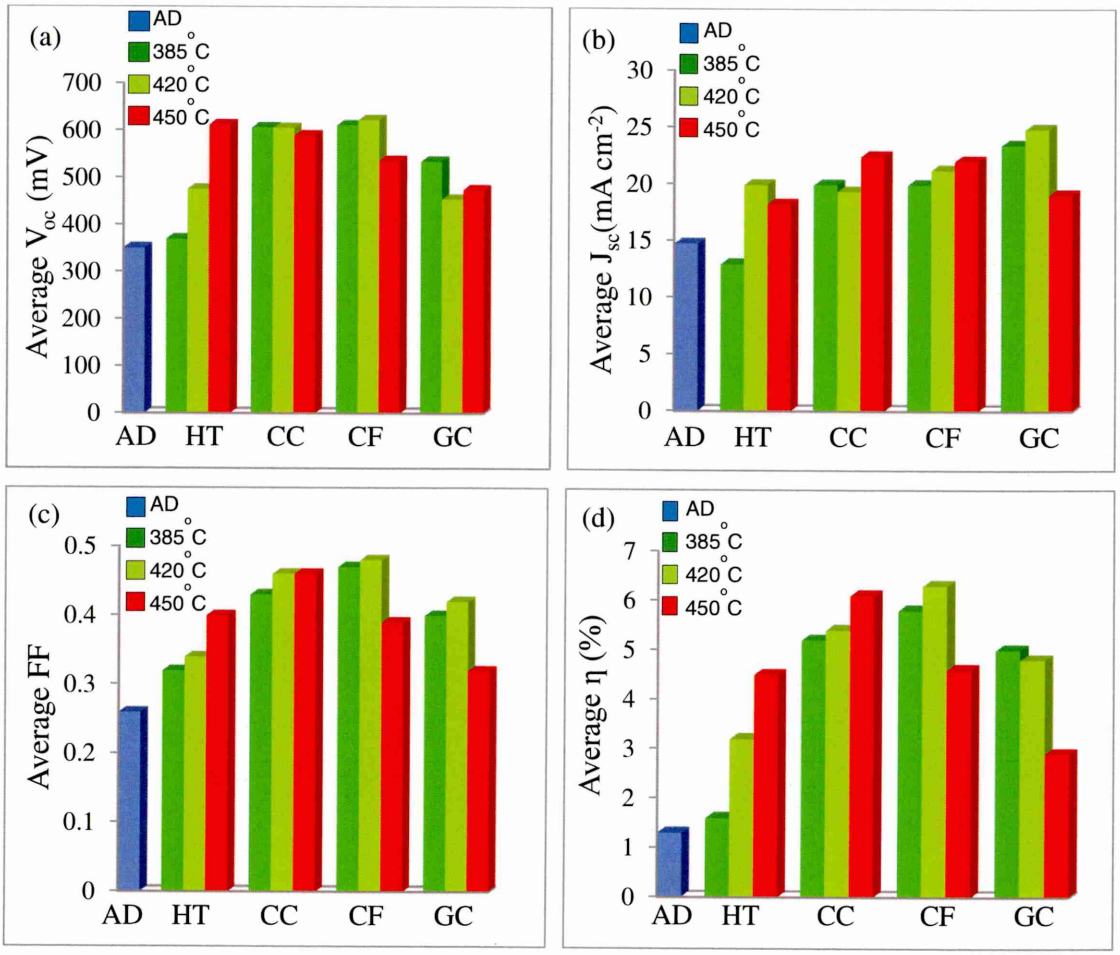


Figure 7.5: The average device parameters of (a) V_{oc}, (b) J_{sc}, (c) *FF* and (d) efficiency of g/FTO/CdS/CdTe/Au solar cells fabricated with various conditions of CdTe layers.

Table 7.5: The measurements of the solar devices fabricated with different CdTe conditions under AM 1.5 illumination. Note that the asterisk represents the highest-efficiency cell.

	Measurement					Average			
Sample ID	No.	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF (%)	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF (%)	η (%)
CT_AD	1	348	14.9	0.26	1.3				
	2	350	13.5	0.25	1.2				
	3*	352	15.6	0.26	1.4	350	14.7	0.26	1.3
CT_HT _385	1*	372	13.6	0.33	1.7				
	2	370	12.0	0.33	1.5				
	3	365	13.1	0.31	1.5	369	12.9	0.32	1.6
CT_HT _420	1*	497	20.3	0.34	3.4				
	2	455	19.4	0.34	3.0				
	3	473	20.0	0.33	3.1	475	19.9	0.34	3.2
CT_HT _450	1	610	18.0	0.40	4.4				
	2	608	17.4	0.40	4.2				
	3*	619	19.1	0.41	4.9	612	18.2	0.40	4.5
CT_CC _385	1*	614	20.1	0.44	5.4				
	2	607	20.0	0.44	5.3				
	3	598	19.7	0.41	4.8	606	19.9	0.43	5.2
CT_CC _420	1*	607	19.8	0.47	5.6				
	2	610	18.5	0.46	5.2				
	3	598	19.7	0.46	5.4	605	19.3	0.46	5.4
CT_CC _450	1*	592	23.7	0.47	6.6				
	2	585	21.4	0.46	5.8				
	3	590	22.2	0.46	6.0	589	22.4	0.46	6.1
CT_CF_ 385	1	609	19.7	0.48	5.8				
	2*	622	20.8	0.48	6.2				
	2	603	19.3	0.46	5.4	611	19.9	0.47	5.8
CT_CF_ 420	1*	625	22.5	0.48	6.8				
	2	622	21.8	0.48	6.5				
	3	619	19.3	0.47	5.6	622	21.2	0.48	6.3
CT_CF_ 450	1*	554	22.5	0.39	4.9				
	2	505	21.4	0.40	4.3				
	3	548	22.1	0.38	4.6	536	22.0	0.39	4.6
CT_GC _385	1*	554	25.4	0.39	5.5				
	2	545	22.9	0.40	5.0				
	3	503	21.8	0.40	4.4	534	23.4	0.40	5.0
CT_GC _420	1	467	26.3	0.43	5.3				
	2*	470	26.0	0.44	5.4				
	3	425	22.0	0.39	3.6	454	24.77	0.42	4.8
CT_GC _450	1*	497	20.3	0.34	3.4				
	2	450	19.2	0.31	2.7	474	18.97	0.32	2.9

	3	476	17.4	0.32	2.7				

The J-V characteristics of the best cells measured (marked with an asterisk) for each CdTe film condition in Table 7.5 have been plotted in Figure 7.6. The device parameters of these cells under dark and illuminated conditions are presented in Table 7.6. The best-efficiency devices observed in this experiment are mainly among the chemically treated CdTe films, especially those treated with $CdCl_2$+CdF_2. Table 7.6 also indicates that the solar cell fabricated with as-deposited CdTe film has a large diode ideality factor, low ϕ_b and small R_{sh}, thus explaining why the *FF*, V_{oc} and the efficiency are low. This is because the as-deposited CdTe has small grain size, low crystallinity, low conductivity and low mobility. The devices annealed without any chemical treatment, however, show an improvement in I_o and ϕ_b together with increases in shunt resistance and all device parameters under illumination, but these improvements are typically low. Then again, the ideality factor obtained for this device is still high. A large ideality factor indicates that the forward biased current is smaller compared to that predicted by the thermionic emission. In fact it is always associated with the defects, Te precipitates and the presence of recombination centers in the material. The defect can cause high density of the surface state with the presence of large number of trapping states and high series resistance within the device while the presence of recombination center may reduce the carrier collection within the device. This is the reason that even the annealing process has improved the formation of the junction, the chemical treatment is needed to remove the defects, and the Te precipitates and initiates the process that occurs at the junction [19, 20].

Devices with $CdCl_2$ treated CdTe had a diode quality factor that varied in the range of 2.20 to 2.79, and the ϕ_b increased from 0.67 to 0.76 eV as the treatment temperature increased from 385°C to 450°C. The R_{sh} also increased up to 420°C and then reduced slightly with higher annealing temperatures, which is believed due to the formation of columnar type of larger grains creating gaps in between and leads to high V_{oc}, lower R_{sh} and *FF*. At 450°C the average V_{oc} is lower than at 420°C, but as a consequence of an improved J_{sc}, the second-best efficiency is acquired at this temperature. The ideality factor, I_o and the ϕ_b of the devices treated with $CdCl_2$+CdF_2 are also in the range of 2.06 to 2.67, 1.26 to 15.8×10^{-9} mA and 0.73 to 0.80 eV, respectively. Then again, the shunt resistance reduces when the $CdCl_2$+CdF_2 treatment temperature is more than 385°C, which may be because the high diffusivity in fluorine

over-treats the films at high temperatures and leads to deterioration of the layer. The *FF* and J_{sc} improved as temperature increased from 385°C to 420°C and then remained almost constant. This could be related to grain size that also follows this trend. The $CdCl_2$+CdF_2+$GaCl_3$ treated device however shows a slight deterioration in the diode quality factor, potential barrier height, and I_o, and consequently the R_{sh}, and all device parameters except the J_{sc} were measured under illumination. As discussed previously, this trend is due to the grain growth together with the widening of the grain boundaries, which increased the leakage path. The best η of solar cell devices in this set of experiments is obtained at cell number one in the device with $CdCl_2$+CdF_2 treated CdTe at 420°C with 6.8%. This cell has good *FF* and the highest V_{oc}, which is associated with the highest potential barrier and good quality factor (n=2.06), which are due to the formation of a better junction and carrier collection and low interface state densities, reduced defects, low interface recombination and few pinholes [21].

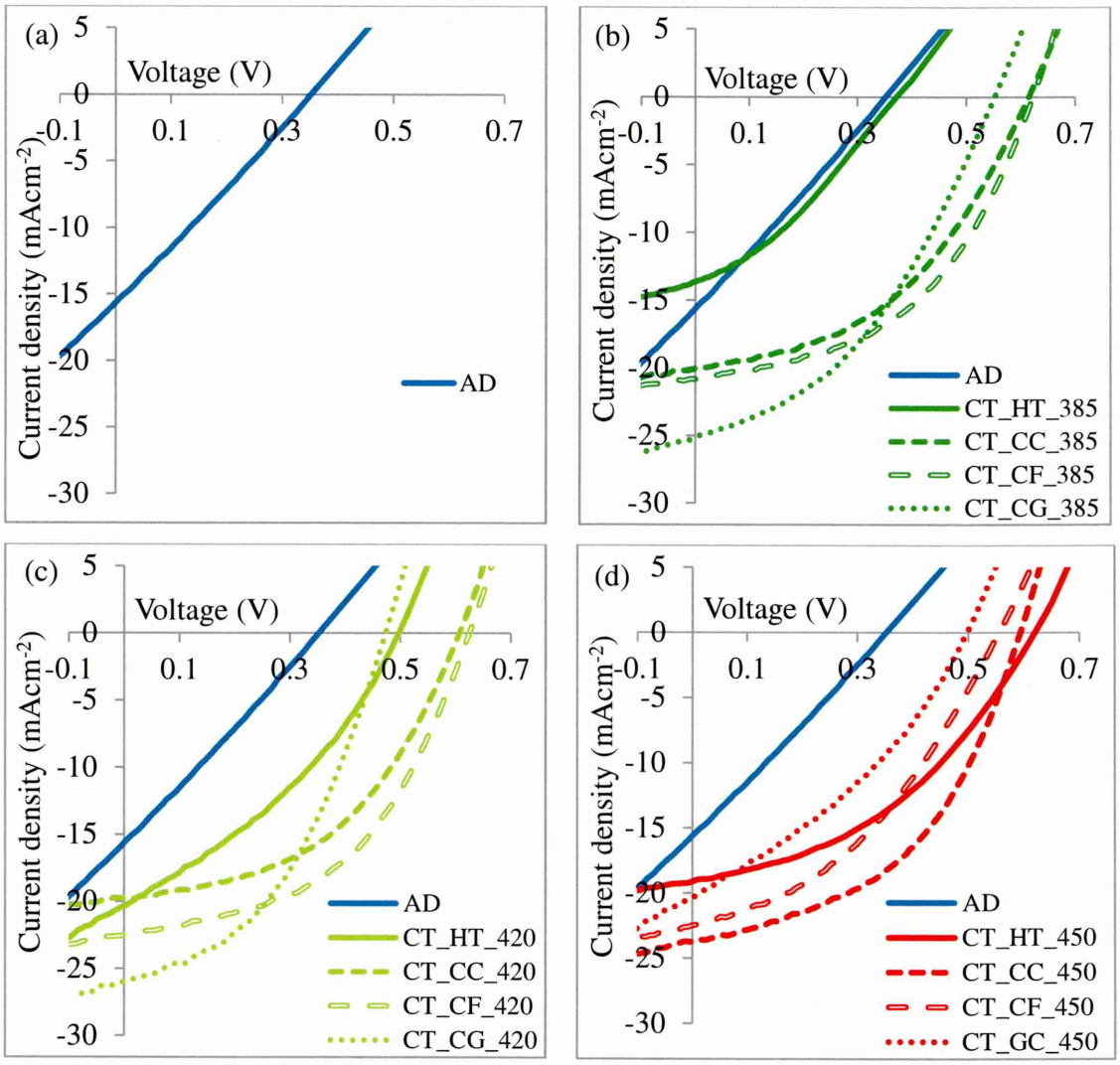


Figure 7.6: The J-V characteristics of the best solar cells measured in Table 7.5 for (a) as-deposited, and annealed with and without chemical treatment at (b) 385°C, (c) 420°C and (d) 450°C.

Table 7.6: The details of the solar cell measurements under AM 1.5 illumination and dark conditions.

Sample ID	Device Parameters								
	Dark I-V			Light I-V					
	n	I_o (mA)	ϕ_b (eV)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	R_s	R_{sh}
CT_AD	10.31	1.26×10^{-4}	>0.49	352	15.6	0.26	1.4	668	811
CT_HT_385	8.70	1.99×10^{-7}	>0.67	372	13.6	0.33	1.7	718	2907
CT_HT_420	7.29	3.16×10^{-5}	>0.53	497	20.3	0.34	3.4	334	1302
CT_HT_450	3.52	1.26×10^{-7}	>0.68	619	19.1	0.42	4.9	426	4757
CT_CC_385	2.44	5.01×10^{-9}	>0.76	614	20.1	0.44	5.4	329	4866
CS_CC_420	2.79	1.58×10^{-8}	>0.73	607	19.8	0.47	5.6	290	5939
CT_CC_450	2.20	1.99×10^{-7}	>0.67	592	23.7	0.47	6.6	221	5329
CT_CF_385	2.11	1.99×10^{-9}	>0.78	622	20.8	0.48	6.2	272	6161
CS_CF_420	2.06	1.26×10^{-9}	>0.80	625	22.5	0.48	6.8	261	4987
CT_CF_450	2.67	1.58×10^{-8}	>0.73	554	22.5	0.39	4.9	384	3409
CT_GC_385	3.05	2.51×10^{-8}	>0.72	554	25.4	0.39	5.5	320	2945
CS_GC_420	2.02	2.00×10^{-9}	>0.78	470	26.0	0.44	5.4	225	2711
CT_GC_450	4.71	3.98×10^{-7}	>0.65	497	20.3	0.34	3.4	334	1309

7.1.2.1 Defect characterisation and study of Fermi-level movement

The effects of $CdCl_2$ treatment on the defect levels have been studied on CdS/CdTe devices grown with as-deposited and after $CdCl_2$ treated CdTe through PL measurement. The sample preparation starts by cleaning 3.0×1.0 cm^2 of a glass/FTO substrate followed by CdS deposition. The film was then treated, which was followed by CdTe deposition for ~1500 nm before the film was cut into three pieces to make three glass/FTO/CdS/CdTe samples. One sample is put aside as a reference sample (as-deposited sample). The second sample was heat-treated once with $CdCl_2$ and the third sample was double heat-treated with $CdCl_2$.

Figure 7.7 and Table 7.7 show the photoluminescence (PL) spectra of the samples with as-deposited, $CdCl_2$-treated and double $CdCl_2$ treated CdTe layers. Four

electron trap levels were observed with varying intensities, indicating that the origin of these defects is mainly the native defects [22]. From the PL spectra peaks, it is observed that the device with $CdCl_2$ treatment eliminates two defect levels (T_1 and T_3) completely and the mid-gap recombination centre (T_2) is reduced drastically after $CdCl_2$ treatment. It is also noted that there is no considerable difference between single and double treatment, except a little further reduction in T_1, T_2 and T_4 peaks. The reductions of the energy distribution of T_1, T_2 and T_4 together with the sharpening of the bandgap peak are excellent results to observe. It is noted that the T_2 is a "killer centre" situated at the mid gap and this reduction is one of the main reasons that the $CdCl_2$ treated CdTe device has a good photovoltaic performance. It seems that chlorine is acting as a fluxing agent for growing highly crystalline CdTe with few defects [22, 23].

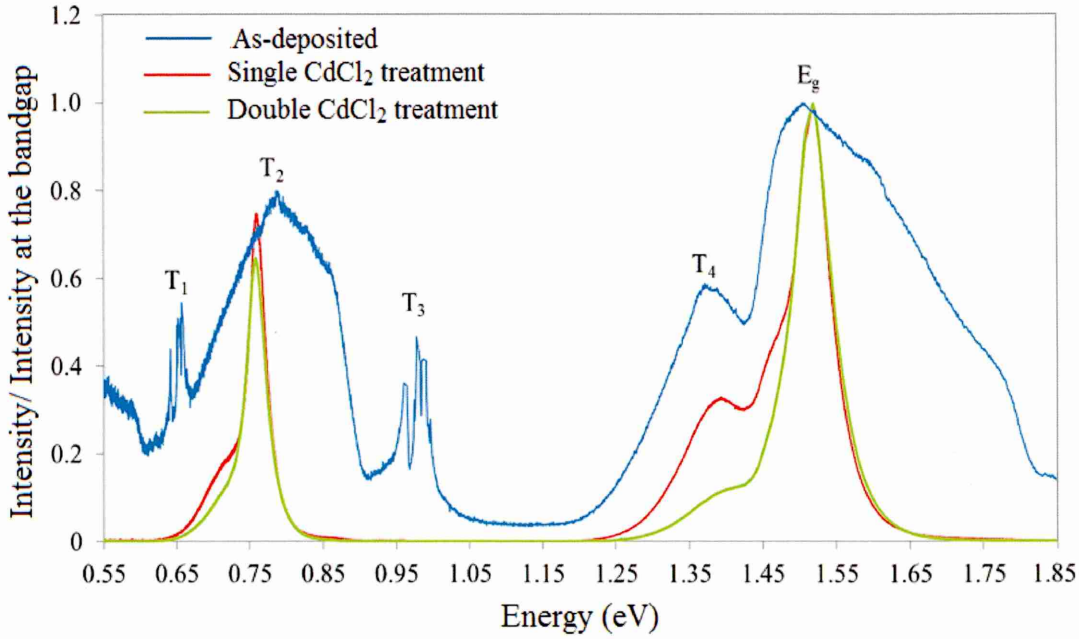


Figure 7.7: PL spectra for as-deposited, single and double $CdCl_2$ treated CdS/CdTe layers. (This measurement has been carried out at University of Louisville, USA, through our research collaboration).

Table 7.7: Details of PL peaks measured at 80 K for glass/FTO/CdS/CdTe samples.

	Defect/Energy Level (eV)				
Sample	T_1	T_2	T_3	T_4	E_g
As-deposited	0.66	0.79	0.98	1.37	1.50
Single $CdCl_2$ treatment	-	0.76	-	1.39	1.51
Double $CdCl_2$ treatment	-	0.76	-	1.39	1.51

An ultra-violet photoemission spectroscopy, UPS, study has been carried out to investigate the changes in doping concentrations and hence indirectly deduce the position of the Fermi level in the CdTe layers during $CdCl_2$ treatment. Similar to the previous preparation in the PL study, the device structure of g/FTO/CdS/CdTe was prepared for the as-deposited measurement and after single $CdCl_2$ treatment and double $CdCl_2$ treatment for this experiment.

Table 7.8 summarises the UPS results for as-deposited and after single and double $CdCl_2$ treatment CdTe layers. The bandgap of CdTe has been taken to be 1.44 eV for calculations of E_c-E_F values [24]. The Fermi-level positions of the as-deposited and after single and double $CdCl_2$ treatment layers are shown in Figure 7.8 for easy reference. It is noted that the as-deposited CdTe for this sample is n-type CdTe. UPS results show that the as-deposited n-CdTe remains an n-type after $CdCl_2$ treatment. The Fermi level tends to stay in the upper half of the bandgap. The $CdCl_2$ treated samples show the settling of the Fermi level in the upper half of the bandgap, showing n-type electrical conductivity. This result contradicts the characterisation made of the single CdTe layer in Chapter 5. From the PEC measurement in Section 5.3.3 in Chapter 5, the as-deposited n-CdTe films converted to p-type after annealing in the presence of $CdCl_2$. It is clear that the native defects and impurities present in the whole device changed the conductivity type of the layer. This creates a challenging task and demands careful experimentation to establish the right conditions for high efficiency devices.

Table 7.8: Position of the Fermi level (E_c-E_f) for measurement with UPS for as-deposited and after single and double $CdCl_2$ treatment CdTe layers on glass/FTO/CdS/CdTe [24].

Sample description	E_f - E_v (eV)		Average E_f-E_v (eV)	E_c- E_f (eV)		Average E_c-E_f (eV)
As-deposited	1.44	1.04	1.24	0.00	0.40	0.20
Single $CdCl_2$ treatment	0.72	1.08	0.90	0.72	0.36	0.54
Double $CdCl_2$ treatment	1.30		1.30	0.14		0.14

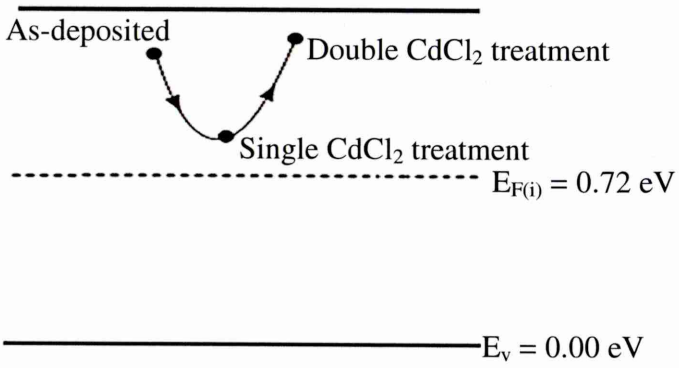


Figure 7.8: Fermi-level positions as determined with UPS for as-deposited and after single and double $CdCl_2$ treatment CdTe layers in glass/FTO/CdS/CdTe devices [24]. (This measurement has been carried out at University of Louisville, USA, through our research collaboration).

7.1.3 The effect of p- or n-absorber layer (CdTe) on CdS/CdTe solar cells

This experiment reports the study on the effect of p- and n-CdTe layers on solar cell device performances. The preparation for this work starts by depositing ~200 nm of CdS on a clean glass/FTO with dimension 2×4 cm^2. The deposited CdS layer was then treated with $CdCl_2$+CdF_2 at 400°C for 20 minutes before being cut into 4 pieces. The first sample was grown at V_g=705 mV for the p-CdTe layer while the second sample was grown at V_g=698 mV for the n-CdTe layer. The thickness of CdTe of these two samples was ~1500 nm. The third sample was coated with ~750 nm of n-CdTe followed by ~750 nm of p-CdTe. The fourth sample was coated with ~1200 nm of n-CdTe followed by ~300 nm of p-CdTe film. The total thickness of CdTe films on the third and fourth samples was also maintained at ~1500 nm for comparison. The details of the device are shown in Table 7.9. All these samples were then annealed at 450°C in presence of $CdCl_2$+CdF_2 and went through the same etching and metallising process.

Table 7.9: The details of the devices fabricated to study the effect of p- and n-CdTe.

Device initial	Device structure
D_np	g/FTO/n-CdS (~200 nm)/p-CdTe (~1500 nm)/Au
D_nn	g/FTO/n-CdS (~200 nm)/n-CdTe (~1500 nm)/Au
D_nnp1	g/FTO/n-CdS (~200 nm)/n-CdTe (~750 nm)/ p-CdTe (~750 nm)/Au
D_nnp2	g/FTO/n-CdS (~200 nm)/n-CdTe (~1200 nm)/ p-CdTe (~300 nm)/Au

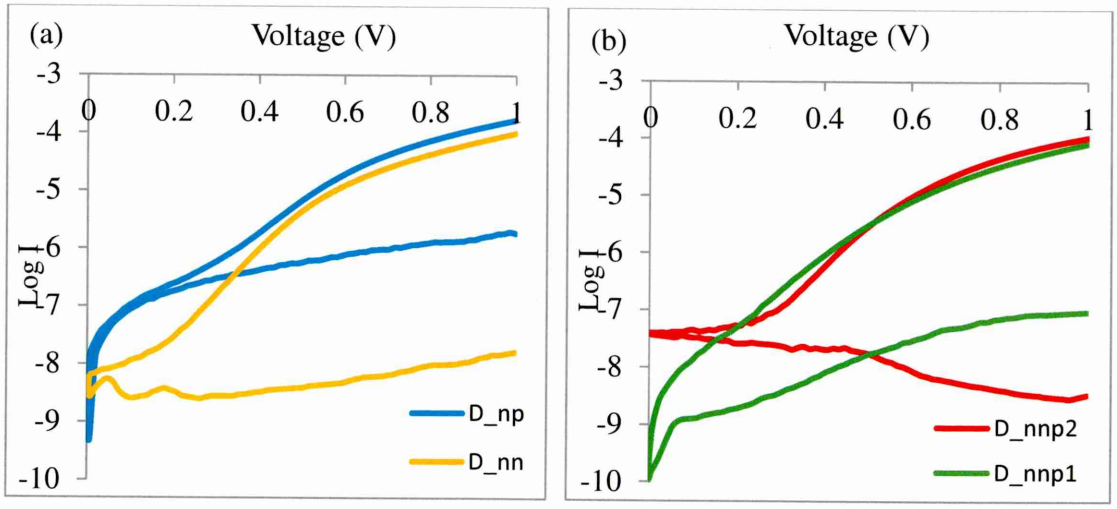
The parameters of the solar cells measured under illumination and dark condition are shown in Table 7.10. The J-V characteristics for measurement under light and typical log linear I-V characteristics under dark conditions are shown in Figure 7.9. By comparing devices fabricated with n-p and n-n structures (D_np and D_nn), it is observed that the rectification factors, diode ideality factor and potential barrier height for devices made from n-CdTe are much improved than those devices made from p-CdTe. Most of the device parameters measured under illumination including J_{sc}, FF, efficiency and series resistance are also considerably better than devices made from p-CdTe. The advantage of n-CdTe films in the fabrication of high-efficiency solar cells has been reported by many researchers [6, 26, 27, 28]. One of the reasons why n-CdTe is better is their high conductivity and mobility properties, as discussed in Section 5.15. Another reason is the existence of two PV active junctions, which are the n-n-heterojunction at the n-CdS/n-CdTe interface and large Schottky barrier at the CdTe/metal interface instead of a typical single p-n junction for an n-CdS/p-CdTe solar cell (see Figure 7.10) [2, 34]. The combination of these junctions will enhance the carrier collections and result in excellent J_{sc} and better efficiency, as shown in Table 7.10. The large Schottky barrier formed at the back metal contact of an n-n solar cell is an advantage since it could change the barrier height depending on the Fermi level pinning at the interface.

Further study has been carried out by fabricating a solar cell with a combination of n- and p-CdTe to form a graded-bandgap solar cell with n-n-p junctions. The first device has the same thicknesses (~750 nm) of n- and p-CdTe, while the second device has a ~1200 nm layer of n-CdTe and a ~300 nm layer of p-CdTe. From the dark measurement, it is shown that the devices fabricated with thicker n- and thinner p-CdTe layers demonstrated an excellent diode with an RF at 1.00 V by about 4.5 orders of magnitude, an n of 2.20, an I_o of 6.61×10^{-10} and a potential barrier greater than 0.81 eV. This means this structure offered a healthier formation of the depletion region than

those with equal n- and p-CdTe thicknesses. The insertion of a thin p-type layer on an n-type CdTe before back metal contact has increased the slope of the band at the n-p homojunction and a metal-semiconductor barrier, which results in a strong built-in electric field [29]. The J_{sc}, however, was slightly lower than in a D_nn device, but the FF and V_{oc} have a better result since a very thin layer of p-CdTe helps to improve the Schottky barrier height. The highest-efficiency cell from this set of experiments has 7.7% with a very thin p-CdTe at the back contact forming a graded-bandgap solar cell in combination with a good-quality n-n heterojunction, n-p homojunction and ohmic contact at the back. It is suggested that future work should be focused to optimise the device architecture based on graded-bandgap structure for high-efficiency solar cells.

Table 7.10: The details of devices measured in the dark and under AM 1.5 illumination.

Device initial	Device Measurement									
	Dark I-V				Light I-V					
	R.F	*n*	I_o (mA)	ϕ_b (eV)	V_{oc} (V)	J_{sc} (mA cm^{-2})	*FF*	η (%)	R_s (Ω)	R_{sh} (Ω)
D_np	$10^{1.91}$	3.13	7.94×10^{-9}	0.75	640	22.1	0.31	4.4	832	2498
D_nn	$10^{3.75}$	2.16	6.31×10^{-10}	0.81	566	31.9	0.36	6.5	371	2437
D_nnp1	$10^{2.93}$	2.67	3.16×10^{-9}	0.77	598	28.4	0.36	6.1	368	1821
D_nnp2	$10^{4.50}$	2.20	6.61×10^{-10}	0.81	650	28.3	0.42	7.7	316	3778



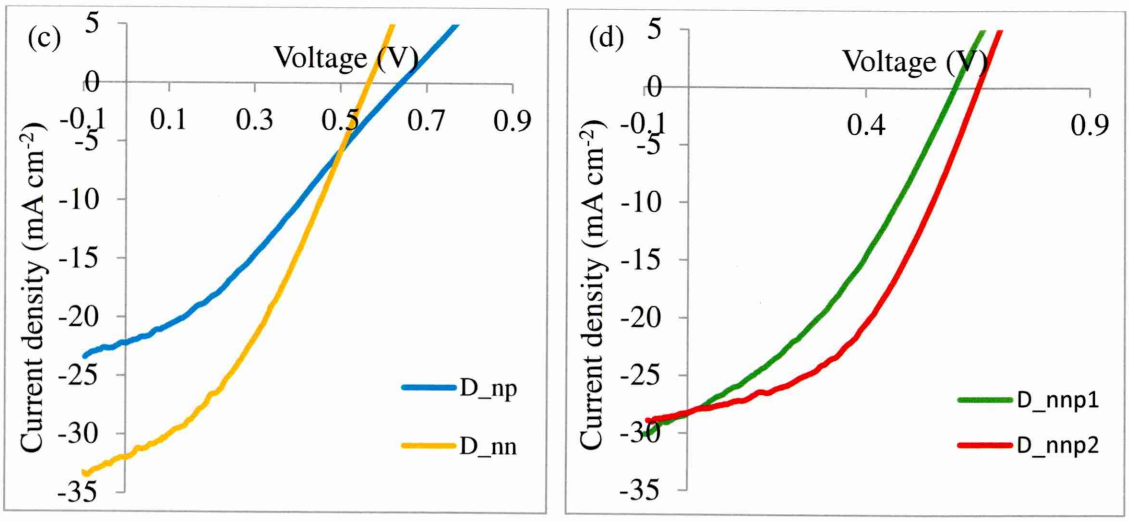


Figure 7.9: The dark log I versus V for device (a) D_np and D_nn along with (b) D_nnp1 and D_nnp2 and the J-V characteristic of CdS/CdTe solar cells measured under AM 1.5 illumination for (c) D_np and D_nn in addition to (d) D_nnp1 and D_nnp2.

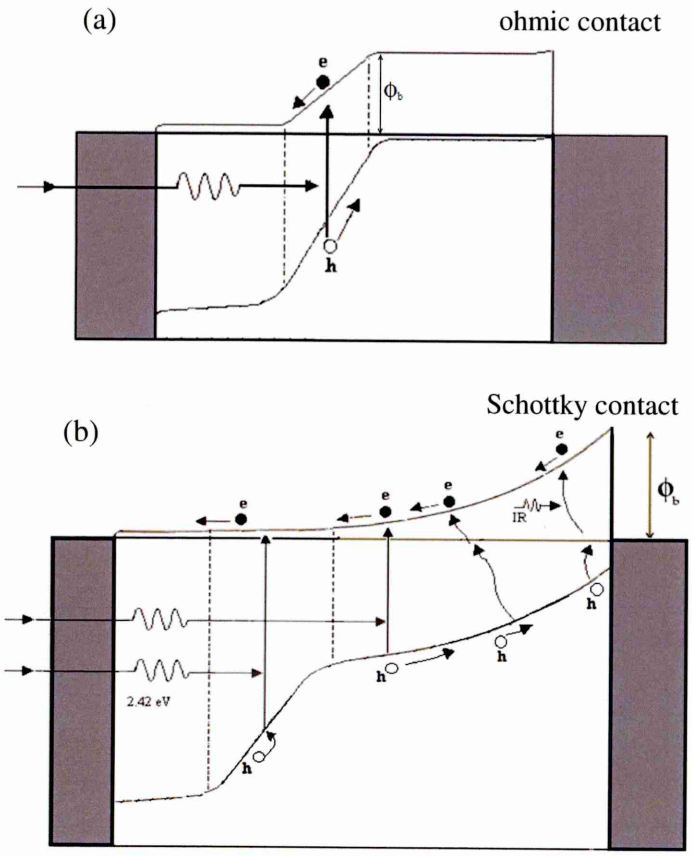


Figure 7.10: The energy band diagram of the (a) device D_np with a typical p-n junction and (b) device D_nn with a n-n heterojunction and a large Schottky barrier at the back metal contact [34].

The C-V measurement for D_np, D_nn, D_nnp1 and D_nnp2 devices has been carried out to study the depletion region and to estimate the diffusion voltage V_{bi} and the doping concentration. The graph for C versus V measured at 1.0 MHz frequency is shown in Figure 7.11, and the depletion capacitance at zero bias, C_o, and the calculated depletion width is shown in Table 7.11. It is observed that the device fabricated with the typical p-n junction using p-CdTe as an absorber layer has a narrow depletion region with 476 nm. A device with a narrow depletion region is basically not good, since the generated carrier needs to pass through the resistive path full of defects and recombination centres before being collected at the metal contact. The device fabricated with an n-n- junction using n-CdTe as an absorber layer shows a depletion width of 932 nm, which is almost double the depletion region of a device with a p-n junction. This explains why this device produces a very high J_{sc}. The depletion region is the heart of a solar cell device, where the incident photons give off energy to generate electron-hole pair [30]. A strong built-in electric field is caused by the wide bandgap. In this case, a strong electric field enhances the separation of the charge carriers and speeds up the photogenerated electron to the FTO and transfers holes to the Au back contact with little or no recombination.

The idea of the same ratio of thicknesses of n- and p-CdTe as absorber layers (Device_nnp1), however, is not as good as was expected, but the attempt to use a 4:1 thickness ratio of n-CdTe to p-CdTe on device D_nnp2 shows a fully depleted region with a strong built-in potential. The ideal depletion region is required to effectively collect the charge carrier and drift through the high-field depletion region without loss due to recombination [31, 32]. Therefore the ideal one is always the fully depleted solar cell, since the generated carrier can directly drift to the respective electrical contacts. A wider depletion region increases the current collection and the electric field of drift carrier collection over the entire absorber region and consequently produces a better solar cell.

The graph of $1/C^2$ versus V and the calculated doping density and fermi-level position is shown in Table 7.11. The Fermi-level calculation for device D_nn (n-CdTe) used equation 3.34, while devices D_np, D_nnp1 and D_nnp2 (p-CdTe, or device with n-p-CdTe) used equation 3.35 for Fermi-level calculation. Both devices have good diode properties. Figure 7.12 (d) shows an ideal $1/C^2$-V curve. Devices D_np, D_nn and D_nnp1, however, show movement of the built-in potential, V_{bi} point due to the

oxidation of the layer caused by the etching process, and the presence of defects. Also, it was observed that the device fabricated with the n-absorber layer has a higher doping density, which brings the Fermi level up to 0.90 eV, and a higher depletion region than those fabricate with solely p-CdTe. The illustration of Fermi-level positions of all devices can be seen in Figure 7.13.

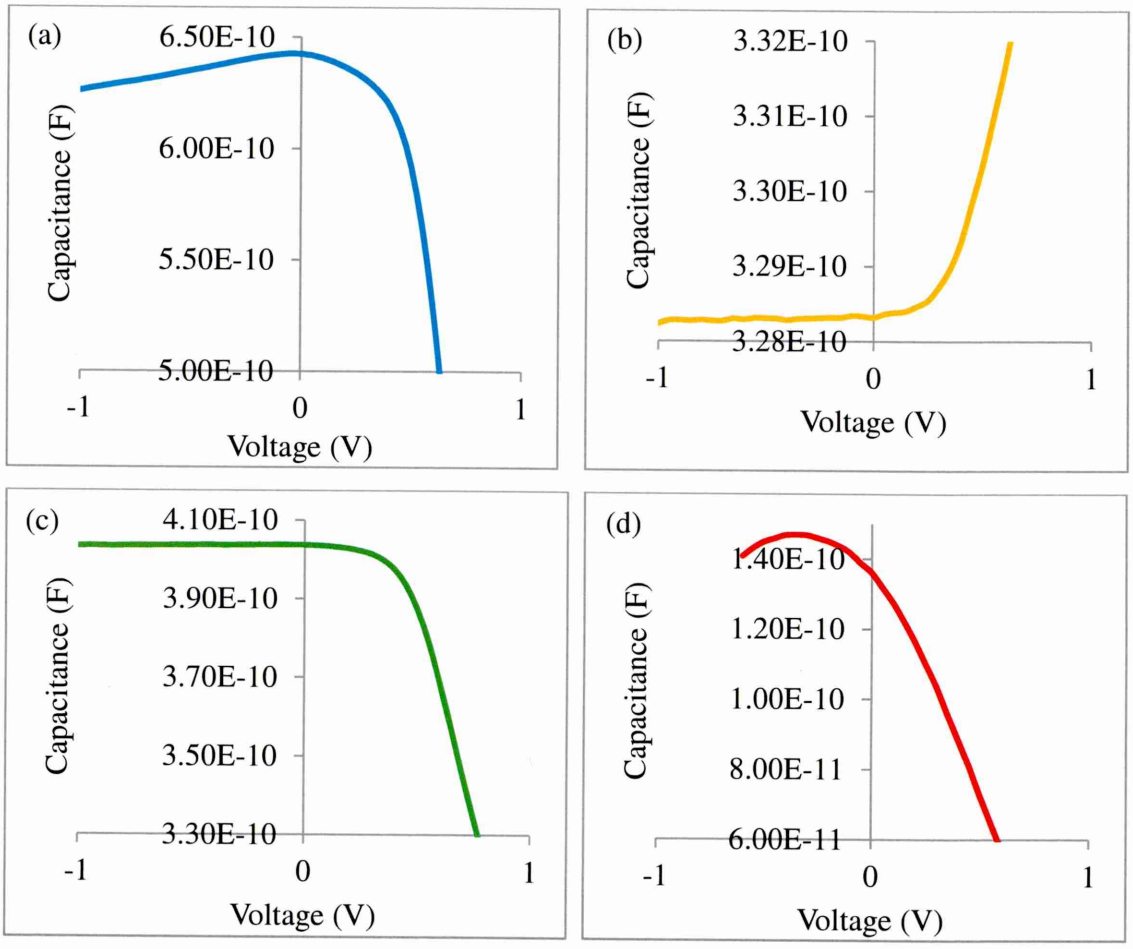


Figure 7.11: The C-V spectra of the solar cell devices fabricated from (a) D_np, (b) D_nn, (c) D_nnp1 and (d) D_nnp2.

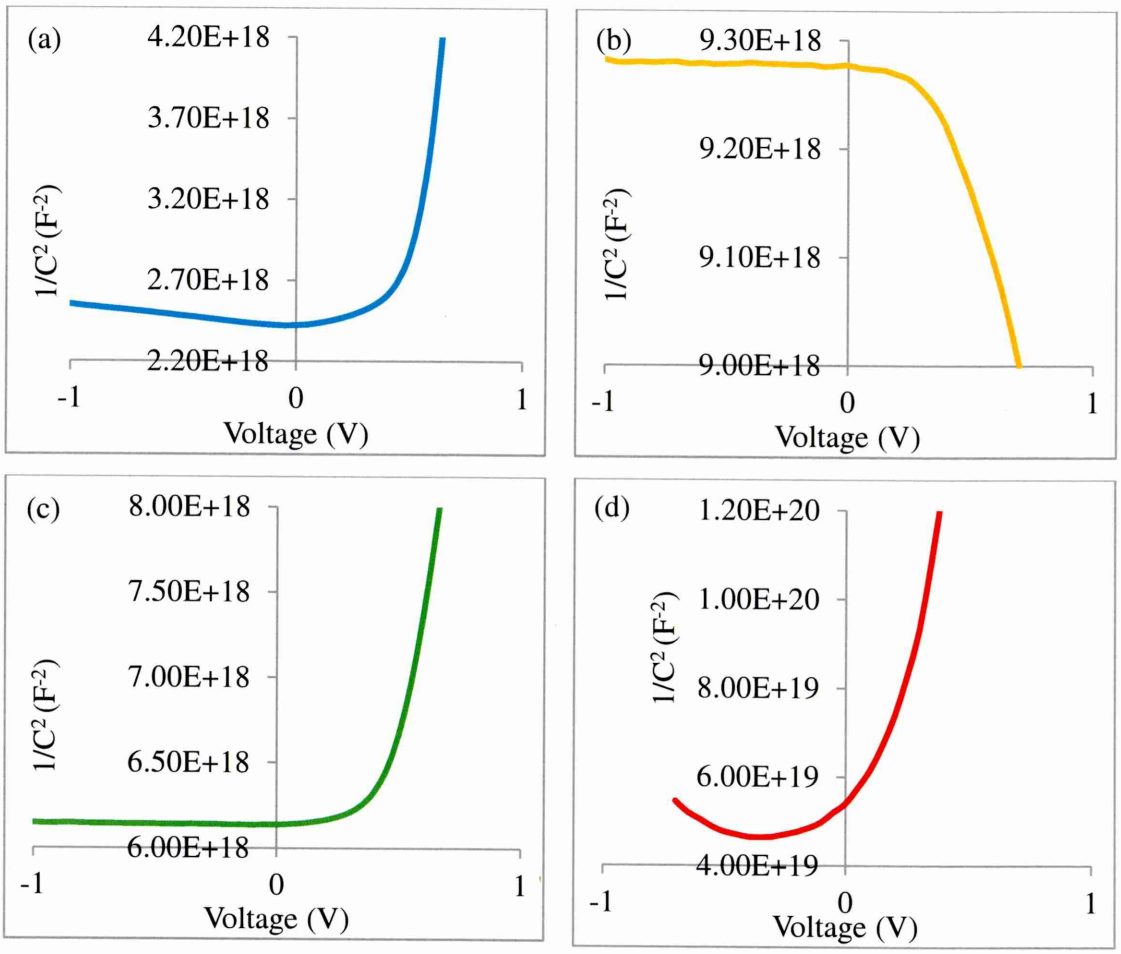


Figure 7.42: The $1/C^2$-V spectra of the solar cell devices fabricated from (a) D_np, (b) D_nn, (c) D_nnp1 and (d) D_nnp2.

Table 7.11: The parameters of the depletion widths, doping densities and fermi-level positions for the measured devices.

Device initial	C_o (F)	W (nm)	n (cm^{-3})	Fermi-level position (eV)	
				E_f-E_v	E_c-E_f
D_np	6.42×10^{-10}	476	6.02×10^{14}	0.59	0.85
D_nn	3.28×10^{-10}	932	1.30×10^{16}	0.98	0.47
D_nnp1	4.04×10^{-10}	758	1.18×10^{15}	0.58	0.87
D_nnp2	1.39×10^{-10}	2053	2.64×10^{13}	0.67	0.78

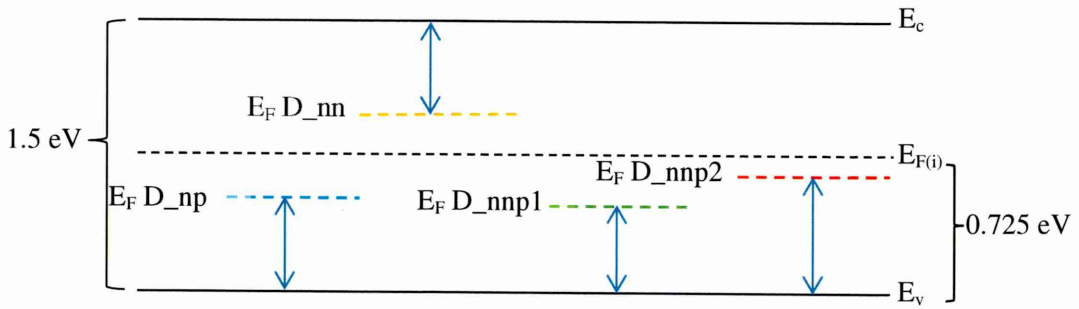


Figure 7.53: The diagram of the Fermi-level position for the measured devices.

7.2 Incorporation of PAni thin films in CdS/CdTe solar cells

In the first part of this section, a set of solar cells was fabricated using PAni as a buffer and pinhole plugging layers with a device structure of glass/FTO/PAni/CdS/CdTe/Au and glass/FTO/CdS/CdTe/PAni/Au, respectively. The conditions of growth and treatment for CdS and CdTe layers were maintained constant throughout this work for effective comparison. Further optimisation of the thicknesses of the PAni layers has been presented in the second part of this work.

7.2.1 The effect of PAni thin films as buffer and pinhole plugging layers in solar cells

On the basis of the study of PAni thin films in the previous chapter, it is suggested that a PAni thin film grown by anodic deposition be used as a buffer layer since it has a wide bandgap (~3.90–4.08 eV) and the cementing effect in the first 20 minutes of deposition, whereas PAni grown by cathodic deposition at a pH of 5.00 has been suggested for use as pinhole plugging layer, since it has a very small and uniform grain size, which can plug the pinholes and helps in filling the gaps. It also has a higher resistivity which helps in creating the MIS device structure. PAni grown by anodic deposition will be referred to as PAni(A), while PAni grown by cathodic deposition in this work will be referred to as PAni(C) in this section. The device measurements under dark and AM 1.5 light are shown in Table 7.12, and the best device measured in this study is shown in Figure 7.14.

Table 7.12: The details of the cell parameters measured for the devices incorporating PAni thin films as buffer and pinhole plugging layers.

Device structure	V_{oc} (mV)	J_{sc} (mA cm^{-2})	$FF(\%)$	η (%)	R_s	R_{sh}
CdS/CdTe	416	16.5	0.36	2.5	425	1848
PAni(A)/CdS/CdTe	-	-	-	-	-	-
PAni(C)/CdS/CdTe	491	8.0	0.26	1.0	2035	2155
CdS/CdTe/PAni (A)	639	15.8	0.42	4.2	493	1825
CdS/CdTe/PAni (C)	521	10.3	0.31	1.7	689	5224

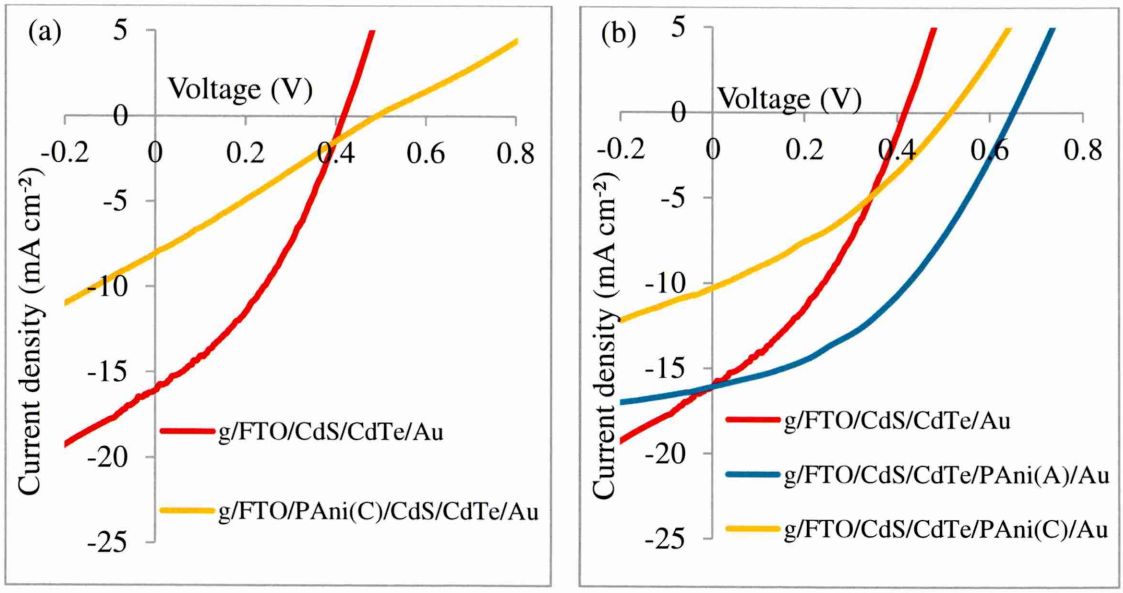


Figure 7.64: The J-V characteristic of the solar cell device using PAni as (a) buffer layer and (b) pinhole plugging layer grown from anodic and cathodic depositions.

The dash value in the Table 7.12 represents the non-surviving device which cracked and peeled during the treatment process. The experiment was repeated three times and the same happened. This was due to the nature of the PAni layer grown by anodic deposition, which makes it sensitive at high temperature. The fabrication of the device based on the CdS/CdTe device required two treatments at temperatures of at least ~400°C for the CdS film and ~420°C for the CdTe film. Despite the decision to incorporate the PAni grown by anodic deposition as a buffer layer, only the device using PAni grown by cathodic deposition survived. However, the efficiency is much lower than for the device grown without the buffer layer. One of the reasons could be the deterioration caused by the two treatments, as mentioned before, and another reason is that a PAni layer grown by anodic deposition has a narrow bandgap (~1.05 to 1.20

eV). A narrow bandgap buffer layer is unhealthy since it limits the photocurrent through the entire solar cell, leading to a drop in all device parameters, especially the J_{sc}. Also, this work shows that organic PAni layer does not provide a good base for inorganic semiconductor to grow well, in order to produce better devices.

The effect of PAni as a pinhole plugging layer has been performed and the summary of the J-V measurements under AM 1.5 illumination for the device with pinhole plugging PAni grown by anodic and cathodic depositions are shown in Table 7.12 and Figure 7.14 (b). The band diagrams of these devices are shown in Figure 7.15. The result of using PAni grown by anodic deposition as the pinhole plugging layer demonstrated better performance and improvement of all three device parameters compared to PAni grown by cathodic deposition. The main improvement was in the V_{oc} (53.6%) and *FF* (16.7%). This result is slightly different from what is being expected. PAni grown by cathodic deposition has been suggested as a pinhole plugging layer due to its narrow bandgap and smaller grain size; however, the cementing effect of PAni grown by anodic deposition seems to do a better job at plugging all the pinholes. In addition, the advantage of having a larger bandgap at the back contact is actually good, since it helps to increase the barrier height and enhances the V_{oc}, as shown in Figure 7.15. However, a proper study of the layer is compulsory, since the large bandgap of the pinhole plugging layer with n-type conductivity might not be helpful, since it may create hole blocking layer at the back contact. In this case, the PAni layer should have p-type conductivity. But the PEC measurement does not show any change in voltage reading, and therefore it is considered that PAni layers as insulating rather than metallic. The V_{oc} improvement may also be caused by the formation of an MIS type electrical contact. Deposition of ultra-thin insulating PAni between the n-CdTe and Au creates an MIS type structure at the back contact and therefore it can increase the potential barrier height enhancing the V_{oc}.

From the I-V curves it is evident that the shunt resistance has increased due to pinhole plugging, and hence the largest improvement appeared in the *FF*, and the increase in J_{sc} is due to the reduced leakage. Ideally, PAni should have insulating properties to completely plug the pinholes and leave a thin film on the CdTe. This layer plugs all other conducting paths in the device and contributes to the increase in the shunt resistance (leakage resistance) and thus improves the shape of the I-V curve and hence the *FF* of the device [35]. The efficiency of the n-CdS/n-CdTe solar cell improves from 2.5% to 4.2% with the insertion of PAni, thus clearly showing the

positive effect of the PAni layer in this work. However, achieving successful pinhole plugging and effective MIS structures simultaneously could be challenging, but the use of semi-insulating layers solves this issue to a certain level [28]. The resistivity of PAni at ~10^6 Ω cm lies in the semi-insulating region and therefore could work well in device structures. In addition to enhancing all these device parameters, MIS type devices have an added advantage. The decoupling of the electrical contact (Au) from the absorber material (CdTe) reduces all interface interactions and hence improves the lifetime of the solar cells [32, 36].

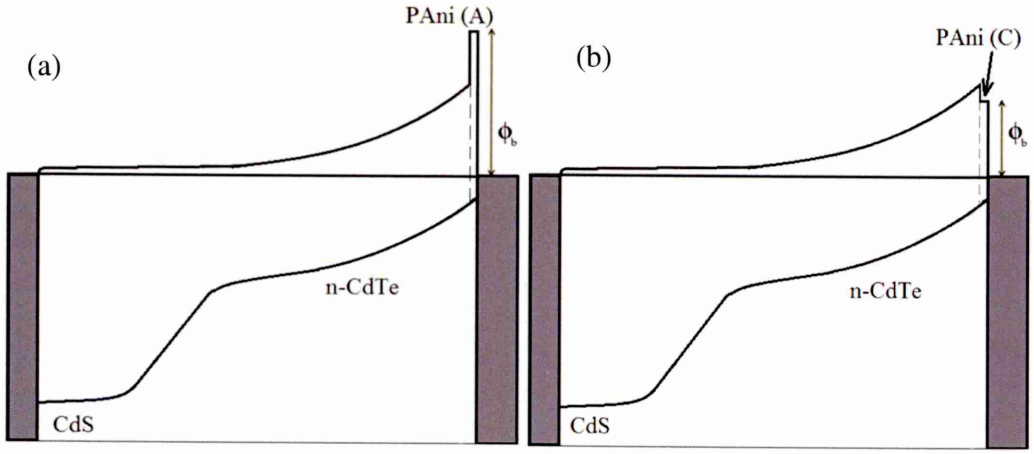


Figure 7.75: The band diagram of the device using PAni as a pinhole plugging layer grown by (a) anodic and (b) cathodic depositions.

7.2.2 The effect of thickness of the PAni thin film as a pinhole plugging layer in solar cells

The treated structure of g/FTO/CdS/CdTe with minor pinhole appearance was selected in this experiment. The purpose of this experiment was to study the effect of thickness of PAni layers as pinhole plugging layers. The solar cell device was cut into five with the dimensions of ~1×1 cm^2. One of the samples was set aside as the reference sample, and the other four samples were deposited with PAni layers for 2 to 15 minutes. All the PAni layers used in this study were grown by applying an anodic potential. The devices were then deposited with Au for a metal back contact and tested with I-V measurements. The data and graphs under illumination are shown in Table 7.13 and Figure 7.16. The thickness value was calculated using the deposition rate (20.3 nm per minute), as discussed in Section 6.1.4.

Table 7.13: Summary of glass/FTO/CdS/CdTe/PAni(C)/Au solar cells fabricated with a variety of thicknesses of PAni layers. Note that the thickness was estimated by using the deposition rate measured by optical profilometry, as discussed in Section 6.1.4.

								Percentage improvement (%)			
Device structure	PAni thickness (nm)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF (%)	η (%)	R_s	R_{sh}	V_{oc}	J_{sc}	FF	η
CdS/CdTe (reference sample)	-	392	16.3	0.37	2.4	362	1583	-	-	-	-
CdS/CdTe/ PAni (2 min)	41	497	16.0	0.39	3.1	476	2395	27	-2	5	29
CdS/CdTe/ PAni (4 min)	81	692	15.8	0.38	4.2	492	7419	77	-3	3	73
CdS/CdTe/ PAni (8 min)	162	414	11.7	0.30	1.5	834	1080	6	-28	-19	-38
CdS/CdTe/ PAni (15 min)	305	632	5.64	0.23	0.8	3518	3726	16	-31	-3	-21

The results in Table 7.13 clearly show that the V_{oc} in all devices improved, as all the devices' pinholes were filled with a plugging layer. As discussed before, the insertion of a semi-insulating layer at the back contact creates the MIS structure, which improved the barrier height and V_{oc} of the solar cell device. The J_{sc}, however, reduced gradually as the thickness of the PAni increased. The fill factor also showed an improvement as the thickness of the pinhole plugging layer increased up to 41 nm, but it reduced slightly at 81 nm and further declined with thicker PAni layers. The best thickness for the pinhole plugging layer is ~81 nm. Above that, the thick PAni layers introduce series resistance at the back contact and thus reducing the carrier collection and the J_{sc} value. The idea in this work is to fill the pinholes with insulating material; but if the insulating layer is too thick, it will increase the series resistance of the device, which diminishes the cell's efficiency. This is the main reason why devices with 162 nm (8 min PAni) and 305 nm (15 min PAni) demonstrate very high R_s of 834 Ω and 3518 Ω, respectively, and all device parameters except V_{oc} deteriorate.

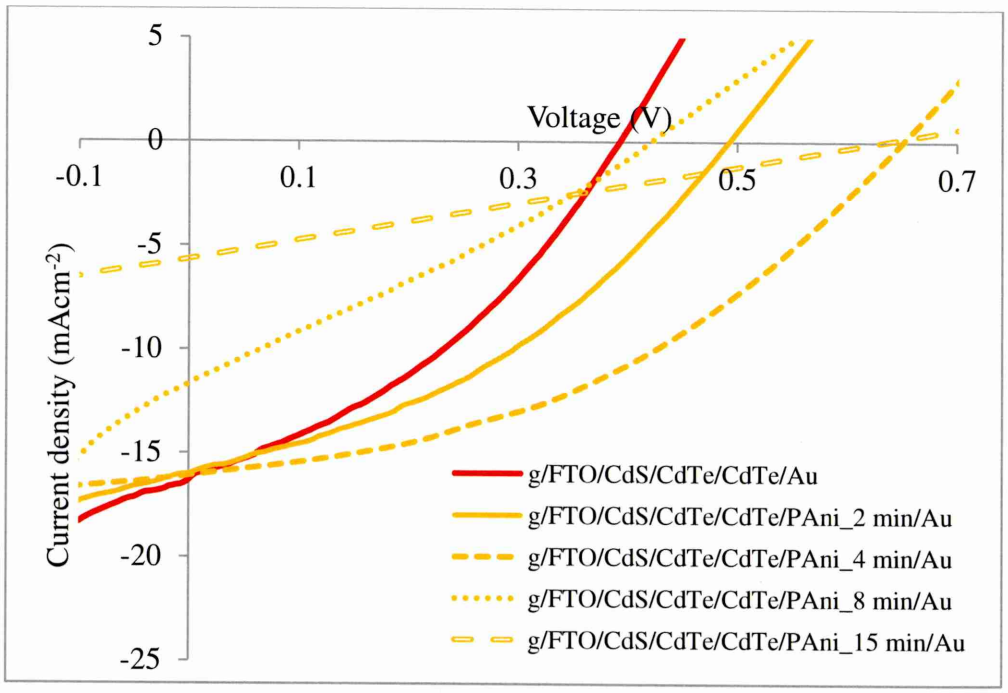


Figure 7.86: The J-V characteristics of solar cells fabricated with a variety of thicknesses of PAni layers grown by cathodic deposition.

7.3 Development of solar cell devices with other device structures

7.3.1 Incorporation of ZnS and CdSe as buffer and/or window layers in solar cells

In this section, the effect of ZnS and CdSe as buffer layers in typical solar cell devices have been studied. These materials have been developed by other researchers in Solar Energy Group, Sheffield Hallam University. The reason why the ZnS was used as a buffer layer is its wider energy bandgap which will allow more photon energy in the solar spectrum to generate more electron hole pairs. In fact, a high J_{sc} has been observed by employing ZnS as a buffer layer in CdTe solar cells [37].

The unique wetting property of CdSe on the g/FTO substrate and the ability to grow uniformly within a very short period of time are the main reasons for the attempt to use CdSe as a buffer layer [38]. A thin layer of ZnS and CdSe have wide bandgaps of 3.70 and 2.50 eV respectively, and n-conductivity type and high transmittance properties at appropriate thicknesses [37, 38]. In this experiment, five sets of samples with typical CdS/CdTe, ZnS/CdTe, ZnS/CdS/CdTe, CdSe/CdTe and CdSe/CdS/CdTe layers were prepared. The results of device measurements are shown in Table 7.14.

Table 7.14: The device parameters under illumination for solar cells with variety of device structures.

Sample ID	Measurement					Average			
	No.	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)
CdS/CdTe	1	462	14.1	0.34	2.2	455	13.0	0.34	2.0
	2	448	11.8	0.33	1.7				
ZnS/CdTe	1	199	2.2	0.25	0.1	192	1.7	0.25	0.1
	2	239	1.7	0.25	0.1				
	3	138	1.3	0.24	0.0				
ZnS/CdS/ CdTe	1	552	16.2	0.36	3.2	549	16.7	0.36	3.2
	2	525	17.1	0.35	3.1				
	3	569	16.7	0.35	3.3				
CdSe/CdTe	1	301	3.3	0.26	0.3	295	2.8	0.25	0.2
	2	284	2.2	0.25	0.2				
	3	300	2.8	0.25	0.2				
CdSe/CdS/ CdTe	1	408	7.2	0.26	0.8	426	6.1	0.25	0.7
	2	418	5.9	0.25	0.6				
	3	453	5.2	0.24	0.6				

The solar cell parameters observed in Table 7.14 show that the attempt to use ZnS as a window layer with the ZnS/CdTe structure is unsuccessful. This could be because the lattice is mismatched between the ZnS and CdTe layers, which results in poor interfaces, and creation of defects and strain in the films. The lattice mismatch of CdS/CdTe is ~10% while the lattice mismatch of ZnS/CdTe is ~16% [39, 40, 41]. As a result, the ZnS/CdTe base solar cell has a low efficiency since the quality of the electrical properties of the heterojunction strongly depends on the performance of the interface and lattice mismatch between the two materials [41]. The performance of these heterojunctions can be improved by adding CdS between the ZnS and CdTe. In this case, ZnS functions as a buffer layer while CdS functions as a window layer, giving a graded-bandgap solar cell with the structure of ZnS/CdS/CdTe. This device shows improvements in all device parameters, including V_{oc} and J_{sc}. The formation of the graded-bandgap structure of ZnS/CdS/CdTe contributes to a high J_{sc} through the impurity PV effect and impact ionisation, as illustrated in Figure 7.18 [29]. The impurity PV effect is the generation of an electron hole pair, using the multi-step photon absorption process, due to the defects and the presence of a strong built-in electric field

in a graded-bandgap solar cell, while impact ionisation is band-to-band electron promotion due to the high kinetic energy electrons and the decrease in the bandgap structure across the device [29]. In fact, the wide bandgap of the ZnS buffer layer makes it possible for more high-energy photons to reach the CdTe absorber layer. The device also produced higher *FF* than others due to the reduction in series resistance.

It is observed that both of the devices incorporating CdSe either as a window layer or buffer layer have considerably low efficiencies. The formation of pinholes observed by Olusola et al. in their CdSe layer after annealing at 385°C may be one of the reasons that the V_{oc} and *FF* of these device are low [38]. The fact that the fabrication of CdTe solar cells required treatments at a temperature of at least 400°C to activate the CdTe properties may worsen the CdSe layer. The device with the graded-bandgap CdSe buffer layer (CdSe/CdS/CdTe) produces a slightly higher V_{oc} and J_{sc} than the CdSe/CdTe devices as a result of its large barrier height and graded bandgap structure. Overall, both devices incorporating a CdSe layer either as a buffer or window layer show low efficiency which may be caused by the non-optimised CdSe layer used in this experiment or by the fact that it is actually not suitable to be used as a buffer and window layer. Further study on this matter should be done to confirm this statement. The best cell for this experiment is the ZnS/CdS/CdTe solar cell with 3.2%.

Further study on the thickness of ZnS in the ZnS/CdS/CdTe structure has been carried out in the following experiment. Table 7.15 and Figure 7.17 show the characteristic of solar cells behaviour under illumination. The J-V characteristics in the two graphs show that the device with a thinner ZnS layer is obviously better than one with a thicker buffer layer. Increased ZnS thickness reduced electrical conductivity, transmittance and increased absorbance, thus all the parameters deteriorated, including V_{oc}, J_{sc} and *FF*. Overall, all the devices measured low due to the non-optimised ZnS and CdSe layers. However, a trend showing improvement when a ZnS buffer layer is inserted has been clearly observed. In conclusion, the better cell for this experiment is cell no. 2 with a 100 nm ZnS buffer layer and efficiency of 3.4%. Even though the efficiency of all devices is still poor, the trend is there and further optimisation of all aspects, including each of the layers, lattice mismatch and thickness should be carried out to enhance their performance.

Table 7.15: The summary of the device results for g/FTO/ZnS/CdS/CdTe/Au with different thicknesses of the ZnS layer.

Sample ID	Measurement					Average			
	No.	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF*	η (%)
ZnS (100 nm) /CdS/CdTe	1	419	18.1	0.34	2.6	450	18.0	0.37	3.0
	2	473	18.2	0.39	3.4				
	3	457	17.8	0.37	3.0				
ZnS (200 nm) /CdS/CdTe	1	241	11.4	0.33	0.9	253	10.0	0.29	0.8
	2	236	8.6	0.27	0.5				
	3	282	10.1	0.28	0.8				

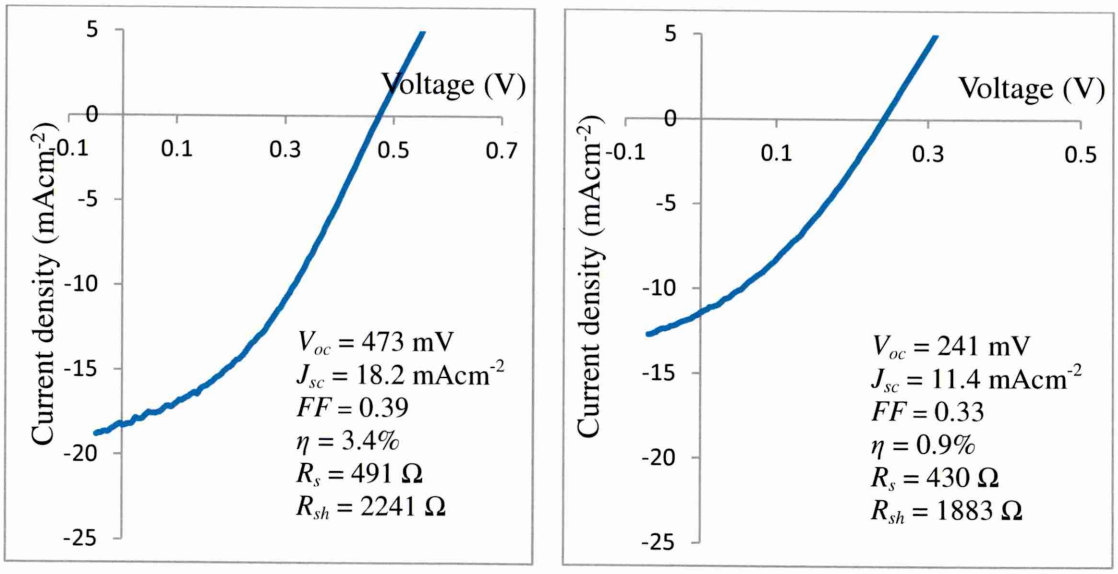


Figure 7.17: The J-V characteristics of g/FTO/ZnS/CdS/CdTe/Au with (a) 100 nm and (b) 200 nm of ZnS layer.

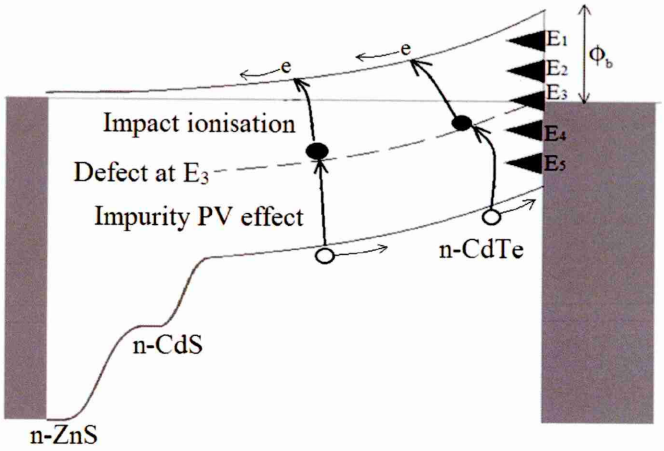


Figure 7.18: The band diagrams of the g/ZnS/CdS/n-CdTe/Au device with the introduction of combined impurity PV effect and impact ionisation.

7.3.2 Incorporation of ZnTe as a capping layer in solar cells

The attempt to use ZnTe as a capping layer in solar cell devices is presented in this section. A capping layer is known as an "etch-stop" layer during the back contact formation process which can reduce the shunting problem. A capping layer should not be too thick to avoid high series resistance. The attempt to use ZnTe in CdTe solar cells has been initiated by Peter Meyers from First Solar [6]. The reasons that a ZnTe layer has been chosen as a capping layer in this study are its semi-insulating properties at room temperature, p-type conductivity, and its high preferential growth along the (111) orientation with a cubic crystal structure, which is perfectly matched with a CdTe layer [42]. Three devices were prepared in this work with the structure of CdS/CdTe, CdS/CdTe/ZnTe (50 nm) and CdS/CdTe/ZnTe (100 nm). The measurement results and J-V characteristics of these devices under illumination are shown in Table 7.16 and Figure 7.19.

Table 7.16: Results of the comparative study of ZnTe capping layers in CdS/CdTe solar cells.

Sample ID	Measurement					Average				R_s*	R_{sh}*
	No.	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF*	η (%)		
CdS/CdTe (ref. sample)	1*	414	15.3	0.40	2.5	405	15.0	0.39	2.4	405	359
	2	409	15.1	0.40	2.5						
	3	392	14.7	0.38	2.2						
CdS/CdTe /ZnTe (50 nm)	1	500	14.2	0.35	2.5	506	15.1	0.36	2.7	671	3461
	2	510	15.2	0.36	2.8						
	3*	507	16.0	0.36	2.9						
CdS/CdTe /ZnTe (100 nm)	1*	512	14.7	0.34	2.6	477	13.0	0.33	2.0	806	3376
	2	438	12.4	0.31	1.7						
	3	480	11.9	0.33	1.9						

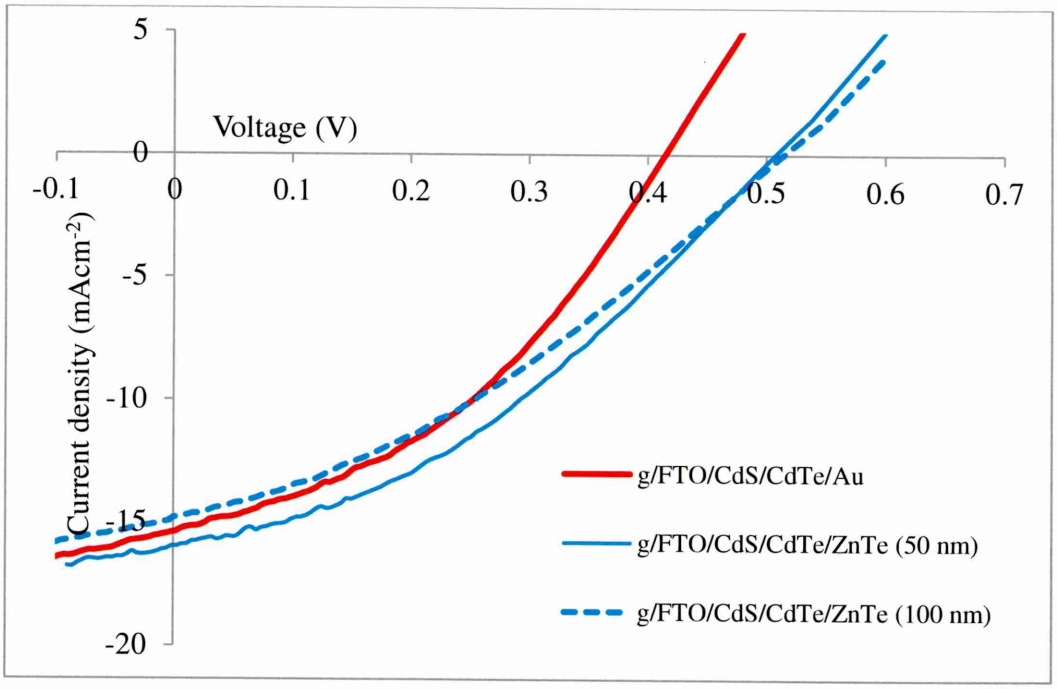


Figure 7.19: The J-V characteristics of CdS/CdTe devices without and with ZnTe capping layers.

It is clearly shown that both devices incorporating ZnTe show improvement in the V_{oc}. ZnTe has a direct bandgap in the range of 2.10 to 2.26 eV, which is higher than that of CdTe [34]. The insertion of ZnTe between n-CdTe and the metal back contact increase the barrier height and results in a higher V_{oc}. In fact, this layer creates the EBDB (electron back diffusion barrier) layer which can prevent electron diffusion to the

back metal contact. The ZnTe layer of higher thickness (~100 nm) can however create a thicker wall for charge carriers to tunnel through. This will then reduce the carrier collection, which results in a high internal resistivity and low J_{sc}. The effect on lower J_{sc} and R_s can be seen in devices using thicker (~100 nm) ZnTe layers. The best efficiency is observed for devices with a 50 nm ZnTe capping layer and the highest efficiency obtained from cell 3 shows 2.9%. Again, the device parameters obtained from this set of experiments are quite low, but the trend from using ZnTe capping layers with two different thicknesses is clearly demonstrated.

7.4 The effect of etching conditions in device fabrication on device performance and study of device lifetime

Further study on the issue has been continued with an investigation into the etching process. In this experiment, the etching process was carried out in different ways. The purpose of this experiment is to study the effect of the traditional etching process used in the lab on solar device performance. At the beginning, a typical solar cell device structure (g/FTO/CdS/CdTe) with the dimension of 4.0×2.0 cm^2 was prepared in this study. The treated sample was cut into four pieces. One of them is purposely set aside without etching, while another three are etched with an acid etchant only, a basic etchant only and both acid and basic etchants, respectively. The details of this procedure are stated in Table 7.17. After chemical etching, all four samples were metallised under similar conditions.

Table 7.17: The details of the etching process organised in this experiment.

Sample ID	Details	Exposure Time, t (sec)	
		Acid etchant	Basic etchant
D_Ref	No etching	-	-
Etch_Normal	Both acid and basic etching	5	120
Etch_B	Only basic etching	-	120
Etch_A	Only acid etching	5	-

Table 7.18 and Figure 7.20 show the detailed measurements under illumination and the comparison of J-V characteristics of the device following different etching procedures. It is clearly seen that the D-Ref device has a low performance in all device parameters. The formation of residues on the CdTe surface after $CdCl_2$ treatment should have to

removed before deposition of Au contacts. Therefore, a suitable etching process is required to remove these unwanted materials and properly produce a good electrical contact to CdTe.

As expected, a typical normal etching process with 5 seconds in acid etchant containing $K_2Cr_2O_7$+H_2SO_4 in 20 ml deionised solution and rinsing prior to 120 seconds (2 minutes) with a basic etchant containing NaOH and $Na_2S_2O_3$ in 50 ml of deionised water improves all device parameters, especially J_{sc}, FF and V_{oc}. This method has been preferably practised for the whole device fabrication in this research programme.

The Etch_B device shows a slight improvement in all device parameters but the improvement is too small compared to the devices etched with an acid etchant. From Table 7.19, it can be seen that the device shows a lower barrier height and results in smaller V_{oc} and FF than Etch_Normal and Etch_A devices. The experiment shows that the basic etching could not completely remove the Te precipitation on the surface and the Fermi-level pinning is located at the upper side of the middle bandgap. This observation is similar to the trend reported by Basol in 1988 [43].

Surprisingly, at least for this set of devices, the Etch_A device shows incredibly high short-circuit current density of 37.4 $mAcm^{-2}$. This is the highest observed in this study. Also, in Table 7.19, it is shown that the ϕ_b is larger than the middle of the bandgap, which indicates that the Fermi-level pinning is at the upper middle band, just above the i-level. It has been reported that etching with acid solution gives a Te-rich surface layer [6, 7]. This device shows slightly different trends, since the barrier height increased, which indicates that the position of the Fermi-level pinning is down from E_2 to E_3 after acid etching. This can be shown in Figure 7.21. This is good since the higher barrier height will increase the V_{oc} and enhance the carrier concentration which raises the J_{sc}. The beneficial effect of acid etching using potassium dichromate has been observed by another research group [44]. It is reported that an acid etchant may lead to the formation of low-resistive Au contacts and increased V_{oc} and FF values [44]. The use of only an acid etchant instead of both an acid and a basic etchant, as is typical, may have an advantage in solar cell production since it can save on costs in terms of chemicals and time for better efficiency. However, further optimisation of this etching study is required to confirm its trend.

Table 7.18: The The device parameters of the solar cells etched following different etching procedures. Note that the best solar cell has been tagged with an asterisk (*).

Sample ID	Measurement					Average				R_s*	R_{sh}*
	No.	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF*	η (%)		
D_Ref	1*	490	8.8	0.26	1.1	489	8.0	0.26	1.0	1895	1980
	2	504	7.3	0.26	1.0						
	3	472	7.9	0.26	1.0						
Etch_ Normal	1	499	20.7	0.29	3.0	467	22.2	0.33	3.4	357	1775
	2*	437	23.9	0.36	3.8						
	3	466	22.0	0.34	3.5						
Etch_B	1	355	19.8	0.32	2.2	361	19.0	0.33	2.3	192	976
	2*	381	20.5	0.37	2.9						
	3	348	16.8	0.31	1.8						
Etch_A	1	382	36.1	0.30	4.1	405	36.7	0.31	4.7	280	819
	2	402	37.4	0.32	4.8						
	3*	431	36.6	0.32	5.1						

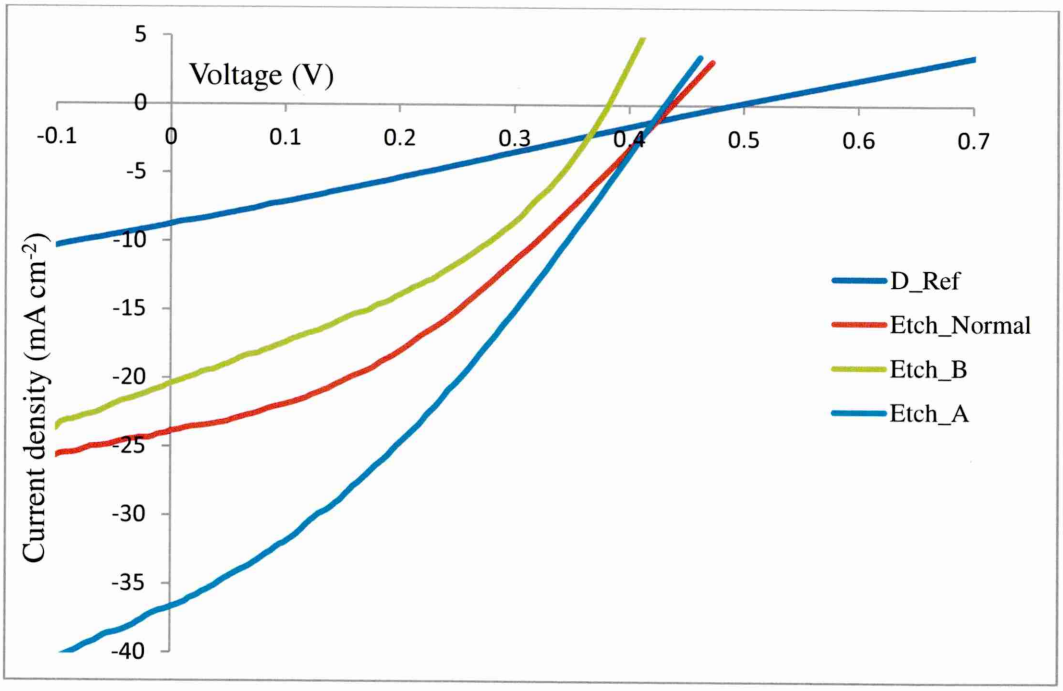


Figure 7.9: The J-V characteristics of the best cell measured in Table 7.18, showing the effect of etching on device characteristics measured under AM 1.5 illumination.

Table 7.19: The device parameters of the best solar cells measured in Table 7.18, observed under AM 1.5 illumination and dark conditions.

Device initial	Device Measurement								
	Dark I-V			Light I-V					
	n	I_o (mA)	ϕ_b (eV)	V_{oc} (V)	J_{sc} (mA cm^{-2})	FF	η (%)	R_s (Ω)	R_{Sh} (Ω)
D_Ref	10.87	1.41×10^{-5}	>0.55	490	8.8	0.26	1.1	1895	1980
Etch_ Normal	6.09	1.00×10^{-6}	>0.62	437	23.9	0.36	3.8	357	1775
Etch_B	7.87	6.17×10^{-6}	>0.58	381	20.5	0.37	2.9	192	976
Etch_A	3.89	6.31×10^{-8}	>0.69	431	36.6	0.32	5.1	280	819

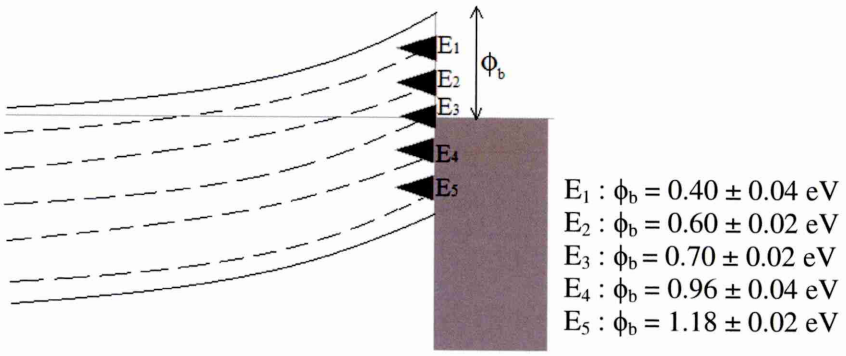


Figure 7.21: The illustration of the position of Fermi-level pinning on a CdTe solar cell [26].

One of the best solar cells obtained from this fabrication work has been monitored for about 1 year to study the stability of the material, lifetime and degradation phenomena of the fabricated solar cell. The average efficiency is obtained from measurement of a few cells in the batch that were recorded from May 2014 to June 2015, which are presented in Figure 7.22. This measurement comes from the device with an n-n-p structure (D_nnp2), which was discussed in section 7.1.3. It is observed that the device maintained more than 83% of its initial efficiency even after 9000 hours. The cell shows a slight improvement from the initial measurement at the initial 10 days followed by a slow decay over time. The improvement is attributed to the improvement in the contact interface between CdTe and the back metal contact after a few days, which brought about better carrier collection and a higher J_{sc}. The device had a maximum average efficiency of 7.6% on day 5. The degradation rate was about 0.1% per month. It is suggested that the degradation of the cell in this experiment is mainly due to the damage to the back contact. Continuous measurements as well as the method of measurement using a small probe damaged some of the cells in this device to some extent (see Figure 7.23). However, Mendoza-Perez observed the degradation of CdTe in

real environment conditions, which was mainly due to the oxidation at the surface, and found that a solar cell with large grains in particular underwent a faster oxidation process [45]. In fact, the shunt resistance also may decrease when metal ions from the back contact diffuse through the cell. In conclusion, a deeper study of the degradation mechanism and how this process of degradation can be slowed down is suggested to focus on the next stage of development.

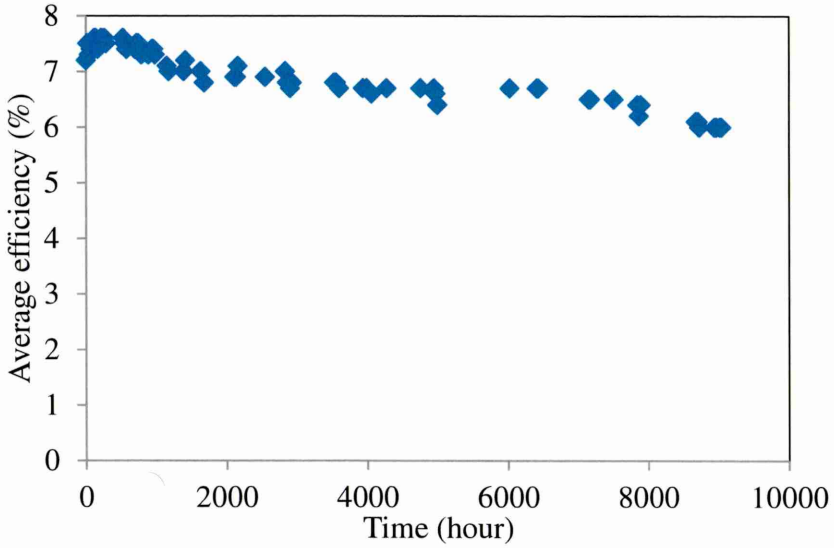


Figure 7.22: The degradation behaviour in the lifetime of device D_nnp2.

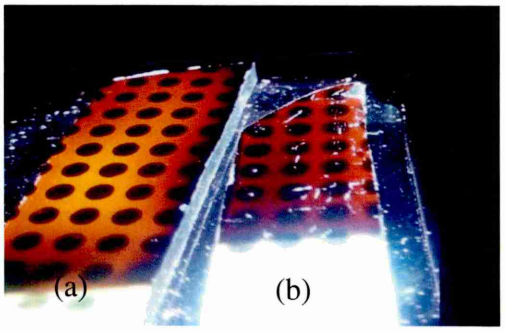


Figure 7.23: The image of the (a) freshly fabricated CdTe solar cell and (b) D_nnp2 solar cell after 1 year of monitoring under light. Note the damages created by repeated measurement using a sharp probe.

7.5 Conclusions

The study on solar cell device performance has been presented in this chapter. The effect of annealing and treatment conditions of CdS layers on device performance

shows that the cells demonstrate greater V_{oc} and efficiency if the window layers are treated at 400°C instead of 450°C. The efficiency of devices increased gradually from CS_AD_400, CS_HT_400, CS_CC_400 to CS_CF_400. The best device obtained is device CS_CF_400 with 5.8%. The effect of annealing temperatures on the untreated CdTe layer and the $CdCl_2$ treated CdTe layer shows that the best device performance is obtained from annealing at 450°C, rather than 385°C and 420°C. However, annealing at 450°C seems too high for devices treated with $CdCl_2$+CdF_2, and so they show a better V_{oc} and the best efficiency at 420°C. Solar cells fabricated using $CdCl_2$+CdF_2+$GaCl_3$ treated CdTe required a lower annealing temperature (~385°C) to activate their performance, but generally all devices treated with $CdCl_2$+CdF_2+$GaCl_3$ show a high J_{sc}. The best cell in this study is device CT_CF_420 with 6.8%. A study on defect and Fermi-level movement for samples with and without $CdCl_2$ treatment has also been carried out in this work. The effect of p- or n-CdTe in the third part of this chapter reveals that the device fabricated using n-CdTe demonstrated better efficiency, predominantly from the high J_{sc} due to the formation of n-n heterojunction and a larger Schottky barrier as well as the high conductivity and the mobility in the n-CdTe layer. The study on the devices which combine n- and p-CdTe to form a graded-bandgap solar cell with n-n-p junctions shows that devices fabricated with thicker n- and thinner p-dTe layers demonstrated excellent diode properties. The highest efficiency cell from this set of experiments gave a measurement of 7.7%. The study on PAni films as buffer layers and pinhole plugging layers demonstrated that PAni grown by anodic deposition does not survive as a buffer layer due to the treatment process at high annealing temperatures for CdS and CdTe layers. The effect of PAni as a pinhole plugging layer shows an improvement in all three device parameters, mainly V_{oc} and FF. The best thickness of pinhole plugging layers is ~81 nm with a 4 minute deposition. Fabrication of devices using other materials shows the possibility of using ZnS as a buffer layer and ZnTe as a capping layer. However, further optimisation of the material properties and thicknesses should be done before applying this material in devices. The study on the etching process demonstrated that the effect of an acid etchant is more prominent than the effect of the basic etchant. The lifetime and degradation measurements in the final section show that after about 1 year of continuous measurements, the device with sample ID:D_nnp2 starts to degrade slowly. This could be due to a physical scratch, oxidation, and diffusion of metal ions through the semiconductor materials or other lifetime issues. The device, however, maintained more than 83% of its initial efficiency after 9000

hours. This slow degradation can be slowed down or removed using ZnTe or PAni type additional layers incorporating in the device structure. Further experiments on all aspects, including materials, treatment, device architecture, etching process, degradation, repeatability, and other issues of device fabrication should be explored more in order to produce high-efficiency solar cells perpetually.

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Chapter 8 - Conclusions and future work

8.0 Intoduction

This chapter presents the general conclusion on the research work and experimental results. The challenges encountered during the work and suggestions for future work are also presented here.

8.1 General conclusions

The aim of this work is to develop low-cost solar cell based on CdTe. The research work covered a wide area of studies from electrochemistry, material science, device physics and PV active devices. Generally, this research can be divided into four stages, which are electrodeposition of thin films, materials characterisation, device fabrication and device measurements and development.

The thesis starts with the electrodeposition and characterisation of CdS thin films. The electrodeposition of CdS thin films aqueous electrolyte bath containing $CdCl_2$ and using $(NH_4)_2S_2O_3$ as sulphur source have been reported. The effects of growth voltages, growth temperature, annealing condition, chemical treatments and sulphur concentration in the electrolytes have been studied systematically. The best V_g of CdS deposition is 1455 mV at temperature 85°C using a two electrode system. Annealing is a vital step to obtain a high quality of CdS. The optimum annealing condition and chemical treatment is at 400°C for 20 minutes, treated with $CdCl_2$+CdF_2. The study on sulphur concentration in the electrolytes suggests that the suitable S/Cd concentration ratio of electrolyte is between 0.2 and 0.5.

A systematically studied of CdTe thin films grown from $CdCl_2$ precursor have been first time reported in Chapter 5. CdTe films have been successfully grown by electrodeposition from an aqueous electrolyte bath containing $CdCl_2 \cdot H_2O$ and TeO_2. The CdTe thin films have been studied in various conditions including growth voltages, annealing conditions and chemical treatments. This work has demonstrated better understanding and clues on the effect of $CdCl_2$ treatment. ED shows the possibility of growing p-, i- and n-type CdTe. The n-type CdTe near the stoichiometric region shows excellent properties of material. The best V_g was obtained at 698 mV in a three electrode system, with respect to calomel electrode. The optimum annealing temperature lies between 420 °C, 20 minutes and 450°C, 15 minutes in the presence of $CdCl_2$+CdF_2 or $CdCl_2$+CdF_2+$GaCl_3$. This work has given better understanding on the material issues and some clues on the effect of $CdCl_2$ treatment.

PAni thin films have been electrodeposited from anodic and cathodic deposition. The pernigraniline salt PAni grown from anodic has an amorphous structure, large bandgap and cementing growth effect. The leucoemeraldine salt PAni grown from cathodic deposition shows the best crystallinity at V_g=1654 mV, smaller grain size, higher resistivity and lower bandgap. However, both PAni layers show degradation with annealing process.

The application of CdS as a window layer has been studied in the form of solar cell device performance. The effect of annealing seems to be more prominent than the chemical treatment. Solar cells demonstrate better V_{oc} when the CdS layer was treated at 400°C instead of 450°C. The best device is obtained with CdS thin films treated with $CdCl_2$+CdF_2 at 400°C with efficiency of 5.8%. The application of CdTe as an absorber layer has been studied and it was observed that the effect of annealing temperature depends on the chemical treatment. CdTe treated with $CdCl_2$ for instance, shows the best performance when annealed at 450°C, but a device treated with $CdCl_2$+CdF_2 and $CdCl_2$+CdF_2+$GaCl_3$ shows better efficiency at temperatures of 420 and 385°C, respectively. The best cell from this study is a device treated with $CdCl_2$+CdF_2 at 420°C with efficiency of 6.8%. The study on the solar cell device performance with n- or p-CdTe demonstrates that a device with n-CdTe shows high J_{sc} due to the formation of n-n heterojunction and a large Schottky barrier as well as high conductivity and mobility in n-CdTe layer. The combination of 1200 nm thickness of n- and 300 nm of p- CdTe demonstrated the highest efficiency with 7.7% efficiency.

It is expected from the characterisation study that the PAni grown from anodic (pernigraniline) is suitable for a buffer layer due to the amorphous structure, large bandgap and cementing growth effect characteristics. However, the layer did not survive during the heat treatment process of CdS and CdTe films. The use of PAni grown from anodic deposition as a plugging layer shows better improvement than PAni grown from cathodic deposition due to the cementing growth nature, larger bandgap and MIS type structure which had plugging for all the pinholes, increased the barrier height and enhanced the V_{oc} and FF. The best thickness for the pinholes plugging layer is ~81 nm with 4 minute deposition. This work has demonstrated the potential of improving the solar cell performance through pinhole pluggin layer.

The fabrication of a device using other materials shows the possibility of using n-ZnS as a buffer layer and p-ZnTe as a capping layer but further optimisation on these materials should be done before applying them in device structure. Proper study on etching process should be undertaken in future. The study on the lifetime of a solar cell

device grown from the combination of 1200 nm thickness of n- and 300 nm of p- CdTe shows slow degradation. The device maintained more than 83% of its initial efficiency after 9000 hours. From this research, it is understood that many factors should be taken into account including the materials, treatments, annealing, device architectures and etching process together with defect elimination in solar cell fabrication in order to produce high efficiency, stable and long life solar cell devices.

8.2 Challenges encountered in this work

The general solar cells fabricated in this research work have several issues that limit the cell efficiency. The main challenge encountered in this work is to produce high efficiency. The following discussion explains why high efficiency is difficult to achieve in this work.

The most difficulty encountered in this work is to maintain the quality of the film from one deposition batch to another. This is associated with the reproducibility and the quality of the eletrodeposited layer [1-2]. Although all parameters including pH, temperature, stirring rate, volume of the electrolyte, growth potential and growth current density have been maintained at the same level as the initial deposition, the concentration of the electrolyte actually changes with deposition. For instance, in CdS and CdTe depositions the amount of constituent ions, which is known at the beginning of the electrodeposition, becomes uncertain after performing several depositions.

It is known that as the deposition starts, these ions are gradually reduced in the electrolyte [2]. The systematic addition of these ionic species from prepared feedstock of separated prepared electrolyte has been practised through the research work. However, the concentration of the electrolyte after the addition of these feedstock ions is still unknown; hence, it becomes the un-known factor in this work. The material properties grown when the electrolyte was initially made is differ after several batches of deposition. Therefore, even though the materials have been fully optimised in the first phase of the research programme, the properties of the materials could be different when we apply them in the device fabrication. This actually seriously affects the reproducibility of the films and consequently disrupts the quality of the solar cell that is fabricated from them.

Achieving a uniform layer with larger grains, dense and pinholes free thin films has been identified as one of the challenges in thin film device work. Although the SEM image of the chemical treated films shows an improvement in grain size, the development of pinholes is formed concurrently in certain layers [3].

Another challenge of this work is that it requires longer deposition time and there is a risk of peeling off. Although the electrodeposition technique sounds simple compared to other deposition techniques, it needs a long time to produce the required layer, in particular CdTe deposition. It took at least four hours to deposit ~1.5 μm of CdTe thin film. The risk of peeling-off is also very high, especially in the last hour of deposition. Therefore, it required consistent monitoring during four hours of deposition. If the film peels off, it will destroy the whole structure including the CdS and/or buffer layer deposited underneath of the CdTe layer. This therefore has wasted the cost of the fabrication process including the growth time taken to prepare the CdS and/or buffer layer and the chemicals used during the fabrication.

8.3 Suggestions for future work

Several suggestions are proposed below in order to improve the experimental work and to produce the device with better efficiency and reproducibility in addition to the review for the next generation of solar cells.

8.3.1 Monitoring the concentration of the electrolyte

Controlling the concentration and ion balance in the electrolyte during the deposition can be achieved by several methods. First, the installation of the automated pump is needed to feed the electrolyte with feedstock ions periodically. For instance, the approximate amount of prepared Cd^{2+}, Te^{4+} or S^{2-} ion is added into the electrolyte for each hour of the deposition. However, this work needs proper calibration at the beginning to sustain the ions addition with the ions lost during the deposition.

Another technique is by inventing the electrolyte concentration analyser to measure the concentration of elements or ions in the electrolyte. Some of the manufacturers such as EasyLyte, Lab-Kits and Labcompare have invented equipment to measure the concentration of elements and ions such as Na^+, K^+, Cl^-, Li^+, Ca^+, F^- and bicarbonate (HCO_3) concentrations in numerous types of electrolyte sample for application in lab and biomedical contexts [4, 5, 6]. The invention of the electrolyte analyser similar to that mentioned, with the ability to measure the Cd^{2+}, Te^{4+} or S^{2-} concentrations, could be an effective solution to maintain the electrolyte concentration in electrodeposition.

The final suggestion is an alternative way of checking the concentration in the electrolytes. This can be done by conducting the EDX or XRF measurements on the electrodeposited films prior to the fabrication process in order to confirm the

concentration of the electrolytes. This, therefore, can maintain the quality and reproducibility of the films used in the solar cell devices.

8.3.2 Comparative study of PAni layers and lifetime issue.

The improvement of all three parameters of solar cells by incorporating a PAni thin film as a pinhole plugging layer was proven in this work. In addition, it is suggested to study the unique properties of PAni material and explore the benefits of this layer in solar cell devices since PAni has also been identified as a hole-transport medium in dye-sensitised solar cells (DSSCs) [7]. The stability over a period of time should also be monitored in order to investigate the lifetime issue of devices incorporating PAni films.

8.3.3 Replace the glass/FTO with more suitable substrate.

The substrate can actually affect the performance of the solar cell. It should have low electrical resistance, high optical transmittance and high photoelectrical response in order to produce a good device. The substrate used in this work is based on glass/FTO substrate. The nature of the glass/FTO substrate, with a rough surface and low optical transmittance, could be one of the reasons for low device efficiency [8]. Therefore, it is suggested to replace this substrate with suitable substrate such as glass/indium tin oxide (ITO) since a glass/ITO substrate has less roughness, high optical transmittance and low series resistance [8]. In fact, Das has also observed that the best substrate for solar cell devices is a glass/ITO substrate [9]. But, as mentioned in Section 3.1.1 earlier the cost of ITO substrate is quite expensive even for the high sheet resistance substrate, in addition to the aim of this work is to produce low-cost solar cell device are the reasons why we used FTO in this research work. The use of ITO can be considered if the goal of research is just about to improve the solar cell efficiency without concern in cost of manufacturing.

8.3.4 Graded bandgap solar cells

High efficiency solar cells can be achieved by improving the device architecture of the devices. This can be done by proper designing the device structure with appropriate bandgap and material properties, or by applying graded bandgap solar cell concept. The idea on device architecture in fully graded bandgap solar cell has been designed within the SHU solar energy group in 2002 by the introduction of a third layer in CdS/CdTe solar cells with an intermediate energy bandgap such as CdSe for smoothing of the slope of the energy band diagram and enhancing the carrier collection [10]. This model

explains the device behaviour in terms of a combination of an n-n heterojunction and a large Schottky barrier at the CdTe interface. These ideas were further developed and fully graded device design were published in 2005 [11]. In the same year, the designs were experimentally tested using well researched GaAs/AlGaAs system grown by MOVPE. The solar cells with V_{oc} of ~1175 mV, *FF* of ~0.83-0.87 and J_{sc} of 12 $mAcm^{-2}$ have been observed and 20% efficiency was achieved using only two growth runs [12]. These solar cells are active in complete darkness proving the existence of impurity PV effect within these devices. The devices also showed 140% quantum efficiency demonstrating impact ionisation in the device [12]. Recently, the graded bandgap has been produced using all-electrodeposited semiconductors using n-ZnS, n-CdS and n-CdTe with 12% of efficiency achievement [13].

Graded bandgap solar cells can be fabricated with a wide bandgap material in the front and gradual reduction of the bandgap towards the back contact to absorb all photons from the UV, visible and IR region [14]. A graded bandgap solar cell can also be produced by the insertion of materials with an appropriate bandgap as a buffer layer, intermediate layer and/or capping layer. These structures are capable of enhancing the photo generated charge carriers due to impurity PV effect and impact ionisation. The schematic of a graded bandgap structure with electroplated materials and its band diagram is shown in Figure 8.4.

At present, research at SHU solar energy group is focused on devices based on electroplated materials and the device structure is shown in Figure 8.4. Production of high J_{sc} values from these devices show high potential of graded bandgap devices for next generation solar cells.

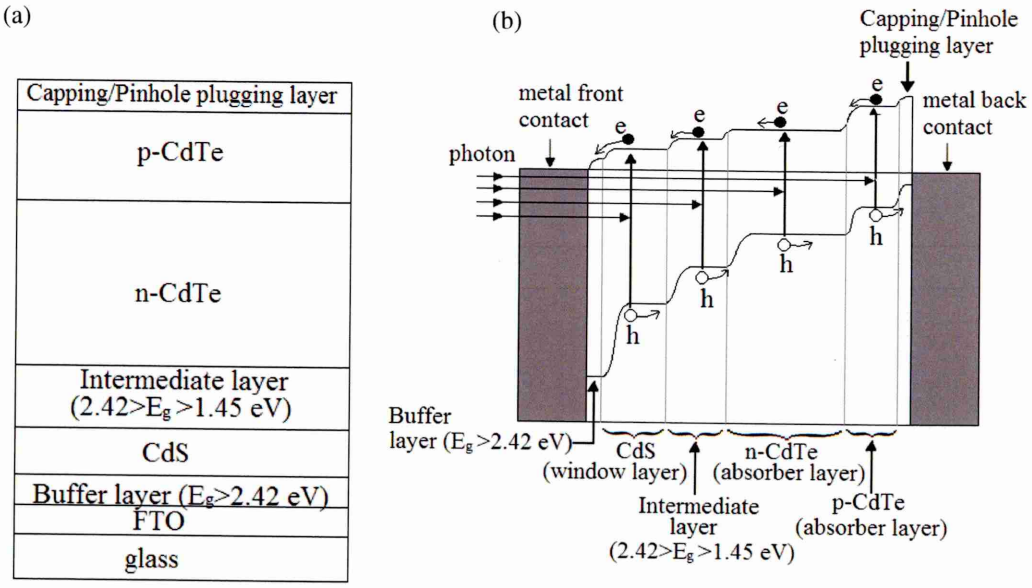

Figure 8.1: Schematic diagram of (a) graded bandgap solar cell structure and (b) energy band diagram of graded bandgap solar cell.

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Appendix

Appendix I: Example of thickness calculation using Faradays's law equation.

Faraday's law:

$$\text{Thickness} = \frac{1}{n\,F\,A} \times \frac{i\,t\,M}{\rho}$$

where n = number of electrons involved in chemical reaction. ($n_{CdTe} = 6$, $n_{CdS} = 8$)

F = Faraday's constant (96485.33 $A \cdot s \cdot mol^{-1}$)

A = Electrodeposited layer

i = Average current growth

t = time

M = Molar mass of material ($M_{CdTe} = 240.01\ g \cdot mol^{-1}$, $M_{CdS} = 144.47\ g \cdot mol^{-1}$)

ρ = density of electrodeposited layer ($\rho_{CdTe} = 5.85\ g \cdot cm^{-3}$, $\rho_{CdS} = 4.29\ g \cdot cm^{-3}$)

In case of electrodeposition of CdTe thin film with current density, $J_g = 150\ \mu A \cdot cm^{-2}$, for 4 hours deposition (14400 s); the thickness can be calculate as:

$$T = \frac{1\,(150 \times 10^{-6})(14400)(240.01)}{6\,(96485.33)(5.85)} \qquad \text{unit} = \frac{mol \cdot A \cdot s \cdot g \cdot cm^3}{A \cdot s \cdot cm^2 \cdot mol \cdot g}$$

$= 1.53 \times 10^{-4}$ cm

$= 1.53 \times 10^{-6}$ m

$= \underline{1.53\ \mu m}$