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Processing of Semiconductors and Thin Film Solar Cells Using Electroplating

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A thesis submitted in partial fulfilment of the requirements of

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Doctor of Philosophy

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Declaration

I hereby declare that the work presented in this thesis is my own work, carried out by me and has not been submitted elsewhere for the award of any degree.

Mohammad Lamido Madugu

Dedication

To the memory of my late uncle, Alhaji Madugu Abubakar for his love and caring, may Allah (S.W.A) have mercy on him.

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List of publications

Journal Publications

1. **M.L. Madugu**, L. Bowen, O.K. Echendu, I.M. Dharmadasa, Preparation of indium selenide thin films by electrochemical technique, J. Mater. Sci. Mater. Electron. 25 (2014) 3977-3983.

2. **M.L. Madugu**, O.I. Olusola, O.K. Echendu, B. Kadem, I.M. Dharmadasa, Intrinsic Doping in Electrodeposited ZnS Thin Films for Application in Large-Area Optoelectronic Devices, J. Eelectron. Mater. (2016).

3. O.I. Olusola, **M.L. Madugu**, I.M. Dharmadasa, Growth of n- and p-type ZnTe semiconductors by intrinsic doping, Mater. Res. Innov. 19 (2015) 497-502.

4. N.A. Abdul-Manaf, H.I. Salim, **M.L. Madugu**, O.I. Olusola, I.M. Dharmadasa, Electroplating and characterisation of CdTe thin films using $CdCl_2$ as the cadmium source, Energies. 8 (2015) 10883-10903.

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6. I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, O.I. Olusola, H.I. Salim, **M.L. Madugu**, A.A. Ojo, Improvement of composition of CdTe thin films during heat treatment in the presence of $CdCl_2$, Submitt. to J. Mater. Sci. Mater. Electron. (2016).

7. A.A. Ojo, H.I. Salim, O.I. Olusola, **M.L. Madugu**, I.M. Dharmadasa, Effect of thickness: A case study of electrodeposited CdS in CdS/CdTe based photovoltaic devices, Submitt. to J. Mater. Sci. Mater. Electron.

8. O.I. Olusola, **M.L. Madugu,** A.A. Ojo, I.M. Dharmadasa, Investigating the effect of $GaCl_3$ incorporation into the usual $CdCl_2$ treatment on CdTe-based solar cell device structures, Curr. Appl. Phys. 17 (2017) 279-289.

9. O.I. Olusola, **M.L. Madugu,** I.M. Dharmadasa, Investigating the electronic properties of multi-junction ZnS/CdS/CdTe graded bandgap solar cells, Submitt. to J. Mater. Chem. and Phys. (2016).

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10. **M.L. Madugu**, P. A. Bingham, H. I. Salim, O. I Olusola and I. M. Dharmadasa, Development of In_xSe_y Buffer Layers for Applications in CdTe Based Thin Film Solar Cells, in: Proc. of 29th European Photovoltaic Solar Energy Conference and Exhibition, Amsterdam, The Netherlands, (2014) pp. 1847-1851. DOI: 10.4229/EUPVSEC20142014-3DV.2.48 (Poster).
11. **M.L. Madugu**, L. Bowen, O.K. Echendu, I.M. Dharmadasa, Characterisation of electrodeposited In_xSe_y for thin film solar cell application, in proc. of PVSAT-10, Loughborough University, UK, (2014), PP 185-188 (Poster).
12. **M.L. Madugu,** I.M. Dharmadasa, Preparation of ZnS thin film for Application in photovoltaic device fabrication, UK Semiconductors, 9-10th July, Sheffield Hallam University, 2014 (Poster).
13. **M.L. Madugu** and I.M. Dharmadasa, Development of CdS/CdTe solar cell using In_xSe_y buffer layer, Material and Engineering Research Institute (MERI) research symposium, May 19-20, 2015, at Sheffield Hallam University, UK. (Oral presentation).
14. **M.L. Madugu, O.I.** Olusola and I.M. Dharmadasa, Electroplating of n-type and p-type ZnS thin films by Intrinsic doping, Photovoltaic Technical Conference (PVTC), "From advance Materials and Processes to Innovative Application, May 27-29, 2015; At Centre de Congrés, Aixen Provence (Oral and Poster presentations).
15. **M.L. Madugu,** I.M. Dharmadasa, The effect of annealing temperature on the structural, optical and and morphological properties of cadmium telluride (CdTe) thin films, UK Semiconductors, 1-2 July, Sheffield Hallam University, 2015 (Poster).
16. O.I. Olusola, **M.L. Madugu**, I.M. Dharmadasa, Development of n- and p-type ZnTe Semiconductors for application in Electronic Devices, UK Semiconductors & UK Nitrides Consortium Summer Meeting, Sheffield, United Kingdom, 1-2 July, 2015, pp. 130 (Poster)
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19. I.M. Dharmadasa, **M.L. Madugu**, O.I. Olusola, O.K. Echendu, F. Fauzi, D.G. Diso, A.R. Weerasinghe, T. Druffel, R. Dharmadasa, B. Lavery, J.B. Jasinski, T.A. Krentsel, G. Sumanasekera, Electroplating of CdTe Thin Films from Cadmium Sulphate Precursor and Comparison of layers grown by 3-electrode and 2-electrode systems, Submitt. to Coatings. (2016).

Abstract

The global need for a clean, sustainable and affordable source of energy has triggered extensive research especially in renewable energy sources. In this sector, photovoltaic has been identified as a cheapest, clean and reliable source of energy. It would be of interest to obtain photovoltaic material in thin film form by using simple and inexpensive semiconductor growth technique such as electroplating. Using this growth technique, four semiconductor materials were electroplated on glass/fluorine-doped tin oxide (FTO) substrate from aqueous electrolytes. These semiconductors are indium selenide (In_xSe_y), zinc sulphide (ZnS), cadmium sulphide (CdS) and cadmium telluride (CdTe). In_xSe_y and ZnS were incorporated as buffer layers while CdS and CdTe layers were utilised as window and absorber layers respectively. All materials were grown using two-electrode (2E) system except for CdTe which was grown using 3E and 2E systems for comparison. To fully optimise the growth conditions, the as-deposited and annealed layers from all the materials were characterised for their structural, morphological, optical, electrical and defects structures using X-ray diffraction (XRD), Raman spectroscopy, scanning electron microscopy (SEM), atomic force microscopy (AFM), optical absorption (UV-Vis spectroscopy), photoelectrochemical (PEC) cell measurements, current-voltage (I-V), capacitance-voltage (C-V), DC electrical measurements, ultraviolet photoelectron spectroscopy (UPS) and photoluminescence (PL) techniques. Results show that In_xSe_y and ZnS layers were amorphous in nature and exhibit both n-type and p-type in electrical conduction. CdS layers are n-type in electrical conduction and show hexagonal and cubic phases in both the as-deposited and after annealing process. CdTe layers show cubic phase structure with both n-type and p-type in electrical conduction. CdTe-based solar cell structures with a n-n heterojunction plus large Schottky barrier, as well as multi-layer graded bandgap solar cells were fabricated. This means that the solar cells investigated in this thesis were not the conventional p-n junction type solar cells. The conventional cadmium chloride ($CdCl_2$ or CC) treatment was applied to the structures to produce high performance devices; however, by modifying the treatment to include cadmium chloride and cadmium fluoride ($CdCl_2$+CdF_2 or CF) device performance could be improved further. The fabricated devices were characterised using I-V and C-V measurement techniques. The highest cell efficiency achieved in this research was ~10%, with an open circuit voltage of 640 mV, short-circuit current density of 38.1 $mAcm^{-2}$, fill factor of 0.41 and doping concentration of 2.07×10^{16} cm^{-3}. These parameters were obtained for the glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cell structure.

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Abbreviations and Symbols

Abbreviations

A	Area
AFM	Atomic force microscopy
Ag/AgCl2	Silver/silver chloride
AM1.5	Air Mass 1.5
Au	Gold
BP	British Petroleum
CBD	Chemical bath deposition
CdO	Cadmium oxide
CdS	Cadmium sulphide
CdTe	Cadmium telluride
Cl	Chlorine
CuInGaSe2	Copper indium gallium diselenide
CSS	Closed space sublimation
C-V	Capacitance voltage
CVD	Chemical vapour deposition
ED	Electrodeposition
FF	Fill factor
FTO	Fluorine-doped tin oxide
FWHM	Full width at half maximum
I_o	Reverse saturation current
In	Indium
ITO	Indium tin oxide
I-V	Current voltage
J_{sc}	Short circuit current density
M	Molar
n	diode ideality factor

NREL	National Renewable Energy Laboratory
PEC	Photoelectrochemical
P_{in}	Input power
R	Resistance
RF	Rectification factor
S	Sulphur
SCE	Saturated calomel electrode
SEM	Scanning electron microscopy
SnO2	Tin oxide
TCO	Transparent conducting oxide
V_{oc}	Open circuit voltage
XRD	X-ray diffraction

Symbols

A*	Effective Richardson constant
e	Magnitude of electronic charge
ε_o	Permittivity of free space
ε_r	Relative permittivity
E_0	Standard reduction potential
F	Faraday's constant
Φ_b	Potential barrier height
Φ_m	Work function of metal
Φ_s	Work function of semiconductor
h	Plank's constant
k	Boltzmann constant
N_A	Acceptor concentration
N_D	Donor concentration
n_i	Intrinsic charge carrier density
ν	Frequency

V_{bi}	Built-in potential
V_i	Intrinsic voltage
σ	Electrical conductivity
ρ	Electrical resistivity

Chapter 1: Introduction

1.1 Global need for renewable energy

It is expected that the world population would increase to 9.6 billion by 2050 from its present 7.4 billion according to the United Nations report [1]. This shows an increase of approximately 35% from 2010 [2]. The main factors favouring population growth includes high fertility rate, low mortality rate, improved health care services, and increase in food production. Consequently, the continued population growth puts more pressure on the limited available energy sources and continues dependency on fossil fuels such coal, petroleum and natural gas for energy. Under this situation, it is important that proactive measures be taken in order to facilitate appropriate laws and new technologies that will help to change the mostly traditional energy sources. These sources of energy are known to be the main suppliers of carbon dioxide (CO_2) and methane which contributes to the global greenhouse gas (GHG) emissions. The increase in the emission of CO_2 causes global warming which was predicted to increase the surface temperature to between 1.4°C and 5.8°C. If not properly checked, it will cause natural disasters such as droughts, floods, sea level rise, glacier melting, interruptions to farming activities and serious damage to the ecosystem [2].

British Petroleum (BP) annual report for 2015 shows that oil consumption stands at 32% for the world total energy consumption followed by coal and natural gas with 30% and 24% respectively. In 2014, fossil fuels accounted for 86% of the total global energy consumption as a result of an annual 2% increase since 2004 [3]. This shows that the remaining 14% was shared among other energy sources, including nuclear and renewables such as hydroelectricity, wind, solar, biofuels, biomass and geothermal. The global energy consumption for the various energy sources for 2015 is shown in Figure 1.1.

The demand for energy mainly comes from lighting, cooling and heating which is mostly dependent on electricity which in turn is sourced majorly from fossil fuels. Increase energy demand will also further escalate the emission of CO_2 which pollutes the environment increasing global warming. The concentration of CO_2 in the atmosphere has continued to rise to approximately 43% since the beginning of the industrial revolution in the mid-eighteenth century. The total concentration of GHG in

the atmosphere rose to 34% between 1990 and 2013, with CO_2 responsible for nearly 80% of that increase [4]. Figure 1.2 shows the annual global CO_2 emission trend for the past fifteen years.

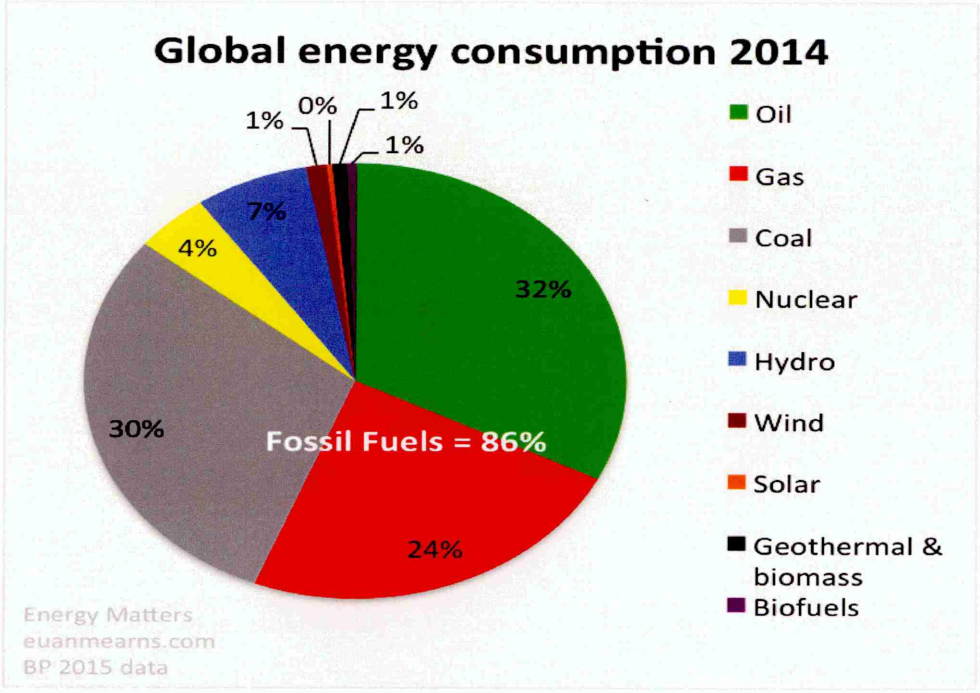

Figure 1-1: BP Statistical Review of World Energy consumption 2014 [3].

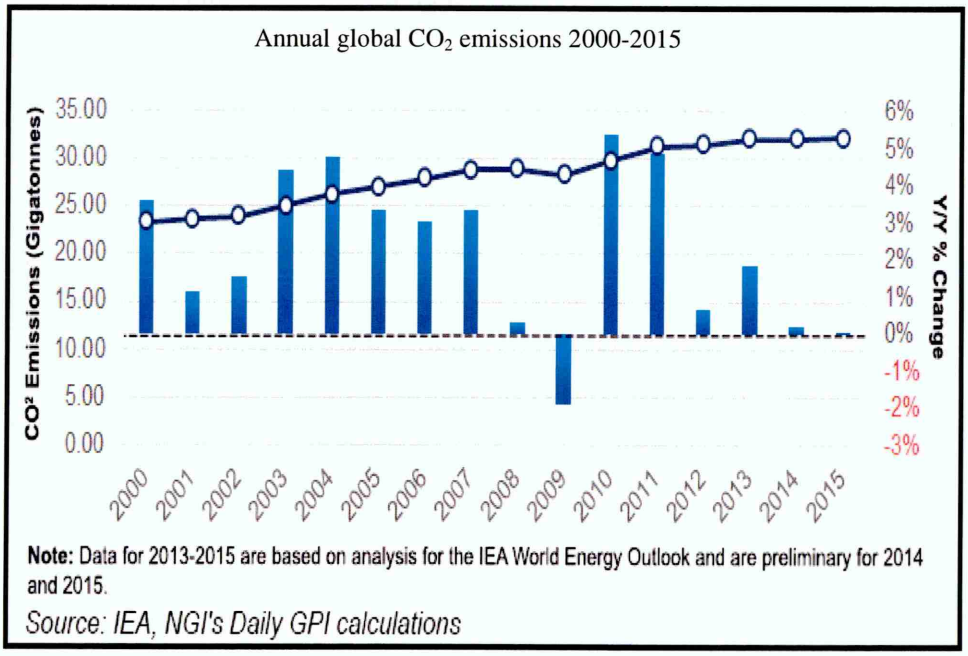

Figure 1-2: Annual Global CO_2 Emission 2000-2015 [5].

At present, China is the largest emitter of CO_2 accounting for approximately one-quarter of total global emissions and is followed by the United States which emits about 18% of the world's GHGs. These two major emitters of CO_2, agreed to the reduction in CO_2 emissions in a meeting on the global emissions agreement held in Paris in 2014. Thereafter, it has been reported by the International Energy Agency [5] that CO_2 emissions in the U.S. decline by 2% which was attributed to shift from coal to natural gas in the generation of electricity. In the same vain, CO_2 emissions in China fell by 1.5% in 2015 due to a drop in the use of coal.

It is observed in Figure 1.2, that CO_2 emissions stood at 32.1 gigatonnes in 2015 and is seen to be flat since 2013. Interestingly, the global economy also grew in parallel by more than 3% during this period which indicates that the hitherto linear relationship between economic growths and the CO_2 emission growth has weakened [5].

In general, the reduction in the effects of global warming can only be achieved by the reduction of CO_2 emission. Apart from the industrial, governmental, non-governmental and civil society's effort in the campaign for the reduction of CO_2, we as individuals can also play our part in our own little way. We can make a difference by taking some steps at home, on the road and in our offices to reduce greenhouse gas emissions and the risk associated with climate change. In fact these measures can as well save us money such as walking or biking to work which can even improve our health. Another way to help reduce GHGs emissions is for one to get involved at the local or state level to support energy efficiency, clean energy and climate programs.

This chapter briefly discussed non-renewable and renewable energy sources and their environmental impact. Renewable energies such as wind, hydroelectric, biomass and solar energy were also briefly presented. Air masses, solar thermal and solar PV were also presented. The last section outlines the aims and objectives of this research programme.

1.2 Non-renewable energy sources

Non-renewable energies are energy sources that can run out one day. These types of energy emit some gases in gas-fired power stations such as oxides of sulphur, carbon and nitrogen into the atmosphere which pollutes the environment [6]. Fossil fuels are

the main sources of non-renewable energies which are the remains of dead plants and animals exposed to heat and pressure in the earth's crust over millions of years.

1.3 Alternative renewable energy sources

These are energy sources that are not from fossil or nuclear fuel such as geothermal, wind, hydroelectric, tidal and solar energy [7]. These energy sources are abundant and can provide more energy than humankind needs and are environmentally friendly. Harnessing energy from renewables provides reliable and sustainable energy source since they are inexhaustible. Renewables such as wind and solar are increasingly playing roles in the economic transformation of many societies through the generation of electricity.

The future should focus more on electricity generation from renewable energies rather than from the fossil fuels which can one day be used up. The cost of renewable energies is coming down and a lot of different technologies are coming in to harness this free and abundant energy. At present, the renewable energy supply accounts for about 20% of the global energy demand. In order to avoid the environmental effect of global warming such as climate change, renewables are the only answer [8].

1.3.1 Wind energy

This is one of the cleanest, safe and free renewable energy sources. Wind is generated as a result of pressure difference between two points or locations. It is the movement of air from an area of high pressure to an area of low pressure. Wind exists due to non-uniformity in the way the sun heats the surface of the earth. As hot air rises, cooler air moves in to fill the vacant space. This form of renewable energy can be used to generate electricity through the conversion of the kinetic energy of the wind to mechanical energy (turbines) and then to electrical. A generator convert the mechanical power into electrical energy. Figure 1.3 schematically shows the stages involved in the conversion of wind energy to electrical energy.

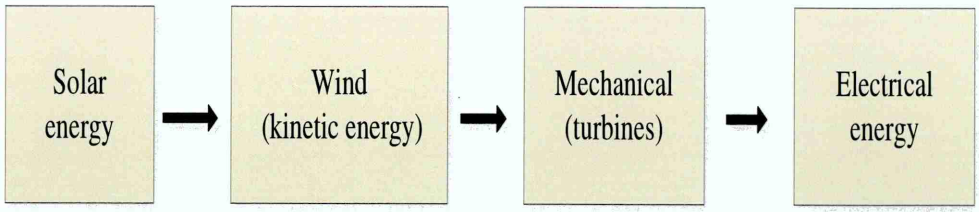

Figure 1-3: Main stages of the electrical energy generation from wind energy [9].

To generate electricity from wind, a turbine is required. At present, the variable speed turbines like the permanent synchronous generators (PMSGs) and the doubly fed induction generators (DFIGs) are most favoured and popular in the market due to their variable speed operations. This give them remarkable advantages of allowing the generator to harvest wind energy during different wind velocity than fixed speed wind turbines. At normal conditions, the PMSG wind turbine is stable and can harvest maximum power with high efficiency [10]. The suitability of sites for wind energy generation does not only depends on the magnitude of the wind but also on proximity to grid and environmental inpact assessment among others [11]. The electrical energy (E) generated by wind is given by equation 1.1.

$$E=\frac{1}{2}\rho A U^{3} \qquad 1.1$$

Where; ρ is the density of air, A is rotor swept area and U is the wind speed.

1.3.2 Biomass

Biomass is one of the renewable energy sources produced from wood, straw, charcoal, methane rich biogas among many other sources. This is the first fuel ever used by mankind and the mainstay of the world fuel economy until the mid 18 century. About 70% of India's cooking energy needs and 32% of primary energy requirement is met with biomass [12]. Currently, biomass generate about 10% of the world's energy with up to 90% in the global poorest countries. Countries that have made giant strides in this area include Sweden, Austria, Brazil and China [13].

However, continued exploitation of biomass energy risk sacrificing natural areas of farm lands and waterways resulting in threats to food supplies and deforestation. While

there are real opportunities in the area of energy generation from biomass, the concerns are also justified [12].

1.3.3 Hydroelectricity

Hydropower is one of the cheapest and reliable renewable energy source because it utilised the continuous flow of water to generate electricity without using up the water resources. Hydroelectricity is the conversion of potential energy of flowing water into electrical energy. This energy source has the capability to produce sustainable energy indefinitely with no emission of pollutant and greenhouse gases [14].

Figure 1.4 shows the schematic diagram of a hydroelectric generating plant. This type of energy generation is heavely dependent on the building of dams, which will affect the ecology and fish migration. It has been reported that 76% of all renewable is supplied by hydropower and it accounts for 16.4% of the world energy in 2015 [15]. China has the world largest hydroelectric generating plant with 22.5 GW capacity while the largest in the United States of America has a generating capacity of 6.8 GW [16].

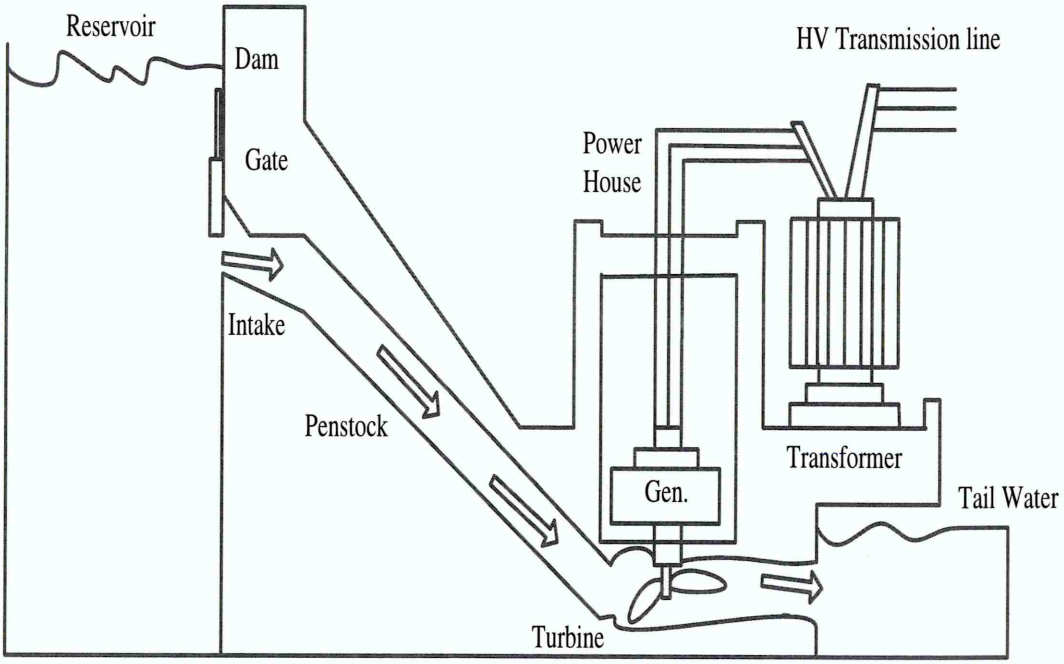

Figure 1-4: Schematic diagram of hydroelectric power plant [Redrawn from [14]].

Any hydroelectric power plant requires a dam constructed on a hilly area to ensure water storage at height (Figure 1.4). Water from the storage is led to the turbine through penstock steel pipe and at this point, the potential energy of the elevated water is

converted to kinetic energy as it flows down due to gravity. Then the kinetic energy of the water drives the turbine to convert hydraulic energy to mechanical energy and the generator converts mechanical energy into electrical energy [17]. Finally the water through the turbine will exit to a river on the downstream side of the dam. The hydraulic turbine used in hydroplant depends on the *head* which is the height difference. Commonly employed turbines includes; propeller or axial turbine, adjustable Kaplan turbine and Frances turbine among others [14]. The hydropower plant play a key role in the supply of electricity for both households and industries. The available power, P can be calculated from equation 1.2 [18].

$$P = \eta \rho Q g h \qquad 1.2$$

where: P is the power in Watts, η is the dimensionless efficiency of the turbine, ρ is the density of water in kilograms per cubic metre, Q is the flow in cubic metres per second, g is the acceleration due to gravity, h is the height differenc between inlet and outlet

Hydropower produces nearly zero CO_2 emission during operation. However, the concern is the materials used for the construction such as the cement and metals serve as the sources for CO_2 and methane (CH_4) emission. Building of hyroplant is a capital intensive project and could lead to environmental deterioration to nearby areas and cause fish migration. Other concerns include the possibility of increased landslide activity due to erosion caused by reduction and over flooding of reservoir water levels among others [19].

1.3.4 Solar energy

Solar energy is the radiant light and heat from the Sun that is harnessed using a range of ever-evolving technologies such as solar heating and photovoltaics (PV). Sun is the largest star in the solar system with a surface temperature of approximately 6000 K [20] and its energy is usually source at its core where hydrogen is converted to helium in a thermonuclear reaction. This energy travels from the core to the surface of the sun where it is finally released with only a small fraction reaching the earth in two forms of heat and light [21]. An approximate energy of 4×10^{14} Joules per day reaches the earth surface from a distance of ~1.5×10^{8} km from the sun in light speed of 8.5 minutes. The Sun is mainly composed of elements such as hydrogen (74%) and helium (25%) while the remaining are traces of some heavy elements. The distribution and intensity of solar radiation vary from one location to the other due to factors such as latitude, season and time of the day [6].

Another important parameter here is the solar constant experimentally given as 1.35 kWm^{-2}. Solar constant is defined as the amount of energy that falls normally on a unit area (1 m^2) of the earth's atmosphere per second when the earth is at its mean distance from the Sun [22]. Solar power determines climate and is the basis for sustaining life.

1.3.4.1 The solar spectrum

The solar spectrum is usually approximated to a black body radiator at a temperature of 6000 K. The Sun's energy is simply radiated as electromagnetic radiation in the ultra-violet to infrared region with Ultra-violet (UV) light (100-400) nm, visible light (400-700) nm and Infra-red (IR) 700 nm and above. This radiation can be short wavelength or high energy (e.g UV) and long wavelength or low-energy (IR) [23]. While on transit to the earth, some of the solar radiations are reflected, absorbed and scattered in the atmosphere before reaching the earth surface. The variation of the attenuation due to the atmosphere is dependent on the path length taken by the light through the atmosphere with longer path length leading to more scattering and absorption of solar radiation by atmospheric constituents such as air molecules, aerosols and water vapour [24]. Minimum path length occurs when the sun is directly overhead and this path length is described in terms of "air mass" (AM).

The air mass can also be defined as;

$$AM=\frac{1}{\cos\theta_z}=\sec\theta_z \qquad 1.3$$

The air mass coefficient is defined as the proportion to the cosine of the zenith angle (θ_z). Where θ_z is the angle between the sun and the normal vector pointing directly up to the zenith of the sky. AM0 corresponds to the solar spectrum outside the earth's atmosphere where there is no absorption and is relevant to space applications. The degree to which the atmosphere affects the sunlight received at the Earth's surface is defined by the "Air Mass" (AM) [25]. When the sun is directly overhead (at zenith), the path length is 1.0 (AM1.0). Therefore, AM1.0 is the solar spectrum received on the surface of the earth when the sun is directly overhead with incident power density of 925 Wm^{-2}. The increase in the zenith angle, θ results in the increase of the air mass by approximately sec θ such that at $\theta=48.2^o$ from the vertical, the air mass is 1.5 (AM1.5) [24]. Figures 1.5 and 1.6 respectively show the solar spectrum and the path length of the sunlight through the atmosphere.

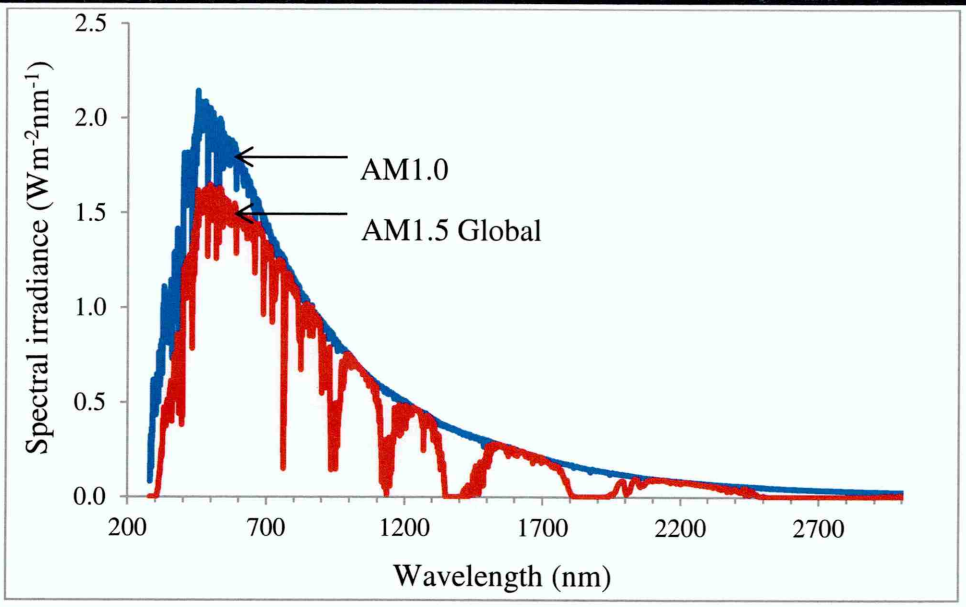

Figure 1-5: The approximate solar radiation spectrum [22].

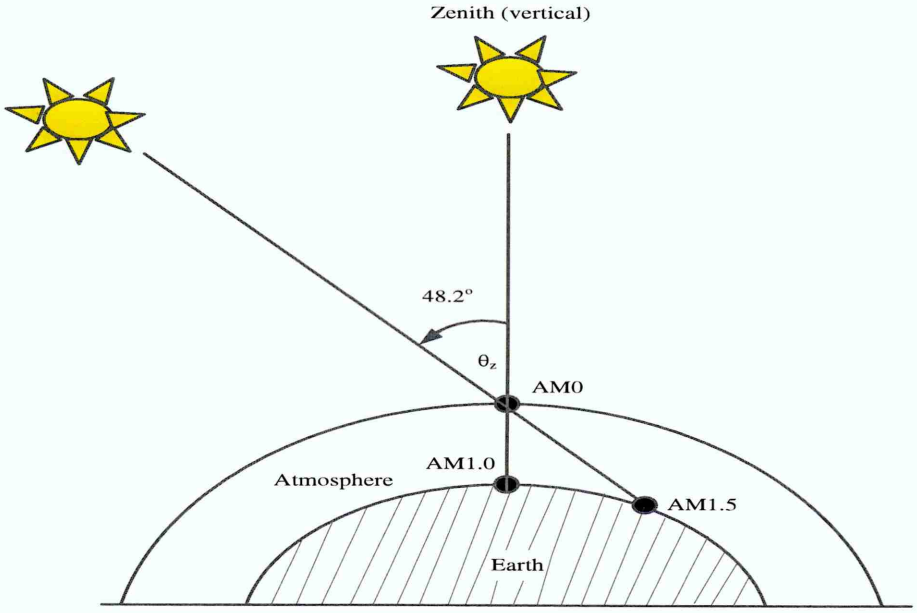

Figure 1-6: Path length of the sunlight through the atmosphere [Redrawn from ref [24]].

The terrestrial standard of evaluating solar cell and solar panels normally uses the AM1.5 solar spectrum. This is the solar spectral irradiance distribution incident at the sea level from the sun at 48.2° with total power incident of ~100 mWcm^{-2} (1000 Wm^{-2}). All fabricated solar cells in this research were characterised using the AM1.5 global standard conditions. On reaching the Earth surface, the solar radiation can be directly converted to useful energy in the form of heat (solar thermal) or electric energy (solar photovoltaic).

Solar energy from the Sun can be converted into useful energy in form of heat or electrical energy. The first method by which solar radiation is converted to heat energy is known as solar thermal. This method utilises appropriate technologies to convert the radiation absorbed from the Sun into heat.

The other method is the photovoltaic (PV) conversion. This is the process by which the radiation from the Sun is directly converted to electrical energy using an electronic device called a solar cell. This electronic devices use special class of materials with specific properties that can absorb photons and convert these photons into useful electrical energy.

1.3.4.2 Solar thermal

Solar thermal technology uses the free energy from the sun to generate low-cost and environmentally friendly thermal energy. The energy generated is used in heating water and other fluids [26]. This type of energy provides heating for homes, schools and other buildings and it is a low-cost and effective energy source [9]. It is estmated that about 200,000,000 billion kWh is received on the earth annually [27]. However, most of this energy is not properly harnessed.

In a solar water heater, the collector panel is mounted on rooftops and tilted towards the sun. This type of system usually consists of three components. The main steel plate absorber is bonded to steel or copper tubing through which water circulates. To maximise solar absorption, the plate is painted black and the whole system is encapsulated within a glass sheet to avoid heat losses [20]. A storage tank and pump circulation system to transfer heat from the panel to the tank is required. The solar thermal principle is also utilised in drying food and other farm produce using solar driers especially in developing countries where there are no high technology storage systems [27].

1.3.4.3 Solar Photovoltaics

Solar photovoltaics (PV) or solar electricity utilises PV effect to directly convert solar energy into electricity. When light energy (photons) with energy equal to or greater than the bandgap is absorbed by a suitable semiconductor material, elecron hole (e-h) pairs are created, separated and forced to the external circuit by the internal electric field before they recombine. This will produce a useful electric current in the external circuit [28]. The photovoltaic effect phenomenon was first discovered by a french scientist

Edmund Becquerel in 1839 [29]. Solar PV is one of the most clean and environmentally friendly source of energy. For effective PV solar energy conversion, four basic process most be satisfied, these include; (i) absorption of photons by a suitable semiconductor material (ii) effective creation of electron-hole (e-h) pairs (iii) separation of e-h pairs before recombination (iv) collection of the photogenerated charge carriers at the external circuit for the creation of useful electric current. However, if one of these processes is not fulfilled, the device will show poor solar to electric conversion efficiency [29]. Figure 1.5 show schematic representation of the PV effect.

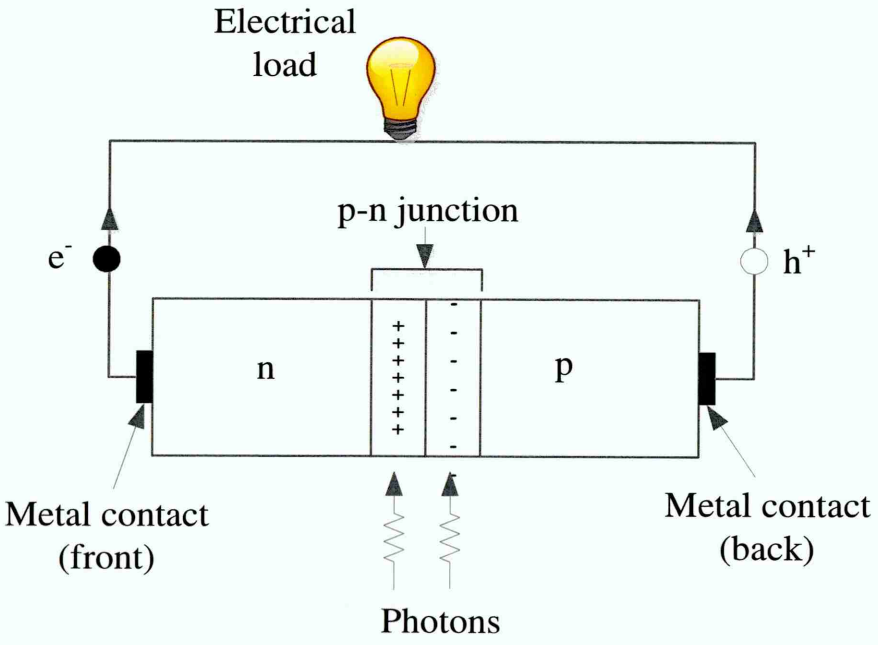

Figure 1-7: p-n juction solar cell showing the absorption of photons, creation of electron-hole pairs, separation and transport them to external circuit to produce useful energy.

Selecting the right semiconductor materials with desirable properties is a challenging task for scientists in this field. Semiconductors are those materials whose electrical conductivity lies between that of metals and insulators. Over the past decades, many semiconductor materials have been developed to our present day situation. Solar cells are basically classified into first, second and third generations devices. The first generation is silicon (Si)-based solar cells which are so far the most efficient for a single junction PV material but with high material processing costs. The second generation solar cells are based on thin films semiconductors such as copper indium gallium diselenide (CIGS), cadmium telluride (CdTe) and amorphous silicon (a-Si) [30,31]. These materials are low-cost but with comparably lower efficiencies to Si-based devices. Third generation solar cells are mostly based on organic dyes, quantum dots

and nanostructures and are actively under research in many laboratories but commercialisation has not yet been successful due to efficiency and stability issues [32]. The goal of the third generation solar cells is to improve the efficiencies of the presently commercialised solar cells by increasing the absorption coverage in the solar spectrum through hybrid systems. At present, the PV community is focusing on device fabrication based on graded bandgap solar cell devices which involves the use of semiconductor materials with different bandgaps for effective absorption of most of the solar spectrum to improve solar to electric conversion efficiencies and also to considerably reduce optical and thermalisation losses in the devices [33].

The efficiency of a solar cell is the percentage of power converted from solar energy to electrical energy under standard test condition (STC) (AM1.5 spectrum, 100 $mWcm^{-2}$ irradiance and 25°C cell temperature) [34]. A theoretical efficiency calculation for a single junction solar cell was first carried out by Schockley-Queisser detailed balance limit at ~30% for a single p-n junction of bandgap of 1.10 eV.[35]. This efficiency was calculated assuming an ideal p-n junction with only radiative recombination. The sun and the cell were also assumed to be black bodies with temperatures of 6000 K and 300 K respectively.

The efficiency of a solar cell depends on the open circuit voltage (V_{oc}), short-circuit current density (J_{sc}) and fill factor (FF). and The trade-off in solar cell is to select a material that can produce maximum efficiency. Figure 1.8 shows the values of the solar cell parameters with changes in the bandgap.

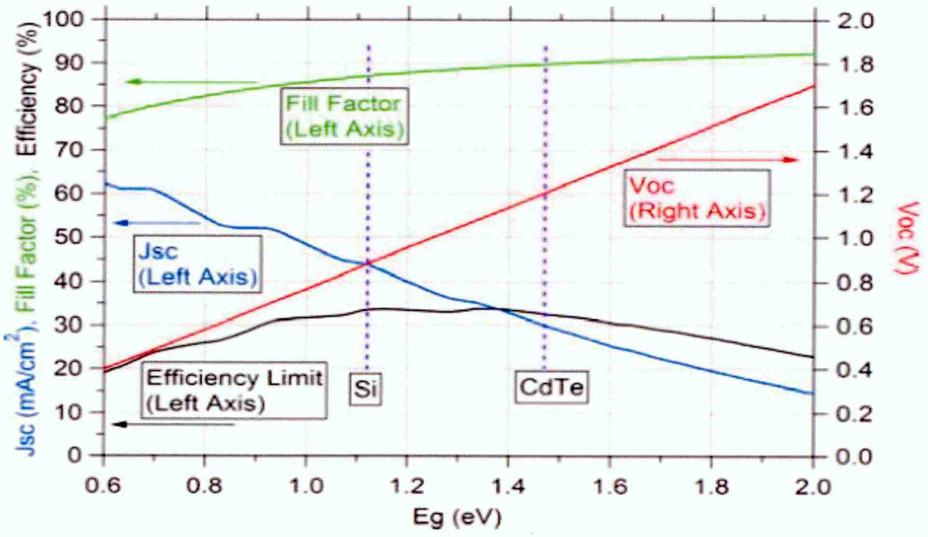

Figure 1-8: Ideal values for *Voc, Jsc, FF* and efficiency with changes in bandgap under standard test conditions [adapted from ref.[34]].

Figure 1.8 shows how the solar cell parameters (V_{oc}, J_{sc} *and FF*) vary with bandgap. J_{sc} is seen to have high values at low bandgaps, while V_{oc} and *FF* are observed to have high values at high bandgaps. Based on the above conditions and with reference to Figure1.8, it is seen that the highest efficiency of ~33% was calculated for a bandgap of ~1.40 eV. It is therefore established that materials whose bandgaps lies close to 1.4 eV are considered to have an ideal bandgap. The ideal PV materials depends on how its bandgap matches the solar spectrum which lies between 1.10-1.70 eV. PV materials whose bandgap falls in this range includes Si (Si, 1.12 eV), gallium arsenide (GaAs, 1.42 eV), cadmium telluride (CdTe, 1.49 eV) and copper indium diselenide (CIGS, 1.0-1.70 eV) [36]. These materials are the primary and widely used PV materials and their bandgaps lies within the near ideal bandgap for a single p-n junction solar cell. This is the reason why the property of "near ideal bandgap" (E_g=1.50 eV) is usually associated with CdTe semiconductor material.

1.4 Aims and objectives of the research

Research and development in the field of CdTe-based solar cell has been stagnated for a period of two decades until recently when First Solar reported the record efficiency of 22.1% [37]. This stagnation was not unconnected with lack of understanding in solid device physics aspect and complex material issues [38]. The PV community mostly work on a p-n hetero-junction solar cell utilising n-type cadmium sulphide (n-CdS) window layer and p-type cadmium telluride (p-CdTe) absorber layer. Britt and Ferekides [39] in 1993 reported an efficiency of 15.8% and nearly a decade later, NREL reported an efficiency of 16.5% in 2001; only an increase of 0.7% for a 10 years' worth of research. After another decade in 2011, First Solar reported a record efficiency of 17.3% which was only 0.8% increase from the previous efficiency record. This shows an increase of only 1.5% for about two decades of research. However, encouraging results started to emerge recently (2013-2016), which saw a rapid increase in efficiency over this period. The details of the efficiency evolution of the CdS/CdTe solar cell will be discussed in Chapter 2.

A new model to develop and further improve the efficiency of the CdS/CdTe solar cell has been proposed, design and reported by Dharmadasa in 2002 [40]. This model is based on the fabrication of a solar cell using a n-n hetero-junction between n-CdS/n-CdTe plus large Schottky barrier at the back metal contact. The proposed cell design has glass/conducting glass/n-CdS/n-CdTe/metal structure. This design moves away from the

conventional structure of single p-n junction solar cell [40]. This alternative model has achieved 18% [41] and 15.3% [42] using all electroplated semiconductors from non-aqueous and aqueous solutions respectively. The scalability and manufacturability of CdS/CdTe thin films solar cells by a simple electroplating technique using aqueous solution has been demonstrated and reported by BP achieving 14.2% [43].

The aim of this research project is to develop low-cost high efficiency multilayer graded bandgap solar cells based on CdTe absorber material. All the semiconducting materials of In_xSe_y, ZnS, CdS utilised in this research were grown using electroplating technique utilising two electrode (2E) system but the CdTe absorber material was grown in an aqueous deionised solution using 3E and 2E systems for comparison.

The objectives of this research work are given below:

i. Growth and optimisation of semiconductor materials of In_xSe_y, ZnS, CdS and CdTe.

ii. To study the structural, optical, morphological and electrical properties of the In_xSe_y, ZnS, CdS and CdTe thin films using available analytical techniques in the Materials and Engineering Research Institute of Sheffield Hallam University (SHU) and external collaborators.

iii. To study the effect of the cadmium chloride, $CdCl_2$ (CC) and cadmium chloride (CC)+cadmium fluoride, CdF_2, (CF) (CC+CF) treatment on the structural, optical and morphological properties of the CdTe absorber.

iv. To study the effect of $CdCl_2$ and $CdCl_2$+CdF_2 on the fabricated solar cell devices.

v. Fabricate n-CdS/n-CdTe hetero-junction solar cells.

vi. Fabricate n-In_xSe_y/n-CdTe hetero-junction solar cells.

vii. Fabricate multi-layer graded bandgap solar cells based on glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au structure.

viii. Fabricate multi-layer graded bandgap solar cells based on glass/FTO/n-ZnS/n-CdS/n-CdTe/Au structure.

ix. Characterisation of the fabricated solar cell devices using current-voltage (I-V) measurement. This is to assess and further optimise the processing steps so that highest possible efficiencies can be achieved.

1.5 Conclusions

This chapter discussed environmental issues as a result of carbon emission and other greenhouse gases (GHG) as they affect the global economy. The continuous dependence on fossil fuels is not helpful for cleaner, healthier, safer and greener ecosystem. It is therefore necessary that the fossil fuels are gradually substituted with renewable energies as the main stay of energy source for reliability, sustainability and growth of the global economy.

Among all the renewables discussed in section 1.3, solar energy is the best option for terrestrial renewable energy applications. The last section of this chapter presents the aims and objectives of this research programme.

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Chapter 2: Solar energy devices and interfaces

2.1 Introduction

The process of direct conversion of solar energy to electrical energy is called photovoltaic effect discovered by the French scientist Edmund Becquerel in 1839 [1,2]. Photovoltaic energy conversion requires special class of materials with specific optoelectronic properties. These materials are called semiconductors whose electrical conductivities lie between that of metals (10^{8}-10^{1}) $(\Omega cm)^{-1}$ and insulators (10^{-8}-10^{-20}) $(\Omega cm)^{-1}$. The fabrication of PV devices requires the formation of an intimate rectifying junctions or interface of materials with accurately known electrical conduction type [3]. Semiconductors basically exist in three types of electrical conductivity from which different solar cell designs were fabricated and commercialised. Figure 2.1 shows pure (intrinsic), n-type and p-type semiconductors. These electrical conductivity types can be achieved either by compositional doping [4] or by the addition of external impurities [5].

In intrinsic or pure semiconductors (Figure 2.1(a)), the concentration of electrons in the conduction band is equal to the concentration of holes in the valence band and the Fermi level (FL), E_{Fi} is right in the middle. In n-type semiconductor material, (Figure 2.1(b)), the concentration of electrons is higher than the concentration of holes and this shift the E_F close to the conduction band minimum. While in p-type semiconductor (Figure 2.1(c)), the concentration of holes is higher than the concentration of electrons and the E_F shift close to the valence band maximum. All PV solar cell devices are designed using the combination of these three types of materials for effective PV action.

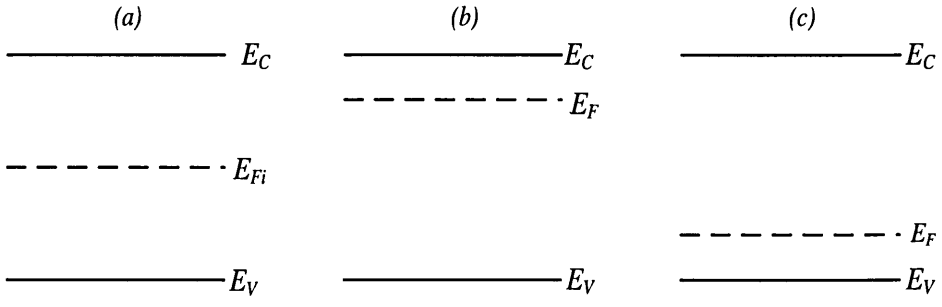


Figure 2-1: Energy level diagrams showing different conductivity types of (a) pure (intrinsic), (b) n-type and (c) p-type semiconductors.

For a semiconductor to be used in efficient solar to electric conversion application, it needs to satisfy some important optoelectronic properties. A bandgap of 1.5 eV has been identified as the optimum bandgap for a single p-n junction device in terrestrial energy conversion. This closely fit well to the energy bandgap range (1.0-1.7) eV of all the well-established solar cell technologies of silicon (Si), copper indium diselenide ($CuInSe_2$), gallium arsenide (GaAs), and cadmium telluride (CdTe) [6]. Another important parameter for a solar cell device is to have moderate doping concentration ~(10^{14}-10^{17}) cm^{-3} [7,8] and effective creation, separation and collection of charge carriers at the external circuit among others. Highly doped materials creates narrow depletion regions which allow the tunnelling of electrons through the barrier and low doping produces a very wide and resistive depletion region [9].

Silicon and GaAs are the most researched semiconductors and used in well-established PV technology of solar cells and are termed the first generation PV technologies. Both technologies especially silicon has been researched for over 60 years and have achieved efficiencies in excess of 25% [10]. With all the high efficiencies demonstrated by these technologies, their expensive material processing and the complex nature of their technologies have offset their efficiencies. Therefore, the search for simple and low-cost materials and technologies such as thin films technologies is continuing.

Thin film based solar cells such as CdTe, CIGS and a-Si:H are classified as second generation solar cells. This class of devices show comparatively low efficiencies than the first generation solar cells. They utilise low cost technologies and require less material for device production and their efficiencies are fast catching up with the crystalline silicon (C-Si). While third generation solar cell technologies are based on the improvement of solar cell efficiencies of the well-established solar cells and novel devices [2]. They are based on dye, quantum dots and nanostructured materials. Solar cell can be made from two or more layers of different electrical conductivities and varied bandgaps into intimate contact for the conversion of solar to electrical energy using p-n, p-i-n, n-n, n-n-n and n-n-p among others [2].

2.2 Silicon solar cells

Silicon (Si) is one of the most abundantly found elements on the Earth and the most extensively studied semiconductor material with over 60 years' research activities [2]. The deep knowledge of material and device aspects of Si over time makes it the champion cell with the highest solar to electricity conversion efficiency >25% [10].

However, the continuous production and sustainability of Si status in the PV community is faced by many challenges. The indirect bandgap (1.1 eV) nature of Si couple with its relatively low absorption coefficient necessitated the use of thick wafers (~200 μm) for the required absorption process. This requirement and the high level of purity required for single crystal Si makes it comparatively the most expensive material for PV solar cell devices. Polycrystalline Si could have been the best alternative for the single crystal Si. However, poly-Si is characterised with low efficiencies attributed to the negative impact of grain boundaries in the material.

The production line and device fabrication of Si involves four processing stages: (a) purification process, (b) crystallisation and wafer production, (c) processing of Si solar cells and (d) assembly of the solar panels. The conversion process of sand into Si solar panels requires the heating of the Si at temperatures above its melting point of 1,414°C. For solar cell fabrication, the Si is repeatedly heated to temperatures above 1,000°C. The main stages of a production line for Si-based devices are shown in Figure 2.2 [2].

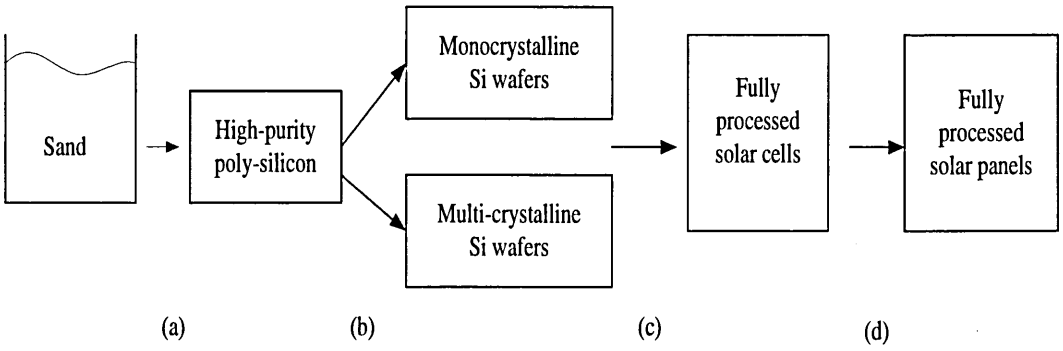


Figure 2-2: Industrial production lines required for manufacturing panels based on crystalline and polycrystalline Si [Redrawn from [2]].

Figure 2.2 shows stages involved in the manufacturing process of Si solar panels. Stage (a) is the purification of sand to high purity poly-silicon and stage (b) shows the production of mono- or multi-crystalline Si wafers from the high-purity poly-Si. The growth of single crystal Si boule was carried out using Czochralski method. Stages (c) and (d) are the final products of solar cells and solar panels respectively. The cost of PV is expressed in equation 2.1.

$$\text{Cost of solar power (\$/W)} = \frac{cost\ of\ production\ (\$)}{number\ of\ watts\ produced} \qquad 2.1$$

2.3 Thin film solar cells

Thin films based solar cell devices provide alternative to the highly expensive Si-based devices. Photovoltaic thin films based on cadmium telluride (CdTe), organic solar cells and dye-sensitised solar cells (DSSC) use less material and simple technologies which is directly related to cost reduction. This section describes in brief thin film technologies based on CdTe, organic and DSSC solar cells.

2.3.1 CdS/CdTe solar cells

Cadmium telluride (CdTe) thin films have received much attention due to their various applications in electronic devices such as solar cells [11] and radiation detectors [12]. The increase in demand for clean and sustainable energy is a huge challenge for the photovoltaic (PV) community to develop low-cost and high efficiency solar cells. The present sources of energy which are mostly from fossil fuel are harmful to the sustainability of our ecosystem. Alternative technologies such as the photovoltaics (PV) which convert sunlight to clean energy have been the main research focus at present [13]. The II-VI semiconductor materials have been found suitable in complementing this effort. Among these semiconductors, CdTe stands out to be one of the most researched and promising semiconductor materials in the production of both laboratory scale and large area optoelectronic devices such as the solar panels.

The main advantages of CdTe are its direct and near ideal bandgap of E_g=1.45 eV for a one bandgap simple p-n junction with high absorption coefficient (>10^4 cm^{-1}) at 300 K [14]. The history of CdTe based solar cell device goes back to Frerichs [15] when he developed phosphors including CdTe and measured its photoconductivity. Loferski in 1956 showed for the first time the possibility of CdTe to be used as material for PV conversion [16]. Afterwards many researchers have reported the growth of CdTe based solar cell devices mostly from high temperature vapour techniques [17,18]. But for the first polycrystalline solar cell based CdS/CdTe in the superstrate configuration was developed in 1969 by Adirovich *et al.* showing solar conversion efficiency > 2% [19]. This superstrate configuration is now taken as a standard for most research laboratories and commercialised solar PV products.

Matsushita (National/Panasonic), a Japanese company was the first company to commercialise PV modules based on screen printing grown CdTe PV modules and has held the world record efficiency of 9% from 1976 to 1980 [20]. Monosolar and Ametek held the world record efficiency of CdTe for 1980 and 1988 respectively [20]. A world

record efficiency of 12.3% on cell area of 0.302 cm^2 in 1989 was brought forward by Photon Energy, United States [21]. In 1991, T. L. Chu *et al.* from the University of South Florida (UoSF) achieved a new world record efficiency of 13.4% on cell area of 1 cm^2 [22]. The substrate used for this cell is fluorine-doped tin oxide (FTO) coated glass and the CdTe was deposited using CSS technique. Chu *et al.* [23] did some improvements on the conventional glass/FTO/CdS/CdTe/metal structure by reducing the CdS thickness, optimising the back contact and incorporating magnesium fluoride (MgF_2) antireflective (AR) coating. This resulted in a world record efficiency of 14.6% in 1992.

Britts and Ferekides [24] in 1993 came up with new record efficiency of 15.8% on area of 1.05 cm^2. The CdTe was grown on glass/FTO/CdS substrate with the use of antireflective coating. In 1997 another world record by H. Ohyama *et al* in Matsushita Battery Industrial Co. Ltd, Japan achieved an efficiency of 16% [25]. They used borosilicate glass/indium tin oxide (glass/ITO) substrate. The CdS was grown using MOCVD while the CdTe was grown using CSS and the devices were completed by depositing carbon and silver electrodes by screen printing and sintering technique. Wu *et al.* [26] at National Renewable Energy Laboratory (NREL) reported the highest achieved efficiency of 16.5% for CdS/CdTe solar cell in 2001. This efficiency was realised due to some modification made on the conventional glass/FTO/CdS/CdTe structure. The modified device structure is made by substituting the traditional FTO substrate with cadmium stannate, Cd_2SnO_4 (CTO) which show good properties of low resistivity, high transmittance and smoother surfaces. Another modification made was the incorporation of highly resistive zinc stannate, Zn_2SnO_4 (ZTO) buffer layer between the TCO and the CdS.

This efficiency value was stagnated for another decade mainly due to lack of full understanding of materials and device issues. The research and development in the PV community received a boost by the birth of a duo of First Solar Inc, in the United States and Q-Cells (Calaxo) in Germany. After 10 years stagnation of the record efficiency, First Solar, in 2011 reported a world record for CdS/CdTe solar cell with efficiency of 17.3% fabricated on area of 1.066 cm^2 [27]. In 2012 General Electric (GE) Company broke the First Solar's world record by achieving 18.3% on 1.032 cm^2 area [28]. First Solar came up with another new world record efficiency of 18.7% in 2013 [29] a slight increase on the previous record of 18.3% by GE. Surprisingly, GE came back to set another world record for CdTe in the middle of 2013 [30] achieving 19.6% efficiency a

reasonable gap from the previous by First Solar. In 2014, First Solar set another world record efficiency of 21.5% [31]. At present (2016), First Solar holds the world champion cell with 22.1% efficiency [32].

The achievement of these efficiencies over time in the PV community could be attributed to improved understanding in material and device physics aspects. Most of the record efficiency cells share many things in common, these include; active cell area of ~1 cm^2, the use of glass/FTO substrate as the front contact, the CdS window layer thickness was mostly in the range (50-100) nm, back contact was made up of graphite paste doped Cu, Ag, Au etc. Another similarity of the cells is that they were coated with anti-reflective materials. The device parameters, efficiency and year of achievement is summarised in Table 2.1 and the efficiency as a function of year of achievement is plotted in Figure 2.3.

Table 2-1: Summary of CdS/CdTe solar cell efficiency

V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	Team	Reference	Year
783	25.0	0.63	12.3	Photon energy	22	1989
840	21.9	0.73	13.4	UoSF	23	1991
850	24.4	0.71	14.6	UoSF	24	1992
843	25.1	0.75	15.8	UoSF	25	1993
840	26.1	0.73	16.0	Matsushita	26	1997
845	25.9	0.76	16.5	NREL	27	2001
842	29.0	0.76	17.3	First Solar	28	2011
857	27.0	0.77	18.3	GE	29	2012
852	28.6	0.77	18.7	First Solar	30	2013
857	28.6	0.80	19.6	GE	30	2013
876	30.3	0.79	21.4	First Solar	31	2014
887	31.7	0.79	22.1	First Solar	32	2016

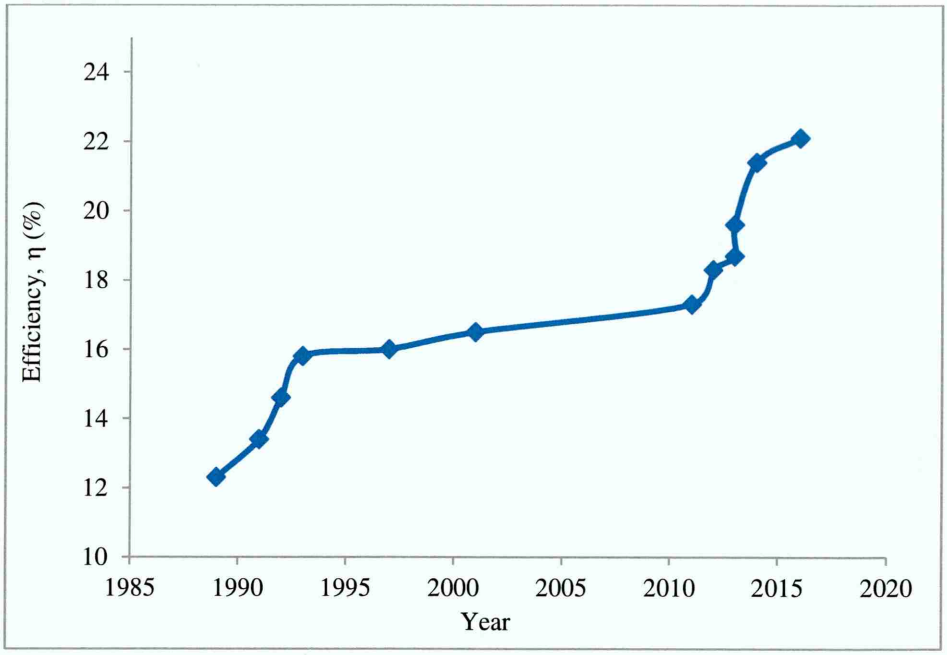


Figure 2-3: Plot of efficiency vs. year for the evolution of the CdS/CdTe solar cell efficiency

Figure 2.3 shows the efficiency vs. year of achievement in the record efficiency evolution trend for CdS/CdTe solar cell from 1989 to 2016. As observed from Figure 2.3, a rapid increase in the efficiency of the CdS/CdTe solar cell is observed between the periods 1989 to 2016. The efficiency is seen to increase from 12.3 in 1989 to 15.8% in 1993 within a period of five years which indicate an average increase of 3.5 over this period. It takes another four years in 1997 when 16.0% was achieved by Matsushita which was only 0.2% increase from the previous efficiency of 15.8% by Britts and Ferekides. It takes another four years to announce another record efficiency of 16.5 in 2001 announced by First Solar Company. This shows an increase of only 4.2% efficiency increase over a period of one decade (1989-2001). The increase in the cell efficiency over this long period of time was not impressive as it looks too slow. The PV community has to spend another decade long to come up with another record efficiency of 17.3% in 2011 brought forward again by First Solar. This is only 0.8% increase from the previous record efficiency by the same First Solar Company. This could rather be a fluctuation in the experimental measurement rather than an increase in the previous record efficiency. The stagnation of the CdS/CdTe cell efficiency over such a long period of time could be attributed to lack of full understanding in devices physics aspect and material issues.

A rapid increase in the cell efficiency is seen from 2011 to date (2016). The efficiency increase within this period (2011-2016) was 4.8%. This means that the equivalent of the

efficiency increase of 4.2% in the past decade was now achieved (4.8%) in just a period of five years. This is an impressive progress and it also indicates improved understanding in device physics aspect and materials issues. Generally, the increase in the cell efficiency over such a long period of time from 1989 to date is only 9.8%. Looking at the cell parameters, more improvement is required in the J_{sc} and V_{oc} values of these devices. Observation has shown that these record efficiencies were mostly achieved by Companies and not by academic based research institutions.

2.3.2 New model on CdS/CdTe solar cell structure

Over a period of 25 years, CdS/CdTe solar cell has been considered as a simple p-n junction device. All experimental results were interpreted assuming a p-n junction, but few key observations could not be explained in terms of p-n junction. Its back contact issues and reproducibility were puzzling researchers for a long period of time. In the scientific community, it is a known fact that the CdTe absorber material can be prepared in both n-type and p-type electrical conduction depending on the stoichiometry [33–36]; Cd-rich CdTe is n-type while Te-rich CdTe is p-type. Therefore, the CdS/CdTe solar cell could exist as a p-n junction or as an n-n+Schottky junction at the back metal contact as shown in Figure 2.4. As a result of extensive research on n-CdTe/metal interface, Dharmadasa *et al.* [37], proposed a new model in 2002, for this device structure. This was based on the Fermi pinning observed at metal/n-CdTe interface and hence the device is a combination of an n-n hetero-junction + large Schottky barrier at the metal/CdTe interface. Both devices are possible for CdS/CdTe solar cells, but for optimised devices, high efficiency solar cells come from the second structure as shown in Figure 2.4

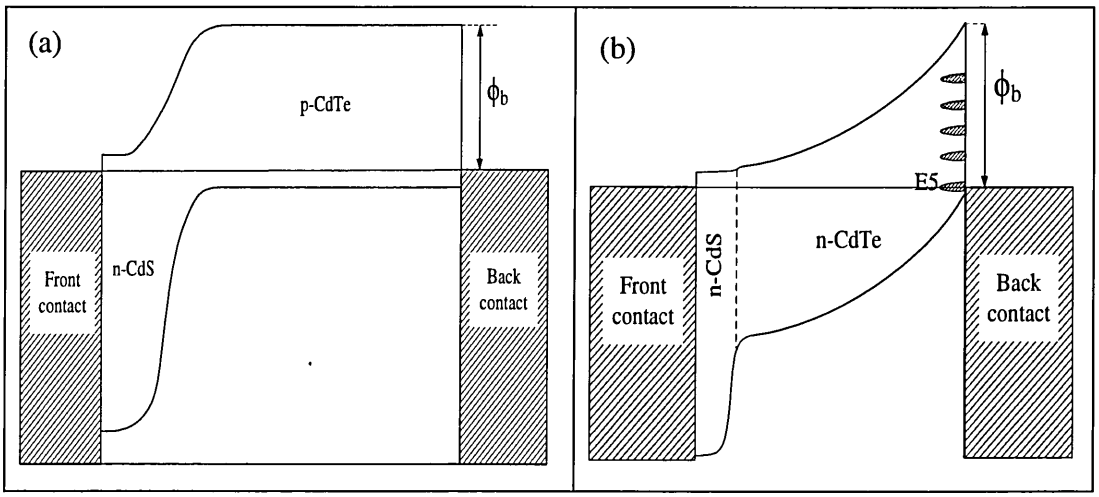


Figure 2-4: Two possible CdS/CdTe device structures based on (a) p-n junction and (b) n-n+Schottky barrier at the back metal contact.

This model is based on the fabrication of CdTe-based solar cells using n-CdTe as the absorber layer with the structure of n-CdS/n-CdTe plus Schottky barrier at the back metal contact (Figure 2.4(b)) away from the conventional p-n junction structure of n-CdS/p-CdTe solar cell. This model has two rectifying junctions of n-n at the CdS/CdTe interface and at the metal/n-CdTe back contact interface. The equivalent band diagram showing the activities of built-in impurity PV effect and impact ionisation incorporated in this new model is shown in Figure 2.5.

In comprehensive experiments using different metal contacts on vacuum cleaved, air-cleaved and chemically etched n-type CdTe surfaces, Dharmadasa identified at least five discrete Fermi level pinning positions [2,13] located at E_1=0.40±0.04, E_2=0.65±0.02, E_3=0.73±0.02, E_4=0.96±0.04 and E_5=1.18±0.02 eV below the conduction band minimum as shown in Figures 2.4(b) and Figure 2.5. Defects E_1, E_2 and E_3 are due to Te-rich surfaces while E_4 and E_5 are due to Cd-richness [38]. CdTe surfaces can be modified using suitable etchants to produce Te-rich or Cd-rich surfaces. Acidic etching using Br-methanol or potassium dichromate and sulphuric acid ($K_2Cr_2O_7$+H_2SO_4) leave CdTe surface with Te-richness while alkaline etching using sodium thiosulphate and sodium hydroxide ($Na_2S_2O_3$ + NaOH) etched leave Cd-rich surface. Depending on the surface stoichiometry, if the CdTe surface is Te-rich the Fermi level will pin at either E_1 or E_2 defect levels close to the midgap while Cd-richness forces the Fermi level to pin at defects levels E_4 or E_5 close to the valence band maximum. Factors such as growth conditions and other device processing procedures will influence the dominance of one defect level over others. For high performance solar cells, Cd-rich surface is preferable due to formation of large Schottky barrier (ϕ_b) at the metal/semiconductor interface [39] which improves the open circuit voltage (V_{oc}) of the device due to strong electric field created by the shape of the band bending within the device due to the high barrier or steep slope formed in the band diagram. Under this situation, the photo-generated charge carriers will be swept to their respective external terminals creating useful energy before they recombine. However, these processes are only true for optimised devices. Otherwise low quality device with poor electronic properties are observed [39]. To date this research group has achieved 18% efficiency based on the new model with materials grown using electrodeposition technique [35].

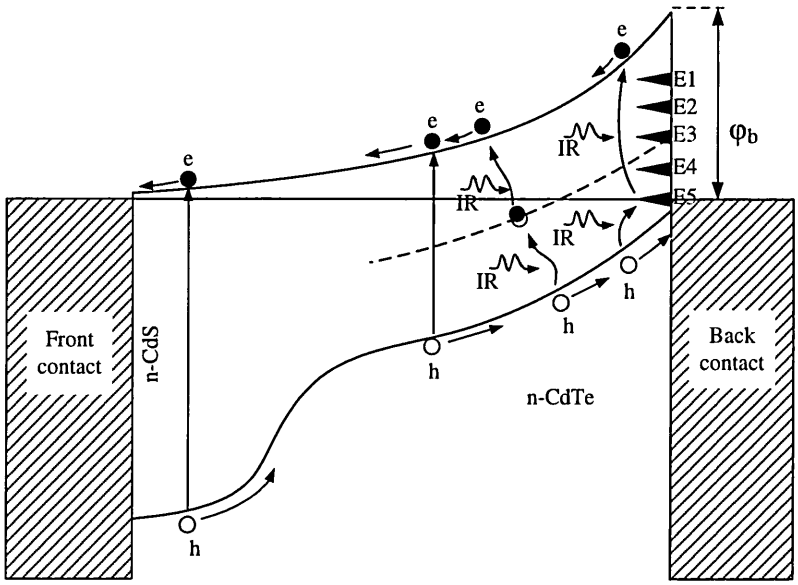


Figure 2-5: The energy band diagram of CdS/CdTe based on the new model of n-n+large Schottky barrier with strong Fermi level pinning at the metal/n-CdTe interface.

Device structure as shown in Figure 2.5, can also contribute to charge carrier generation via impurity PV effect (IPV) and impact ionisation. As shown in the diagram, defects can be involved in IPV effect, utilising infra-red radiations. Impact ionisation can also occur creating charge carriers by band-to-band or defect-level to conduction band promotion of electrons. These two contributions can contribute to increase in J_{sc} of these devices.

All the high efficiency solar cells reported in section 2.3.1 are grown from the costly and complex techniques such as closed space sublimation. While the PV market is moving from strength to strength, one key issue to focus on is further reduction in the cost of materials and manufacturing processes if the PV market is to compete favourably with the conventional and dominant fossil fuels. Electrodeposition (ED), a simple and low cost technique has so far shown promising results comparable to those obtained from high temperature growth techniques [11,35,40].

These materials (CdS and CdTe) can also be grown using a variety of deposition techniques which includes close-spaced sublimation (CSS) [12], molecular beam epitaxy (MBE) [41], metalorganic chemical vapour deposition (MOCVD) [42] and sputtering [43] among others.

CIGS solar cells are also developing in parallel, achieving ~22% efficient solar cells. Since this thesis is mainly on CdS/CdTe solar cells, focus will only be on CdS/CdTe solar cells.

2.4 Semiconductor junctions and interfaces

The fabrication of solar cells involves the formation of intimate contact between two or more similar or dissimilar semiconductors. The interface or junction formed can be rectifying or ohmic contact depending on the material and the contacting metal. Junction formed between semiconductors of the same material is called homo-junction while junction involving two semiconductors from two different materials with different bandgaps is called hetero-junction device. This section will discuss the types of junctions; p-n junction, p-i-n junction, hetero-junction, ohmic and rectifying (Schottky) contacts, used in PV devices.

2.4.1 P-n junction

A p-n junction is the basic of all electronic devices and is formed when an n-type semiconductor formed an intimate contact with a p-type semiconductor. In a p-type material, the majority carriers are holes while in the n-type material, the majority carriers are electrons. This junction can be a homo- or hetero-junction depending on whether the junction is formed between semiconductors of the same material or not. A homo-junction is an interface formed between two semiconductors of the same material when brought into intimate contact such that one is doped n-type and the other p-type while the lattice structure continues undisturbed. The electrical properties of this type of junction depends on the method by which it is made [44]. In hetero-junction type devices, the junction is formed between two dissimilar semiconductors. When in contact, electrons from the n-type semiconductor diffuse into the p-type semiconductor and holes from the p-type semiconductor will diffuse into the n-type semiconductor [45]. When this continues, a barrier known as the p-n junction is formed at the interface between the two semiconductors. Due to the formation of oppositely charge ions on either side of the junction, a built-in electric field $(E=-dV/dX)$ is established due to potential barrier formed at the junction [2]. This is represented by the slope in the Figure 2.6(b). Figure 2.6 shows the energy band diagram of a p-n junction before and after junction formation.

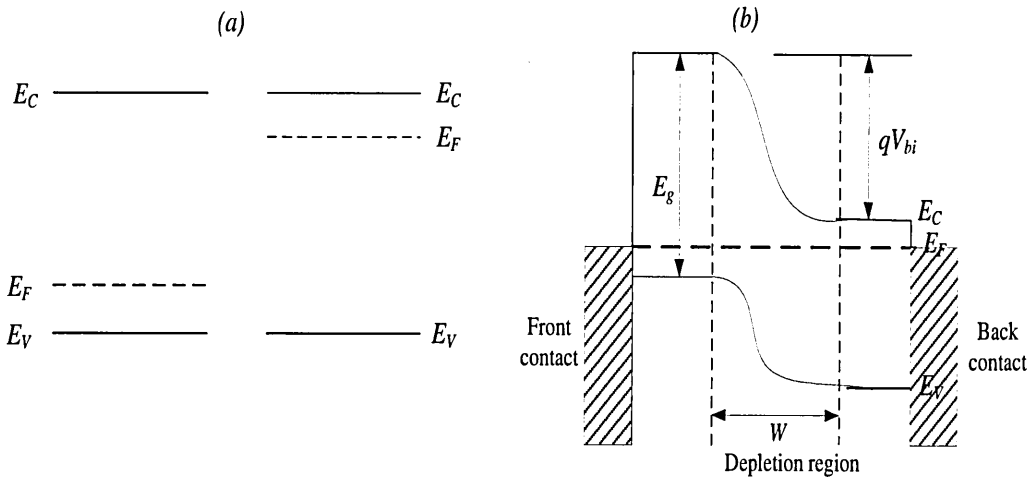


Figure 2-6: Energy band diagram for the formation of p-n junction (a) before junction formation and (b) after junction formation.

The built-in potential V_{bi} (V) at the depletion region can be estimated using equation 2.2.

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \qquad 2.2$$

where n_i^2 is the intrinsic concentration of electrons (in cm^{-3}) and other symbols have their usual meanings.

The depletion width, W (cm) is obtained using equation 2.3.

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)} \qquad 2.3$$

Where; ε_s is the dielectric constant of the semiconductor.

In an abrupt p^+-n junction, such that $N_A \gg N_D$, the depletion width is mostly concentrated on the n-region of the junction and equation 2.3 takes the form of equation 2.4.

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}} \qquad 2.4$$

2.4.2 p-i-n Junction

In a *p-n* junction type device, *p-* and *n-type* semiconductors are brought into direct contact to form the junction. However, a modification is made such that an *i-type* layer is sandwiched between the *p-type* and *n-type* semiconductors to form *p-i-n* type device. In solar cells, wide depletion region is desirable for the fabrication of high efficiency devices. This is achieved by the incorporation of low doped material between the p and n-type materials. It is known that heavily doped materials are characterised by thin depletion region which is not helpful for the fabrication of high performance solar cells. As observed in the band diagram of *p-i-n* shown in Figure 2.7, the Fermi levels of the *p* and *n* layers is seen to align through the *i*-layer and this create strong electric field throughout the *i*-layer. However, there should be optimum thick requirement for the *i*-layer absorber. This structure helps to control the width of the depletion region [2]. Figure 2.7 shows the energy band diagram of p-i-n junction device. In practice, it is difficult to produce i-type material, due to difficulty in stoichiometric control of the constituent ions during growth.

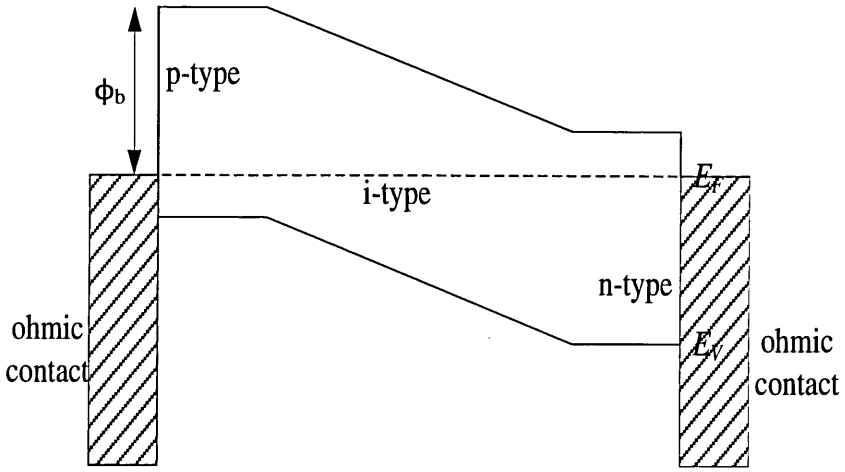


Figure 2-7: Energy band diagram of p-i-n junction device [Redrawn from ref.[2]].

2.4.3 Hetero-junction

A hetero-junction utilise two dissimilar semiconductor materials to form the junction structures usually from materials with two different bandgaps. Figure 2.8 shows an energy band diagram of a p-n hetero-junction structure. In PV devices, the material with wide bandgap, E_{g1} (CdS) serves as the window layer while the material with narrow bandgap, E_{g2} (CdTe) serves as the absorber material such that $E_{g1}>E_{g2}$ [46]. The advantage of this device over the p-n homo-junction is that, it can effectively absorb a

wider portion of the solar spectrum due to the varied energy bandgaps in the device. All photons with energy equal to or greater than the bandgaps (E_{g1} and E_{g2}) can be absorbed in the device for the creation of electron hole pairs (e-h).

The high energy photons enters the device through the wider bandgap window layer with ~100 nm thick to allow for the transmission of the incident photon to reach the interface for the creation of photo-generated charge carriers. The challenge of this type of device is that, the junction is made with two different materials (window and absorber layers) which obviously possessed different physical and chemical properties. This is very likely to introduce detrimental surface states and lattice mismatch between the metallurgical junctions formed between the two layers. This is as a result of conduction and valence band discontinuities formed at the CdS/CdTe interface. This situation impedes the creation of a healthy depletion region that can create and effectively separate the charge carriers to their respective electrode.

For efficient solar cell fabrication, the interface between the CdS window and the CdTe absorber should possessed minimum interface states which act as recombination centers [47]. The abrupt nature of the junction should also be removed or well passivated by high temperature growth of materials or post growth annealing with chemical such as $CdCl_2$ (CC), $CdCl_2$+CdF_2 (CF) or other suitable fluxing agents. This helps in smooth transition at the junction between the window and the absorber layers.

Anderson in 1962 [48] proposed the transport mechanism for heterojunctions as an extension to the homo-junction model. Figure 2.8 shows the energy band diagram of n-CdS and P-CdTe hetero-junction solar cell before junction formation. Based on the Anderson model, the essential semiconductor parameters used to characterise the hetero-junctions are the electron affinity χ, energy bandgap E_g and work function Φ. When the two semiconductors are brought into intimate contact, The Fermi level in the two semiconductors must align throughout the device length. This alignment forces band bending in the device structure which in turn creates electric field in the device. Then there will be diffusion of charge carriers to the opposite side of the junction and as this continuous, a depletion region is formed at the junction. The barrier height for an ideal interface is given by equation 2.5:

$$qV_b = E_{g2} + \Delta E_c - \delta_n - \delta_p \qquad 2.5$$

Where E_{g2} is the bandgap of the p-type semiconductor (CdTe), ΔE_C is the conduction band discontinuity at the junction while the displacement of the Fermi level from the conduction and valence band edges for the *n*-type and *p*-type semiconductors are given by δ_n and δ_p respectively. The band discontinuities at the conduction band (ΔE_C) and the valence band (ΔE_V) edges are given by equations 2.6 and 2.7:

$$\Delta E_C = \chi_p - \chi_n \qquad 2.6$$

$$\Delta E_V = (E_{g1} - E_{g2}) - \Delta E_C \qquad 2.7$$

Where; χ_p and χ_n are respectively the electron affinities of the p-type and n-type semiconductors and E_{g1} is the bandgap of the n-type material (CdS).

The discontinuity at the conduction band edge act like a "spike" which impede smooth flow of photo-generated charge carriers across the junction [48]. Figure 2.9 depicts the n-CdS/p-CdTe device showing untreated and treated junctions. Niles and Höchst [47] study for the first time the band alignment property of the n-CdS/p-CdTe hetero-junction employing synchrotron radiation photoelectron spectroscopy in which they obtained a valence band offset ΔE_V=0.65 eV. Except for this study, all other experiments on band alignment consistently show a valence band offset at the CdS/CdTe junction to be ΔE_V=1.0±0.05 eV which corresponds to conduction band offset of about $\Delta E_C \cong$-0.10 eV. This indicates that the conduction band of CdTe is at higher energy than that of CdS which also help in the achievement of high efficiency by the CdS/CdTe solar cells [49].

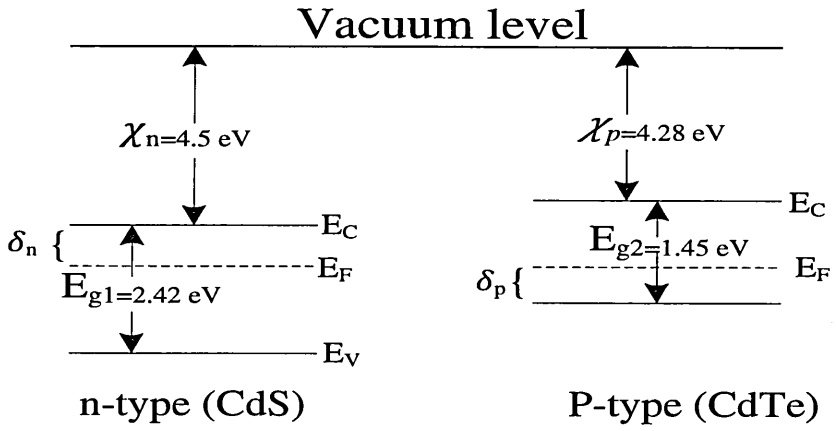


Figure 2-8: Energy band diagram of *n*-CdS and *p*-CdTe before junction formation [diagram redrawn from [50]].

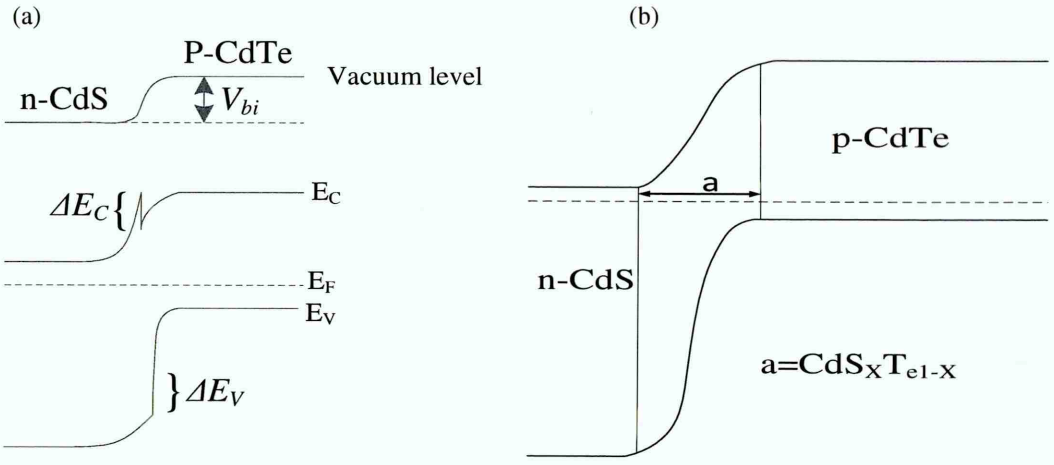


Figure 2-9: Energy band diagram of n-CdS/P-CdTe for (a) not activated and (b) Cl activated junction.

Figure 2.9 shows the energy band diagram of CdS/CdTe interface for not activated and activated junctions. The difference in the lattice constants of CdS, 5.82Å and CdTe, 6.48Å is responsible for the large lattice mismatch that exists at the CdS/CdTe hetero-junction. The lattice mismatch between CdS and CdTe is ~10% [51] and result to defects states at the junction which serves as recombination centres [52]. Other sources at the interface could be native of the materials and impurities incorporated into the device during processing procedures. The formation of the ternary alloy CdS_XTe_{1-X} at the CdS/CdTe interface during annealing process is well documented [53,54]. The existent of this intermediate layer is responsible for removing the abrupt nature at the interface and reduction of defects density due to S diffusion into CdTe [55,56]. The extend of this diffusion depends on many processing factors such as growth temperature of the materials and the $CdCl_2$ annealing condition [57]. Many studies have shown that annealing of the CdS/CdTe structure in the presence of either $CdCl_2$ (CC) [58,59] or $CdCl_2$+CdF_2 (CF) [56,60] is accompanied by grain growth, grain boundary passivation, recrystallisation [61,62] increased in minority charge carriers [52,63], reduced internal stress [64], reduced material resistivity [65]. Both chlorine (Cl) and fluorine F are fluxing agents which diffuse through the grain boundaries during annealing process impacting positively on both material and device properties. Reports show that treatment with the mixture of Cl and F have shown to produce better devices due to double effect in the two elements than in Cl only [5,60,66]. F is known to have small atomic radii than Cl and can diffuse easily through the grain boundaries than Cl.

In the as-deposited materials, the grain boundaries act as recombination and electron scattering sites impeding the free flow of electrons but after CC treatment, these grain boundaries are mostly passivated and help in the fast transport and separation of photo-generated charge carriers to their respective external contact. The as-deposited material is compost of smaller grains which indicate high density of grain boundaries and when incorporated in devices, it is obvious that it has to undergo the CC treatment else the device will be full of grain boundaries in the bulk of the materials and defects at the interface.

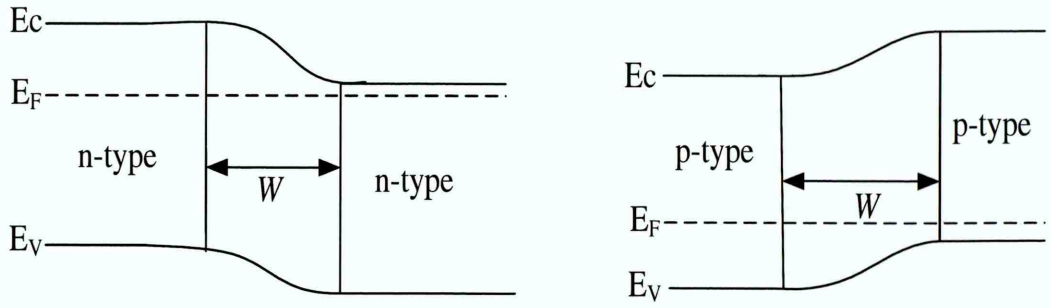
Abbas *et al.* [67] reported on the effect of CC treatment on the conversion efficiency of CdS/CdTe solar cell. This experiment was carried out by subjecting two CdS/CdTe samples to the same processing step. However, one of the samples was treated in CC to study the effect of this important treatment. The untreated sample show efficiency of 0.1% while the CC treated sample showed an efficiency of 11.8% attributed to recrystallisation in the material. This practically indicates the effectiveness of some of the benefits on the CC treatment mentioned above. This shows the imperativeness of fabrication of solar cells with highly crystalline materials. On the other hand, if the material is not crystalline the conversion efficiency is always poor due to lack of the CC treatment. The effect of CC or CF with untreated samples has been studied in Chapter 8 of this thesis. It shows that devices treated with CC or CF show better performance.

Generally, PV materials require high growth or post growth annealing temperature in the presence of CC activation treatment for high efficiency performance solar cell devices [3]. With all these beneficial properties of the CC activation, the PV community still do not fully understand the exact mechanism of this important activation treatment.

Unlike in the silicon p-n homo-junction, hetero-junction devices such as CdS/CdTe can easily be fabricated with simple and low-cost deposition techniques like electroplating technique and can yield a very good working solar cell [68].

2.4.4 n-n$^+$ and p-p$^+$ Junctions

It is also possible to create internal electric field by using only one type of semiconductor materials [2] with different bandgaps as shown in Figure 2.9. It is observed that the barrier height created at each step is small. However, designs can be made such that these small steps are joined together to form a graded bandgap multi-layer solar cells discussed in the next section.



(a) n-n^+ junction (b) p-p^+ junction

Figure 2-10: Hetero-junction interfaces based on n-n^+ and p-p^+ junctions with small steps potential barriers.

2.4.5 Multi-layer graded bandgap devices

This type of device is purposely made to effectively absorb all photons from all regions of ultraviolet (UV), visible and infrared (IR) of the solar spectrum to improve the efficiency of the solar cell. There are two possible ways to implement this device structure: (1) by putting different semiconductor materials with varying bandgap together in grading manner. (2) It can also be formed by one compound whose bandgap can be altered by alloying the main semiconductor material like in the case of adding Al in GaAs to increase its bandgap. There are two designs structures for the fabrication of multi-layer graded bandgap solar cells (MGBSCs) depending on whether the starting window layer is n-type or p-type in electrical conduction. If the starting window layer is n-type material, the electrical conduction type of the series of layers in the device will gradually change from n^+ to p^+ through the stack of layers that consists n^+, n, i, p, and p^+ as indicated in Figure 2.10(a) where n^+, n, and i denotes heavily n-doped, moderately n-doped and intrinsic semiconducting layer. Similar definition applies to the p-type layers [69]. But if the starting material is p-type, the conduction type of the device will gradually change from p-type to n-type in the form p^+-p-i-n-n^+ as shown in Figure 2.10(b). The device can be structured such that, the layers are arranged so that the bandgap is decreasing while the conductivity type is gradually changing. It is also obvious that device structures based on p-type window layers which show decreasing bandgap of the device toward the back of the solar cell (see Figure 2.10(b)) give a better device option that will produce the highest possible potential barrier height (ϕ_b) relative to devices based on n-type window layer [70]. The barrier height produced in this device structure is nearly equal to the bandgap of the wide bandgap window material

and since ϕ_b is a function of the V_{oc}, the device is therefore capable of achieving highest possible V_{oc} value improving the device efficiency. This device also provides the highest slope which is the strongest electric field for electron movement.

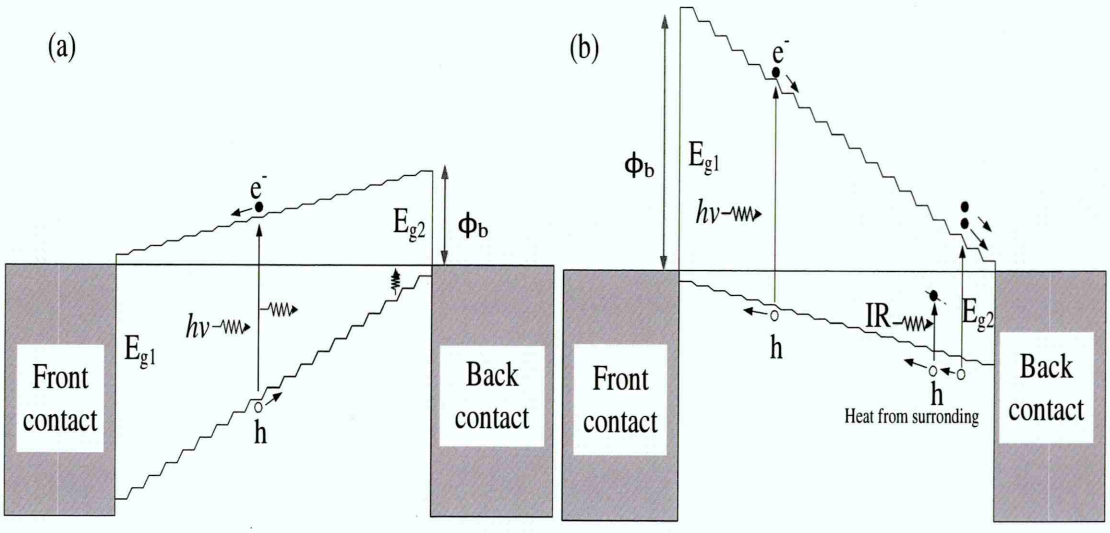


Figure 2-11: Energy band diagrams of multi-layer graded bandgap solar cell with (a) n-type window and (b) p-type window layers

Figure 2.11 presents the energy band diagram for MGBSCs based on n-type and p-type windows. This design was purposely made to effectively absorb photons in almost all portions of the solar spectrum to generate as much as possible electron hole pairs. In this type of devices, the high energy photons are absorbed by the larger bandgap layers while the low energy photons will be absorbed by the narrow bandgap materials at the rear of the device. The incorporation of mechanisms such as impurity PV effect and impact ionisation will further enhance the photo-activity of these devices. The impurities and native defects usually in the interface area at the rear of the device is positively utilised. The impurity PV (IPV) effect occurs when low energy photons from the sun or IR from the surroundings promote an electron from the valence band to one of the defect levels in the device. The hole left behind by this electron will be swept away to the front contact due to the nature of the band bending in the device (Figure 2.11(b)). While the electron is at the defect level, another low energy photon will promote it to another defect level close to the conduction band where it will be knocked off to the conduction band through impact ionisation and the electron will be accelerated to the front contact by the strong built-in electric field in the device impacting positively on the J_{sc} of the device. In this device, absorption of two or more IR photons at different absorption stages could create one e-h pair. With effective implementation of these mechanisms, the efficiency of the solar cell will be markedly

improved and negative effects such as thermalisation will be reduced. And this also explains the possible reasons for the high J_{sc} recorded in the fabricated devices in this research [71].

2.5 Metal-semiconductor contacts

Metal-semiconductor (MS) interface is an intimate contact between a suitable metal and a semiconductor so that important PV properties of the devices can be improved. Any metal/semiconductor device must at least have two metal contacts, one on either side of the semiconductor to effectively collect the photo-generated charge carriers for onward delivery to the external circuit. Depending on the design, the solar cell device can have either ohmic or rectifying (Schottky) electrical contacts [72]. This section will discuss basic metal-semiconductor junctions; ohmic contacts, rectifying (Schottky) contacts, and MIS junctions.

2.5.1 Ohmic MS contacts

Ohmic contact is a MS contact that has a negligible contact resistance relative to the bulk semiconductor resistance. Important notable parameters under this subject are the work function of the metal contact (ϕ_m), work function of the semiconductor (ϕ_s) and the electron affinity of the semiconductor (χ_s). If an n-type semiconductor makes an intimate contact with a metal contact such that, ($\phi_m<\phi_s$), the bands in the semiconductor bends downward and gives rise to an ohmic contact. Ohmic contact can also be formed if a p-type semiconductor is brought into an intimate contact with metal contact such that ($\phi_m> \phi_s$) the bands in the semiconductor will bends upwards [73]. In any case the band bending is always formed in the semiconductor near the interface irrespective of whether the contact is ohmic or rectifying. Figure 2.11 shows a schematic of MS with two ohmic contacts one at either side of the semiconductor. Alternatives for achieving ohmic contact is the surface modification of the semiconductor using suitable etchant like potassium dichromate which leave the CdTe surface with thin Te-rich layer before the metal contacts are made. The other alternative is to incorporate a highly doped material layer to narrow down the depletion region enhancing the tunnelling of charge carriers [45].

In an ohmic contact, the depletion region formed in the semiconductor is narrow with approximate barrier height less than 0.30 eV. It is also important to note that metal-semiconductor interfaces are difficult to deal with due to non-ideal nature of the

semiconductor surface due to formation of oxide layers on the semiconductor [45]. This usual non-ideality at the metal/semiconductor interface makes the subject difficult to deal with such that these interfaces do not follow strictly the metal-semiconductor theories [7,74–76]. Fermi level pinning due to defects, in real semiconductor/metal interfaces makes the subject more complicated.

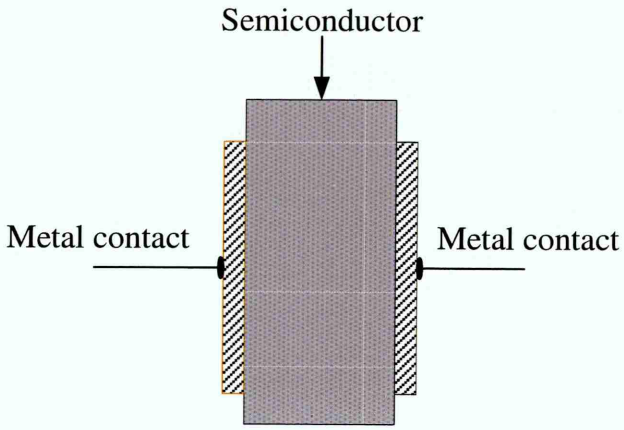


Figure 2-12: Schematic of semiconductor device showing two metal contacts semiconductor device structure.

2.5.2 Rectifying (Schottky) MS contacts

The formation of rectifying Schottky contact between a metal and a semiconductor is directly influence by the work functions of the metal and the semiconductor involve. It is desirable that the work functions of the metal and semiconductor are different. If an n-type semiconductor is brought into intimate contact with a metal contact such that ($\phi_m > \phi_s$) then a rectifying Schottky contact is formed. If the semiconductor is p-type such that ($\phi_m < \phi_s$), then a rectifying Schottky junction can also be formed. Figure 2.12 shows the energy band diagram of a metal/n-type semiconductor interface.

For an ideal semiconductor, with no surface states and other defects, the barrier formed is estimated using equation 2.5. Figure 2.12(a) shows that the work function of the metal is higher than that of the n-type semiconductor ($\Phi_m > \Phi_s$). In Figure 2.12(a), it is also seen that the Fermi level (FL) of the semiconductor is higher than the Fermi level of the contacting metal. After the formation of intimate contact (Figure 2.12(b)), electrons will flow from the semiconductor into the metal. This will continue until the two Fermi levels of the metal and semiconductor align forcing the conduction band and the valence band in the semiconductor to bend upward. Then the two materials are said to be in thermal equilibrium.

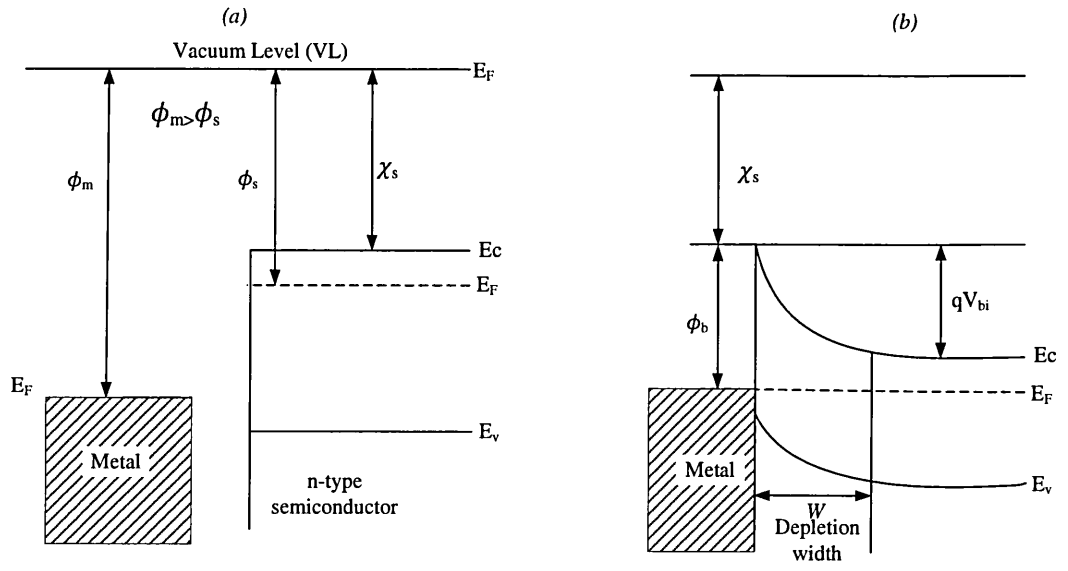


Figure 2-13: Energy band diagram showing the formation of potential barrier at metal/n-type semiconductor interface.

The upward bending of the semiconductor creates a potential barrier to electron flow into the metal (see Figure 2.12(b)). At this point, negative charges are created on the metal side of the junction whereas positive charges are created on the semiconductor surface leading to the formation of a depletion region (W) in the semiconductor close to the metal contact. This situation creates an internal electric field (E) in the device. If the width of the depletion region is narrowed down, electrons can tunnel through the barrier. The barrier height formed can be found using equation 2.8.

$$\phi_{bn} = \phi_m - \chi_s \qquad 2.8$$

If similar junction is formed between a metal and p-type semiconductor, a reverse situation is obtained (i.e $\Phi_m < \Phi_s$) with the band bending in the opposite direction creating a potential barrier for holes expressed by equation 2.9. Figure 2.13 shows a rectifying Schottky contact on p-type semiconductor.

$$\phi_{bp} = E_g - (\phi_m - \chi_s) \qquad 2.9$$

These simple explanations are valid only for ideal interfaces. However, for real interfaces involving thin film semiconductors, defects levels can dominate and Fermi level pinning can decide the height of the potential barrier. In these cases, potential barrier height can be independent of the metal work function.

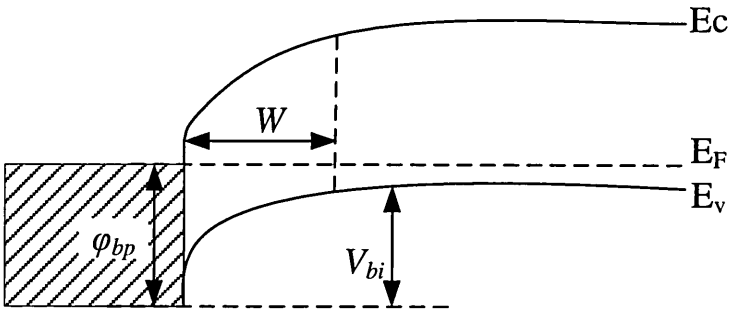


Figure 2-14: Rectifying (Schottky) contact formed between a metal and a p-type semiconductor.

2.5.3 Metal-insulator-semiconductor interface

The MS Schottky devices presented in section 2.5.2 are characterised by low barrier height (ϕ_b) when compared with simple p-n junction [2,72]. Since ϕ_b is a function of V_{oc}. Therefore, the V_{oc} obtained from p-n junction solar cells is higher than that of MS structures. Under ideal interface, the Schottky barrier is approximately half of the p-n junction as presented in Figure 2.14 thus the reason for observed low ϕ_b. However, this challenging situation can be eliminated if a thin insulating layer is sandwiched at the metal/semiconductor interface. The device structure is now modified to metal-insulator-semiconductor (MIS) structure. When incorporated with optimum layer thickness (δ) [2], the *i-layer* decouples the metal from the semiconductor and increases the potential barrier provided by the band bending as shown in Figure 2.15. The rectification property of this device is improved and is given by equation 2.10 [2].

$$I_D = SA^*T^2 \exp\left(-\chi^{\frac{1}{2}}\delta\right)\exp\left(\frac{-\phi_b}{kT}\right)\exp\left(\frac{eV}{nkT}\right) \qquad 2.10$$

Where χ is the mean barrier height achieved by the intermediate insulating layer of thickness, δ, in Angstrom (Å).

This modification is one method used to improve the V_{oc} of Schottky based devices since ϕ_b is directly related to V_{oc}. Another advantage of the insulating layer is that, by decoupling the metal and the semiconductor, interface interaction between the metal and the semiconductor is removed. This also leads to reduced degradation of the contact electrode of the device which in turn improves the stability and lifetime of the device.

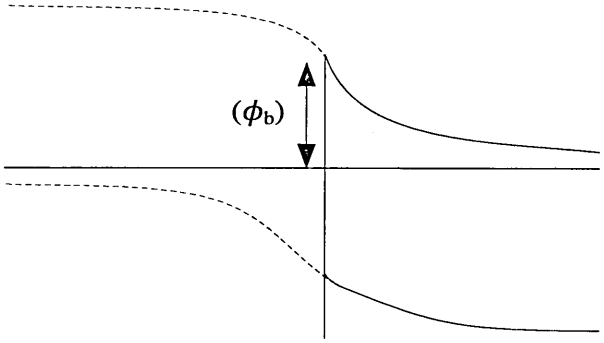


Figure 2-15: Schematic diagram showing that Schottky barrier is only a half of a p-n junction for an ideal interface.

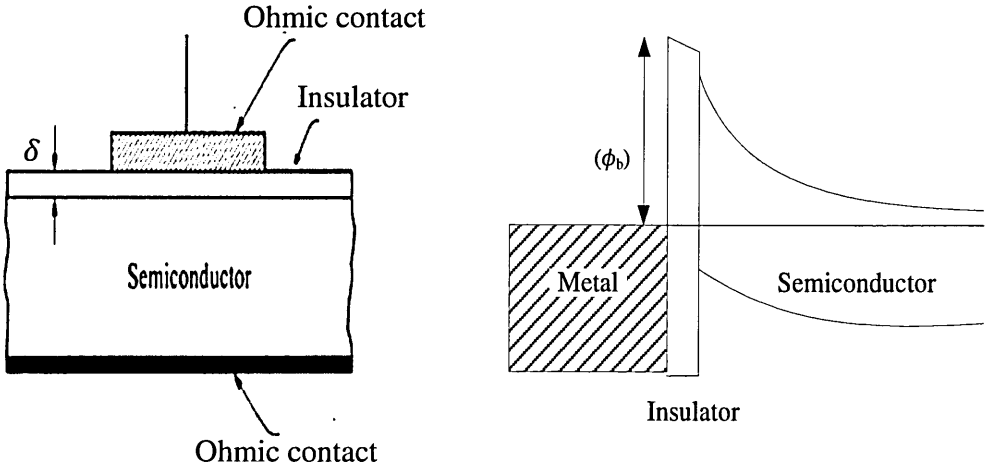


Figure 2-16: Schematic diagram of MIS structure incorporating an insulating layer between a metal and semiconductor to increase the potential barrier height.

2.6 Conclusions

Solid materials were introduced and are classified into three groups; conductors, semiconductors and insulators. The simple distinguishing property between these is the extend of the bandgap and the concentration of electrons in the solid material. Discussed also is the electrical conductivity type of material which was based on the position of the Fermi level within the bandgap of material.

Different semiconductor materials and which includes; p-n, pin and MIS junctions were discussed. Other interfaces introduced were Schottky, heterojunctions and graded bandgap structures. The understanding of these junctions and interfaces will help in no small measure in the understanding of solar cells and other semiconductor interface properties.

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Chapter 3: Experimental techniques used for growth and characterisation of materials and devices

3.1 Introduction

The structural, chemical, physical, optical and electronic properties of thin films are dependent upon the growth technique, condition of growth and growth thickness. Thin films technologies come with advantages such as the reduction of materials used for device fabrication unlike in the case of bulk semiconductors that require thicker layers in the order of hundreds of microns which is comparatively not cost effective considering the energy expended. Thin films range may vary from a few nanometres to tens of micrometres. Thin film technologies have been used in the deposition of various thin film materials for applications in semiconductor and other electronic devices such as in the fabrication of solar cells [1,2], gas sensors [3] and transistors [4].

Thin films deposition techniques are playing a key role in the advancement of thin films semiconductor and optoelectronic devices. Thin film growth technologies are basically group into physical vapour deposition (PVD) and liquid phase deposition (LPD). The PVD is a class of high temperature deposition techniques such as closed space sublimation (CSS), molecular beam epitaxy (MBE), sputtering etc. This class of deposition technique utilise high temperature vacuum system and are very expensive and complex while the LPD is low temperature growth techniques such as chemical bath deposition (CBD), electrodeposition (ED), spin coating etc. These techniques are simple and low-cost when compared with the vapour phase systems.

This chapter describes three important materials deposition techniques of CSS, CBD and ED involved in the growth of CdTe solar cells. However, ED is the growth technique of this research programme.

This chapter describes the growth techniques of CSS, CBD and ED. Electrodeposition (ED) is the growth technique used for the growth of all semiconductor materials in this thesis. This chapter also describes the necessary material characterisation techniques for their structural, optical, morphological and electrical properties. The last section present device characterisation techniques of I-V and C-V used to examine the performance of solar cell devices

3.2 Thin films growth techniques

This section outlines some important thin films deposition techniques used in the fabrication of optoelectronic devices especially solar cells as mentioned above. This section will mainly focus on the discussion of basic semiconductor growth techniques of close spaced sublimation (CSS), chemical bath deposition (CBD) and electrodepositions (ED) since general review is not possible.

3.2.1 Closed space sublimation

Closed space sublimation (CSS) is one of the physical vapour deposition (PVD) techniques used in the deposition of materials with usually high melting point. CSS is a well-known and widely used technique for the deposition of semiconductor compounds (e.g. CdTe). Figure 3.1 shows the schematic diagram of CSS deposition system. Important parameters in this deposition procedure are substrate temperature, source temperature, source/substrate spacing, pressure and ambient. The deposition process is done in such a way that the source materials are kept at higher temperature than the substrate (500-600)^{o}C [5] and the temperature difference between the source and the substrate is normally kept at between 50-100^{o}C. In this technique, the source material sublimes and condenses on the substrate which is usually placed at about 11 mm from the substrate [6].

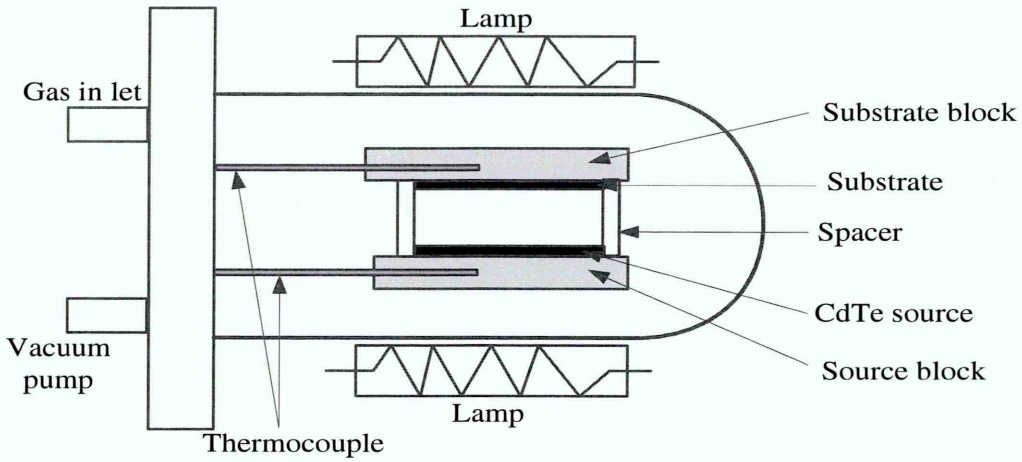

Figure 3-1: Schematic diagram of CSS deposition system. Redrawn from [8].

The deposition is usually carried out in an atmosphere containing inert gases such as Argon (Ar) filled through the gas inlet. During deposition, the constituent elements dissociate into its individual elements and recombine at the substrate surface. Before

deposition, the vacuum chamber pressure is pumped down to 10^{-1} Pa (10^{-3} mbar) using a rotary pump [7].

The chamber consists of source material (e.g. CdTe or CdS) and a substrate separated by quartz spacers. The source is placed on the source block at the underside and the substrate is placed above. The thermocouples attached to the two graphite blocks monitor the temperatures of the source and the substrate. The temperature difference between the source and the substrate is to enable diffusion controlled transport mechanism. The tungsten halogen lamps provide heating for the graphite blocks which in turn heat the source and the substrate [9]. The heating of the graphite blocks can also be done using electrical current (resistance heating) [8]. So far, CSS and its modified version are the best technique for growing high efficiency CdS/CdTe solar cells. In fact, it holds the highest record efficiencies for both lab scale (22.1%) and CdTe thin film module (18.6%) [10] using vapour transport deposition method. Apart from CdTe, this technique has been utilised in the deposition of a number of other semiconductor materials such as; CdS [11,12], ZnS [13], ZnTe [14] among others.

3.2.2 Chemical bath deposition

Chemical bath deposition (CBD) is a simple, low-cost and scalable semiconductor growth technique. It is found suitable in the deposition of numerous semiconductors. The layer deposition in this technique is based on a controlled chemical reaction from which a thin film layer is deposited by precipitation. For instance, if a substrate is immersed in an alkaline solution containing say ions of Cd and S then a solid layer of CdS layer can be deposited on the substrate if the ionic concentrations product (K_{IP}) of $[Cd^{2+}]$ $[S^{2-}]$ exceeds the solubility product (K_{SP}) of CdS [15]. The control of the rate of the release of ions is provided by a complexing agent added to the solution in a controlled manner. CBD process is affected by complexing agent introduced, pH and temperature, duration of the reaction, nature and concentration of reactants.

Figure 3.2 shows a typical CBD deposition Bath. CBD grown CdS is the most widely used in the manufacture of CdTe solar cells due to their compact and small grains nature. It also demonstrate smoother surface with less pinholes and good film adhesion. Another advantage of the CBD process is that it can grow on any contacting substrate irrespective of whether it is conducting or not and it can also deposit even on irregular shape substrates. The growth of the CBD process require a complexing agent that

controls the release of the metallic ions [15,16]. The layer thickness of CBD grown materials like CdS depends on the duration of growth.

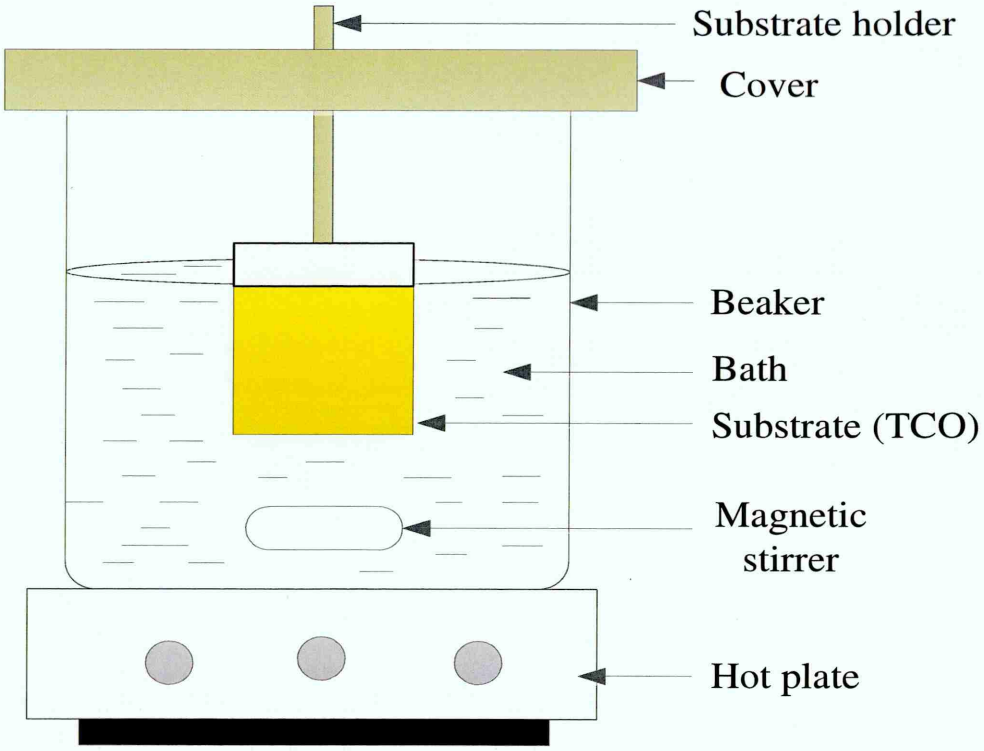

Figure 3-2: Schematic diagram of chemical bath deposition (CBD) set-up.

CBD technique has been in use for the deposition of semiconductors for over 100 years [15]. Using this process, numerous semiconductor materials have been deposited for use in various electronic applications especially in the development of solar cells. These includes CdS [17–19], ZnS [20], SnO_2 [21], ZnO [22], PbS [15], CdTe [23] among others. The main disadvantage of this technique is the production of large quantities of toxic waste (Cd-containing) from this batch process. Although the method is simple and low-cost, the toxic waste management in a manufacturing process could be very expensive.

3.2.3 Electroplating

Electroplating or electrodeposition (ED) is the process of depositing metals or compound semiconductors on a conducting substrate by passing electric current through an aqueous ionic electrolyte [24]. Electrodeposition technique is centred around Faraday's law which relies on electrolysing a metallic salt to reduce the metal cation at the cathode [25]. Conventional ED set up consist of deposition container (beakers), hot-plate, magnetic stirrer, cathode (working electrode), anode (counter electrode),

reference electrode, power supply, and deposition electrolyte. Figure 3.3 and Figure 3.4 are respectively the electrodeposition set-ups for three-electrode (3E) and two-electrode (2E) systems.

The 3E system is the conventional and widely used electrodeposition cell. A potentiostat provide and maintain the potential difference (p.d) between the working electrode (cathode) and the reference electrode. The reference electrode has a stable and well-known electrode potential and that is why it is used as reference in electrochemical cell for the control of potential and measurement [26]. The cathode (working electrode) is the conducting substrate electrode in the electrochemical cell on which the reaction of the semiconductor takes place or occurs (e.g. TCOs and metallic substrates). The counter electrode is usually an inert conductor (Pt or graphite) used to pass electric current to the electrolyte.

The 3E system is known to be a stable system since the voltage is measured between the cathode and the reference electrode because the concentration of the electrolyte in the reference electrode does not vary during deposition process. Two major and commonly used reference electrodes are Ag/AgCl electrode and SCE (saturated calomel electrode). The main concern in the 3E system is the possible leakage of Ag and K ions from the reference electrode into the deposition electrolyte [27]. The detrimental effect on CdS/CdTe solar cell of ions such as Ag was studied by Dennison in 1994 [28]. Since these ions are known p-type dopants hence can negatively affect the conversion efficiency of solar cell when n-CdTe is used as the absorber layer due to compensation process. Therefore, it is safer, if the reference electrode is omitted to benefit from advantages of simplifying the system, reduction of cost. Also, the omission of the reference electrode gives room for increase in the deposition temperature to (80-90)^{o}C, which is higher than the recommended operating temperature of the reference electrode which will increase films crystallinity. The reference electrodes have lower operating temperatures (~70^{o}C) based on the manufacturer's guide.

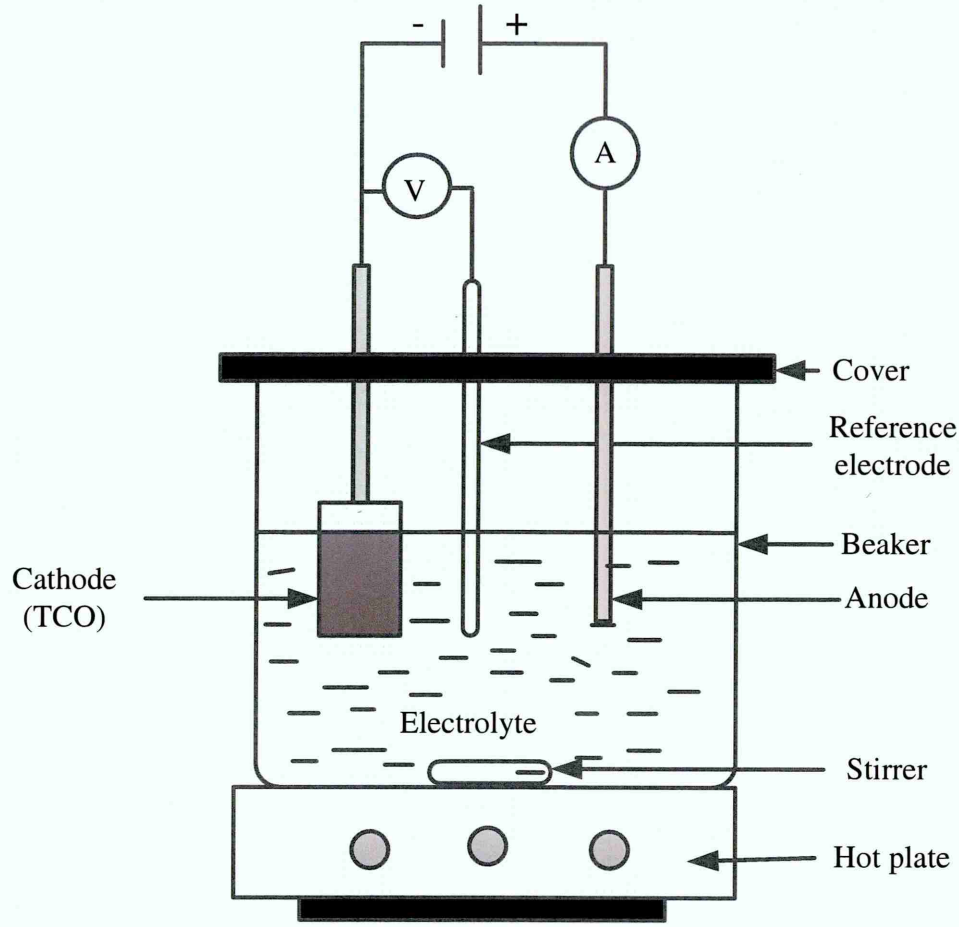

Figure 3-3: Three-electrode (3E) electroplating system set-up.

Figure 3.4 shows schematic representation of the 2E system set-up. The only difference between 3E and 2E systems is the omission of the reference electrode in the 2E system. Unlike in the 3E system, the potential in the 2E system is measured between the cathode and the anode. This could result to unstable potential due to possible voltage drop at the cathode surface. As mention earlier, the main advantages of the 2E system is system simplification, cost reduction since it does not require buying or replacing the reference electrode. In terms of device performance, experimental evidence have shown that all electrodeposited materials (CdS and CdTe) grown using 2E system can equally give high efficiency solar cells [1,2]. In a recent report on the comparison between 3E and 2E systems, literature have shown that both systems can produce electronic quality grade semiconductor materials for solar cell application [29,30].

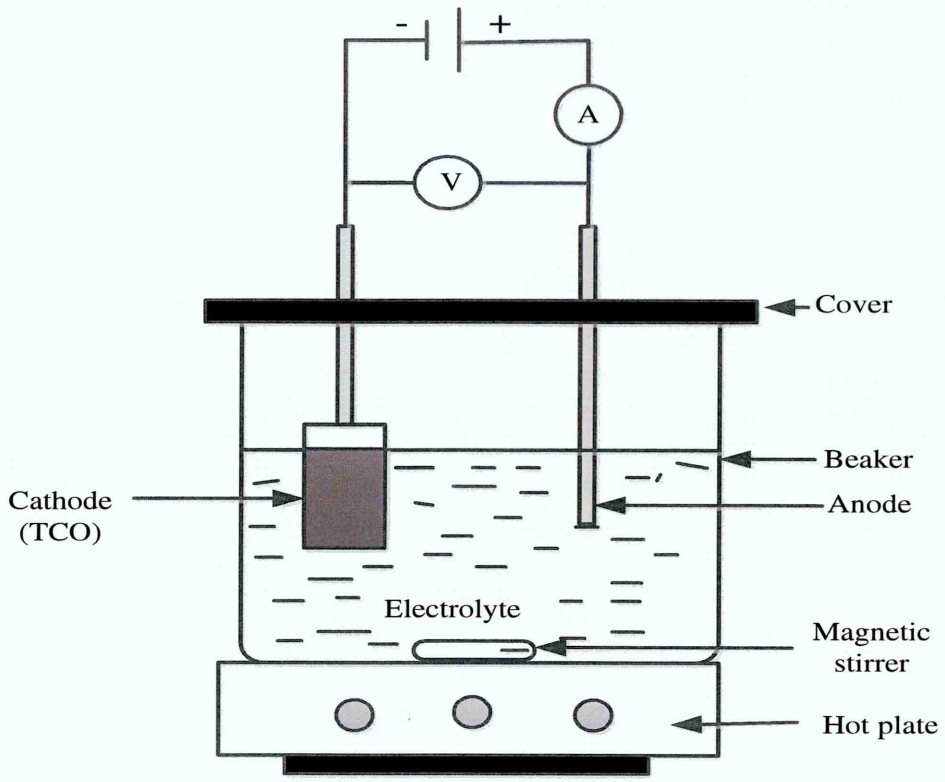

Figure 3-4: Two- electrode (2E) electroplating system set-up.

In ED, the thickness T (in cm) of the electrodeposited layers can be calculated using Faraday's law of electrolysis as given in equation 3.1.

$$T = \frac{JtM}{nF\rho} \qquad 3.1$$

where; n is the number of electrons transferred during deposition of 1 mole of the substance, F is the Faraday's constant (96485 $Cmol^{-1}$), A is the area (cm^2), I is the average current (A), t is the deposition time (s), M is the molar mass of the substance ($gmol^{-1}$), ρ is the density of the deposited material (gcm^{-3}).

Generally, electrodeposition is a simple, low temperature and continuous growth technique. This method can grow both n-type and p-type materials by simply changing the deposition voltage. Self-purification, minimum waste of materials, scalability and manufacturability are the other advantages of this technique [31]. Electrodeposition has been used for the deposition of electronic quality semiconductor materials for the fabrication of solar cells and other electronic devices. Using this technique, a large number of semiconductor materials have been successfully grown. These materials includes; CdTe [32–34], CdS [35–37], ZnS [38,39], CdSe [40], InSe [41,42], CIGS [43] among others.

3.3 Materials characterisation techniques

Owing to their vast application in the area of optoelectronic devices, thin films require careful characterisation using various analytical techniques so that important information on material properties can be analysed. These characterisations give the basic information of suitability or otherwise of a particular material for application in optoelectronic devices. Since information from one technique is not enough to optimise and assess the required material properties for solar cell application, several appropriate techniques should be used. This section will discuss on some important semiconductor characterisation techniques that provide information about their structural, optical, morphological and electronic properties.

3.3.1 X-ray diffraction

X-ray diffraction (XRD) is one of the basic and important techniques for structural studies of semiconductor materials including thin films. XRD is a non-contact and non-destructive technique based on the constructive interference of monochromatic X-rays reflected from a crystalline sample. Using this technique, important parameters such as phase identification, crystallinity, crystal structure and crystallites size can be determined. Figure 3.5 shows the X-ray diffraction machine set-up with the three basic components which include the X-ray source, sample holder and X-ray detector. The incident X-rays are provided by the X-ray source or X-ray tube and after interaction with sample, the diffracted rays are detected by the X-ray detector. As the sample rotate by an angle θ, the X-ray detector moves with angle 2θ.

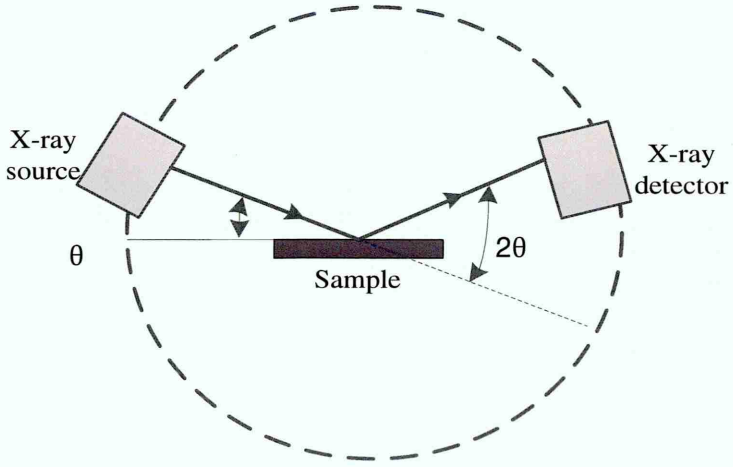

Figure 3-5: X-ray diffraction set-up to determine the structural properties of layers.

The principle of XRD is based on the constructive interference of X-rays diffracted by the atomic planes in a crystal. The intensity of the reflected X-rays is recorded by the detector as it rotates at an angle 2θ (see Figure 3.5). So that whenever the incident X-rays satisfy the Bragg's condition, constructive interference will occur and peak in intensity will occur as a result. According to Figure 3.6, the path difference between two adjacent beams is given by

$$2x = d\sin\theta \qquad 3.2$$

where d and θ are the inter-planar spacing and the angle between the atomic plane and the incident X-ray beam respectively.

If the Bragg's law holds, such that the path difference between the two interfering waves must be equal to a whole number n of wavelength, λ, then Bragg's law (equation 3.3) is satisfied and the angle at which it occurs is called Bragg's angle [44].

$$n\lambda = 2d\sin\theta \qquad 3.3$$

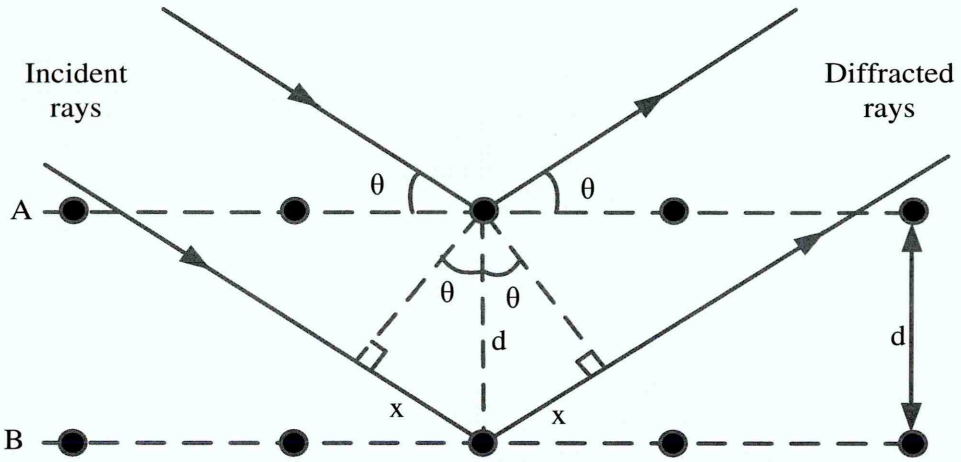

Figure 3-6: The principle of X-ray diffraction showing the reflection from two atomic planes in a crystal lattice.

The output XRD diffractogram is a plot of the X-ray counts as a function of the diffraction angle, 2θ as shown in Figure 3.7. The crystallite size is obtained by further analysis of the XRD peak. This is done by evaluating the full width at half maximum (FWHM), of the peak of interest. The crystallite size is calculated using Debye-Scherrer equation given in equation 3.4.

$$D = \frac{0.94\lambda}{\beta \cos\theta} \qquad 3.4$$

Where D is the crystallite size (in nm), λ is the wavelength of incident radiation (in nm), β is the full width at half maximum (FWHM) (in radian) and θ is the diffraction angle.

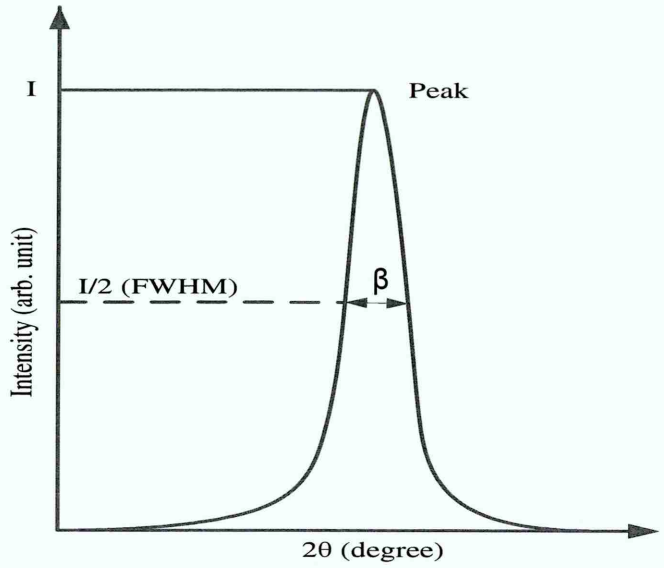

Figure 3-7: Typical XRD peak showing full width at half maximum (FWHM).

The XRD study was carried out by first running the XRD to obtain the diffraction pattern on the substrate on which the materials are coated. In this case, the diffraction pattern of a bare FTO glass substrate is used as a baseline before running the XRD on coated samples. The obtained diffraction pattern from the crystals of the coated sample is identified by comparing it with that of a standard single-phase material provided by the Joint Committee on Powder Diffraction and Standard (JCPDS). The main errors in XRD are mainly associated with the limitation of both the Scherer formula and the XRD machine.

In this research, Philip X'Pert Pro diffractometer (Philips analytical) with Cu-K_α radiation source with excitation wavelength of 1.541 Å was used for structural study of all films presented in this thesis. The source voltage and current are respectively 40 kV and 40 mA.

3.3.2 Raman spectroscopy

Raman spectroscopy (RS) is a convenient and non-destructive technique based on inelastic scattering of monochromatic light, usually from laser source [45]. Inelastic scattering in the sense that the frequency of the monochromatic light (photons) changes

when irradiated on a sample. From Figure 3.8, when a monochromatic laser light with initial frequency υ_i, is incident on a sample, it will excite the molecules and transform them into oscillating dipoles. These oscillating dipoles emit light with three different frequencies.

When photons with initial frequency υ_i are incident on a sample specimen, the photons are absorbed and scattered by the sample and most of the scattered photons falls back exactly to their initial vibrational level with the emission of photon with the same frequency υ_i, this is called *Rayleigh scatter* or elastic scattering (Figure 3.8 (a)). In this process, electrons are excited into higher energy levels (virtual state) and then fall back to its initial vibrational level with the emission of a scattered photon.

But inelastic scattering occurs when a very small fraction of the incident photons are scattered at different frequencies leading to a change or shift in the initial frequency of the incident photons [46]. This is called *Raman Effect*. This phenomenon was discovered in 1928 by C.V. Raman and K.S. Krishnan. The scattering may be due to change in vibrational or electronic energy of the molecule. Raman Effect can be elastic or inelastic in nature depending on the final frequency of the scattered photons.

If a photon with initial frequency υ_i is absorbed by a molecule and in the process transferred part of its energy to the molecule then the frequency of the scattered photon will reduced to υ_i-υ_f. This type of Raman scatter is called *Stokes frequency* [45] as shown in Figure 3.8(b). If on the other hand, the incident photons with initial frequency, υ_i is absorbed by a molecule which is in already excited vibrational level, then excess energy from the excited molecule is released and the molecule falls back to its original vibrational level with increased final frequency, υ_i+υ_f. This type of Raman is called *anti-Stokes frequency* [45] as shown in Figure 3.8(c).

Figure 3.8 shows schematic Raman transitional schemes. The energy difference between the incident and scattered photons is represented by arrows of different lengths.

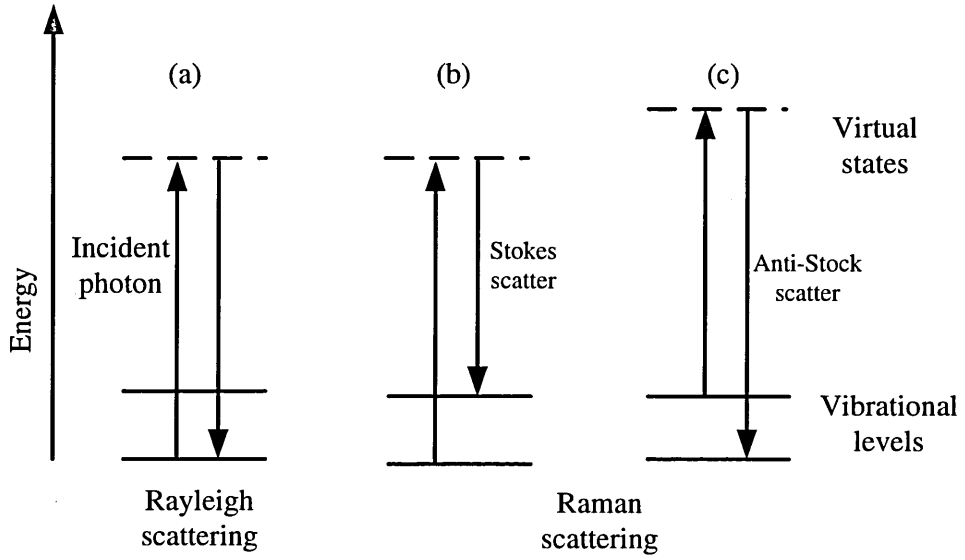

Figure 3-8: Schematic representation of the Raman transitional schemes (a) Rayleigh scattering (b) Stokes Raman scattering and (c) Anti-Stokes Raman scattering.

The main components of the Raman instrument are laser source, lens and mirrors, spectrometry and the detector. Raman spectroscopy can be conducted on solids, liquids and gases. The Raman studies presented in this thesis were carried out using Renishaw's Raman microscope with Argon ion laser wavelength 514 nm.

3.3.3 Photoelectrochemical cell measurement

It is necessary that the electrical conductivity type of a material be accurately known before use in any semiconductor or solar cell device fabrication [47]. Photoelectrochemical (PEC) cell measurement is a quick and simple way to check the electrical conductivity type of semiconductor materials. The ideal and conventional method to do this is by the Hall Effect experiment. However this experiment cannot be performed on materials grown using electrodeposition method due to the presence of transparent conducting oxide (TCO) substrate. And the option of layer isolation from the substrate is difficult and virtually impossible due to the strong layer/FTO adhesion. It is also important to note that, these layers are thin films with approximate thicknesses in the region (100-2000) nm hence; they are very easy to damage. Therefore, measurement using Hall Effect on these materials is not reliable since the electric current find the lowest resistive path. PEC cell has been a suitable alternative to carry out this experiment and the set-up of this technique is shown in Figure 3.9.

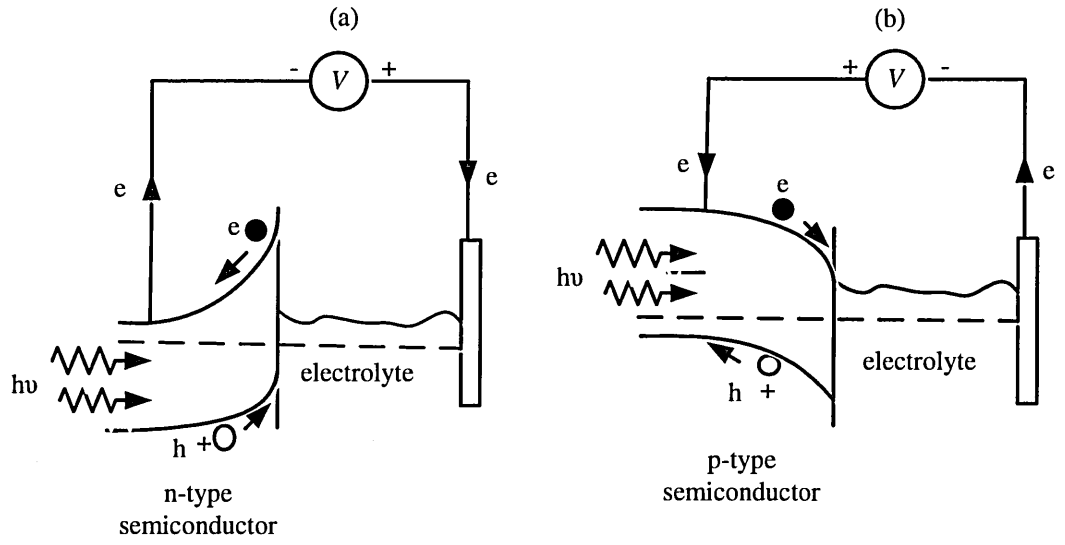

Figure 3-9: Schematic representation of the PEC cell arrangement showing solid/liquid interface behaviour for (a) n-type and (b) p-type semiconductors.

PEC cell technique is based on a solid/liquid junction such that when a semiconductor is immersed into a suitable electrolyte, a solid/liquid junction is formed at the semiconductor/electrolyte interface similar to a weak Schottky junction as shown in Figures 3.9(a) and 3.9(b). This contact result to the formation of band bending at the solid/liquid junction. The band bending geometry will be either upward or downward depending on the electrical conductivity type of the semiconductor material. If the junction is formed with n-type semiconductor, the band bending is upward as shown in Figure 3.9(a) and if the junction is made with p-type semiconductor, the band bending is downward as indicated by Figure 3.9(b). The voltage across the FTO substrate and the graphite rod is recorded using a voltmeter under dark and illuminated conditions. The difference between the voltage under illumination (V_L) and the voltage under dark (V_D) conditions gives the magnitude of the PEC signal and the sign of the PEC signal determine the conduction type of the semiconductor. Negative PEC signal indicate n-type semiconductor while positive PEC signal indicate p-type semiconductor. It is important that the PEC system is first calibrated with a material of known electrical conductivity to avoid misleading results. The opposite band bending nature in the PEC signal of the n-type and p-type semiconductors is similar to the observed differences in the band bending in the Schottky contact described in section 2.5.2 in chapter 2. In an n-type semiconductor, the electrons move into the bulk of the semiconductor while the holes move to the semiconductor surface and the reverse is the case for a p-type material. The magnitude of the PEC signal indicates qualitative idea about the doping concentration in the semiconductor material [48]. The electrolyte used in this thesis is

0.1 M $Na_2S_2O_3$ and each PEC signal is an average of 3 readings for all the PEC cell measurements presented in this research.

3.3.4 Direct current resistivity measurement

Direct current (DC) conductivity measurement is a simple technique used to determine the electrical resistivity (ρ) and conductivity (σ) of a semiconductor material using Ohm's law. The experiment is done by applying a variable DC voltage across two ohmic contacts to the semiconductor as shown in Figure 3.10. The applied voltage is usually from -1.0 V to +1.0 V with proportional increment in current and voltage. The results obtained from Figure 3.10 give a straight line passing through the origin when a graph of current vs. voltage (I-V) is plotted as shown in Figure 3.11. The slope of the straight line was used to calculate the resistance (R) while the conductivity (σ) of the semiconductor was calculated by applying Ohm's law given in equation 3.5.

$$R = \frac{\Delta V}{\Delta I} \qquad 3.5$$

The resistance R (Ω) and the electrical resistivity ρ (Ωcm) of a semiconductor are related by equation 3.6 [49].

$$R = \rho\frac{L}{A} \quad \text{and therefore} \quad \rho = \frac{RA}{L} \qquad 3.6$$

Where R is the resistance (Ω), ρ (Ω.cm) is the electrical resistivity, A is the cross-sectional area (cm^2) and L (cm) is the thickness of the semiconducting layer.

The electrical conductivity σ $(\Omega.cm)^{-1}$ of the semiconductor is obtained using equation 3.7 by taking the reciprocal of equation 3.6.

$$\sigma = \frac{1}{\rho} \qquad 3.7$$

The I-V measurements presented in this thesis were carried out using fully automated I-V system using Keithley 2401 source meter with power supply unit and solar simulator.

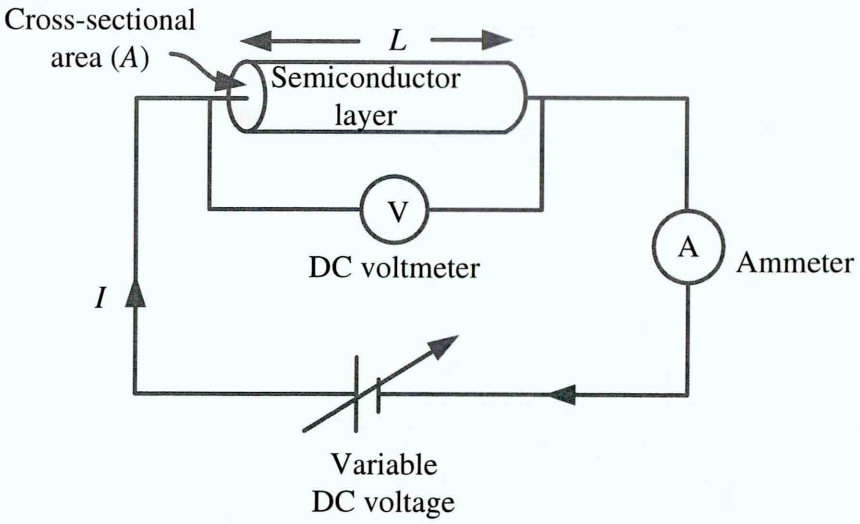

Figure 3-10: The electrical circuit used to measure I-V characteristics of a semiconductor with two ohmic contacts.

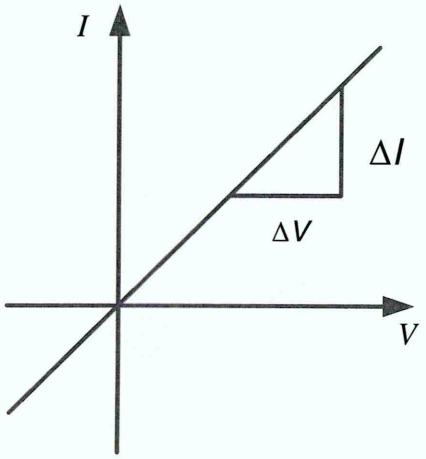

Figure 3-11: Typical I-V characteristics used to measure the resistance of a semiconductor.

3.3.5 Scanning electron microscopy

Scanning electron microscopy (SEM) is a technique employed to study the morphology of material surfaces. This technique reveals the pattern of grain arrangement, sizes of grains, grain boundaries and surface roughness. Figure 3.12 shows the schematic representation of SEM equipment. The main components of SEM equipment include the electron gun, the anode, lenses, scanning coils and objective lenses.

In SEM technique, the sample is placed on a sample stage in a chamber and the pressure of the chamber is pumped down to (10^{-5}-10^{-7}) mbar [50]. The electron gun, tungsten filament heats up to a temperature of about 2400°C, emit electrons that will be

accelerated towards the anode and through the magnetic lens where they will be focused to a small spot. The accelerating potential is in the range (1-30) kV [51]. These lenses also regulate the number of electrons that will fall on a sample specimen. While on transit through scanning coils, the electrons are deflected both horizontally and vertically before reaching the objective lens. The electron beam will further be directed to the sample specimen by the objective lens. When the beam finally hit the sample surface, electrons are then ejected from the sample and are detected by the secondary electron detector which now converts the signal to image of the sample surface.

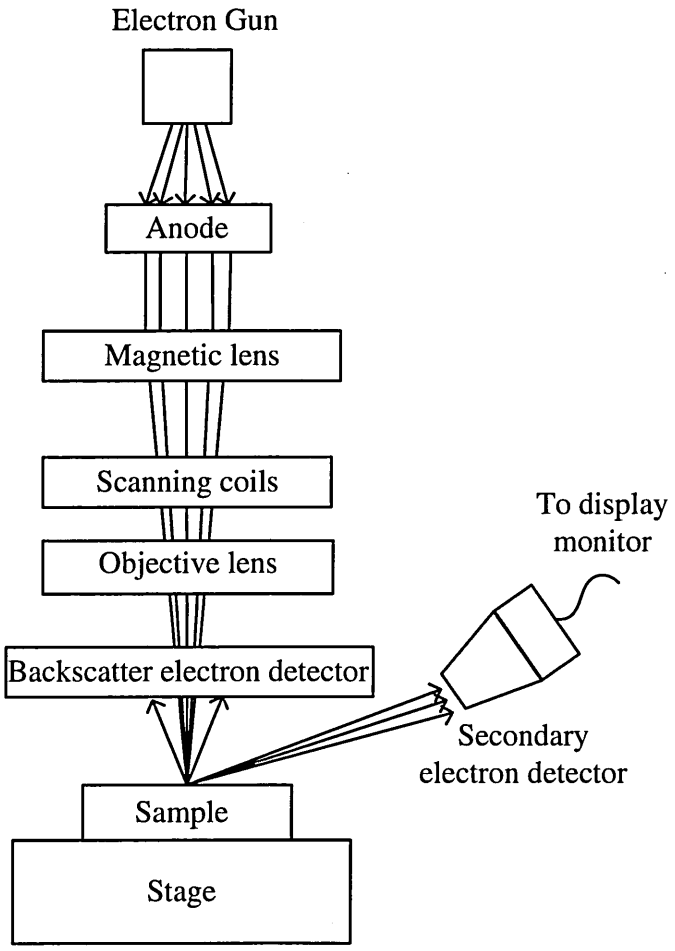

Figure 3-12: Schematic representation of the scanning electron microscope.

The interaction between the incident electron beam and the sample specimen results in the emission of different signals such as secondary electrons, backscattered electrons and X-rays. These signals are emitted at varying depth in the sample and the promotion of these signals depends on the initial energy of the impinging electron beam. The emitted electrons are detected by backscattered electron detector and the secondary electron detector. The high energy electrons resulting from the interaction of the incident electrons and the nuclei of the atoms are detected by the backscattered electron

detector. And the low energy electrons resulting from the interaction between the incident electrons and the electrons in the sample specimen are detected by the secondary electron detector. The detected electrons are converted to images that can be viewed on a computer monitor. The sample preparation for SEM measurement is to clean the sample so that good representation of the sample is obtained. Another thing is to make sure that the sample is electrically conducting since this involves the use of vacuum and electrons. For non-conducting sample, the sample needs to be made conducting by coating the sample surface with a very thin layer of gold (10-15) nm [52]. This research work used silver paint to connect the semiconducting layer with the metallic sample holder over the glass insulating substrate to avoid charging effect. [53]. The magnification of SEM can reach up to 100,000 [54]. All the SEM images presented in this thesis were acquired using FEI Nova 200 NanoSEM.

3.3.6 Optical absorption study

The determination of the optical properties of semiconductors for intended use in the fabrication of solar cell require some special optical properties of each material involved in the fabrication process depending on the role the material plays when incorporated in the device. In the basic structure of the CdS/CdTe solar cell, the CdS window layer should possessed properties such as high transmittance and low reflectance to allow for maximum incident photons to be transmitted to the device active junction. On the other hand the absorber CdTe material should possessed high absorption property such that all photons reaching it are fully absorbed for maximum PV action.

It is known that when light falls on a semiconductor material, part of it is reflected, part absorbed and part is transmitted through the semiconductor. Using this experiment parameters such as optical bandgap, transmittance and absorbance are obtained for full evaluation of the optical properties of materials based on their role when incorporated in solar cell devices. The light spectrum range can be adjusted to suit the semiconductor property under evaluation. Most materials are scanned in the wavelength range (200-800) nm which covers from the UV-Vis spectrum and may sometimes extend into the infrared region. The main components of a UV-Vis spectrometer includes, light source, monochromator, slit, sample holder and detector as shown in Figure 3.13.

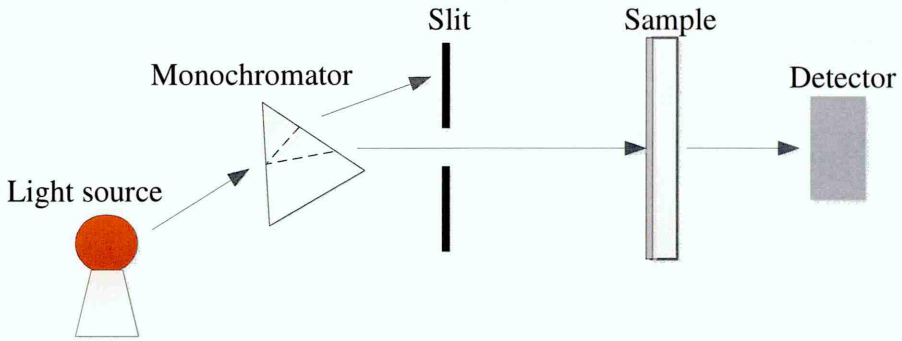

Figure 3-13: Schematic set-up of optical absorption measurement system. Redrawn from [55].

The schematic set-up diagram shown in Figure 3.13 is based on a single beam set up where the reference sample is first measured to get the baseline reading before the coated samples are measured. It can be seen that light from the source passes through the monochromator where the light is tuned and the desired wavelength is transmitted through the slit to the sample. If the energy of the incident light is equal to or greater than the bandgap of the semiconductor, the photons will be absorbed while transmitted light will be detected by a photodiode in the detector. The photodiode convert the light into electrical signal where it will be amplified then receive as output to be monitored on a screen. A default setting is provided in the software such that one can select absorbance, transmittance and reflectance depending on the need.

This experiment was mainly conducted to determine the energy bandgap (E_g) of the semiconducting materials reported in this thesis. The analysis of the bandgap of semiconductors is done using absolute absorption coefficient, $\alpha\ (cm^{-1})$ vs. hv (eV), from which bandgaps are obtained by extrapolating the straight line portion of the α curve to the photon energy (hv) axis (where $\alpha = 0$) [56]. The errors in this measurements was found to be ±0.02 eV (25 nm). This error was estimated by comparing the variations in the bandgaps of several samples grown using the same growth parameters. The bandgap can be estimated for both direct and indirect transitions according to Tauc relationship using equations 3.8.

$$\alpha = \frac{C\left(h\nu - E_g\right)^{\frac{n}{2}}}{h\nu} \qquad 3.8$$

where α is the absorption coefficient, C is a constant of proportionality and is material dependent, h is Planck's constant, υ is the frequency of the incident photon, E_g is the energy bandgap of the semiconductor and n takes the value of 1 for direct bandgap and

4 for indirect bandgap semiconductor. All the optical absorption measurements reported in this thesis were carried out using Cary 50 UV/Vis spectrophotometer.

3.3.7 Photoluminescence spectroscopy

Photoluminescence (PL) is a contactless and non-destructive technique employed to study defects distribution levels in the bandgap of semiconductor materials. In this experiment, photons are usually excited by a high energy light source from valence band to conduction band. Thereafter, these electrons are allowed to fall back to the valence band. While on transit back to the valence band, these electrons are trapped by defects at different energy levels which result in emission of light (luminescence) at different defect levels within the bandgap of the semiconductor as shown in Figure 3.14. But if on return, the transition is directly from the conduction band to valence band then the transition is said to be band to band transition and the emitted luminescence will correspond to the bandgap of the semiconductor material [57].

The finger prints of defect levels are studied by plotting the intensity of the PL spectra as a function of photon energy ($h\upsilon$).

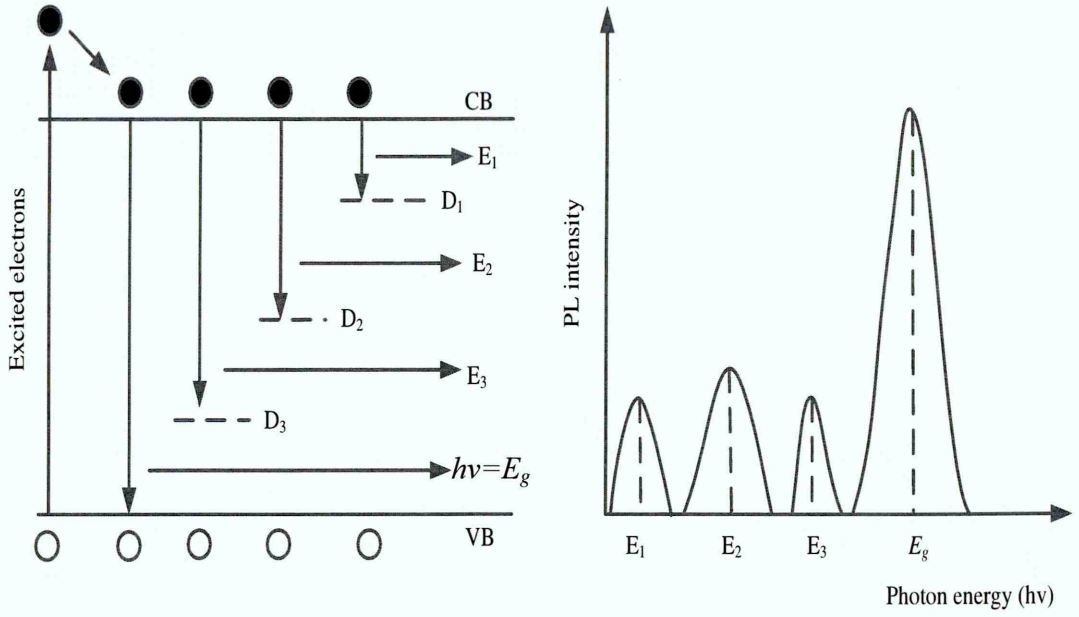

Figure 3-14: (a) Schematic illustration of the principle of PL showing defect levels D_1 to D_3 and (b) showing the intensities of the corresponding defect levels. Redrawn from [57].

The PL results presented in this thesis was carried out using Renishaw inVia Raman microscope with a 632 nm (~1.96 eV) He-Ne laser source. These measurements were

carried out at the Conn centre for the renewable research in University of Louisville, through our existing collaboration.

3.4 Device characterisation techniques

The fabricated solar cell devices in this research were characterised using (a) current-voltage (I-V) and (b) Capacitance-voltage (C-V) techniques. Measurements were carried out under dark and standard illumination conditions (AM1.5 illumination). An equivalent circuit of a practical solar cell device is presented in Figure 3.15. Using this Figure, important solar cell parameters under two different situations of dark and illumination conditions can be evaluated. This section outlines the basic solar cell device performance parameters under dark and illumination conditions.

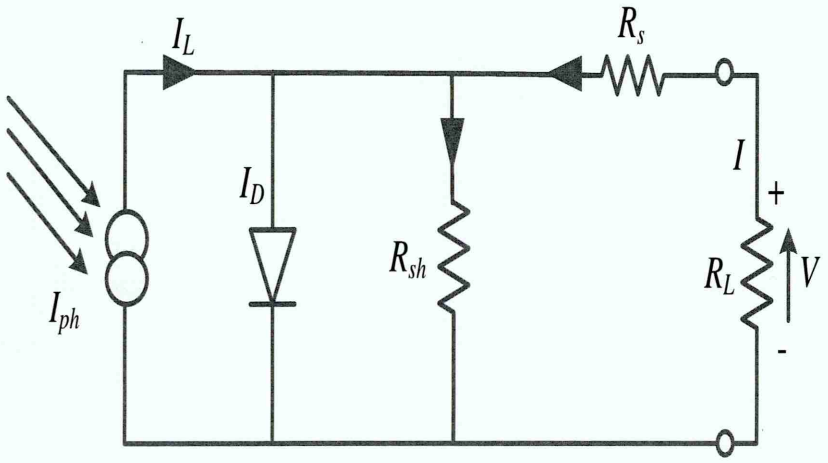

Figure 3-15: Equivalent circuit of a practical solar cell.

3.4.1 Current-voltage (I-V) characterisation

Current-voltage (I-V) is a very important characterisation technique as far as solar cell device assessment is concerned. It is the standard means by which the efficiency of solar cells are evaluated. Using this technique, solar cell parameters are measured under two different situations of dark and illuminated conditions. Under dark, parameters such as rectification factor (RF), ideality factor (n), saturation current (I_o), potential barrier height (Φ_b), series resistance (R_s), shunt resistance (R_{sh}) were measured while under illumination, parameters such as open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF), conversion efficiency (η), series resistance (R_s) and shunt resistance (R_{sh}) were obtained.

3.4.2 Device characterisation under dark condition

Dark current-voltage (dark I-V) measurements were normally carried out to analyse the electrical characteristics of solar cells which provides practical means of determining major performance parameters [58]. Solar cell devices normally behave like a rectifying diode when under dark conditions such that the flow of current is only in one direction with high current flow in forward bias and a very small or zero current is observed under reverse biased. Figure 3.16 shows the plots of log-linear and linear-linear for detailed study of the dark I-V behaviour of solar cells devices.

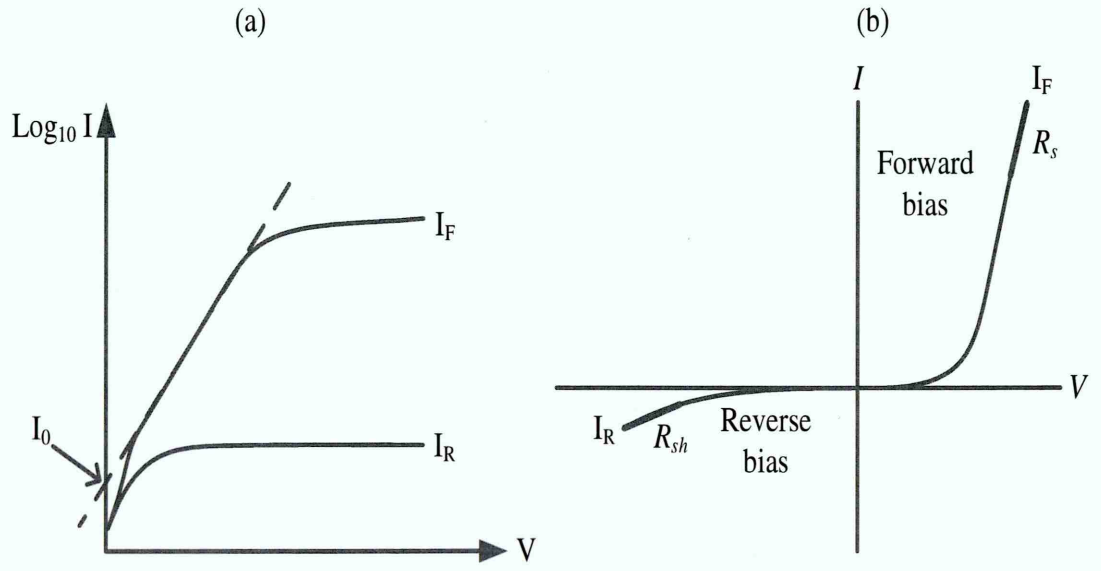

Figure 3-16: The plot of (a) log-linear and (b) linear-linear graphs for analysis of dark I-V characteristics of PV solar devices [59].

The current-voltage (I-V) behaviour of a rectifying Schottky diode is expressed using equation 3.9 [59].

$$I_D = SA^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \qquad 3.9$$

where I_D is the dark current (A), S is the diode contact area (m^2), A^* is the effective Richardson constant for thermionic emission ($Acm^{-2}K^{-2}$), T is the temperature in Kelvin, q is the electronic charge (1.602×10^{-19} C), ϕ_b is the potential barrier height, k is the Boltzmann constant (1.3806×10^{-23} JK^{-1}), n is the diode ideality factor, V is the applied voltage

with $I_o = SA * T^2 . \exp\left(\frac{-q\phi_b}{kT}\right)$ 3.10

equation 3.9, can be re-written as,

$$I_D = I_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad 3.11$$

When the applied voltage across the diode, V≥75 mV, the term $\exp\left(\frac{qV}{nkT}\right) \gg 1$, therefore equation 3.11 can simply take the form;

$$I_D = I_o . \exp\left(\frac{qV}{nkT}\right) \quad 3.12$$

Where I_o is the diode reverse saturation current

Taking the natural log of both sides of equation 3.12 gives;

$$\ln I_D = \left(\frac{qV}{nkT}\right) + \ln I_o \quad 3.13$$

Equation 3.13 is now converted to base ten log and take the form

$$\log_{10} I_D = \left(\frac{q}{2.303nkT}\right)V + \log_{10} I_o \quad 3.14$$

The graph of $\log_{10} I_D$ Vs. V, in equation 3.14 is given in Figure 3.16 (a) and enables the extraction of some important diode parameters such as *RF*, *n*, I_o and Φ_b.

The *RF* is the ratio of the forward (I_F) current to reverse (I_R) current (I_F/I_R) obtained at a particular voltage (e.g. at V=1.0 V). *RF* is the measure of the quality of the rectifying diode. Therefore, higher RF values are required for high performance solar cells, though an *RF* value of approximately 10^3 is sufficient for a high performance solar cell [59]. *RF* is evaluated using equation 3.15.

$$RF = \left(\frac{I_F}{I_R}\right)_{V=1.0} \quad 3.15$$

The diode ideality factor, *n* gives information about the nature of current transport through the diode [59]. It is obtained from the gradient of the extrapolated straight line

portion of the plot of $\log_{10} I_D$ Vs. V given in equation 3.14. The value of n can be calculated from equation 3.16. The current transport in ideal diodes is only by thermionic emission over the potential barrier with n value equal unity (1.00). However, where the depletion region and the interface is dominated by recombination and generation (R&G) centres, the current transport is dominated by R&G process and the value of n is 2.00. Since practical diodes are not ideal, both thermionic emission and R&G take place in parallel and n value is between 1.00 and 2.00 [59].

$$n = \left(\frac{q}{2.303kT}\right) \times \frac{1}{Gradient} \qquad 3.16$$

The n is also heavily affected by the diode series resistance (R_s) showing a linear relation. Therefore, large values of R_s reduce the gradient of the log-linear at the high forward current thereby increasing the value of n. Another reason for large n values could be due to tunnelling process in the device. For accurate values of n, I_o and other parameters, large gradient of the curve (Figure 3.16(a)) should be taken for accurate analysis. The I_o is expressed using equation 3.10 from which the Φ_b can further be evaluated using equation 3.17.

$$I_o = SA^*T^2.\exp\left(\frac{-q\phi_b}{kT}\right) \qquad 3.17$$

$$\phi_b = \frac{kT}{q}\ln\left(\frac{SA^*T^2}{I_o}\right) \qquad 3.18$$

From the linear-linear plot shown in Figure 3.16(b), important parameters such as series resistance (R_s) and shunt resistance can be extracted for further device analysis. The R_s is the total resistance of the contacts and that of the bulk of the semiconductor materials. The R_s value of a diode is determined from the slope of the highest forward current. Ideal diodes show zero R_s values (R_s=0). It is desirable to have low value of R_s for practical and efficient solar cell devices.

Shunt resistance (R_{sh}) is another important parameter that can be extracted from Figure 3.16(b) and is obtained from the reverse current portion. R_{sh} is defined as the resistance arising due to leakage path in the solar cell. Ideal solar cells should have infinite R_{sh} ($R_{sh}\rightarrow\infty$). However, large value of R_{sh} is required for an efficient solar cell.

3.4.3 Current-voltage (I-V) under illumination

Figure 3.17 shows the characteristics of solar cell under dark and illuminated conditions. The V_{oc} is the voltage measured under illumination condition when no current flows to the external circuit and it is determined from the x-intercept of the I-V under illumination. Short circuit current density I_{sc} is the current flowing through the device when the two contacts are short circuited. The magnitude of the I_{sc} depends on the incident light density. However, for easy comparison between devices of different contact areas, J_{sc} is usually used and the conversion is given in equation 3.19.

$$J_{sc} = \frac{I_{sc}}{S} \qquad 3.19$$

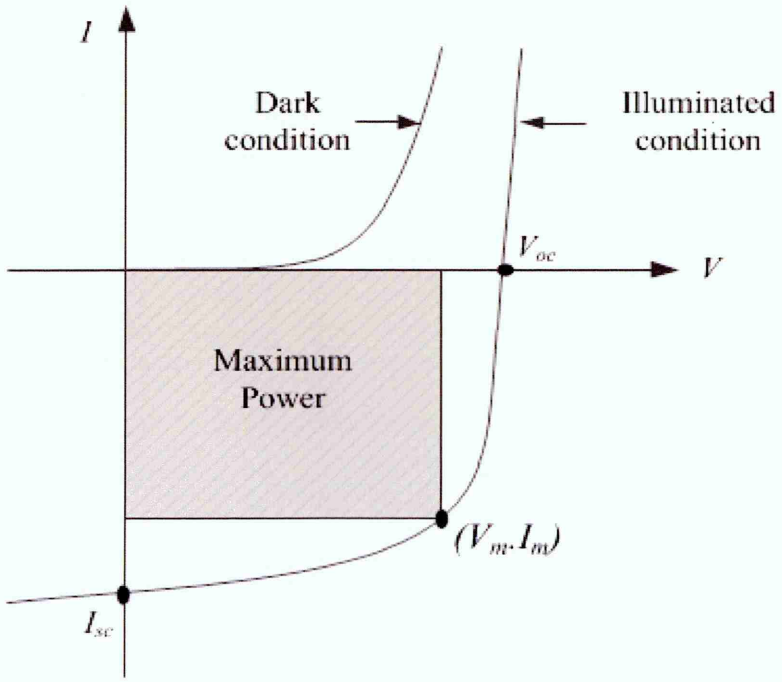

Figure 3-17: I-V characteristics of a solar cell under dark and illuminated conditions.

Fill factor (FF) is the fraction of electrical power that can be extracted from the solar cell given by equation 3.20.

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \qquad 3.20$$

where V_m and I_m are the parameters at maximum power extraction point $(V_m I_m)$ and the efficiency (η) is the solar to electric conversion efficiency defined as;

$$\eta = \frac{OutputPower}{InputPower} = \frac{V_m I_m}{P_{in}} = \frac{V_{oc}.I_{sc}.FF}{P_{in}} \qquad 3.21$$

where P_{in} is the power density of the incident radiation per unit area. Replacing I_{sc} by J_{sc}, equation 3.21 is re-written as [59].

$$\eta(\%) = \frac{V_{oc} J_{sc} FF}{P_{in}} \qquad 3.22$$

All Solar cell efficiencies in this thesis were measured under standard AM1.5 illumination conditions with P_{in} of 1000 Wm^{-2} (100 $mWcm^{-2}$).

The most important parameters crucial for solar cell development are obtained under illumination conditions from I-V characteristics as shown in Figure 3.17. Parameters obtained from this plot include open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF) and the efficiency (η). Other parameters like series resistance (R_s) *and* shunt resistance (R_{sh}) can also be measured under illumination. While the V_{oc} and the J_{sc} are directly obtainable from the I-V curve, the FF factor is obtained from the largest possible rectangle through the maximum power point voltage, V_m and current I_m as indicated in the graph (Figure 3.17). The efficiency, η of the device is obtained using equation 3.22. The R_s and R_{sh} are obtained from the highest forward and reverse current as previously explained.

With reference to Figure 3.15 the total current flowing into the solar cell is given by equation 3.23.

$$I_L = I_D - I_{ph} \qquad 3.23$$

Where; I_L is the total current in the diode, I_D is the diode current under dark condition and I_{ph} is the photo-generated current under illumination condition. Substituting equation 3.11 into 3.23, we have,

$$I_L = I_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] - I_{ph} \qquad 3.24$$

The combine plot of equations 3.11 and 3.23 is given in Figure 3.17. When no external current flows through the device, then I_L=0 and $V = V_{oc}$. Equation 3.24 becomes,

$$0 = I_o\left[\exp\left(\frac{qV_{oc}}{nkT}\right)-1\right]-I_{ph} \qquad 3.25$$

Substituting equation 3.10 into equation 3.25 and rearranging we now have;

$$SA^*T^2.\exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV_{oc}}{nkT}\right)-1\right]=I_{ph} \qquad 3.26$$

By rearranging and replacing I_{ph} with short circuit current, I_{sc} equation 3.26 will then be expressed in short circuit current density, J_{sc} ($J_{SC}=\frac{I_{sc}}{s}=\frac{I_{ph}}{s}$).

Taking the natural log of both side of equation 3.26 we have;

$$\ln\exp\left(\frac{-q\phi_b}{kT}\right).\ln\exp\left(\frac{qV_{oc}}{nkT}\right)=\ln\exp\left(\frac{J_{sc}}{A^*T^2}\right) \qquad 3.27$$

$$\frac{q}{kT}\left(\frac{-\phi_b}{1}+\frac{V_{oc}}{n}\right)=\ln\left(\frac{J_{sc}}{A^*T^2}\right) \qquad 3.28$$

Therefore, the V_{oc} of the solar cell is expressed by equation 3.29;

$$V_{oc}=n\left[\phi_b+\frac{kT}{q}.\ln\left(\frac{J_{sc}}{A^*T^2}\right)\right] \qquad 3.29$$

It is seen that the V_{oc} of the device is dependent on the values of n, ϕ_b, J_{sc} and T. This shows that high n values are required to obtain high V_{oc} values. However, high n values (say >2.00) affect negatively the performance of the solar cell. This is because high n values indicate R&G in the device which is known to hinder efficient separation of photo-generated charge carriers to the external circuit. This situation leads to low J_{sc} and V_{oc} values. It is therefore, desirable to have n values in the region of 1.00-2.00 for efficient solar cells [59]. High barrier height can also yield high V_{oc} values. The incorporation of thin insulating layer at the metal/semiconductor interface is one option used to increase barrier height and the n value of a solar cell. The operating temperature of the solar cell also affect V_{oc} that is, the higher the T, the lower the V_{oc} and vice versa.

3.5 Capacitance-voltage (C-V) measurement

Capacitance-voltage measurement is a technique to determine important parameters of semiconductors such as doping density, potential barrier height, junction depletion width and indirectly conductivity type of the semiconductor [60]. The electron hole pairs existing in a *p-n* or Schottky junction are synonymous to parallel plate capacitors. The charged layers generated at the junction due to potential barrier formation are called the junction capacitance. The junction capacitance, C of a depletion region is given by the equation 3.30.

$$C = \frac{\varepsilon_s A}{W} = \frac{\varepsilon_o \varepsilon_r A}{W} \qquad 3.30$$

Where; $\varepsilon_s = \varepsilon_o \varepsilon_r$ is the permittivity of semiconductor (Fcm^{-1}), ε_o is the permittivity of free space (8.85×10^{-14} Fcm^{-1}), ε_r is the relative permittivity of the semiconductor material, A is the cell contact area, W is the width of depletion region (cm), When the capacitance is expressed in capacitance per unit area (C_A), the equation 3.30 can be re-written

$$C_A = \frac{C}{A} = \frac{\varepsilon_S}{W} \qquad 3.31$$

The depletion width, W for an abrupt p^+-n junction is given by,

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN}} \qquad 3.32$$

Substituting equation 3.32 into equation 3.31,

$$\frac{C}{A} = \frac{\varepsilon_s}{\sqrt{\frac{2\varepsilon_s V_{bi}}{qN}}} \qquad 3.33$$

$$C_A = \sqrt{\frac{qN\varepsilon_s}{2V_{bi}}} \qquad 3.34$$

Equation 3.34 holds when there is no externally applied voltage. However, when an external voltage is applied across the junction, the total potential across the junction is modified to $(V_{bi} - V)$. Where V is positive for forward bias and negative for reverse bias. Therefore, equation 3.34 becomes;

$$C_A = \sqrt{\frac{qN\varepsilon_s}{2(V_{bi} - V)}} \qquad 3.35$$

$$C_A = \sqrt{\frac{qN\varepsilon_s}{2}}(V_{bi} - V)^{-\frac{1}{2}} \qquad 3.36$$

The N in equation 3.35 represents the uncompensated doping density. For n-type semiconductor, $N = N_D$-N_A and $N = N_A$-N_D for p-type semiconductor. Figure 3.18 shows the graph of C_A versus applied voltage, V. The capacitance per unit area (C_o) at zero bias ($V = 0$) indicates the depletion capacitance at zero bias. The obtained C_o value from this graph is used to calculate the depletion width using equation 3.30.

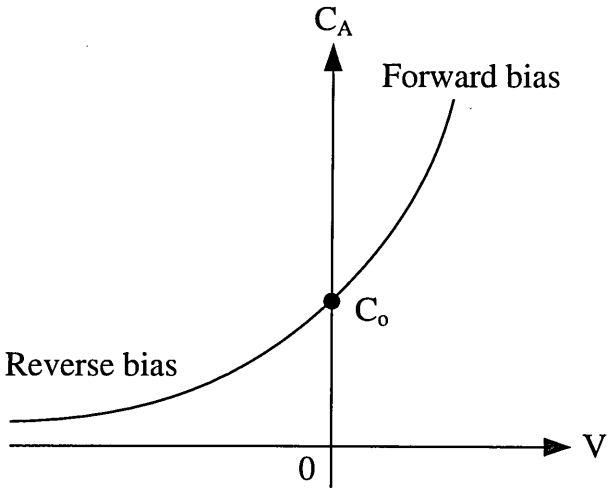

Figure 3-18: Typical plot of C_A vs. V characteristics of a solar cell showing forward and reverse bias regions.

To calculate doping concentration (N_D-N_A) and built-in potential (V_{bi}) further evaluation of equation 3.35 is required. This can be rearrange to give,

$$\frac{1}{C_A^2} = \frac{2}{qN\varepsilon_s A^2}(V_{bi} - V) \qquad 3.37$$

The Mott-Schottky or the plot of $1/C^2$ *vs.* V from equation 3.37 is shown in Figure 3.19. From this Figure, doping concentration (N) and the built-in potential (V_{bi}) can be extracted. The quantity ($2/q\varepsilon_s NA^2$) represents the slope of the Mott-Schottky plot which was used for the determination of the doping concentration of the devices while the intercept on the V-axis give the built-in potential (V_{bi}) of the device [61]. The N in equation 3.36 represents the uncompensated doping concentration of the semiconductor.

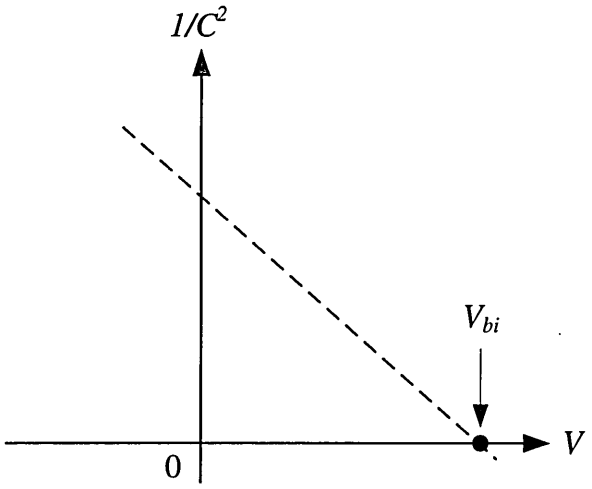

Figure 3-19: Mott-Schottky plot for an ideal diode showing the V_{bi} on the intersection of the V-axis where $1/C^2 = 0$.

All C-V measurements in this research were carried out using Hewlett Packard 4284A-20 Hz - 1 MHz precision LCR meter instrument. Measurements were done using a high frequency of 1 MHz with AC voltage of 50 mV at room temperature under dark condition in a parallel mode. At high frequency of 1 MHz, it is difficult for the surface states to follow the variation of the A.C. signal [62] and a relatively smoother curve is obtained.

3.6 Conclusions

Thin films deposition and characterisation techniques have been outline in this chapter. In the thin films deposition techniques, only three growth techniques of CSS, CBD and ED were discussed. The CSS growth technique is a high temperature vapour phase growth technique while CBD and ED are low temperature liquid phase growth techniques.

Each of the above mentioned growth technique has its own advantages and disadvantages depending on need and area of application. In the high temperature vapour phase deposition techniques, vacuum systems are required for the deposition process making the system complex and very expensive relative to the liquid phase techniques. However, they produce high quality thin films relative to the other deposition techniques.

The liquid phase deposition techniques such as electroplating and chemical bath deposition are low-cost and favours large area scaling up. In the PV field, the most

important factors for the production of solar panel is the reduction of cost, reproducibility, scalability and manufacturability.

In the device characterisation section, fully fabricated devices were characterised using I-V and C-V techniques. This is performed to study the electronic behaviour of the solar cells under investigation. Study using I-V measurements reveals information that helps to optimised growth and device processing procedure. The doping concentration of the devices was calculated from the C-V measurement.

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Chapter 4: Growth and characterisation of In_xSe_y layers

4.1 Introduction

Indium selenide (In_xSe_y) is a layered III-VI semiconductor with a direct energy bandgap of 1.80 eV at room temperature [1]. However, the bandgap is tunable depending on the growth and post growth processes. The basic structure of In_xSe_y layers were made from two *In* and two *Se* sublayers and the interlayer (Se-Se) bonding is of the Van der Waals type. Due to this bonding structure, there exist less dangling bonds at the surface which provides ideal condition for fabricating metal-semiconductor or p-n hetero-junctions. Thus, the interfaces between such layered materials are unstrained even for the relatively high lattice mismatches [2]. In_xSe_y is a complicated system due to its multiphase nature. It can exist in different phases such InSe, In_2Se_3, In_4Se_3 and In_6Se_7 [3]. In_xSe_y can exist in both n-type [4,5] and p-type [1,6] in electrical conduction depending on the growth conditions. This material is attractive due to its optoelectronic properties and have found applications in areas such as solar cells [2,7], switching devices [8], radiation detectors [9] and gas sensors [10]. In_xSe_y is deposited using variety of techniques such as Bridgeman-stocberger [5], electrodeposition [11], and thermal evaporation [12] among others.

The low density of dangling bonds on the surface of layered semiconductors such as In_xSe_y and GaSe makes them very good materials for the fabrication of hetero-junction devices [13] with minimum lattice mismatch [14–16]. Cadmium sulphide (CdS) is up to now the best hetero-junction partner in both CIGS and CdTe-based solar cells. The incorporation of CdS as a buffer/window layer in both device structures yielded efficiencies in excess of 21% [17]. However, due to health and environmental issues, it is important to replace CdS with less toxic alternative buffer materials such as ZnSe, $ZnIn_xSe_y$ and In_xSe_y. Gordillo and Calderon incorporated In_xSe_y in ZnO/InSe/CIS/Mo solar cell structure achieving 9.2% efficiency, Konagai *et al.* [18] incorporated In_xSe_y as a buffer layer in ZnO/In_xSe_y/CIGS solar cell with cell efficiency of 13%. This indicates why In_xSe_y will be very good candidate for incorporation as buffer layer in multi-layer graded bandgap devices based on CdTe solar cells.

This chapter presents the growth and characterisation of In_xSe_y thin film layers. After growth, the films were characterised for their structural, optical, morphological and electrical properties for full optimisation process. The films were characterised using available material characterisation techniques in the Materials and Engineering Research Institute (MERI) of Sheffield Hallam University.

4.2 Preparation of In_xSe_y deposition electrolyte

The electrolyte for the deposition of In_xSe_y was prepared from 0.1 M $InCl_3$ of purity 5N (99.999%) and 0.025 M SeO_2 of purity 5N (99.999%) which are the sources of indium (In) and selenium (Se) respectively. The chemicals were dissolved in 200 ml aqueous solution of deionised water. The pH of the electrolyte was adjusted to 1.50±0.02 at room temperature using HCl or NH_4OH. The temperature of the bath was set at ~40°C before deposition. All chemicals and substrates were purchased from Sigma-Aldrich, UK.

To remove grease and other contaminants on the glass/FTO substrates, they were first washed with soap solution and rinsed in deionised water. Then the substrates were clean with methanol followed by deionised water. The working electrode (glass/FTO) was attached to a carbon rod using polytetrafluoroethylene (PTFE) tape while the anode is a high purity carbon rod and the two electrodes were suspended vertically inside the electrolyte during deposition. The deposition was done in aqueous acidic solution using 2-electrode system in a cathodic mode. The heat was provided by hot plate with attached stirring system and the source of power was a Gill AC potentiostat (ACM instrument).

4.3 Results and discussion

4.3.1 Cyclic voltammetry

In electrodeposition, the cyclic voltammetry is a tool used to approximate the deposition window for a near stoichiometric material. Figure 4.1 depicts the current-voltage (I-V) relationship (voltammogram) obtained for the reduction of In_xSe_y compound on glass/FTO cathode. The temperature of the bath was set to ~40°C, and the voltammogram was recorded for voltage range from zero to 2000 mV and back to zero with scan rate of 3 mVs^{-1}.

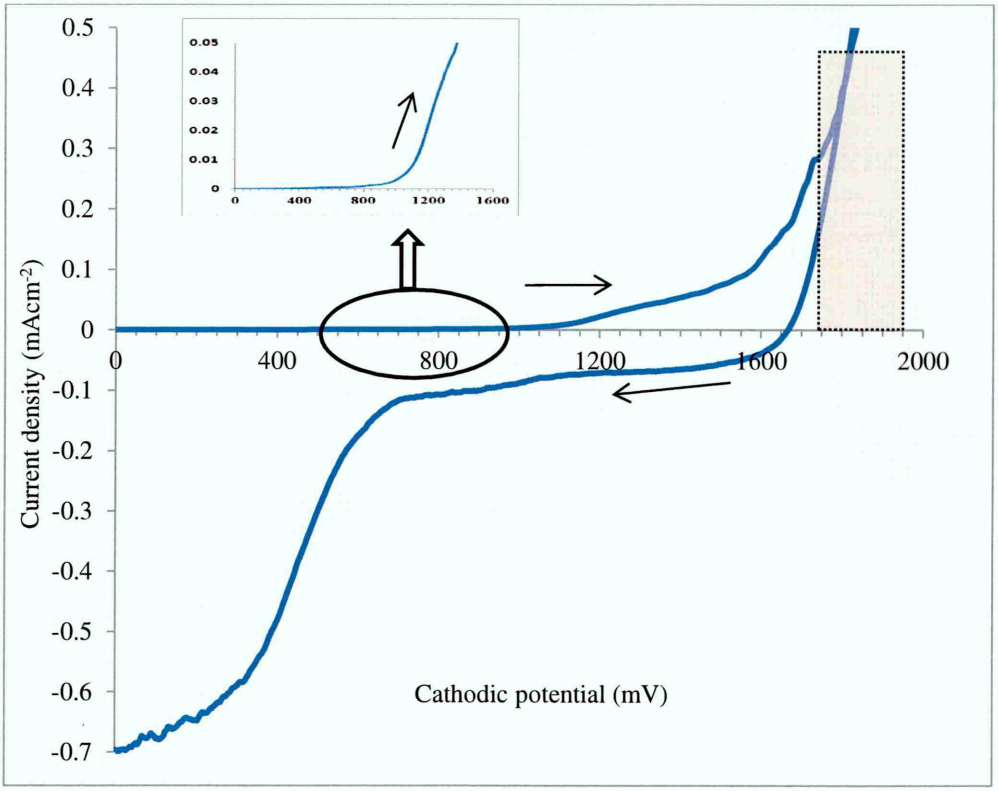

Figure 4-1: Cyclic voltammogram of aqueous solution containing 0.1 M $InCl_3$ + 0.025 M SeO_2, with glass/FTO cathode and graphite anode. The pH and temperature of the electrolyte were 1.50±0.02 and ~40°C respectively.

Looking at Figure 4.1 and with reference to the reduction potentials of the constituent ions, (E^0 of Se=+0.740 V, and E^0 of In=-0.338 V) [19], Se will starts to reduce on the cathode at voltage around 550 mV as is clearly seen from the inset diagram of Figure 4.1. A steady increase in deposition current from cathodic voltage around 1000 mV could be due to the incorporation of *In* on the cathode. This means that *Se* with the low reduction potential is first deposited at low cathodic voltages while *In* with the higher reduction potential will reduce at higher cathodic voltages. The approximate deposition potential for near stoichiometric In_xSe_y is expected in the voltage range (1700-1950) mV as indicated by the shaded portion of the voltammogram. At larger cathodic voltages, *In* is reduced instead of the desired In_xSe_y. This voltage region was avoided due to poor film quality which as a result cannot withstand device processing procedures.

During the reverse cycle process, elemental *In* and *In* from In_xSe_y starts to dissolve into the electrolytic bath at low cathodic voltages around 1650 mV. At this cathodic voltage, the deposition current becomes equal to dissolution current. The negative broad peak at

cathodic voltage around 300 mV can be attributed to the dissolution of *Se* from the glass/FTO cathode.

4.3.2 X-ray diffraction

The structural properties of the In_xSe_y layers were studied using X-ray diffraction (XRD) in the 2θ range (20-70)°. This work was carried out by growing In_xSe_y layers for one hour on glass/FTO substrate at different growth voltages within the identified approximate deposition voltage obtained from the voltammogram scan. Ten In_xSe_y layers were grown at different growth voltages in step of 10 mV in order to find near stoichiometric growth voltage range for the deposition of In_xSe_y semiconductor thin films. After growth, the samples were cleaned with deionised water and dried in air.

The as-deposited sample at each of the ten growth voltages was divided into 2 samples. The first set of ten samples was left as-deposited (AD) and the other set annealed at 300°C for 10 minutes in air. The layers were then cleaned with deionised water and dried in air. Figure 4.2 shows the XRD spectra for (a) as-deposited and (b) annealed In_xSe_y layers grown at different growth voltages close to the transition or inversion voltage (V_i).

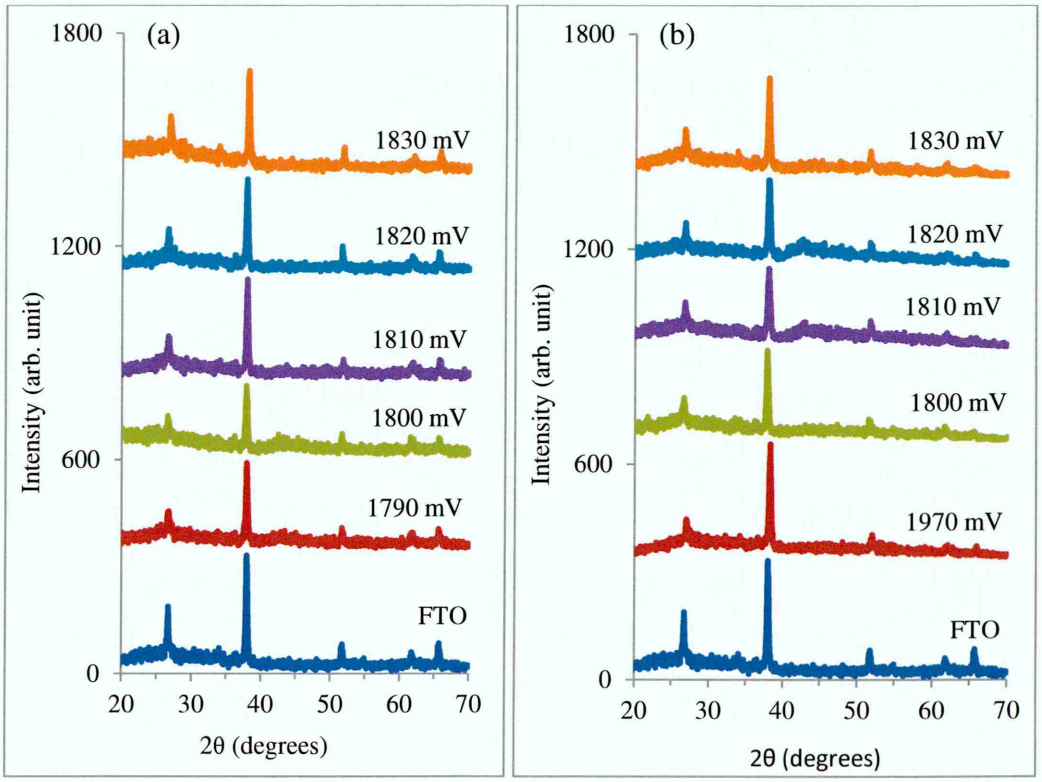

Figure 4-2: XRD patterns for (a) as-deposited and (b) annealed In_xSe_y layers grown at different growth voltages. Annealing was carried out at 300°C for 10 minutes in air.

The V_i voltage in this case was found to be ~1810 mV as will be discuss later under the PEC cell measurements in this chapter. The V_i, is the voltage at which the conductivity type of the material changed from p-type to n-type or vice versa. The XRD spectrum for the glass/FTO substrate was included in both as-deposited and annealed samples for easy comparison. Results from both as-deposited (Figure 4.2(a)) and annealed (Figure 4.2(b)) show that the material is amorphous with no In_xSe_y related peaks. All observed peaks are due to the underlying glass/FTO substrate under the growth conditions used in this experiment. The growth of both polycrystalline [3,20] and amorphous [6,21] In_xSe_y has been reported in the literature.

4.3.3 Optical studies

4.3.3.1 Effect of growth voltage on the optical bandgap of In_xSe_y layers

This investigation was carried out to study how the variation of growth voltage affects the bandgap of the In_xSe_y layers. Three In_xSe_y layers were grown on glass/FTO substrate at three different growth voltage of 1790, 1810 and 1820 mV. After growth, the samples were rinsed with deionised water and dried. Thereafter, the as-deposited sample grown at each growth voltage was divided into two. The first set of three samples was left as-deposited and the other set of three samples was annealed at 300°C for 10 minutes in air. The bandgaps of the layers in both as-deposited and after heat treatment were estimated using Tauc method [22] from the plot of absorption coefficient versus photon energy (α vs. hv) and by extrapolating the straight line portion of the absorption coefficient (α) to photon energy (hv) axis (at α=0).

Figure 4.3 shows respectively the absorbance vs. wavelength for (a) as-deposited and (b) annealed In_xSe_y layers at different growth voltages. It is observed that absorption of the layers increases with increase in growth voltage. The highest absorbance is observed in layer grown at growth voltage of 1820 mV while the least absorbance is found in layer grown at 1790 mV.

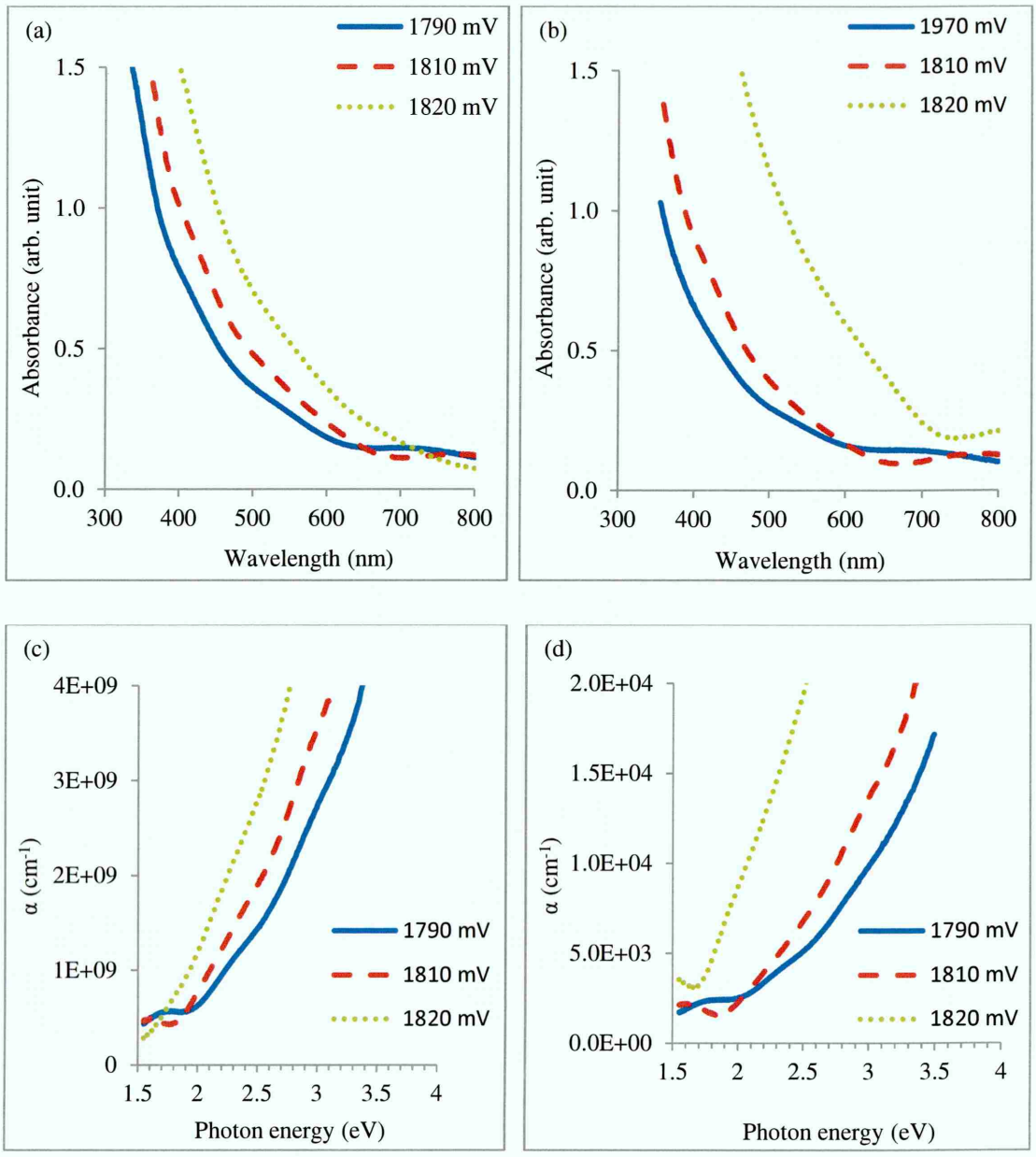

Figure 4-3: Optical absorbance spectra (A vs λ) for (a) as-deposited and (b) annealed In_xSe_y layers while (c) and (d) are their corresponding α vs hν graphs. Annealing was carried out at 300°C for 10 minutes in air.

Figure 4.3(c) and 4.3(d) illustrate absorption coefficient vs. photon energy (α vs hν) for as-deposited and annealed samples respectively. The estimated bandgaps in the as-deposited samples grown at 1790, 1810 and 1820 mV are 2.30, 2.00 and 1.90 eV respectively. It is observed that, the bandgaps of the layers were affected by varying the growth voltage such that the bandgaps were seen to decrease with increase in the growth voltage. This could be due to incorporation of more metallic indium on the cathode thereby reducing the bandgap as observed in the as-deposited layers.

After annealing the layers, their bandgaps shift to 2.50, 2.10 and 1.60 eV for layers grown at 1790, 1810 and 1820 mV respectively. Similar bandgaps were reported for In_xSe_y thin films [23].

The structural and optoelectronic properties of materials are dependent on parameters such as layer thickness, annealing temperature and annealing time. One of the advantages offered by electrodeposition as a semiconductor growth technique is the ease in the control of growth parameters. The achievement of wide bandgap In_xSe_y layers in this research will further improve the optical absorption in solar cells when this layer is used as a buffer layer in different solar cell structures.

4.3.4 Variation of thickness with growth time for In_xSe_y layers

The knowledge of layer thickness in photovoltaic device development is crucial as film thickness affect device performance especially in thin film solar cells. In this research, In_xSe_y is majorly used as a buffer layer hence it requires careful optimisation of its thickness to achieve desired optoelectronic properties for application as a buffer layer avoiding window absorption. It is for this reason that thicknesses of these layers were carefully tuned so that optimum performance can be achieved avoiding possible pinholes formation. It is known that the creation of pinholes in the window layers can adversely affect all device parameters [24] in solar cells. Therefore careful optimisation of layer thicknesses of In_xSe_y layers were experimentally estimated using UBM microfocus optical depth profilometer (UBM, Messetecknik GmbH, Ettlingen, Germany). The measurement error in this instrument is $\pm$50 nm.

Figure 4.4 shows the variation of In_xSe_y layer thickness vs. growth time. The results shows that film thickness increase with increase in growth time as expected. The plot of layer thickness vs. growth time show approximately linear relationship. It is observed that a layer thickness of ~450 nm will be grown in one hour. However, it is also important to note that layer thickness can be affected by parameters such as deposition current density, pH, growth time, concentration of ions and growth temperature.

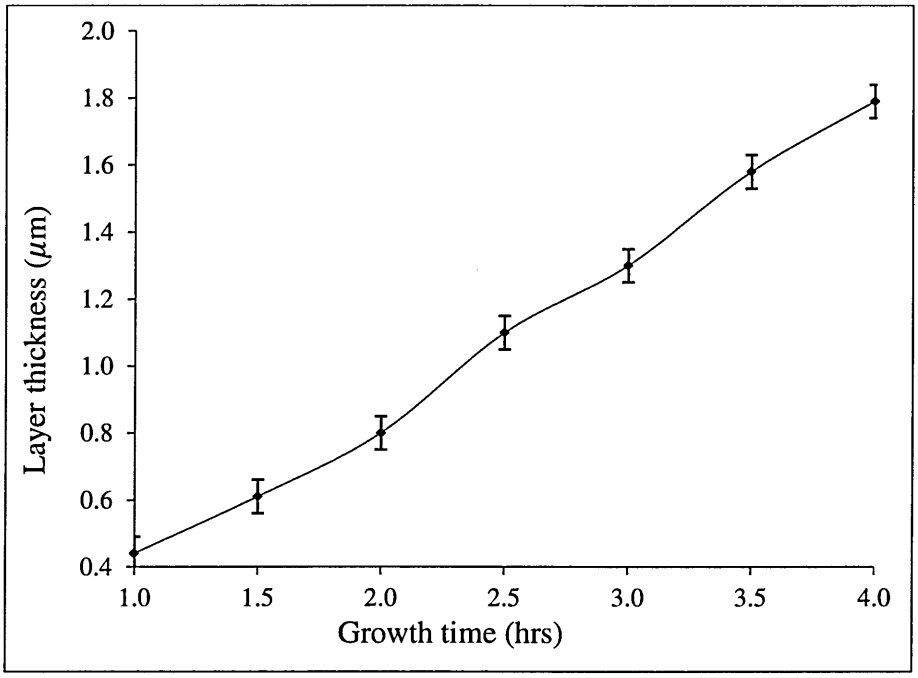

Figure 4-4: Plot of experimentally measured thicknesses vs. growth time for as-deposited In_xSe_y layers. All other parameters; growth voltage, growth temperature and pH were kept constant.

4.3.5 Morphological studies

4.3.5.1 Scanning electron microscopy

Scanning electron microscopy (SEM) was carried out to investigate the effect of different annealing temperature on the surface morphology of In_xSe_y layers. Figure 4.5 shows the SEM image of glass/FTO/In_xSe_y layers annealed at different temperatures. The investigation was carried out on layers grown for one hour and cleaned with deionised water and dried in air. Thereafter, the as-deposited sample was cut into three samples and annealed at three different temperatures of 100, 200 and 300°C in air.

Figure 4.5 shows SEM images of glass/FTO/In_xSe_y annealed at (a) 100, (b) 200 and (c) 300°C for 10 minutes in air. The films annealed at 100°C show islands with non-uniform coverage of the glass/FTO substrate. This film show wide gaps between material clusters. For samples annealed at 200°C (Figure 4.5(b)), it is observed that the glass/FTO substrate is fully covered with molten-like In_xSe_y thin films with virtually no clear cluster boundaries. It also shows complete wetting of the FTO surface and continuous In_xSe_y layer with full glass/FTO coverage with virtually no grain boundary demarcations. However, few scattered pinholes were observed possibly due to the heat treatment temperature of this layer. These layers show good wetting property and if

properly optimised, it will make an excellent candidate as a buffer or window layer for fabrication of high efficiency solar cell devices.

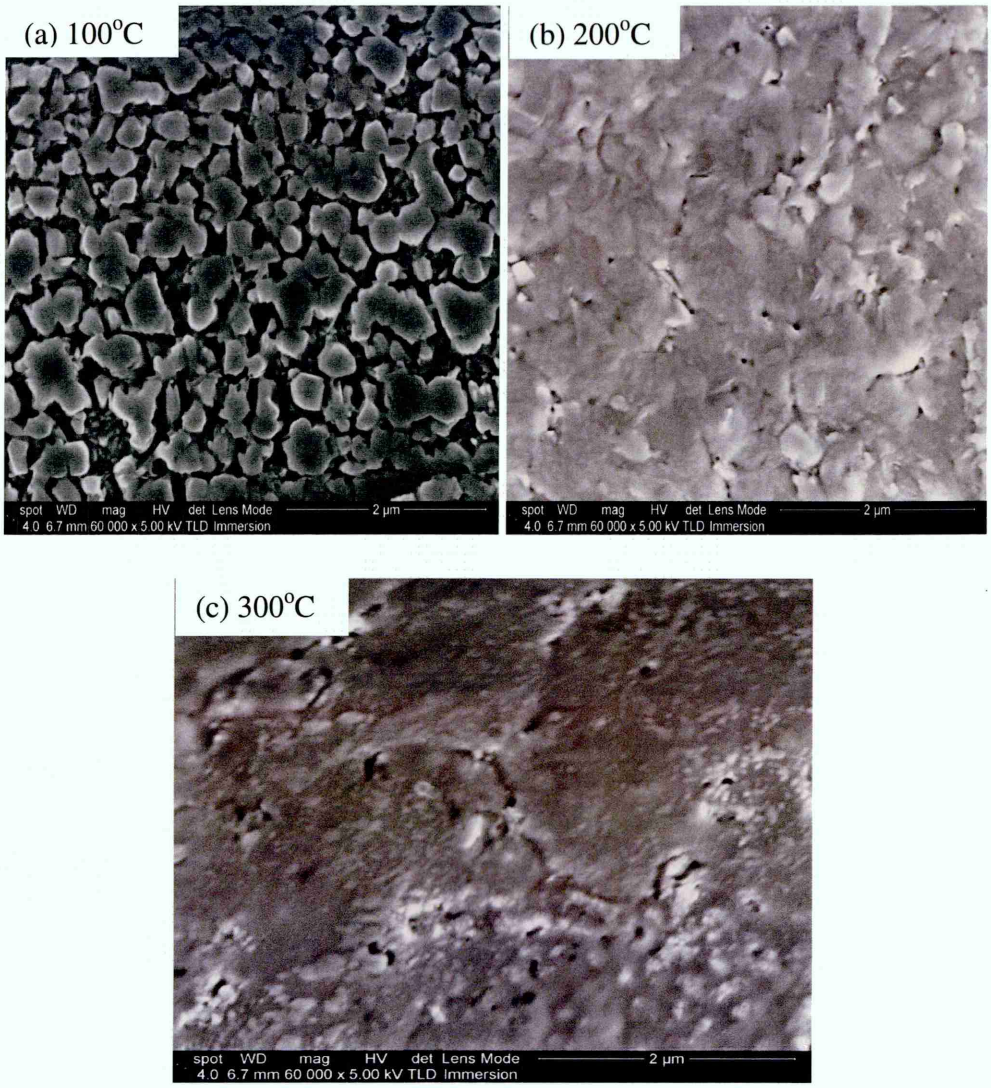

Figure 4-5: SEM images of In_xSe_y layers annealed at (a) 100°C, (b) 200°C and (c) 300°C, for 10 minutes in air.

Figure 4.6 shows the SEM cross-section image of glass/FTO/In_xSe_y layer. This work was conducted to study further the wetting property of the In_xSe_y thin films on the glass/FTO substrate. Since glass/FTO substrates are known to have rough surfaces which are known to affect solar cell performance due to possible creation of pinholes if the FTO spikes were not well covered by the buffer or window layers due to layer non-uniformity or law thickness. Materials with good surface wetting property such as In_xSe_y could be helpful in filling the valleys in FTO layer smoothening out the surface roughness. The cross-sectional image shown in Figure 4.6 revealed that the layer is seen to follow the FTO surface pattern covering the FTO spikes. This image reveals full coverage of the FTO surface by the layer, reducing significantly its surface roughness

avoiding shorting of the device. This property can also help in the reduction of the CdS window layer thickness especially in multi-layer graded bandgap devices which will improve the optoelectronic properties of the window layers that will positively affect both the V_{oc} and the FF of the devices [24].

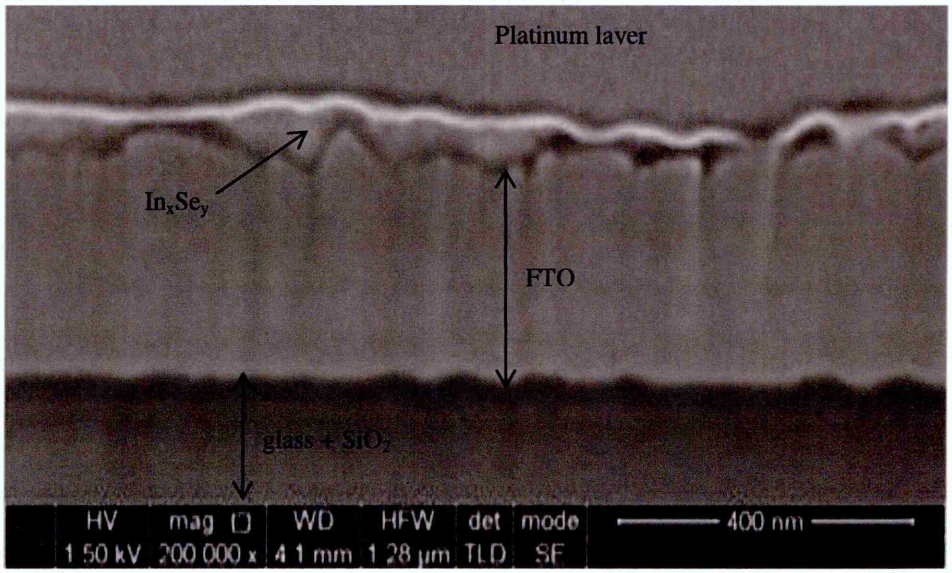

Figure 4-6: A typical SEM cross-section image of a glass/FTO/In_xSe_y structure indicating smoothening effect on the FTO rough surface.

4.3.5.2 Atomic Force Microscopy

Figure 4.7 shows 2-D AFM images of heat-treated In_xSe_y layer grown at 1800 mV on glass/FTO substrate. The images revealed a molten-like and continuous surface morphology of the In_xSe_y layer showing no gaps between material clusters and fairly smooth morphology similar to the SEM images presented in Figure 4.5.

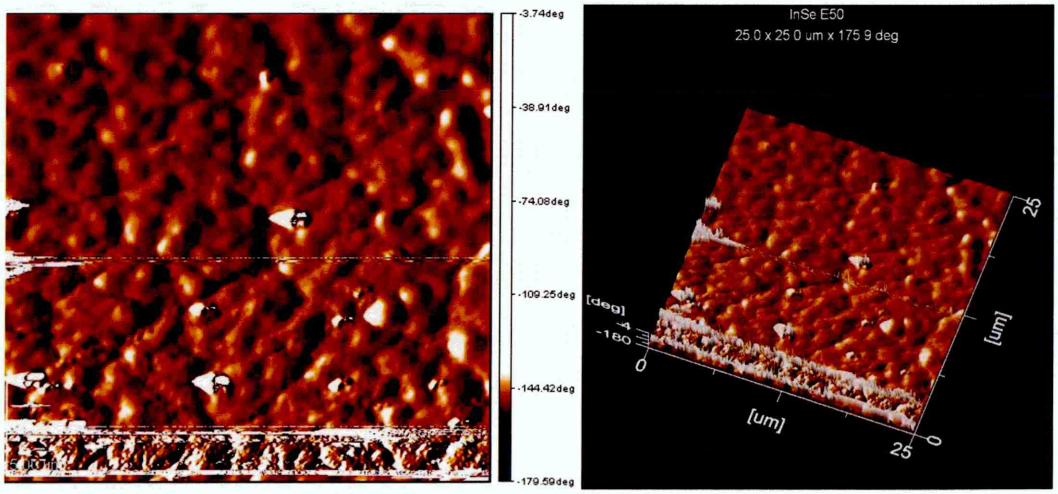

Figure 4-7: 2D AFM images of annealed In_xSe_y layer grown for 60 minutes and annealed at 300°C for 10 minutes in air.

4.3.6 Photoelectrochemical cell measurement

Photoelectrochemical (PEC) cell measurements were performed on the layers to confirm their electrical conductivity type. The experiments were carried out by growing ten In_xSe_y layers on glass/FTO substrate at growth voltages in the range (1750-1850) mV earlier estimated from the voltammogram shown in Figure 4.1. Figure 4.8 shows the plot of PEC signal vs. growth voltage of In_xSe_y layers grown in steps of 10 mV in both as-deposited and annealed condition. In the as-deposited layers, it is observed that at lower voltages (1750-1800) mV, the layers were Se-rich and p-type in electrical conduction while at higher growth voltages (1810-1850) mV, the layers were In-rich and n-type in electrical conduction. Between these two regions, there exists an inversion voltage (V_i) where the electrical conduction type changes from p-type to n-type or n-type to p-type. Materials grown at this point are near stoichiometric in composition and ideal for fabrication of high efficiency solar cell devices [25]. The obtained V_i in this work is ~1810 mV. Therefore materials grown at voltages lower than 1810 mV are p-type due to Se-richness while those grown above 1810 mV are n-type due to In-richness.

It is observed that by simply changing the growth voltage, the conductivity type of In_xSe_y can be altered by intrinsic doping or doping by varying the composition.

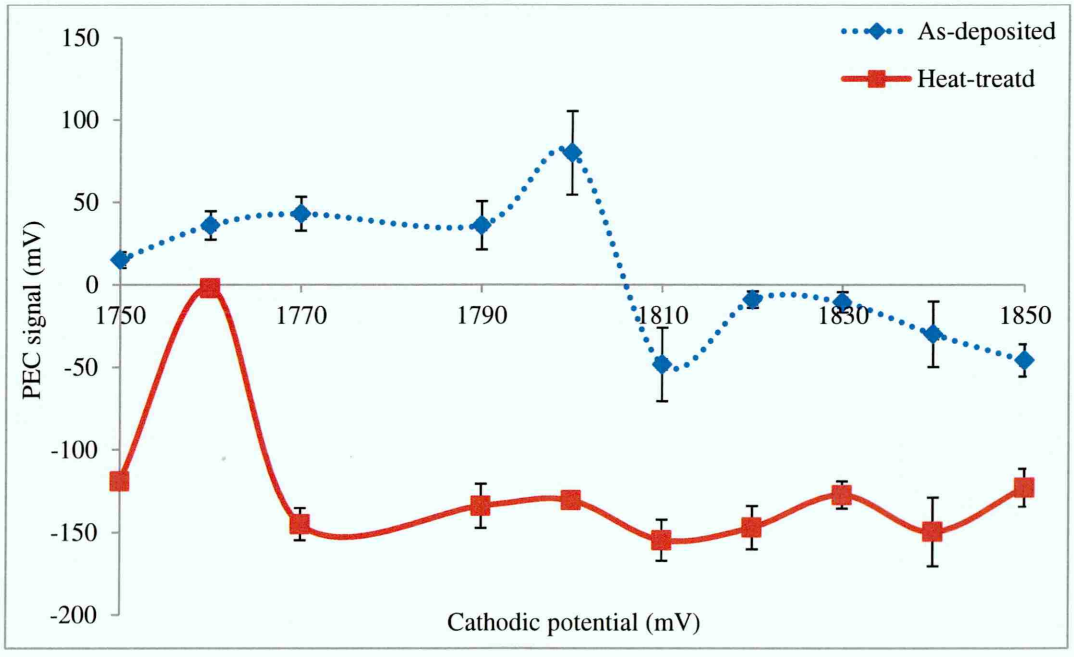

Figure 4-8: PEC signal vs. growth voltage for In_xSe_y layers grown at different growth voltages.

It is also important to point out that the value of the V_i can shift depending on parameters such as Selenium concentration, growth temperature, pH and stirring rate. After annealing, all layers move to n-type as can be observed in Figure 4.8. This change could be as a result of defects redistribution and/or annealing out defects in the films during heat treatment. Though electrodeposition provides the room for the deposition of both n-type and p-type in various semiconductors such as CdTe [26], ZnSe [27], ZnTe [28], ZnS [29], this is the first time the growth of both n-type and p-type In_xSe_y semiconductor is demonstrated from a single electrolyte.

4.4 Conclusions

The electroplating and characterisation of InSe thin films were successfully carried out from aqueous acidic electrolyte using a simple 2-electrode system. XRD studies show that the material grown is amorphous in both as-deposited and heat-treated layers. PEC cell measurements show that both n-type and p-type In_xSe_y thin films were obtained by varying the growth voltage. Surface morphology for both as-deposited and after heat-treatment show virtually no improvement which further indicates the amorphous nature of these layers. The bandgaps of the layers in both as-deposited and heat-treated were found in the range (1.9-2.5) eV. The In_xSe_y materials were incorporated into different device structures as buffer layers.

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Chapter 5: Growth and characterisation of ZnS buffer layers

5.1 Introduction

Zinc sulphide (ZnS) is an important wide bandgap II-VI semiconductor material with a direct optical bandgap of 3.70 eV [1]. This bandgap is ideal for the window/buffer layer in solar cells [2,3]. ZnS has also found applications in the areas of electroluminescent devices [4] and in antireflective coatings [5] due to its high transparency in the short wavelength region (350–550) nm when compared to CdS with bandgap of 2.42 eV.

ZnS can be n-type or p-type [6] in electrical conduction depending on the growth conditions. This material usually grows in zinc blende and/or wurtzite crystal structures, which in both cases show a direct optical energy gap [7]. In solar cells, ZnS can be used as a buffer or window layer in CdTe and CIGS based solar cells. The incorporation of Cd-free CBD-ZnS as a buffer/window has yielded an efficiency of 18.6% in the ZnS/Cu(In,Ga)Se_2 solar cell comparable to 19.2% efficiency achieved using CdS [8]. Echendu *et al.* [2] incorporated n-type ED-ZnS as a window layer in ZnS/CdTe solar cell structure achieving 12% efficiency. Junfeng Han and co-workers [9] used ZnS as a buffer layer in ZnS/CdS/CdTe solar cell structure achieving a solar conversion efficiency of over 10%. Pudov *et al.* [10] used CBD-ZnS as a window layer in CIGS based solar cell and achieved a conversion efficiency of 18.1%.

The effort to substitute the well-known CdS which is so far the best heterojunction-partner to CdTe with a wider bandgap material such ZnS is on course so that solar conversion efficiencies can be further improved avoiding the detrimental effects of Cd. However, one challenge when using ZnS especially in CdTe-based devices is the large lattice mismatch of ~16% that exists at the ZnS/CdTe interface [11] as compared to ~10% [12,13] for the CdS/CdTe interface. ZnS thin films have been grown using variety of techniques some of which were described in Chapter 3.

This chapter presents the growth and characterisation of ZnS thin films electrochemically synthesised in a single electrolytic cell using the 2-electrode configuration. Layers with both n-type and p-type electrical conductivity were obtained by simply changing the deposition potential. Full optimisation of growth voltage was carried out using variety of analytical techniques within the Materials and Engineering

Research Institute (MERI), Sheffield Hallam University. These include; X-ray diffraction, PEC cell measurements, Raman studies, surface morphology, optical properties, and DC electrical resistivity measurement.

5.2 Preparation of deposition electrolyte

The deposition electrolyte for the preparation of ZnS thin films was made by dissolving 0.15 M $ZnSO_4$ of purity 5N (99.999%) and 0.15 M $(NH_4)_2S_2O_3$ (purity 98%) in 400 ml of deionised water. The 500 ml Teflon beaker containing the 400 ml of the electrolyte was housed in water bath using 1000 ml glass beaker. All chemicals were purchased from Sigma-Aldrich, UK. A Teflon beaker was used to avoid the possible leaching of ions such as Na into the deposition electrolyte since the deposition medium was acidic. It is well known that atoms of groups 1A and 1B are acceptor dopants to II-VI semiconductors [14,15] which degrade device performance when incorporated during growth; especially in n-type CdTe-based devices. This precaution is taken due to the fact that devices fabricated in this research are based on n-type CdTe.

5.3 Substrate preparation

The substrates used for the deposition of ZnS are glass/FTO with sheet resistance of 7 or 15 Ω/square purchased from Sigma-Aldrich, UK. The glass/FTO substrates were cleaned using soap solution to degrease and remove dust particles rinsed in de-ionised water then cleaned with methanol and again rinsed in de-ionised water and dried in air before deposition. After the cleaning process, each of the glass/FTO substrates (working electrode) was attached to carbon electrode using polytetrafluoroethylene (PTFE) tape before insertion into the electrolyte. The cleaning of the substrates before deposition is important so that dust and other contaminants on the substrate surface are thoroughly removed before deposition. If the cleaning is not properly done, it may affect the deposited layer property in many ways ranging from layer non-uniformity, voids which can result in poor contact between the FTO and the deposited layers and it can also introduce pinholes. These effects become obvious in heat treated layers where the pinholes appear clearly and may also result to peeling of the layer due to poor adhesion. Substrate cleaning should be taken seriously as the output of of solar cells depends largely on the electronic property of the interface. This cleaning procedure is implemented prior to deposition of all layers.

5.4 Experimental procedure

5.4.1 Cyclic voltammetry

In electroplating of semiconductor materials, it is important to obtain the approximate deposition voltages for the growth of near stoichiometric thin films of ZnS layers. This is helpful for depositing material with the required electronic properties for optimum performance when used in the fabrication of devices. This study was carried out using cyclic voltammetry.

Figure 5.1 shows the cyclic voltammogram carried out using 2-electrode system within the growth voltage range (0-2000) mV. The cathode and anode were glass/FTO substrate and high purity carbon rod respectively. The pH of the bath was adjusted to 4.00 ± 0.02 using dilute sulphuric acid (H_2SO_4) or ammonium hydroxide (NH_4OH) at room temperature and the deposition temperature was set to ~30°C. The voltammogram with a scan rate of 3 mVs^{-1} was carried out using a computerised Gill AC potentiostat system. The source of heat and stirring was a hot plate with magnetic stirrer, and the stirring rate of the bath was moderate and maintained throughout the deposition process.

The decision to stay with growth temperature of ~30°C is due to precipitation in the electrolyte at higher temperatures. Precipitation starts to form at a growth temperature of ~50°C, which turns the electrolyte cloudy with undissolved particles settling at the bottom of the bath. Observation has also shown that this precipitation lead to instability in the pH of the electrolyte; hence the decision to stay with 30°C, at which temperature the electrolyte is clear and stable [16]. A similar observation was reported by Echendu [17].

Looking at the voltammogram and with respect to the redox potential of the constituents ions of Zn and S, sulphur (S) with lower reduction potential of E^0= +0.144 V [18] starts to deposit immediately at the beginning of the deposition as revealed by the inset diagram of Figure 5.1 during the forward cycle. The deposition of sulphur continues at the lower voltages and at voltages around 1000 mV, a steady increase in current is observed which could be due to the incorporation of Zn (E^o=-0.762 V) and the rapid increase in the deposition current at voltages around 1300 mV could be attributed to the co-deposition of Zn and S. The window for the growth of near stoichiometric ZnS is approximately in the range (1350-1550) mV. At higher growth voltages around 1600 mV, dark Zn-rich ZnS layers are deposited. This dark layers consist mostly of elemental

Zn which result in poor quality layers that will not withstand the necessary post growth processing procedure.

During the reverse cycle, elemental Zn and Zn from ZnS starts to dissolve at cathodic voltage around 1300 mV while the negative peak at voltage around 570 mV could be due to dissolution of sulphur from the cathode. The deposition of ZnS films on the cathode is given by the electrochemical equation 5.1.

$$Zn^{+2} + 2e^{-} + S \rightarrow ZnS \qquad 5.1$$

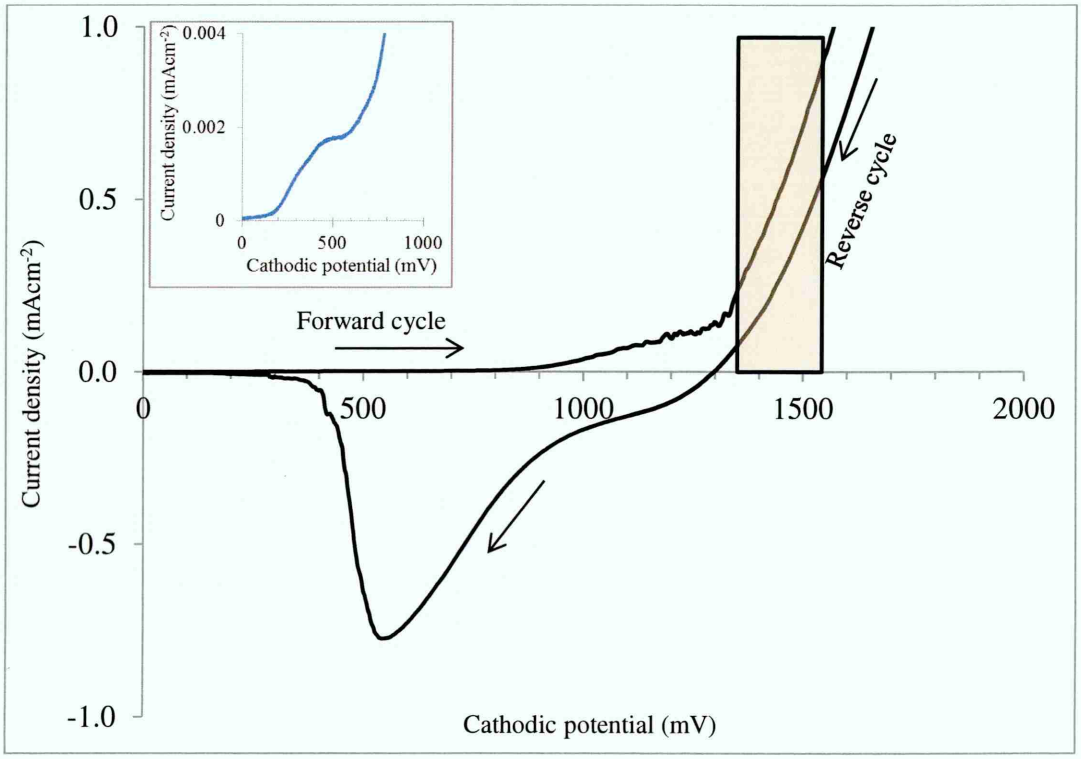

Figure 5-1: Cyclic voltammogram of aqueous solution containing 0.15M $ZnSO_4$ + 0.15 M $(NH_4)_2S_2O_3$ in 400 ml of de-ionised water. Both the growth temperature and the pH were set to ~30°C and 4.00±0.02 respectively.

5.4.2 X-ray Diffraction

Figure 5.2 shows the X-ray diffractogram of (a) as-deposited and (b) heat treated ZnS layers grown at different growth voltages. After growth, the as-deposited glass/FTO/ZnS sample grown at each voltage was cut into two smaller samples. The first set was left as-deposited and the other set was heat treated at 350°C for 15 minutes in air. In each case the FTO pattern is included for easy comparison. The XRD patterns for both the as-deposited and heat treated samples show no XRD peaks from the ZnS

films. All the observed peaks are due to the underlying FTO substrates. This is a clear indication that this material is amorphous under the growth conditions used in this experiment. Similar results on the growth of amorphous ZnS thin films was also reported by Echendu *et al.*[19,6].

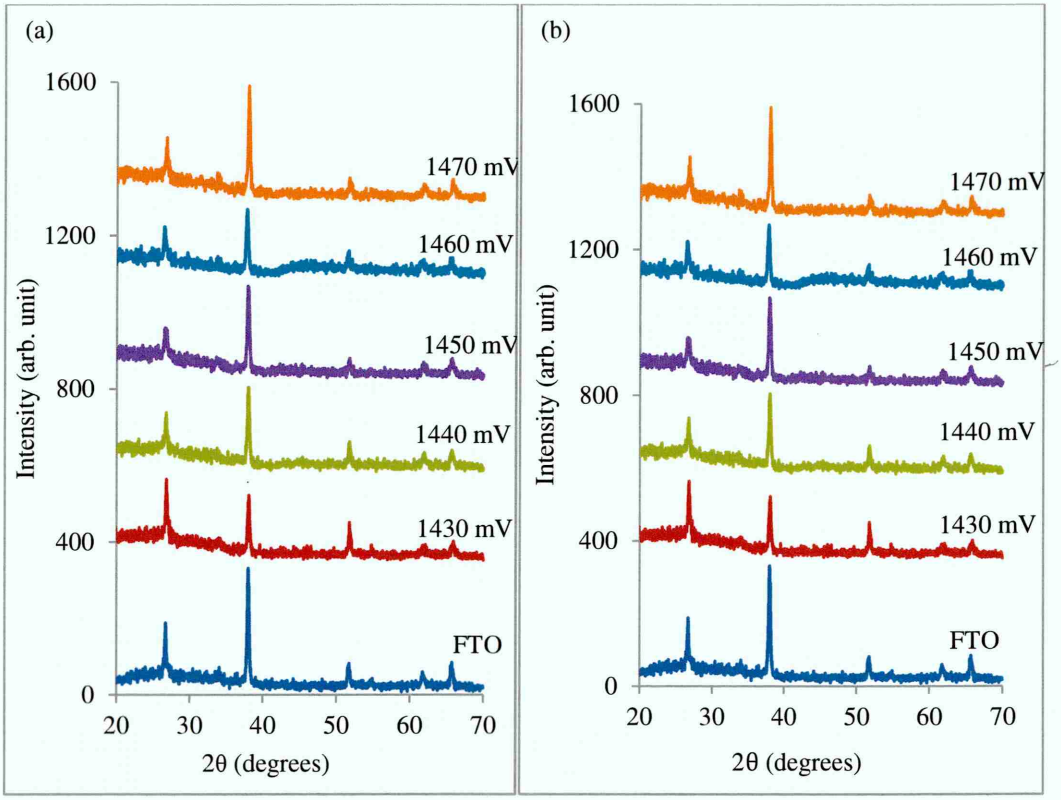

Figure 5-2: XRD patterns of ZnS layers grown on glass/FTO substrate at different cathodic potentials for (a) as-deposited and (b) heat-treated (at 350°C for 15 minutes in air) layers.

5.4.3 Photoelectrochemical Cell studies

The Photoelectrochemical (PEC) cell study was carried out to confirm the conductivity type of the ZnS layers. Several layers were grown and their conduction type established as shown in Figure 5.3. Ten samples were grown based on the approximate range observed from the voltammogram presented in Figure 5.1. The layers were grown at voltages from 1400 to 1500 mV in steps of 10 mV. As shown in Figure 5.3, the conductivity type of the samples for both the as-deposited and heat treated films was obtained. Prior to measurements, the PEC system was calibrated with material of known conductivity type such as CdS before measurement to avoid inaccurate results.

Figure 5.3 shows the PEC signal as a function of growth voltage for several ZnS layers grown at different growth voltages. The results show that the ZnS layers grown at lower

cathodic voltages (1400-1440) mV were S-rich and p-type in electrical conduction while those grown at higher cathodic voltage range (1460-1500) mV are Zn-rich and n-type in electrical conduction. There exists between these two regions a transition or inversion voltage (V_i), where stoichiometric ZnS with intrinsic electronic properties can be found. As observed in this experiment, the V_i corresponds to a growth voltage of ~1450 mV. Materials grown at voltages lower than the V_i are S-rich and p-type in electrical conduction while all films grown at voltages higher than the V_i are Zn-rich and n-type in electrical conduction. Increase in the growth voltage incorporate more Zn which is the electron source on the cathode thereby increasing the n-type doping. While decreasing in the growth voltage from the V_i, incorporates more S which increases the p-type doping on the cathode; thereby increasing the p-type nature of the layer. This is doping by composition and is due to the variation of growth voltage as demonstrated in this experiment.

Compositional or intrinsic doping due to variation in growth voltage in a single cell has also been demonstrated in materials such as CdTe [20,21], ZnSe [22] and ZnTe [23]. However, this is the first time both n-type and p-type ZnS thin films were demonstrated and reported [24] using a single electrolytic cell. It is also important to note that the value of V_i may shift depending on factors such as sulphur concentration, stirring rate, pH and growth temperature.

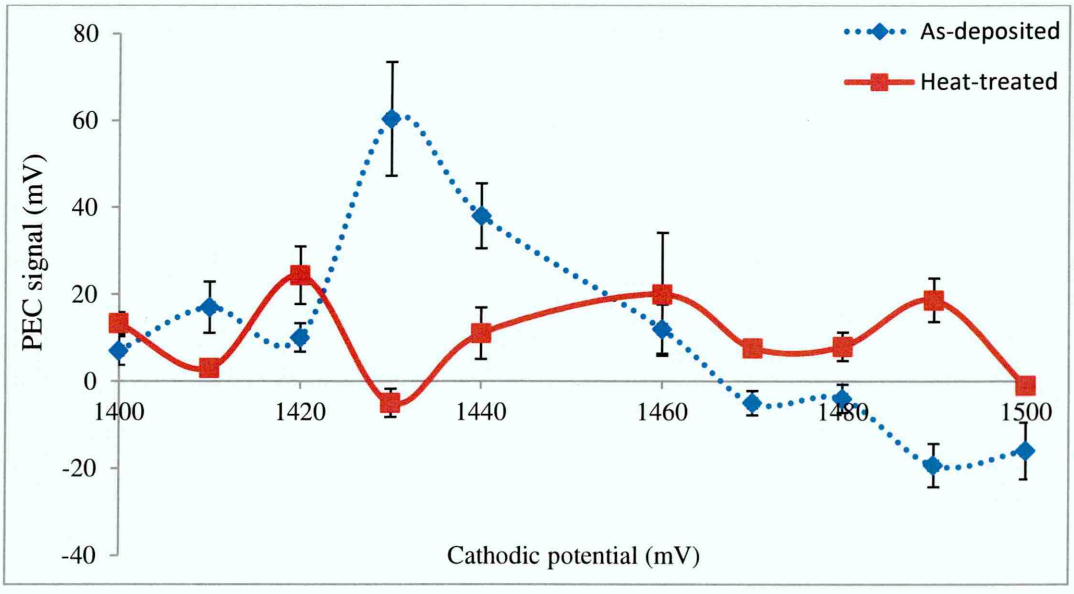

Figure 5-3: PEC signal measurements as a function of growth voltage for both as-deposited and heat-treated ZnS layers.

5.4.4 Raman spectroscopy

Raman spectroscopy is a technique that gives information on the molecular vibration and other structural properties such as crystallinity and phases of the materials. Figure 5.4 shows the Raman spectra of ZnS thin films grown on glass/FTO substrate at room temperature. Observed from the spectra are two broad peaks at 147 and 217 cm^{-1} identified as 2TA and 2LA optical mode phonons for ZnS respectively [25]. The broad nature of these peaks complements the XRD which revealed that this material is amorphous. It can be observed in the as-deposited condition, that the material shows amorphous behaviour with virtually no peaks. However, after heat-treatment, an improvement is observed, with the emergence of a small broad peak at 217 cm^{-1}.

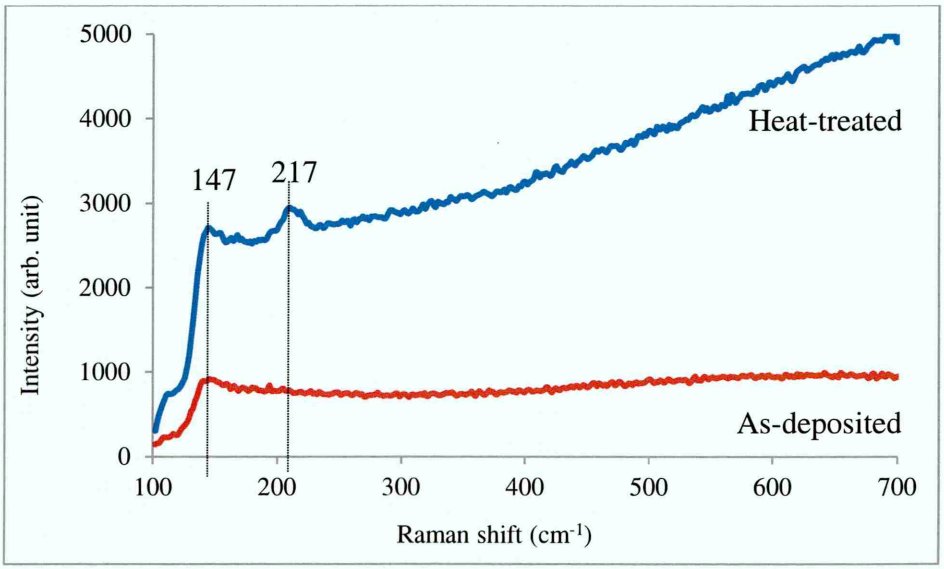

Figure 5-4: Raman scattering spectra recorded on glass/FTO/ZnS thin films of as-deposited and heat-treated (at 350°C for 15 min in air) samples.

5.4.5 Optical studies

Optical properties of semiconductors for intended use in optoelectronics devices such as solar cells are important and useful properties critical to device performance. These properties indicate the suitability of a particular material for a specific application when incorporated in the solar cell device. Each of the solar cell layers; the buffer, window and absorber should have a well-defined set of optical properties required to satisfy its role when incorporated in a solar cell. Hence they require systematic optimisation before use. Important optical properties studied include; absorbance (A), transmittance (T) and optical energy bandgap (E_g) spectra of the ZnS layers.

5.4.5.1 Effects of growth voltage on the optical properties of ZnS layers

This experiment was carried out to investigate the effect of variation in growth voltage on electrodeposited ZnS thin films. To perform this experiment, three layers were grown at three different growth voltages of 1400, 1450 and 1500 mV including the optimum growth voltage. The samples were grown for one hour.

After growth, each sample was divided into two smaller samples, one was left as-deposited and the other annealed at 350°C for 15 minutes in air. Figures 5.5(a) and 5.5(b) show respectively the absorbance spectra for the as-deposited and heat treated layers. With reference to the as-deposited samples (Figure 5.5(a)), and the wavelength (400-700) nm explored, observation showed that, the layer grown at 1500 mV recorded the highest absorbance while the least absorbance is observed in layer grown at 1400 mV. It is known that increase in growth voltage will increase deposition current density which increases material deposition on the cathode thereby increasing layer thickness. After heat treatment (Figure 5(b)), all the layers show improvement in their optical properties with significant reduction in absorbance. This has also highlighted the importance of heat treatment of materials for solar cell device application.

Figures 5(c) and 5(d) show respectively the corresponding transmittance spectra for the as-deposited and annealed ZnS layers. It shows that the transmittance of the layers increases with decrease in growth voltage in both as-deposited and annealed layers. The comparison of the transmittance in the wavelength range (400-700) nm of the as-deposited samples grown at 1400, 1450 and 1500 mV are (34-62)%, (42-65)% and (70-86)% respectively. After annealing, all the layers show improved transmittance. The transmittance in the annealed samples is in the range (54-71)% for the layer grown at 1400 mV while the transmittances for samples grown at 1450 and 1500 mV are approximately in the range (70-92)%. The heat treatment is seen to improve the optical properties of these layers which could be due to annealing out defects which improved both the optical and structural properties. However, the 350°C annealing temperature used in this experiment seems too high for the layers due to the formation of pinholes. Therefore, subsequent samples were annealed at 300°C for time duration between 10-15 minutes.

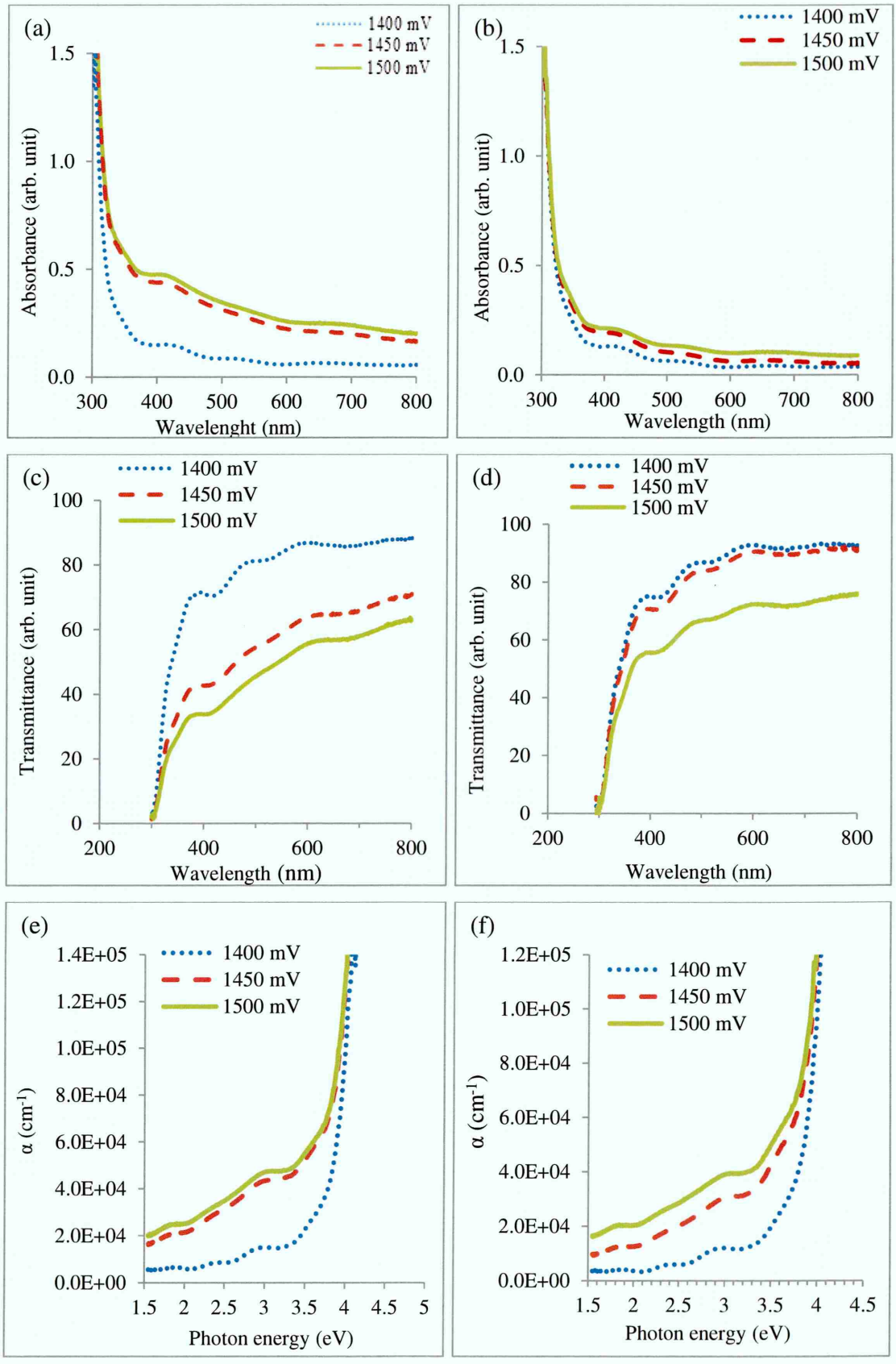

Figure 5-5: (a,c,e) are the optical absorbance (A), transmittance and absorption coefficient (α vs hν) for as-deposited and (b,d,f) are the optical absorbance,

transmittance and absorption coefficient (α vs hν) for the annealed ZnS layers grown at different voltages.

Figures 5.5(e) and 5.5(f) show respectively the optical bandgap spectra for as-deposited and heat treated ZnS layers grown at different growth voltages. The bandgaps were estimated by plotting absorption coefficient (α) vs. photon energy (α vs. $h\nu$) and by extrapolating the straight line portion of the absorption coefficient (α) to the photon energy ($h\nu$) axis (at α=0) [26]. It is observed that the optical bandgaps in the as-deposited samples as estimated from Figure 5.5(e) vary in the range (3.75-3.80) eV which are in agreement with reported values of ZnS thin films in the literature [27–29]. The sample grown at a cathodic voltage of 1400 mV shows the larger bandgap of 3.80 eV while layers grown at 1450 and 1500 mV both indicate similar bandgaps of 3.75 eV. This slight variation in the bandgap is attributed to the variation in the deposition current density which increases with increase in growth voltage as mentioned earlier. Therefore, materials grown at lower voltages are expected to show a higher bandgap due to low film thickness that can allow the passage of all wavelengths of light through the layer which translates to a wider bandgap. Layers grown at higher voltages will show lower bandgaps due to incorporation of more material on the cathode especially Zn which tends to reduce the bandgap due to its metallic nature. Irrespective of the large differences in the growth voltages, the bandgaps exhibited by all the layers are within the reported bandgap of ZnS thin films. This also shows that ZnS can be grown over a wide range with similar optical properties. The errors in the bandgap measurement is within ±0.02 eV.

After annealing (Figure 5.5(f)), the bandgaps of all the layers were observed to decrease towards lower photon energy. The estimated bandgaps of the layers show that the layer grown at 1400 mV show a bandgap of 3.80 eV while the other two layers grown at 1450 and 1500 mV show similar values of 3.70 eV which matches closely with the bulk E_g of ZnS [1]. The improvement in the bandgaps of the layers after heat treatment could be due to annealing out defects and improvement in structural and electronic properties of the layers.

5.4.5.2 Effects of growth temperature on the optical properties of ZnS thin films

The influence of growth temperature on the optical properties of ZnS layers was carried out by growing ZnS layers at three different temperatures of 30, 60 and 80°C at the growth voltage of 1450 mV. Growth duration for all layers was one hour. After growth, the as-deposited sample at each growth temperature was cut into two smaller samples

cleaned and dried in air within the laboratory ambient temperature. The first set was left as-deposited and the other set annealed at 300°C for 10 minutes in air.

Figure 5.6 shows the absorbance versus wavelength and α versus hv of the three layers grown at the three different growth temperatures. Figures 5.6(a) and 5.6(b) respectively show the absorbance spectra for the as-deposited (AD) and heat treated (HT) layers. In both Figures, the absorbance is seen to increase with increase in deposition temperature. A slight improvement in the absorbance edges especially in film deposited at 30°C is observed and can be attributed to the improvement after the annealing process.

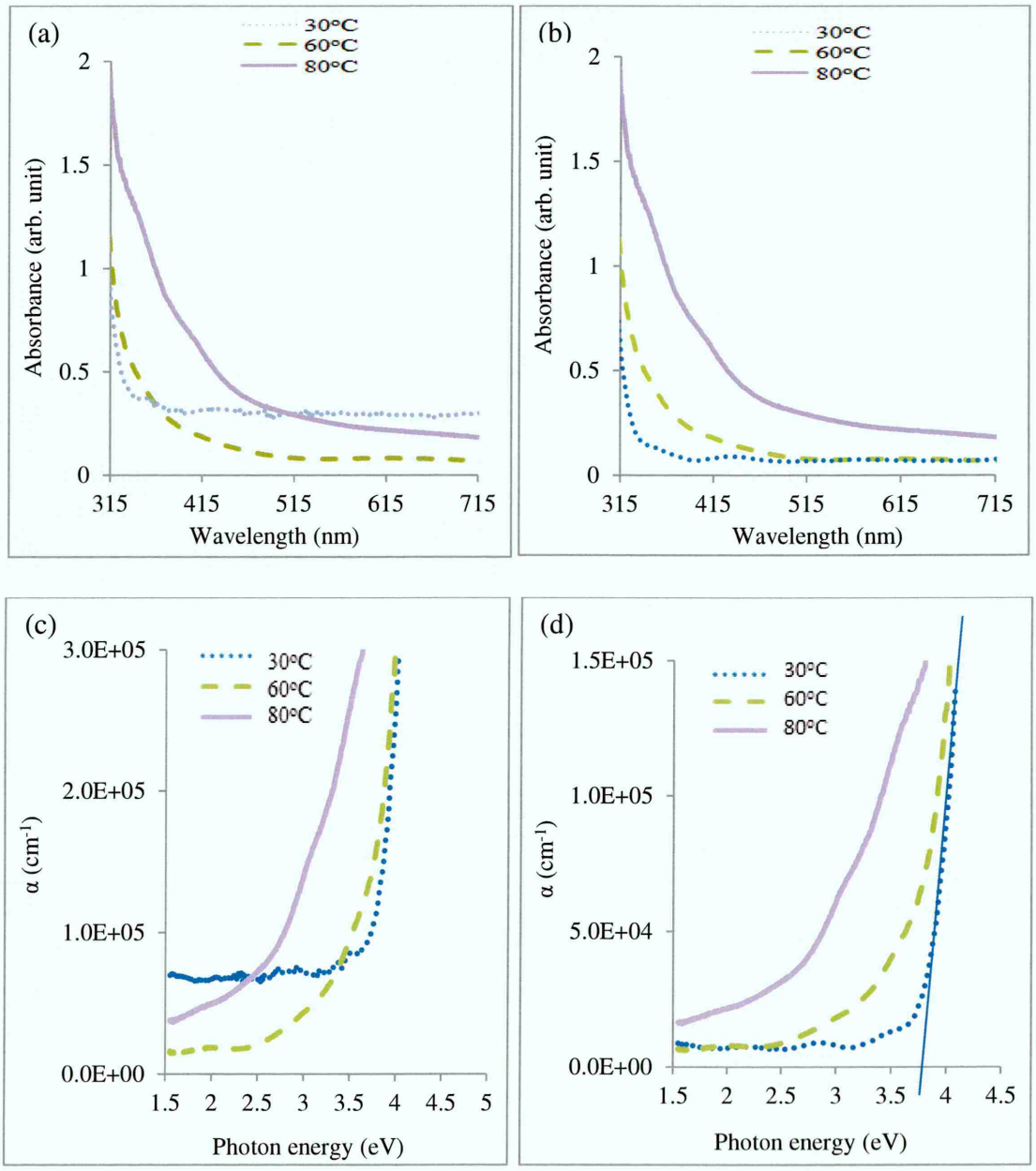

Figure 5-6: (a,b) optical absorbance Vs λ for as-deposited and annealed layers while (c,d) are their respective absorption coefficient versus hν plots for samples grown at different temperatures.

Figure 5.6(c) and 5.6(d) show the absorption coefficient vs photon energy (α vs hν) for as-deposited and heat treated layers respectively. In the as-deposited layers, the estimated bandgaps were found to be 3.85, 3.70 and 3.05 eV for layers grown at temperatures of 30, 60 and 80°C respectively. It is observed that the bandgap values decreased with increase in growth temperature. This is attributed to layer thickness due to variation in growth temperature. Low temperature grown layers are relatively thinner than those grown at high temperature. It is known that increase in temperature of the deposition electrolyte, results in the increase in the electrochemical reaction between the constituents ions of the electrolyte which influences surface diffusion of the adsorbed atoms (adatoms) [30] on the cathode surface. In this way, the variation of growth temperature can affect the optical properties of materials, with layer thicknesses increasing with increase in deposition temperatures.

After annealing (Figure 5.6(d)), the optical bandgaps of the layers grown at 1400, 1450 and 1500 mV were 3.80, 3.70 and 2.70 eV respectively. It is observed there is an increased in the bandgap in each of layers after annealing. The slight increased in the bandgaps could be attributed to the amorphous nature of the material. However the smoothening of the absorption edges of the films after heat treatment especially in sample grown at 30°C is observed. The bandgaps in these layers are in agreement with reported bandgaps of ZnS in the literature [31].

5.4.5.3 Effects of annealing temperature on the optical properties of ZnS thin films

This experiment was carried by growing a ~500 nm thick ZnS layer. The as-deposited layer was divided into three smaller samples for heat treatment at three different temperatures (100, 200 and 300°C). All samples were heat treated for 15 minutes in air. Figure 5.7(a) shows the transmittance spectra for the samples heat treated at different temperatures. It is observed that higher transmittance is obtained in samples annealed at 300°C and the least in samples annealed at 100°C. The percentage transmittance of the layers was estimated from the wavelength range (400-700) nm. The obtained transmittance range for the samples is (39-47)%, (46-59)% and (70-88)% for layers annealed at 100, 200 and 300°C respectively.

Figure 5.7(b) and 5.7(c) are respectively the A vs λ and α vs $h\nu$ of the three ZnS layers. Figures 5.7(b) shows that absorbance decreased with increase in annealing temperature. The layer annealed at 100°C shows higher absorbance while the layer annealed at 300°C shows the least absorbance. It is observed that improved absorbance is recorded as the annealing temperature increases from 100 to 300°C. This could be due to improvement

in structural properties of the layers or possibly due to material sublimation reducing the layer thickness. Figure 5.7(c) shows that, the samples heat treated at a temperature of 100°C show a bandgap of 3.70 eV while samples annealed at 200°C and 300°C showed similar bandgap of 3.75 eV.

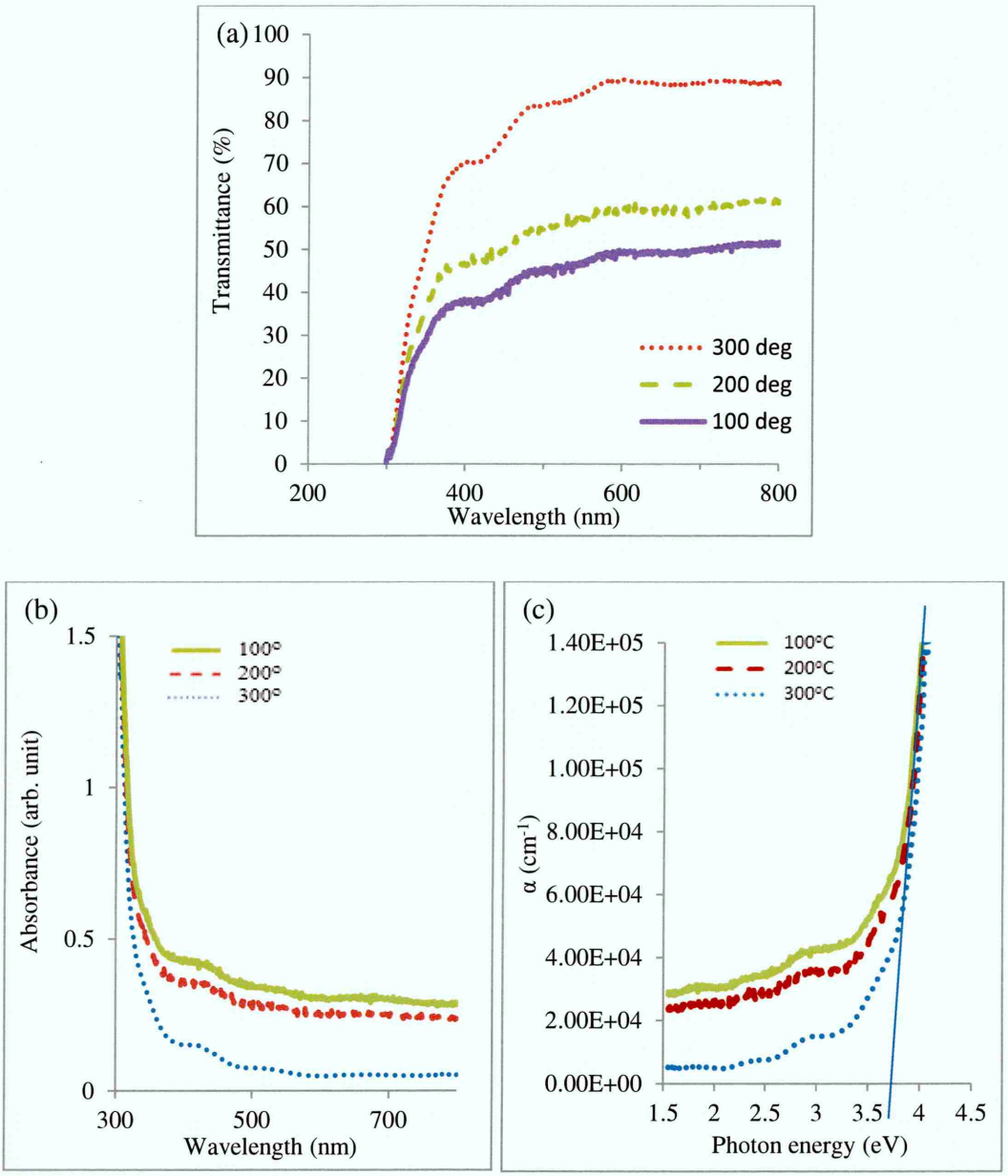

Figure 5-7: The plots of (a) transmittance, (b) absorbance (c) absorption coefficient vs hν spectra for ZnS layers heat treated at different temperatures for 15 minutes in air.

The results show that the heat treatment temperature is a very important parameter from which desired optical properties of layers can be achieved if properly optimised. The transmittance obtained in the layer annealed at 300°C shows a very good transmittance range required for buffer layers so that absorption of photons at the window layers is minimised for increased photocurrent and overall conversion efficiency of the solar cell.

5.4.6 Morphological studies

5.4.6.1 Effects of annealing temperature on the morphology of ZnS thin films

Scanning electron microscopy (SEM) was carried out to study the effects of different heat-treatment temperatures on the surface morphology of ZnS films. Figure 5.8 shows SEM images of glass/FTO/ZnS substrates annealed at different temperatures.

A layer was grown at cathodic potential of 1450 mV to achieve near stoichiometric ZnS thin films. After growth, the layer was divided into four samples. The first sample was left as-deposited and the other three samples were heat-treated at three different temperatures of 100, 200 and 300°C for 15 minutes in air.

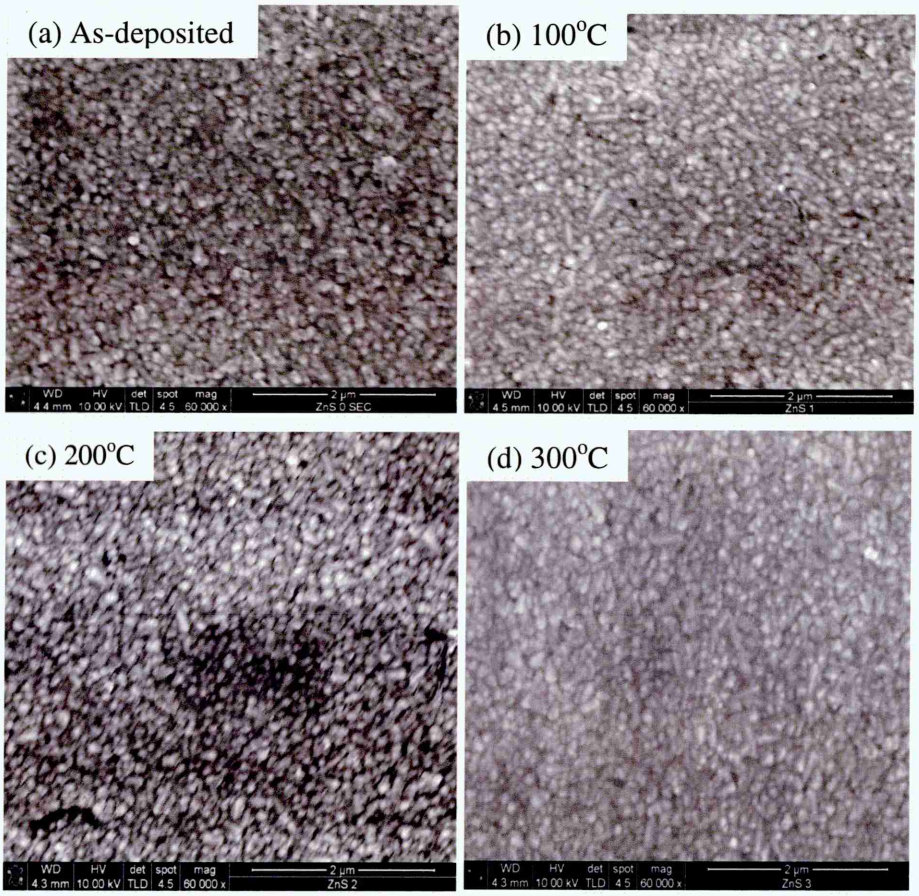

Figure 5-8: SEM images for (a) as-deposited and (b), (c), and (d) are heat-treated glass/FTO/ZnS layers at 100, 200 and 300°C respectively for 15 min in air.

The films morphology shows a fairly uniform coverage of the glass/FTO substrate. The heat-treatment at different temperatures was done to study the effects of heat-treatment on the surface morphology of the films. However, close observation shows that there is no significant improvement upon annealing on the morphology of the films irrespective of the annealing temperature. This agrees well with the optical properties of layers

studied in section 5.4.5.3 which shows little or no variation in their bandgap values. This further confirms the amorphous nature of these materials.

5.4.6.2 Effects of growth temperature on the surface morphology of ZnS thin films

Figure 5.9 shows the surface morphology of as-deposited (AD) and heat treated (HT) thin films of ZnS grown at different growth temperatures for one hour on glass/FTO substrates. There is virtually no difference between the surface images of the as-deposited and annealed layers grown at each growth temperature.

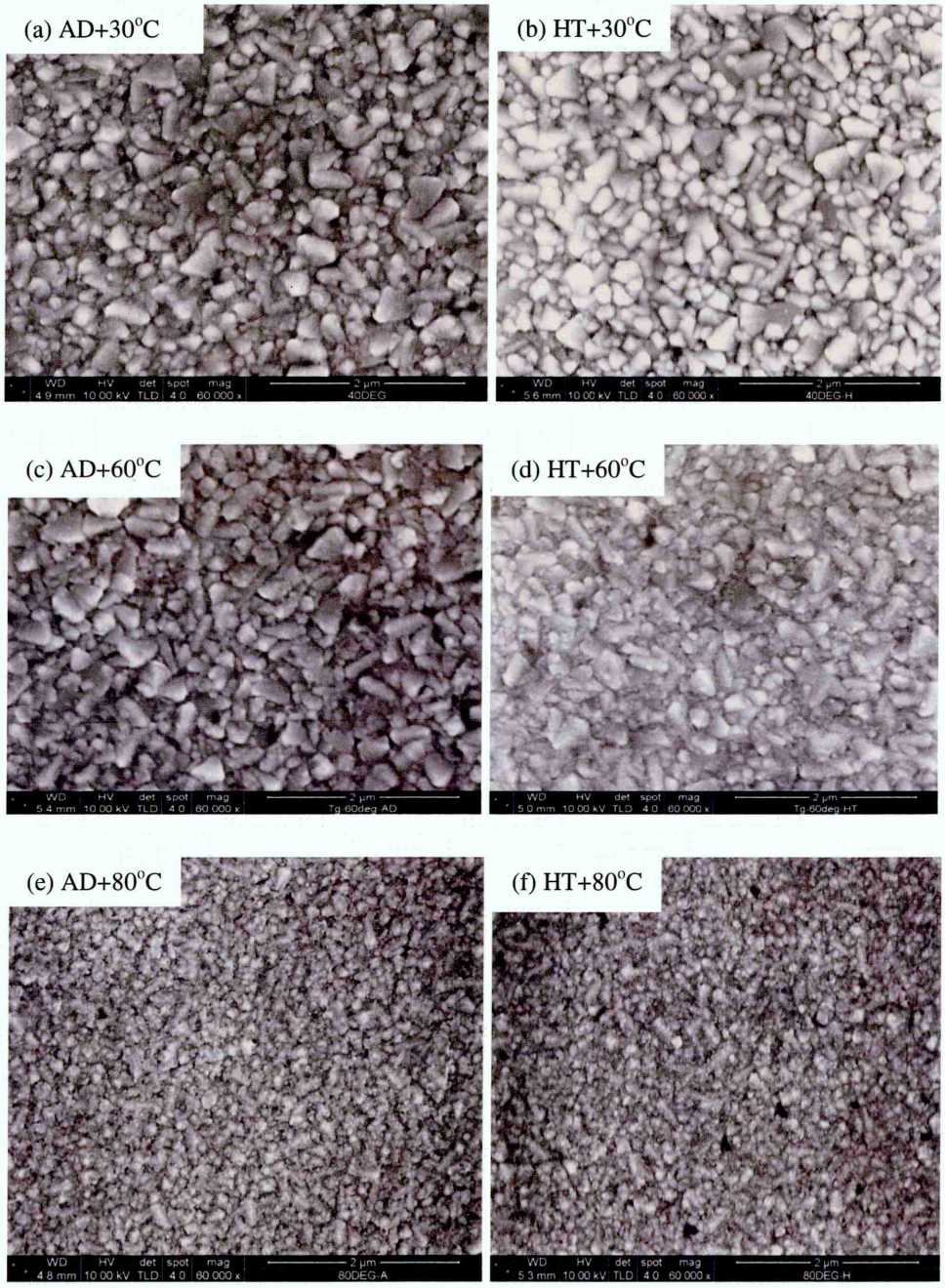

Figure 5-9: SEM images of glass/FTO/ZnS layers grown at different growth temperature (a,c,e) as-deposited and (b,d,f) annealed samples.

However, it is observed that layer thickness increases with increase in growth temperature. This is due to an increase in surface diffusion as the deposition temperature increases from 30°C to 80°C as explained under the optical properties of these layers discussed in section 5.4.5.2. The layer grown at 30°C (Figure 5.9(a)) shows a thin layer of ZnS for both the as-deposited and heat treated samples. The layer thickness continues to increase with increase in temperature with the thicker layer observed in samples grown at 80°C.

As mentioned earlier the variation in the layer thicknesses was attributed to an increase in surface diffusion due to an increase reaction rate between the ions as the growth temperature increases. The morphologies remained virtually the same even after heat treatment for each growth temperature which further confirmed the amorphous behaviour of these layers. However few pinholes are observed in the sample grown at 80°C after heat treatment (HT+80°C)) which could be due to the material loss or sublimation after heat treatment.

5.4.7 Atomic Force Microscopy Studies

The atomic force microscopy (AFM) studies were carried out to determine the surface topographies of the ZnS thin films under study. Figures 5.10(a) and 5.10(b) show respectively the 2D and 3D AFM images for as-deposited and heat-treated ZnS thin films. A small decrease in surface roughness after heat-treatment was observed. The average surface roughness of this material was estimated to be ~18 nm in the as-deposited layers and reduced to ~17 nm after heat-treatment. This values show that the surface roughness in both as-deposited and the heat treated layers remained virtually the same agreeing with previous results on the amorphous nature of this material. The roughness in thin films could be due to the nature of the substrate used. In the electrodeposition technique, the films usually start to nucleate at the spiky tips of the FTO owing to high electric field at these points. This is due to the fact that materials growth in electroplating is electric field driven. To reduce surface roughness and pinholes in thin films, substrates with low surface roughness should be used. This is important since surface roughness affects device performance and can open up pinholes which are detrimental as they cause shunting in thin film solar cell devices. It is for this reason that reasonably thick layers are deposited to avoid the formation of the pinholes

in the films. It requires careful optimisation of the layer thickness so that none of the solar cell parameters suffers.

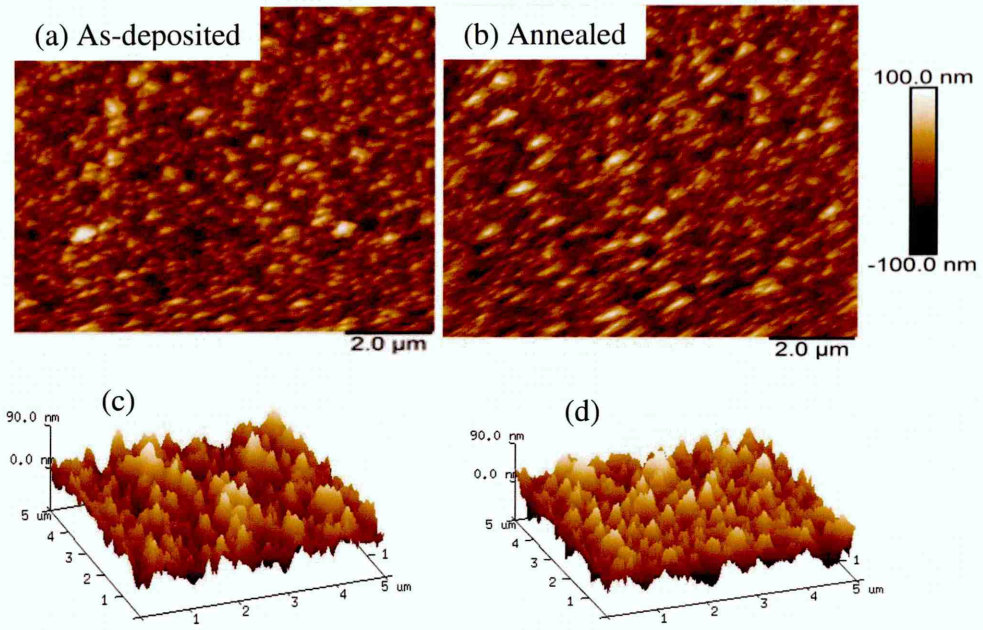

Figure 5-10: 2D AFM images of (a) as-deposited and (b) heat-treated ZnS layers while (c) and (d) are the corresponding 3D AFM images of the layers grown on glass/FTO substrate.

5.4.8 Variation of thickness with growth time for ZnS layers

Film thickness of semiconductor materials for application in solar cells is a very important parameter for achieving high performance devices. Thin film properties such as structural, chemical, optical and device performance are directly dependent on the film thickness. The thicknesses of thin films are dependent on their specific role when incorporated into a solar cell or other optoelectronic device structures. A thin film semiconductor can be used either as a buffer, window or absorber material which suggests the films have different thickness in each case. In this research, ZnS layers were incorporated as buffer layers in CdS/CdTe solar cell device structure which requires films thickness of ~100 nm thick to allow for high transmission of the incident photons.

In this study, the theoretical thickness of the ZnS layers were calculated using Faraday's law of electrolysis while the experimental measurement was carried out using UBM microfocus optical depth profilometer (UBM, Messetecknik GmbH, Ettlingen, Germany). The two methods were performed so that comparison will be made as shown

in Figure 5.11. The theoretical calculations were obtained using the Faradays law given in equation 5.2.

$$T = \frac{JtM}{nF\rho} \qquad 5.2$$

Where; T is the thickness, J is the average deposition current density, M is the molecular weight of ZnS, n is the number of electrons transferred in the formation of 1 mole of ZnS, F is the Faraday constant and ρ is the density of ZnS.

Both methods show fairly linear variation when film thickness is plotted as a function of growth time. It can be observed that the theoretically measured values are higher than the experimentally measured ones. This is due to the fact that not all the electronic charges were involved in the layer deposition process as assumed by the Faraday's law. The lost charges were used in the electrolysis of water. This is the main reason for the observed differences in the two methods. The comparatively low thickness recorded for samples grown for duration of 150 minutes could be due to a low sulphur concentration in the bath. As observed in Figure 5.11, (100-150) nm thick ZnS layer can be deposited at a growth time range (30-60) minutes which is the average thickness used for the purpose of device fabrication. It is also important to note that, factors such as sulphur concentration, growth temperature, stirring rate and pH will affect layer thickness.

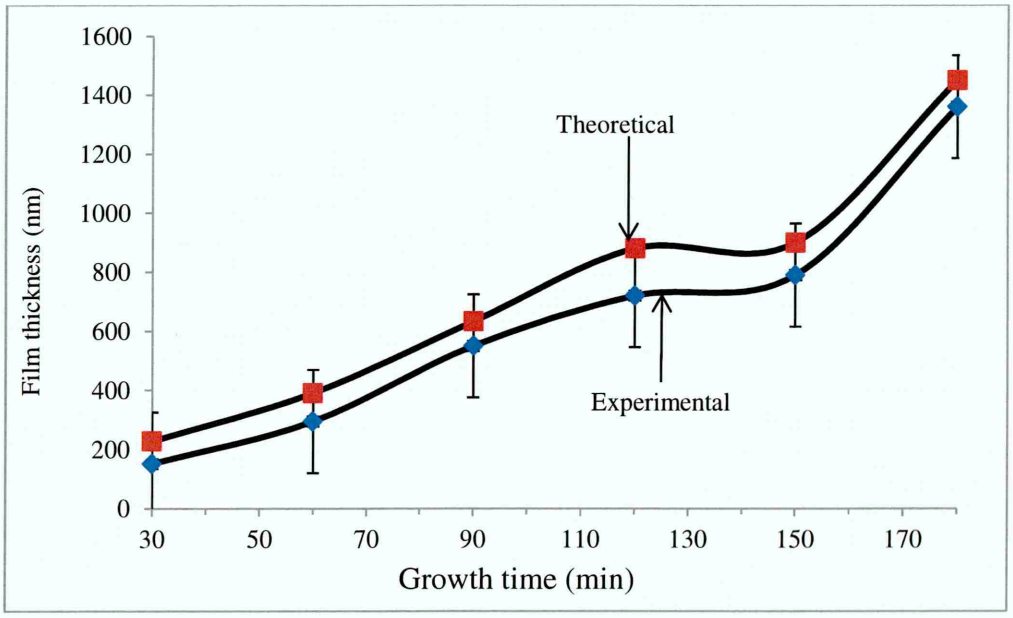

Figure 5-11: Plot of theoretical and experimental thickness estimated for electroplated ZnS films.

5.4.9 DC electrical resistivity studies

The current-voltage (I-V) measurement was performed to obtain the DC electrical resistivity of the ZnS thin films. As-deposited ZnS samples were divided into two pieces one of the samples was left as-deposited and the other heat treated at 300°C for 10 minutes in air. The electrical conductivity type of both samples was confirmed to be p-type in electrical conduction using PEC cell measurement. Ohmic contacts were made on the samples by evaporating 2 mm diameter Au circular contacts. Prior to contacts evaporation, the samples were cleaned in methanol and rinsed in de-ionised water, dried in air and arranged on a metal mask of 2 mm diameter dots and placed inside a Quorum 150T sputtering system. The evaporation was done at pressure of 10^{-3} mbar to complete the glass/FTO/Au device structure. The I-V measurements were performed at room temperature using fully automated series 2401 sourceMeter solar simulator and I-V system purchased from Lot-QuantumDesign Ltd. The resistivity of the film was calculated using $\rho = RA/l$, where; R is the average resistance measured, ρ is the resistivity of the material, l is the thickness of the layer and A is the area of metal (Au) contacts (0.0314 cm^2). It was found that the resistivity (ρ) of the film was ~$6.7x10^4$ Ωcm for the as-deposited and increased to ~$6.9x10^4$ Ωcm after heat-treatment. This shows similar resistivity values for both as-deposited and heat-treated samples. The small increase in the resistivity value could be due to surface oxidation to form ZnO or reduction in the film thickness after heat-treatment possibly due to loss of material through sublimation which reduces the film thickness. The resistivity values obtained in both conditions in this experiment also confirmed the amorphous nature of this material. Similar resistivity value of 10^4 Ωcm for n-type ZnS thin films was reported by Echendu *et al.* [6].

5.5 Conclusions

Successful deposition of ZnS thin films from aqueous acidic solution was achieved using a simple 2-electrode system in a single cell configuration. Structural studies using XRD revealed that the material is amorphous as evident from both the as-deposited and annealed XRD patterns. PEC cell measurements show that by varying the growth voltages, both n-type and p-type ZnS can be achieved by compositional doping. Surface morphology studies using SEM show little or no improvement of the layers even after heat treatment. This indicates the amorphous nature of this material. Surface roughness studied using AFM, show slight decrease in the surface roughness of the layer after

annealing. Optical properties investigated show slight improvement in the layer after heat treatment with obtained energy bandgaps in the range (3.0-3.80) eV as investigated under different conditions. The resistivity of the ZnS thin films show comparable results for both the as-deposited and heat treated layers.

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Chapter 6: Growth and characterisation of CdS window layers

6.1 Introduction

Cadmium sulphide (CdS) is a wide bandgap II-VI semiconductor material with a direct optical bandgap of 2.42 eV (λ=514.5 nm) [1] at room temperature. CdS is an n-type material with absorption coefficient of 4×10^4 cm^{-1} [2]. These optoelectronic properties make CdS suitable especially as a window layer in solar cells when paired with absorber materials such as CdTe [3–5] and CIGS [6,7]. CdS has also been utilised in areas such as sensors [8], transistors [9] and radiation detectors [10,11]. The growth of CdS has been demonstrated by a variety of deposition techniques some of which have been discussed in Chapter 3. The deposition of CdS thin films has been demonstrated using both high temperature complex systems such as closed space sublimation (CSS) [12,13] and low-cost methods such as electrodeposition [14,15]. The main focus of the PV community is to reduce the $\$W^{-1}$ cost using low-cost materials and processing methods. Electrodeposition, a low-cost method of semiconductor growth has shown the flexibility of semiconductor growth from both aqueous and non-aqueous solutions [16] and has been proven to be manufacturable in the production of solar panels [17]. It also provides advantage for the control of deposition parameters, and hence material properties.

Electrodeposition of CdS thin films has been carried out using both 3-electrode [18] and 2-electrode [15] systems. Another simple method used to produce electronic quality CdS is by the use of chemical bath deposition (CBD) method. However, this method is not suitable due to its batch process of chemical waste which is a great environmental concern due to the Cd element contained therein. This is where electrodeposition; a continues process with less chemical waste, is considered a better option.

Presented in this chapter is the cathodic electrodeposition of CdS thin films using 2-electrode system for use as window layers in CdS/CdTe solar cell devices. Prior to incorporation into devices, the films were characterised using various analytical techniques for their structural, optical, morphological and electrical properties so that high electronic quality CdS can be used for the fabrication of high-efficiency solar cells.

6.2 Preparation of CdS electroplating electrolyte

The CdS was prepared using 300 ml of the deposition electrolyte, composed of deionised water containing 0.075 M $CdCl_2$ (purity 99.995%) and 0.15 M $(NH_4)_2S_2O_3$ (purity 98%); which are the sources of Cd and S ions, respectively. The electrolyte was contained in a 500 ml Teflon beaker which in turn was contained in a 1000 ml glass beaker filled with deionised water (i.e. a water bath) to maintain uniform heating of the electrolyte. The pH of the electrolyte was adjusted to 2.50±0.02 using HCl or NH_4OH. The temperature of the bath was set at ~85°C at the beginning of deposition. All chemicals and the substrates were purchased from Sigma-Aldrich, UK.

The cleaning of the substrate was carried out using soap solution then rinsed in deionised water. The substrate was further degreased in methanol and then rinsed in deionised water and dried in air afterwards. The glass/FTO cathode was attached to a carbon electrode using polytetrafluoroethylene (PTFE) tape while the anode is a high purity carbon rod. The electrodeposition process was carried out using computerised Gill AC potentiostat (ACM instrument). Glass/FTO substrate was used for the deposition of all CdS layers in this thesis.

6.3 Result and discussion

6.3.1 Cyclic voltammetry

The approximate growth voltage for the deposition of CdS thin films was determined using cyclic voltammetry. Using this approximate voltage range, several CdS layers were deposited and characterised to obtain the best growth voltage (V_g) for the deposition of near stoichiometric CdS layers. Figure 6.1 shows the cyclic voltammogram for the deposition of CdS from aqueous acidic solution. The pH of the electrolyte was adjusted to 2.50±0.02 at room temperature using NH_4OH or HCl and the deposition was carried out at ~85°C with a scan rate of 3 mVs^{-1}. The cyclic voltammetry was taken in the voltage range (0-1500) mV. Based on the reduction potential of sulphur (E^0=+0.144 V) [1] and Cd (E^0=-0.403 V) [19], sulphur with more positive redox potential, will start to deposit first on the cathode [1] at voltages around 200 mV where the deposition current begins to rise (as observed in the inset diagram of Figure 6.1). It is expected that Cd with more negative redox potential will start to deposit at a voltage around 850 mV where a sharp increase in deposition current is noticed.

The electrochemical equation for the deposition of CdS from Cd^{2+} and $S_2O_3^{2-}$ is given by equation 1 [2].

$$Cd^{2+} + S_2O_3^{2-} + 2e^- \Leftrightarrow CdS + SO_3^{2-} \qquad 6.1$$

The co-deposition of S and Cd to form near stoichiometric CdS is expected to occur at voltages around 1100 mV to 1300 mV. As shown in the voltammogram (Figure 6.1), the shaded portion indicates (not to scale) the region for the deposition of near stoichiometric CdS thin films. Thin films of electronic quality CdS can be deposited within a wide voltage range as experimentally confirmed.

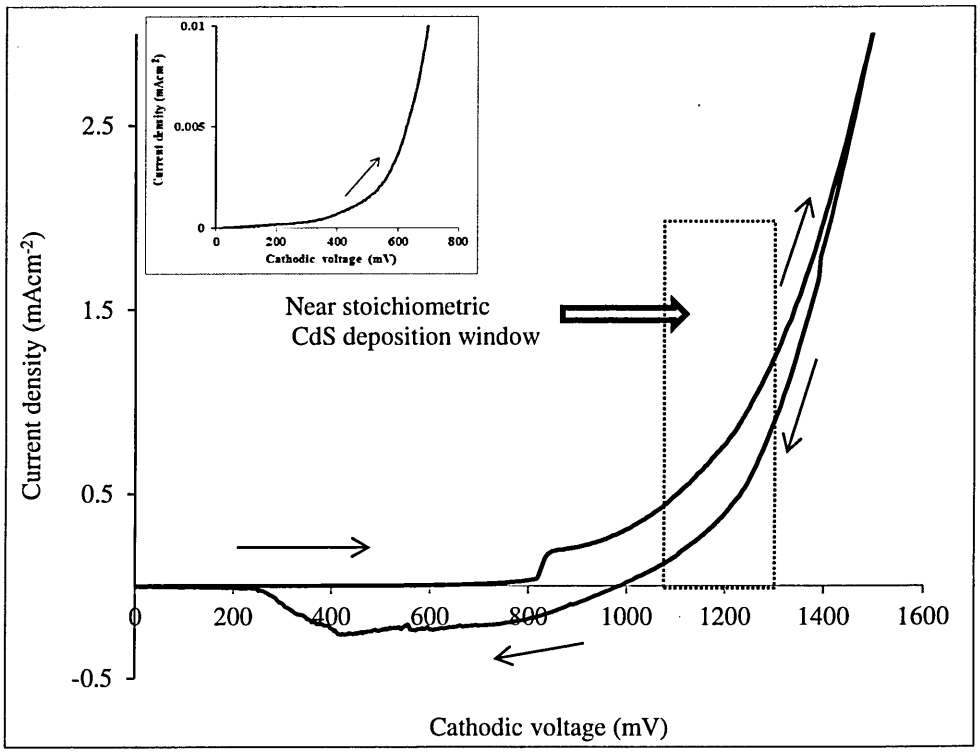

Figure 6-1: Cyclic voltammogram for an electrolyte consisting of 0.075 M $CdCl_2$ and 0.15 M $(NH_4)_2S_2O_3$. The pH and temperature of the electrolyte were 2.50±0.02 and ~85°C respectively.

At higher voltages around 1400 mV, deposition of dendrites on the cathode was observed. Therefore, this region was avoided due to their poor electronic quality.

In the reverse cycle, elemental Cd and Cd from CdS start to dissolve into the bath at voltages around 980 mV and the negative peak at around 400 mV could be due to dissolution of S from the cathode.

6.3.2 X-ray diffraction

Figure 6.2 shows the XRD patterns of (a) as-deposited and (b) cadmium chloride (CC) treated thin films of CdS grown at different growth voltages. The XRD patterns were studied in the 2θ range (20-70)°. The growth voltages were selected based on the approximate deposition voltages obtained from the voltammogram scan for the growth of near stoichiometric CdS thin films. The growth voltages were changed in steps of 5 mV within the estimated voltage range and each CdS layer was grown for a duration of one hour. After growth, the samples were rinsed with deionised water and dried in air. The as-deposited samples grown at each voltage were cut into two. One of the samples set was left as-deposited and the other annealed in the presence of CC at 400°C for 20 minutes in air. After characterisation, the growth voltages were further narrowed down close to the near stoichiometric region in the range (1220-1245) mV for the purpose of analysis. The best material was obtained by monitoring the most intense peak among the entire XRD spectra.

The XRD spectra of both (a) as-deposited and (b) CC treated CdS layers shown in Figure 6.2 revealed that the films were polycrystalline in nature and consists of both hexagonal and cubic crystal structures in both as-deposited and after CC treatment. The three diffraction peaks observed at approximate 2θ values of 24.9, 28.3 and 26.5° corresponds to reflections from (100), (002) and (101) hexagonal phase of CdS respectively. These peaks match well with JCPDS file number: 01-080-0006 for hexagonal CdS crystal phase. The peak at 2θ=~26.5 corresponding to (002) was however not considered for further analysis because of its overlap with the peak of the underlying FTO substrate ((022)H+FTO). The small peak at 2θ=~43.5° corresponds to reflection from (220) cubic phase of CdS. The observation of (100), (002) and (101) reflections in CdS films is well documented in the literature [14–16,20]. The peak at 2θ=~32.1° for sample gown at 1220 mV can be observed and is related to the reflection from the (044) orthorhombic elemental S phase. The presence of this peak in CdS films has been reported for both CBD [21] and electrodeposited CdS [22]. The appearance of this peak in CBD grown CdS was attributed to the high concentration of S used in the deposition solution [21] which correlates to the higher concentration of sulphur than cadmium used in this experiment.

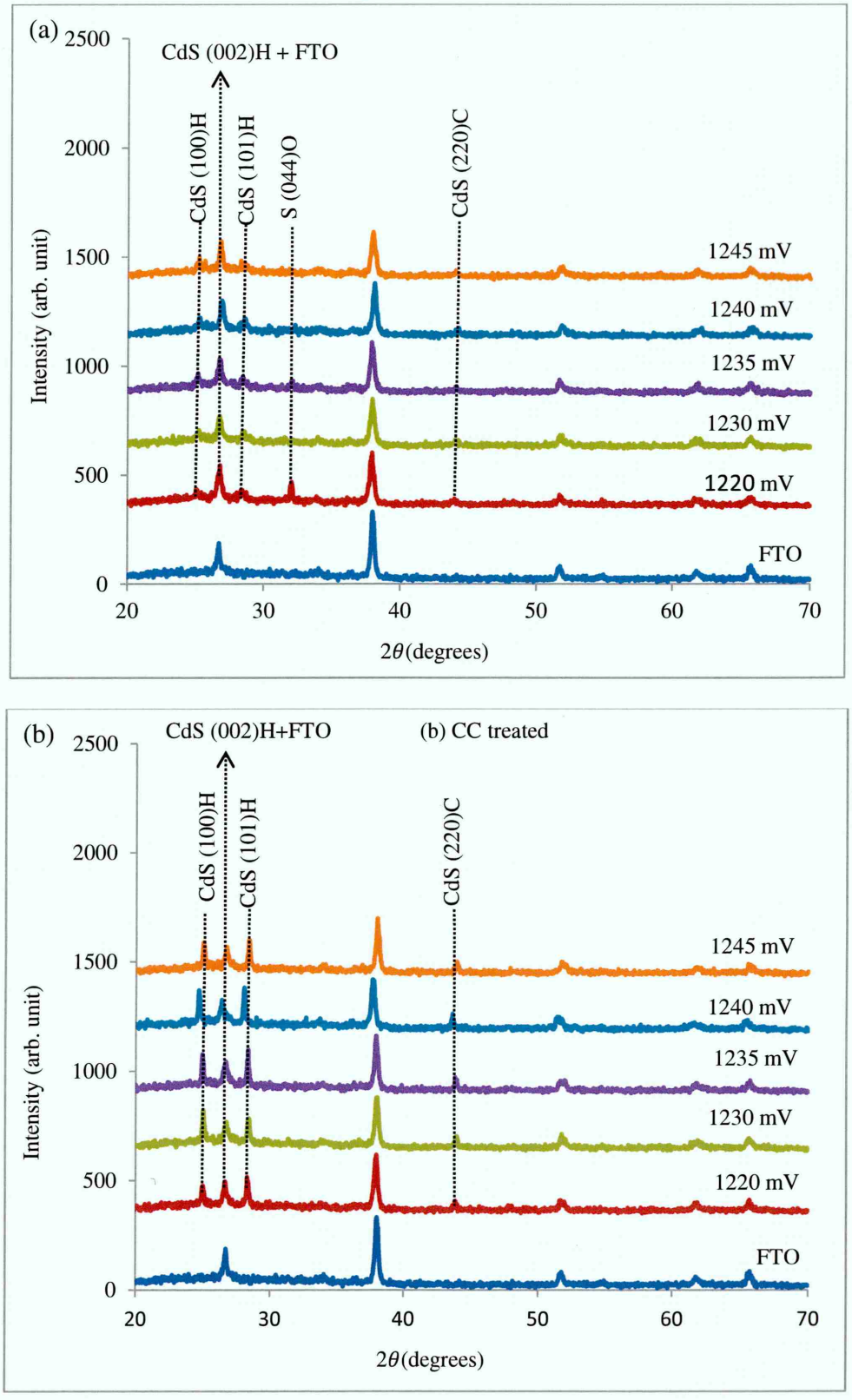

Figure 6-2: X-ray diffraction pattern for (a) as-deposited and (b) CC annealed layers at 400°C for 20 minutes in air.

Based on the peak intensities in these films, the preferred orientation is along the (100) hexagonal phase of CdS at 2θ=~24.9° grown at voltage of 1235 mV. This peak shows the highest intensity and was therefore considered the best CdS growth voltage for the

as-deposited films. Figure 6.2(b) shows the XRD patterns of the films after annealing the samples in the presence of CC at 400°C for 20 minutes in air. After CC annealing, the previously weak and poorly crystalline peaks of (100) and (101) corresponding to hexagonal CdS has shown significant improvement in their peak intensities while reverse is the case for the previously intense peak corresponding to (002) H+FTO peak. The increase in intensities of the two peaks indicates increase in grain growth and recrystallisation due to the incorporation of the CC fluxing agent during annealing of the films. The increase in the intensities of the hexagonal (100)H and (101)H phases of CdS after CC treatment was also reported by Fathy *et al.* [23].

The increase in the peak intensities of the CdS peaks such that they dominate the (002)H peak after the CC annealing is very interesting to see. Observed also is the disappearance of the (044) orthorhombic peak related to S at $2\theta=\sim32.1^{o}$ in these films. The disappearance of the S peak after CC treatment was also observed by Fauzi [22]. The highest crystallinity in these samples has shifted from the 1235 mV in the as-deposited films to sample grown at 1240 mV after the CC treatment. Therefore, the preferred orientation in the CC annealed films is along the (100) hexagonal phase of CdS at $2\theta=\sim24.9^{o}$ for sample grown at voltage of 1240 mV. Though, most of the samples show comparable peak intensities for both the as-deposited and CC treated states.

Figure 6.3 shows the plot of the XRD peak intensities vs. growth voltage for the (a) as-deposited and (b) CC annealed layers of CdS. It is clearly seen that the intensity of (100)H peak in the as-deposited samples settled at ~100 counts for all samples. After annealing in the presence of CC, the samples showed an increase in their peak intensities indicating improved crystallinity in the layers. The highest peak intensity shifted from the growth voltage of 1235 to 1240 after the CC treatment. However, the intensities of these layers are still comparable. This shows that CdS layers with better crystallinity can be grown at a wide voltage range.

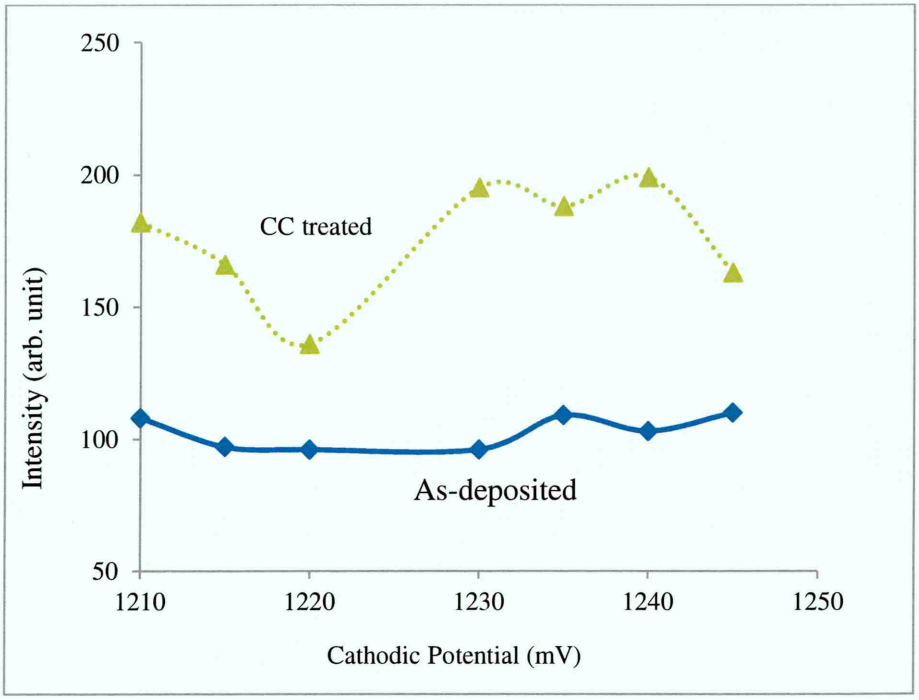

Figure 6-3: XRD peak intensity vs. growth voltage for as-deposited and CC treated thin films of CdS.

6.3.3 Optical studies

Figure 6.4 shows the plots of absorption coefficient, α versus photon energy (hv) for the (a) as-deposited and (b) CC treated CdS layers grown at different growth voltages. The plotted spectra are for layers grown at voltages close to the optimum growth voltage. All the layers were grown on glass/FTO substrates for one hour. After growth, the as-deposited sample at each growth voltage was cut into two samples. The first set of samples was left as-deposited and the other samples set was annealed in the presence of CC at 400°C for 20 minutes in air. The bandgaps in each case were estimated by extrapolating the straight line portion of the absorption coefficient edge to photon energy (at α=0) [24].

The bandgaps were obtained for as-deposited samples grown in the range (1210-1245) mV with the bandgaps scattered in the range (2.37-2.45) eV as shown in Table 6.1. It is observed that all the obtained bandgaps were close but lower than the bulk bandgap of CdS (2.42 eV) with no particular trend. The lower bandgaps values in the as-deposited layers could be attributed to the excess sulphur concentration in the deposition electrolyte.

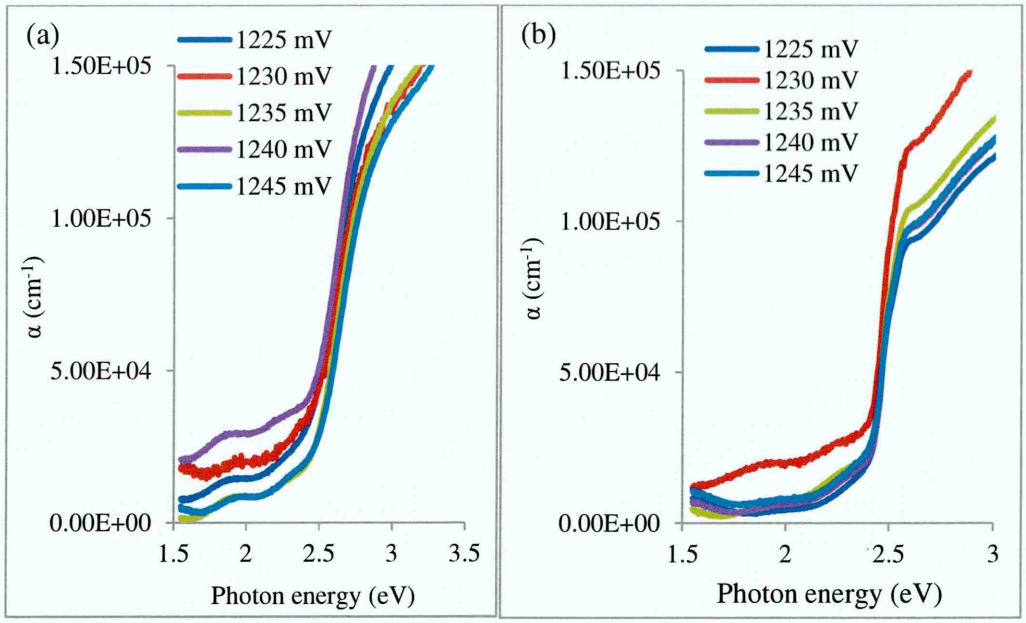

Figure 6-4: α vs hv (a) as-deposited and (b) CC treated CdS layers grown at different voltages.

After annealing in the presence of CC (Figure 6.4(b)), very interesting results in all the layers were observed irrespective of the growth voltage of the films. The estimated bandgaps for all layers show 2.42 eV equal to the bulk energy bandgap of CdS (E_g=2.42 eV) as seen in Table 6.1 and Figure 6.5. The decrease in the bandgaps of the as-deposited layers to lower photon energy corresponding to energy bandgap of 2.42 eV after CC annealing is interesting to see. This indicates the paramount importance of annealing thin films in the presence of CC in order to activate their optoelectronic photovoltaics for high performance solar cell devices. The advantages of the CC treatment include grain growth, recrystallisation and defect passivation [25]. During CC heat treatment, the small grains in the as-deposited layer will coalesce to form bigger grains which reduce the concentration of grain boundaries in the films. As a result, most of the grain boundaries are consumed thereby reducing light transmittance through these gaps and the measured bandgaps will give values close to the bulk bandgap of the CdS material.

This experiment has also shown that CdS thin films can be grown over a wide voltage range without compromising its essential optoelectronic properties suitable for application as a window material in the fabrication of relevant device structures.

Table 6-1: Variation of energy bandgap with growth voltage for the as-deposited and CC annealed CdS layers at 400°C for 20 minutes in air.

Growth voltage (mV)	Energy bandgap, E_g (eV)	
	As-deposited	CC treated
1215	2.38	2.42
1220	2.40	2.42
1225	2.38	2.42
1230	2.38	2.42
1235	2.40	2.42
1240	2.37	2.42
1245	2.40	2.42

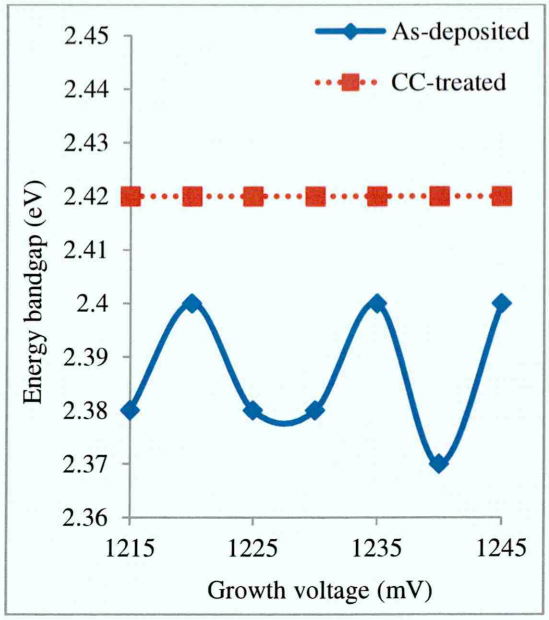

Figure 6-5: Energy bandgap estimation for as-deposited and CC treated CdS layers grown on glass/FTO substrates at different growth voltage range (1215-1245) mV for one hour.

Further to the absorption coefficient measurement analysis, the transmittance of the layers was estimated in the wavelength range (530-700) nm. Figure 6.6(a) shows that all the as-deposited samples measured within the wavelength range show transmittance in the range (58-95)%.

For the annealed samples in the presence of CC (Figure 6.6(b)), the transmittance of all layers is seen to slightly improve in the range (60-96)% with smooth and sharper absorption edges when compared with the as-deposited layers.

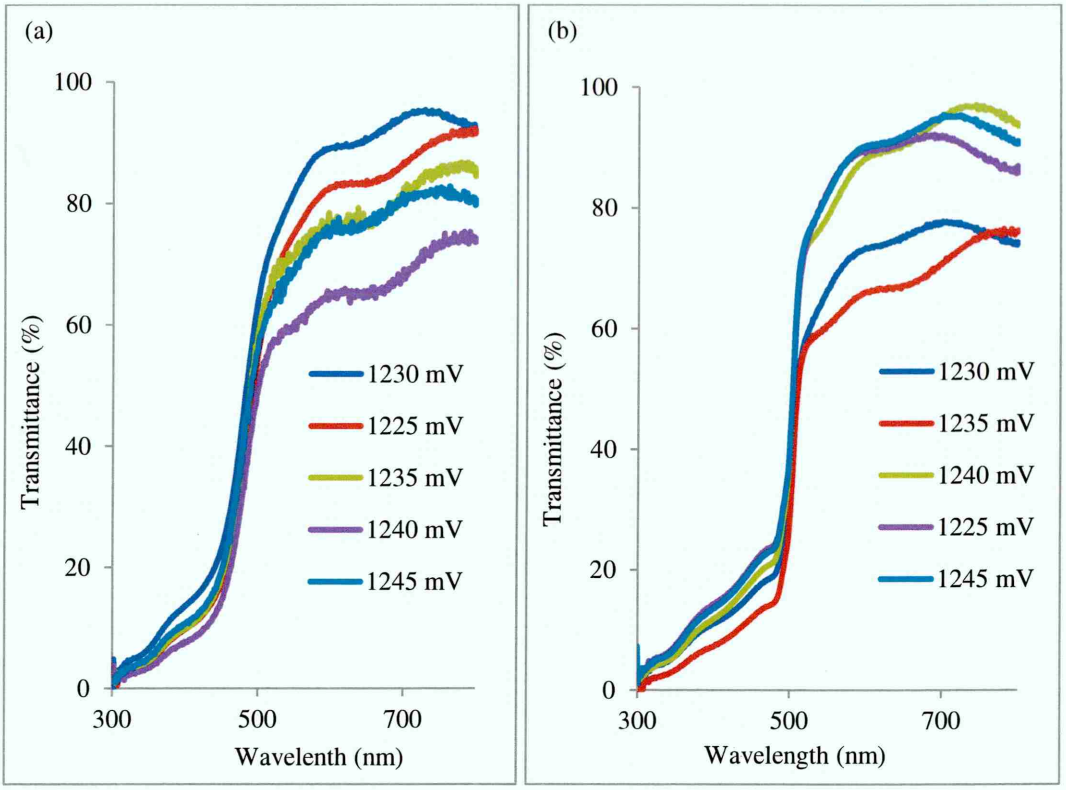

Figure 6-6: Transmittance spectra for (a) as-deposited and (b) CC treated CdS layers grown for one hour at different growth voltage (annealing was carried out at 400°C for 20 minutes in air).

6.3.4 Scanning electron microscopy

To study the effect of CC surface treatment of the CdS layers, a layer was grown on glass/FTO substrate for one hour at the optimised voltage of 1240 mV. Thereafter, the layer was divided into two samples. One piece was left as-deposited and the other annealed in the presence of CC at 400°C for 20 minutes in air for comparison.

Figure 6.7 shows the SEM images of (a) as-deposited and (b) CC treated CdS layer. It is seen that the as-deposited sample is covered with agglomerations of small grains showing good surface morphology with virtually no exposure of pinholes and fairly smooth morphology. After annealing in the presence of CC (Figure 6.7(b)), it is observed that the films show a very dense and compact morphology with reduced grain boundaries.

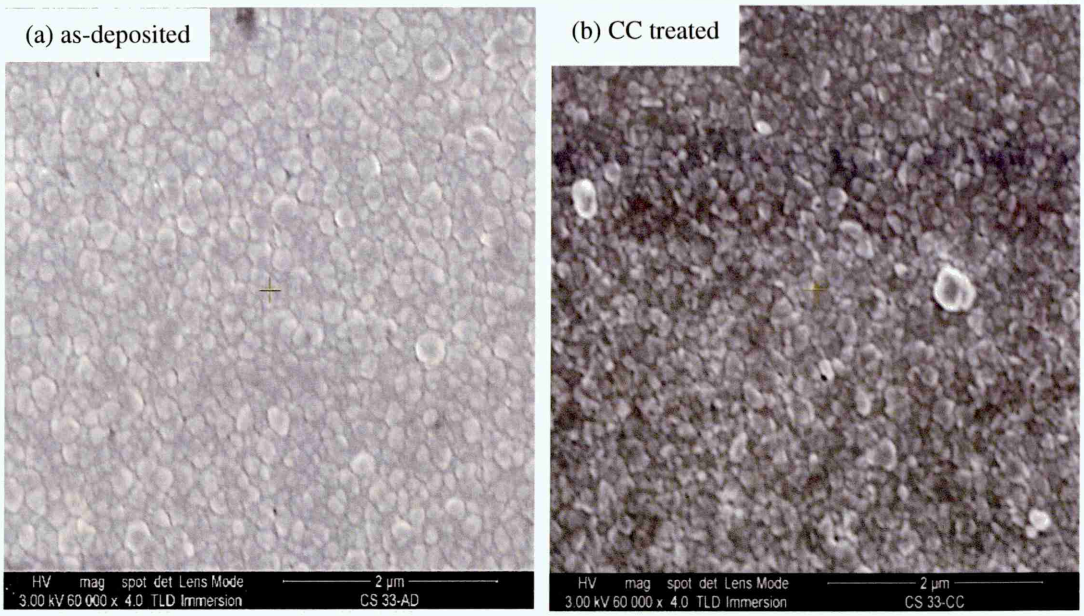

Figure 6-7: SEM images of (a) as-deposited and (b) CC treated CdS layers annealed at 400°C for 20 minutes in air.

6.3.5 Photoelectrochemical cell measurements

Photoelectrochemical (PEC) cell measurements of electrodeposited CdS grown at different growth voltages were carried out on both as-deposited (AD) and $CdCl_2$ (CC) treated samples to confirm the electrical conductivity type of the layers and to also study how the CC treatment affected the electrical properties of these layers. All samples were grown for one hour using a voltage range (1210-1245) mV. The as-deposited CdS layers grown at each voltage were divided into 2 samples and the first set of eight samples were left AD while the other set of eight samples were annealed in the presence of CC at 400°C for 20 minutes in air. All the samples in both as-deposited and CC treated cases, showed n-type behaviour. The magnitude of the PEC signal is seen to increase in the CC treated layers which are due to improvement in both structural and electrical properties of the layers. The measured PEC signal for AD and CC treated CdS layers grown at different growth voltages were summarised in Table 6.2 and plotted in Figure 6.8 for easy reference.

All samples show n-type electrical conductivity in both AD and CC treated conditions as expected. The naturally n-type electrical conduction type of CdS is attributed to S vacancies and Cd interstitials which are intrinsic donor defects in CdS semiconductor material [26].

Table 6-2: PEC cell measurements of AD and CC treated CdS layers grown at different voltages.

Growth voltage, V_g (mV)	PEC signal (mV)	
	AD	CC
1210	-35	-207
1215	-32	-251
1220	-36	-241
1225	-65	-244
1230	-66	-236
1235	-69	-231
1240	-24	-273
1245	-121	-243

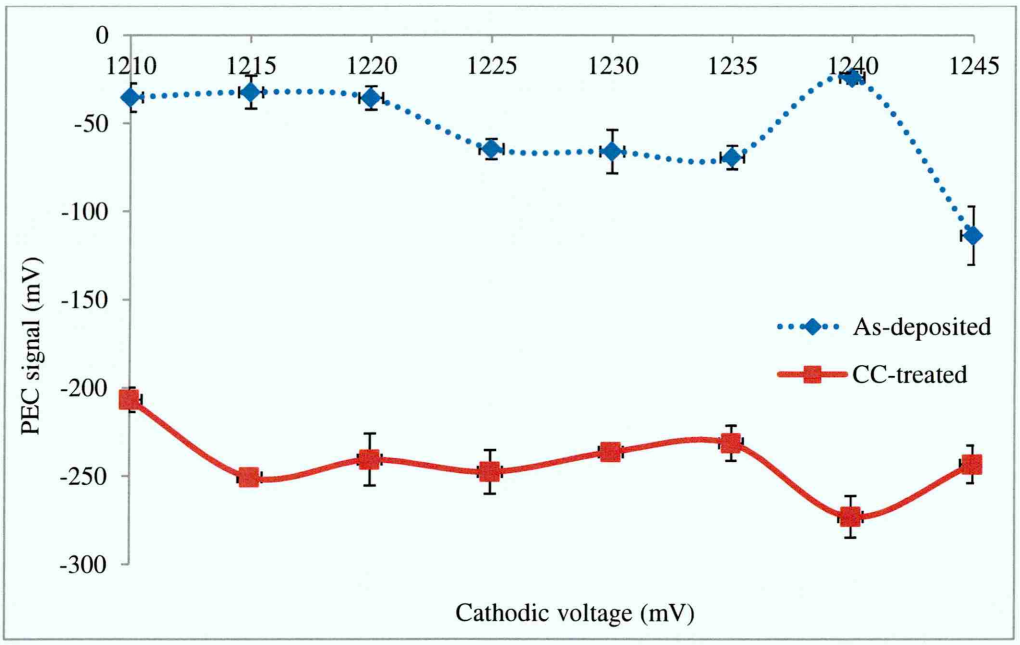

Figure 6-8: PEC signal measurements as a function of cathodic voltage for CdS layers grown at different growth voltages.

6.4 Conclusions

CdS thin films were successfully grown using electroplating technique from 2-elecrode system in a cathodic mode. The growth temperature and pH of all layers were ~85°C and 2.50±0.02 respectively. The suitable deposition voltage was established after

employing relevant characterisation techniques and the best growth voltage range was found to be between 1220 and 1250 mV.

Structural properties using XRD show that CdS thin films were polycrystalline in nature in both the as-deposited and CC treated cases. The as-deposited films, consist of sulphur rich layers with the elemental sulphur peak observed in layers grown at deposition voltage of 1220 mV. The XRD spectra show the presence of hexagonal and cubic crystal phases in both as-deposited and CC annealed layers. After annealing at 400°C for 20 minutes in the presence of CC, the peak related to sulphur is seen to disappear. The annealing process is usually carried out to improve the optoelectronic properties of the semiconducting layers. In this experiment, all bandgaps were observed to shift to the bulk bandgap of CdS (2.42 eV).

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Chapter 7: Electroplating and Characterisation of CdTe Absorber Material

7.1 Introduction

Presented in this chapter, are the results of CdTe thin films grown on glass/FTO substrates from aqueous acidic electrolyte containing 1 M $CdSO_4$ and TeO_2 using potentiostatic cathodic electrodeposition. ED-CdTe layers grown using three electrode (3E) and two electrode (2E) systems have been compared for their various properties using analytical techniques outlined in chapter 3. Optimisation of growth voltage using PEC cell measurement and XRD for both growth systems has been performed. The effects of $CdCl_2$ (CC) and $CdCl_2$+CdF_2 on the structural, optical, and electronic properties of the layers have been investigated. The study of defect structure of CdTe layers using PL has also been presented. The effect of CC treatment on the Fermi level movement on the CdTe layers was carried out using UPS.

7.2 Preparation of deposition electrolyte

The electrolytic bath was prepared from 800 ml de-ionised aqueous solution containing 1M $CdSO_4$ (purity ≥99%) and TeO_2 (purity 99.999%) in a 1000 ml Teflon beaker housed in a Pyrex glass of 2000 ml water bath containing de-ionised water. This helps to maintain uniform temperature of the deposition electrolyte. The solution containing only $CdSO_4$ was electro-purified for ~50 hours before adding the high purity dilute TeO_2 solution. This is done by applying a potential just below the reduction potential of Cd. The TeO_2 solution was separately prepared by dissolving 2g of TeO_2 powder in 230 ml of de-ionise water and sulphuric acid for addition into the electrolyte. The pH of the bath was adjusted to 2.00±0.02 using H_2SO_4 acid or NH_4OH at the beginning of experiment. The cathode (working electrode) and the anode (counter electrode) were glass/fluorine-doped tin oxide (FTO) substrate and Platinum sheet for both 3E and 2E systems. While the reference electrode used in the 3E system was a saturated calomel electrode (SCE).

The choice of materials to be employed for this experiment is very important since the medium of growth is acidic (pH=2.00). The acidic electrolyte has been shown to leach

out impurities from glass containers in direct contact than with Teflon containers [13], hence the Teflon beakers were used as the electrolyte containing vessel. This is to minimise impurities such as Na ions which are detrimental when incorporated into n-CdTe-based devices [1]. The outer jacket 2000 ml Pyrex glass filled with about 600 ml of de-ionised water houses the Teflon electrolyte containing beaker and this arrangement is usually done to maintain uniform temperature in the electrolytic bath.

7.3 Results and discussion

7.3.1 Cyclic voltammetry for 3E and 2E systems

In the electrodeposition (ED) method of semiconductor growth, cyclic voltammetry is usually employed to determine the approximate deposition potential for materials. This technique measures the current-voltage (I-V) through a conducting aqueous solution containing the ionic species of the semiconductor materials. Figure 7.1 shows the voltammogram scan for an aqueous solution containing 1M $CdSO_4$ and a small amount of TeO_2 for both 3E and 2E systems. The use of small amount of TeO_2 is due to the high difference in the reduction potential (E^0) values of the constituent species of Cd (E^0=-0.403 V) and Te (E^0=+0.593 V) [2] materials. The growth temperatures (T_g) were ~70°C and ~85°C for 3E and 2E systems respectively. The pH of the bath was adjusted to 2.00±0.02 in both configurations using dilute aqueous solution of H_2SO_4 or NH_4OH. The voltammograms with a scan rate of 3 mVs^{-1} was carried out using computerised Gill AC system in the cathodic voltage range of (0-1000) mV for the 3E and (0-2500) mV for the 2E systems respectively. The heat source was a hot-plate with attached stirring system. The relatively low temperature growth for the 3E is due to the manufacturer's temperature limit of 80°C for the reference electrode as earlier mentioned.

The mechanism for the deposition of CdTe on the cathode from acidic aqueous electrolyte as proposed by Panicker *et al.* [3] and was given below using equations 7.1 and 7.2. The first process is a diffusion control which involves the reduction of $HTeO_2^+$ to Te which reacts with Cd^{2+} to form CdTe on the cathode surface. The overall equations for the formation of CdTe on the cathode are given in equations 7.1 and 7.2.

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \qquad 7.1$$

$$Cd^{2+} + Te + 2e^- \rightarrow CdTe \qquad 7.2$$

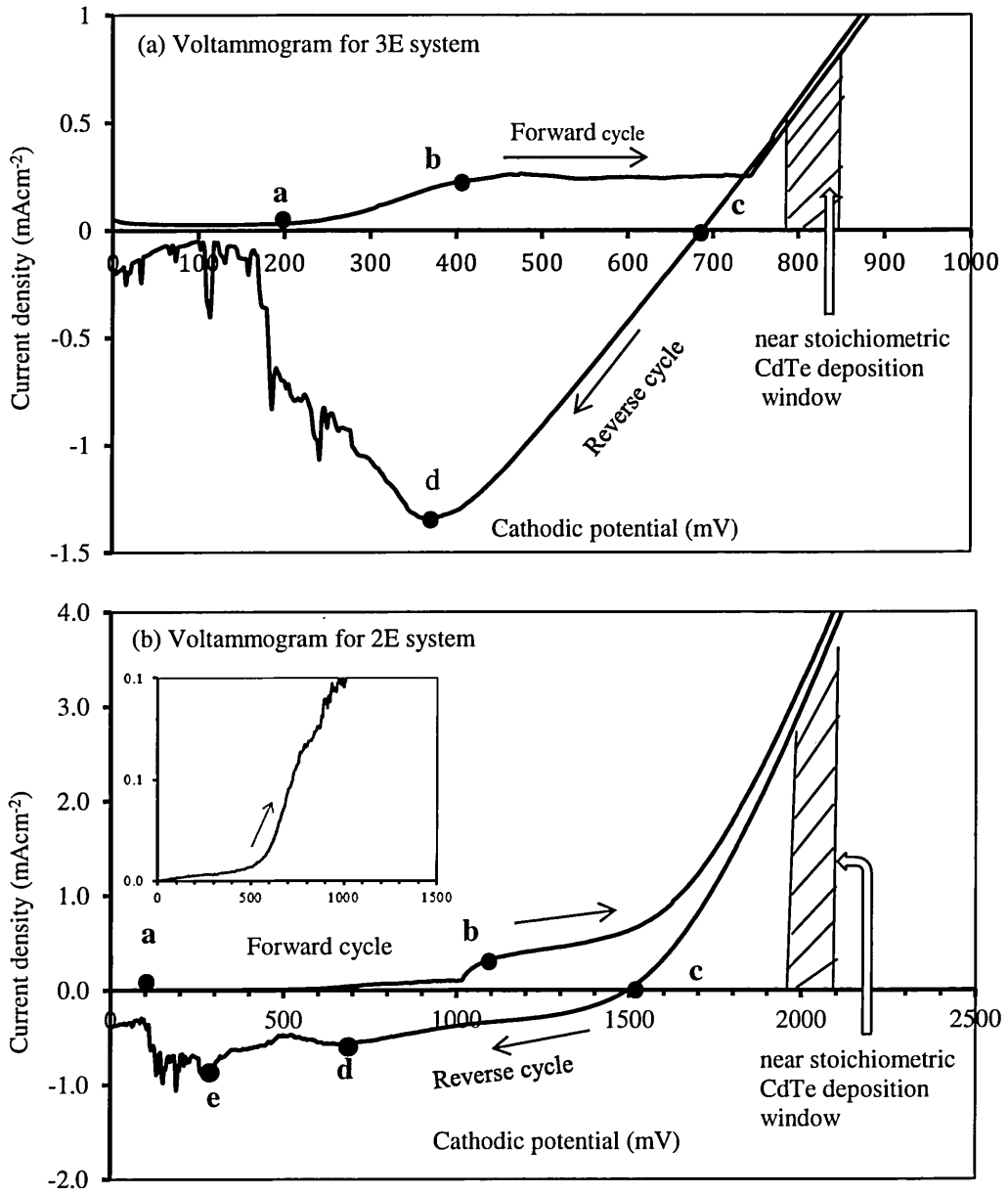

Figure 7-1: Cyclic voltammograms of aqueous solution consisting of 1M $CdSO_4$ and TeO_2 with glass/FTO cathode in (a) 3E and (b) 2E systems. The reference electrode used for the 3E system is standard calomel electrode (SCE).

The formation of CdTe thin films on the cathode is highly influenced by diffusion process. Looking at the voltammogram for the 3E system (Figure 7.1(a)) and with reference to the reduction potential (E^0) values of the elements involve in the electrochemical process, Te with redox potential of +0.593 V, will deposit first on the cathode and this starts at cathodic voltage around 200 mV (point *a*) and cadmium with

redox potential of -0.403 V starts to deposit at cathodic voltage around 450 mV (point ***b***). The deposition of near stoichiometric CdTe window was narrowed down and is indicated by the shaded portion of the voltammogram in the cathodic voltage range (780-840) mV. In the reverse cycle, it is observed that the dissolution of elemental Cd and Cd from CdTe starts to occur at growth voltage of 695 mV (point ***c***). A large negative peak at cathodic voltage around 370 mV (point ***d***) could be due to dissolution of Te from the cathode.

For the 2E system, Te deposition starts around 50 mV (point ***a***) as shown in the inset diagram of Figure 1(b) and Cd deposition starts around 1000 mV (point ***b***). The growth of near stoichiometric CdTe thin films window is narrowed down and is indicated by the shaded portion of the voltammogram in the cathodic potential range of (1950-2090) mV. At larger cathodic voltages, electrolysis of water is initiated and Cd dendrites starts to deposit on the cathode surface forming a mixed phase with poor material quality which cannot withstand device fabrication processes such as heat treatment and etching procedure. In the reverse direction elemental Cd and Cd from CdTe starts to dissolve. At cathodic voltage of 1500 mV (point ***c***) at this point, the deposition current becomes equal to dissolution current. Two negative peaks at points ***d*** and ***e*** are associated with the dissolution of Te.

7.3.2 Characterisation of CdTe thin films grown using 3E and 2E systems

7.3.2.1 X-ray diffraction

The X-ray diffraction (XRD) was carried out to study the structural properties of the CdTe thin films. In this study, the CdTe thin films were electroplated using 3E and 2E systems. Figure 7.2 shows the XRD spectra for the as-deposited (AD) CdTe layers grown using (a) 3E and (b) 2E systems, while Figure 7.3 shows the XRD spectra for the CdTe layers after $CdCl_2$ (CC) treatment (a) 3E and (b) 2E system. It shows that the growth voltages were changed in steps of 2 mV and 5 mV for 3E and 2E respectively in order to obtain the approximate deposition range for the growth of near stoichiometric CdTe material with the highest crystallinity. To achieve this, the growth voltage for the 3E (Figure 7.2(a)) was narrowed down in the range of (830-838) mV within the vicinity of the inversion voltage (V_i) and it shows that the material grown at the cathodic voltage of 834 mV shows better crystallinity with the highest (111) peak intensity for the as-deposited films. Therefore, this growth voltage is considered the best for the as-deposited materials.

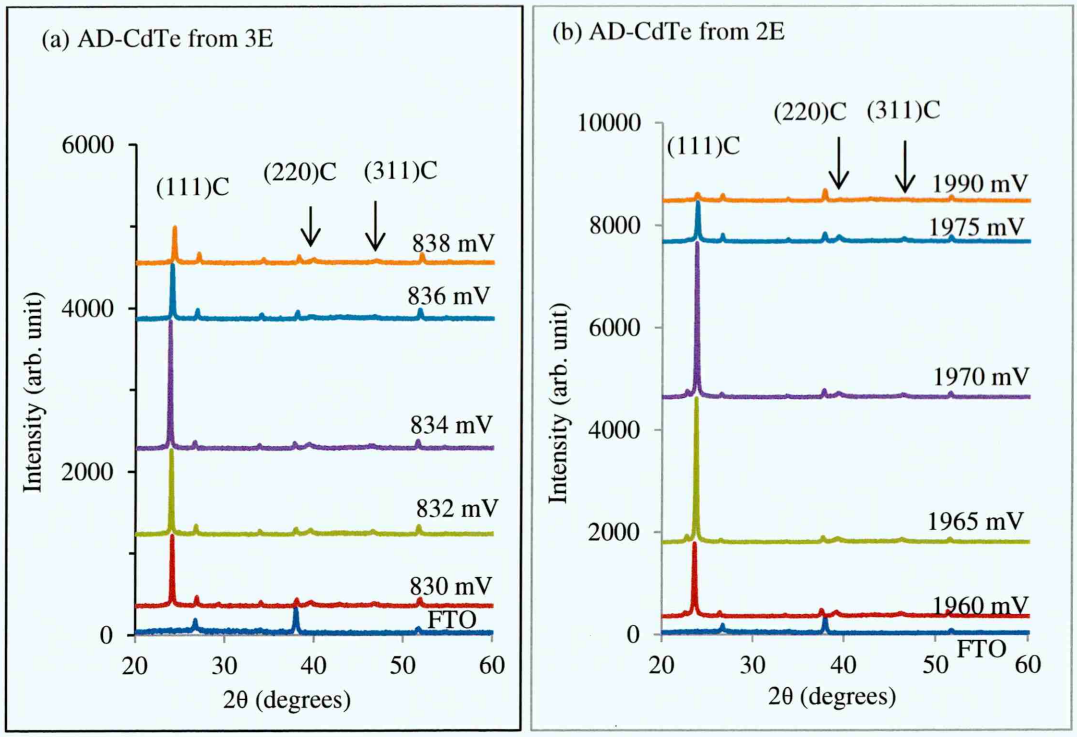

Figure 7-2: XRD spectra of as-deposited CdTe thin films deposited at different growth voltages using (a) 3E and (b) 2E systems.

Figure 7.2(b) shows the XRD spectra recorded for samples grown within the vicinity of the inversion voltage (V_i) for 2E systems. In this system, the deposition voltages were narrowed down in the range (1960-1990) mV, and the material grown at cathodic voltage of 1970 mV show the highest crystallinity hence it is considered the best growth voltage for the as-deposited material for the 2E system. The XRD pattern, irrespective of growth voltage and system (3E or 2E) the CdTe thin films are polycrystalline in nature with strong preferred orientation along the (111) cubic phase of CdTe at $2\theta = \sim 24.0^{o}$. CdTe usually grows with a preferred orientation along the (111) peak for low temperature grown materials irrespective of the growth method [4]. Other two weak peaks at approximately 2θ values of $\sim 39.8^{o}$ and $\sim 46.7^{o}$ correspond to reflections from (220) and (311) cubic phases of CdTe respectively. These peaks data matches well with Joint Committee on Powder Diffraction Standards (JCPDS) reference file number 01-075-2086.

The strict requirements in the quality of materials for application in solid-state electronics especially solar cells are not only important but necessary for optimum device performance. The as-deposited films are usually not suitable for application in solar cell due to their poor electronic properties as a result of defects and high density of grain boundaries. Therefore, the as-deposited materials must undergo a post growth heat

treatment in the presence of $CdCl_2$ (CC) or $CdCl_2$+CdF_2 (CF) or any other suitable Cl containing salt. After CC heat treatment, for layers grown using 3E system (Figure 7.3(a)), the highest crystallinity in the sample grown at 834 mV in the as-deposited films shifted to a layer grown at 830 mV. This is attributed to recrystallisation and annealing out defects in these materials. Therefore, 830 mV is taken as the best material growth voltage for the 3E system with respect to SCE under the experimental condition used in this work.

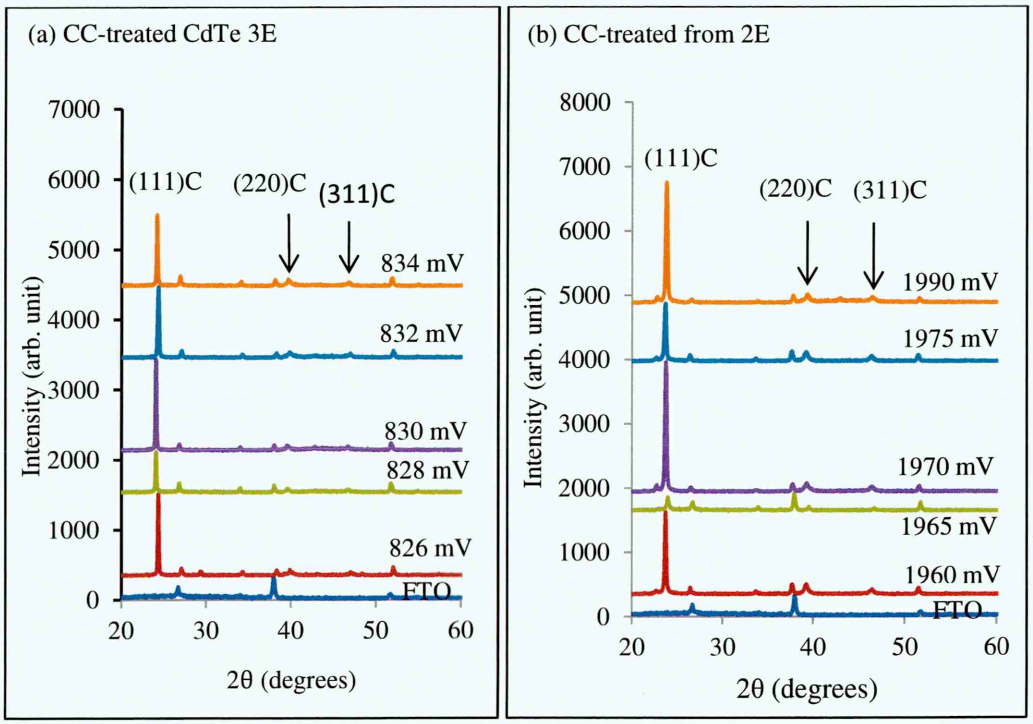

Figure 7-3: XRD spectra of CC treated CdTe thin films deposited at different growth voltages using (a) 3E and (b) 2E systems. All heat-treatments were carried out at 400°C for 15 minutes in air.

In the 2E system, the material grown at 1970 mV was identified as the best and near stoichiometric with the highest (111) peak intensity in both as-deposited and after CC-treatment (see Figure 7.3(b)). The XRD patterns in both growth configurations look very similar, but the growth rate is faster in 2E system which comes with advantages of growing comparably thicker layers with better crstallinity and reduced time for manufacturing process. In the case of heat treated samples in the presence of CC, the (220) and (311) show very weak peaks. This is because the CdTe layers at low temperature, preferentially grow along the (111) orientation.

It is important to get materials that show highest possible XRD peaks which mean high crystallinity suitable for applications in solar cells. Table 7.1 shows the summary of the

XRD parameters obtained for the best materials in the as-deposited and the CC treated CdTe thin films with respect to the (111) peak. The parameters obtained from the XRD machine includes; the angle position (2θ), d-spacing (Å) and crystallite size. The crystallite size (D) of the films was calculated using the full width at half maximum (FWHM), β, using the Scherer's formula [5] given in equation 7.3.

$$D = \frac{0.94\lambda}{\beta \cos\theta} \qquad 7.3$$

Where D is the crystallite size in nm, β is the FWHM in radian, λ =1.54 Å is the wavelength and θ is the position of the angle in degrees (Bragg's angle).

The obtained parameters in the table show that the surface treatments have modified their structural properties which indicate recrystallisation, defects passivation and the release of compressive stress incorporated into the material during growth. The crystallite sizes were calculated for the best growth voltages for 3E and 2E systems.

Table 7-1: Summary of XRD data for the best growth voltages for as-deposited (AD) and CC treated CdTe layers grown using 3E and 2E systems.

Growth system	Treatment	V_g (mV)	2θ (deg.)	d-spacing (Å)	FWHM (deg.)	Crystallite size, D (nm)	Plane of orientation	Assignment
3E	AD	834	23.9	3.73	0.162	52.3	(111)	CdTe/Cubic
	CC	830	24.1	3.70	0.129	65.2	(111)	CdTe/Cubic
2E	AD	1970	23.8	3.73	0.162	52.3	(111)	CdTe/cubic
	CC	1970	23.7	3.73	0.129	65.2	(111)	CdTe/cubic

In XRD, the magnitude of intensity signifies how crystalline a material is. While it is desirable to fabricate solar cells with highly possible crystalline materials, the photovoltaic output of the devices does not solely depend on the crystallinity of the material but equally on some other important factors such as the quality of the heterojunction, optimum doping concentration etc. Another observation is the decrease in the full width at half maximum (FWHM) from 0.162 Å in the as-deposited to 0.129 Å for layers annealed in the presence of CC for both systems. This indicates grain growth and recrystallisation in these films [6]. In other words, crystallite size increases with decrease in FWHM as shown in Table 7.1.

7.3.2.2 Effect of $CdCl_2$ and $CdCl_2$+CdF_2 treatments on the XRD pattern of CdTe thin films at different temperatures grown using 2E system

In this experiment, a CdTe layer of ~800 nm thick was grown on glass/FTO substrate. The as-deposited layer was divided into 7 pieces of smaller samples. The first part was left as-deposited and second 3 samples were annealed in the presence of $CdCl_2$ (CC) at 380, 420 and 450°C while the last 3 samples were annealed in the presence of $CdCl_2$+CdF_2 (CF) at 380, 420 and 450°C. All heat-treatment was carried out for 20 minutes in air and the XRD patterns for this experiment are shown in Figure 7.4.

Figure 7.4(a) and 7.4(b) show XRD patterns of CdTe thin films annealed at different temperatures in the presence of CC and CF respectively. In each case the AD sample was included in the XRD pattern for easy comparison. Heat treatment at 380°C in the presence of CC and CF for both layers improved the intensity of (111) peak. Therefore, the (111) peak is considered the preferred orientation when compared with the very weak intensities of the (220) and (311) peaks. The increased in intensity of the (111) peak is attributed to grain growth and recrystallisation induced by the respective treatments.

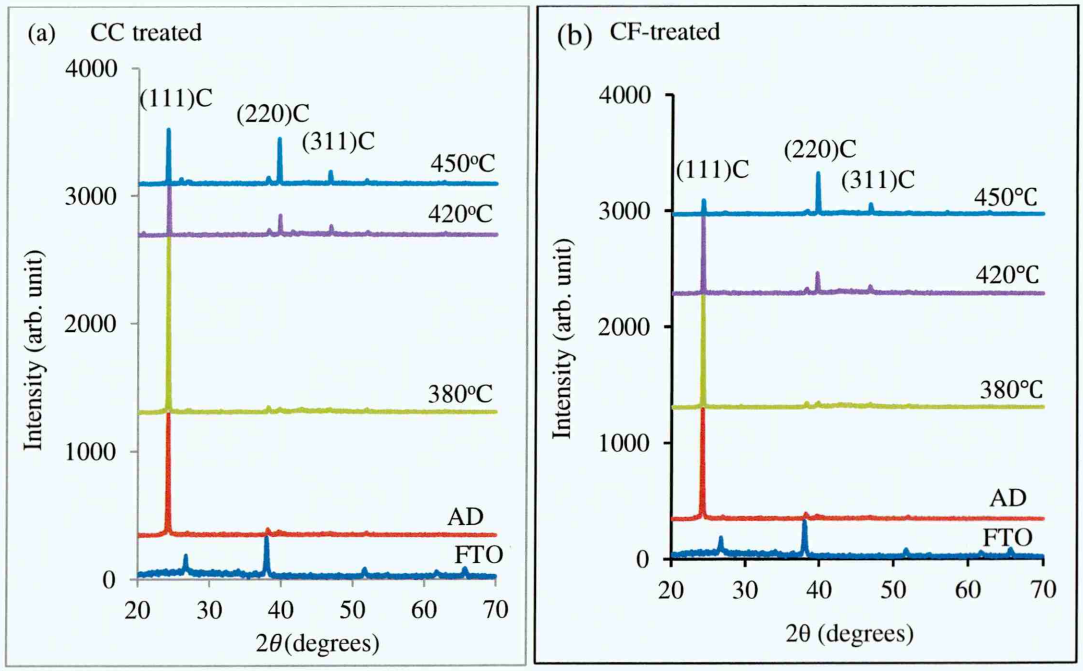

Figure 7-4: XRD patterns of CdTe thin films of (a) CC and (b) CF treated at different temperatures for 20 minutes in air,

After annealing at 420°C, a structural transition is noticed in films treated in both CC and CF due to a reduction in the intensity of the (111) peak. This transition has to do with the drastic reduction of the (111) peak and the improved intensity of the (220) and (311) peaks indicating that these peaks do not share same temperature regime with the (111) peak [7] as earlier mentioned. To further buttress this point, it was observed that the (220) and (311) peaks increased only at temperature at which the (111) peak collapse. These structural transitions have to do with further recrystallisation and randomisation of the layers in both treatments at this temperature [8]. This random nature is associated with the melting of the grain boundaries due to the incorporation of CC or CF impurities which are known to diffuse into the grain boundaries during the annealing process impacting positively on the optoelectronic properties of the material. The CdTe crystals floating in melted grain boundaries during heat treatment will recrystallise and freeze in random manner after cooling. In an experiment to monitor the phase transition of CC treated CdTe, Kim *et al.* [9] have reported similar observations at this temperature range.

At 450°C, it was observed that, the intensity of the (111) peak in sample treated with CC increased slightly while the (220) and the (311) peaks show further increase in their intensities with the (220) peak being more prominent with almost same intensity level with the (111) peak. However, a very interesting result occurs in sample treated in the presence of CF which show complete collapse of the (111) peak with the highest intensity transferred to (220) peak. The (220) peak is now the preferred orientation in this sample since its peak intensity is the highest when compared with other peaks.

To better understand and summarise the varied temperature transition regimes in the phase transition of CdTe material as reported by many researchers as discussed above, Dharmadasa *et al.*[14] identified 3 regions with 2 transition temperatures in the phase transition of low temperature grown CdTe thin films as shown in Figure 7.6. This Figure illustrates the XRD patterns, grains orientation, and approximate efficiencies at each temperature regime. Region1 indicate low-temperature growth regime in which the CdTe grown at this region show strong preferred orientation along the (111) cubic phase of CdTe and the two other peaks of (220) and (311) are weak in this region. In the second region, the (111) peak is seen to collapse while the intensity of (220) and (311) peaks are enhanced. The transition from region 1 to region 2 is at temperature of 385±5°C which matches well with the result obtained in this experiment. So region 2 is at $385^{\circ}C < T < 430^{\circ}C$ temperature range and the transition to region 3 is at temperature

of ≥430°C. As observed, the experimental results presented in this work matches well with descriptions given by Dharmadasa *et al.* [10]. In an experiment using the alternative low-cost ultrafast intense pulsed light (IPL) heat treatment of CC treated CdTe carried out by Dharmadasa *et al.* [12] and Druffel *et al.* [13] have also reported similar observations suggesting the transition and the randomised texture of the CdTe at region 2 is attributed to the melting of the grain boundaries due to the incorporation of the Cl impurities during annealing process.

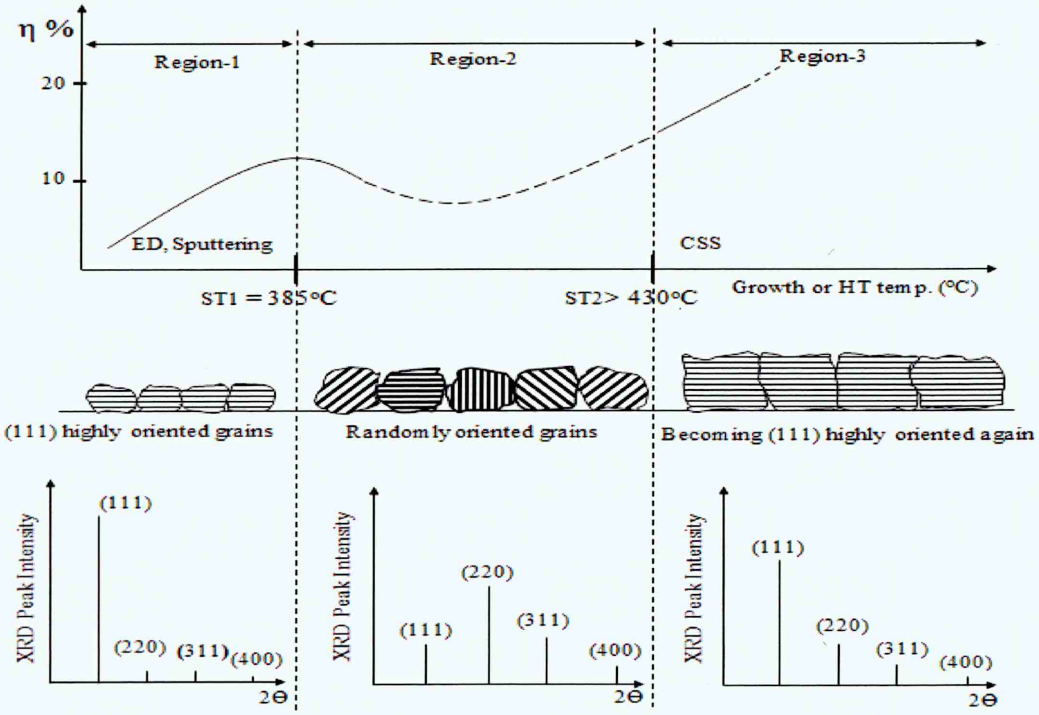

Figure 7-5: Schematic diagrams of CdTe XRD transition patterns, grain orientation and probable solar cell efficiencies as a function of growth/annealing temperature. Figure adapted from ref. [10].

The heat treatments temperatures of 380, 420 and 450°C utilised for device optimisation in chapter 8 were based on the experiment shown on Figure 7.5 which shows how efficiencies fares with annealing temperatures. This Figure shows that better efficiency devices are obtained when annealed at temperatures of around 400°C and above.

Figure 7.6 presents the graphs of the variation of the intensity of the (111), (220) and (311) at different annealing temperatures for (a) CC and (b) CF treated samples respectively and (c,d) are the corresponding crystallite sizes for the CC and CF treated layers respectively. The optimum temperature for heat treatment is therefore just above 400°C. Beyond this temperature, material degrades again.

As observed in Table 7.2, the crystallites gradually increase from as-deposited to layers annealed at 420°C in each case but decreased to 52 nm at 450°C for both treatments. This could be due to the disintegration of the crystals within larger grains into smaller crystallite sizes at higher temperatures [15,16]. This can also be associated with the relaxation of excessive stress in the crystal lattice [17]. Moutinho *et al.* [18] reported a reduction in the crystallite size of their CSS grown CdTe layer from 2.7 μm in the as-deposited to 2.6 μm after annealing at temperature of 400°C in the presence of CC. One other reason is the sublimation of CdTe at higher temperatures, and this was clearly shown in a similar work by Abdul-Manaf [19].

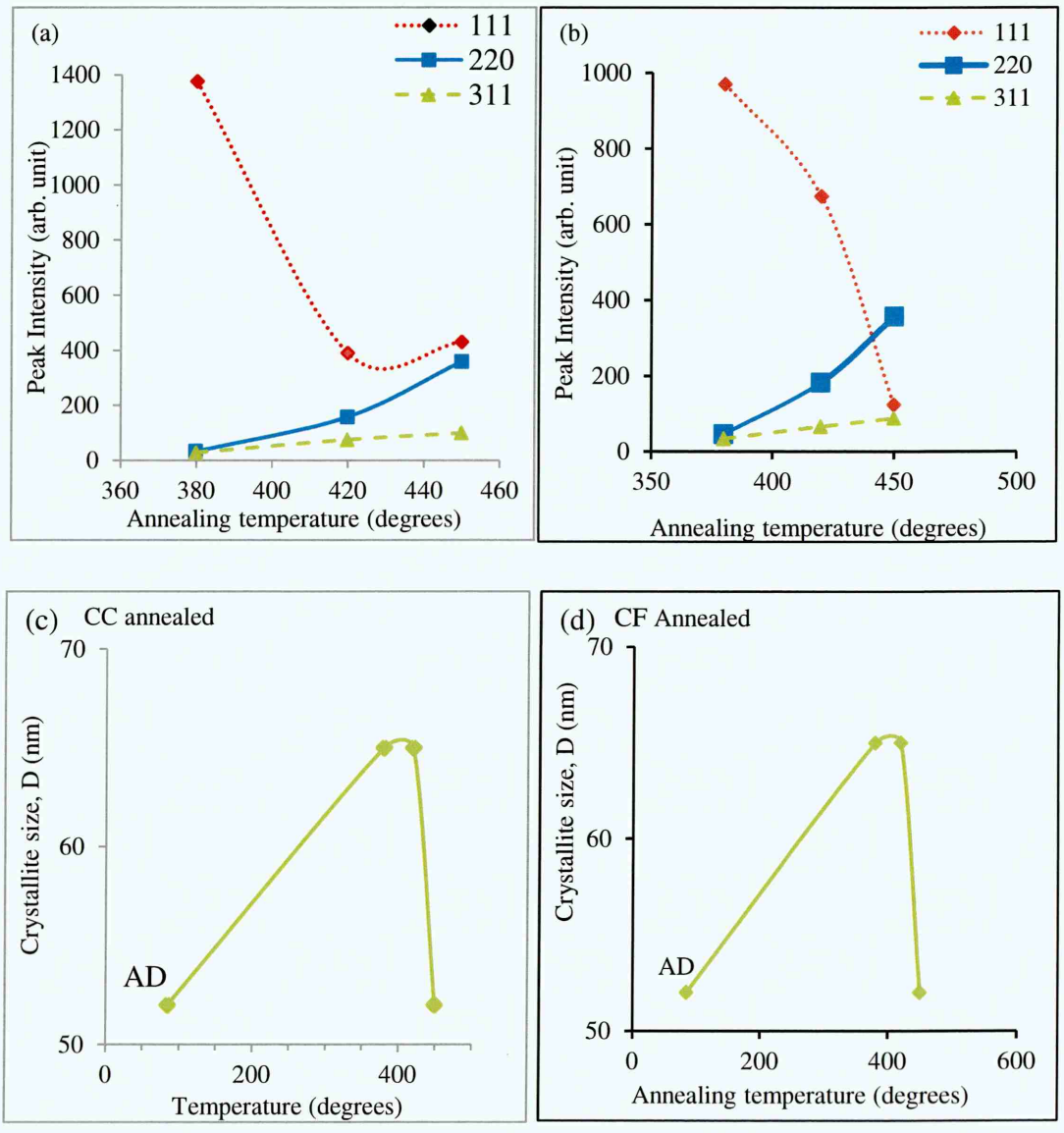

Figure 7-6: Variation of intensities of the (111), (220) and (311) peaks as a function of annealing temperature (a) CC & (b) CF respectively and (c) & (d) are respectively the corresponding crystallites sizes for the CC and CF treated layers.

Table 7-2: Summary of FWHM and crystallite size for layers treated with CC and CF at different temperatures.

Treatment		2θ of (111) peak (degrees)	FWHM of (111) peak (degree)	Crystallites size of (111) peak (nm)
AD		24.20	0.162	52
CC-treated	380°C	24.24	0.129	65
	420°C	24.27	0.129	65
	450°C	24.13	0.162	52
CF-treated	380°C	24.24	0.129	65
	420°C	24.21	0.129	65
	450°C	24.25	0.162	52

Many reports in the literature have shown the positive effects of the inclusion of F in the usual CC treatment. Romeo *et al.* [20] have demonstrated the use of Freon, a F containing gas in the CC annealing achieving efficiency of about 16%. Echendu *et al* [21] and Fauzi [22] have recently reported a better solar cell device parameters with films annealed in the presence of CF than with the usual CC treatment. The work reported in this thesis has also achieved better device parameters with films annealed in the presence of CF than with the usual CC treatment. Fluorine (F) is one of the group VII (halogens) elements with the least atomic radii, than that of Cl which makes it easier to diffuse through the grain boundaries [21] impacting positively on both the structural and electronic properties of the layers.

7.3.2.3 Effects of growth temperature on XRD patterns of CdTe thin films grown using 2E system

This experiment was performed by growing four CdTe layers at different temperatures of 25, 45, 65 and 80°C on Te-rich side close to the V_i in order to reveal any significance influence of the CC treatment on the layers. After deposition, sample grown at each temperature was cut into 2 pieces one part left as-deposited and the other part annealed in the presence of CC. Figure 7.7 shows the XRD patterns of four samples of (a) as-deposited and (b) CC annealed CdTe thin films. Annealing was carried out at 400°C for 15 minutes in air.

In the as-deposited (AD) films (Figure 7.7(a)), the CdTe layers grown at temperatures of 25 and 45°C show complete amorphous behaviour with no XRD peaks due to CdTe. When the growth temperature was increased to 65°C, a peak along the (111) cubic phase of CdTe starts to emerge. Further increase in the (111) peak and the emergence of (220) and (311) peaks are noticed for sample grown at 80°C. This indicates improved crystallinity due to the increase in the deposition temperature. The XRD pattern of glass/FTO substrate was also included to help identify peaks due to FTO layer.

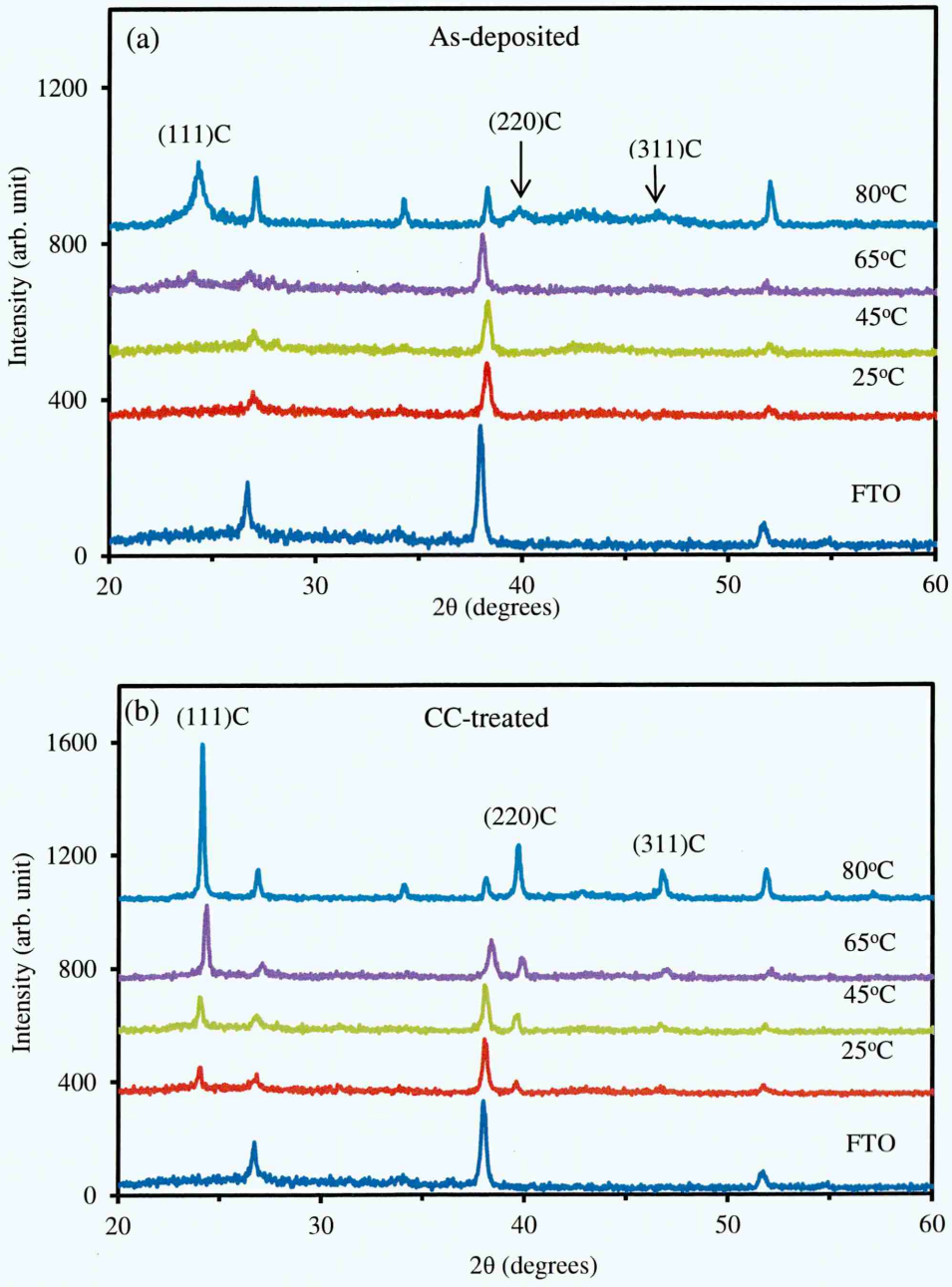

Figure 7-7: XRD pattern of CdTe thin films grown at different temperatures for (a) as-deposited and (b) CC-annealed at 400°C for 15 minutes in air.

Figure 7.7(b) shows the XRD spectra for the samples annealed in the presence of CC. All samples show improved crystallinity due to the CC heat treatment. All the films show preferred orientation along the (111) peak as expected. Another noticeable influence of this treatment is the appearance of the (111), (220) and (311) peaks even in samples grown at 25 and 45°C which were completely missing in the as-deposited films. This is expected since the heat treatment temperature of 400°C exceeds the first transition temperature of 385±5°C. The crystallinity of the peaks is seen to gradually increase with increase in the growth temperature with the highest peak observed in film grown at the temperature of 80°C. As mentioned earlier, the (111) cubic phase of CdTe remains the dominant peak in all the layers. This shows the influence of the growth temperature on the structural properties of the CdTe layers. This result has also shown that thin films require high temperature growth or post growth annealing process in order to attain high quality materials appropriate for application in electronic devices such as solar cells. This is because materials grown at room temperature show poor crystallinity due to excess Te [23].

7.3.2.4 Morphology of CdTe layers grown using 3E system

Figure 7.8 shows three CdTe layers grown for 1 hour using 3E system at three different cathodic voltages of 826, 828 and 830 mV within the vicinity of the V_i. After growth, each sample was cut into three parts for as-deposited (AD), $CdCl_2$ (CC) and $CdCl_2$+CdF_2 (CF) treatments.

Figure 7.8 (a-c) shows AD, CC and CF treated CdTe layers grown at 826 mV and Figure 7.8 (d-f) shows AD, CC and CF annealed CdTe layers grown at 828 mV while Figure 7.8 (g-i) shows AD, CC and CF treated CdTe layers grown at 830 mV. The AD films in each case were covered with large clusters or agglomerations of small grains consisting of nano-crystallites. The clusters have varying sizes up to sub-micron sizes for largest ones. The small cluster size is in the range (200-400) nm. The morphology of this layer shows fairly compacted clusters with scattered pinholes. After annealing in the presence of CC and CF at 400°C for 15 minutes in air, the films show grain growth and recrystallisation becoming more compact with an increase in the average cluster size in the range (200-500) nm for both layers annealed in the presence of CC and CF respectively. It is observed that layers annealed in the presence of CF in each case show better crystallinity indicating compact and less pinholes when compared with the other treatments which could be due to the incorporation of F.

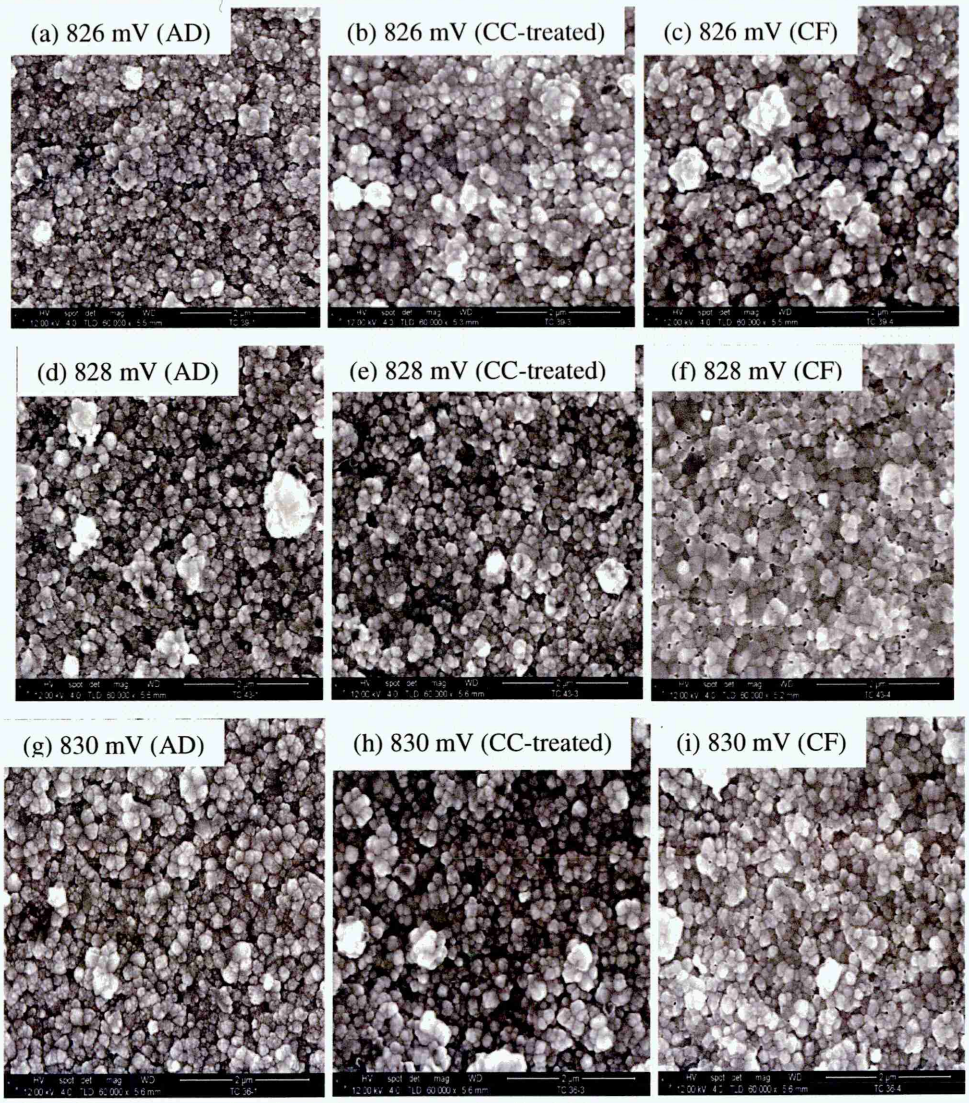

Figure 7-8: Typical SEM images for CdTe thin films grown at different growth voltages using the 3E system. All annealing was done at 400°C for 15 min in air.

7.3.2.5 Effect of $CdCl_2$ and $CdCl_2$+CdF_2 on the surface morphology of CdTe thin films grown using 3E system and annealed at different temperatures.

This study was carried out to study the effect of CC and CF on ED-CdTe layers grown using the 3E system. A CdTe film of ~700 nm thick was grown on glass/FTO substrate. After growth, the as-deposited sample was cut into seven smaller samples. One of the samples was left as-deposited, 3 samples were annealed with CC at temperatures of 380, 420 and 450°C and the other 3samples were annealed with CF at the same temperatures of 380, 420 and 450°C. All Samples were annealed for 20 minutes in air.

Figure 7.9 (a-d) shows the as-deposited and samples annealed in the presence of CC at different temperatures. The AD film shows agglomerations or clusters of grains covering the glass/FTO substrate revealing rough surface with cluster size in the range

(20-300) nm. After annealing at 380°C (Figure 7.9(b)), the smaller grains coalesced to form bigger ones. The grain sizes in this film were in the range of (200-400) nm. At a temperature of 420°C (Figure 7.9 (c)), the small grains further coalesced to form larger ones as a result of recrystallisation and grain growth. The 420°C annealed layer show a substantial increase in grain size in the range (400-600) nm. The morphology of this film revealed rough surface with pinholes. The white powder-like particles seen on the CdTe surface annealed at 420 and 450°C are residues from the CC treatment carried out prior to the CC- annealing step. It was observed that the layer annealed at 450°C (Figure 7.9 (d)) shows a drastic increase in the grain size. The morphology exhibit closely packed and dense surface with grain size in the range (400-1000) nm.

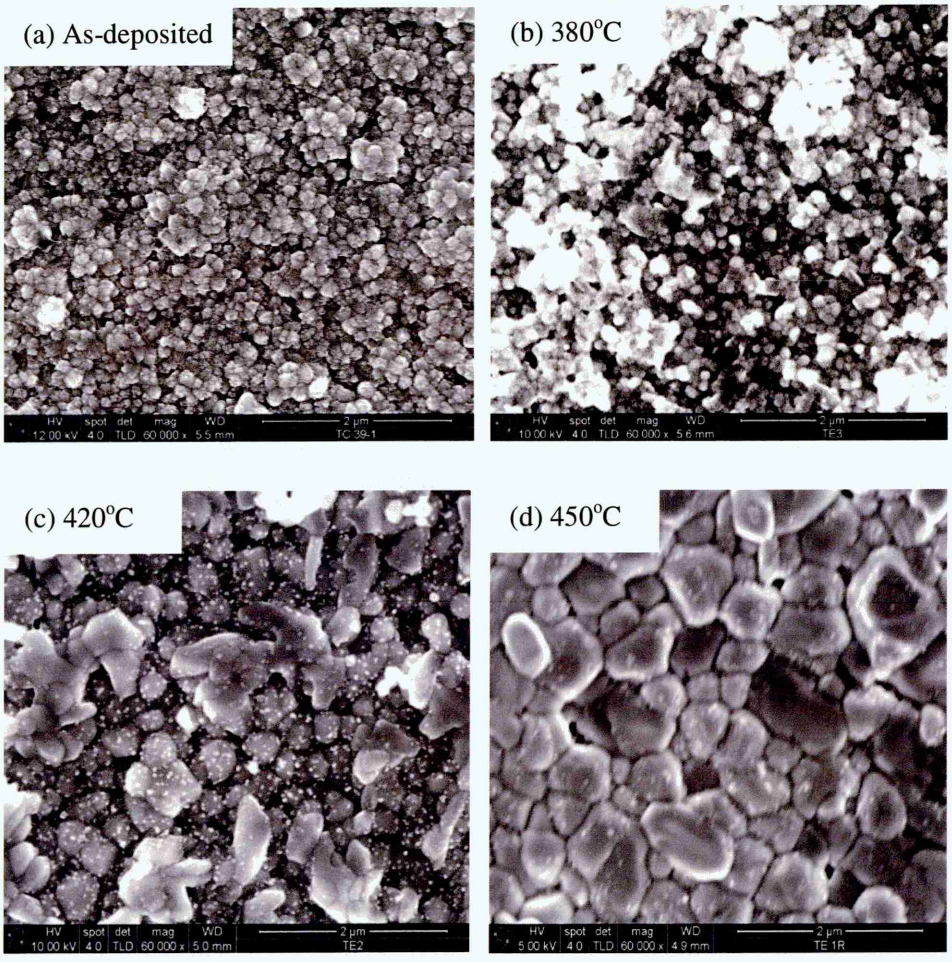

Figure 7-9: SEM images of as-deposited and layers annealed at different temperatures in the presence of CC. Annealing time was 20 minutes in air atmosphere.

Figure 7.10 (a-d) shows CdTe thin films of AD and samples annealed in the presence of CF at different temperatures. The AD sample is same with the previous one in the CC treated layers. The layer annealed at 380°C is seen to have grain clusters with respect to the as-deposited one. The increase in the grain growth is associated with coalescence of

small grains to form larger ones resulting from the CF treatment and the annealing temperature. The grain sizes in this film were in the range (200-350) nm. At 420°C the grain sizes increased to the range of (400-550) nm which also showed clear demarcation between grain boundaries in this film. The layer annealed at 450°C show further increased in the average grain sizes of up to 1500 nm. This layer exhibits closely packed and dense surface morphology.

The as-deposited CdTe consist of small grains with strong preferred orientation along the (111) cubic phase of CdTe but at ≥385°C, rapid structural transition occurs in the CdTe. At temperatures greater than 385°C, grain boundaries begin to melt depending on the amount of CC or CF concentration diffused into the grain boundaries during heat treatment. The sample annealed at the temperature of 420°C falls within this second region and it shows a melted like morphology and hence the collapse of the (111) peak.

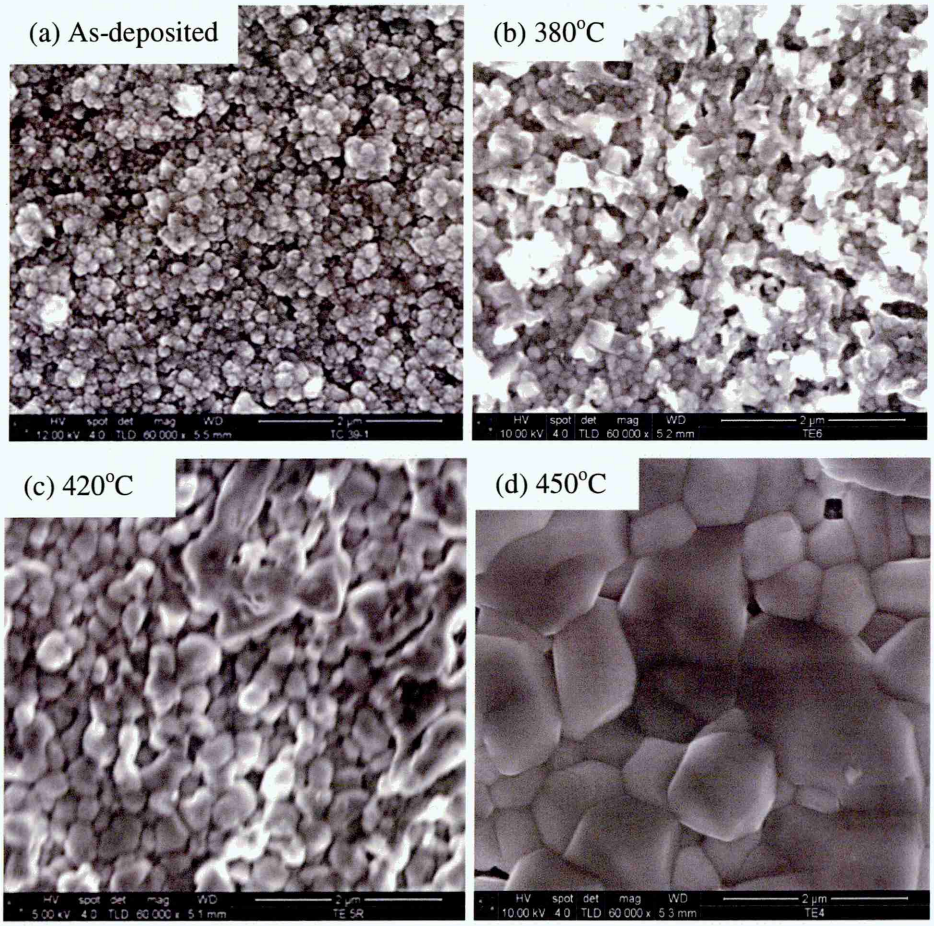

Figure 7-10: SEM images of as-deposited and layers annealed at different temperatures in the presence of CF. Annealing time was 20 minutes in air atmosphere.

Observation from sample annealed at 450°C shows a drastic reduction in grain boundaries and defect density with increased in grain sizes. While the increased in grain

sizes is a desirable property, it also increases the surface roughness and sometimes may open up pinholes in the films which can negatively affect device performance by creating shunting paths. It is for this reason that both layer thickness and heat treatment need to be systematically optimise to reduce these effects. As expected, the images show an increase in grain size as the annealing temperature is increased.

7.3.2.6 Effect of $CdCl_2$ and $CdCl_2$+CdF_2 on the morphology of CdTe thin films grown using 2E system and annealed at different temperatures

This experiment was carried out to investigate the effect of $CdCl_2$ (CC) and $CdCl_2$+CdF_2 (CF) on the morphology of as-deposited CdTe thin films using ~800 nm thick layer grown on glass/FTO substrate. All heat treatments were carried out for 20 minutes in air. To carry out this investigation, SEM technique was employed to study the surface morphology of the CdTe thin films. The as-deposited sample was divided into seven smaller samples. The first part was left as-deposited with no surface treatment. The next 3 samples were annealed in the presence of CC at 3 different temperatures of 380, 420 and 450°C and the last 3 samples were annealed in the presence of CF at 380, 420 and 450°C. The SEM magnification of 60,000 was used for this experiment.

Figure 7.11 shows as-deposited and samples annealed in the presence of CC at different temperatures. In the as-deposited films (Figure 7.11(a)), the film is covered with closely packed and dense clusters or agglomerations of grains. The morphology show few scattered pin-holes with grain cluster size in the range of (200-400) nm with relative smooth surface. After annealing at 380°C (Figure 7.11 (b)), the as-deposited clusters coalesced to form larger ones as observed. However, this coalescence opens up gaps in between grain boundaries in the films. The grain cluster size in these films is in the range (200-500) nm. At 420°C (Figure 7.11(c)), a significant increase in the grain size is observed due to coalescence of grains clusters. Unlike in the previous films, the grain boundaries are obvious and clearly mapped. The average cluster sizes of (200-500) nm in the previous film have coalesced to produce grain size of (300-1000) nm in this film.

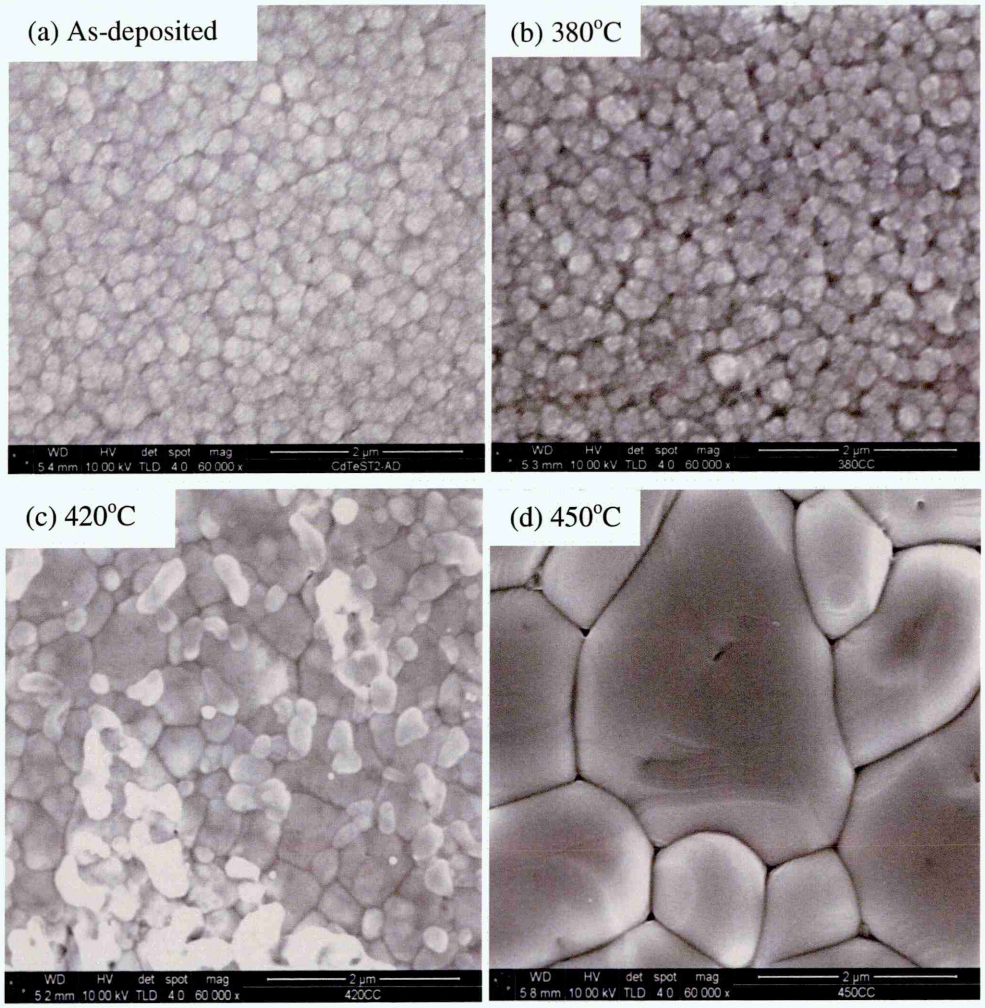

Figure 7-11: As-deposited and CdTe thin films annealed at different temperatures in the presence of CC for 20 minutes in air.

Heat-treatment at 450°C show further improvement due to coalescence of grain clusters resulting in drastic increase of grain size with well-defined and reduced number of grain boundaries. The grain size in this film is in the range (1000-3000) nm. Figure 7.11 (a-d) shows the gradual increase in the grain size as the heat treatment temperature is increased. While the increase in grain size is induced by the CC treatment, it is directly dependent on the temperature. The literature is rich with reports on the influence of the CC heat treatment on the structural and morphological properties of CdTe thin films. The CC treatment is known to increase grain growth and recrystallisation [24,25], with benefits such as grain boundary passivation, increased grain size, reduction of grain boundaries, annealing out defects, CdS/CdTe interface alloying and improved solar cell performance [11,15,26–28]. These benefits will enhance carrier collection due to drastic reduction in grain boundaries which acts as scattering centres or traps for charge carriers [29].

Figure 7.12(a-d) shows the as-deposited and the last part of 3 samples annealed at 380°C, 420°C and 450°C in the presence of CF. The morphology of these films shows a similar trend as in the previously CC treated films. The films annealed at 420°C show a molten-like morphology which is in agreement with the structural transition in this temperature region. The grain sizes in these films were in the range (400-1000) nm. Films annealed at 450°C, show drastic reduction in grain boundaries with increase in grain size due to coalescence of many grain clusters forming grain size in the range (1000-4500) nm. The variation in the grain sizes for films annealed in the presence of CF could be due to the inclusion of F in the treatment. The grain size obtained in this experiment is reasonably comparable with high temperature growth techniques such as the CSS.

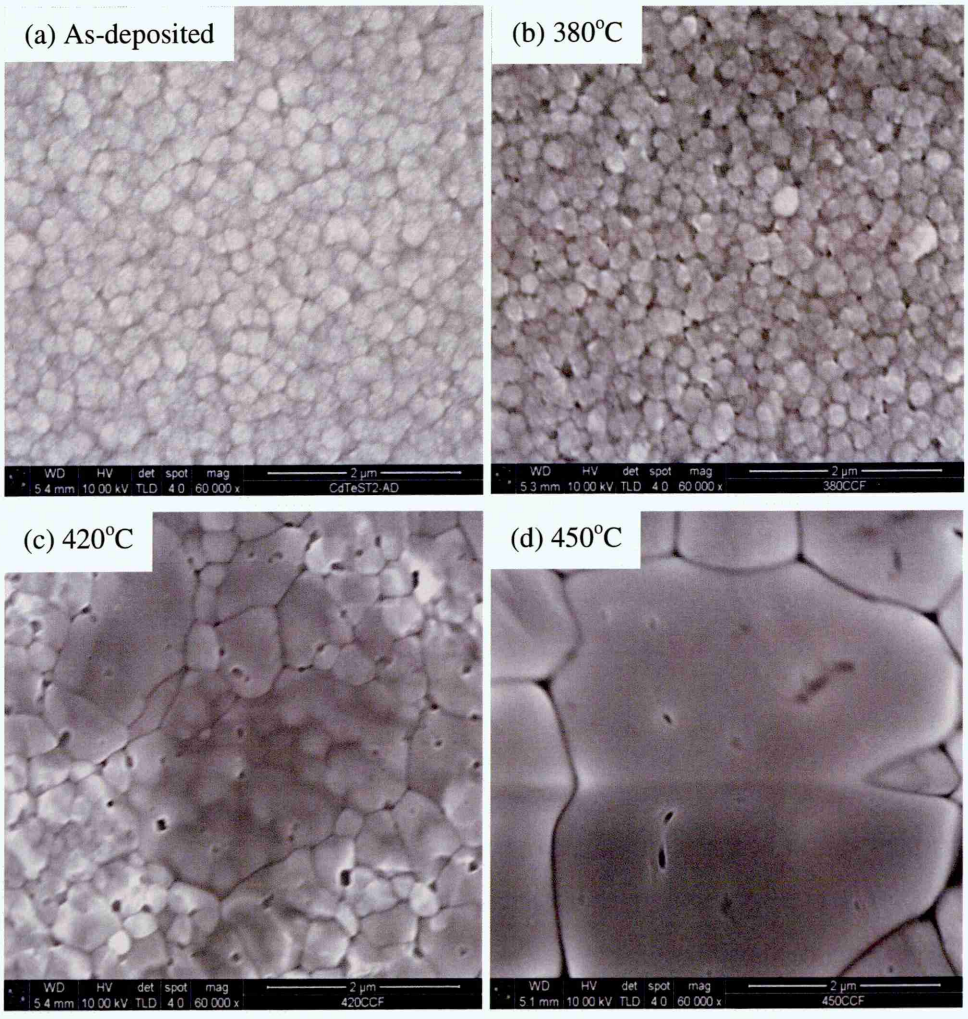

Figure 7-12: As-deposited and CdTe thin films annealed at different temperatures in the presence of CF for 20 minutes in air.

There are reports on the enhancement of device performance when F is included in the usual CC treatment of CdS/CdTe solar cells. This treatment could be in the form of solution [22,30–32] or gaseous phase [33–35]. In an experiment using the alternative low-cost ultrafast intense pulsed light (IPL) heat treatment of CC treated CdTe carried out by Dharmadasa *et al.* [12,13] have all reported similar observations suggesting the transition and the randomised texture of the CdTe at region 2 is due to melting of the grain boundaries influenced by the incorporation of the Cl impurities during annealing process.

The SEM images of both 3E and 2E systems discussed show similar trends of the increase in the grain size with increase in annealing temperature. Therefore, CdTe grown from both systems show similar structural and electrical properties appropriate for device fabrication. However, it can be observed that the grain sizes are larger in the 2E system; this is attributed to the difference in the thickness of the two layers due to difference in the deposition current density which is higher in the 2E system due to relatively higher growth temperature.

7.3.2.7 Atomic Force Microscopy

This experiment was carried out to study the effects of CC and CF on the surface roughness of the CdTe films. Figure 7.13 shows surface topography of two dimensional (2D) and three dimensional (3D) AFM images of glass/FTO/CdTe structure for (a) as-deposited (AD) and (b), (c) & (d) are for samples annealed in the presence of CC at different temperatures for 20 minutes in air.

This is a complementary technique to SEM in the study of material surfaces. But AFM studies provide surface topographies which give information on the surface roughness of materials. The variation in the brightness of sites on the layer surface indicates non-uniformity of the deposited layer. Bright sites indicate peaks while dark sites indicate valleys in the samples. The AD film shows a uniform coverage due to smaller grain size nature similar to the AD SEM image shown in Figure 7.11(a). It shows that surface roughness increased with increase in annealing temperature as indicated by the 3D images. The approximate surface roughness obtained for AD, and samples annealed at 380, 420 and 450^{o}C are 14, 30, 36 and 49 nm respectively.

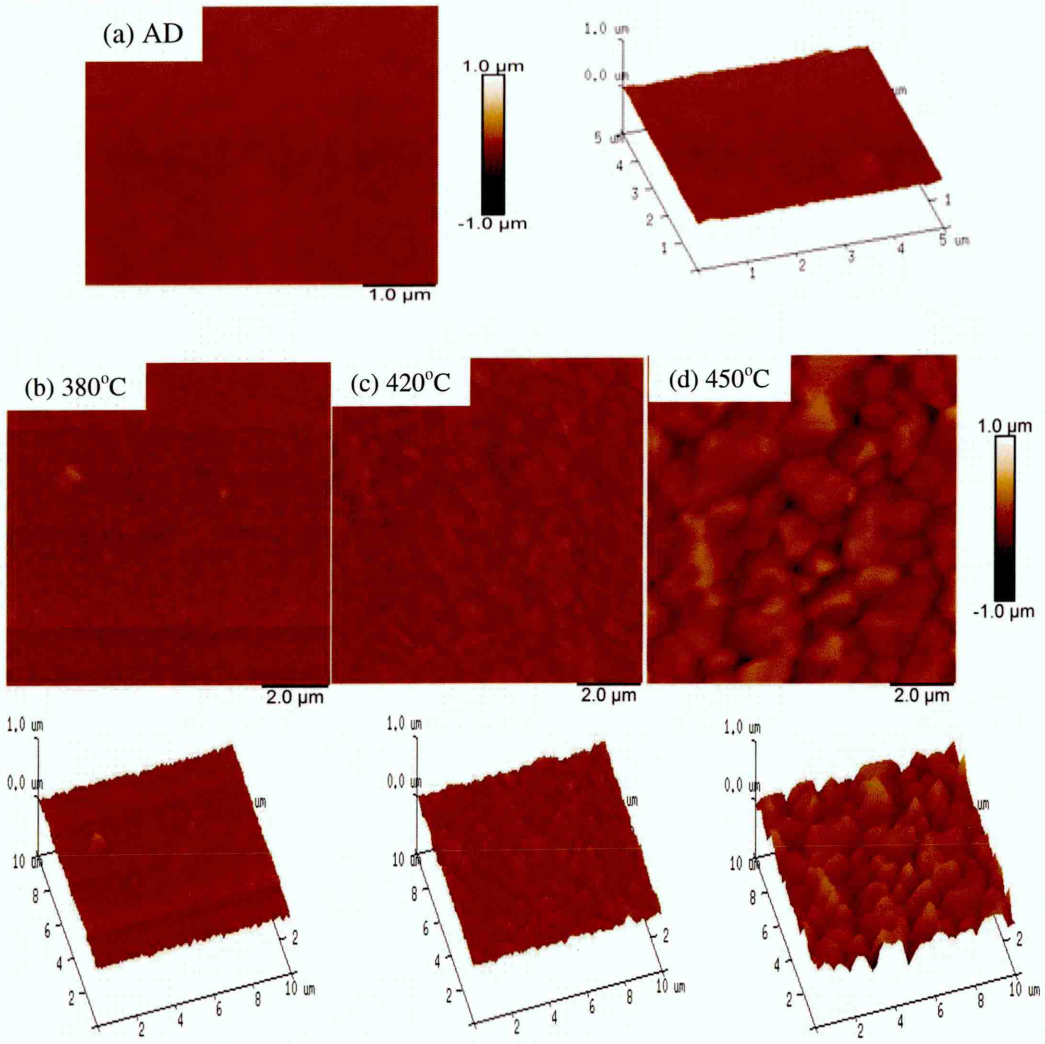

Figure 7-13: Typical AFM topographical images of 2D and corresponding 3D images of CdTe thin films of as-deposited and films annealed with CC at different temperatures.

Figure 7.14 (a-c) shows the AFM topographies of layers treated in the presence of CF at different temperatures. As with the case of sample treated in the presence of CC, samples treated in CF also showed increase in surface roughness with increase in grain size. The approximate surface roughness of these films was approximately found to be 21, 26 and 80 nm for samples annealed at temperatures of 380, 420 and 450°C respectively. The summary of the AFM surface roughness obtained for layers treated in CC and CF is given in Table 7.3.

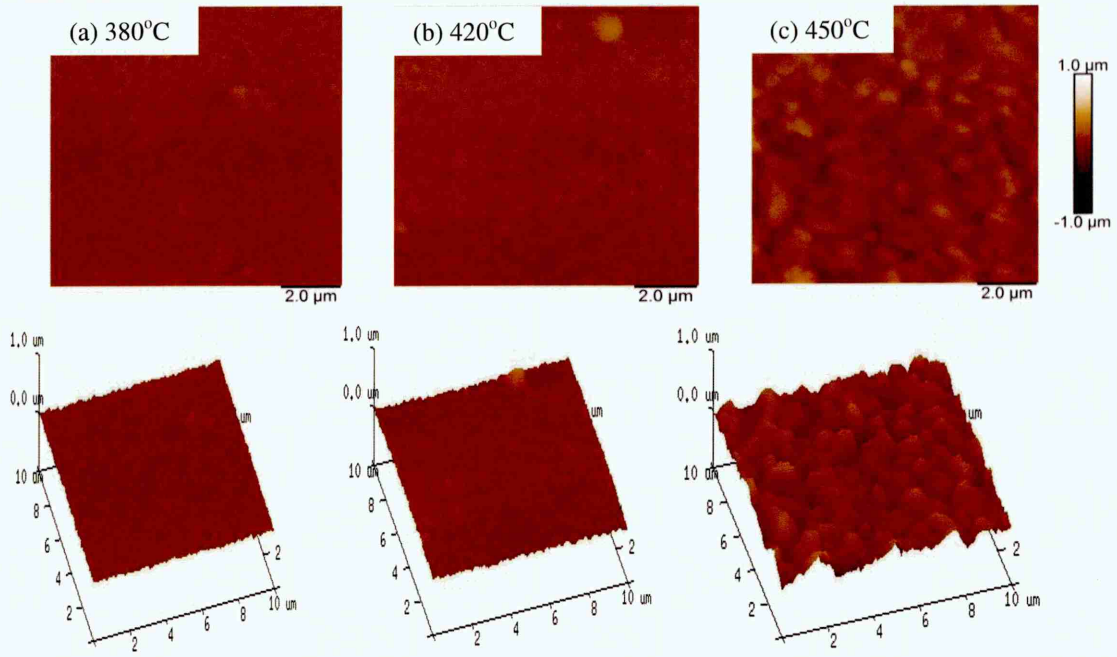

Figure 7-14: Typical AFM topographical images of 2D and corresponding 3D surfaces of CdTe thin films annealed with CF at different temperatures.

Surface roughness is detrimental in the fabrication of thin film solar cell devices because it can short circuit the device due to either layer non-uniformity or when the deposited layer thickness is lower than the surface roughness of the substrate. Larger grain sizes are important for solar cells but may also be detrimental especially when they open up pinholes or gaps in between grains.

Table 7-3: Summary of CdTe thin films roughness for AD, CC and CF layers annealed at different temperatures.

Annealing condition	R_{sm} (nm)	Annealing condition	R_{sm} (nm)
AD	14	AD	14
CC+380°C	30	CF+380°C	21
CC+420°C	36	CF+420°C	26
CC+450°C	49	CF+450°C	80

Since CdTe preferentially grow as columns, this may easily influence the formation of shunting paths perpendicular to the substrate that lowers the shunt resistance values [14]. However, this device can produce excellent result if the metal contact is made on continuous CdTe columnar grains from top to bottom of the device. This will lead to

high mobility values since these columns have less grain boundaries and defects passivated by the Cl or F fluxing agent. The effect of roughness can be cushion using reasonably thick layers while pinholes can be solved by incorporating a pinhole plugging layers such as Polyaniline (PAni) [19] or Zinc telluride (ZnTe) [22]. To minimised error in the value of the roughness of each sample, measurements were carried out at three different places and the average is taken as the roughness of the sample.

7.3.2.8 Effect of growth time on the CdTe layer thickness

Figure 7.15 shows the plots of thickness as a function of growth time for (a) 3E and (b) 2E systems. The knowledge of film thickness for application in electronic devices especially solar cells is necessary so that right film thickness is utilised for optimum performance. The theoretical thicknesses were calculated based on Faraday's law of electrolysis given in equation 7.4.

$$T = \frac{JtM}{n\rho F} \qquad 7.4$$

Where T is the thickness of the layer, J is the average current density in $mAcm^{-2}$, t is the growth time in seconds, M is the molar mass of CdTe, n is the number of electrons involved in the formation of one mole of CdTe (n=6), ρ is the density of CdTe and F is the Faraday's constant. The estimated thickness is based on the assumption that the whole electronic charges released during deposition were fully involved in the thin films deposition process.

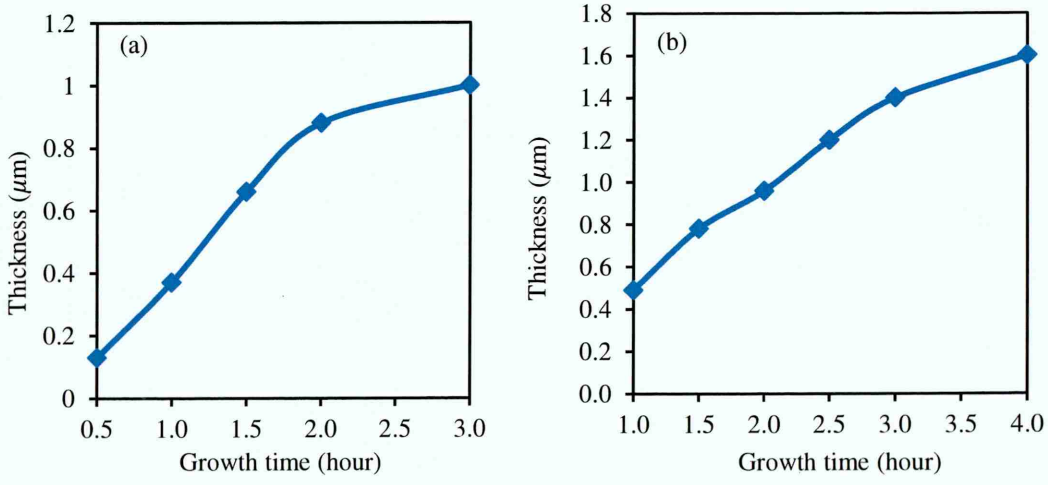

Figure 7-15: Plots of theoretical thickness estimations for CdTe films grown using (a) 3E and (b) 2E systems.

The average layer thickness required for CdTe absorber for the fabrication of solar cell device is ~1500 nm. Since an approximate CdTe layer thickness of ~2000 nm is enough to absorb nearly 100% of the incident photons with energy, E≥ Eg. Previous experimental results have established that CdTe layer thickness in the range (1500-2000) nm can be deposited in ~4 hours when the deposition current density is between (150-180) μAcm^{-2} for the 2E system. But the deposition current density in the 3E system is usually in the region of (90-120) μAcm^{-2} which requires about 5 hours growth to achieve CdTe layer thickness of (1500-2000) nm. However, the layer thickness is directly related to the deposition current density which in turn depends on parameters such as $HTeO_2^+$ concentration in the deposition bath, deposition temperature, pH and the stirring rate [14]. Based on the results plotted in Figure 7.15, the 3E system requires about one hour to grow a layer thickness of ~400 nm whereas it takes the same time to grow a layer thickness of about 500 nm in the case of the 2E system. The error in thickness calculation using Faraday's equation is about ±1 nm while the error for thickness measurements using optical depth profilometer is ±50 nm. The thickness of each sample is an average of three readings taken at different areas.

7.3.2.9 Photoelectrochemical cell measurements

Photoelectrochemical (PEC) cell measurements were carried out to confirm the electrical conductivity type of the CdTe thin films. Many samples were grown at different growth voltages using 2E and 3E systems. For the 3E system, the samples were grown at voltages between (820-836) mV while for the 2E system, the growth voltages were in the range (1940-2010) mV as shown in Figure 7.16.

Figure 7.16(a) and 7.16(b) show the PEC signals observed for as-deposited and CC treated CdTe layers grown from 3E and 2E systems. The CdTe layers grown at low cathodic voltages are Te-rich and p-type in electrical conduction, while at higher cathodic voltages; the layers are Cd-rich and n-type in electrical conduction. In between these two regions, there exists an inversion voltage (V_i) which produces near stoichiometric material with highest crystallinity and suitable electronic properties for solar cell fabrication. The inversion voltage (V_i) for CdTe films grown using 3E and 2E are ~828 and ~1965 mV respectively.

Materials grown at this point are near stoichiometric with intrinsic semiconducting properties and the Fermi level should be right in the mid-gap. In both systems moving

to higher voltages from the V_i increases n-type doping while moving to lower voltages increases the p-type doping as can be observed in Figure 7.16(a) and 7.16(b). Materials grown at voltages higher than the V_i are Cd-rich and the possible defects at this region are Te-vacancies (V_{Te}), Cd in Te sites (Cd_{Te}) and Cd interstitials (Cd_i). Whereas the films grown at voltages lower than the V_i are Te-rich with possible defects of Cd-vacancies (V_{Cd}), Te in Cd sites (Te_{Cd}) and Te interstitials (Te_i). The value of V_i may shift, depending on the factors such as Te concentration, stirring rate, growth temperature and pH value.

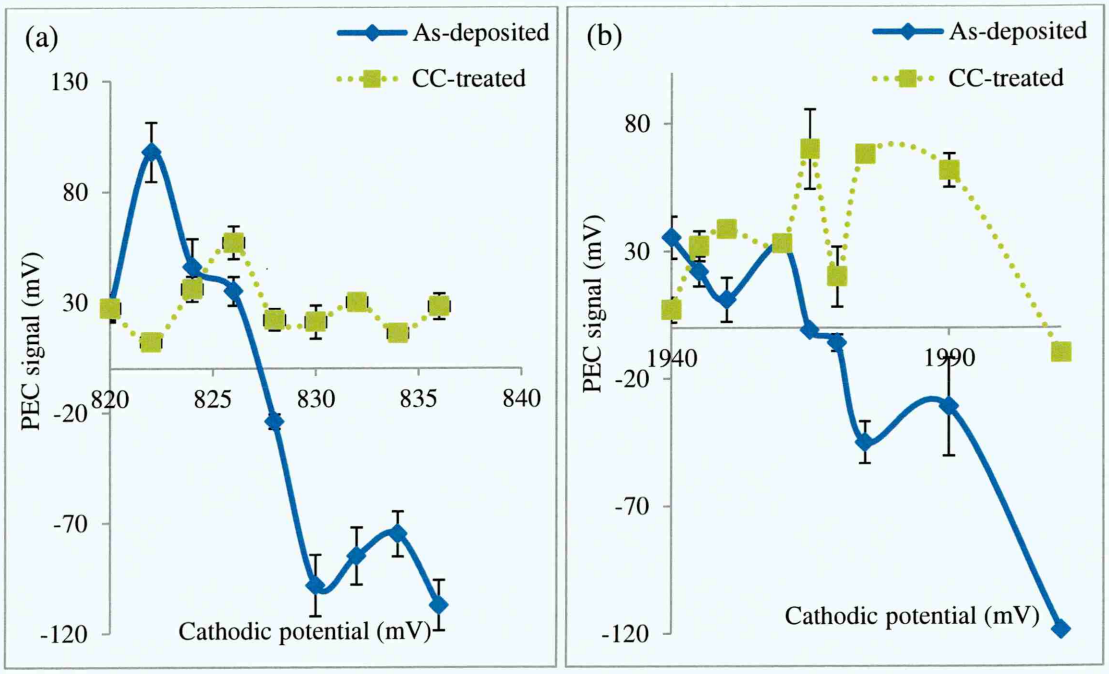

Figure 7-16: PEC signal as a function of growth voltage for as-deposited and $CdCl_2$-treated CdTe thin films grown using (a) 3E and (b) 2E systems at different cathodic voltages. Samples were annealed in the presence of $CdCl_2$ at 400°C for 15 minutes in air.

After CC treatment, both materials show similar behaviour such that p-type materials move towards n and n-type materials move towards p-type conduction. It should be noted that this is due to Fermi level (FL) movement within the CdTe bandgap. There is a possibility for a material to move from p-type to n-type [36,37] and from n-type to p-type [38,39] after annealing. This shows the direction of movement of the FL in the bandgap depending on the initial condition of the layer, doping effects and heat-treatment conditions.

7.3.2.10 Raman spectroscopy

Raman spectroscopy (RS) is a convenient, non-destructive, non-contact and surface sensitive technique used to determine the crystallinity, phases and finger prints of materials based on inelastic scattering of monochromatic wavelength of radiation. The spectra were obtained using argon ion laser (λ= 514 nm). RS rely on the low-frequency phonon mode due to rotational and vibrational modes of the molecules.

Figure 7.17 shows a typical Raman spectra for CdTe layers grown using 3E (Figure 7.17(a,c)) and 2E (Figure 7.17(b,d)) systems. In the as-deposited film grown using 3E (Figure 7.17(a)), a prominent peak at 121 cm^{-1} represents elemental Te while the peak at 140 cm^{-1} is related to both transverse optical CdTe and elemental Te, TO(CdTe)+(E)Te. Raman studies carried out on CdTe layers by Abdul-Manaf et al [25] and Diso [40] have also observed peaks due to both elemental Te and CdTe.

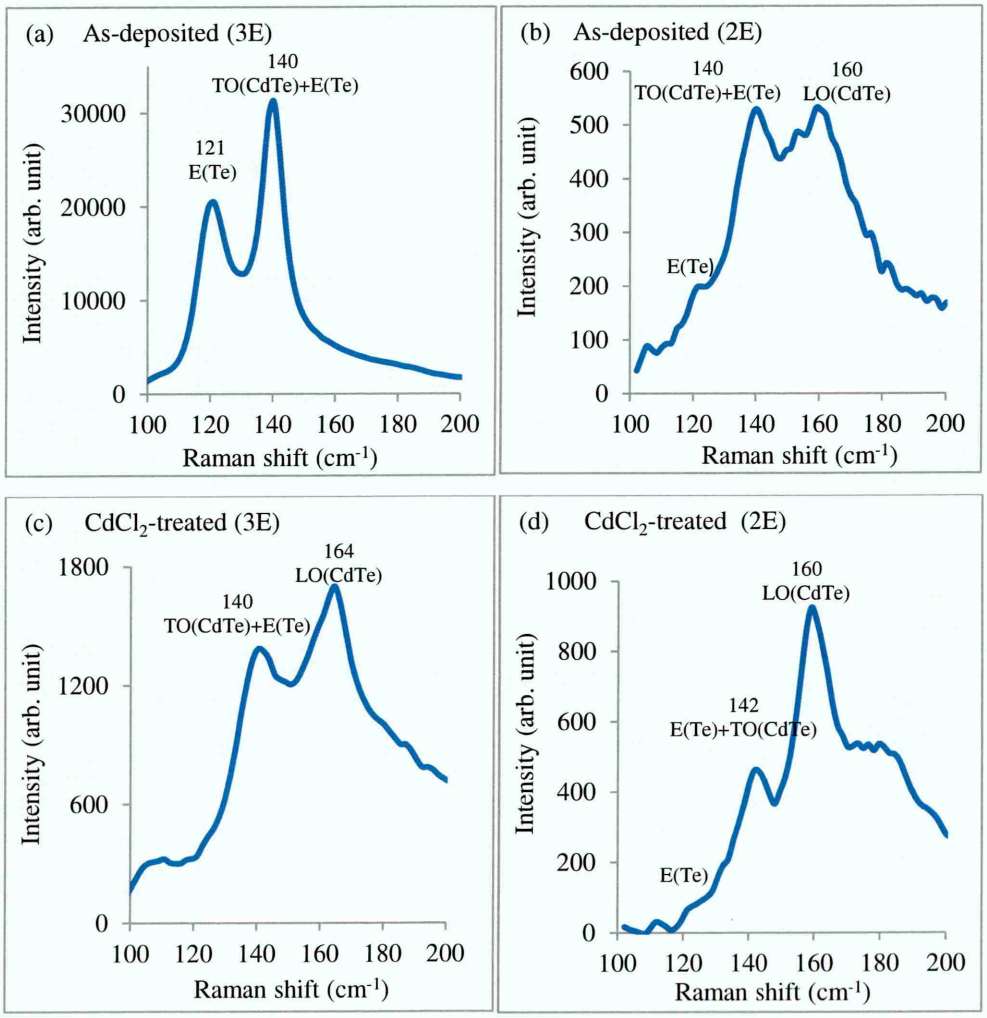

Figure 7-17: Typical Raman spectra for as-deposited (a) & (b) grown from 3E and 2E system respectively. And (c) & (d) are 3E and 2E samples after heat-treatment at 400°C for 10 minutes in air in the presence of CC.

After heat-treatment in the presence of CC (Figure 7.17(c)), a dramatic change in the structure of this material is observed. The elemental Te peak at 121 cm^{-1} disappears completely and a drastic reduction in the peak intensity of the TO(CdTe)+E(Te) is noticed. It is also interesting to see the appearance of a new peak at 164 cm^{-1} corresponding to longitudinal optical CdTe, LO(CdTe) which was completely missing in the as-deposited film. The structural enhancement is due to recrystallisation and grain growth during the CC treatment. Another reason for this could be due to the reaction of the Cd used in the CC treatment with excess Te to form CdTe [11] thereby enhancing both the structural and electrical properties of the material.

Figure 7.17(b) and (d) show Raman spectra of CdTe of as-deposited and annealed with CC grown using 2E system. In the as-deposited spectrum (Figure 7.17(b)), a weak peak is observed at 121 cm^{-1} which is due to elemental Te while a peak at 140 cm^{-1} is related to TO(CdTe)+E(Te). Another peak at 160 is associated with LO(CdTe) which shows appreciable increase after the CC treatment. In both systems, the effects of the CC treatment on both structures and composition are obvious in improving both the structural and electronic properties of the layers. The features of materials grown from both systems are same but may have different peak intensities which could be due to the initial condition of the layers. All Te related peaks are either completely eliminated or drastically reduced in both 3E and 2E systems. After the CC treatment, irrespective of the growth system, the LO(CdTe) peak at 160 cm^{-1} remained the dominant peak. This further affirms the comparability of the two growth system in producing device grade material after CC treatment.

7.3.2.11 Optical absorption studies

Optical absorption studies were carried out to estimate the optical energy band gap (E_g) of the materials. Figure 7.18 shows the plot of absorption coefficient (α) versus photon energy (eV) from which the bandgaps were estimated by extrapolating the straight line portion of absorption coefficient edge to the photon energy (hv) axis (α=0) [41]. Figure 7.18 shows the plots obtained for α vs hv of electroplated CdTe layers grown using 3E (a,b) and 2E (c,d) systems. These selected samples were grown at different potentials during optimisation of growth voltage.

In this experiment, as-deposited CdTe layers grown at different potentials using 3E and 2E systems were cut into two pieces. The first set of the samples each for 3E and 2E was left as-deposited and the other set annealed in the presence of CC at 400°C for 15

minutes in air. This is to check the effects of the CC treatment on the initial material properties and how it affects the bandgap of these layers.

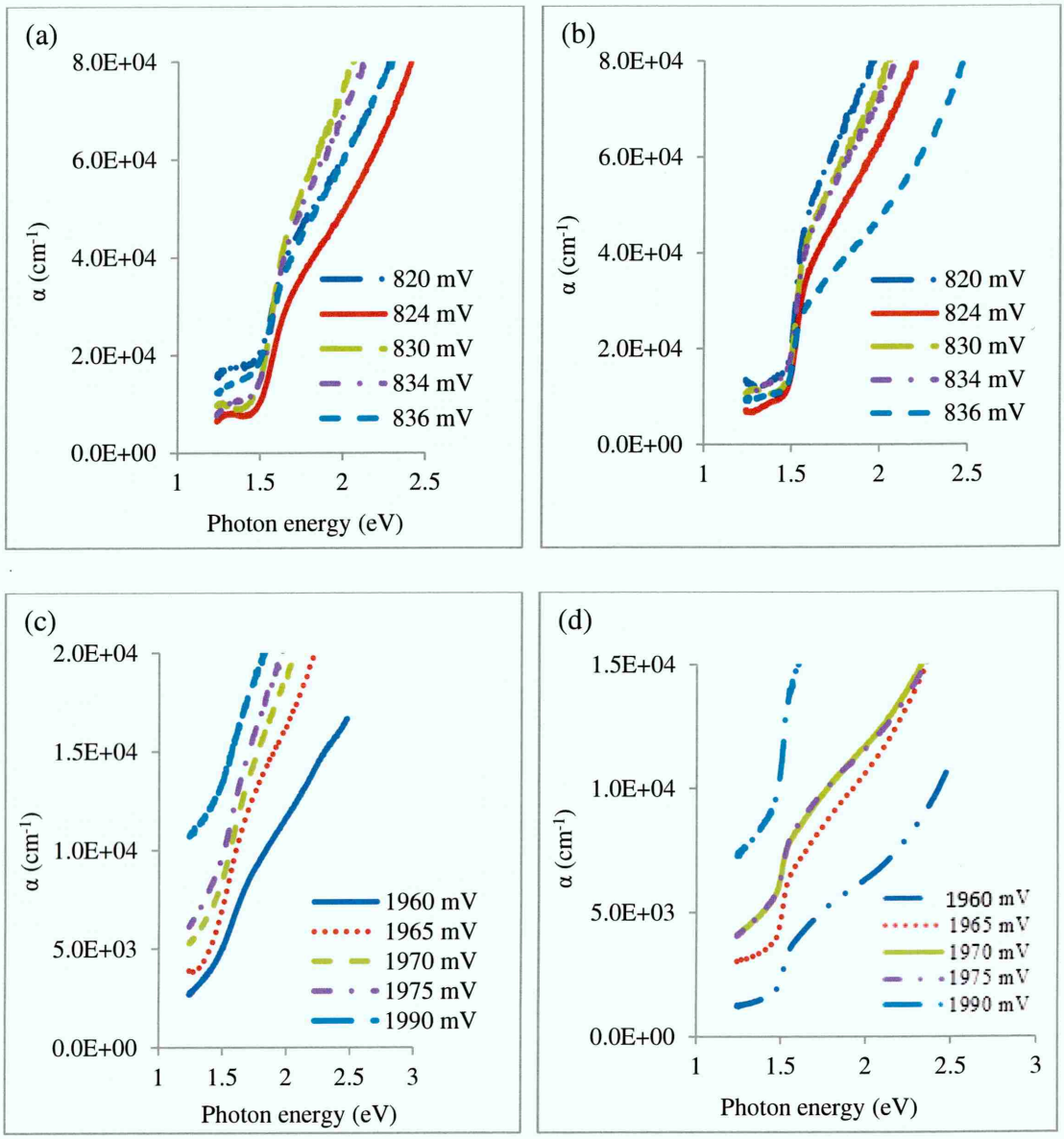

Figure 7-18: Absorption coefficient for as-deposited and $CdCl_2$-treated CdTe layers grown using 3E (a,b) and 2E (c,d) systems at different growth potentials. The films were CC-treated at 400°C for 15 minutes in air.

As-deposited CdTe layers grown using 3E show estimated bandgaps in the range (1.44-1.45) eV. While after CC treatment, the bandgaps were in the range (1.40-1.45) eV for near stoichiometric CdTe layers grown using both 3E and 2E systems. The slight improvement towards the bulk bandgap of CdTe (1.45 eV) could be due to recrystallisation and grain growth in these layers due to the CC treatment. Another important process could be the reaction between the excess Cd from the CC treatment with Te to form more CdTe compound thereby improving the material stoichiometry.

As-deposited CdTe samples grown using 2E system show a bandgaps in the range (1.40-1.45) eV while after CC treatment, the bandgaps were found in the range (1.40-1.45) eV. The obtained bandgaps are very close to the bulk bandgap of CdTe (1.45 eV). The Presence of multiphase in a layer tends to produce smaller crystallites thereby producing slightly larger E_g values. Incorporation of more metallic Cd in the layer will contribute to the reduction of the bandgap. Another reason could be due to the difference in the surface to volume ratio in the as-deposited and the CC treated layers. The surface to volume ratio is higher in the as-deposited and lower in the CC samples due to grain growth property for CC treated layers. Materials grown from both systems show similar bandgaps and are therefore comparable in their optical bandgap estimation.

7.3.3 Effect of growth temperature on the optical bandgap of CdTe thin films grown using 2E system

This experiment was performed by growing four CdTe layers at different temperatures of 25, 45, 65 and 80°C on Te-rich side close to the V_i. The optical absorption measurements were performed on these layers to study the effects of growth temperature on the optical bandgap behaviour of the CdTe thin films. Figures 7.19(a) and (b) show the plot of absorption coefficient (α) vs. photon energy (eV) to estimate the bandgaps for both the AD and CC annealed films. All the layers were annealed at 400°C for 15 minutes in air. The estimated bandgap for the AD films were in the range (1.15-1.35) eV while after annealing in the presence of CC, the bandgaps were in the range (1.35-1.45) eV. It is interesting to observe the gradual increase in the sharpness of the absorption edge with an increase in deposition temperature. The bandgaps obtained for the CC annealed films are close to 1.45 eV for all samples which matches well with the bulk bandgap of CdTe (E_g=1.45 eV). And the sharpest absorption edge occurred at 80°C similar to the AD films. The obtained bandgaps agree with reported bandgaps of CdTe in the literature [42]. This further confirmed the imperativeness of annealing the CdTe thin films with CC to improve their optoelectronic properties suitable for device fabrication.

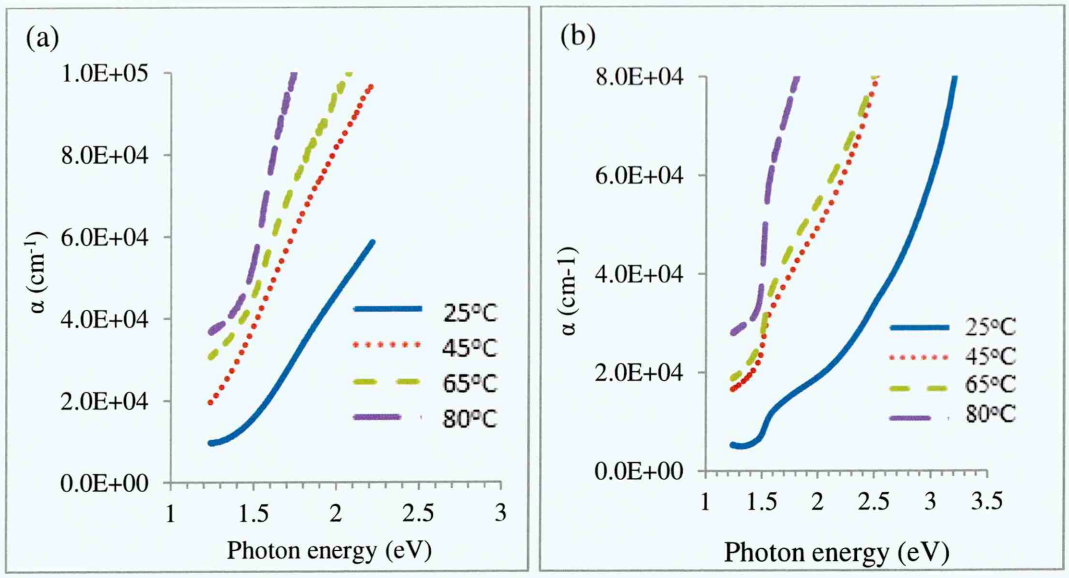

Figure 7-19: Optical absorption spectra of CdTe thin films (a) AD and (b) CC annealed at 400°C for15 minutes in air.

Table 7-4: Summary of the bandgaps of CdTe films grown at different temperatures for AD and CC annealed.

Growth temp. (degree)	Bandgap (eV) ±(0.02)	
	AD	CC
25	1.30	1.40
45	1.15	1.40
65	1.15	1.40
80	1.35	1.45

7.3.4 Effect of annealing temperature on the optical properties of $CdCl_2$ and $CdCl_2$+CdF_2 treated CdTe layers.

Figure 7.20(a) and 7.20(b) show the plot of absorbance as a function of photon wavelength (A vs. λ) for CdTe thin films heat treated at different temperatures in the presence of (a) CC only and (b) CF. Like in the previous case, the AD layer was included for comparison and easy reference. The AD film shows the lowest absorbance but is seen to increase with increase heat treatment temperature. The layers heat treated at 380 and 420°C in the presence of both CC and CF show comparable absorbance.

After annealing at 450°C in both conditions, a drastic increase in absorbance is noticed and attributed to increased grain growth, recrystallisation and annealing out defects.

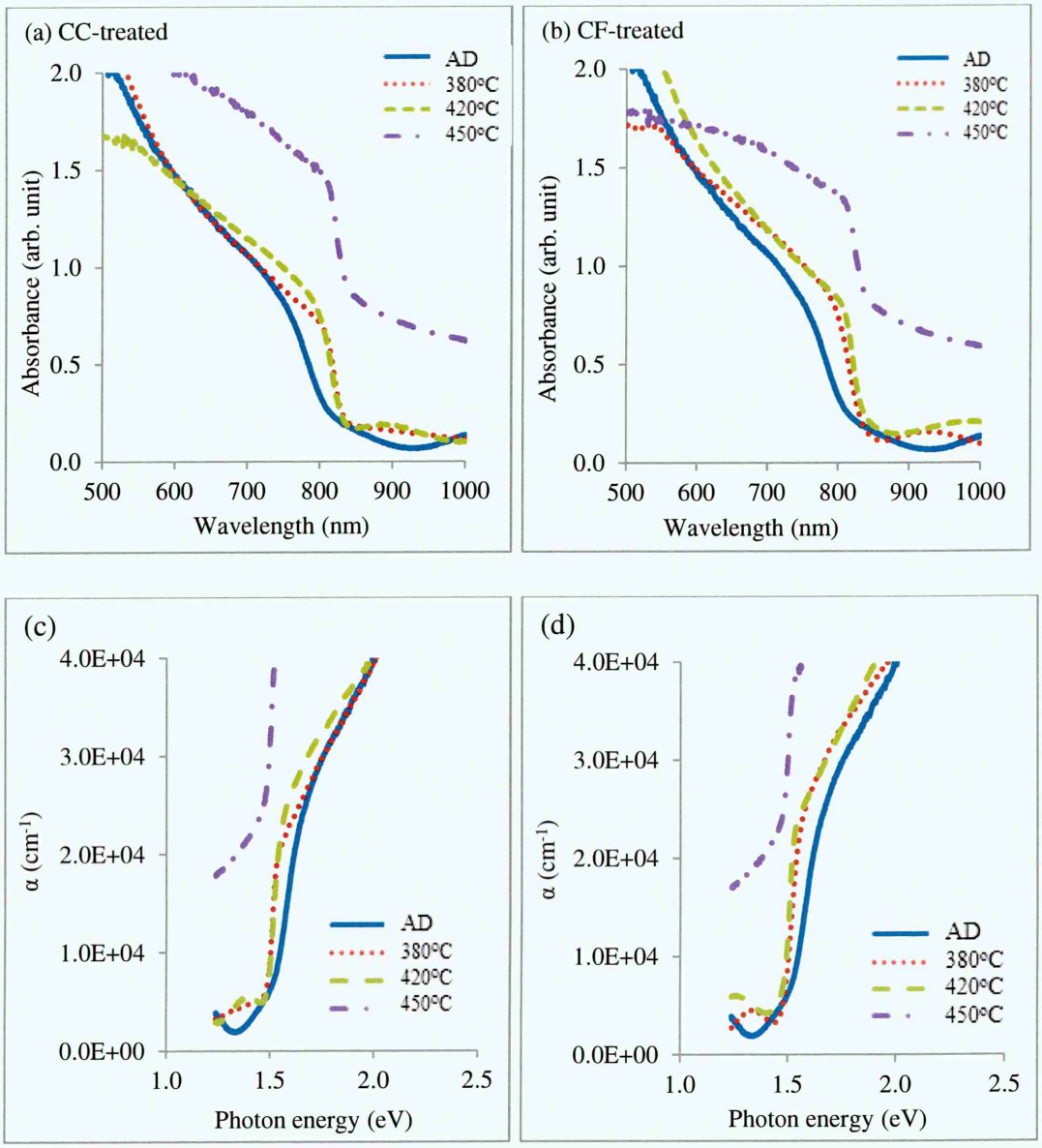

Figure 7-20: Optical absorption spectra (A vs λ) for (a) CC and (b) CF while (c) & (d) are their respective α vs hν. All heat treatments were carried out for 20 minutes in air.

This experiment was conducted using a CdTe layer of ~800 nm thick grown on glass/FTO substrate. After growth, the as-deposited layer was divided into seven parts. The first part was left as-deposited (AD) and the next three parts were heat treated at three different temperatures of 380, 420 and 450°C in the presence of $CdCl_2$ (CC) only. The last three parts were also heat treated at 380, 420 and 450°C in the presence of $CdCl_2$+CdF_2 (CF). All heat treatments were done for 20 minutes in air. Figures 7.20(a) and 7.20(b) show the optical absorbance spectra for two cases. Figure 7.20(c) and

7.20(d) show the corresponding plots of absorption coefficient (α) as a function of photon energy (hν) (α vs. hν) for CdTe thin films heat treated at different temperatures in the presence of (c) CC only and (d) CF. In each case the spectra of the AD sample is included for easy comparison. The result show that the absorption edges of these films continue to be sharper as the heat treatment temperature increases relative to the AD sample.

The estimated bandgap value of the AD sample is 1.55 eV. The samples heat treated at 380°C and 420°C in both CC and CF show the same bandgap value of 1.48 eV. While samples annealed at 450°C in the presence of CC and CF show bandgaps of 1.44 eV and 1.42 eV respectively. A significant improvement in the absorption edges of these films becoming sharper when compared with the AD films. An improvement is observed in CdTe layers heat treated at 450°C in both CC and CF.

Irrespective of the heat treatment condition, the absorption edges of the films increasingly become sharper from the reference AD to films annealed at 450°C with decreased bandgap to lower photon energy as heat treatment temperature increases. The improvement in the absorption edges and decrease in the bandgap indicate increased grain growth and recrystallisation thereby reducing the surface to volume ratio in these films [43] making layers more dense, compact and increased light absorption. The cumulative result of this is the increase in photo-generated charge carriers in the CdTe layers since more photons are absorbed. The films annealed at 450°C under both conditions show similar bandgap energy values to bulk bandgap of CdTe (1.45 eV).

7.4 DC electrical conductivity measurements

In this experiment, as-deposited CdTe thin film sample with a thickness of ~700 nm grown on glass/FTO substrate was cut into 10 pieces, five each for making ohmic and Schottky contacts. The prior knowledge of the conductivity type of these materials is crucial and basic step toward fabrication of any electronic device structure especially in solar cell development. The p-type electrical conductivity of the layers both in as-deposited and samples annealed with different surface treatments were confirmed by PEC cell measurements system. The five samples in each case include as-deposited (AD), annealed in air only (HT) and layers treated with cadmium chloride (CC), cadmium chloride + cadmium fluoride (CF) and cadmium chloride+gallium chloride (CG). After treatments, the layers were allowed to dry in fume hood laboratory atmosphere and then annealed at 400°C for 20 minutes in air and were allowed to cool

down slowly. Thereafter, the samples were cleaned with de-ionised water to remove the chemical residues and other contaminants incorporated during the heat treatments on the layers surfaces. The layers were dried and ready for back contacts metallisation.

For layers intended for conductivity measurements, ohmic contacts were made by evaporating circular Au contacts of 0.031 cm^2 on the p-CdTe surfaces at a vacuum pressure of 10^{-6} mbar. Fully automated I-V system with Keithley 2401 source meter was used to measure the current-voltage (I-V) relation under dark condition. The resistance of each sample was obtained by measuring several contacts on each sample from which the average resistance, the resistivity and conductivity of each layer was calculated using equations 3.6 and 3.7 in chapter 3. Table 7.5 shows the variation of resistivity with different chemical treatments and the data plotted using bar chart in Figure 7.21.

Table 7.5: Resistivity and conductivity values measured for CdTe thin films with different surface treatments of glass/FTO/CdTe/Au structures.

Sample condition	ρ (Ω.cm)$\times 10^4$	σ $(\Omega.cm)^{-1}$ $\times 10^{-5}$
AD	3.22	3.10
HT	2.54	3.93
CF	1.75	5.69
CC	1.54	6.48
CG	1.06	9.37

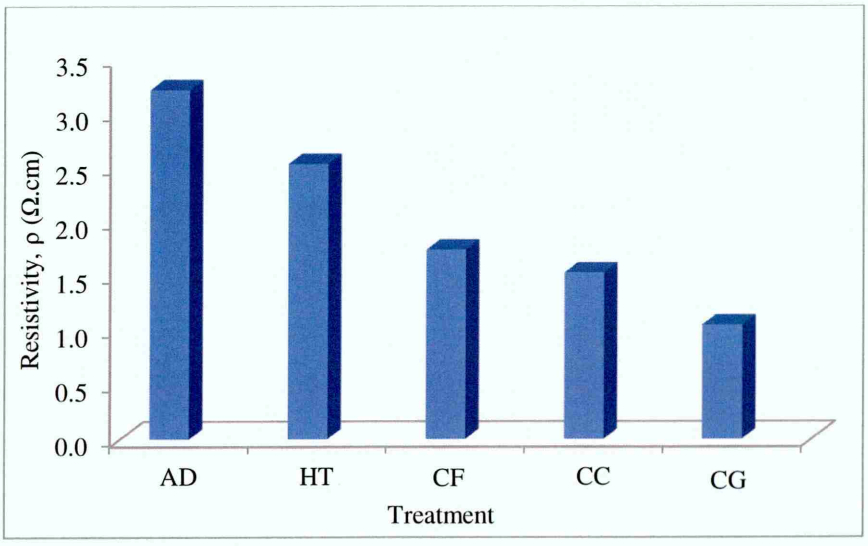

Figure 7-21: The variation of electrical resistivity as a function of CdTe layer annealing conditions.

The calculated resistivity values are 3.22×10^4, 2.54×10^4, 1.75×10^4, 1.54×10^4 and 1.06×10^4 Ω.cm for AD, HT, CF, CC and CG layers respectively. The obtained resistivities were in agreement with earlier reported values for ED-CdTe thin films [19,22]. The resistivity is highest in the AD and least in CG treated films and for a good solar cell devices, the resistance and capacitance values should be kept as low as possible [44]. The high resistivity recorded for the AD films is due to the high density of both grain boundaries and other defects in the films. After annealing in air with no surface treatment, the films show a decrease in the resistivity which is attributed to improvement in the electronic properties due to annealing out defects and the reduction in the density of grain boundaries which serves as scattering centres for electrons and improving carrier collection in the devices. The highest electrical conductivity is achieved when treated with CG, as seen from Table 7.5 and Figure 7.21.

Figure 7.22 shows the schematic cross-sectional diagram of layer equivalent of (a) AD and (b) CC or CF treated CdTe thin films to illustrate the nature of grain pattern in the as-deposited and heat-treated with chemical treatments. After heat treatment with chemicals crystallites of the size (20-60) nm merge into large crystals due to large surface to volume ratio. Then the small grain clusters in the range of (200-400) nm coalesce to form few microns size grains. This process passivates the grain boundaries improving carrier collections along the grain boundaries due to drastic reduction of boundaries and diffusion of chemicals into remaining grain boundaries. In this type of material (7.22(b)), the mobility values measured perpendicular ($\mu_\perp$) to the substrate give high values than the mobility measured parallel ($\mu_\parallel$) to the substrate since parallel measurement is highly obstructed due to high density of grain boundaries acting as scattering centres. This leads to low mobility values than the perpendicularly measured values due to less grain boundaries in the treated samples [19]. The columnar growth nature of CdTe perpendicular to the substrate also helps in this process when the resistivity is measured in perpendicular direction. Figure 7.22 can be visualised to the CdTe SEM images of AD and CC treated presented in section 7.3.2.6. Conventional Hall Effect measurements estimate $\mu_\parallel$ and these values are not applicable for solar cell devices. During PV action, charge carriers flow in perpendicular to the substrate, and therefore $\mu_\perp$ is applicable.

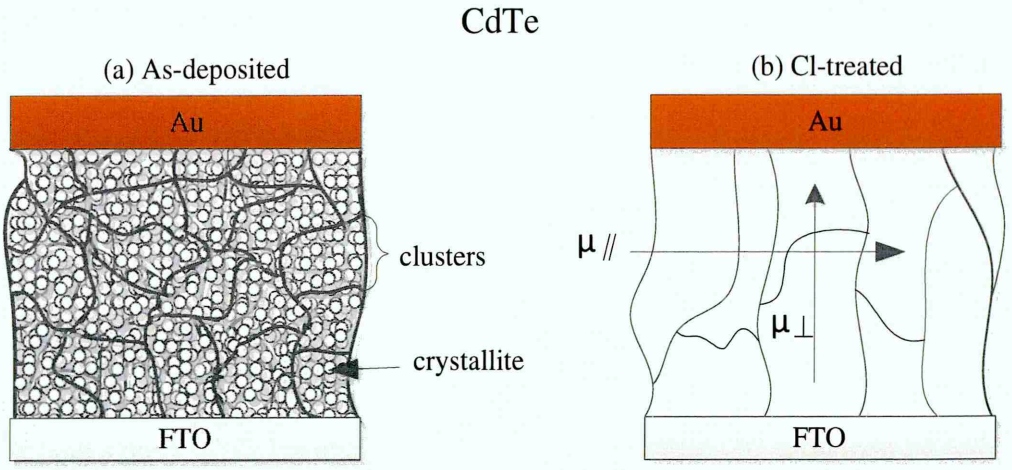

Figure 7-22: Schematic cross-sectional diagram of (a) as-deposited and (b) heat treated CdTe layers with $CdCl_2$, CdF_2 or $GaCl_3$ (Figures not to scale).

This experiment has shown the imperativeness of annealing CdTe thin films in the presence of chemicals rather than annealing without any treatment. This is further confirmed by the calculated charge carrier mobilities in these films (Table 7.5). It has also been shown that after the CC treatment, the grain boundaries participate in carrier collection rather than being recombination centres [11,45].

7.5 C-V measurements of Schottky contacts

Figure 7.23(a) and 7.23(b) show the capacitance Vs voltage (C versus V) and (b) the Mott-Schottky ($1/C^2$-V) plot of Schottky contacts made on as-deposited CdTe thin films. For the Schottky contact, Aluminium (Al) circular dots of area 0.031 m^2 were evaporated on the CdTe surfaces. The C-V characteristics of the cells were measured under dark condition using a frequency of 1 MHz at room temperature. Under these conditions, CdTe layers treated with different Cl containing salts were measured to check the effects of these treatments on the mobility and doping characteristics of these layers. The use of high frequency of 1 MHz was to avoid response from defects [46]. Measurements using lower frequency values could lead to defects response thereby introducing noise to the measured C-V spectra.

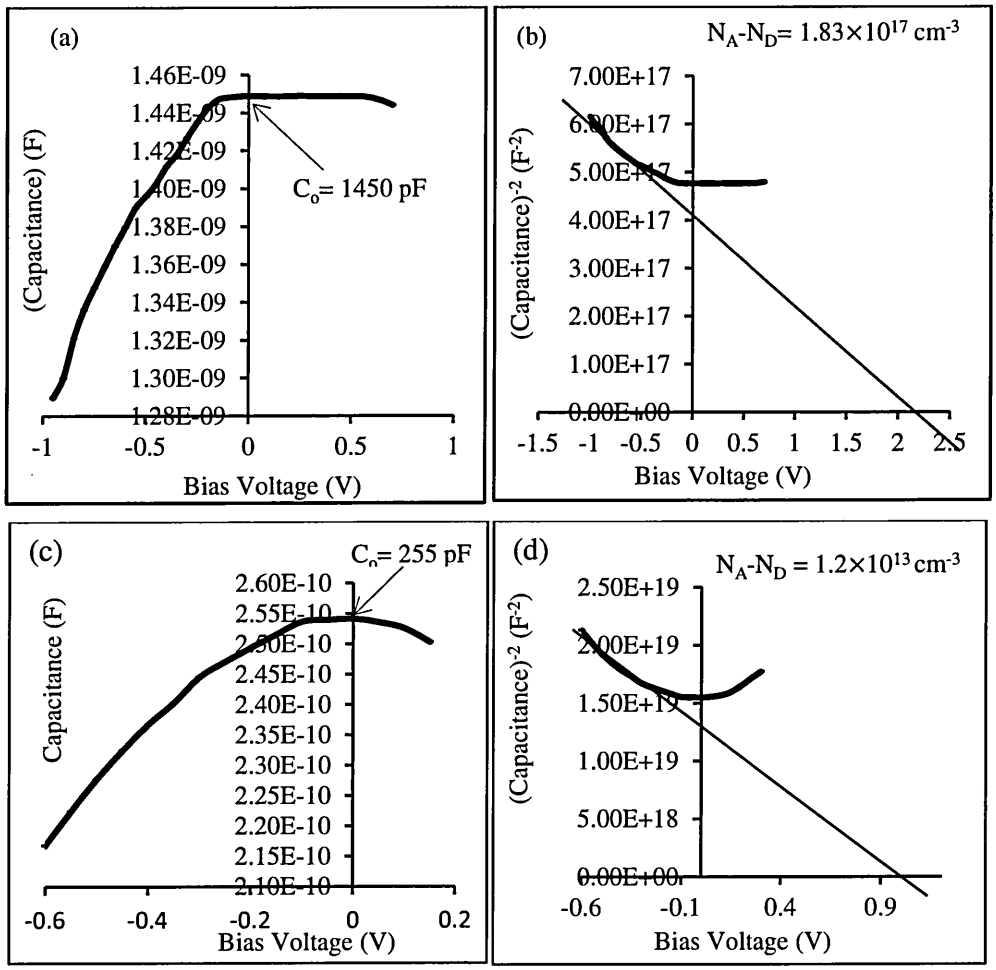

Figure 7-23: Typical plots of C-V (a,c) and $1/C^2$ vs V (b,d) of glass/FTO/p-CdTe/Al structures for as-deposited (a,b) and CG (c,d) CdTe thin films. Annealing was done at 400°C for 20 minutes in air with CG treatment.

C-V measurements were performed on all samples and relevant information extracted. However, only the C-V and $1/C^{-2}$ vs. V plots of two layers with the highest and lowest values of resistivity are presented for brevity. Figure 7.23 (c) and (d) show (a) C-V and $1/C^2$ vs. V plots for CG treated CdTe layers. All extracted parameters are summarised in Table 7.5. It is noticed that resistivity and depletion capacitance are higher in the AD layer and lowest in the CG treated layer while mobility values are higher in the CG layer. This difference has to do with effect of the chemical treatments discussed above. The mobility values were calculated using equation 7.5 from the conductivity and the doping concentration obtained from the DC conductivity and the CV measurements.

$$\mu = \sigma / qN \qquad 7.5$$

Where μ is the mobility, σ the conductivity, q is the electronic charge and N is the doping density.

The summary of the doping concentration and their respective mobilities ($\mu_\perp$) are given in Table 7.5 and the bar chart representation of the mobility ($\mu_\perp$) as a function of treatment for each layer is given in Figure 7.24. Most of the devices show doping concentration reasonably agreeing with reported doping concentrations producing efficiencies in excess of 10% for CdTe-based devices [47–50].

Table 7-5: Summary of the doping concentration and the mobility ($\boldsymbol{\mu_\perp}$) values extracted from the C vs V and $1/C^2$ vs V for glass/FTO/p-CdTe/Al structures heat treated with different chemical treatments.

Sample	ρ (Ω.cm)$\times10^4$	C_o (pF)	doping concentration, N_A-N_D (cm^{-3})	Mobility, μ ($cm^2V^{-1}s^{-1}$)
AD	3.22	1450	1.83×10^{17}	1.1×10^{-3}
HT	2.54	1190	4.05×10^{15}	6.1×10^{-2}
CF	1.75	740	3.20×10^{13}	10.9
CC	1.54	320	3.13×10^{12}	43.2
CG	1.06	250	1.20×10^{13}	49.3

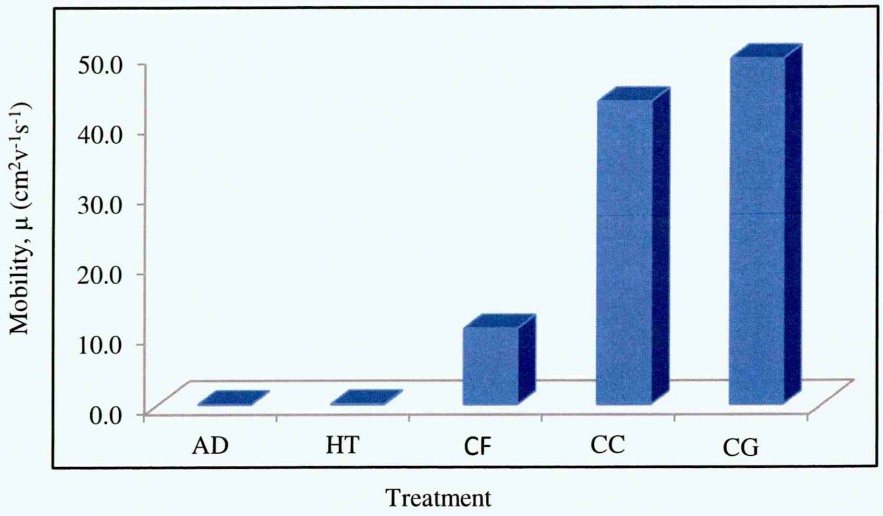

Figure 7-24: Variation of hole mobility ($\boldsymbol{\mu_\perp}$) as a function of annealing conditions of CdTe thin films. Heat treatment was carried out at 400°C for 20 minutes in air.

7.6 Ultraviolet photoelectron spectroscopy

Ultraviolet photoelectron spectroscopy (UPS) was used to study the positions of the valence band maximum (E_V) and the Fermi level (E_F) of CdTe layers. This experiment was carried out at the University of Louisville, USA by our research collaborators. To carry out this measurement, as-deposited (AD) CdTe layer with ~700 nm thickness was

grown on glass/FTO substrate using 3E system. The sample was cut into two pieces. One of the samples was left as-deposited and the other treated in the presence of CC at 400°C for 15 minutes in air. The layers were prepared for UPS by sputtering gold (Au) films on half of the CdTe layers. In this way, the Fermi level of the Au films and that of the CdTe film will align based on the metal-semiconductor contact theory. Therefore, the Fermi level of Au was taken as the Fermi level of the CdTe.

The spectrum of the Au film was taken to determine the low kinetic energy (KE) cut-off edge and the high KE Fermi level for gold. Similarly, a spectrum for CdTe film was also taken to determine both the low KE cut-off and high KE cut-off of valence band edge for CdTe. These parameters were used to calculate the Fermi level position within the bandgap of the CdTe thin films.

Table 7.6 shows the summary of UPS measured parameters for as-deposited CdTe thin films. The Au E_F (eV) and CdTe E_F (eV) are the high KE cut-off of the Au and CdTe films respectively. The position of the Fermi level within the bandgap of the AD CdTe films was calculated from the high energy KE cut-off values for Au and CdTe layers. To calculate the location of the Fermi level position in both as-deposited and CC annealed layers, the bandgap of CdTe was taken as 1.44 eV. The position of the Fermi level in the as-deposited CdTe film was found to be -0.56 eV above the conduction band minimum or 2.00 eV above the valence band maximum. This indicates that the as-deposited CdTe film is heavily doped, n^+-type in electrical conduction and a degenerate semiconductor.

Table 7-6: Summary of UPS measured parameters for the as-deposited CdTe thin films.

As-deposited	Au E_F cut-off (eV)	CdTe E_V cut-off (eV)		$E_F - E_V$ (eV)		$E_C - E_F$ (eV)	
	25.60	23.58	23.62	2.02	1.98	-0.58	-0.54
				2.00		-0.56	

Table 7.7 shows the summary of UPS measured parameters for the CC annealed CdTe films. This result shows that after the CC annealing process, the Fermi level positon has moved down to 0.07 eV below the conduction band minimum or 1.37 eV above the valence band maximum. This shows the decrease in the n-doping concentration of the layer after CC-treatment.

Table 7-7: Summary of measured UPS parameters for the CC-treated CdTe thin films.

	Au E_F cut-off (eV)	CdTe E_V cut-off (eV)		$E_F - E_V$ (eV)		$E_C - E_F$ (eV)	
CC-treated	25.05	23.65	23.71	1.40	1.34	0.04	0.10
				1.37		0.07	

The initial position of the Fermi level of the AD layer and after CC-treatment shows that the Fermi level is moving from n-type in the AD towards p-type after the CC-treatment. This trend is in agreement with the PEC results presented in Figure 7.16. The Fermi level positions for AD and CC CdTe films with respect to the conduction band are summarised in Table 7.8 and the schematic diagram depicting these positions and their movement within the CdTe bandgap are shown in Figure 7.25.

Table 7-8: Summary of measured Fermi level positions for AD and CC annealed layers.

AD	CC annealed
$E_C - E_F$ (eV)	$E_C - E_F$ (eV)
-0.56	0.07

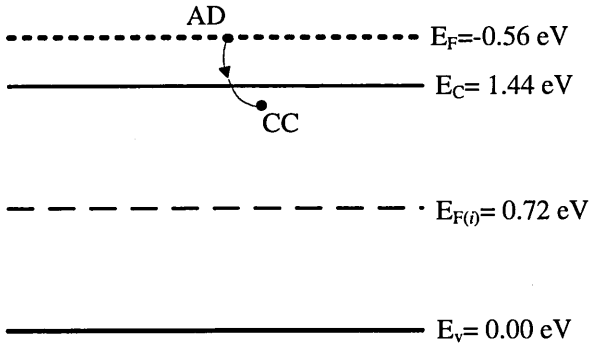

Figure 7-25: Fermi level position for AD and after CC treatment for the CdTe layer used for UPS measurements.

As observed in Figure 7.25, the Fermi level is seen to move from its initial position of -0.56 eV above the conduction band minimum in the AD to 0.07 eV below the conduction band minimum in the CC annealed film. Since the conductivity of the CdTe layers is established to be n-type in both AD and in CC annealed films, the electron

density can now be calculated from the respective Fermi level positions in these films using equation 7.6.

$$n = N_C \exp\left(\frac{-(E_C - E_F)}{KT}\right) \qquad 7.6$$

where;

n is the electron density in the conduction band (cm^{-3}), N_C is the effective density of states in the conduction band $\left(7.9\times10^{17} cm^{-3}\right)$, k is the Boltzmann constant $\left(1.36\times10^{-23} JK^{-1}\right)$

T is the room temperature (300 K)

The calculated values of electron concentration in the AD and the CC annealed CdTe films are presented in Table 7.9. The difference in the values of n for the AD (1.94×10^{27} cm^{-3}) and CC annealed films (5.29×10^{16} cm^{-3}) can be attributed to the CC annealing step which is well known in changing both the structural and electronic properties of semiconductor materials. The CC annealing step is known to either increase or decrease the electrons concentration depending on the processing conditions and the initial condition of the layer. Factors such as the annealing temperature, duration of annealing, the doping density of the films and the amount of the CC or CF can affect the final Fermi level position. Getting the right parameters that will take the Fermi level to settle in the upper half of the bandgap with doping density in the range (10^{14}-10^{15}) cm^{-3} is a task that involves a lot of inputs from material growth to post growth annealing processes [51].

Table 7-9: The calculated values of electron concentration with respect to the Fermi level position of the CdTe layers.

Fermi level position	E_C-E_F	$n\ (cm^{-3})$
AD	-0.56	1.940×10^{27}
CC-treated	0.07	5.295×10^{16}

The Fermi level position for the as-deposited material settled at -0.56 eV above the conduction band minimum corresponding to electron concentration (n) of 1.94×10^{27}

cm^{-3} and 0.07 eV below the conduction band minimum after CC-treatment corresponding to electron concentration (n) of 5.29×10^{16} cm^{-3}. This doping is considered moderate and will produce good performing devices [47,52].

7.7 Photoluminescence (PL) studies

This study was conducted to examine defects structure within the bandgap of ED-CdTe layers and their response to the $CdCl_2$ annealing treatment. Annealing the CdS/CdTe in the presence of Cl is proven to improve structural, electronic and overall device performance. In this experiment, as-deposited CdTe layer grown on glass/FTO substrate using 3E system was cut into two pieces one left as-deposited and the other annealed in the presence of CC at 400°C for 15 minutes in air. The chemical treatment was carried out by spreading a layer of saturated CC on the CdTe layer and allowed to dry in an open air atmosphere. Figure 7.26 Shows typical PL spectra obtained at 80 K for as-deposited and CC annealed CdTe thin films.

PL is based on the excitation of electrons from the valence band to the conduction band and subsequent transitions back to the valence band and defect levels. While on transit back to the valence band, PL peaks are observed at different defect levels within the bandgap of the material. The CdTe thin films were excited by 632 nm (1.96 eV) laser light thereby pumping electrons from the valence band to the conduction band. On their way back to the valence band, these electrons are captured by electron traps (defects) at different levels in the bandgap resulting to the emission of photons with different energies thereby creating PL peaks.

In this study, a wide energy range was chosen from 0.55-1.85 eV below the conduction band (CB) and both AD and CC annealed samples were scanned to check the defect modification after the Cl surface treatment on these materials. In agreement with a recent comprehensive study on the effects of CC treatment on deep levels in CdTe thin films using PL, Dharmadasa *et al.* [53] have reported four PL peaks within the bandgap of CdTe. In this work, similar four CdTe peaks were observed within the energy range of 0.55-1.85 eV and are summarised in Table 7.10.

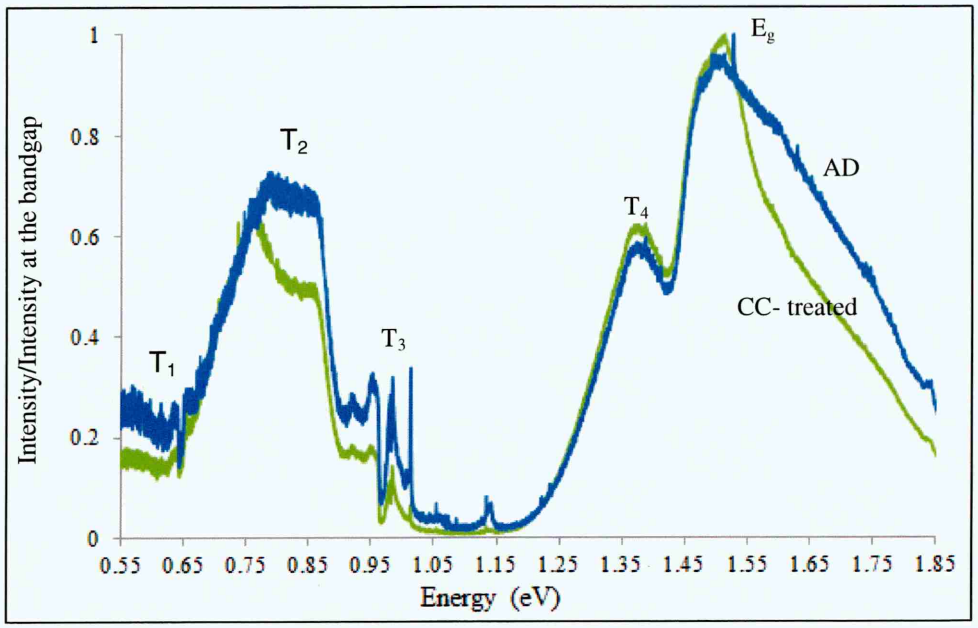

Figure 7-26: Photoluminescence spectra obtained at 80 K for as-deposited and CC-treated CdTe thin films grown from the 3E system. Annealing was carried out at 400°C for 15 minutes in air.

Table 7-10: Summary of electron traps at 80 K for CdTe layers electroplated using the 3E system with Pt anode and saturated calomel reference electrode.

Energy (eV)	T_1±0.02	T_2±0.15	T_3±0.03	T_4±0.08	E_g peak
CdTe-AD	0.66	0.75	0.97	1.37	1.50
CdTe-CC-treated	-	0.77	0.97	1.37	1.50

The electrons traps observed are T_1, T_2, T_3, and T_4 while the broad peak at 1.50 eV is inclusive of the bandgap energy (E_g) where band-to-band transition is observed. The defect levels T_1 and T_3 are narrower when compared with other defects at T_2 and T_4. The defect level at T_2 (0.75 eV) which fall in the middle of the bandgap show a wide range distribution of up to 0.30 eV and serve as recombination centres or otherwise known as "The killer centres". These killer centres are due to Te-richness [54,55] detrimental to device performance. The performance of solar cell will be significantly enhanced if the mid-gap defects are completely removed. Even after the CC annealing (see Figure 7.26), the defects at T_2 still remained with little reduction in its intensity. But the defects at T_1 were almost passivated while the one at T_3 was drastically reduced after the CC annealing treatment. The defect level at T_4 (1.37 eV) is broad and very close to the band

gap, E_g (1.50 eV) of this material. After the CC annealing, the width of defect T_4 is reduced. Observation has also shown that the intensity of this defect level (T_4) is increased which will support Fermi level pinning close to the valence band maximum thereby achieving large barrier height. The increased in the peak intensity and the reduction in the width of the defect level indicates the reduction in the defects in the bandgap of this material.

7.8 Conclusions

Thin films of CdTe have been successfully electroplated from an aqueous electrolyte on glass/FTO substrate from aqueous acidic electrolyte using 3E and 2E systems. In the 3E system, saturated calomel electrode (SCE) was used as the reference electrode. The working electrode (cathode) and the anode in both systems were glass/FTO substrate and platinum sheet respectively. The CdTe semiconductor was electroplated from aqueous electrolyte consisting Cd and Te ions. PEC results of the as-deposited in both systems indicate that both n-type and p-type electrical conduction types can be achieved by simply changing the deposition voltage.

Structural studies using XRD show that the CdTe films are polycrystalline in nature with a preferred orientation along the (111) cubic phase. The AD films show clusters consisting of small grains in the range (200-300) nm but after CC or CF treatments, the grains coalesced to form few microns size grains. It also shows that increase in grain size is dependent on the annealing temperature. Optical absorption studies show that, irrespective of growth voltage and growth system, the bandgaps shift toward the bulk bandgap of CdTe (1.45 eV) when heat-treated with CC or CF.

DC conductivity measurements for layers annealed in different surface treatment show a drastic reduction of resistivity after heat-treatment. This is due to enhanced carrier mobility as a result of increase in grain growth and annealing out defects. The resistivity is highest in the AD and lowest in the CG treated layer. Comparison of layers grown using both 3E and 2E systems show that the materials possessed similar properties in almost all the characterisations performed. However, fast deposition is normally obtained in 2E system which will reduce cost and time in manufacturing process.

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Chapter 8: CdTe-based solar cells: Fabrication and Characterisation

8.1 Introduction

This chapter deals with the fabrication processes, development and assessment of different solar cell structures based on CdTe absorber material. The solar cells were fabricated using thin films of In_xSe_y, ZnS, CdS and CdTe semiconductor materials. In_xSe_y and ZnS were incorporated into different device structures either as buffer or window layers while CdS and CdTe are respectively used as window and absorber layers. This research focuses on the development of n-CdS/n-CdTe solar cell based on a new model discussed in section 2.3.2 brought forward by Dharmadasa and reported in Dharmadasa *et al.*[1]. This model is based on the fabrication of CdTe-based solar cells using n-CdTe with the structure of n-CdS/n-CdTe plus large Schottky barrier at the back metal contact away from the conventional p-n junction structure of n-CdS/p-CdTe solar cells. This model was proposed after extensive work carried out by Dharmadasa on n-CdTe/metal interfaces [2–6].

The above mentioned semiconductor materials were combined to develop different solar cell structures. These structures include; glass/FTO/n-CdS/n-CdTe/Au, glass/FTO/n-In_xSe_y/n-CdTe/Au, and multi-layer graded bandgap devices [1] with structures, glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells. The devices were also activated using different chemical treatments such as cadmium chloride ($CdCl_2$ or CC), cadmium chloride (CC)+cadmium fluoride (CdF_2 or CF), cadmium chloride (CC)+gallium chloride ($GaCl_3$ or GC), indium chloride ($InCl_3$), (IC) and ammonium chloride (AC). The etching of the devices was carried out using both acidic (H_2SO_4+$K_2Cr_2O_7$) and alkaline (NaOH+$Na_2S_2O_3$) aqueous solutions [7]. Finally gold (Au) back metal contacts were evaporated on the etched CdTe surfaces. The devices were characterised both under AM1.5 illuminated and dark conditions to extract relevant electronic parameters to evaluate their solar to electricity conversion efficiencies. Capacitance-voltage (C-V), and Mott-Schottky ($1/C^2$-V) plots of some of the fabricated devices were implemented to further study the electronic properties of these devices.

8.2 CdS/CdTe solar cell fabrication process

This process was taken as a standard for all solar cells fabrication procedure in this research. Glass/FTO substrate with a sheet resistance of (7-13) Ω/square was used as the substrate for all fabricated solar cell devices. The fabrication of basic CdTe-based device structures involves the sequential deposition of the two layers of CdS window layer and the CdTe absorber layer. The first step was the cleaning of the glass/FTO substrates using soap solution then rinsed in de-ionised water and degreased in methanol, rinsed with deionised water and dried in air. For a 3-layer graded bandgap device, a buffer layer is deposited between the FTO and the CdS window layer. The typical thickness range of buffer and window layers are ~(80-250) nm, and ~(1500-2500) nm thick for the CdTe absorber layer.

For basic CdS/CdTe solar cells, CdS window layers of ~100 nm thick were electroplated on glass/FTO substrates. After growth, the layers were rinsed with de-ionised water and dried in air. Thereafter, the cadmium chloride (CC) activation treatment was carried out by either dipping or spreading saturated aqueous CC solution on the CdS layers and allowing it to dry inside a fume cupboard in air. Then the layers were annealed at 400°C for 20 minutes in air using a conventional furnace, and allowed to cool down slowly in air. The CC heat treatment was carried out to activate the photovoltaic properties of the CdS layers and improve charge carrier transport. The samples were then rinsed with de-ionised water to remove the CC powder residue and other contaminants on the layer surface and dried in air.

The next step is the electroplating of n-CdTe absorber layers on the glass/FTO/CdS substrate. The CdTe layers were grown at voltages higher than the V_i to obtain Cd-rich CdTe desired for the n-type CdTe layer in line with our device model. After growth, the CdTe layers were rinsed in de-ionised water and dried in air. The next step is the chemical activation treatment of the CdTe layers necessary for high performance solar cell devices [8]. The activation step was carried out by dipping or spreading the chemical solution on the CdTe surface. After drying, the samples were then annealed in air at temperatures between 400-450°C within the duration of 10-20 minutes in air and allowed to cool down slowly. The samples were then cleaned with de-ionised water to remove any powder residue used for the activation treatment and other contaminants on the CdTe surfaces and dried. Figure 8.1 shows the complete device fabrication process for the n-CdS/n-CdTe solar cell while Figure 8.2 shows the layer deposition sequence

on the (a) glass/FTO substrate, (b) glass/FTO/n-CdS, (c) glass/FTO/n-CdS/n-CdTe and (d) glass/FTO/n-CdS/n-CdTe/Au complete solar cell device.

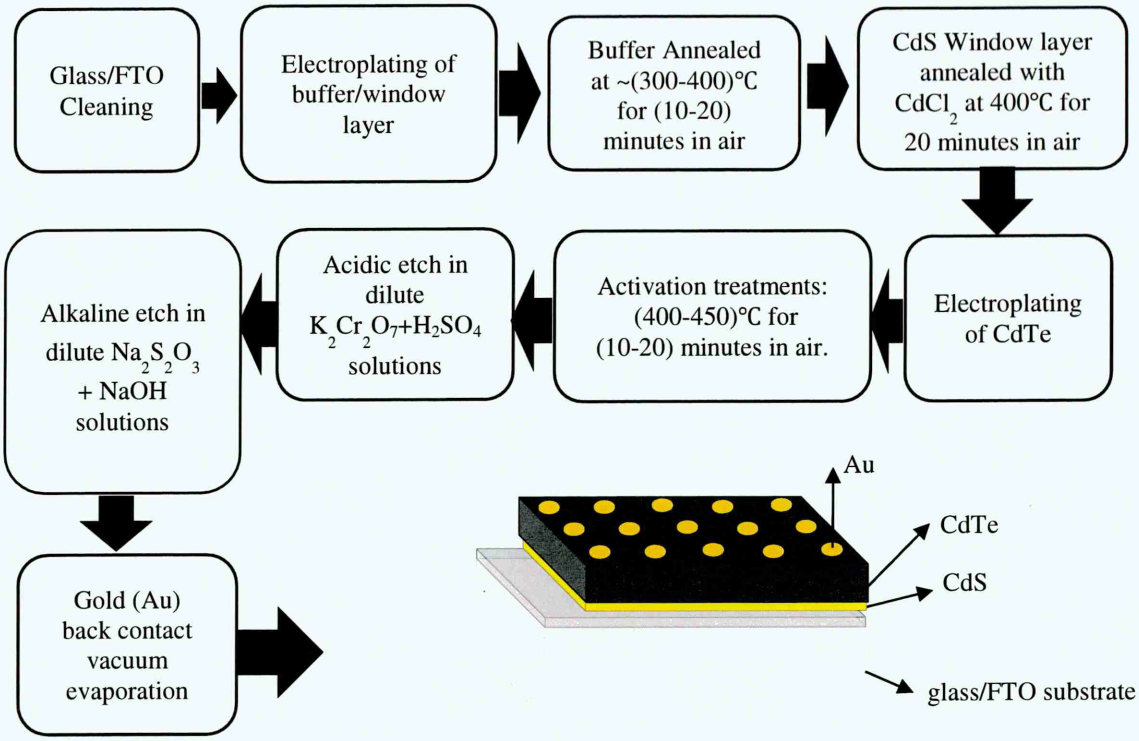


Figure 8-1: Processing steps for CdS/CdTe solar cell device fabrication.

The next step is the etching of the devices in acidic and alkaline solution. As earlier mentioned, the etching procedures and etchants used are selected to leave Cd-rich CdTe surface rather than Te-rich surface and also to eliminate or reduce surface defects. Figure 8.3 depicts the band diagrams of these two situations of Te-rich (Figure 8.3(a)) and Cd-rich (Figure 8.3(b)) CdTe surfaces. For high performance solar cells, Cd-rich CdTe surfaces are preferable due to formation of large Schottky barrier height (ϕ_b) at the n-CdTe/metal interface [9] which improves the open circuit voltage (V_{oc}) of the device due to high potential barrier created by the shape of the band bending formed within the device as shown in the energy band diagram of Figure 8.3(b). Under this situation, the charge carriers will be forced to their respective electrical contacts of the external circuit, creating useful energy before they recombine. However, these processes are only true for optimised devices. Otherwise low quality device with poor electronic properties are observed [9].

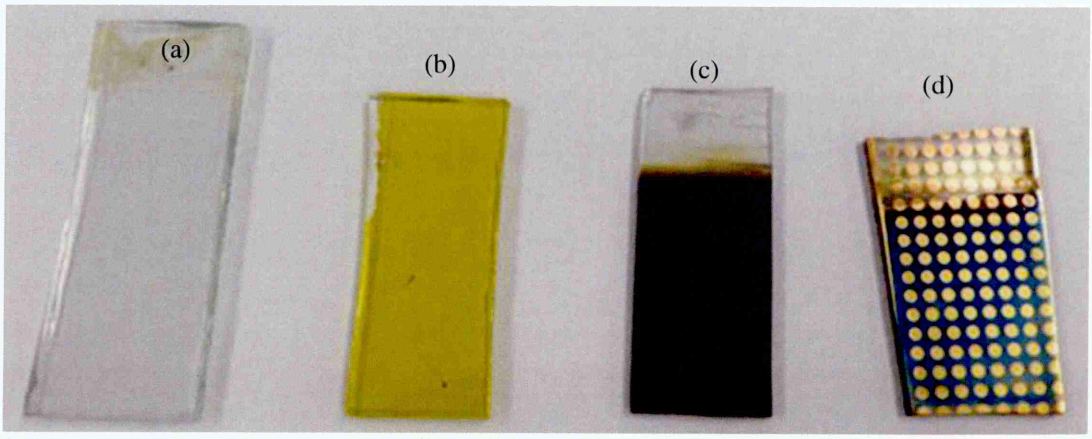


Figure 8-2: Layer deposition steps for the fabrication of n-CdS/n-CdTe-based solar cell. (a) glass/FTO substrate (b) glass/FTO/n-CdS (c) glass/FTO/n-CdS/n-CdTe and (d) complete glass/FTO/n-CdS/n-CdTe/Au solar cells.

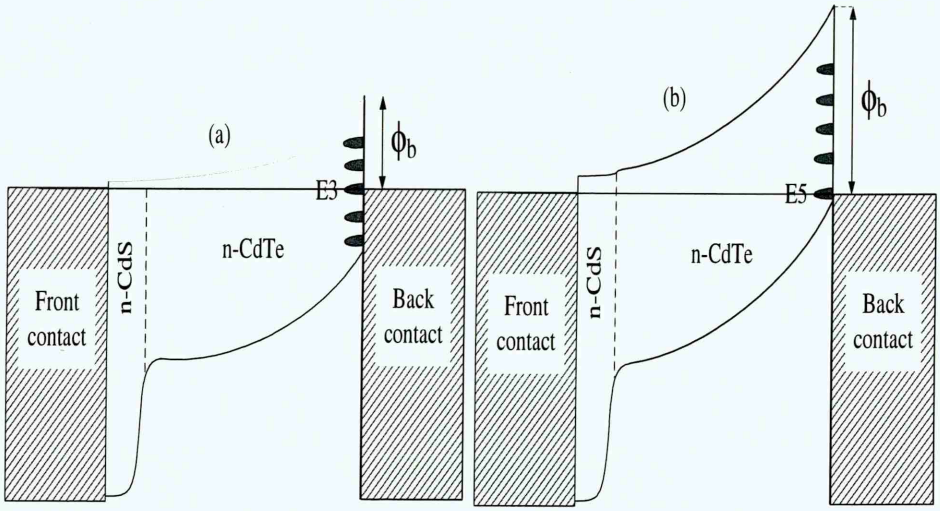


Figure 8-3: Fermi level pinning positions and barrier height for n-CdTe/metal interface of (a) Te-rich and (b) Cd-rich layer. Note the Fermi level is at the midgap for Te-rich surface while for the Cd-rich surface, the Fermi level is pinned close to the valence band maximum.

After etching, the device structures were rinsed in de-ionised water and dried in air. The devices were completed by evaporating gold (Au) metal back contacts on the etched CdTe surfaces. This step was carried out using Edwards 306 vacuum metalliser shown in Figure 8.4. A piece of Au wire, 99.995% purity purchased from Fisher Scientific

Company was placed on a tungsten filament. After arranging the samples on a metallic mask with 2 mm diameter circular holes, they were then transferred to the Edwards 306 vacuum system and the pressure of the chamber was 10^{-4} Pa (10^{-6} mbar) before Au evaporation. The evaporation rate and the thickness of the contacts were controlled using FTM7 thickness monitor attached to the metalliser and the thickness used was ~100 nm. Each of these Au contacts is a solar cell ready for electrical characterisations. Figure 8.5 shows the fully automated I-V system of Keithley 2401 source meter with embedded power supply unit and solar simulator used for device characterisation.

Figure 8-4: Edwards Auto 306 automatic vacuum metalliser used to deposit Au back contacts.

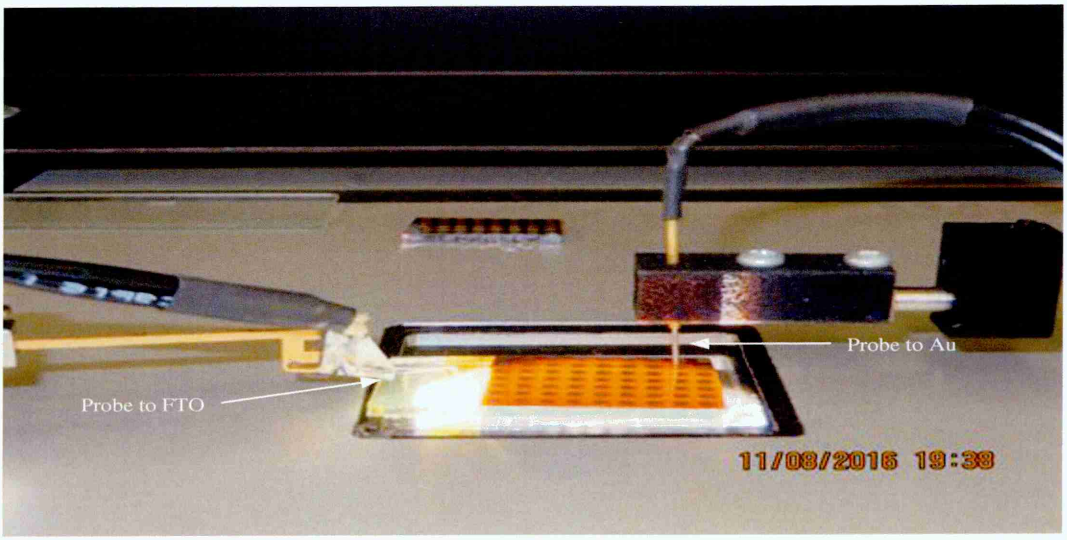


Figure 8-5: The sample holder of the fully automated I-V system used for device measurement and characterisation.

8.3 Fabrication of glass/FTO/n-CdS/n-CdTe/Au solar cell

Figure 8.6 shows the energy band diagram of glass/FTO/n-CdS/n-CdTe/Au solar cell device. The description of band diagram based on this structure was given in section 2.3.2. However, this band diagram is presented here for ease of discussion. This experiment was conducted to investigate the effects of different surface treatments on glass/FTO/n-CdS/n-CdTe/Au solar cell devices. Similar procedure outline in section 8.2 was followed to deposit ~250 nm and ~2200 nm thicknesses of CdS and CdTe layers respectively. The CC treatment of CdS has been reported to form a better CdS/CdTe junction with enhanced solar cell conversion efficiency [10]. Afterwards, n-CdTe layer of ~2200 nm thick was deposited on the glass/FTO/CdS substrate.

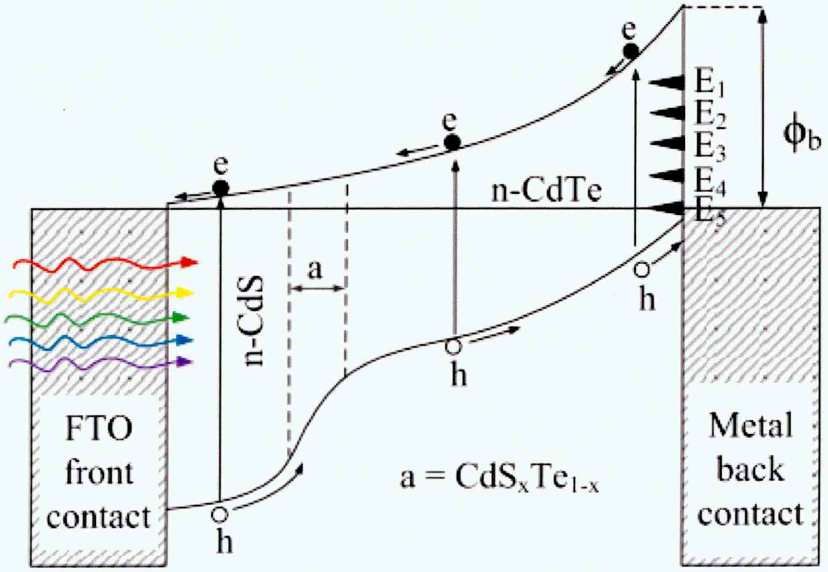


Figure 8-6: The energy band diagram of an n-n+Schottky barrier for glass/FTO/n-CdS/n-CdTe/Au solar cell device.

The high lattice mismatch of ~10% [10–12] between CdS and CdTe should produce poor devices if not for the interface miscibility between the CdS and CdTe [10]. The lattice mismatch notwithstanding, CdS has so far remained the best heterojunction partner to CdTe for the manufacture of low-cost and efficient CdS/CdTe solar cell devices [13–16].

The miscibility between the CdS and the CdTe occurring at the CdS/CdTe interface result in the formation of the CdS_xTe_{1-x} ternary alloy marked as region "a" which helps in removing the abrupt nature of the junction by smoothening out the interface and reducing recombination centres [17]. This alloy occurs due to diffusion of sulphur from

the CdS into CdTe during annealing process. The junction miscibility depends on the rate of the interface diffusion which in turn depends on the level of Cl and the annealing temperature. The intermixing at the interface also assists in the grading of the bandgap removing any spikes which can effectively harness most of the photons at different regions of the solar spectrum thereby reducing thermalisation effect. But excessive intermixing of the junction can cause the diffusion of Te into the CdS leading to reduced CdS bandgap thereby increasing the window absorption which will impact negatively on the device short-circuit current density (J_{sc}) [18–20]. In this device structure, the possible incorporation of processes such as the impurity PV effect and impact ionisation can contribute significantly to the solar cell performance. This device utilised the impurity states at the rear of the device and the IR to improve the conversion efficiency.

The benefits of the post growth chemical treatment step include grain growth, grain boundary passivation, CdS/CdTe interface alloying and reduced lattice mismatch between the CdS and CdTe layers [8,21]. The nature of the bandgap grading in the diagram indicates that electron-hole pairs can be created throughout the thickness of the device. The fundamental losses in solar cells are due to optical, electrical and recombination losses [22]. Optical losses are usually from the window layers of the device. These losses included reflection from the glass substrate, FTO and the CdS window layers [22]. To reduce absorption losses, the use of thinner CdS layers is usually emphasised so that high energy photons can reach the CdTe absorber for the creation of photo-generated charge carriers in the device [23]. However, thinning down the CdS will impact negatively on V_{oc} and FF due to possible formation of FTO/CdTe parallel junctions [17,24,25]. The V_{oc} is mostly affected by consumption of the thin CdS layers into the CdTe layer creating pinhole or low resistive paths between the FTO and the CdTe [26]. The layers of polycrystalline CdS deposited on rough FTO surface should be thick enough to cover the FTO spikes. This is further complicated due to the growth method (electroplating) which is electric field driven. In this growth method, nucleation starts at the FTO spikes leaving gaps between grains or agglomerations which can contribute to the layer non-uniformity. Coalescence of grains may be helpful when submicron grains coalesced to form a block of grain of few micron sizes that will enhance charge carrier transport. On the other hand, it is likely that the coalescence will open up pinholes along the grains boundaries that will ultimately short the device. Scratching the FTO surface or the completed device structure with sharp objects during cleaning or other device processing procedures can also lead to the formation of

pinholes in the device. Etching procedure should be carefully done within an appropriate duration; etching for a long period of time can also result to loss of layers and opening of pinholes. Shorting of device occurs when a back contact metal sit on a pinhole extending from the FTO to the CdTe surface forming glass/FTO/Au parallel junction structure instead of the desired glass/FTO/In_xSe_y/n-CdS/n-CdTe/Au structure. The former device structures will lead to poor device parameters while the latter devices will produce better solar cell device parameters.

Prior to the post growth activation step, the as-deposited n-CdS/n-CdTe sample was cut into three parts for three different surface treatments with CC, CF and CG. All samples were heat-treated (HT) at 420°C for 20 minutes in air. Table 8.1 presents the summary of the device parameters measured under AM1.5 conditions for the best 3 cells from each heat treatment condition and the plot of the J-V curves for the best 3 cells one from each heat treatment condition are presented in Figure 8.7.

The results show that, cells treated in the presence of CF show relatively better performance followed by the cells treated in CC while the least performance was observed in cells treated in the presence of CG. The relatively better performance observed in CF treated cells could be due to the incorporation of F in the usual CC solution. There are reports on the improvement in solar conversion efficiency when F is included in the CC treatment either in wet chemical treatment [27–30] or in a gaseous form [31,32]. Fluorine (F) is a member of group VII (halogens) with the smallest ionic radii and low density which makes it easier to diffuse through the device grain boundaries impacting positively on both structural and electrical properties of the device.

The relatively low performance exhibited by cells annealed in CC could be due to high series resistance as a result of possible formation of oxides layers (CdO, TeO_2, $CdTeO_x$) at the n-CdTe/Au interface due to incomplete surface passivation by the etching process [33,34]. The same possible reasons hold for the poor performance in devices treated in the presence of CG. However, as illustrated in Figure 8.7, the CG treated layers show very high series resistance and low shunt when compared to the other devices. In addition to the above reasons, the observed low efficiencies in the CG treated device structures could be due to the creation of shunting paths through which useful currents are lost.

Table 8-1: Summary of measured parameters for glass/FTO/n-CdS/n-CdTe/Au solar cell device under AM1.5 conditions. Samples were all annealed at 420°C for 20 minutes in air.

Device ID	HT at 420°C with CC			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
CD1	548	16.5	0.31	2.8
CD2	519	14.9	0.38	2.9
CD3	499	16.7	0.36	3.0
Average	**524**	**15.6**	**0.36**	**2.9**
Device ID	HT at 420°C with CF			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
FDI	565	16.4	0.40	3.7
FD2	562	16.4	0.41	3.8
FD3	552	16.3	0.43	3.9
Average	**560**	**16.4**	**0.41**	**3.8**
Device ID	HT at 420°C with CG			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
GD1	482	10.3	0.31	1.5
GD1	399	12.9	0.33	1.7
GD1	471	12.7	0.32	1.9
Average	**451**	**12.0**	**0.32**	**1.7**

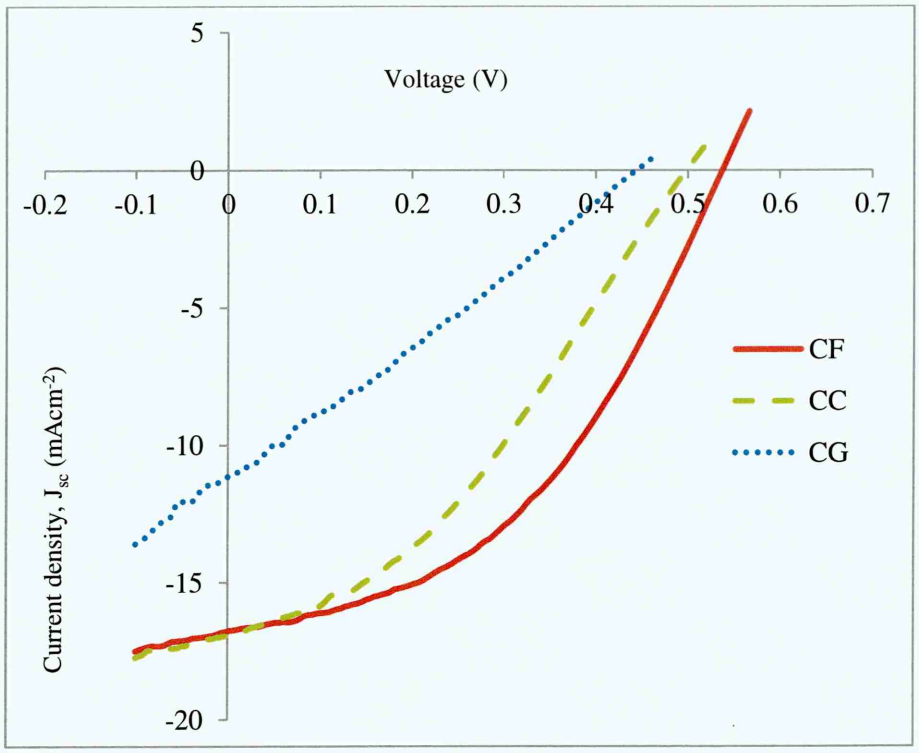


Figure 8-7: J-V characteristics under AM1.5 condition for glass/FTO/n-CdS/n-CdTe/Au solar cells annealed with different surface treatments. Heat-treatment was done at 420°C for 20 minutes in air.

8.4 Fabrication of n-In_xSe_y/n-CdTe/Au solar cells

In this study, a wide bandgap (2.90 eV) In_xSe_y layer was used as a window layer in n-In_xSe_y/n-CdTe/Au solar cell configuration. Firstly, In_xSe_y layer of ~150 nm thick was electroplated on glass/FTO substrate. After growth, the layer was rinsed with de-ionised water, allowed to dry in air and then annealed in a conventional furnace at a temperature of 300°C for 10 minutes in air. Afterwards, n-CdTe layer of ~1800 nm thick was deposited on the glass/FTO/n-In_xSe_y substrate. Thereafter, the layer was rinsed with de-ionised water and allowed to dry in air. The sample stack was then divided into 3 separate samples for surface treatments with CC, CF and IC. The device structure was allowed to dry in air before annealing in furnace at temperature of 400°C for 10 minutes in air. The layers were then allowed to cool down slowly in air before etching. After etching, the devices were completed by evaporating Au metal back contacts. The summary of measured parameters under AM1.5 illumination conditions is presented in Table 8.2 and the highest efficiency of 0.13% was observed in cell annealed with CF and plotted in Figure 8.8.

The annealing times and temperatures for these semiconductors were optimised during characterisation process under material growth parameter optimisation. Solar cell devices are require high temperature annealing in the region of 400°C for high performance. In_xSe_y was optimised at an annealing temperature of 300°C for 10 minutes as shown in Figure 4.3. Though, this may change depending on the material thickness and device structure. Another point to consider is that, In_xSe_y does not require high temperature heat treatment due to volatile nature of Selenium. The annealing temperature of around for 400°C for CdTe device fabrication is well documented in the literature [35,36]. These reports show that for high efficiency solar cells, CdTe is usually annealed at temperatures from above 400°C. This corroborates with the results obtained in this research as will be seen later in this thesis. Another reason was based on the result published in Figure 7.5 in this thesis. This Figure summarised solar cell efficiency as a function of annealing/growth temperature.

These results show that irrespective of the heat treatment conditions, all the devices show poor solar to electricity conversion parameters. The poor performance could majorly be due to the large R_s and low R_{sh} in these devices. The best cell achieved in this experiment (Figure 8.8) shows a R_s of 312 Ω and R_{sh} of 355 Ω under illumination condition. The large R_s could be due to surface oxidation prior to metallisation process which adds more resistance to the devices resulting to low J_{sc} values. Another reason for the low J_{sc} could also be as a result of recombination centres in the bulk materials or at the interface which kill the photo-generated charge carriers within the device. The low R_{sh} observed could be due to shunting path within the devices which is associated with the low FF values in these devices.

A good solar cell should have low R_s and high R_{sh}. The generally poor performance observed in these set of devices can be mainly attributed to their high R_s and low R_{sh} as observed from Figure 8.8. This exercise shows that the In_xSe_y require further optimisation as window layer for a better performance in CdTe based solar cells.

Table 8-2: Measured solar cell parameters for n-In_xSe_y/n-CdTe/Au under AM1.5 illumination conditions.

Sample ID	HT at 400°C with CC			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η(%)
CC-D1	009	5.4	0.25	0.01
CC-D2	010	6.1	0.25	0.02
Average	**095**	**5.8**	**0.25**	**0.03**
Sample ID	HT at 400°C with CF			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
CCF-D1	042	6.9	0.26	0.07
CCF-D2	071	7.2	0.25	0.13
Average	**057**	**7.1**	**0.51**	**0.1**
Sample ID	HT at 400°C with IC			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
ICC-D1	045	0.8	0.24	0.01
ICC-D2	109	1.4	0.24	0.04
Average	**77**	**1.1**	**0.24**	**0.05**

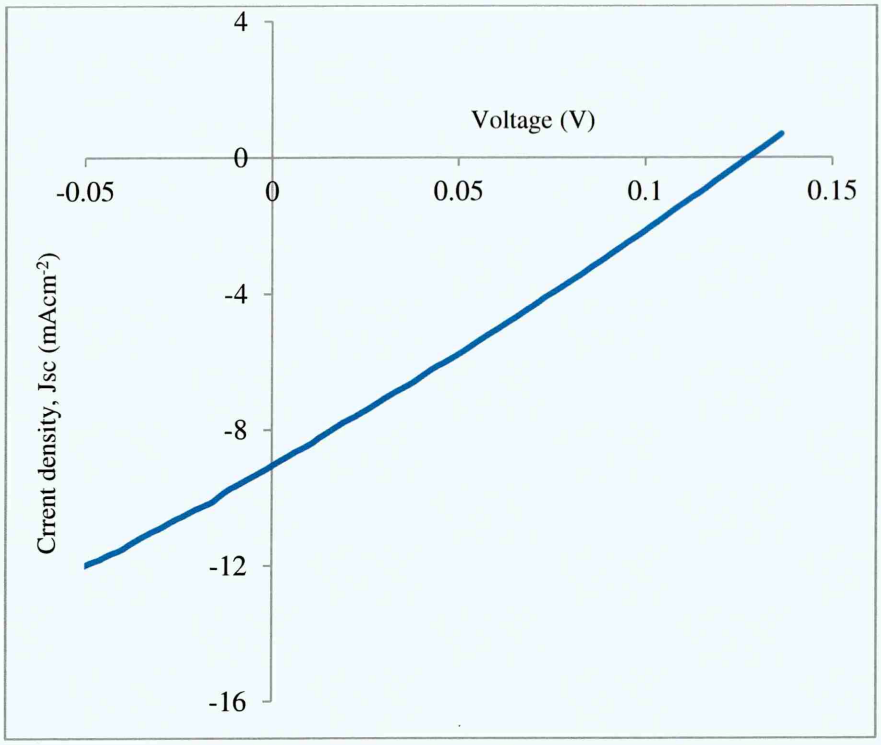


Figure 8-8: Typical Light J-V curve plot for glass/n-In_xSe_y/n-CdTe/Au solar cell under AM1.5 illumination conditions.

8.5 Fabrication of multi-layer graded bandgap solar cell devices

This section presents solar cells based on the multi-layer graded bandgap devices that was earlier introduced in section 2.4.5. At present, the existing solar cell structures are based on p-n homo-or heterojunction type structures or p-i-n type devices. The homo-junction can only absorb photons from a particular region of the solar spectrum due to their single bandgap nature. This situation is improved if the device is a hetero-junction type having two different bandgaps so that the absorption region can be further extended for improved device performance.

The best and effective means to harvest photons from most of the solar spectrum is by the use of multi-layer graded bandgap devices [37]. This device structure was explained in section 2.4.5. The multi-layer graded bandgap design structure shown in Figure 2.10 was experimentally tested and reported by Dharmadasa *et al.* [38] in 2005 using well established AlGaAs grown using MOCVD method. The device structure was based on p-i-n AlGaAs graded bandgap solar cells achieving efficiency of ~20% within only two growths. This device exhibited a record V_{oc} value of 1175 mV for a single device with FF 0.85. The observation of V_{oc} of 950 mV under complete darkness indicates

contributions from impurity PV effect confirming the incorporation of IR in these devices as shown from the responsivity plots reported in reference [39].

After testing the viability of this device design using costly material and process, the task ahead is to test this design using low-cost materials and less expensive growth process like electrodeposition technique. The solar energy research group at Sheffield Hallam University has made a significant progress in the development of multi-layer graded bandgap solar cells using low-cost electroplating technique. In 2014, Echendu *et al.* [29] reported an efficiency of 10.4% based on this device structure. In 2016, Olusola *et al.* [40] increased this efficiency to 12.8%. Another breakthrough in the same year (2016) was achieved when Ojo and Dharmadasa [16] reported 15.3% efficient devices. The research and development of solar cells based on graded bandgap using low cost electroplating process is continuing from strength to strength to achieve highest possible solar cell efficiencies.

In this section, the devices were made from 3-layer graded bandgap structures incorporating In_xSe_y and ZnS as buffer layers in glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au respectively.

8.5.1 The effect of different annealing condition on the performance of glass/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells

These experiments were carried out to study the effect of different annealing temperature on the performance of these device structures. Figure 8.9 shows the energy band diagram of a multilayer graded bandgap device based on glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cell structure. The 3-layer device was fabricated using In_xSe_y, CdS and CdTe thin films with approximate layer thickness of 100 nm, 200 nm and 2500 nm respectively. The bandgaps of In_xSe_y, CdS and CdTe used in these experiments were 2.90, 2.42 and 1.45 eV respectively. In_xSe_y with a wider bandgap of 2.90 eV was incorporated as a buffer layer between the glass/FTO and the CdS window layer in the n-CdS/n-CdTe solar cells. The incorporation of wide bandgap In_xSe_y is mainly to grade the bandgaps of the device structure and increase wider absorption coverage from the solar spectrum. This bandgap can transmit most of the incident high energy photons into the device with minimum window absorption. After sequential growth of In_xSe_y and CdS, the sample was annealed with CC at 400°C for 20 minutes in air. Then n-CdTe was deposited and the sample stack was divided into three samples for processing under different conditions. Each of the three samples was further cut into three samples.

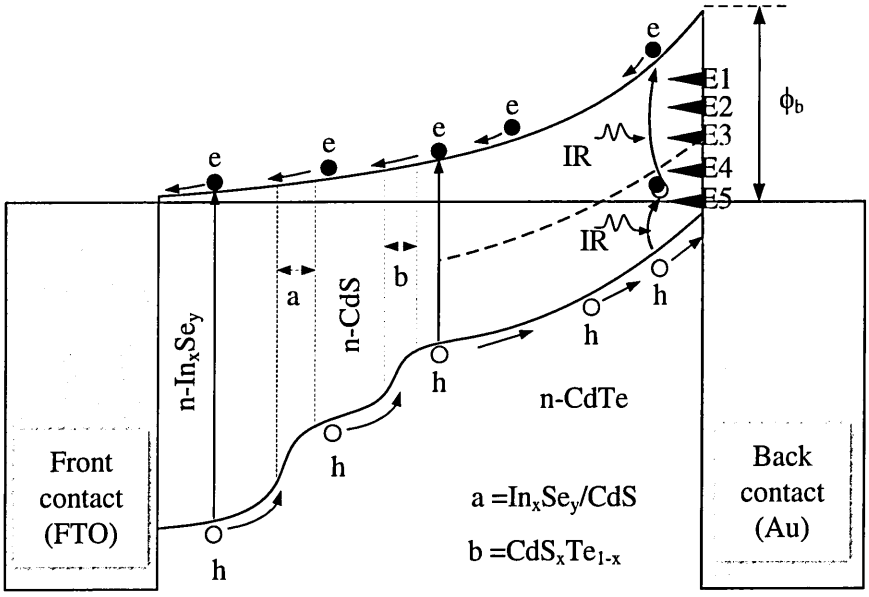


Figure 8-9: Energy band diagram of glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au [Diagram not to scale].

The first three samples were annealed in air only (HT) at temperatures of 380, 420 and 450°C. The second three samples were annealed at 380, 420 and 450°C in the presence of CC while the last three samples were annealed with CF at 380, 420 and 450°C. All annealing was carried out for 20 minutes in air. However, samples annealed at 450°C in both CC and CF could not survive the heat treatment as they were characterised by high density of pinholes probably due to the high temperature coupled with the chemical treatment. Another possible reason for this could be due to the volatile nature of selenium especially when high temperatures are used [41]. This will lead to sublimation of the layer creating pinholes in the devices.

Table 8.3 shows the summary of measured parameters under AM1.5 illumination conditions for the best 3 cells from each heat treatment temperature. Note that these samples were annealed at different temperatures in air only and Figure 8.10 depicts the J-V curves for the best 3 cells one from each heat treatment temperature. Observation from Table 8.3 and Figure 8.10 shows a generally poor performance for all devices irrespective of the heat treatment temperature.

Table 8-3: Summary of measured device parameters for glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au for 3 devices annealed at 380, 400 and 450°C for 20 minutes in air. Note that samples were only annealed in air without any chemical treatment.

Device ID	HT at 450°C (No chemical treatment)			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
C154-1D1	485	12.3	0.31	1.8
C154-1D2	469	13.4	0.31	1.9
C154-1D3	499	14.7	0.33	2.4
Average	**481**	**13.5**	**0.32**	**2.0**
Device ID	HT at 400°C (No chemical treatment)			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
C154-2D1	500	9.3	0.28	1.3
C154-2D2	474	10.7	0.29	1.5
C154-2D3	470	13.0	0.30	1.8
Average	**481**	**11.0**	**0.29**	**1.5**
Device ID	HT at 380°C (No chemical treatment)			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
C154-3D1	564	14.2	0.29	2.3
C154-3D2	564	14.9	0.31	2.6
C154-3D3	478	15.9	0.36	2.7
Average	**535**	**15.0**	**32.0**	**2.5**

All devices show comparable solar cell parameters. The poor performance can be attributed to the elimination of the activation step necessary for high performance solar cell devices [8]. The benefits of the activation step such as grain growth, grain boundary passivation, and junction intermixing are all missing in these devices. This indicates that the photovoltaic properties of these devices were not well activated and are full of

defect states and recombination centres. To improve these devices, the remaining two sets of the sample were activated using chemical treatments as will be discussed later in this section.

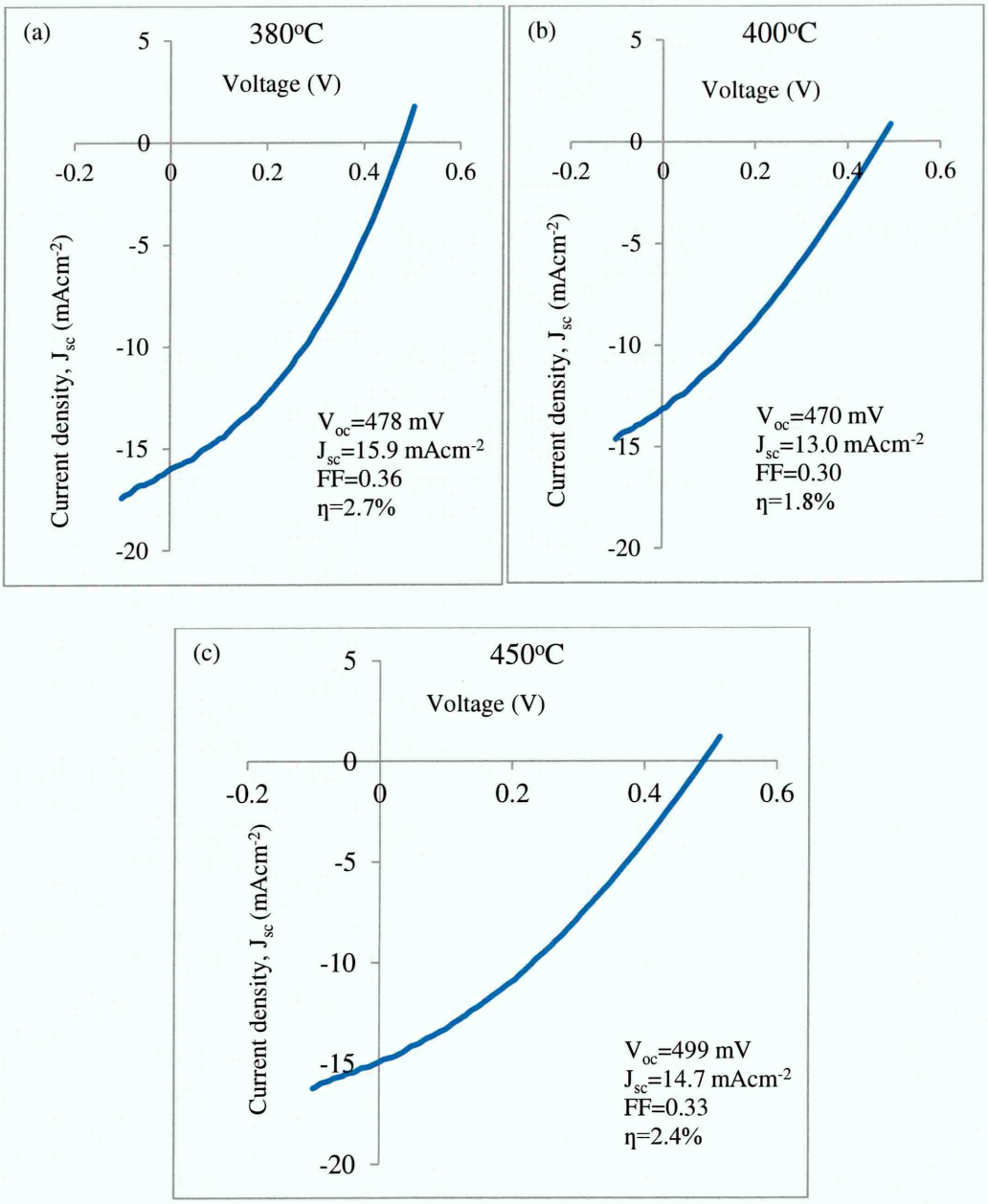


Figure 8-10: Typical J-V curves under AM1.5 illumination for the best 3 cells of glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au devices annealed in air at (a) 380°C, (b) 400°C and (c) 450°C.

This study was carried out in continuation of the previous experiments to investigate the effect of surface treatments on the remaining two sets of the samples. Each of these sets consist of three samples as earlier mentioned, one of the set was annealed with CC at 380, 400 and 450°C while the other set was annealed with CF at 380, 400 and 450°C.

However, the samples annealed at 450°C in both treatments could not survive this treatment temperature possibly due to the earlier mentioned reasons. Table 8.4 shows the summary of measured device parameters under AM1.5 illumination conditions for the best 3 cells from each heat treatment condition. The J-V curves for the best cell selected from Table 8.4 under the two different surface treatment conditions are plotted on the same graph in Figure 8.11 for easy comparison. For these set of devices, the heat treatment condition was 380°C for 20 minutes in air. After annealing in the presence of CC and CF, improvement in device parameters such as V_{oc}, J_{sc} and FF were observed when compared with the previous experiment of only air annealed samples (see Table 8.3). The improvements in device parameters after CC [21,42] or CF [43,44] heat treatments are abundantly available in the literature. The post growth heat-treatment of CdTe-based devices in the presence of Cl comes with benefits such as recrystallisation, grain growth, grain boundary passivation, junction intermix, increase in charge carrier lifetime and collection at the external circuit. All these features contributed to the devices improvements. The results show that the device parameters were comparable in both treatments though the highest efficiency was recorded in sample annealed in the presence of CF. The highest efficiency recorded for the sample annealed in the presence of CC (cell S83-33) show V_{oc}, J_{sc}, FF and η of 564 mV, 16.2 $mAcm^{-2}$, 0.48 and 4.4% respectively. While the highest efficiency cell (cell S83-23) annealed in the presence of CF show V_{oc}, J_{sc}, FF and η of 583 mV, 16.8 $mAcm^{-2}$, 0.49 and 4.8% respectively.

The improvement in the V_{oc} values of these devices could be attributed to increased defects passivation within the device and on the CdTe surface which improve carrier collections at both the In_xSe_y/CdS and at the CdS/CdTe interfaces. The alloys formed at these two interfaces help in the gradual grading of the devices removing the supposedly abrupt junction nature. This also helps to improve the band bending in the device structure due to enhanced electric field as a result of improved junction quality within the solar cell impacting positively on the J_{sc} of the devices. The relatively higher device parameters obtained in the CF treated sample could be due to the inclusion of F in the CC treatment. Fluorine is one of the halides of group VII with the least atomic radii and density than Cl in the group hence it can diffuse more easily through the grain boundaries [44] impacting positively on the carrier separation and collection.

Table 8-4: Summary of device parameters measured under AM1.5 illumination conditions for glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells. All samples were heat treated at 380°C for 20 minutes in air in the presence of CC and CF.

Device ID	HT at 380°C with CC			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
S83-31	568	16.2	0.45	4.1
S83-32	572	15.0	0.49	4.2
S83-33	564	16.2	0.48	4.4
Average	**568**	**15.8**	**0.47**	**4.2**
Device ID	HT at 380°C with CF			
S83-21	594	16.5	0.46	4.5
S83-22	580	18.2	0.45	4.7
S83-23	583	16.8	0.49	4.8
Average	**586**	**17.2**	**46.3**	**4.6**

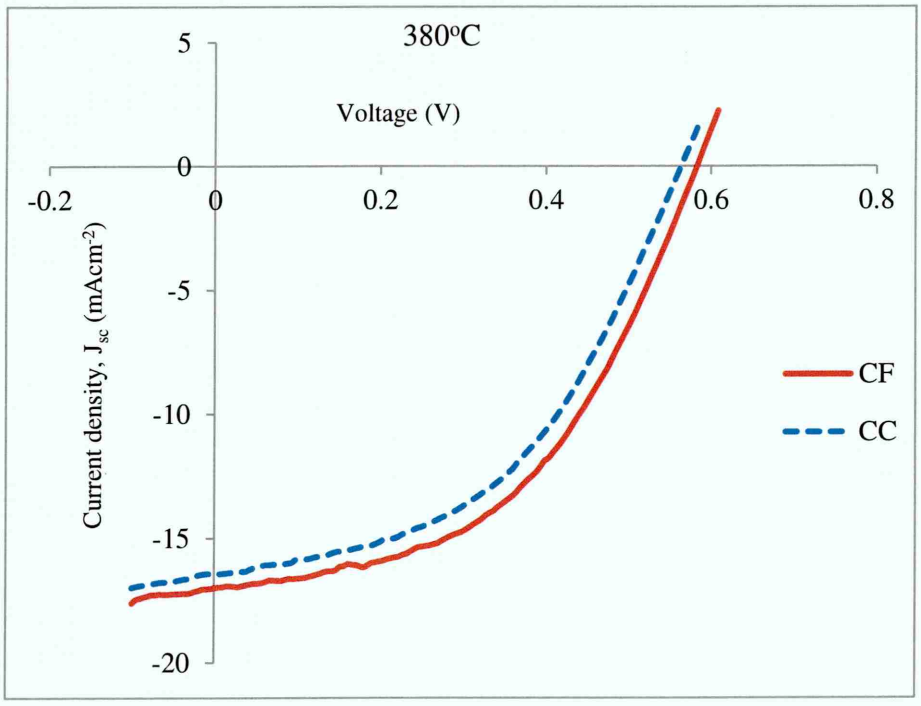


Figure 8-11: J-V curves for glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells under AM1.5 illumination conditions. Samples were heat-treated at 380°C for 20 minutes in the presence of CC and CF.

Table 8.5 shows the summary of measured device parameters under AM1.5 illumination conditions while Figure 8.12 illustrates the J-V curves of the best cell obtained for each of the treatment. After annealing at 400°C, a reduction in all device parameters for cells annealed in the presence of CC is observed while significant improvement is noticed in cells annealed in the presence of CF. The relatively low performance registered in the CC treated cells could either be due to the high series resistance as a result of surface oxidation prior to back contacts metallisation. In fact, this is very likely as observed in the J-V curve of the CC treated cell shown in Figure 8.12.

Table 8-5: Summary of device parameters measured under AM1.5 illumination conditions for glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells. All samples were annealed in the presence of CC and CF at 400°C for 20 minutes in air.

Device ID measured	HT at 400°C with CC			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
S83-31	539	13.5	0.32	2.3
S183-32	503	13.4	0.37	2.5
S83-33	513	14.2	0.36	2.6
Average	**518**	**13.7**	**0.35**	**2.5**
Device ID measured	HT at 400°C with CF			
S83-21	582	19.4	0.51	5.8
S83-22	589	21.5	0.50	6.3
S83-23	594	21.9	0.50	6.5
Average	**588**	**20.9**	**0.50**	**6.2**

The low R_{sh} could be due to formation of pinholes in the devices. Comparatively, the cells annealed in the presence of CF show better device performance in all solar cell parameters. The highest efficiency cell treated with CC show electronic parameters of V_{oc}, J_{sc}, FF and η of 513 mV, 14.2 $mAcm^{-2}$, 0.36 and 2.6% respectively. While the highest efficiency cell treated in the presence of CF recorded parameters of V_{oc}, J_{sc}, FF and η of 594 mV, 21.9 $mAcm^{-2}$, 0.50 and 6.5% respectively. This significant difference

in the conversion parameters of the two treatments has to do with the inclusion of the F. Since both CC and CF act as fluxing agents influencing grain growth and recrystallisation [25] in CdTe solar cells; therefore, it is reasonable to credit the improved device parameters in the CF treatment to combined effect when CF is used rather than when only CC treatment is used. The results of the CF cell show improved surface states passivation, healthy junctions' quality with reduced recombination centres and improved optical properties of the window layers.

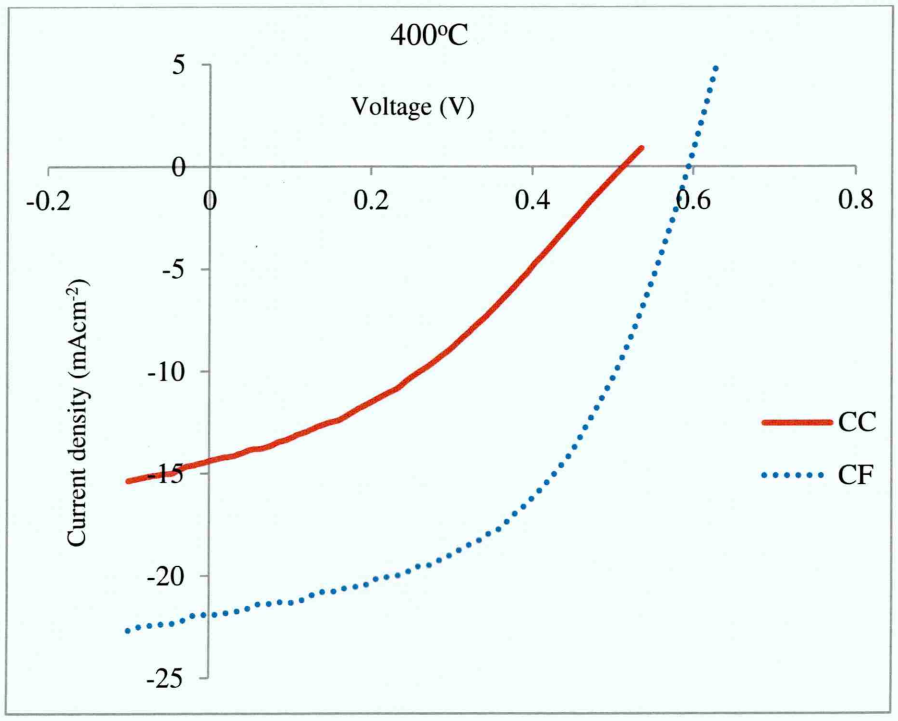
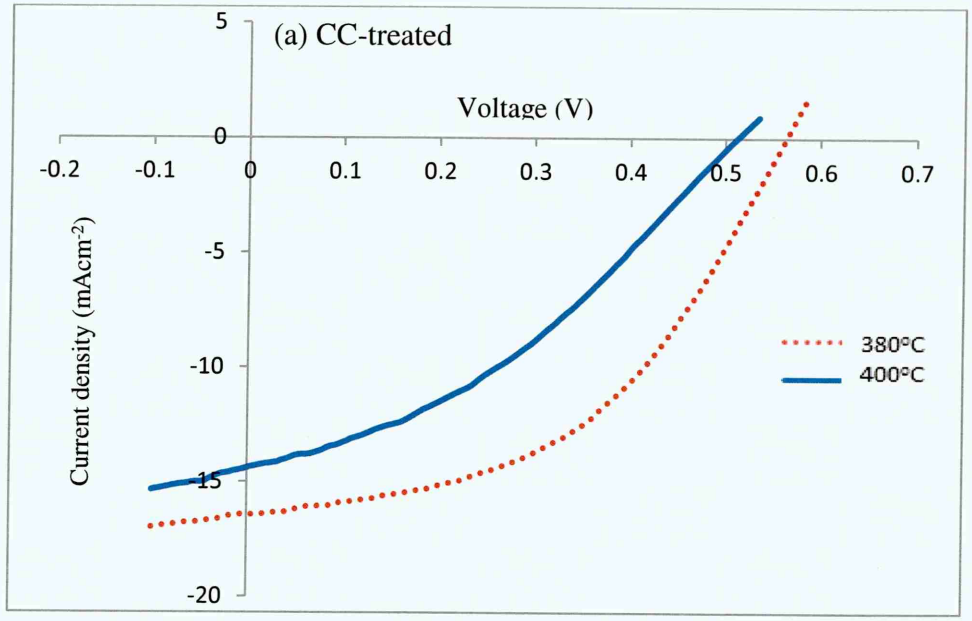


Figure 8-12: J-V curves under AM1.5 illumination of glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells. Samples were heat-treated at 400°C for 20 minutes in the presence of CC and CF.

Figure 8.13 shows the plot of the J-V curves for the effect of annealing temperature for (a) CC and (b) CF treated for the above fabricated solar cells. It is observed that in Figure 8.13(a), the cell annealed at 380°C show higher efficiency parameters than the cell annealed at 400°C. This could be due to formation of oxides on the layer prior to back contact formation. Another reason for this could be as a result of pinholes which affect all device parameters.

In Figure 8.13(b), it is seen that the cell annealed at 400°C show higher efficiency than the cell annealed at 380°C. This is attributed to increased crystallinity with temperature which reduces grain boundaries and increased current collection in this cell.



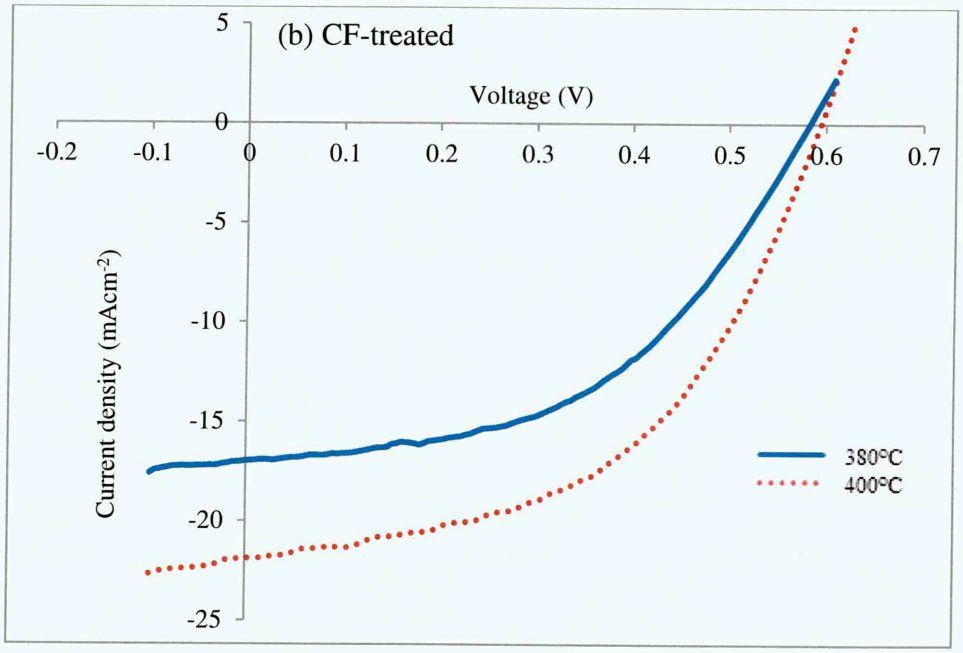


Figure 8.13: The effect of annealing temperature (a) CC treated and (b) CF treated on the fabricated solar cell devices.

The high efficiency cell of 6.5% obtained in this experiment was further analysed under dark condition. Figure 8.14 shows (a) log-linear and (b) linear I-V behaviour of the cell under dark condition. The parameters obtained under dark condition for this cell are;

$RF=10^{1.7}$, $I_o=1.58\times10^{7}$ A and n=4.0. The R_s and R_{sh} under illumination conditions are 156 Ω and 3364 Ω respectively.

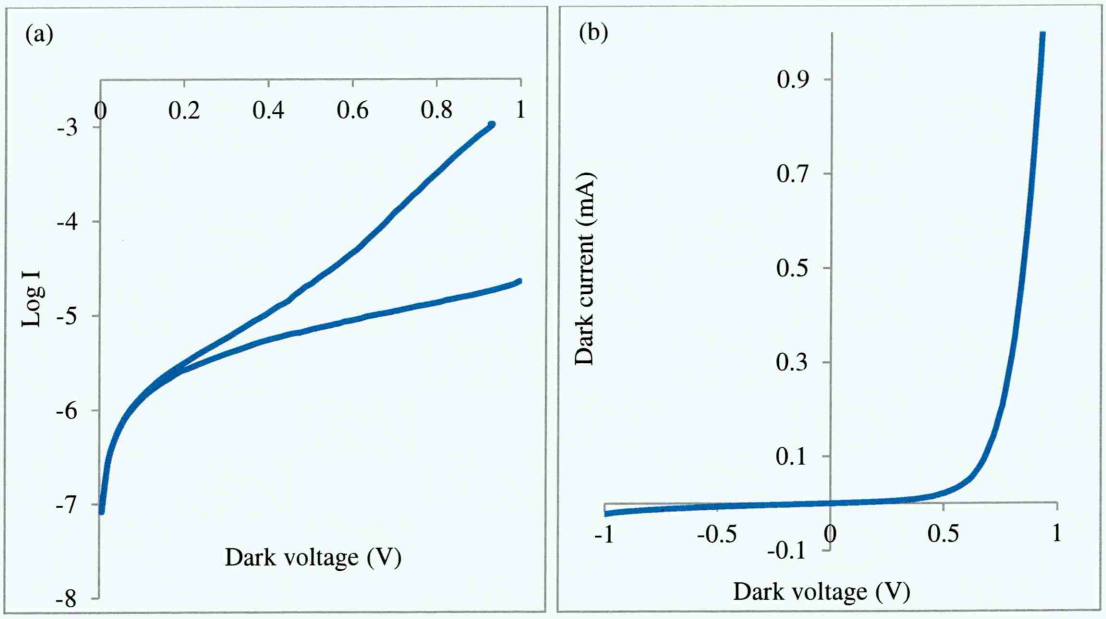


Figure 8.14: I-V characteristics of glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au under dark condition (a) Log-linear and (b) Linear-linear plots.

In furtherance to this investigation, the next discussion will be focused on experiments involving device structure and growth conditions with a reduced In_xSe_y buffer thickness to improve photocurrent without compromising the V_{oc}.

8.5.2 The effect of different surface treatments on the performance of glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells at different temperatures

As mentioned earlier, this experiment was carried out as a follow up to the previous experiment. The CdS and CdTe thicknesses remained ~200 nm and ~2500 nm respectively as in the previous experiment while the In_xSe_y buffer layer was thinned down to ~80 nm as compared to ~150 nm in the previous experiment. This is to improve the optical properties of the window layers thereby reducing window absorption at the front side of the device. This will help by improving optical transmission through the front layers so that most of the incident photons can reach the CdTe absorber for the creation of useful photocurrent with minimum optical and recombination losses. In an effort to enhance the CdS/CdTe solar cells photocurrent, some researchers suggests the reduction of the CdS window layer to the minimum possible value [45,46] while others [47,48] use ~(70-100) nm thick CdS to allow

maximum transmission of the incident photons through the window layers with minimum optical losses. However, thinning down the CdS window layer can impact negatively on the V_{oc} and FF of the device [14] as earlier explained.

In addition to the CC and CF surface treatments used in the previous experiment, cadmium chloride ($CdCl_2$) +gallium chloride ($GaCl_3$), (CG) was also used as one of the chemical treatment for this device. The CG was prepared from 1g of $Ga(SO_4)_3$, 2.5 ml of HCl acid and 50 ml of saturated CC solution. The introduction of CG treatment followed an earlier report by Fernandez [49] when Ga is used, it remove Te precipitates in single crystal CdTe. The annealing temperature used for the glass/n-In_xSe_y/n-CdS/n-CdTe/Au remained at 400°C to avoid layer deterioration or creation of excessive pinholes when heat-treated at 450°C as observed in section 8.5.1.

Table 8.6 shows the summary of measured device parameters under AM1.5 illumination conditions for the best 3 cells from each heat treatment condition while Figure 8.13 illustrates the J-V curves of the best cell obtained for each of the treatment. A drastic improvement in all device parameters of V_{oc}, J_{sc}, FF and the conversion efficiency, η was recorded in these devices especially in the CC and CF treated samples. However, the sample treated with CG show comparatively low solar conversion parameters. The highest efficiency recorded in the CC sample is 7.8% with V_{oc}=580 mV, J_{sc}=29.2 $mAcm^{-2}$ and FF= 0.46. The cell with the highest efficiency in the CF shows ~10% with V_{oc}, J_{sc} and FF of 640 mV, 38.1 $mAcm^{-2}$ and 0.41 respectively. For the CG treated sample, the recorded highest efficiency was 3.1% with V_{oc}=400 mV, J_{sc}=21.6 $mAcm^{-2}$ and FF=0.36. The highest efficiency in this experiment was recorded in cells annealed with CF.

Table 8-6: Summary of device parameters measured under AM1.5 illumination conditions for glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells.

Device ID	HT at 400°C with CC			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
S70-1D1	580	33.6	0.36	7.0
S70-1D2	560	32.3	0.42	7.6
S70-1D3	580	29.2	0.46	7.8
Average	**573**	**31.7**	**0.41**	**7.5**
Device ID	HT at 400°C with CF			
S70-2D1	650	30.5	0.44	8.7
S70-2D2	630	34.4	0.43	9.3
S70-2D3	640	38.1	0.41	10.0
Average	**640**	**34.3**	**0.43**	**9.3**
Device ID	HT at 400°C with CG			
S70-3D1	320	25.3	0.30	2.4
S70-3D2	400	21.6	0.36	3.1
S70-3D3	520	14.9	0.39	3.0
Average	**413**	**20.6**	**0.35**	**2.8**

The general improvement in the V_{oc} values in the CC and CF most especially in the CF is possibly due to defect passivation, creation of high potential barrier height at the n-CdTe/Au interface due to defects passivation and reduced recombination at both the In_xSe_y/CdS and at the CdS/CdTe interfaces. This situation provided the desired band bending in the device coupled with healthy depletion region with strong electric field that will separate the photo-generated charge carriers to their respective electrical contacts with minimum recombination losses. Another advantage of this graded-bandgap device is the possible contribution from impurity PV effect utilising the surrounding IR and impact ionisation in these devices. The contributions from these two processes could be responsible for the high J_{sc} values in these devices.

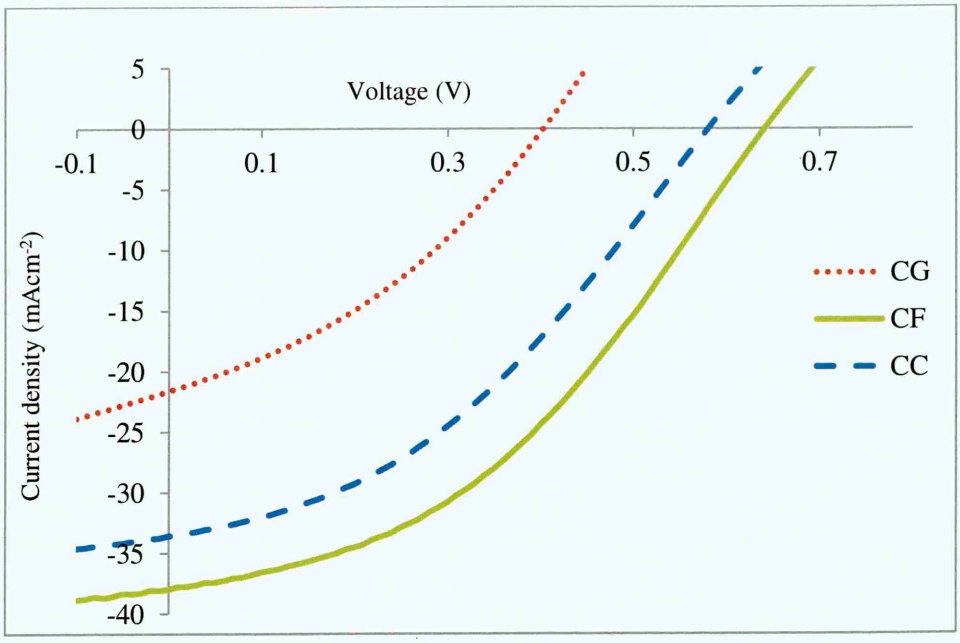


Figure 8-13: Typical J-V curves under AM1.5 illumination for the best 3 cells treated with different surface treatments in this experiment.

The possible absorption of photons from all the wavelength regions of the solar spectrum has dramatically improved the device J_{sc} values which contributed significantly to the overall efficiencies achieved in these devices. The obtained results from these series of experiments performed revealed a very interesting trend. The results presented are consistent with the previous trends which showed that the device heat-treated in the presence of CF at each stage of the experiment show higher solar to electricity conversion parameters. The annealing temperature of 400°C has been shown to be the best annealing temperature in this research.

As shown earlier, the highest efficiency of 10% (cell A) achieved in this research programme show device parameters with V_{oc} =0.64 V, J_{sc} =38.1 mAcm^{-2} and FF =0.41. However, a record efficiency solar cell of 21.4% (cell B) produced by First Solar and discussed in section 2.3.1 show V_{oc} =0.876 V, J_{sc} =30.3 mAcm^{-2} and FF =0.79. Comparing the parameters of these two cells show that cell A requires drastic improvement in both the V_{oc} and FF values for it to enter into category of the high efficiency cells. But the J_{sc} value observed in cell A is higher than that observed for cell B which could possibly be due to the difference in the device structure. Cell A is based on n-CdS/n-CdTe plus Schottky barrier while cell B is based on the n-CdS/p-CdTe. The reason for the high value of J_{sc} observed in cell A will be discussed later in this chapter.

The high V_{oc} and FF generally observed in the high efficiency cells presented in Table 2.1 could be due to low R_s and high R_{sh} in these devices. The low R_s values in solar cells are usually attributed to low resistance in the bulk of the semiconductor materials and the contact electrodes. This could be due to the high temperature processing (~600°C) [13] involved in the fabrication of these devices since most of them utilised closed space sublimation method of material growth. The Low values of R_s will improve both V_{oc} and FF of the cells [50]. The high FF values recorded in these cells indicate high R_{sh} lead (shunting paths) within the devices which will positively affect the efficiency of the solar cells [51]. Another reason for the generally high efficiencies recorded in these cells could be associated with the high purity of 5N (99.999%) starting material used in the fabrication of these high efficiency cells which was shown to be effective in reducing bulk recombination in solar cell devices [52].

It is therefore, necessary that the R_s values in cell A devices be reduced to lowest possible values and to maximise the R_{sh} to the highest possible values for achieving higher efficiency solar cells. The use of low resistance and high transmittance front contacts (e.g. Cd_2SnO_4) will help in reducing both the R_s and pinholes formation in the devices [14]. This will further improve the solar cell device efficiencies.

8.6 Characterisation of glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au solar cell under dark condition

The current-voltage characteristics of the three best diodes of the previous experiments treated in CC, CF and CG were measured under dark condition at room temperature to determine their diode parameters. Figure 8.14 shows dark I-V curves for the best 3 devices discussed under section 1.5.2 plotted using log-linear I-V and linear-linear I-V from which important diode parameters of the three cells were extracted. The parameters obtained from log-linear I-V include rectification factor (*RF*), ideality factor (n), reverse saturation current (I_o) and barrier height (ϕ_b). The information extracted from these parameters indicates the quality of the depletion region and the current transport mechanisms in the device. The *RF* values were obtained by dividing the forward current by the reverse current at the high bias voltage of 1.0 V. The n values were calculated from equation 3.15 using the obtained highest gradient of the forward bias of the log-linear I-V curve.

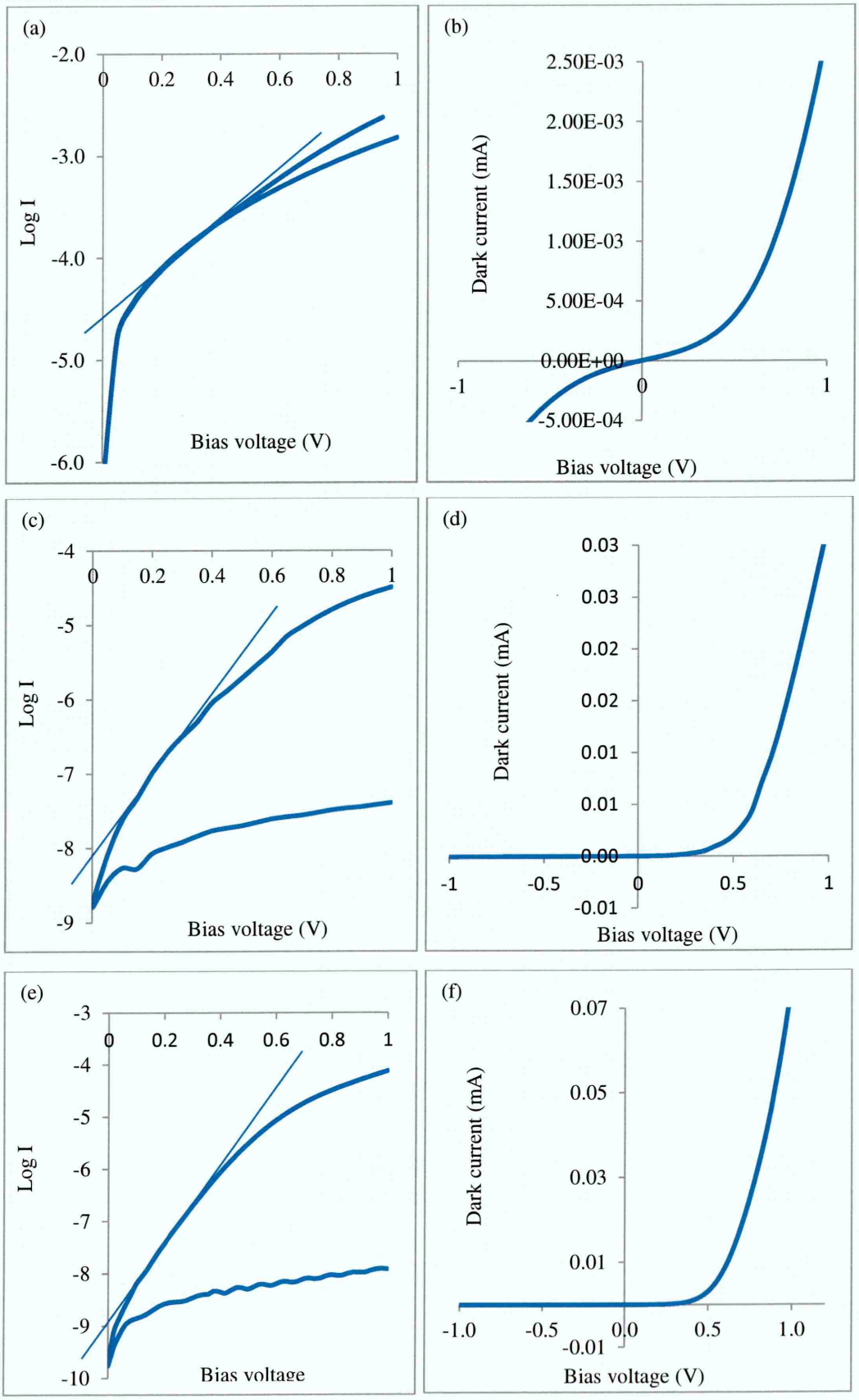


Figure 8-14: Dark I-V curves for the best 3 cells plotted using (a,c,e) log-linear and (b,d,f) linear-linear scales for (a,b) CG, (c,d) CC and (e,f) CF- treated devices (all annealing was carried out at 400°C for 20 minutes in air).

The I_o is the intercept obtained on log I axis when the straight line portion of the log I-V curve is extrapolated to meet the current axis at V=0, as illustrated in Figure 8.14(a). The obtained parameters from dark J-V and light J-V curves for the three cells are summarised in Table 8.7.

The *RF* values for the cells were calculated using equation 3.14 and were found to be in the range ($10^{0.2}$-$10^{4.0}$) as shown in Table 8.7. The highest efficiency solar cell achieved in this research has *RF* of $10^{4.0}$, n=2.00, I_o=1.3×10^{-9} A and ϕ_b>0.81 eV. It has been reported that *RF* of $10^{3.0}$ is enough requirement for efficient solar cells [50]. The ideality factor, n gives information on the type of current transport mechanisms within the diode. An ideal diode should have an n value nearly equal to unity but practical diodes usually show values of n in excess of 1 due to non-ideality introduced when the depletion region and the interface are dominated by recombination and generation (R&G) centres [50].

The obtained value of n =2 indicates recombination process at the interface region [50,53]. The I_o values obtained for the cells with sample ID S70-ID and S70-2D are in the range (1.3-2.0)×10^{-9} A, while solar cell with sample ID S70-3D has large I_o value of 2.0×10^{-5} A. It is also observed that the highest efficiency cell shows the lowest I_o value of 1.3×10^{-9} A. The I_o values were used to calculate the barrier heights of the solar cells.

Table 8-7: Summary of solar cell parameters measured under dark and AM1.5 illumination conditions for the 3 best cells observed in this work. All samples were heat treated in the presence of CG (S70-3D), CC (S70-1D) and CF (S70-2D) at 400°C for 20 minutes in air.

Device ID	Dark I-V					
	RF	n	I_o (A)			ϕ_b (eV)
S70-3D (CG)	$10^{0.2}$	5.96	2.0×10^{-5}			----
S70-1D (CC)	$10^{3.0}$	1.51	2.0×10^{-9}			>0.74
S70-2D (CF)	$10^{4.0}$	2.00	1.3×10^{-9}			>0.81
	AM 1.5 illumination					
Device ID	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	R_s (Ω)	R_{sh} (Ω)
S70-3D (CG)	520	14.9	0.39	3.0	320	1385
S70-1D (CC)	580	29.2	0.46	7.8	309	3538
S70-2D (CF)	640	38.1	0.41	10	309	4549

The calculated barrier heights in these devices are in the range >(0.74-0.81) eV and the largest barrier of >0.81 eV was recorded for the highest efficiency cell. For high efficiency solar cells, the I_o should be kept as low as possible so as to achieve a healthy junction with reduced recombination losses. Large values of I_o is usually attributed to presence of recombination centres which are known to reduce charge carrier lifetime [54].

The barrier height, ϕ_b >0.81 eV recorded for the highest efficiency cell suggest that the Fermi level pins close to the valence band maximum. The large n values recorded in these devices indicate that the ϕ_b values are underestimated. The barrier obtained and possible incorporation of impurity PV effect and impact ionisation in this cell could have been the reason for the high J_{sc} value observed.

The estimated values of R_s and R_{sh} from the light J-V curve (Figure 8.13) are in the range (309-320) Ω and (1385-4549) Ω respectively. An ideal diode should have R_s=0 and $R_{sh}\rightarrow \infty$ values [50]. Low values of R_s indicate low resistance of the bulk materials and electrical contacts of the device while high R_{sh} values show a reduced leakage path in the cell. Minimum values of R_s and infinite R_{sh} will improve the V_{oc}, J_{sc}, FF and the overall conversion efficiency of the device.

8.7 C-V measurements of glass/n-In_xSe_y/n-CdS/n-CdTe/Au solar cells under dark condition

Capacitance-voltage (C-V) relationships are developed to explain metal/semiconductor interfaces not affected by high level of defects and intermediate insulating layers. Use of these measurements should also have extreme care when applied to multi-layer electronic devices. However, C-V measurements were carried out in order to extract some ideas on doping concentrations of devices under development. C-V technique was employed to estimate the doping concentration of the 3 best n-n-n+Schottky diodes presented in Figure 8.7 of the previous section. Dark capacitance-voltage (C-V) and Mott-Schottky ($1/C^2$ vs. V) plots at room temperature (300 K) using a high frequency 1 MHz detection signal at bias voltage range of (-1.0 to +1.0) V were conducted on the high efficiency 10% cell obtained in this research. Figures 8.15(a) and 8.15(b) are respectively the C-V characteristics and the $1/C^2$ vs. V plot of the 10% solar cell with device structure glass/n-In_xSe_y/n-CdS/n-CdTe/Au.

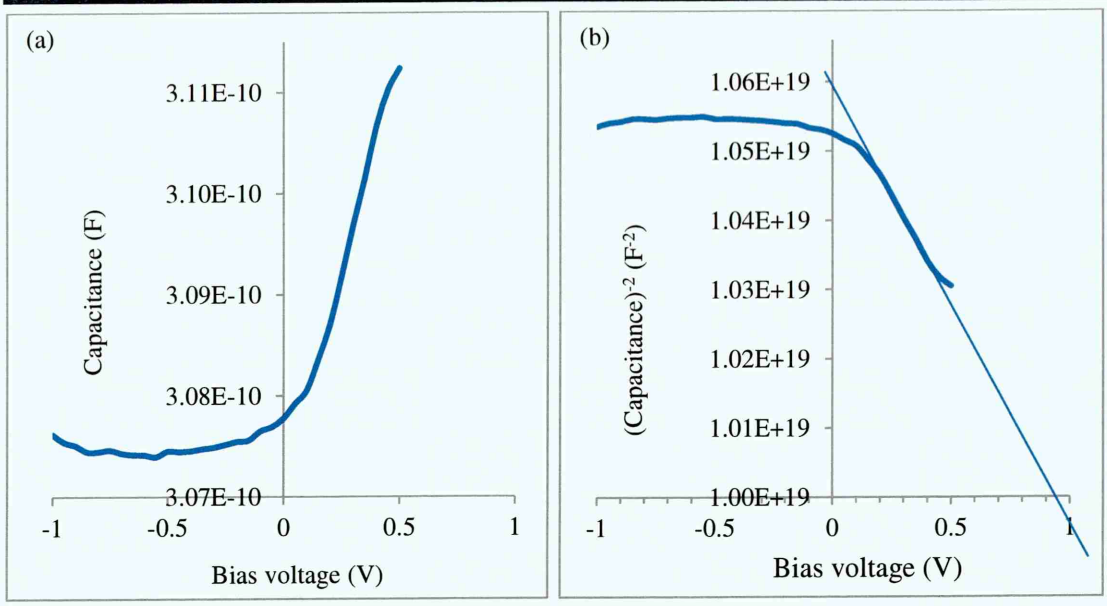


Figure 8-15: The plots of dark (a) C vs. V and (b) $1/C^2$ vs. V of glass/n-In_xSe_y/n-CdS/n-CdTe/Au 10% efficiency solar cell device.

Results from Figure 8.15(a) shows a fairly constant depletion capacitance at reverse bias but starts to increase near the zero bias into the forward bias showing a decrease in the depletion width, *W*. The depletion capacitance at zero bias (C_o) for the 10% solar cell was 308 pF as obtained from the C-V plot. The geometrical capacitance is normally estimated at zero bias (V=0) using equation 8.4.

$$W_o = \frac{\varepsilon_o \varepsilon_r A}{C_o} \qquad 8.4$$

Where W_o is the depletion width at zero bias, ε_o =~8.85×10^{-12} Fm^{-1} is the permittivity of free space, ε_r ~ 11 is the relative permittivity of CdTe, A ~0.031 cm^2 is the device active area and C_o is the junction capacitance at zero bias. As shown in the Mott-Schottky plot (Figure 8.15(b)), a steady drop of C^{-2} is observed in the forward region as the bias voltage increases. In efficient solar cells, it is possible that the depletion width is almost equal to the device thickness; then the device is said to be fully depleted. In such devices, there exists an active depletion region throughout the device. In such a situation the electron-hole (e-h) pairs created are swiftly separated and collected at their respective electrodes with minimum recombination. The relevant device parameters extracted from Figures 8.15(a) and 8.15(b) include; depletion capacitance (C_o=380 pF), depletion width (W_o=993 nm) and doping concentration (N_D-N_A=2.07×10^{16} cm^{-3}).

Similar doping concentration and depletion widths were also reported by refs [55,56]. Mahabaduge *et al.*[57] reported a CdTe-based solar cell of 14% efficiency with depletion width and doping concentration of 1250 nm and 4.30×10^{14} cm^{-3} respectively.

8.8 Fabrication of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au multi-layer graded bandgap solar cell devices

Figure 8.16 shows the band diagram of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au multi-layer graded bandgap devices. This experiment was carried out to study the effect of different annealing condition on glass/FTO/n-ZnS/n-CdS/n-CdTe/Au structure. The incorporation of ZnS as the buffer layer is to mainly grade the device and to allow the transmittance of high energy photons into the solar cells. In the present device, the bandgaps of the buffer (ZnS), window (CdS) and the absorber (CdTe) are ~3.70, 2.42 and 1.45 eV respectively. The wider bandgap ZnS (3.70 eV) was made the buffer layer and the narrow bandgap CdTe (1.45 eV) was the absorber while CdS (2.42 eV) served as the intermediate layer between the ZnS buffer and the CdTe absorber layers.

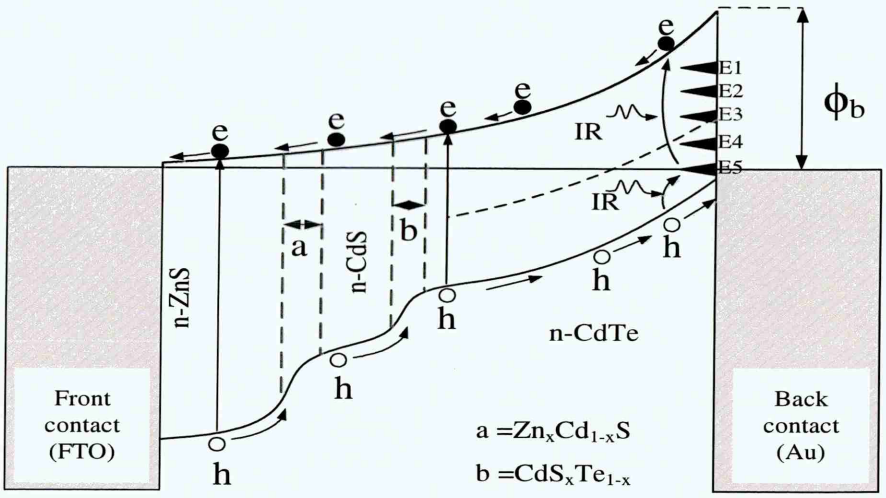


Figure 8-16: The energy band diagram of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au multi-layer graded bandgap solar cell device [Diagram not to scale].

The lattice mismatch at the ZnS/CdS and CdS/CdTe interfaces are ~6% [58] and ~10% [10] respectively. During annealing process, there is possible intermixing at the various junctions in the device. The regions labelled "a" and "b" in Figure 8.16 represent the alloys of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} formed during annealing at the ZnS/CdS and CdS/CdTe interfaces respectively. The benefits of these alloys are to remove the abrupt nature of the junctions and help in gradual transition at the interface and reducing

interface recombination centres. Processes like impurity PV effect and impact ionisation can also combine to significantly improve the device performance if well optimised.

The experiment was carried out by electroplating ~100 nm thick of n-ZnS layer on glass/FTO substrate. The layer was then annealed at 300°C for 10 minutes in air. Then a CdS layer of ~100 nm thick was then deposited on the glass/FTO/n-ZnS substrate, rinsed in de-ionised water and dried in air. The sample was then annealed in the presence of CC at 400°C for 20 minutes in air and allowed to cool down slowly. The sample was then rinsed in de-ionised water to remove the CC residue on the CdS surface. Afterwards, n-CdTe layer of ~1600 nm thick was electroplated on the CdS to form glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structure. After growth, the sample stack was rinsed in de-ionised water, dried in air and was cut into 4 parts. The first part was annealed in air only with no surface treatments, the second, third and fourth parts were treated in the presence of CC, CF and ammonium chloride (AC) respectively. All samples were annealed at 400°C for 20 minutes in air. Afterwards, the samples were then rinsed, dried, etched and completed by evaporating ~100 nm Au metal contacts on the etched CdTe surfaces.

The summary of device parameters for the best 3 cells for each annealing condition are given in Table 8.8 and Figure 8.17 depicts the J-V curves for the best 4 cells one from each surface treatment.

It is observed that irrespective of the surface treatment, all devices show similar V_{oc} and FF values while J_{sc} of cells treated in CC and CF show relatively higher values than those treated in AC. The observed efficiency values were in the range (1.2-3.3)%. The comparatively highest efficiency of 3.3% was observed in sample treated in the presence of CF. One of the reasons for the poor performance in these devices is the high series resistance (R_s) and low shunt resistance (R_{sh}) as observed in the J-V curves presented in Figure 8.15. Reasons such as incomplete defect passivation at the device junctions will lead to the formation of active recombination centres which kill the photo-generated charge carriers impacting negatively on the J_{sc} and other device parameters. The low R_{sh} in the devices with respect to the J-V curves suggests the possible formation of pinholes or low resistive path in these devices which can directly affect the V_{oc} and FF of the solar cells.

Table 8-8: Summary of device results for glass/FTO/n-ZnS/n-CdS/n-CdTe/Au for different post growth annealing conditions, measured under AM1.5 illuminated conditions.

Device ID	HT at 400°C in air			
	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
HTD1	389	12.3	0.33	1.6
HTD2	410	14.9	0.33	2.0
HTD3	434	14.2	0.34	2.1
Average	**411**	**13.8**	**0.33**	**1.9**
Device ID	HT at 400°C with CC			
CCD1	483	17.9	0.31	2.7
CCD2	474	19.5	0.30	2.8
CCD3	439	23.0	0.29	2.9
Average	**465**	**20.1**	**0.30**	**2.8**
Device ID	HT at 400°C with CF			
CFD1	403	23.1	0.32	3.0
CFD2	440	24.0	0.31	3.2
CFD3	445	21.9	0.34	3.3
Average	**429**	**23.0**	**0.32**	**3.2**
Device ID	HT at 400°C with AC			
ACD1	446	9.4	0.29	1.2
ACD2	407	11.3	0.30	1.4
ACD3	404	14.7	0.31	1.8
Average	**419**	**35.4**	**0.30**	**1.5**

In a similar device structure, Oladeji *et al* [59] used $Cd_{1-x}Zn_xS$/CdS/CdTe device structure to achieve conversion efficiency of 10%. This device utilised CSS deposited CdTe. However, Echendu *et al* [37] achieved ~10.4% efficiency using low cost all electroplated layers with ZnS/CdS/CdTe device structure. The use of materials such as

Zinc oxide (ZnO) [60], Alumimium zinc oxide (Al-ZnO) [61], Indium sulphide (In_2S_3) [62], tin oxide (SnO) [63], zinc stannate (ZTO) [14] as buffer layers are available in the literature.

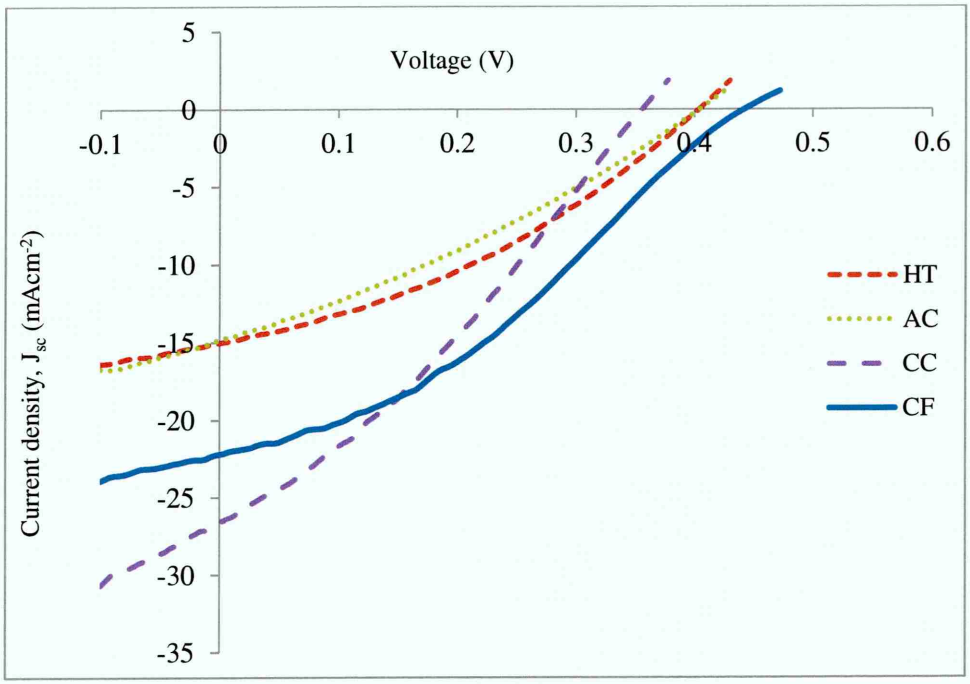


Figure 8-17: Typical J-V plots of the four best cells, one from each set of heat treatment condition.

8.9 Possible reasons for the observed high short-circuit current density (J_{sc}) values

Some devices reported in this thesis show high J_{sc} values which are outside the theoretically calculated and reported highest achievable J_{sc} for a single p-n junction. In solar cell fabrication process, the choice of materials with appropriate energy bandgap (E_g) in the design of devices is critical for high performance solar cells. This is even more important in the design of multi-layer graded bandgap devices for effective charge carrier collection and separation.

The maximum short-circuit current density (J_{sc}) theoretically calculated for a single junction CdTe device was based on the assumption that every photon with energy greater than E_g creates only one electron-hole pair in the solar cell and all photons with energy less than the bandgap are considered to not contribute to the creation of e-h pairs. Another assumption is that the electrons are transported to the external circuit with no losses in the device. In this device (p-n junction), the highest achievable J_{sc} value was calculated to be ~27.0 mAcm^{-2} based on the bandgap of 1.45 eV of CdTe

[64]. A detailed work on the estimation of efficiency parameters of some of the most common PV semiconductors (InP, GaAs and CdTe) was reported by Loferski in 1956 [65]. In this report, the computation on the number of photons that can be absorbed by a semiconductor material as a function of their energy gap was provided. The approximate current density of any semiconductor depends on the number of photons converted to useful energy. The number of photons as a function of energy band gap, n_{Ph} (E_g) were calculated by counting the number of photons whose energy exceeds the energy gap (E_g) of the semiconductor material, using the solar spectrum and is given in the formula below:

$$n_{ph}(E_g) = \sum_{v=E_g/h}^{v=v_{max}} n_{ph}(v) \qquad 8.5$$

Where $n_{ph}(v)$ is the number of photons with energy hv in the intervals $\Delta(1/\lambda)= 10^{-5}$ cm^{-1} and v_{max} is the maximum frequency in the solar spectrum [65].

In this thesis, a J_{sc} value of 38.1 $mAcm^{-2}$ was reported which is higher than the calculated maximum value for a single p-n junction solar cell. The observation of very large short circuit current density for CdTe-based devices have been reported by Dharmadasa *et al.* [1], Chaure *et al.* [66] and Echendu *et al.* [29]. All these devices were fabricated from n-CdS and n-CdTe which formed the structure of n-n plus Schottky barrier at the metal/semiconductor interface. This indicates that, there are some mechanisms which are responsible for this observed high J_{sc} values.

Figure 8.9 is a typical solar cell structure producing large current values. In this device, electron-hole pairs can be created throughout the solar cell structure due to the existence of electric field across the entire device structure. In p-n junction devices, if photoexcitation of e-h pairs occurs outside the depletion region, there exists high probability for these photo-generated charge carriers to recombine due to the absence of electric field in these regions. The present device utilised two important built-in processes of impurity PV (*IPV*) effect and impact ionisation that are possibly responsible for the observed high J_{sc} values. The evidence of collection due to *IPV* was observed using responsivity technique in a similar graded bandgap device structure reported by Dharmadasa *et al.* [67].

Solar cell is usually surrounded by heat energy and infra-red (*IR*) photons which help in the creation of e-h pairs utilising the defects distribution at the rear of the device. These

IR photons are low energy photons which cannot directly create band-to-band excitation but can promote the electrons from the valence band to some defect levels within the bandgap. Since the left behind hole is very close to the back contact, it can easily be collected at the external circuit due to the electric field in the device without allowing room for recombination. While the electron is in suspense at some defect level, another low energy *IR* can promote it to the conduction band. In this way, two low energy *IR* photons can produce one electron-hole pair. This process is called impurity PV effect. The incorporation of *IPV* was observed and reported by Dharmadasa *et al.* in 2011 [64].

The other contributing mechanism to the high J_{sc} values is the impact ionisation. When a low energy *IR* photon promote an electron from the valence band to some defect levels within the bandgap, while the electron is suspended at one of the defect levels, it can be knocked off to the conduction band by an accelerating electron from the steep slope of the potential barrier of the device structure. This electron is swept to the back contact of the device for creation of useful electricity. This mechanism is called impact ionisation. These two mechanisms can reduce significantly the effect of thermalisation and contribute to the large J_{sc} values observed. However, it is important to also mention that these explanations are only valid for optimised solar cell devices otherwise low output electronic parameters are observed.

8.10 Conclusions

Using 2E system, different device structures based on n-CdS/n-CdTe solar cells have been fabricated and assessed. In_xSe_y/CdTe/Au solar cell structures were fabricated but the results showed poor performance and need further experimentation to test whether higher efficiency values can be obtained. Buffer layers of In_xSe_y and ZnS were incorporated in n-CdS/n-CdTe to fabricate multi-layer graded bandgap devices. The highest conversion efficiency of 10% devices was achieved using In_xSe_y buffer layer with glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au multi-layer graded bandgap structures treated in the presence of CF annealed at 400°C for 20 minutes in air. This efficiency was recorded after thinning down the In_xSe_y buffer from ~150 nm to ~80 nm thick. This study has also proved the possibility of incorporation of In_xSe_y films in CdTe-based solar cell devices and achieving 10% efficiency for the first time.

The incorporation of ZnS buffer in glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures show low conversion efficiencies during this work, although other researchers in this group achieved efficiencies above 10%. Based on the experimental evidence

observed in this research, treatment with CF has shown to produce best solar cell devices in all experiments carried out in this research programme. Results showed that both surface treatments and low buffer layer thickness ~(80-100) nm are necessary for high performance solar cells. The doping concentration of the highest efficiency as calculated from the dark Mott- Schottky plot gave a moderate doping density of 2.07×10^{16} cm^{-3}.

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Chapter 9: Conclusions and future work

9.1 Conclusions

Presented in this thesis was the processing of four different semiconductor materials (In_xSe_y, ZnS, CdS and CdTe) in order to develop low-cost and efficient solar cell devices using CdTe as the absorber material. These layers were grown using electroplating from aqueous electrolytes using a 2-electrode system on cathode surface. This research was able to achieve intrinsic n-type and p-type electrical conduction in ZnS and In_xSe_y semiconductor materials for the first time. The fabricated solar cell device structures were based on the n-CdS/n-CdTe plus Schottky contact type solar cell devices rather than the conventional p-n junction type devices.

The experimental results were presented in chapters 4 to 8. Chapters 4-7 presented results on the growth and characterisation of In_xSe_y, ZnS, CdS and CdTe semiconductor materials. In_xSe_y and ZnS were found to be amorphous in nature while CdS and CdTe were both polycrystalline. CdS was grown in both hexagonal and cubic phases while CdTe films showed a cubic crystal phase. The materials were characterised using varied analytical techniques in order to fully optimise the best range for the growth of electronic quality layers. The effects of surface treatment on the CdTe absorber layers using CC and CF at different annealing temperatures of 380°C, 420°C and 450°C were investigated. Results show that larger grains were obtained in both treatments. It was also observed that the achievement of the larger grains depends mainly on the annealing temperature.

Chapter 8 discussed the fabrication, development and assessment of n-n-n plus Schottky barrier type solar cell devices. The photovoltaic properties of the devices were activated using different chemical treatments but two chemical treatments of CC and CF stand out to be the best. The highest efficiency cell obtained in the CC treated devices is 7.8% with parameters of V_{oc}, J_{sc} and FF of 580 mV, 29.2 $mAcm^{-2}$ and 0.46 respectively. While the highest efficiency cell of ~10% was achieved in CF treated devices with parameters of V_{oc}, J_{sc} and FF of 640 mV, 38.1 $mAcm^{-2}$ and 0.41 respectively. The highest cell efficiency achieved in this research program is ~10%. However, the overall highest solar cell parameters obtained in this research are V_{oc}=650 mV, J_{sc}=38.1 which are found in layers treated in CF while the highest, FF=0.46 was obtained in layers

annealed in the presence of CC. These parameters were obtained in a multi-layer graded bandgap with glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au device structure. The most challenging aspect of this research work is the reproducibility of the highest efficiency devices, as a result of the low FF recorded in the devices. As shown in Table 8.6, the main difference between the devices activated using the conventional CC and the improved CF is the V_{oc} values which are higher in the case of CF than in the CC treated layers. This was attributed to improved passivation of the surface states at the back contact interface. It is also observed that the reduction in the In_xSe_y buffer layer from 80-150 nm has played a prominent role in the enhancement of all device parameters. The 400°C annealing was found suitable for obtaining efficient devices in this thesis as compared to devices annealed at other temperatures. This is because annealing at 450°C produced poor devices characterised by high density of pinholes.

9.2 Future work

Based on the experimental work presented in this thesis, a number of suggestions for future work will be helpful in order to further improve the solar cell efficiencies using the low-cost electroplating technique. Since the efficiency of a solar cell depends on the V_{oc}, J_{sc} and FF, and with respect to the parameters achieved in this research, there is still room for significant improvement in the performance of these devices especially in the V_{oc} and the FF.

9.2.1 Purity of starting materials

To develop low-cost energy, the source materials and the solar cell processing should be as cheap as possible. The purity of starting materials is very important not only in the electroplating technique but also in the high temperature growth techniques alike. The purity of the starting materials as reported in this thesis were in the range 98-99.999% and were the main focus of developing low-cost CdS/CdTe thin film solar cell devices. The high purity chemicals of say ≥5N (99.999%) are very costly which when used will ultimately effect the cost of the solar panels. However, it is also very important to mention here that the efficiency of solar cells also depends on the careful optimisation of growth and post growth processing parameters. When the growth and post growth processing of materials are fully optimised, high efficiency solar cell devices can be achieved.

This group has recently published 15.3% efficient solar cell based on multi-layer graded bandgap solar cell devices. Though, the use of high purity starting material is desirable for the manufacture of high efficiency solar cells, since it helps in the reduction of bulk recombination, the efficiency of solar cell is equally dependent on other important parameters such as annealing condition, etching process and the doping concentration.

9.2.2 CdTe electrolyte replenishment using Cd^{2+} and $HTeO_2^+$

The quality of electroplated layers depends on the stoichiometry of the deposited layers which depends on a number of growth conditions. The stoichiometry of the layers depends on parameters such as concentration of Cd and Te ions in the bath, growth voltage, growth temperature, stirring rate and the pH of the electrolyte. Since during the deposition process, the constituent ions of Cd and Te are depleted in the deposition electrolyte. It is for this reason that effective and reliable method of replenishing of the electrolyte with these ions is of paramount importance so that continued growth of high quality layers are ensured. Therefore, it is advisable that during material optimisation process, all other deposition parameters be fixed so that only Cd and Te ion concentrations in the electrolyte will be dealt with. Under this condition it is easy to pin point based on the experience accumulated during this research programme whether the electrolyte is Cd or Te deficient. This is done by monitoring the deposition current and visual appearance of the deposited layers.

Deposition of stoichiometric CdTe requires high concentration or sea of Cd ions while the concentration of Te ions is kept much lower than that of the Cd concentration. This is due to the large difference in the reduction potential, (E^0) values of the constituent species of Cd (E^0=-0.403 V) and Te (E^0=+0.593 V). Therefore, the deposition of CdTe depends on the Te ions concentration and not on Cd ions concentration. One of the challenges encountered in the course of this research is the effective and reliable means of Te ions addition into the electrolyte. For this purpose, 2.0 g of TeO_2 powder (purity =99.999%) was dissolved in 230 ml of de-ionised water and sulphuric acid kept for the purpose of replenishing Te ions concentration in the electrolyte.

The deposition current density for the deposition of near stoichiometric CdTe is usually between 150 to 200 μAcm^{-2}. If the deposition current density is dropped to around 130 μAcm^{-2}, it indicates a low level of Te ions in the electrolyte, Therefore, 2-3 ml of TeO_2 dilute aqueous solution is added to replenish the Te ions concentration in the electrolyte.

The present method of Te addition in the electrolyte needs to be improved and suggestion for future work is the use of automated method of Te addition using a pumping system that will maintain constant and low level of Te ions in the electrolyte. Another simple method worth trying in the future will be the use of a Te anode for continues injection of Te ions into the deposition electrolyte.

9.2.3 Front contact

The efficiency of solar cells can be affected by the optoelectronic properties of the transparent conducting oxide (TCO) front contact. For instance, if TCO with high resistance (R_s) is used, it will reduce the J_{sc} and the FF which will in turn affect device efficiency. The efficiency of solar cells can be improved by substituting the FTO front contact used in this research with a lower resistivity and higher transmittance front contact. Novel in this category are cadmium tin oxide (CTO or Cd_2SnO_4) with resistivity of 1.28×10^{-4} and transmittance of around 90%.

9.3 Multi-layer Graded bandgap device structures

The effective way to absorb photons from all wavelengths from the solar spectrum is by the use of multi-layer graded bandgap devices similar to the designed by Dharmadasa in 2005. Graded bandgap utilising layers from different materials with different bandgap as presented in chapter 2 and 8 have been the main focus at present to increase the efficiency of solar cell devices. Further optimisation of the growth and post growth device processing of the four semiconducting materials reported in this thesis will significantly enhance photovoltaic parameters of these devices.