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*Design optimization and evaluation of integrating sound level meters.*

HOLDING, John Michael.

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DESIGN OPTIMIZATION AND EVALUATION OF  
INTEGRATING SOUND LEVEL METERS

by

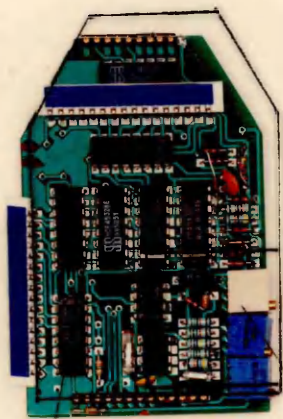
JOHN MICHAEL HOLDING BSc ARCS

A thesis submitted to the Council for National Academic Awards in partial fulfilment of the requirements for the degree of Doctor of Philosophy.

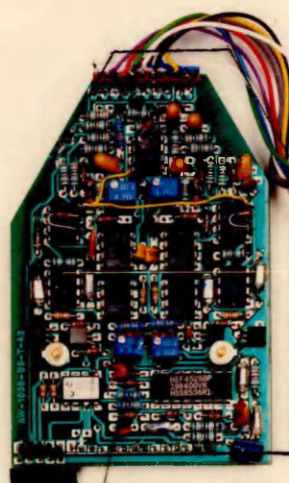
Sponsoring Establishment: Department of Mechanical and  
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Sheffield City Polytechnic

Collaborating Establishment: Cirrus Research Ltd

July 1987



Log Converter



Dual Integrator

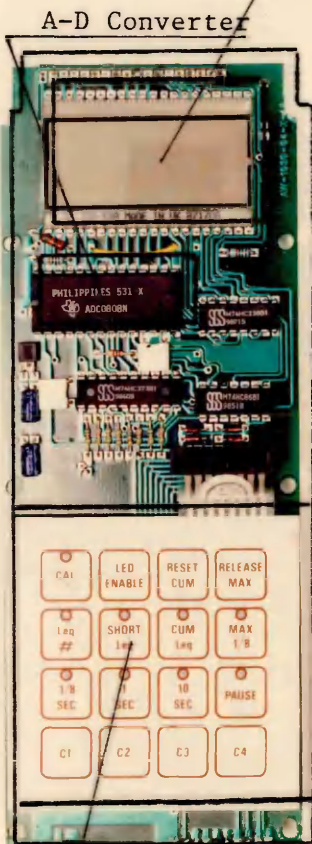


Input Amplifier and Weighting Network

Digital Storage & Ladder Logic

Program EPROM

Display (driver/below)

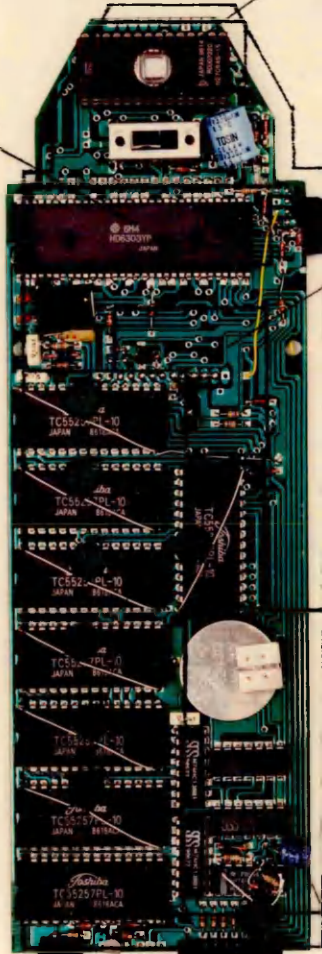


A-D Converter

CPU

RS 232 Driver

Keyboard



Storage RAM

Decoding & Backup Circuitry



Power Supply

ADVANCED MICROPROCESSOR-BASED INSTRUMENT PCBs

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## ABSTRACT

### Design Optimization and Evaluation of Integrating Sound Level Meters

J M Holding

Previous work has shown that the risk of hearing loss is related to the cumulative sound energy received by the ear. The instrument which computes a measure of this parameter is an integrating sound level meter (ISLM). Optimum design requirements for ISLMs which meet a variety of demanding specifications have been determined. Evaluation procedures have been proposed and the necessary specialized tone burst signal sources have been designed. An early survey of instruments which were available revealed serious shortcomings in their ability to integrate accurately a typical impulsive signal. The aim of this work was to determine and critically evaluate the limiting mechanism, and to subsequently investigate design strategies leading to high performance instruments. Techniques for extending the performance of several standard circuits have been developed. In addition, a novel method for storing data in analogue and digital form and subsequently recovering a continuous output has been developed and is fully described. Combinations of analogue, random logic and microprocessor-based techniques have been investigated. Complete instruments which utilize different combinations have been designed and evaluated. The optimum performance for an instrument which meets the highest specification is shown to be achieved by the use of analogue techniques for the majority of the signal processing, with a combination of random logic and microprocessor-based techniques for control and data storage.

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## CHAPTER ONE

### INTRODUCTION

An increasing awareness of the risk of hearing damage due to noise has encouraged research into the mechanism of hearing loss. It is now generally accepted that the degree of hearing impairment is a function of the duration of the exposure as well as the level.

The concept of an Equivalent Continuous Sound Level,  $L_{eq}$  was introduced in the 1950's after animal and human experiments showed that the same degree of hearing damage could be obtained by doubling the sound intensity and halving the sound exposure or vice versa. The concept of the equivalent continuous sound level is to impart the same amount of energy to the ear as the impulsive or varying sounds which actually occur, over a given time interval.

$L_{eq}$  is therefore defined as the mean-value of the sound intensity with respect to time, expressed in decibels:

$$L_{eq} = 10 \log_{10} \frac{1}{T} \int_0^T \frac{P^2(t)}{P_0^2} dt$$

where  $T$  is the measurement duration in seconds

$P$  is the instantaneous sound pressure in pascals

$P_0$  is the reference sound pressure having an r.m.s. value of  $2 \times 10^{-5}$  pascal

The unreferenced integral represents the energy content of the sound and is called the dose ( $\text{Dose} = \int_0^T P^2(t)dt$ ). This is usually expressed in  $(\text{pascal})^2$  hours.

The referenced integral can also be logged on its own and has the special name of sound exposure.

$$\text{Sound Exposure} = 10 \log_{10} \int_0^T \frac{P^2(t)}{P_0^2} dt$$

Sound Exposure (SE) can therefore be related simply to  $L_{eq}$ :

$$SE = L_{eq} + 10 \log_{10} T$$

It can be seen from this that sound exposure and  $L_{eq}$  are identical when the measurement duration is one second.

The principal advantage of an integrating sound level meter (ISLM) compared to a conventional sound level meter (SLM) is its ability to average stochastic sound signals of wide variance over long time periods. If the noise profile were to consist of several different, but constant, levels, the  $L_{eq}$  could be determined using a conventional SLM and stopwatch technique. However, noise sources such as are commonly found in industry, often contain impulsive or short bursts of high intensity sound. A practical ISLM must therefore be capable of integrating over a wide space of signal levels, and over a wide range of measurement periods.

The aim of this research was firstly to investigate and assess various techniques for the measurement of  $L_{eq}$  and thus to develop evaluation procedures and standards. Following this, an optimized design for an ISLM capable of accommodating the range of signals found in an industrial environment, was to be undertaken.

It was anticipated that the measurement techniques would initially capitalize on the analogue design experience of the collaborating body, and that the work would develop naturally through the use of hybrid techniques, to culminate in the design of a microprocessor-based digital instrument as the final phase of the PhD programme. The work was

undertaken following this initial plan, however the value and subsequent effect on instrument performance of the optimized analogue stages was significantly greater than originally appreciated.

## PHYSIOLOGICAL ACOUSTICS

In order to define and assess correctly the properties of an integrating sound level meter one must have some knowledge of the physiology of the hearing process and the mechanisms leading to hearing loss. A summary of basic anatomy and physical properties is followed by a description of normal and noise-induced hearing loss. Evidence from researchers performing experiments on animals together with a number of government reports is used to support the Equal Energy Hypothesis. This hypothesis forms the basic justification of the need for an integrating sound level meter.

## 2.1 Introduction

The constituent elements of the auditory system perform the translation from the pressure variations of the sounds reaching the ear into the nerve signals within the brain. The outer and middle ear amplify the air-borne pressure variations and couple them to the fluid of the inner ear.

The structures of the inner ear perform frequency analysis on these vibration signals and pass nerve impulses via the cochlear nerve fibres to the auditory receptive centres of the brain.

The construction of the ear is such that the internal background sources of noise are reasonably well rejected, allowing the ear to have a particularly high sensitivity to external sound signals.

## 2.2 Anatomy of the Ear

The acoustic pressure variations impinging on the outer ear or pinna (Figure 2.1) are scattered or focussed, depending upon wavelength, into the auditory canal or meatus. The meatus is a slightly tapered horn which helps match the impedance of the ear drum or tympanic membrane to the free field. A typical length for the meatus is 25 mm which accounts for the lightly damped resonance at about 3 kHz. The resonance produces an increase of up to 10 dB over a fairly broad range of frequencies centred around 3 kHz. This roughly corresponds with the important consonant sounds in human speech and is therefore of some benefit.

In ordinary conversation the displacement of the tympanic membrane is about  $10^{-10}$  m, ie the diameter of a hydrogen molecule. This displacement is amplified by three ossicles: the malleus, incus and stapes (Figure 2.1). The dimensions and physical arrangement of those bones is such that an increase in thrust by a factor of about 1.3 results. The stapes and associated ligaments form the oval window to the cochlea of the inner ear (Figure 2.1). As the area of the oval window is smaller than that of the tympanic membrane, the actual pressure at the foot of the stapes is further increased to about 25 dB above the received pressure level. This virtually compensates for the theoretical loss due to the transfer from air pressure to the fluid pressure of the inner ear.

Although the ossicles only provide a fairly modest increase in pressure, there are a number of advantages in this seemingly over-complex arrangement. Firstly, the asymmetrical arrangement of the malleus and incus contributes to the rejection of bone conducted signals, thus improving the basic system noise level. Secondly,

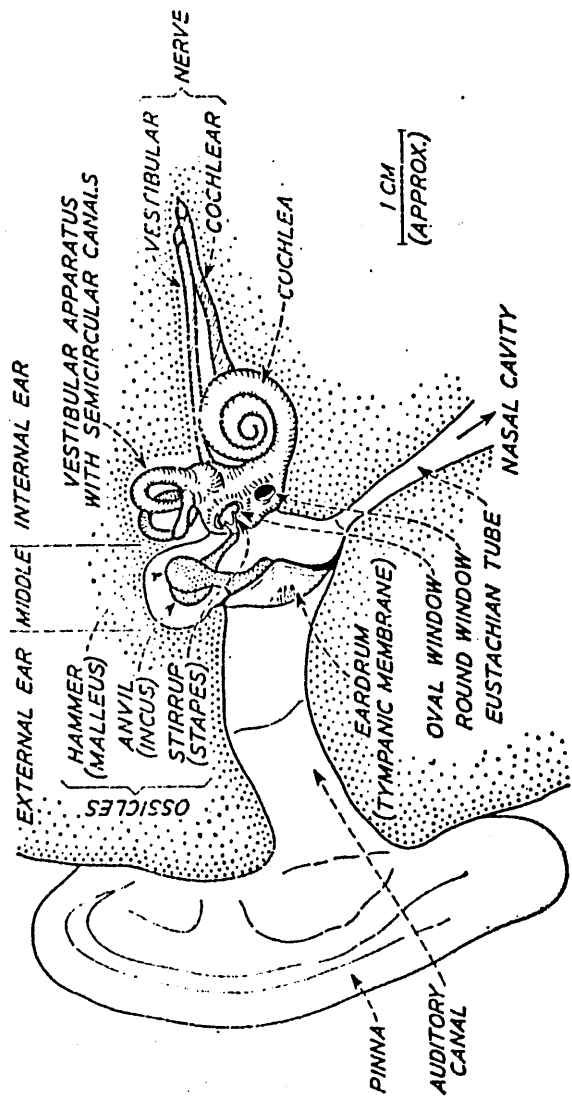


FIGURE 2.1 Anatomy of the Ear

the restriction of the bones to very small amplitude displacements, which is possible with this arrangement, helps minimize nonlinearities and finally, the presence of three bones allows the inclusion of a protective overload device to limit damage to the hearing mechanism. This overload protection arises due to a change in vibration mode of the ossicles for very intense sounds (> 140 dB). A second protective device within the middle ear consists of two small muscles which draw the tympanic membrane inwards and the stapes outwards. These muscles are normally stimulated by reflex action to sounds of > 90 dB which last for longer than 10 ms. The effect of these muscles is to reduce low and medium frequency sounds by 30 dB.

The inner ear is a system of liquid filled canals, protected both mechanically and acoustically by being in the temporal bone of the skull. The cochlea is the part of the inner ear which contributes to the hearing process. It is a hollow coil of bone filled with liquid. It has a total length of about 40 mm and is divided along its length by the basilar membrane apart from a small gap at the end known as the helicotrema. The two main divisions of the canal are called the scala vestibuli and scala tympani. The oval window in the wall of the latter and the round window in the wall of the former. About 24000 nerve endings terminate in hair cells embedded within the basilar membrane. These hair cells are responsible for the frequency analysis of the vibration signal. The particular mechanism of the transformation from vibration energy to nerve impulse is the subject of debate beyond the scope of this thesis. Intense sounds can damage or destroy any of the moving parts of the ear, but when hearing damage results from prolonged exposure to



high levels of noise, it is generally the hair cells that are damaged.

### 2.3 Characteristics of Normal Hearing

Otologically normal subjects have an amplitude hearing range of about 140 dB from the threshold of hearing, which is 20  $\mu$ Pa at 1 kHz, up to the threshold of pain where instantaneous damage or acoustic trauma can result. The range of frequencies which can be detected by the ear is roughly 20 Hz to 20 kHz. The ear is non-linear in both amplitude and frequency sensitivity; there is approximately 70 dB difference in the threshold of hearing between 3 kHz and 20 Hz. As the level increases the bandwidth of the ear generally increases. The threshold of hearing for normal subjects is shown in Figure 2.2.

In the midband region, where the ear is most sensitive, the minimum detectable sound pressure is only just greater than the pressure variation due to thermal agitation of the air molecules. This provides a noise floor for any hearing mechanism. Animals who can hear more than humans therefore do so as a result of greater bandwidth.

A significant problem in assessing characteristics of hearing is relating objective measurements to subjective responses. Attempts at obtaining objective responses are discussed later, but the techniques used are generally highly invasive in nature and are hence often used only in animal experiments.

As discussed earlier, the hearing process is extremely complex, and not fully understood, but some of the phenomena of hearing are of

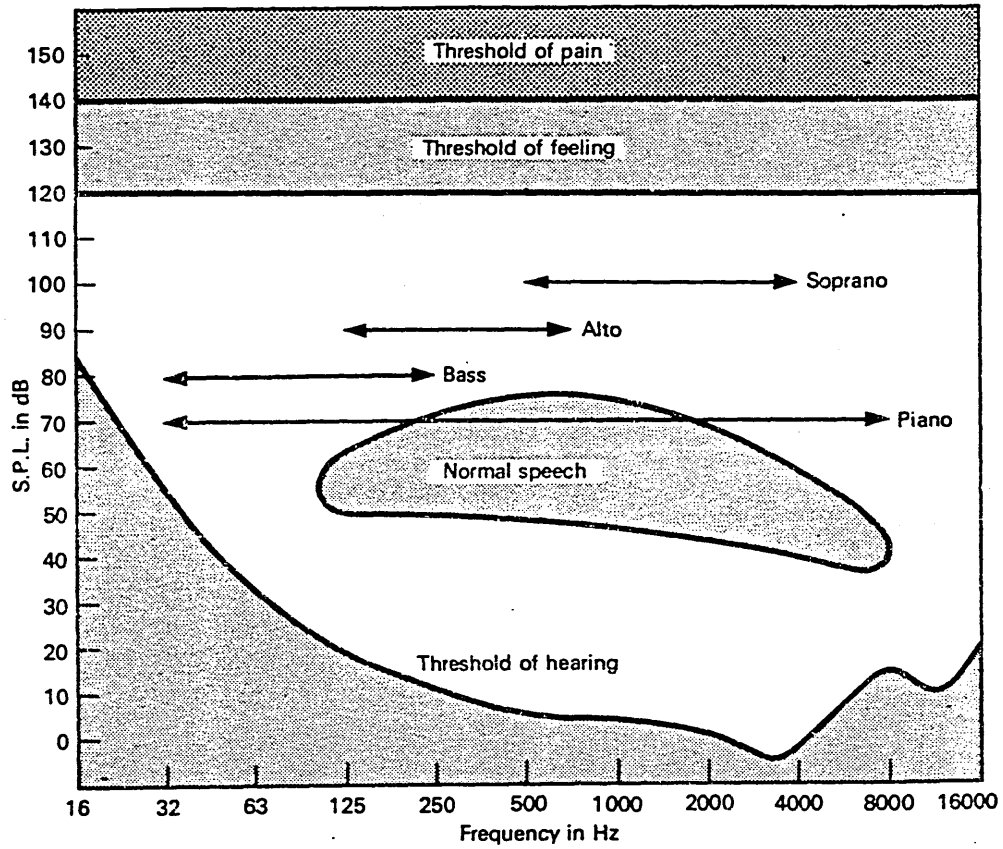


FIGURE 2.2 Threshold of Hearing for Normal Subjects

particular importance when designing a measuring instrument which is essentially trying to simulate the response of the human ear. The intensity of a sound is a precise physical quantity, capable of being defined analytically and measured practically. The subjective response to intensity, which is loudness, is a function of frequency as well as intensity. Equal loudness level contours are shown in Figure 2.3 .

The frequency selective hair cell process in the basilar membrane has critical bandwidths associated with its operation. This means that over a narrow bandwidth of input frequencies, exactly the same nerve stimulation will result from a particular input level. Further, if an input signal stimulates a number of hair cells, ie it has greater than the critical bandwidth, the loudness is greater than if the sound intensity were all within the critical bandwidth. This frequency weighting is also level dependant.

The equal loudness contours of Figure 2.3 do not represent a true loudness scale, ie equal increments in loudness level do not correspond to equal increments in subjective loudness. One true loudness scale has been determined by Fletcher [1] using the assumption that pure tones, of equal loudness, which stimulate different portions of the basilar membrane would have an additive effect. The perceived loudness of two such tones acting at once is taken as twice that of each individual component. The result of Fletcher's experiments is an empirical relationship between loudness level in phons and loudness in sones. The sone is the unit of loudness which is defined as being the loudness of a 1 kHz tone of 40 dB intensity level. This is equal to the loudness of any sound having a loudness level of 40 dB. A graph which summarises

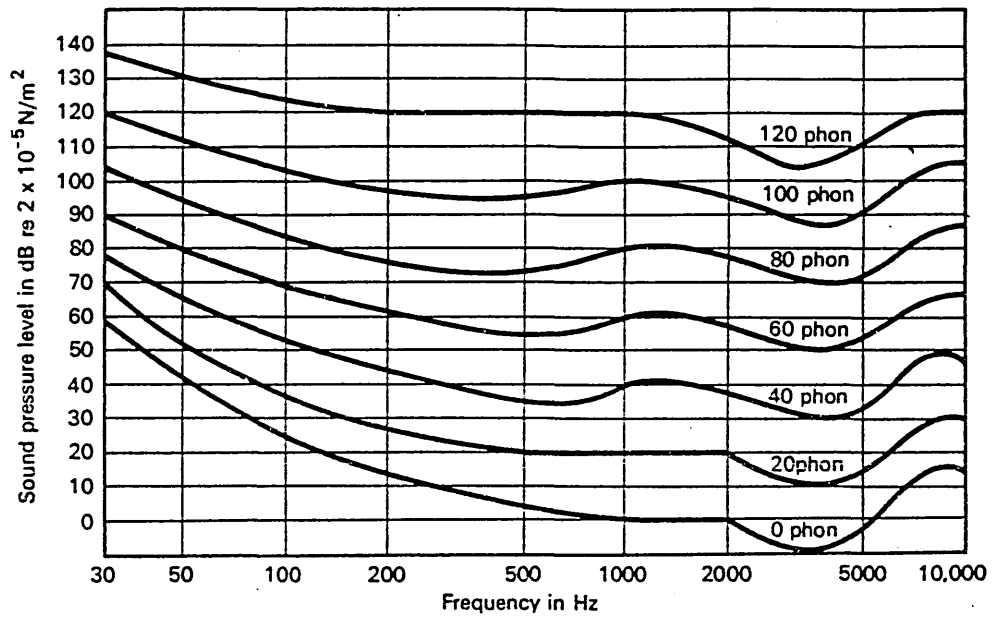


FIGURE 2.3 Equal Loudness Level Contours

the conclusions of Fletcher's work is shown in in Figure 2.4. The curve is represented by the following equation:

$$\begin{aligned}\log L &= 0.033 (LL - 40) \\ &= 0.033 LL - 1.32\end{aligned}\tag{2.1}$$

where  $L$  is the loudness in sones

$LL$  is the loudness level in phons

For a 1 kHz pure tone the loudness level in phons is numerically equal to the intensity level in dB:

$$LL = 10 \log \frac{I}{I_0}$$

where  $I$  is the intensity in  $\text{Wm}^{-2}$

$I_0$  is the reference intensity of  $10^{-12} \text{Wm}^{-2}$

Therefore,

$$LL = 10 \log I + 120$$

Substituting this value of  $LL$  into equation 2.1 gives:

$$\begin{aligned}\log L &= 0.033 (10 \log I + 120 - 1.32) \\ &= 0.33 \log I + 2.64\end{aligned}$$

Therefore:

$$L = 445 I^{0.33}$$

The subjective loudness  $L$  of a pure tone at 1 kHz therefore varies as the cube root of the intensity in  $\text{Wm}^{-2}$ . To achieve a doubling in subjective loudness, it is necessary to increase the sound power by a factor of eight.

In order to estimate the subjective response to a broad band signal the following procedure should be followed:

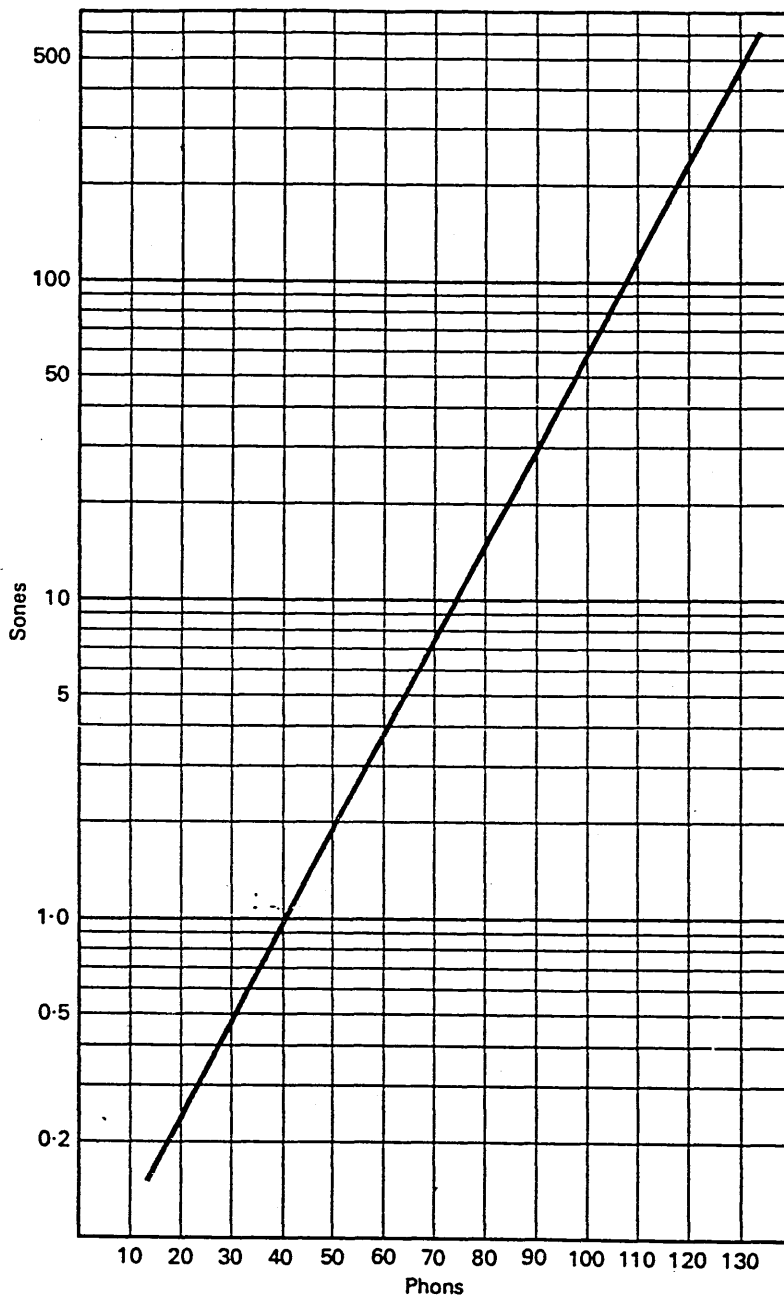


FIGURE 2.4 Relationship Between Sones and Phons

- 1 For each frequency component, or bandwidth less than the critical bandwidth, determine the loudness level in phons corresponding to the intensity level using the curves of Figure 2.3.
- 2 Use the empirical relationship of Figure 2.4 to determine the loudness levels in sones.
- 3 Add the individual values of loudness to determine the total loudness.
- 4 Use Figure 2.4 again to determine the overall loudness level in phons.

This is the intensity which a 1 kHz pure tone would need to have in order to produce the same apparent loudness.

A measuring instrument to measure loudness would be impractically complex as it would have to provide a continuously variable level and frequency sensitive weighting network. The generally accepted compromise is to use a sound level meter with a number of fixed frequency weighting networks which correspond to the response of the ear at different average sound levels. These are the A-, B- and C- weighting responses shown in Figure 2.5. Recent practice has been to rely almost solely on the A- weighting network for most noise measurements, independent of level. This is inconsistent with the risk of hearing damage predicted by the Equal-Energy Hypothesis discussed later in this chapter.

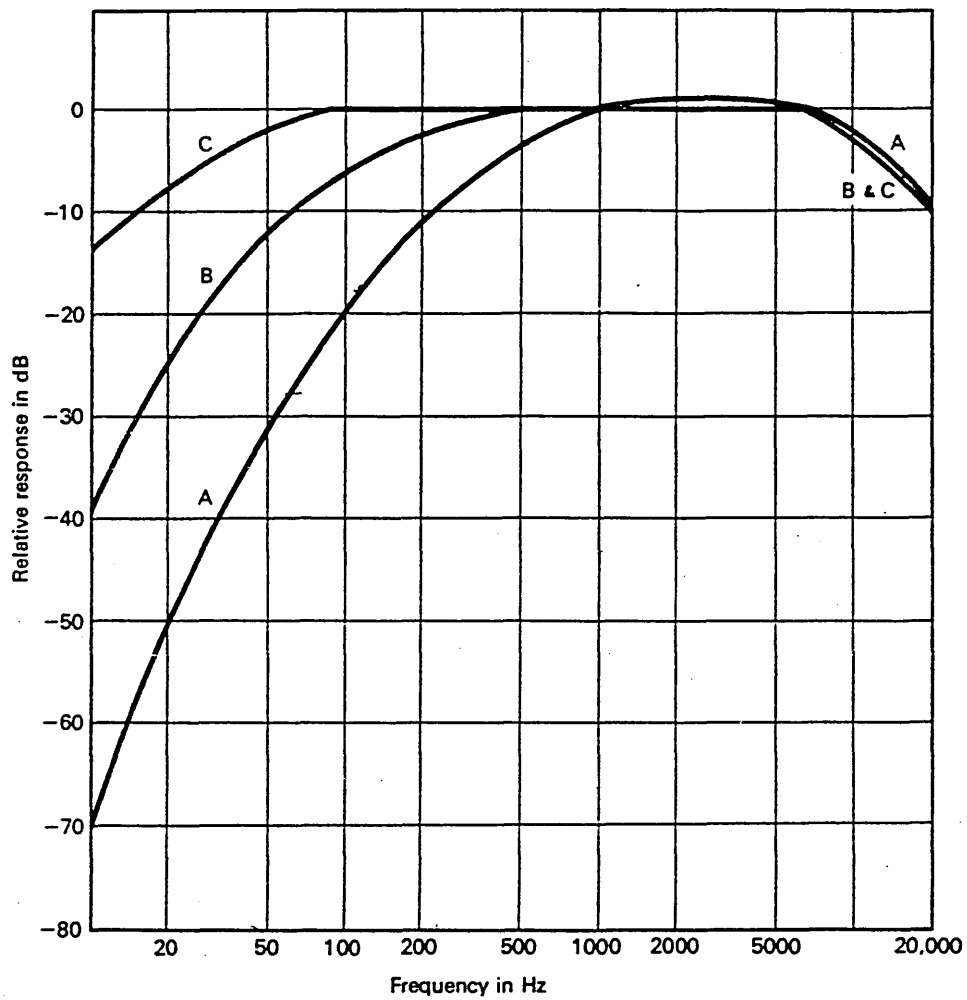


FIGURE 2.5 Frequency Weighting Curves



## 2.4 Hearing Defects not caused by noise

In attempting to analyse and validate theories which relate exposure to noise with hearing loss, it is important to determine the significance of the hearing loss. There are a number of natural causes of hearing defects which must be considered before ascribing a subject's hearing loss to noise exposure. Recent government legislation and codes of practice have encouraged companies to monitor their employees hearing on a regular basis, so that those with an initial hearing defect or with a particularly sensitive hearing mechanism can be identified and protected.

### 2.4.1 Presbycusis

The threshold of hearing for normal subjects, shown in Figure 2.2 represents the average threshold for adult subjects less than 25 years old with normal hearing. Presbycusis is the gradual degradation of hearing with age. It is characterised by a decrease in the hearing bandwidth at the high frequency limit. It is unclear whether presbycusis is a true ageing process or a noise induced hearing loss due to exposure to a normal acoustic environment. A survey of a primitive tribe who had been exposed only to low levels of environmental noise revealed that the typical hearing response of a 70 year old from this group had hearing acuity comparable with the average 30 year old American. It is usually very difficult to confidently separate the effect of presbycusis from any hearing loss which is noise induced.

#### 2.4.2 Tinnitus

Tinnitus is characterised by a high-pitched ringing in the ear. Some people suffer from this condition permanently and as a result often have speech problems. The condition often occurs temporarily in most people, particularly after exposure to high noise levels.

#### 2.4.3 Deafness

There are three identifiable classes of deafness :  
conductive, nerve and cortical.

Conductive deafness can result from thickening of the ear drum, stiffening of the joints of the ossicles or blocking of the external canal by wax. Bone conductive bypasses the defective elements and hence limits the hearing loss to between 50 and 55 dB, though this still represents a serious loss. Some causes of conductive hearing loss can be relieved by surgery. Otosclerosis which immobilises the stapes can be helped by fenestration, where a new window is introduced into the lateral semi-circular canals. Perforated ear drums which can be caused by disease or acoustic trauma may heal naturally or may be replaced by an artificial ear drum. Conductive deafness is characterised by an attenuation which is independent of amplitude.

Nerve deafness is due to a loss of sensitivity in the sensory cells in the inner ear or to a defect in the auditory canal. There is generally no cure and the hearing loss varies with frequencies.

Cortical deafness chiefly affects old people and is due to a

defect in the brain centres.

## 2.5 Noise induced hearing defects

Immediate permanent deafness caused by noise is due to sound pressures of around 150 dB or greater. Such sound pressures are generally only the result of a blast or explosion, therefore a noise induced hearing loss is rarely caused traumatically. The more usual situation is for the hearing loss to occur gradually over a period of time with exposure level and duration being factors affecting the rate of loss.

### 2.5.1 Temporary and Permanent Threshold Shift

If a subject is exposed to a fairly high noise level the sensitivity of the hearing will reduce. This is determined by measuring the threshold of hearing at various frequencies and comparing these results with the average response of Figure 2.2. Unlike the effect of presbycusis which reduces the overall bandwidth, a noise induced threshold shift is normally observed. This threshold shift is almost invariably centred around 4 kHz, largely independent of the characteristics of the noise.

If sufficient time is allowed between exposures, the hearing recovers and the subject has suffered only a temporary threshold shift (TTS). However, if the exposure is repeated before the hearing recovers, and if the exposure is of a sufficiently high level, a permanent threshold shift (PTS) will result.

The initial dip in sensitivity at 4 kHz continues to

increase for about 10 years. After this time the maximum hearing loss stabilises but the threshold shift then spreads out to affect a progressively greater portion of the hearing bandwidth. As discussed in section 2.2, the important speech energy of consonants is around the 4 kHz region and therefore these will be the first sounds to be affected. The widening of the affected bandwidth results in more and more of the speech energy being lost, with human speech becoming less and less intelligible.

## 2.6 Criteria for Assessing the Risk of Hearing Damage

Sound level meters with specified performance were available as long ago as 1944 [2]. Since that time it became apparent that there was a link between the duration and level of exposure in determining either the degree of TTS or PTS. Early animal studies led to an inconclusive debate about the relative importance of these two factors.

### 2.6.1 Equal Energy Hypothesis

The advent of the jet engine led to particularly noisy working environments for ground servicing personnel. These environments provided a focus for a number of research projects sponsored by the USAF. "Damage Risk Criteria" were proposed by Rosenblith and Stevens in 1952 [3]. The levels recommended by these criteria tended to be rather conservative as they were based on almost continuous exposure. A more realistic study which included the effects of short time exposure was published by Eldred, Gannon and Von Gierke in 1955 [4]. Although this work presented no

specific results, it offered the work of Eldredge and Covell [5,6] as evidence to support the equal-energy hypothesis (EEH). The EEH is based on an exact equivalence between sound intensity and exposure duration, that is the total energy received by the ear is important, rather than the manner in which it was received. The work of Eldred et al was proposed as a code of practice for minimising hearing damage to the service personnel. In addition to the adoption of the EEH, it established 135 dB as the maximum exposure level for the unprotected ear on the basis that this represented the lower limit for the threshold of pain for subjects with tender ears.

The recommendations of this work were formally established in the United States by Air Force Regulation AFR 160-3, 1956. Other work [7,8,9,10,11] advanced arguments in favour of both the EEH and other intensity-exposure relationships. What was generally accepted was that the EEH would ensure better protection, particularly for exposure to impulsive noises. The exchange rate implied by the EEH is that a doubling of intensity or a doubling of exposure duration would lead to the same increase in received energy. The intensity is doubled by increasing the sound pressure by 3 dB, therefore the exchange rate implicit in the EEH is often referred to as 3 dB doubling. A number of pressure groups proposed different exchange rates. The Walsh-Healey Act (1969) formalised 5 dB doubling within the United States. Dixon Ward and Nelson [12] described the adoption of 5 dB doubling as being a "guesstimate" which was more political than scientific in nature.

Within the United States there remains a duality of standards for personal noise dosimeters, however, 3 dB doubling is universally accepted as being appropriate for integrating sound level meters.

In Britain, the route to adopting the principles of the EEH as part of noise legislation has been via the Wilson Committee Report (1963), which proposed various exposure damage risk criteria, and the "Noise in Industry" report of Burns and Robinson (1970). This latter report formed a basis for the Code of Practice for Reducing the Exposure of Employed Persons to Noise (1972). The Health and Safety at Work Act (1974) was the legal instrument designed to enforce the principles of the code. These basic principles are a maximum of 90 dB, 8-hour equivalent continuous sound level ( $L_{eq}$ ) and a maximum level of 135 dB for the unprotected ear, as proposed in 1955 by Eldred, Gannon and Von Gierke.

The only unresolved question relating to the EEH is what average intensity provides an acceptable risk of hearing damage. Most countries have accepted 90 dB as the maximum  $L_{eq}$  for an 8 hour day. Wealthier countries such as the United States and Sweden have reduced this level to 85 dB to minimise the risk for their workers. It is unlikely that there will be pressure to reduce exposure to less than this as there is evidence that no measurable hearing loss occurs as a result of exposure to sound levels of 80 dB and below. This is almost certainly due to masking by the normally occurring hearing degradation of presbycusis.

THE NATURE AND MEASUREMENT OF  $L_{eq}$ 

Before the main body of the work on the design and evaluation of integrating sound level meters could begin, it was necessary to investigate the standard equation for  $L_{eq}$ , in order to understand how best to generate the constituent components of the  $L_{eq}$  function, and to determine whether an approximate solution based on numerical methods would be viable.

The standard equation for  $L_{eq}$  is defined by:

$$L_{eq} = 10 \log_{10} \frac{1}{T} \int_0^T \frac{P^2(t)}{P_0^2} dt$$

$L_{eq}$  is therefore the mean value integral of the sound intensity expressed on a logarithmic scale. This can be contrasted with the equation for sound pressure level:

$$SPL = 20 \log_{10} \sqrt{\frac{P^2}{P_0^2}}$$

The two functions are very similar, but the averaging time of sound level is one second or less. The averaging methods are also different; in that with sound pressure level, the averaging is an exponential function so that its integrating period is usually much less than the measurement period.

The long integrating capability implied in the  $L_{eq}$  equation is central to the value of  $L_{eq}$  in assessing the risk of hearing damage due to a varying noise climate. It is important for the integration to be continuous throughout the measurement period, as a short, high-level transient can form a large contribution to the final  $L_{eq}$  if the general

level is low.

It is profitable to consider the general form of the mean value integral, as expressed in the mean-value theorem:

$$f(\xi) = \frac{1}{(b-a)} \int_a^b f(x) dx \quad \text{where } a \leq \xi \leq b$$

This equation justifies the basis for  $L_{eq}$ , as it shows that a single value of the function,  $f(\xi)$ , can be used to represent the mean value of  $f(x)$  over the integration range. In an ISLM, the function  $f(x)$  is proportional to the sound intensity. The equation also shows that the mean value of the intensity corresponds to the actual value of the intensity at time  $\xi$ . In a typical noise pattern, the level may rise and fall many times during the integration period, so that  $\xi$  would probably correspond to a large number of elapsed times. Therefore the value of  $\xi$  has no physical significance for  $L_{eq}$  as it is generally a many valued function.

Reference to the block diagram of Figure 3.1 shows how the  $L_{eq}$  function can be constructed from basic analogue building blocks. The squaring element is performed by a combination of a logarithmic amplifier and an antilogarithmic amplifier. The input signal to the logarithmic amplifier must be unipolar, which explains the inclusion of the absolute value or precision full-wave rectifier stage. The square of the input signal can be integrated continuously with an analogue integrator to yield a stored value of the dose. A similar store representing the elapsed time can be constructed so that when the stored value of dose is divided by the stored value corresponding to the elapsed time and the logarithm of the quotient derived, the result is a representation of the  $L_{eq}$  of the input signal.



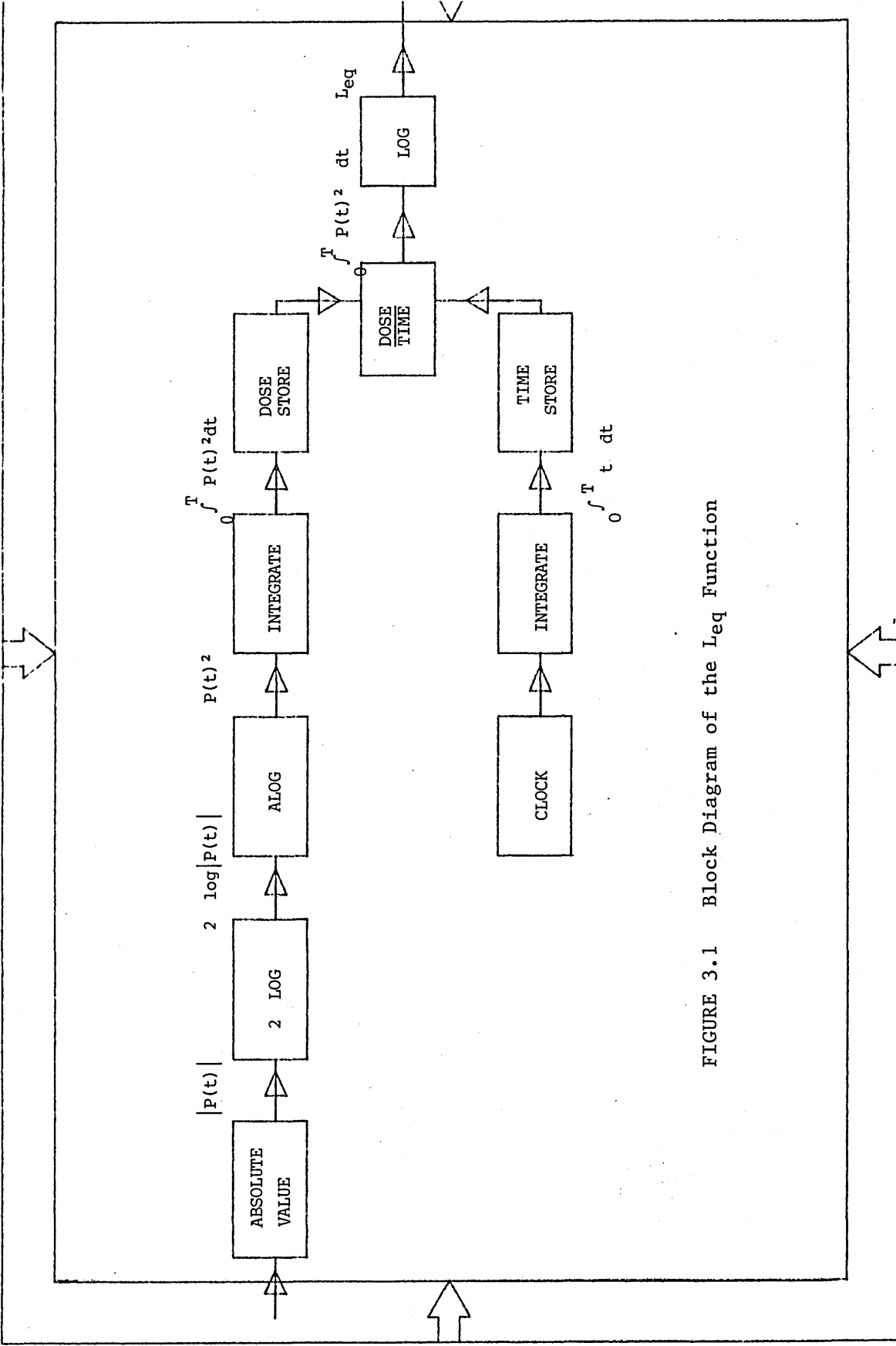


FIGURE 3.1 Block Diagram of the Leq Function

The straightforward approach to generating  $L_{eq}$  when using analogue building blocks must be modified if an approximate solution is envisaged. If the input signal were digitized, the integration would have to be performed numerically. A good approximation can be gained by using Simpson's Rule for a range divided into  $n$  parts:

$$\int_a^b f(x) dx = \frac{h}{3} \{f_0 + f_n + 4(f_1 + f_3 + \dots + f_{n-1}) + 2(f_2 + f_4 + \dots + f_{n-2})\}$$

where  $n$  is the number of strips

$h$  is the width of each strip

The two summation terms would represent very large numbers if a large number of samples were being integrated. This would generally be the case since, to ensure accurate resolution of a 24 kHz sinewave, which would be necessary for 1/3 octave frequency analysis, 10  $\mu$ second sampling would be required. The effect of an increasing number of samples on the store capacity needed to accommodate the summation terms would be to increase the storage length by one bit for each doubling of the number of samples. The conversion accuracy required to encompass the large dynamic range of industrial noise signals is approaching 20 bits. Therefore as the number of samples is increased, the size of digital stores required soon becomes extremely large.

The logarithmic conversion can also be performed using numerical methods. The usual method is to use a power series expansion as follows:

$$\frac{1}{2} \log_e \left[ \frac{1+x}{1-x} \right] = x + \frac{x^3}{3} + \frac{x^5}{5} + \dots \quad \text{for } -1 < x < 1$$

To obtain the resolution which would be required for a precision grade instrument, a large number of terms would need to be evaluated. The dose integral could be a large number, and so the value of  $x$  in the power series expansion given above would be very close to unity. This leads to

smaller differences between terms in the series and hence increases the number of terms which would need to be considered for a given resolution. Although the magnitude of the numbers involved would not be affected greatly by increasing the number of terms considered, it may lead to an increase in processing time for each logarithmic conversion.

When the plan of work was proposed, it was envisaged that significant advances in digital signal processing component technology would enable the difficulties outlined above to be overcome. The microelectronic industry has, however, tended to concentrate on the industrial controller microprocessors (microcontrollers), and there has been limited progress on the development of certain aspects of 8- and 16-bit microprocessors. A significant limitation of relevance to the present application was the lack of CMOS technology processors. The low power consumption of CMOS processors is essential to the development of a hand-held instrument. Thus it was realized that the section of the proposed plan which was concerned with total signal processing by the microprocessor would not be viable. Attention was therefore focused on the selective use of the microprocessor in a control function in those areas of the processing to which it would lend enhancement.

## EVALUATION METHODS FOR INTEGRATING SOUND LEVEL METERS

Integrating Sound Level Meters (ISLMs) are almost exclusively calibrated with a continuous input signal. This only confirms the meter's ability to measure sound pressure level, but tells nothing about the meter's ability to measure impulsive signals - the type of signals which require the use of an ISLM in place of a conventional sound level meter. When this work was started, there was no accepted method for testing ISLMs. Although this is still an issue for dispute, several proposals have since been put forward; one in particular was being considered in draft form for issue by the International Electrotechnical Commission (IEC) as an international standard. This has been issued subsequently as IEC 804.

In the absence of any standard, it was decided to test and evaluate ISLM designs using electrical signals substituted in place of the microphone, and to construct specialized signal sources so that these electrical signals would quantify certain parameters of particular relevance to the measurement of  $L_{eq}$ . Shortly after this time the Health and Safety Executive (HSE) proposed a draft standard for ISLMs as part of a commercial tender on behalf of H.M. Factory Inspectorate. The testing procedures embodied in this draft standard are broadly the same as those which had been considered previously for use in this work. The HSE-produced draft standard was therefore adopted so that results produced as part of this work could be compared readily with results from tests performed by the HSE and any other researchers who adopted the HSE draft standard. The principles embodied within the HSE draft standard subsequently formed a substantial part of IEC 804 draft standard referred to earlier. Constant interaction with the HSE and other

professional acousticians at meetings and conferences has allowed the ideas resulting from this work to contribute to the current, and proposed, national (UK & USA) and international standards.

Instruments which generate the parameter  $L_{eq}$  are integrating sound level meters, so as well as performing tests to ascertain the amplitude linearity in the same way as with a conventional sound level meter, the integrating function of the meter must also be checked. The trading relationship between sound pressure level and time is usually referred to as the exchange rate. For an ISLM based on the Equal-Energy Hypothesis, the exchange rate is 3 dB. This means that for a constant value  $L_{eq}$ , if the measurement duration is halved, the sound pressure level must be increased by 3 dB, and conversely, if the measurement duration is doubled, the sound pressure level must be reduced by 3 dB. This is often referred to as 3 dB doubling.

It is usually overlooked that the value of 3 dB is derived from  $10 \log_{10} 2$ , which is more precisely 3.01 dB. This discrepancy is of little significance when dealing with conventional sound level meters with a fairly restricted dynamic range, but over the extended dynamic range of an ISLM, the discrepancy could exceed the measurement tolerance allowed. However, an exact relationship between measurement duration and level does exist, which is that an increase in measurement duration of an order of magnitude is equivalent to a decrease in level of 10 dB, and vice versa, since  $10 \log_{10} 10 = 10$ . It is this latter relationship which is employed in the tests described in this work.

For a single range instrument operating under the fairly well controlled environmental conditions of a laboratory, there are three basic parameters which characterize the performance of a particular ISLM.

These are the dynamic span, the exchange rate tolerance and the peak factor capability. These parameters are detailed below:

#### 4.1 Dynamic Span

The dynamic span is a measure of the range of signal amplitudes and frequencies which can be applied to an ISLM so that it is capable of calculating  $L_{eq}$  to within a certain tolerance. Four different grades of instrument are recognized in the HSE draft standard in accordance with IEC 651, the consolidated revision of the sound level meter standards, these are designated Types 0, 1, 2 and 3; the different grades being required to respond with different accuracies and over different frequency ranges, as shown in Table 4.1.

ISLM Type	0	1	2	3
Frequency range	20Hz-16kHz	20Hz-12.5kHz	31.5Hz-8kHz	31.5Hz-8kHz
Within indicator range (dB)	±0.4	±0.6	±0.8	±1.5
Outside indicator range (dB)	±0.8	±1.0	±1.5	±3.0

TABLE 4.1 Dynamic Span Tolerances

The test procedure consists of applying a sinusoidal input signal of frequency within the range specified for the particular grade of meter to be tested. The amplitude of the input signal is adjusted in fine increments, say 0.1 dB, and the meter reading is noted after it has stabilized to better than 0.2 dB for Type 0 and 1 meters, better than 0.5 dB for Type 2 meters, and better than

1.0 dB for Type 3 meters. To test the linearity of the dynamic span above the indicator range, a sequence of tone bursts is used to give a value of  $L_{eq}$  within the indicator range. The dynamic span is then the difference in r.m.s. levels, expressed in decibels, between the upper and lower signal levels within which the tolerances of Table 4.1 are met. The dynamic span required for the different grades of instrument are shown in Table 4.2.

ISLM Type	0	1	2	3
Dynamic span (dB)	70	60	50	40

TABLE 4.2 Dynamic Span

For reasons discussed in Chapter Five concerning electrical circuit design, the higher frequencies usually present the greater problem to ISLMs, so in order to determine whether a particular meter satisfies the standard for its specified grade, testing would normally begin at the higher frequencies. However, to determine the performance characteristics of an ISLM over the whole range of input signal amplitudes and frequencies is very time consuming, so a restricted frequency range will probably have to be specified in an international standard for abbreviated testing of a meter's dynamic span.

#### 4.2 Exchange Rate Tolerance

A test which is much quicker to perform, and does not require the use of expensive 0.1 dB step attenuators, is the exchange rate tolerance test. As described earlier, this test is based on the equivalence of a change in signal duration by an order of

magnitude and a change in signal level of 10 dB. A specially constructed tone burst generator is used to alter the mark/space ratio of the signal. The signal amplitude is adjusted accordingly so as to maintain a constant value  $L_{eq}$  input.

Initially, a reference is established, using a continuous sinusoidal input of frequency 6 kHz, at a level 10 dB above the lowest point of the indicator range or the lowest point of the dynamic span, whichever is the higher. A sequence of tone bursts of 6 kHz sinusoids is then substituted at such a level as to give an input  $L_{eq}$  of identical value to that of the continuous signal. The readings obtained with the tone burst input should differ from the reference level by no more than the tolerances specified in Table 4.3. In this table there are two values corresponding to each tone burst duration and instrument category. The upper figure is that proposed by the HSE and the lower figure is that adopted by IEC 804.

Intermediate mark/space ratios may be used to check that the exchange rate tolerance does not exceed that of the next higher ratio. Such a test would help reveal any non-linearities in the meter's response; a task which the exchange rate test can perform more speedily than the continuous signal linearity test.

The HSE standard demands that the tone bursts used in the exchange rate test should be of such a duration as to "ensure that there are no limitations incurred as a result of peak factor limitations". The peak factor test and the difference between peak and non-peak category meters will be explained fully in the next section, however it is necessary that in the peak factor test, tone bursts



ISLM Type		0						1						2						3					
		Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak	Peak	Non-Peak						
Category	Relative Amplitude																								
Tone Burst mark/space 1:9	+ 10 dB	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2	± 0.2						
Tone Burst mark/space 1:99	+ 20 dB	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4	± 0.4						
Tone Burst mark/space 1:999	+ 30 dB	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0	± 0.6	± 1.0						
Tone Burst mark/space 1:9999	+ 40 dB	± 0.8		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0							
Tone Burst mark/space 1:99999	+ 50 dB	± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0		± 1.0							

TABLE 4.3 Exchange Rate Tolerance

10000  
1000000

10000  
100000000

10000  
1000000000

10000  
10000000000

10000  
100000000000

10000  
1000000000000

10000000000000

100000000000000

1000000000000000

have a duration between 1 millisecond and 1 second for peak meters, and between 200 milliseconds and 1 second for non-peak meters. Since the maximum amplitude signal used in the peak factor test is always 10 dB less than the corresponding maximum amplitude signal used in the peak factor test for a particular grade of instrument, it is assumed that if tone bursts used in the exchange rate test are not shorter than those used in the peak factor test, then the previously mentioned criterion will have been met.

It has been suggested that a further factor of ten times should be allowed by restricting the minimum exchange rate test tone burst to ten times the minimum peak factor test tone burst. This appears to be misunderstanding the usefulness of the exchange rate test. As well as confirming that a meter integrates according to the correct function, the exchange rate test also checks the impulse linearity of the meter over the lower section of the dynamic span, which the peak factor test fails to do.

The test frequency of 6 kHz used for the exchange rate test was probably chosen as it roughly coincides with the second frequency where the Linear and A-weighting network responses coincide; the first crossover frequency being 1 kHz, previously used in the sound level meter tests. As the frequency for the tests is not exactly the frequency where the two networks' responses coincide, there would appear to be little significance in its value, other than ensuring that if an ISLM is fitted with A-weighting response only, the full range of input signal amplitudes can be applied without overloading the input stage.

A tone burst of six complete cycles of 6 kHz provides the 1 millisecond tone burst duration required to test the peak category

meters. Tone bursts of single cycles of 6 kHz have been used in some of these tests, but such tests are outside the scope of the draft standard.

It is important that although the tone bursts are of 6 kHz sinusoids, the overall frequency spectrum of the input also includes frequencies corresponding to the period of the tone burst and the period between the bursts. Thus the instrument is being subjected to a fairly broad-band input. A typical input signal is shown in Figure 4.1 and the corresponding frequency analysis is shown in Figure 4.2. It is clear that the exchange rate test is a fairly comprehensive one, providing information about many aspects of ISLM performance.

#### 4.3 Peak Factor

Reference was made earlier to two categories of ISLM within each grade of instrument, namely peak and non-peak meters. The only difference between these two categories is in their capability to respond accurately to short duration input signals. The peak category meter's response is limited to signals having an amplitude which is considerably less than the upper extreme of its dynamic span.

The non-peak category ISLMs appear to be irrelevant, as the only advantage they have over the next lower grade of peak meter is a slight increase in frequency range and a marginal improvement on some of the test tolerances specified. Non-peak category meters have not been incorporated into IEC 804.

The peak factor test is performed by applying a single burst of

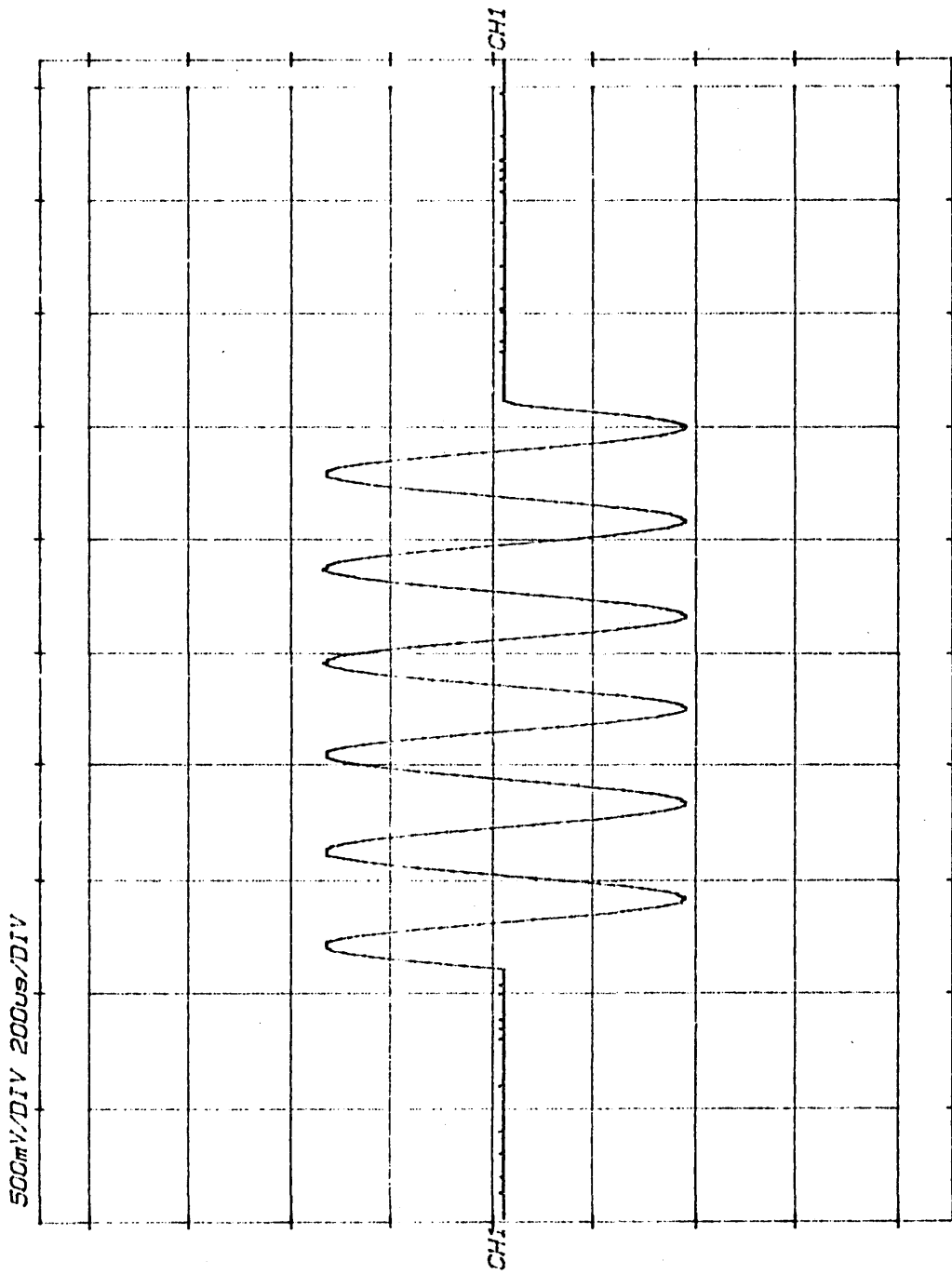


FIGURE 4.1 Tone Burst Used in Exchange Rate Test

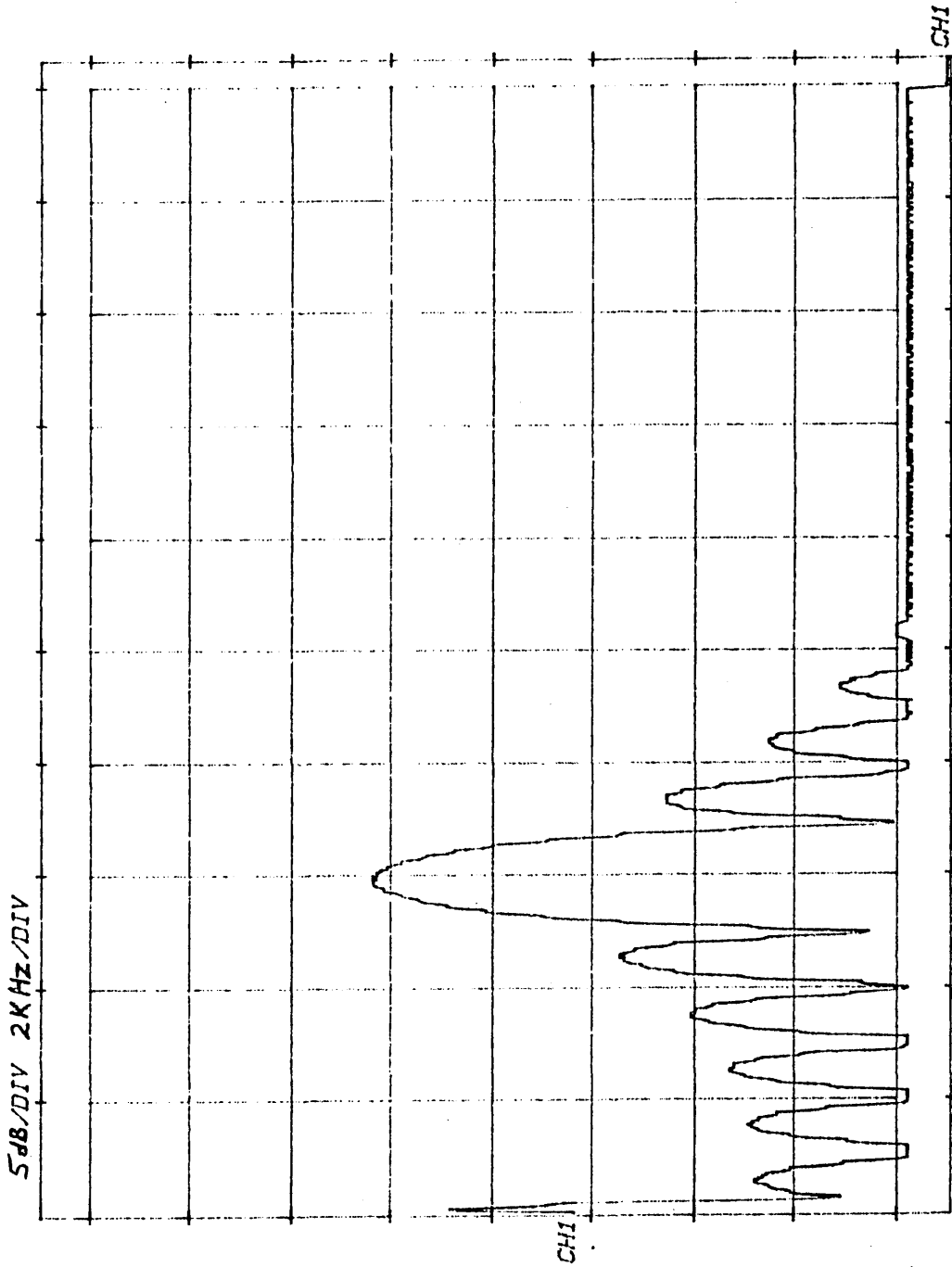


FIGURE 4.2 Input Spectrum for Exchange Rate Test

6 kHz sinusoid in the presence of a background of a continuous sinusoidal signal with a frequency of 6 kHz set to a level corresponding to the lower limit of the dynamic span. The background and the tone burst have to be in phase, as shown by the example waveform of Figure 4.3. The period of the tone burst should be, as mentioned earlier, between 1 millisecond and 1 second for peak meters and between 200 milliseconds and 1 second for non-peak meters.

The amplitude of the tone burst is increased in 1 dB steps until the indicated  $L_{eq}$  differs from the calculated  $L_{eq}$  by more than 0.5 dB (0.8 dB(A)) for Types 0, 1 and 2, and 1.0 dB (1.0 dB(A)) for Type 3 meters than that permitted by the linearity tolerances. The ratio of the peak value of the lowest amplitude tone burst which reaches this limit to the r.m.s. level of the background signal is the peak factor for the particular ISLM. The peak factor test is normally performed with the ISLM set to Linear response, but some meters may be fitted with A-weighting only and this accounts for the increased tolerance shown in brackets. The peak factor capability required for the various grades and categories of meters are shown in Table 4.4.

ISLM Type	0	1	2	3
Peak category (dB)	73	63	53	43
Non-peak category (dB)	40	30	25	20

TABLE 4.4 Peak Factor Capability

The peak factor test not only quantifies the maximum level of short

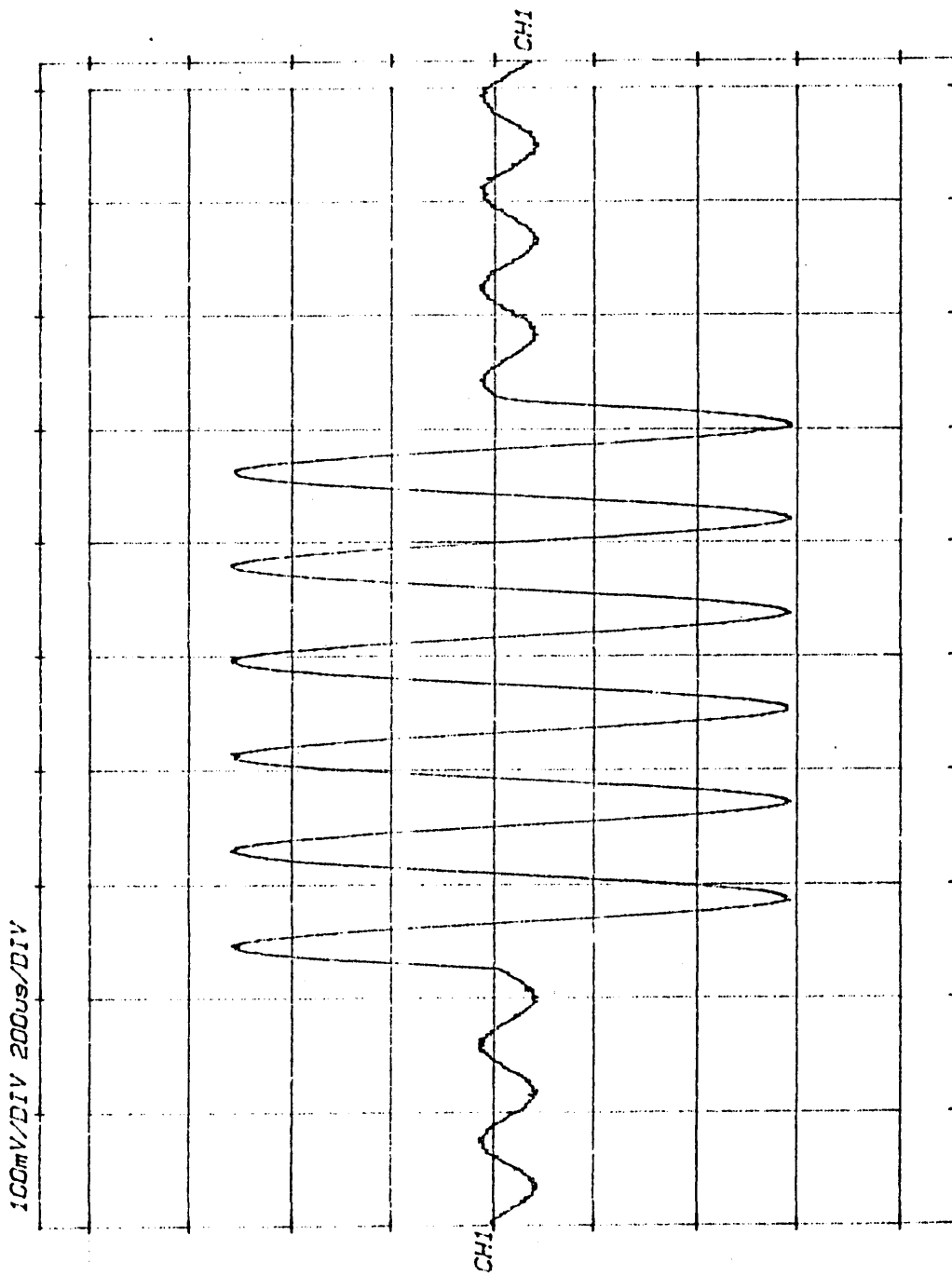


FIGURE 4.3 Tune Burst Used in Peak Factor Test



duration signal that the ISLM can measure, but also checks the impulse linearity over the upper section of the dynamic span. The test is difficult to perform on the non-peak meters due to the limitations of the tone burst duration and peak level. The non-peak meters do seem to be of limited use, providing little increased measuring capacity over a conventional sound level meter.

## DESIGN AND DEVELOPMENT OF AN ANALOGUE INSTRUMENT

The function  $L_{eq}$ , as discussed in the chapter on the evolution of  $L_{eq}$ , is the logarithm of a mean-value integral of the square of the sound pressure. As a result of the available expertise within the collaborating body, it was decided to investigate methods for generating this function using analogue techniques. It was realized that any meters or individual circuits developed as a result of this investigation could be used for comparison with designs embodying digital techniques, a development expected to form an extension of the basic work.

The squaring part of the function is usually formed by generating twice the logarithm of the input voltage, usually referred to as  $2\log V$ , and then antilogging the resultant current to give a final output current proportional to the square of the input voltage. Having the output in the form of a current is very convenient as it is easily integrated using a conventional Miller integrator. Unfortunately, it is only possible to construct a logarithmic amplifier which operates in one quadrant; this means that the input voltage and the reference must both be unipolar. The conversion from bipolar to unipolar input signal for the  $2\log V$ -alog stage is performed by an absolute value circuit.

### 5.1 Absolute Value Circuit

The absolute value circuit is a full-wave rectifier which avoids the usual forward voltage drop of a simple diode by incorporating it in the feedback loop of an operational amplifier. The forward voltage drop of this combination is the forward voltage drop of the diode divided by the open-loop gain of the operational amplifier;

which is considerable at low frequencies. An added advantage of placing the diode in the feedback loop of the operational amplifier is that the exponential forward conduction characteristic of the diode is linearized. The operation of the absolute value circuit, shown in Figure 5.1, is fully described elsewhere, but the heart of the absolute value circuit, which is the precision half-wave rectifier shown in Figure 5.2, needs to be considered in order to understand the limitations of the circuit. Diodes D1 and D2 change the feedback arrangement of A1 for different polarities of input. It is in the switching of diodes D1 and D2 that the problems arise, particularly with the combination of low signal level and high frequency. There is a deadband around zero resulting from the limited slew rate and gain in A1, and from capacitance and charge storage effects in the diodes. This deadband is a result of the finite time taken for A1 to swing through two diode voltage drops. The operational amplifier's limitations and the effects of the diodes, which compound the operational amplifier's problems, can cause this transition to be comparatively slow and hence introduce considerable distortion into the signal. An example of an input signal with its correctly formed absolute value trace is shown in Figure 5.3, and a sequence of absolute value traces, obtained using a constant low level input of increasing frequency is shown in Figure 5.4. The distortion of the waveform, even at modest frequencies, is quite evident, and this distortion would lead to a lower value of the energy integral and hence an underestimation of  $L_{eq}$ .

There are several ways of reducing the problems outlined above:

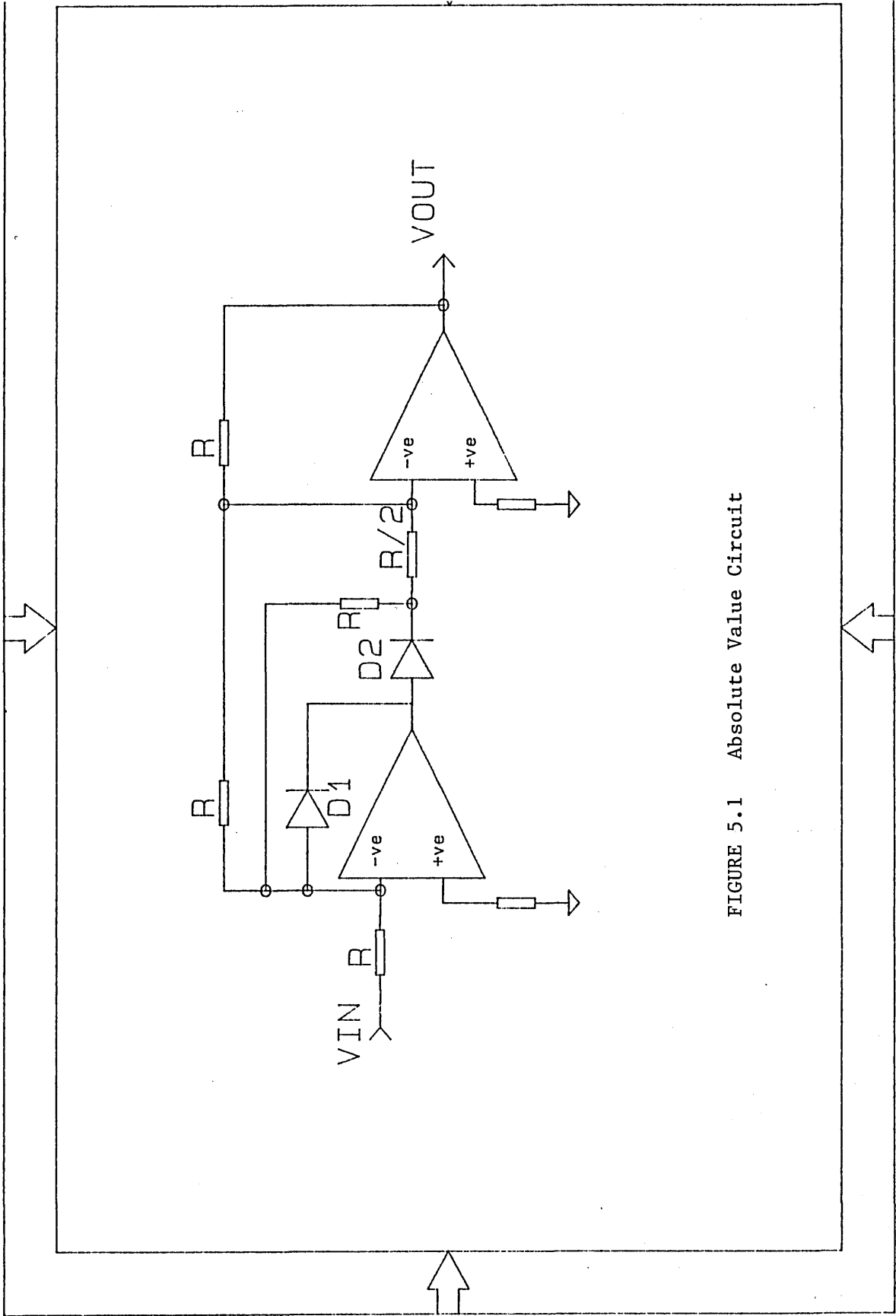


FIGURE 5.1 Absolute Value Circuit

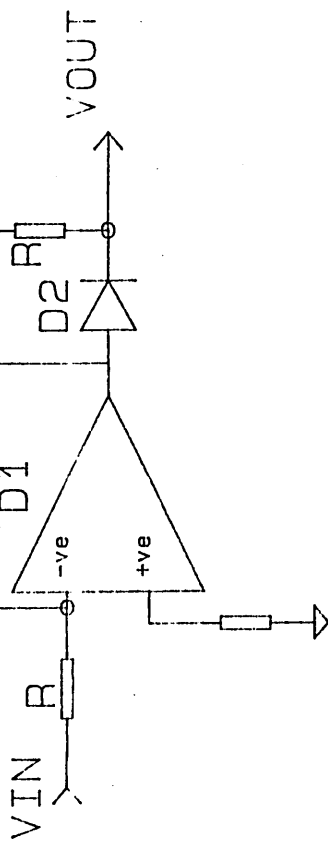


FIGURE 5.2 Precision Half-Wave Rectifier

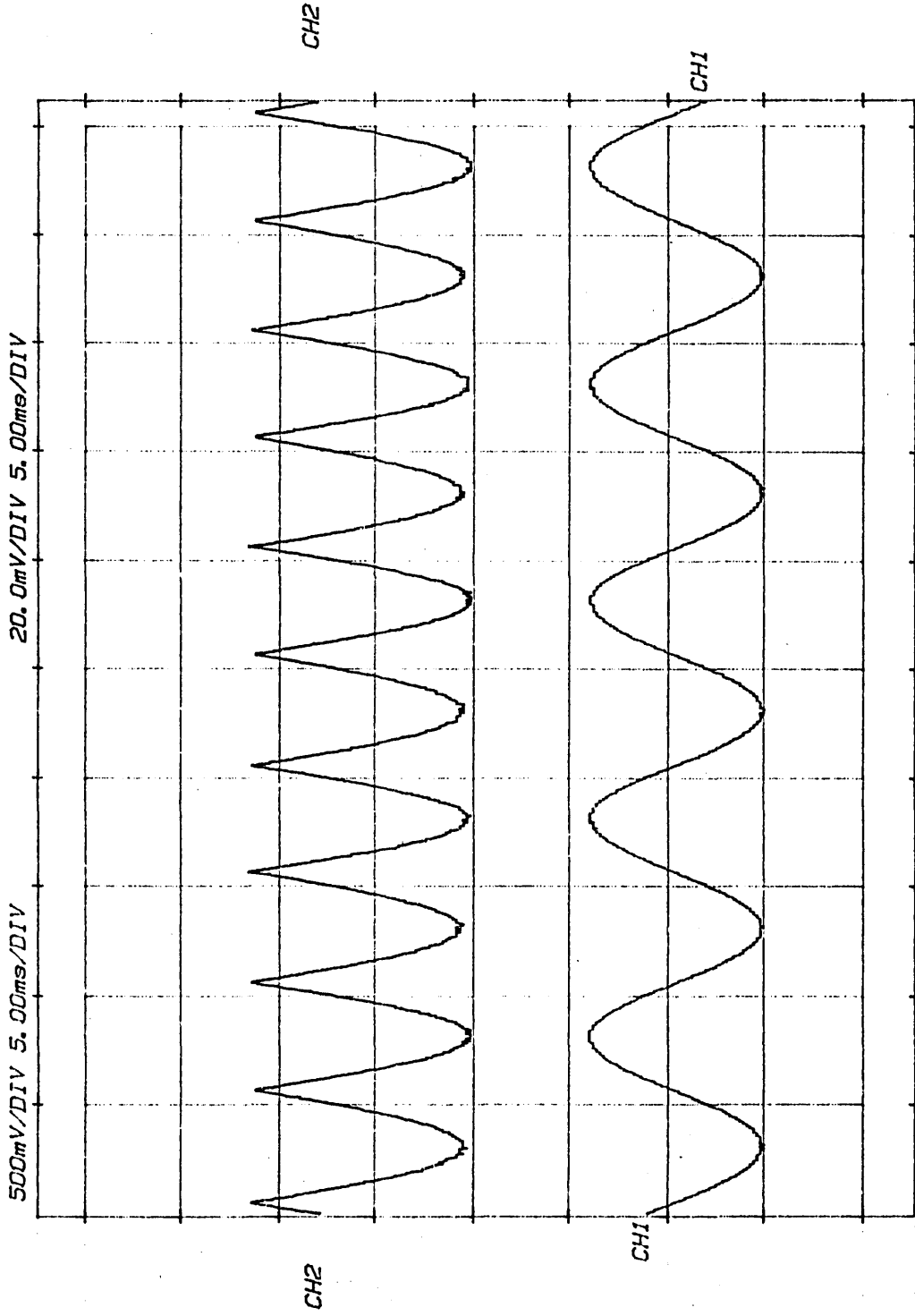


FIGURE 5.3 Input Signal (CH1) and Absolute Value (CH2)

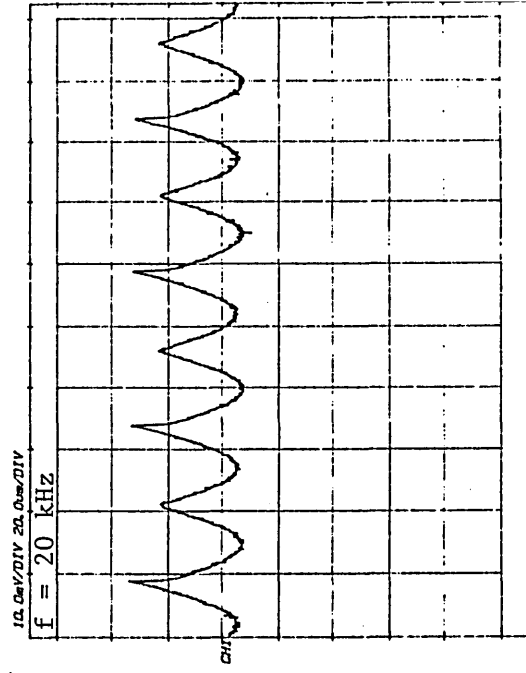
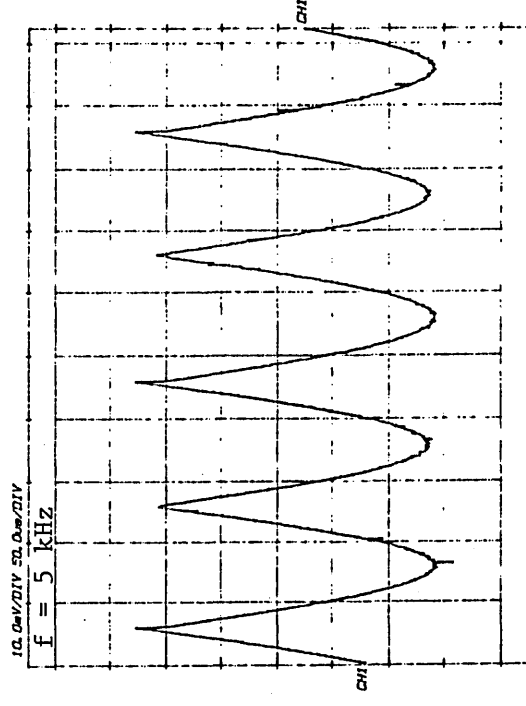
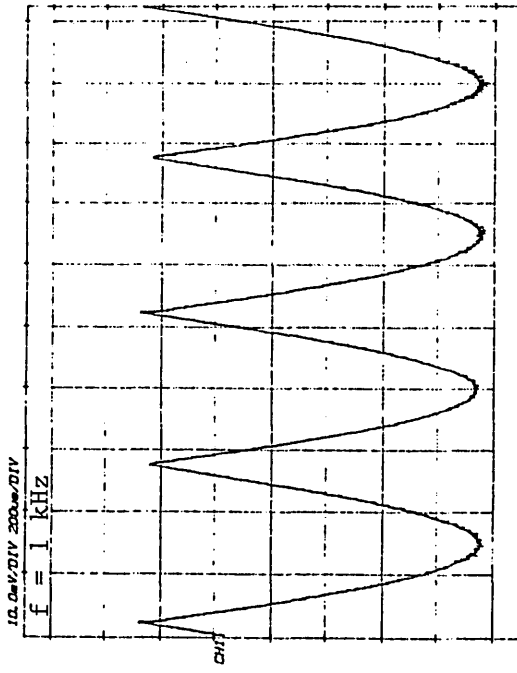
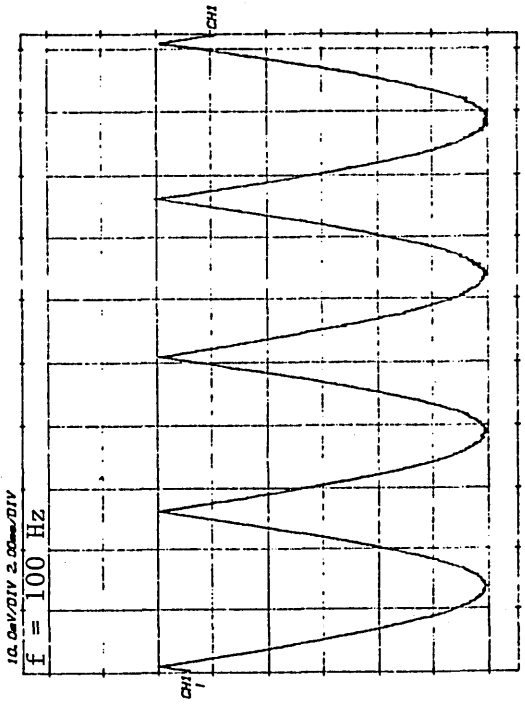


FIGURE 5.4 Performance of Absolute Value Stage as a Function of Frequency

1. A1 is chosen to have a high gain-bandwidth product and a high slewing rate.
2. Diodes D1 and D2 are chosen to have low reverse leakage, low forward voltage drop and a very short reverse recovery time.
3. The frequency compensation for the operational amplifier is carefully designed so as to keep the bandwidth as high as possible.

Initially, a fairly standard operational amplifier, an LM 301A, was used for A1, and 1N914 diodes were used for D1 and D2. Satisfactory performance was obtained at frequencies up to 100Hz, but severe shortcomings were apparent at higher frequencies.

To boost the gain-bandwidth of the operational amplifier, a complementary transistor stage was inserted between the operational amplifier and the diodes, as shown in Figure 5.5. The standard diodes were replaced by Fairchild FD700 computer diodes, chosen for their fast reverse recovery time. With the increased amplifier bandwidth and the improved diodes, it was possible to achieve about a 60 dB dynamic range at 10 kHz, however the circuit tended to oscillate and introduced a significant time delay. It became clear by using this circuit that in general, to achieve a larger dynamic range demands the use of higher static currents in the amplifier stage.

The LM 301A and transistor booster stage was therefore replaced by an operational amplifier with a high gain-bandwidth and high output current capability, an RCA CA3130 substituted for A1. This gave a 70 dB dynamic range at 2 kHz and between 60 dB and 70 dB at 20 kHz.



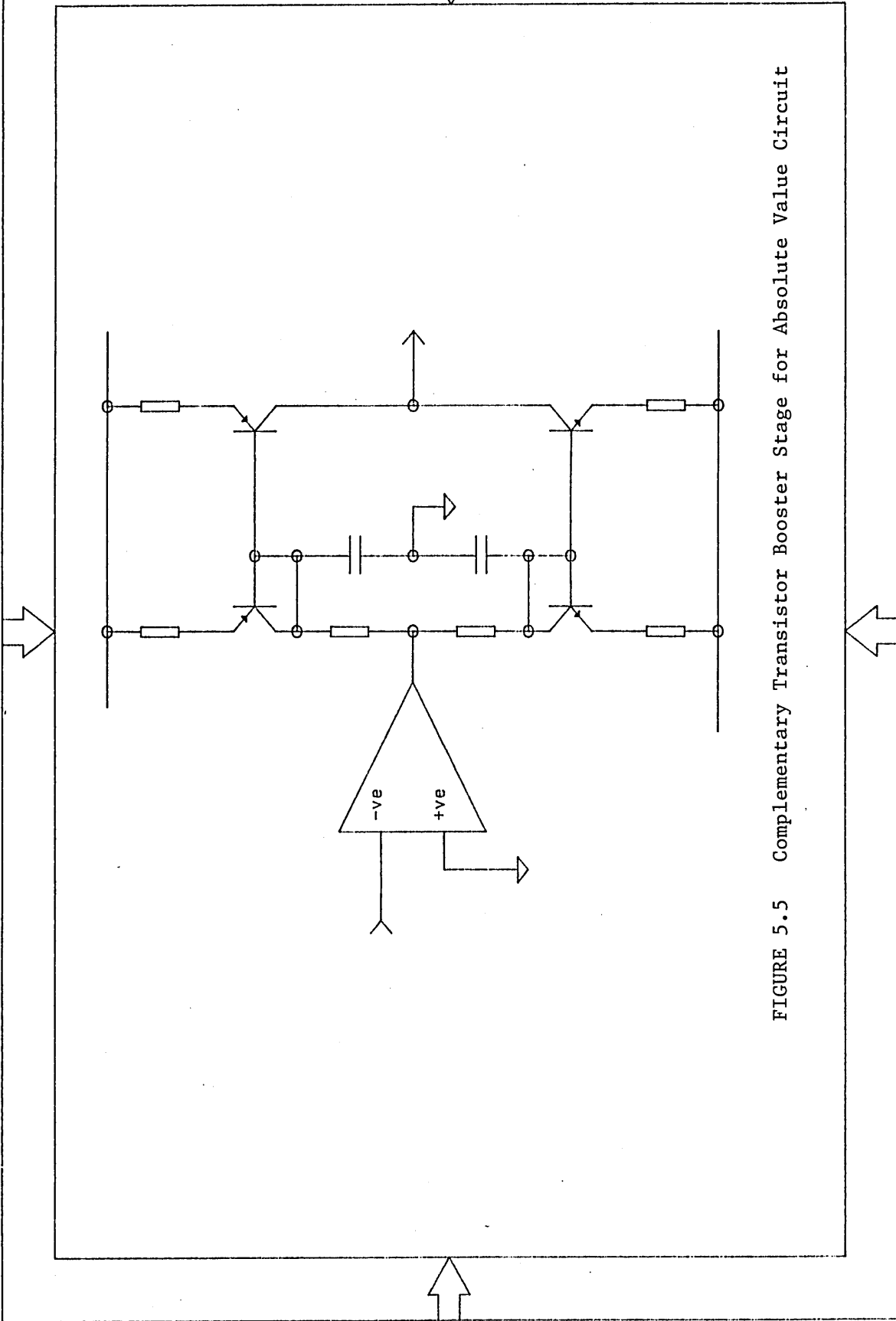


FIGURE 5.5 Complementary Transistor Booster Stage for Absolute Value Circuit

Unfortunately the CA3130 was running very hot as it was drawing 16.5 mA from the power rails, which is far too high for an instrument intended to run from battery power.

Changing the CA3130 to an exotic, that is expensive, Harris 2625 operational amplifier brought the current consumption down to under 5 mA and increased the stability of the circuit. The dynamic range at 2 kHz was now in the region 70 dB to 80 dB depending on how accurately the circuit was set up, and at 20 kHz the dynamic range was in the region 50 dB to 60 dB. One of the problems with the circuit was the phase error introduced. This becomes more apparent if the precision half-wave rectifier is coupled to a second operational amplifier to complete the full-wave rectification.

An application note from National Semiconductor [13] explains how their LM 108A family of operational amplifiers can be given higher gain at high frequencies by using a type of frequency compensation which they term feedforward compensation. The advantage of this type of compensation is that it allows the use of an operational amplifier with a low static current drain, typically 300  $\mu$ A, but increases the standard gain-bandwidth of the operational amplifier by eliminating some relatively slow PNP transistors from the signal chain at high frequencies. At the same time as changing to this amplifier configuration, a number of different diode families were also considered. The most successful family tested was the Hewlett Packard range of hot carrier diodes.

The hot carrier diode is a very close approximation to an ideal diode; it has essentially zero forward voltage drop, an extremely fast reverse recovery time due to the absence of minority carrier charge storage and the only trade-off between different members of

the family is reverse leakage versus forward resistance.

An optimized version of the absolute value circuit is shown in Figure 5.6. An LM 308A was used for A1 and A2 and the hot carrier diodes with the best compromise of parameters to give minimum gain error and maximum dynamic range were the Hewlett Packard 50822835. The amount of feedforward compensation in the final circuit is significantly larger than recommended in the application note, particularly in view of the 20 pF and 3.3 pF speed-up capacitors, but the pulse response of the circuit is not important in this application.

The dynamic range of the optimized circuit was about 90 dB at 6 kHz, falling to about 70 dB at 20 kHz; which is consistent with the performance required for a Type 0 meter, and significantly in excess of other published performance.

## 5.2 The Squaring Circuit

Having converted the input signal to unipolar form with the absolute value circuit, the squaring operation can be performed using the  $2\log V$ -alog stage mentioned in the introduction to the circuit design. The basic circuit is shown in Figure 5.7. The operation of the circuit relies on the logarithmic relationship between collector current and base-emitter voltage of a bipolar junction transistor. In this particular circuit, there are two transistors in the feedback loop of the operational amplifier to give a voltage at the emitter of Q2 which is twice the base-emitter voltage of a single transistor. Figure 5.8 shows the a.c. component of the waveform at this point (CH2) resulting from an

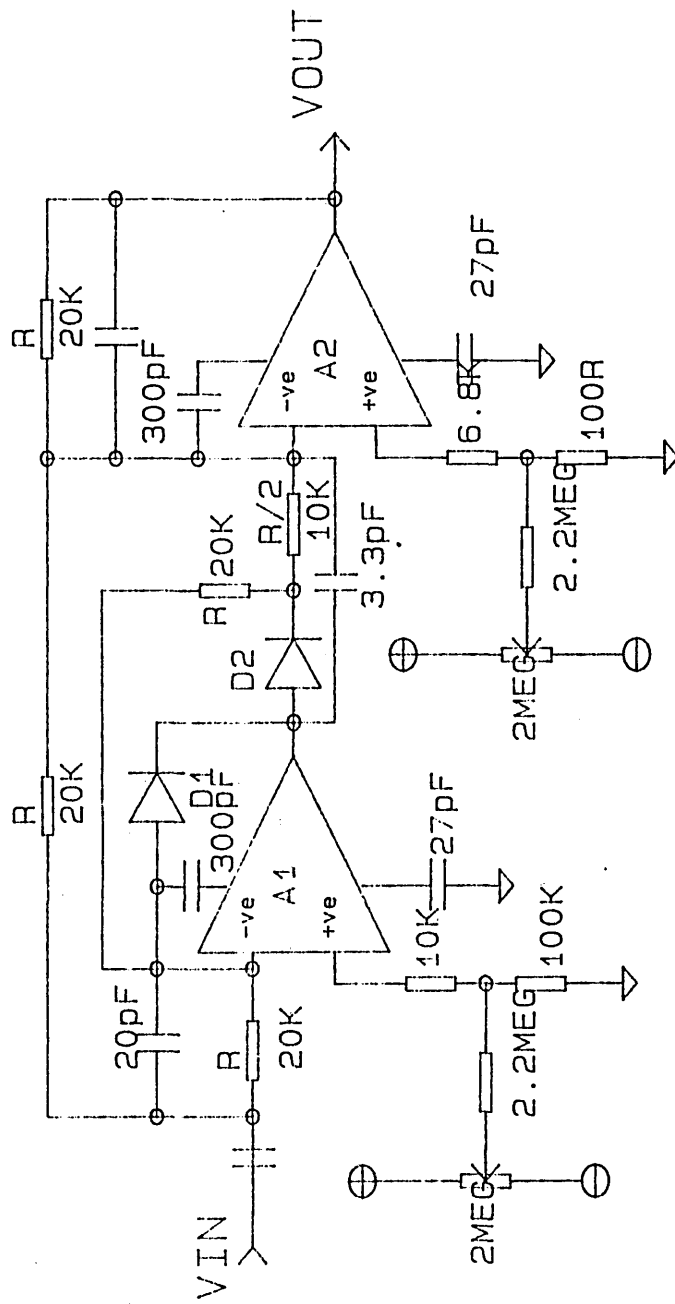


FIGURE 5.6 Optimized Version of Absolute Value Circuit

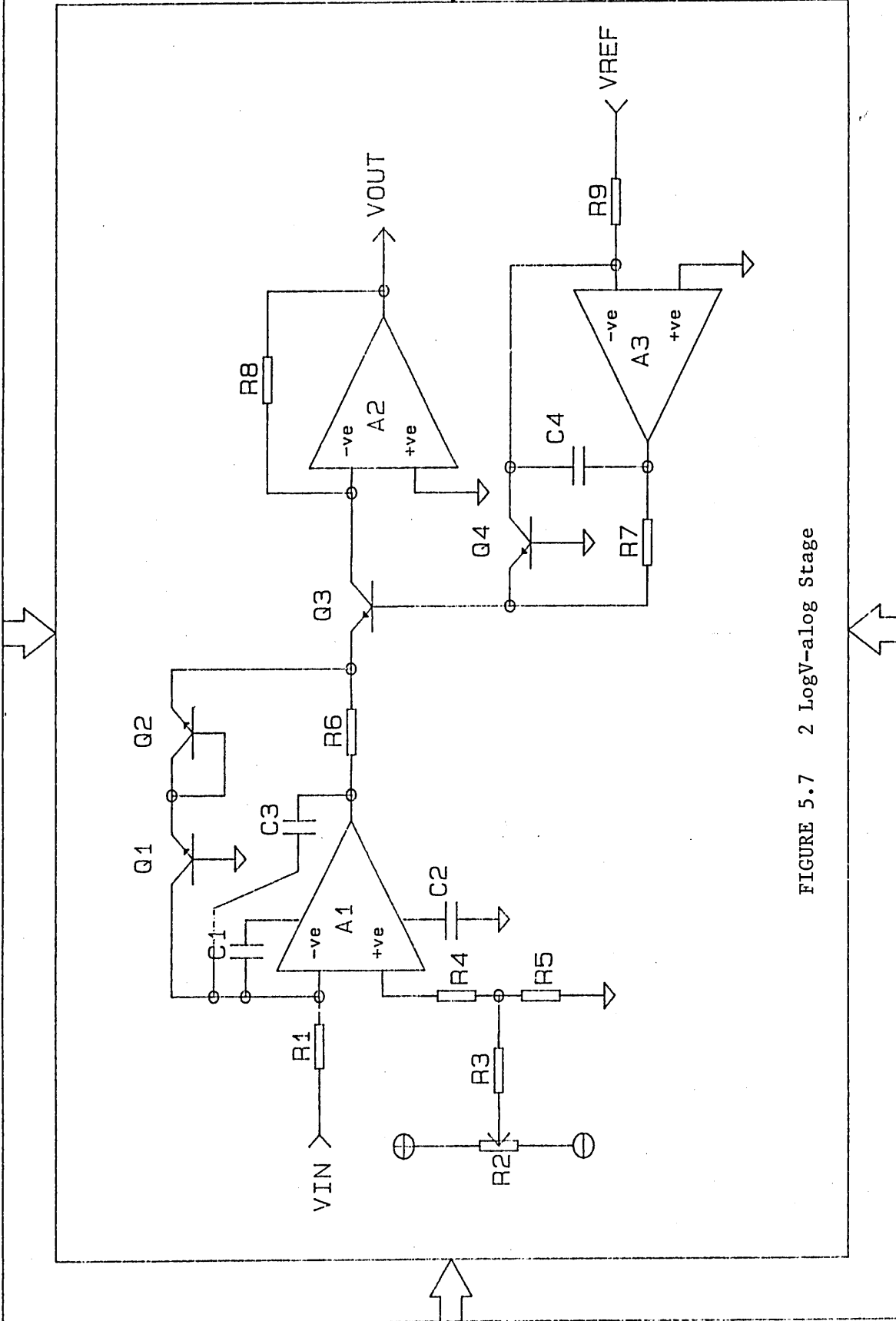


FIGURE 5.7 2 LogV-a-log Stage

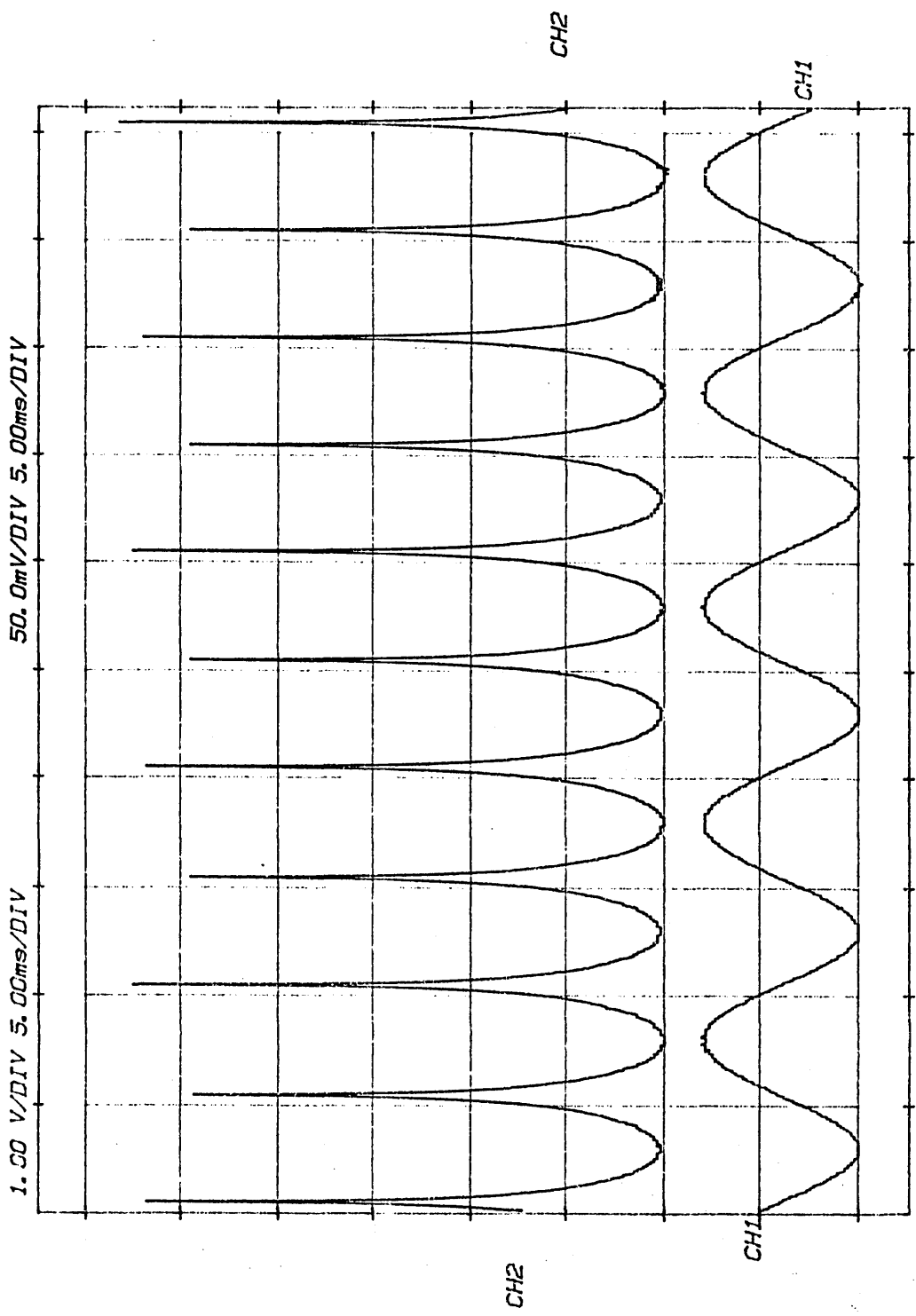


FIGURE 5.8 A.C. Component of 2 log V Signal (CH2) Resulting from Input Signal (CH1)

input signal of 100 Hz (CH1). The current drawn into the antilogging transistor, Q3, is therefore proportional to the square of the current passing through the logging transistors, Q1 and Q2.

A serious problem of logarithmic amplifiers, used to good advantage in semiconductor temperature transducers, is that the relationship between collector current and base-emitter voltage is highly temperature sensitive. This is due to two temperature sensitive components of the characteristics as shown below:

$$v_{be} = \eta V_T (\ln I_C - \ln I_S)$$

where

$v_{be}$  is the base-emitter voltage

$\eta$  is a device constant

$V_T$  is the thermal voltage, given by  $V_T = \frac{kT}{q}$

$k$  is Boltzmann's constant

$T$  is the absolute temperature in kelvin

$q$  is the electronic charge

$I_C$  is the collector current

$I_S$  is the reverse saturation current

There is a temperature sensitive scale factor,  $\eta V_T$ , and a temperature sensitive offset term,  $\eta V_T \ln I_S$ . The offset term is compensated for by feeding a constant current via Q4 and Q3 into A1. Q1-4 are identical types contained in a monolithic transistor array, so the current through Q4 and Q3 will match and thermally track the offset term of Q1 and Q2. The current into the collector of Q3 is therefore the antilogarithm of the combined base-emitter voltages of Q1 and Q2, but with the four offset terms exactly cancelling.

The constant current into Q4 and Q3 determines the scale factor, effectively the base of the logarithm, and the use of a transistor array helps overcome the problems of temperature sensitivity by the close thermal tracking of the devices. Initially, a simple resistor from the positive supply rail was used as the constant current source, but the seven decade range of collector current for Q3 resulted in large gain changes for Q3 which altered the reference current and hence the scale factor. This problem is overcome in the circuit of Figure 5.7 by supplying the reference current to the virtual earth of an operational amplifier so that the reference is stable, and so that any excess base current demands for Q3, as a result of gain changes, can be supplied from A2 without altering the scale factor.

The device selected for A1 was an LM 308A, as it had to overcome the problem of switching the transistors on and off at high frequencies and low signal levels. As in the absolute value circuit, the optimum performance was obtained with frequency compensation well in excess of the standard value. The performance requirements of A2 are that it should have as small an input offset voltage as possible, but more importantly, it should have a low input bias current. Both these requirements are so that the small reference current is not affected. The reference current is of the order of  $1 \mu\text{A}$ , so the input bias current should be significantly less than this, over the full operating temperature range of the  $L_{eq}$  meter. A BIFET operational amplifier type TL062IN from Texas Instruments was selected as it has the lowest input offset voltage over the temperature range, coupled with the low input bias current of a JFET input.



With the circuit of Figure 5.7 coupled to the circuit of Figure 5.6, so that the summing function of A2, Figure 5.6, is replaced by A1, Figure 5.7, the dynamic range for accurate generation of  $2\log V - \log$  was in excess of 70 dB. This refers to the range of input signals, as the range of collector currents was therefore 140 dB or seven decades.

### 5.3 The Dose Integrator

The integral of the square of the sound pressure with respect to time, a measure of the total energy received by the microphone, is usually referred to as the dose. The operating requirements of an  $L_{eq}$  meter intended for use in measuring industrial noise impose stringent requirements on the performance of the dose integrator. These are that the 140 dB range of input currents should be capable of being integrated over a period at least as long as the working day. The two possible extremes of dose are a high level signal occurring for a long period, and a low level signal requiring to be resolved after a short measurement period. The limitation in the former case is the finite capacity of any integrator, and in the latter case it is the problem of ensuring that the integrator output can be resolved with a sufficiently high degree of accuracy. A combination of these extremes, where a high level signal occurs for a short period but the total measurement period is long, demands the use of an integrator with very low leakage and drift.

The linearity of better than 0.1 dB, about 1%, over a wide range of integrator speeds is also required for oscilloscope timebase generators, but typically in this case the input current is used to vary the speed over one decade only with one particular integration

capacitor. In the case of the  $L_{eq}$  meter though, the speed of the integrator is a function of the varying voltage produced by the microphone, and therefore the integrator must be ready to respond at any speed within its capability.

A conventional analogue integrator, consisting of a capacitor in the feedback loop of an operational amplifier, has obvious limitations on its performance, particularly on its ability to integrate a constant current for long periods, due to finite power supply voltages, and in its ability to generate slow ramps with high precision, due to operational amplifier limitations and inevitable leakage currents.

Having constructed an analogue integrator using the latest, low input current operational amplifiers in combination with low leakage capacitors, it became clear that these limitations would preclude the design of an instrument which relied solely on analogue techniques. The development of the logarithmic amplifier, which would be needed as the stage following the integrator to complete the instrument, was postponed, so that attention could be focused on digital techniques for providing the required storage capacity.

## EXTENSION OF THE PERFORMANCE OF THE ANALOGUE INSTRUMENT USING HYBRID TECHNIQUES

The circuits which were developed as part of the analogue instrument programme provided a sound basis for the design of a hybrid  $L_{eq}$  meter. The advantages to be gained by using digital techniques to store the dose information are that large amounts of data can be stored, and that the data is not corrupted so long as the power supply is maintained.

The combination of the digital store with the analogue signal conditioning which precedes it, needs to overcome the limitations of generating a slow ramp with high precision and integrating over long periods. In particular, the digital store should not introduce extra limitations due to quantization errors.

Many of these limitations can be overcome by the use of a novel technique, developed as part of this work, which effectively increases the maximum integration period, or allows a medium speed integrator to generate extremely slow ramps.

One way to overcome the problems of integrator drift and leakage would be to use the integrator as a sweep generator whose sweep speed is determined by the input current. This current to frequency converter would then have to be coupled to a digital store so that the dose information would remain stable so long as the power supply were maintained. To understand the difficulties associated with such a scheme, it is necessary to quantify the operating range of the current to frequency converter. To obtain accurate readings on the  $L_{eq}$  meter at the bottom end of the scale, it is necessary to have the linearity extend to about -5 dB relative to scale zero. If readings are required

in a relatively short period, say 10 seconds, then a minimum of 10 counts would have to have been placed in the digital store to give 10% resolution, about 1 dB. At the top end of the dynamic span, again allowing a 5 dB margin to ensure linearity, the sweep speed would be increased by 70 dB, ie by a factor of  $10^7$ , giving a maximum sweep frequency of 10 MHz. The problems associated with designing a sweep generator to operate over this frequency range would be immense, particularly at the 10 MHz sweep frequency, where the retrace circuitry would have to discharge the integration capacitor in the order of nanoseconds, to minimize the loss of dose information. In the new approach, the advantage of the semi-infinite store of the digital system is coupled with the advantages of a continuous analogue integrator to produce a system with any predetermined capacity, but which has a completely continuous output.

For an instrument with a 60 dB dynamic span, the variation in integrator speeds is in the ratio  $10^6:1$ , however about an extra order of magnitude is required in the design of such an integrator to ensure linearity at the extremes of the range, and to allow for tolerance in components and other practical considerations. The maximum current which the integrator of a battery powered instrument can be expected to operate at is of the order of milliamps. This places the bottom end of the range in the nanoamp region. To make a practical integrator using an operational amplifier, the input bias current must be an order of magnitude lower than this; which therefore suggests the use of a FET input operational amplifier.

Due to finite power supply voltage available, the integrator has a finite maximum integration time. Once the upper limit for current has been set, the maximum integration time is a function of the value of the

capacitor only. The dielectric leakage of the capacitor must be less than the input bias current of the operational amplifier in order to realize the full potential of the integrator. If a maximum integrator of 9 volts is assumed, the leakage resistance of the capacitor must at least be of the order of  $10^{12}$  ohms. This puts an upper limit on the value of the integrator capacitor which can be used in practice. Typically, a polystyrene or teflon capacitor of about  $0.47 \mu\text{F}$  is used. With the maximum current set at 1 mA, a maximum integrator output voltage of 9 volts and an integrator capacitor of  $0.47 \mu\text{F}$ , the maximum integration period works out to be about 4 milliseconds, using  $CV=IT$ . Clearly this is nowhere near long enough for use as the sole means of integration in an  $L_{\text{eq}}$  meter, where a maximum integration period of 8 hours would be more typical. Provision has therefore been made in the integrator design to reset the integrator when the output reaches a present threshold. Each time the integrator is reset, a shift register is incremented so that no information is lost; each count corresponding to an identical value of energy having been stored on the capacitor.

If the conditions at the other extreme of the input range are considered, where the input current is  $10^6$  times smaller, the maximum integration period works out as 4000 seconds, or about 1.1 hours. Even if no readings were required from the  $L_{\text{eq}}$  meter with a continuous bottom scale input before the end of an 8 hour measurement period, there would only be seven counts in the shift register, which corresponds to an uncertainty in the final answer of about 8 dB. Means must therefore be provided to use the information from the integrator and the shift register so that accurate readings can be obtained within periods short in comparison with 8 hours. It is in the method of combination of these data which improves on the conventional integrator alone or on a current to frequency converter and shift register where only data from the shift

register is used. The section of the instrument which performs the necessary combination and equalization is called the auto-ranging ladder network.

### 6.1 Auto-ranging Ladder Network

The information stored in the shift register is stable so long as the power supply is maintained and there is no breakthrough from other circuits. Therefore, when a significant number of counts have been incremented into the shift register, drift on the integrator can largely be ignored. It is the function of the auto-ranging ladder network to optimize the output from the shift register so that the information from the integrator can be utilized, but so that when sufficient counts have been accumulated in the shift register, the variation in output due to integrator drift is minimized. When decoding purely digital information into analogue form, the most common system employed is an R-2R ladder network. The advantage of such a ladder network is that the R-2R network uses only two values of resistance, whereas the values of the binary weighted resistor network vary over a very wide range, making matching and tracking very difficult. The price paid for using the R-2R ladder network is that it requires twice as many resistors for a given number of bits in the network.

The operation of the conventional R-2R ladder network is based on the current into each bit on the ladder splitting equally, half going towards the output of the ladder and half going towards the base of the ladder. This current splitting is repeated at every node where a new bit on the ladder joins, and gives the correct weighting to each bit on the ladder.

Since the least significant bit (LSB) on the ladder is equivalent to the integrator capacitor being completely charged, any method of combining the shift register output and the output from the integrator must maintain this equivalence. It can be seen by reference to Figure 6.1, that both ends of the ladder network are terminated by  $2R$  resistors, one end to ground and the other to the virtual earth of the operational amplifier. If the  $2R$  resistor terminating the ladder to ground is connected to a low impedance point having a voltage which is completely variable between 0 and  $+V_{ref}$ , then it can be shown that the output of the operational amplifier can be continuously varied between 0 and  $+V_{ref}$ , using this low impedance voltage source and the bits of the ladder network. Further, it is clear that there is no detectable difference in operational amplifier output between having the low impedance voltage at  $+V_{ref}$  with the LSB off, or having the low impedance voltage source at ground with the LSB on.

Referring to Figure 6.2, with the low impedance voltage source  $V$  such that  $0 \leq V \leq V_{ref}$  and all the ladder bits off, the voltage at node  $n$  is:

$$V_{\text{node } n} = V \cdot \frac{1}{3}$$

Since the impedance looking down the ladder or towards the LSB switch is  $2R$ . The voltage at node 1 is:

$$V_{\text{node } 1} = V \cdot \frac{1}{3} \cdot \frac{1}{2^{n-1}}$$

Hence the output voltage is:

$$V_{\text{out}} = V \cdot \frac{1}{3} \cdot \frac{1}{2^{n-1}} \cdot 3 = V \cdot \frac{1}{2^n}$$

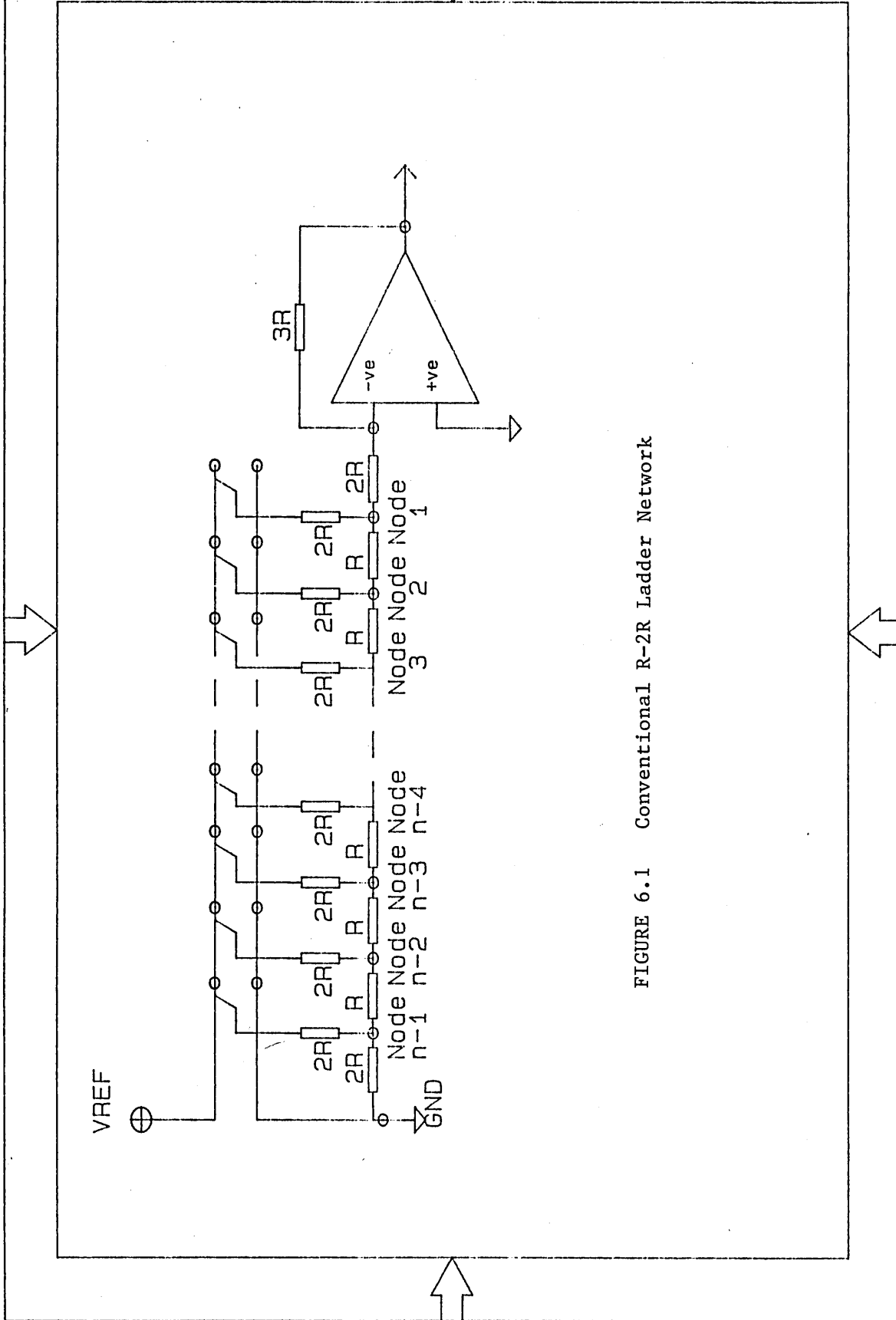


FIGURE 6.1 Conventional R-2R Ladder Network



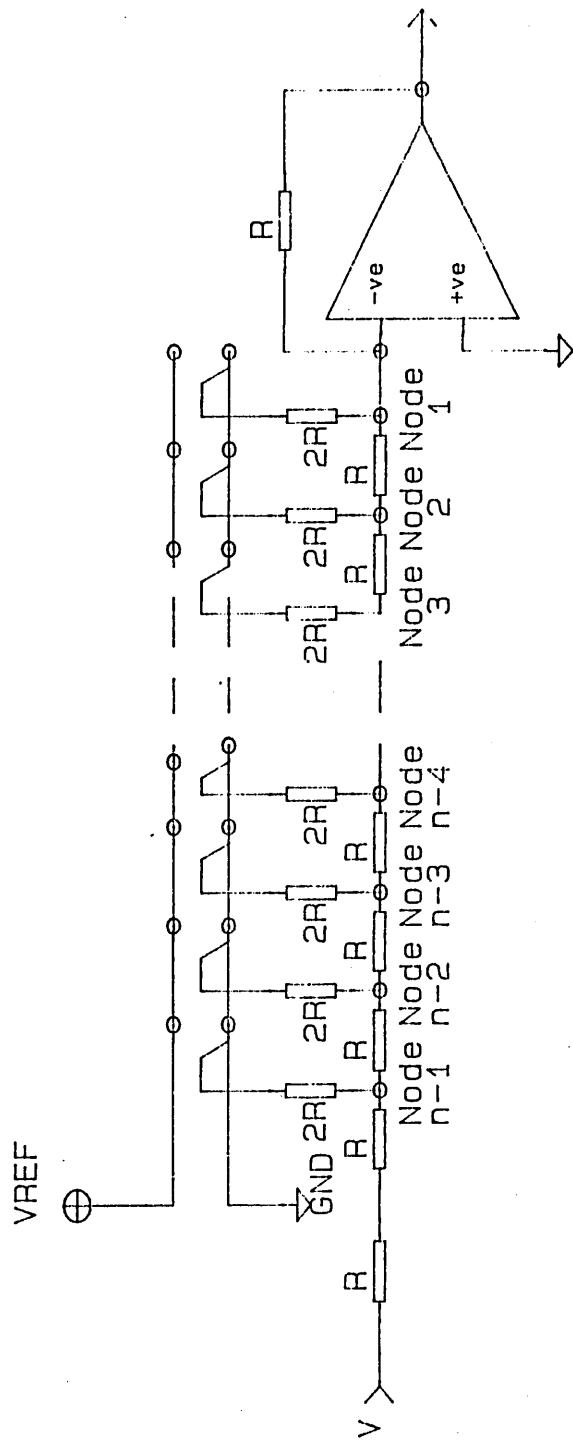


FIGURE 6.2 Modified Ladder Network with All Shift Register Bits at 0 Volts

Therefore the low impedance voltage source has the same weight as the LSB. As the integrator ramps up, is reset and the shift register incremented, the output of the operational amplifier increases monotonically and linearly as though the limitations of the integrator were increased by a factor  $2^B$ , where B is the number of bits in the ladder.

The dynamic range of current from the ladder network is a function of the number of bits in the ladder and the required resolution of the analogue integrator's output. Typically, in a system where the extension of the analogue integrator is to be used to best advantage, this range of current will be large. It is likely that any stage which follows the ladder network will have an input signal dynamic range capability which is significantly less than the dynamic range which the integrator and shift register can produce. This mismatch problem can be overcome by restricting the range of current from the ladder to that which the following stage is capable of handling, and then compensating at a later stage.

The modifications required to be able to control the current from the ladder involves a fundamental change to the way in which the current is taken from the ladder. The  $2R$  resistor which connected the ladder to the virtual earth of the operational amplifier is omitted, and to keep the output voltage as before, the  $3R$  amplifier feedback resistor is changed to  $R$ . The ladder network is no longer symmetrical, so it is necessary to demonstrate that this arrangement will work.

With the MSB high and all the other bits low, the output voltage is as previously:

$$V_{\text{out}} = V_{\text{ref}} \cdot \frac{R}{2R} = \frac{V_{\text{ref}}}{2}$$

The other resistors connected to the virtual earth have no effect as they are all connected to zero volts at their other ends. With the second MSB high and the rest low, the voltage at node 2 (Figure 6.3) will be:

$$V_{\text{node 2}} = V_{\text{ref}} \cdot \frac{2}{3} \cdot \frac{3}{8} = \frac{V_{\text{ref}}}{4}$$

since the impedance to the left of the node 2 remains  $2R$  and the parallel combination of  $R$  and  $2R$  is  $\frac{2R}{3}$ . The gain of the amplifier from node 2 is unity, so the output voltage is  $\frac{V_{\text{ref}}}{4}$  as before.

With the third MSB high and the rest low, the voltage at node 3 will be as shown in Figure 6.4. The impedance from node 2 to ground is  $\frac{2R}{3}$  and the impedance from node 3 to ground is  $2R // \frac{5R}{3} = \frac{10R}{11}$ . The voltage at node 3 is:

$$V_{\text{node 3}} = V_{\text{ref}} \cdot \frac{10}{32} = V_{\text{ref}} \cdot \frac{5}{16}$$

The voltage at node 2 is:

$$V_{\text{node 2}} = V_{\text{ref}} \cdot \frac{5}{16} \cdot \frac{2}{3} \cdot \frac{3}{5} = \frac{V_{\text{ref}}}{8}$$

The gain of the amplifier from node 2 is unity, therefore the output voltage is:

$$V_{\text{out}} = \frac{V_{\text{ref}}}{8}$$

The process can be continued to show that each bit on the ladder has exactly the same weighting as before.

An incidental advantage of using the R-2R ladder network in this way is that it is more electrically efficient. The proportion of current reaching the output of the ladder from a given bit is

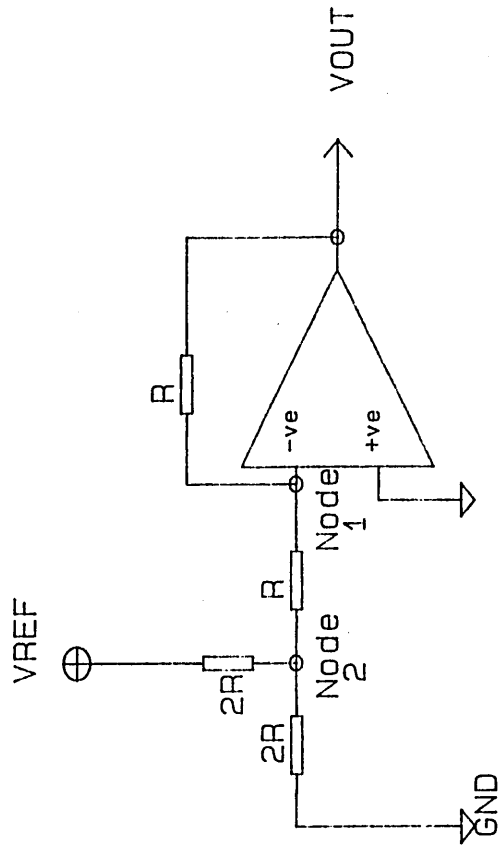


FIGURE 6.3 Equivalent Circuit of Ladder Network with Second MSB High and the Rest Low

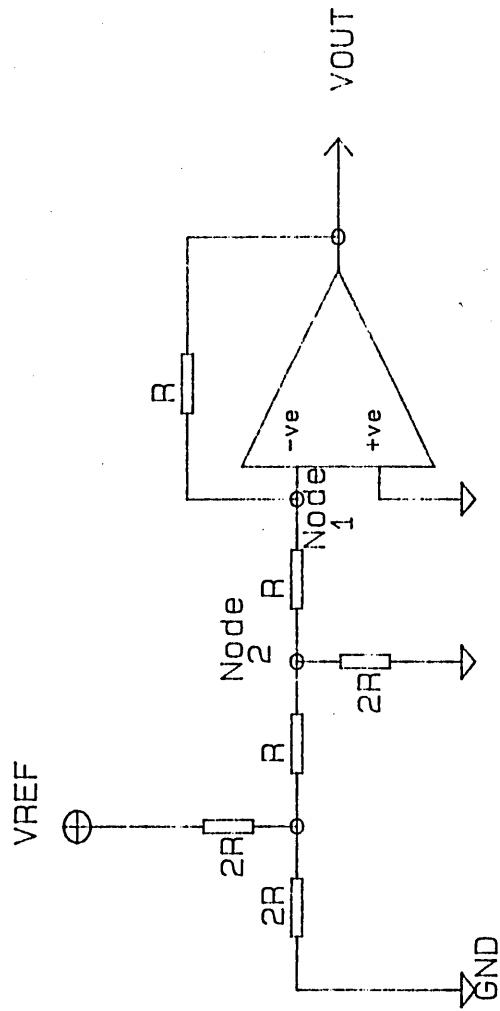


FIGURE 6.4 Equivalent Circuit of Ladder Network with Third MSB High and the Rest Low

always higher with this modified ladder; with the MSB high alone, 100% of the current arrives at the output, compared with 50% for the conventional arrangement.

The main advantage of this modified arrangement, however, is that any of the nodes on the ladder can be used as the output, so long as all the bits higher up the ladder than the output node are low. As long as this criterion is maintained, for every node that the output is moved down the ladder, the output current is doubled. Moving five bits down the ladder leads to an increase in output current of  $2^5$ , about 30 dB.

The value for R is chosen so that the maximum current from the ladder, twice that due to the MSB alone, is equal to the upper limit of input to the following stage, assuming that current consumption limitations are not imposed. In order to minimize the number of taps on the ladder, to simplify the control circuitry, the positions of the taps are chosen so that the change in magnification between successive taps corresponds to just less than the dynamic range of the following stage.

The maximum amplification possible is when the analogue integrator is used as a tap. In this case, the node where the integrator couples to the ladder will not give the correct current; it will in fact give half that required. To obtain the correct current, the feed could be taken direct from the integrator's low impedance output via a resistor of value R. A more efficient approach would be to split the  $2R$  resistor which couples the integrator to the ladder into two separate resistors of value R. The tap corresponding to using the integrator alone would therefore be the

midpoint of these resistors. A further advantage would be that if a monolithic resistor pack of the ladder network were made, to ensure good matching and thermal tracking of the resistors, a tap in this position would also serve as the connection point for cascading several networks together.

To optimize the current from the ladder, the tap giving the highest amplification is selected until a bit beyond the tap in use goes high, at which point the next higher tap is selected, and so on until the shift register is full. Such control can be performed using fairly simple logic and switching.

The way in which the excess gain compensation is applied is completely dependent upon the type of stage which follows the enhanced integrator. If the stage following the enhanced integrator is a logarithmic amplifier, as it is in an  $L_{eq}$  meter, the auto-ranging system is easiest to implement and is most use. The auto-ranging circuitry helps optimize the large dynamic range of the integrator for the logarithmic amplifier's relatively small dynamic range, and the magnification of the input current to the logarithmic amplifier causes a simple level shift in the output which is easy to compensate. The situation is even better when calculating a parameter such as  $L_{eq}$ , which is derived from two signals only, dose and time, which affect the computed parameter in opposite senses. In these cases it is possible to arrange for two ladder networks to switch synchronously so that no further compensation is required. The tap on the ladders being used would be determined by the shift register with the largest accumulated count.

## 6.2 Elapsed Time Integrator

The elapsed time is required as an analogue signal, so the most obvious way to measure it is to employ the same integrator and shift register combination as used in the dose integrator. The input to the integrator is a constant current whose value can alter the scale of the final  $L_{eq}$ , but, since such a facility already exists by using the reference current to the antilogarithm stage, all that is required of the elapsed time integrator is that the ramp speed should be stable. The value for the constant current and the size of the capacitor are chosen so as to minimize leakage and offset errors and drift.

## 6.3 The Log-ratio Circuit & the Auto-ranging Output Circuit

The dose and time information are available as continuous analogue signals, so  $L_{eq}$  can be computed by taking the logarithm of dose divided by time. It is usual to do division of analogue signals by taking the logarithm of each signal, subtracting one from the other and then antilogging the result. Since  $L_{eq}$  is specified on a logarithmic scale, the antilogging can be omitted, and the difference between the log of the two integrals is  $L_{eq}$ .

In all published application notes for log-ratio circuits, the function is generated explicitly and serially, as above. A new approach has been devised as part of this project, in which instead of feeding each signal into its own logarithmic amplifier, each with a separate reference current, the two signals are fed into opposite sides of the same logarithmic amplifier, as shown in Figure 6.5. The reference current normally supplied to one input is replaced by one of the signals, so that the logarithm of the



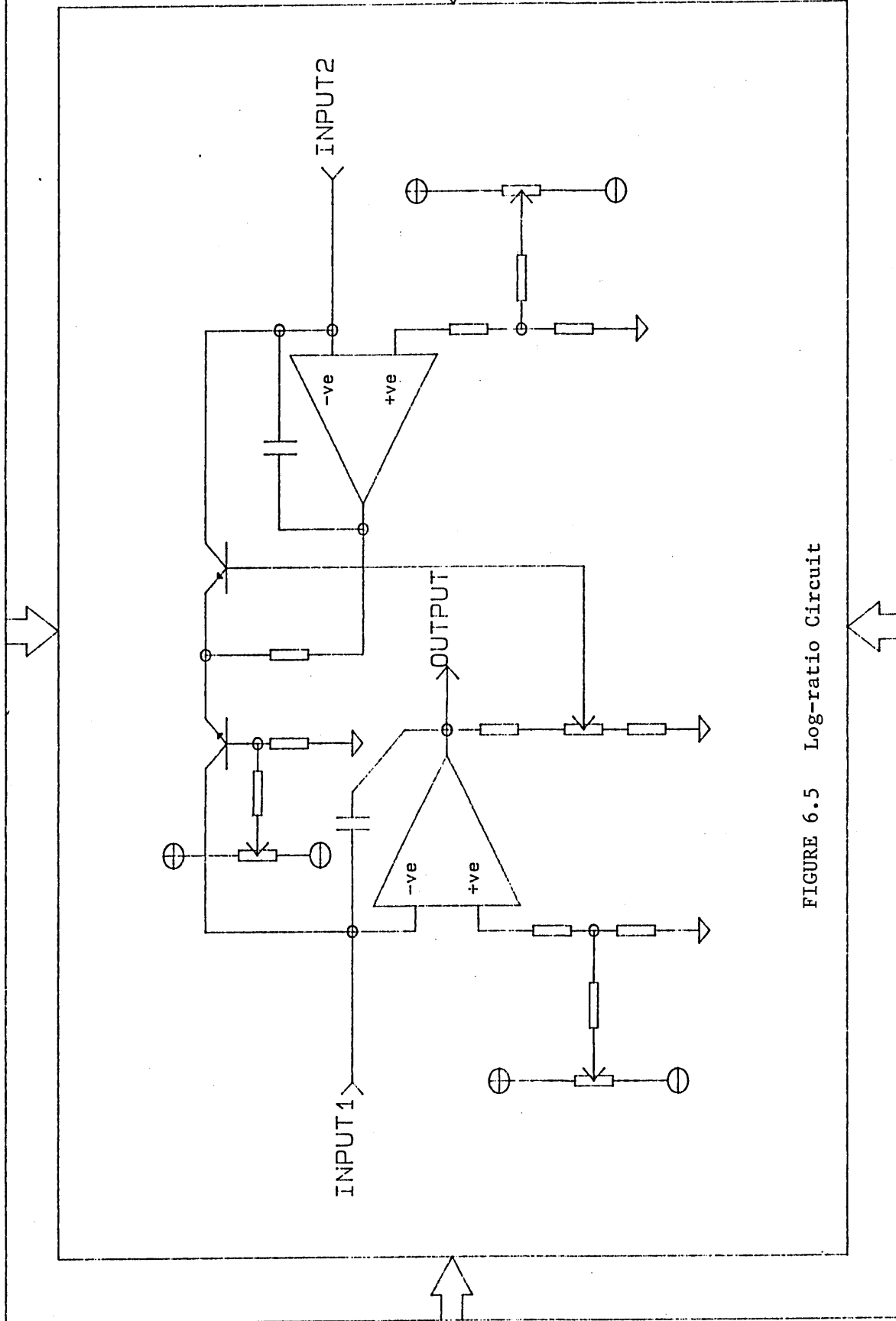


FIGURE 6.5 Log-ratio Circuit

other signal has a varying reference. The range of input signals which this modified log-ratio circuit can accept is about double (the number of dB) which the basic circuit can accept. A table of the results of a test on the log-ratio circuit of Figure 6.5 is shown in Table 6.1. With both inputs allowed to move over their extreme ranges, a dynamic range for the log-ratio circuit of 150 dB is obtained.

The auto-ranging control circuitry optimizes the current into the logarithmic amplifier so that it is operating with as high an input current as possible. The control circuitry performs this function by selecting the appropriate tap on the ladder network, such that the maximum output current is available but so that each bit on the ladder network maintains its correct weighting. The necessary algorithm is discussed in the section on the auto-ranging ladder network.

The optimized output of the logarithmic amplifier represents the correctly scaled value of  $L_{eq}$ , so that a conventional voltmeter can be used as the display device.

The performance of the hybrid ISLM is summarized in the Institute of Acoustics paper which is contained within Appendix D. The hybrid instrument shows an improvement over other commercially available instruments and demonstrates that a precision grade instrument, as defined in the draft standard, can be produced.

Left/dB	Right/dB	Output/Volts	Error/dB
0	0	0.001	+0.02
0	-10	-0.498	+0.04
0	-20	-1.000	0.0
0	-30	-1.502	-0.04
0	-40	-2.003	-0.06
0	-50	-2.507	-0.14
0	-60	-3.010	-0.20
0	-70	-3.518	-0.36
0	0	0.001	+0.02
-10	0	0.498	-0.04
-20	0	1.000	0.0
-30	0	1.501	+0.02
-40	0	2.002	+0.04
-50	0	2.504	+0.08
-60	0	3.005	+0.10
-70	0	3.501	+0.02
-80	0	3.980	-0.40

TABLE 6.1 Log-ratio Circuit Performance

**MICROPROCESSOR BASED INTEGRATING SOUND LEVEL METER**

The previous chapters highlighted the analogue and hybrid instrument development and showed how discrete stages were developed and evaluated. This basis was necessary for the development of a complete microprocessor-based instrument. This chapter describes development and evaluation of the integrating sound level meter and shows that it is feasible to design a microprocessor-based instrument with enhanced capabilities. As with the hybrid instrument, the performance of the constituent elements can be optimized to meet a wide variety of demanding design criteria.

**7.1 Background Design Considerations**

The problems of designing an analogue ISLM are that a totally digital solution based on microprocessor technology represents an impractical approach. This is evident by considering that to perform A-D conversion on the input signal requires about 19 or 20 bit resolution on the converter. Even if it were possible to perform the required accuracy of conversion in a short enough period, the subsequent processing of such a large digital word is beyond the scope of those current microprocessors which can be considered for inclusion in a hand-held integrating sound level meter. This is exacerbated by the further requirement to square the input signal.

Having assessed and rejected the approach involving direct conversion of the input signal, it was necessary to consider where to incorporate the microprocessor in the integrating sound level

meter such that it could offer performance improvements over the hybrid instrument. Although the performance of the hybrid ISLM is capable of meeting the envisaged precision grade standard, it has limitations in the possible loss of dose information during integrator switchback and in the possible drift in the logarithmic amplifiers at extreme temperatures. A further advantage to accrue, if this latter stage were replaced by a microprocessor system, would be the elimination of the time consuming setting up procedure which is required to obtain optimum performance from the logarithmic amplifiers. The microprocessor should therefore be responsible for the signal processing after the proven  $2\log V$ -alog circuit, which was developed as part of the analogue  $L_{eq}$  meter.

To feed a signal proportional to the square of the microphone voltage into the microprocessor involves some form of analogue to digital conversion. Several digitizing techniques were considered; each requiring some form of integration to condition the signal.

A straight adaptation of the analogue integrator with switchback circuit would lead to a current to frequency converter. Neither the precision and linearity of the ramp, nor the possible delay in switchback, would detract from the performance of such a converter, so long as the current to frequency relationship were linear. As with the hybrid system, each count would represent a quantum of dose, so the total count fed into the  $L_{eq}$  meter would represent the total dose. The disadvantage of such a system would be that in order to achieve sufficient resolution of a low level input after a short period, the integrator would have to operate over a range of about 10 Hz to 10 MHz (60 dB). As the typical instruction cycle time of currently available microprocessors is greater than 1  $\mu$ S,

it was clear that such a current to frequency converter was not a viable solution.

A further development of the current to frequency converter system would be to operate the converter at a much slower speed and use an A-D converter to resolve the actual voltage of the ramp when required for calculation purposes. This would be essentially the same as the hybrid ISLM system, but with the microprocessor taking over the function of the special R-2R ladder network and the auto-ranging circuitry. Although the possible drift problems of the logarithmic amplifiers would be overcome by this arrangement, it would reintroduce problems associated with switchback of the integrator and would need a relatively complex hardware and software configuration.

The solution which was finally adopted for incorporating the microprocessor into the ISLM was again based on the original analogue integrator. Instead of switching back the integrator after the output has reached a preset level, as in the hybrid ISLM, the microprocessor is used to implement a charge-balancing algorithm. The advantage of charge-balancing is that there is no loss of dose information so long as the integrator output does not saturate, ie ensuring that the inverting input of the integrator remains at a virtual earth.

## 7.2 Outline Strategy for the Instrument

The digital accumulation of dose information, which in the hybrid ISLM was represented by the number of times the integrator had been reset, is performed by the microprocessor counting how many discrete quanta of charge it has injected into the integrator to

restore the balance conditions. The microprocessor has to perform a relatively simple control function and requires only simple interfacing between itself and the integrator.

The quantum of charge is determined by the microprocessor switching on a constant current source for a preset period. To get adequate resolution of a low level signal after a short period suggests that either the current source is small or the on period is short. This is contrary to the requirement of a much larger quantum needed to balance high level signals occurring over long periods. To cover this range of requirements, but without reintroducing the dynamic range problems of the current to frequency converter, two or more constant current sources have been used. The ratio between the currents was chosen to be  $2^6$  as this makes the dose register structure relatively simple. To fulfil commercial requirements of the collaborating body, the initial microprocessor-based instrument was designed to meet an industrial grade specification. Although this would initially preclude direct comparison with the precision grade hybrid instrument, it offered the challenge of optimizing the analogue stages against a different set of criteria. It soon became evident that the overall system performance was strongly influenced by the analogue stages and therefore the software developed for an industrial grade ISLM would be easily adaptable to more stringent requirements at a later date. The particular requirement was for an educational instrument, an application of particular interest to the author.

For the industrial grade meter, the dose register consists of a three-byte word. The major task of the ISLM is now to process this word by dividing by the elapsed time and taking the logarithm. The

problem of taking the logarithm of a three-byte (or greater) word is the more demanding of the two problems, as the division can be implemented by subtracting the logarithms of the two quantities.

Logarithmic conversion would not normally be attempted on an 8-bit microprocessor single chip system, as there is insufficient processing power to perform the power series approximations usually employed. An algorithm has been developed as part of this work for performing logarithmic conversion within the single-chip microprocessor. The technique has not been seen elsewhere by the author or the supervisors, but the method is powerful and should find many applications in signal processing where it is necessary to compress or expand an M byte word into an N byte word logarithmically.

In the particular application of the industrial grade meter, it is necessary to compress a possible three byte word into a single byte. The algorithm relies on the equivalence of rotating a bit pattern to left and multiplying by two. This results in an offset addition or subtraction to the final logarithm. The particular bit pattern that exists is rotated left until it is fully left hand justified. The most significant eight bits are then used to form the address for a look-up table. The resultant logarithm is adjusted to account for the number of non-zero bytes and the number of rotations performed. The look-up table only needs to contain 128 values, corresponding to addresses  $80_{16}$  to  $FF_{16}$ .

Having acquired the logarithm of both dose and time, and having subtracted the logarithm of the elapsed time from that of dose, it is a simple matter to make the result available on an output port



so that a suitable display device can be driven.

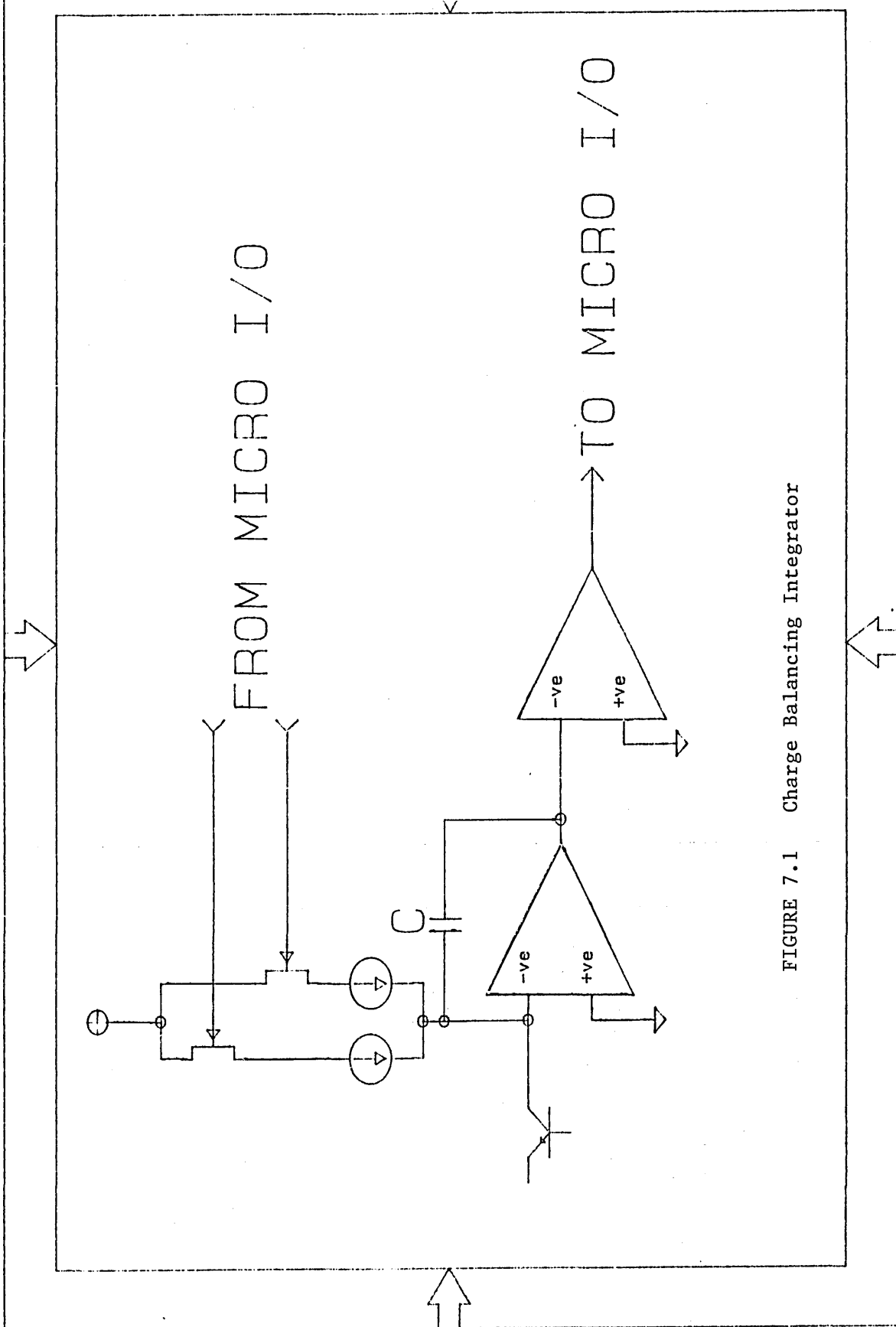
### 7.3 Detailed Circuit Description

The front end of the instrument, ranging, weighting and gain stages including the generation of  $2 \log V$  are derived from those of the hybrid ISLM. The subsequent antilogarithmic stage is similar but unswitched and the units diverge at the integrator. In the microprocessor-based instrument a charge-balancing integrator is used.

#### 7.3.1 Charge Balancing Integrator

The output current from the antilog transistor emitter is fed into the summing junction of the charge-balancing integrator, Figure 7.1. This integrator is essentially the same as that used in the hybrid instrument, but is not based on the principle of allowing the voltage across the integration capacitor 'C', Figure 7.1, to build up to a finite value before switching back the integrator. Instead the action of the antilog transistor current, which is attempting to ramp the output of the integrator in a positive direction, is balanced by a switched constant current, under the control of a microprocessor, which acts in the opposite sense so as to maintain the integrator output as near zero volts as possible.

The critical parameters affecting the performance of the circuit are: the input bias current of the operational amplifier, the leakage current of the antilog transistor, the printed circuit board leakage, the leakage of the capacitor, the size of the capacitor and hence the range of



the input currents. The offset voltage of the operational amplifier is not particularly important as the integrator will centre on the offset voltage instead of absolute zero. The range of values for the critical parameters can be best determined by considering the equivalent ramp speed which the hybrid instrument integrator would operate at so that the "reservoir" capacity of the charge balancing integrator can be calculated. Knowing that the microprocessor which controls the switched constant current into the integrator is also sampling the sound level for the  $L_{10}$  and  $L_{90}$  computation, and that a reasonable sampling rate to capture the FAST response would be of the order of 10 ms, it seems sensible to choose the fastest equivalent ramp speed to be 10 ms also. This implies that if the  $L_{10}/L_{90}$  data acquisition can be done in a time which is short in comparison with the 10 ms sampling rate, the magnitude of switched constant current will be approximately the same as the maximum current from the antilog transistor.

Having made a decision on the maximum current it is worthwhile trying typical values for the power supply voltage rail and the integration capacitor size to determine whether this decision leads to any inconsistencies. If the operational amplifier of the integrator is constrained within the usual +5 V supply for the microprocessor, and the largest practical capacitor size of 0.47  $\mu\text{F}$  is chosen, the maximum current can be worked out from  $I = \frac{CV}{T}$ . Substituting in the values gives  $I = 235 \mu\text{A}$ .

As the dynamic range of the ISLM was to be 40 dB and as the

voltage from the microphone is squared before being fed into the integrator as a current, the input current to the integrator corresponding to the bottom of the dynamic span must therefore be  $235 \mu\text{A} \times 10^{-4}$  ie 23.5 nA. The algebraic sum of all the errors previously mentioned must therefore be less than this, preferably by about one order.

The capacitor leakage problem is relatively small as a result of the balancing technique used; if the capacitor has no voltage across it, there can be no leakage current. However, taking the worst case of 5 volts across the capacitor and the worst case insulation resistance of  $10^{10} \Omega$ , still only gives a leakage of 500 pA. An examination of operational amplifier data sheets reveals that devices are available with picoamp input bias currents at a reasonable cost combined with fairly modest power consumptions. If the printed circuit board leakage is reduced to minimal levels by careful layout, the only remaining critical parameter is that of antilog transistor leakage current. In the CRL 2.22, an industrial grade variant of the hybrid design, the transistors used in the absolute value and 2log-alog stages have a typical leakage of 2 nA. This is within the range determined by setting the capacitor size, the range of currents and so on. If the antilog transistor leakage current did prove to be a problem, then the range of input currents could be shifted upwards without exceeding the maximum current for the transistor. The main detrimental effect of such an action would be to increase current consumption and therefore

decrease the battery life of the instrument.

A comparator connected to the output of the integrator operational amplifier and to the zero volts line detects whether the integrator output is positive or negative and signals this to the microprocessor so that it may modify its control of the switched constant current appropriately. There are no particularly critical parameters; the offset voltage of the comparator has the same effect as the offset voltage of the integrator operational amplifier, so that the integrator will actually balance at a voltage equal to the algebraic sum of the two offsets. As with any comparator, the device must be capable of coming out of saturation at a reasonable speed, but there is no particularly stringent performance requirements.

The control for this integrator can therefore be effected with only two parts of the microprocessor; one to receive data from the comparator and one to send instructions to the constant current switch. If the microprocessor records how much charge it has injected into the integrator summing junction to restore the balance condition, this will be a measure of the dose received by the microphone. By measuring the time in which this dose was received, a value for  $L_{eq}$  can be computed.

#### 7.4 Microprocessor Control Strategy

The microprocessor has several functions to perform:

- 1 Acquisition of the sound level time history for the  $L_{10}/L_{90}$

computation.

- 2 Control of the charge-balancing integrator and the recording of dose.
- 3 Calculation of  $L_{eq}$ .
- 4 Calculation of  $L_{10}/L_{90}$ .

In view of the particular educational application, it was considered preferable to be able to measure  $L_{eq}$  and  $L_{10}/L_{90}$  from the same data. This implies that the microprocessor would have to acquire sound level and dose data simultaneously. Estimates of likely software processing cycles showed that this was possible and that the  $L_{eq}$  calculation could be updated constantly. However, in order to execute a large number of statements in a given period necessitates increasing the microprocessor operating frequency and hence increase the current consumption. It was therefore not considered important to attempt any  $L_{10}/L_{90}$  computation until the end of the measurement period.

During the measurement period, the microprocessor is in a program loop where it acquires a value of sound level, spends a predetermined period balancing the integrator and accumulating dose data, makes a calculation of the current  $L_{eq}$  value and then outputs this value. At the end of the measurement period, the microprocessor calculates the values of  $L_{10}$  and  $L_{90}$  and stores them.

#### 7.4.1 Sound Level Time History Recording

The dc logged output from the standard sound level meter circuitry is digitized and fed into the microprocessor. An 8-bit I/O port is used to feed a byte from the microprocessor through an R-2R ladder network and one to one

input of a comparator. The other comparator input is fed with the dc logged sound level signal and its output is fed back to the microprocessor. The comparator output signal is detected by the microprocessor which implements either a counter ramp or successive approximation technique to perform the A-D conversion. The advantages of using the microprocessor's I/O ports to perform the D-A conversion directly and feed the comparator, are that the chip count and hence the current consumption are kept small. The conversion time is minimized because the final value is always in a microprocessor register when the conversion is complete.

#### 7.4.2 Dose Data Recording

To optimize the dynamic range of the  $L_{eq}$  calculation it is important that the microprocessor spends a large proportion of its time controlling the charge-balancing integrator. It is equally important that a full scale input would generate a large amount of data over the full measurement period so that if a signal corresponding to the bottom of the range is fed in to the meter, it will be capable of generating enough data to allow the  $L_{eq}$  calculation to be made reasonably accurately after a short period.

In controlling the integrator, the microprocessor must repeatedly test the state of the comparator until it detects that an input to the integrator has caused the output to ramp in a positive direction. When such a signal has been received, the microprocessor enables the switched constant current to cause the integrator to ramp back towards zero.

The microprocessor must retest the state of the comparator until the signal is received indicating to the microprocessor that the integrator output is zero, or very slightly negative. The time between testing and retesting the state of the comparator, when the current is enabled, corresponds to a quantum of dose. For each quantum of dose, the contents of a register are incremented. A further register, which records elapsed time since the reset button was last pressed and hence determines the measurement period, is used in conjunction with this dose register to compute  $L_{eq}$ . The size of dose register required can be determined by considering the condition of minimum output to the integrator, combined with the requirement for a reliable answer in a short time, say 10 seconds. To get within  $\pm 1$  dB of the final answer, one needs at least 10% resolution. Therefore a minimum of 10 quanta must be recorded in 10 seconds at the bottom of the indicator range. The number of quanta which would correspond to this acquisition rate for a number of input signal levels over the minimum and maximum measurement durations is shown in Table 7.1.

Level	0 dB	25 dB	40 dB
Duration	Number of Quanta		
10 seconds	10	$3.16 \times 10^3$	$10^5$
10 minutes	600	$1.89 \times 10^5$	$6 \times 10^7$

TABLE 7.1 Dose Register Size



It is clear that a 3 byte register would be needed for a constant level at the proposed top of the indicator range (25 dB), but that 3 bytes is insufficient to accommodate a top of the dynamic range signal for 10 minutes. This measurement duration was considered to be appropriate for capturing a representative sample of the signal, both for  $L_{eq}$  measurements and for the statistical analysis of sound level data. The use of a three-byte register would however accommodate all signal levels which would eventually result in an on-scale reading.

To determine the time corresponding to the size of dose quanta, one has to divide the total number of counts corresponding to the maximum input by the total measurement time:

$$\frac{6 \times 10^6}{6 \times 10^2} = 10^4 \quad \text{counts per second}$$

To complete the testing, incrementing and any necessary switching in 100  $\mu$ s is by no means impractical, but when the machine code is determined it requires running the microprocessor at a high speed and consequent high current. One technique which would reduce the need for such a high data acquisition rate is to use two separate constant current sources with a known, preferably binary based, ratio between them. This option is shown Figure 7.1.

The quanta of each need to be recorded in separate registers, but the data acquisition rate can be reduced because the low current can be used when the input from the antilog transistor is low and similarly the higher current source can be selected if the antilog transistor output

current is high. The microprocessor initially chooses the lower constant current and tests to see if the comparator has changed state. If after some predetermined period the comparator has not changed state, then the higher constant current is selected until the comparator changes state. The two separate data registers have to be combined to give an overall value for the dose.

#### 7.4.3 $L_{eq}$ Calculation

As previously discussed, it is desirable for  $L_{eq}$  to be calculated from the dose and elapsed time during the measurement period and to be continuously updated. As  $L_{eq}$  is the result of the logarithm of dose divided by elapsed time, it appears that the microprocessor needs to be capable of division. This is not necessarily so as the individual dose and elapsed time registers can be logged and then the result of subtracting the logarithm of elapsed time from the logarithm of dose gives the correct value for  $L_{eq}$ .

The logarithmic conversion must condense the possible 3-byte register to a scale which still allows small amounts of data to have their correct weighting. The simplest and therefore probably the quickest way to perform the logarithmic conversion would be to use a look-up table. It is not necessary to convert all the significant bits of register, as this would lead to an impractically large look-up table. To minimize the number of bits to convert and to choose the appropriate bits, one first needs to determine the most significant bit of the register which is in the high state. The bits in the register immediately below this highest

enabled bit always have the same weighting relative to this bit independent of its position in the register. The number of the highest enabled bit is therefore combined with a value derived from the look-up table based on the bits immediately below it.

The look-up table is situated in ROM and occupies a maximum of 256 locations as this provides sufficient resolution. The result of subtracting the two logged registers is condensed to less than a single byte; thus the result can be output via an I/O port and subsequently converted by a DAC to allow display on the analogue meter.

#### 7.4.4 L<sub>10</sub> and L<sub>90</sub> Calculation

At the end of the measurement period there is an array of registers whose contents correspond to the frequency of occurrence of each sound level, and a separate register which has recorded the elapsed time or the number of sound level samples taken. The microprocessor then adds the total number of counts in each register, starting from the top, until the sum is equal to one tenth of the total number of samples taken. The register which contained the last counts to be added in before this condition was met represents the value of L<sub>10</sub>. Similarly, starting from the bottom of the array and working upwards, L<sub>90</sub> may be evaluated. The values of L<sub>10</sub> and L<sub>90</sub> are stored in separate registers ready for access when a request is signalled to the microprocessor.

In order that the conversion may be performed as quickly as possible it is possible to convert with less than 8-bit

resolution. To achieve  $\pm 1$  dB accuracy in the final answer, it is possible to convert using only 6 bits. Each time the microprocessor increments the register which is being output from the port, it has to subsequently test the state of the comparator. To minimize the number of program steps in the loop the comparator output generate a signal for the external interrupt, thereby eliminating the need to read and logically test an input port during the cycle.

The total conversion time needs to be less than the time taken for the charge-balancing integrator to ramp up to the supply rail with the maximum input current. This is because when the microprocessor is recording the sound level time history it is not providing a balance current for the integrator. As the fastest ramp speed has been chosen nominally to be 10 ms, this condition will be met quite easily. A sensible target for the conversion time would be under 1 ms, remembering that CMOS microprocessor power consumption is virtually proportional to the clock frequency.

The result of the conversion corresponds to a particular sound level, so a number of classes or bins are provided, one for each level. If 6-bit conversion is performed this requires 64 bins. As the conversion is performed every 10 ms, a constant sound level would fill one bin at a rate of 100 counts per second. Given the required 10 minute measuring period, this would correspond to a total of 60,000 counts. This implies the use of 2 x 8-bit bytes for each bin, that is a total capacity of 65,536 counts at each

level. However, if 2 bytes were allocated for each of the 64 levels this would take up all the available RAM space of a typical single chip microprocessor (8049). Several techniques may be employed to overcome this difficulty. They include reducing the conversion to 40 levels, ie 1 dB resolution or only allocating 2 bytes to a restricted range of sound levels, eg the indicator range. If the class widths for the  $L_{10}$  and  $L_{90}$  calculation are increased beyond 1 dB, even greater savings in RAM space can be made and the conversion could be reduced to say 5 bit accuracy, giving 1.25 dB resolution. This would give a battery life improvement as well. In the prototype instrument a 1 dB class width was used, needing 80 bytes of RAM.

#### 7.4.5 Output Display of the Data

Although one might assume that having calculated  $L_{eq}$ ,  $L_{10}$  and  $L_{90}$  using a digital microprocessor, a digital display would be the most appropriate, this is not so. The sound level needs to be displayed, so a special digital panel meter would have to be provided. The signal from the digital panel meter and the output from a suitable display decoder/driver would have to be combined and the appropriate one selected for display. However, if an analogue meter is used for the display, the selection of the sound level signal or an output from the microprocessor can be made by a simple switch and the output from the microprocessor can be readily D-A converted by several simple techniques. These techniques include using an R-2R ladder from an I/O port on the microprocessor or by using a single bit output port on the microprocessor and pulse width modulating its output to

obtain the desired meter deflection. A digital display could be provided in addition to the analogue meter, but the heavy current consumption incurred would make it an expensive option. The draft international standard requires that if a digital display is provided, it should resolve to 0.1 dB. This hardly seems consistent with a design requirement for only  $\pm 1$  dB accuracy. A 30 dB analogue meter was used, fed from the microprocessor I/O port via an R-2R ladder network.

The final version of the software for this design is included within Appendix C.

## 7.5 The Advanced Microprocessor-based Instrument

When the design specification for the initial microprocessor-based instrument was determined, it was envisaged that a precision grade instrument would result subsequently. This section describes the development of such an instrument.

The basic specification was that it should at least equal the performance of the precision grade hybrid instrument by developing the principles of the earlier microprocessor-based instrument. Specifically this implies a 60 dB dynamic span together with the capacity to integrate over a measurement period at least equal to the normal working day (8 hours).

Re-evaluation of the design constraints considered previously showed that a charge-balancing integrator using two balancing currents would not provide the necessary dynamic span. A logical extension was therefore to investigate the use of three balance

currents. Similarly, examination of Table 7.2 shows that changing from a 3 byte to a 4 byte register would provide sufficient capacity for the dose data. This should be accomplished by relatively minor software modifications.

Level	0 dB	34 dB	60 dB
Duration	Number of Quanta		
10 seconds	10	$2.5 \times 10^4$	$10^7$
10 minutes	600	$1.5 \times 10^6$	$6 \times 10^9$
10 hours	$3.6 \times 10^4$	$9 \times 10^7$	$3.6 \times 10^{10}$

TABLE 7.2 Dose Register Requirements for the Advanced Instrument

A prototype embodying these principles was constructed. The maximum balance current was selected to be 3 mA, as this was sufficient to balance the maximum available current from the 2logV-alog stage. The two lower currents were initially set to be  $2^8$  submultiples of the maximum, but the resulting minimum quanta of charge were too small. The ratio of currents was changed to  $2^7$ . This arrangement proved capable of balancing a wide range of input signals, but the circuit was particularly prone to drift problems.

The fundamental problem was to control the lowest balance current accurately. As in the earlier microprocessor-based instrument, the 5 volt supply was used as the reference for the balance currents. This presented no problems for the higher currents, but no stable method could be found to determine the lowest balance current of 183 nA. One method was to employ a potential divider to step the

reference supply down in order that a high stability resistor could be used. The shortcoming with this arrangement was that the FET input operational amplifier, which had been selected for its low input bias current, had a significant temperature-sensitive input offset voltage. Although the circuit could be set up, the integrator soon started to drift, in either direction.

#### 7.5.1 Short $L_{eq}$

An exciting development presented in a definitive paper in 1981 [14], was the introduction of the concept of Short  $L_{eq}$ . In this method, numerous short term  $L_{eq}$  measurements are recorded in a data store. Subsequent processing allows synthesis of Global  $L_{eq}$ s over any desired period within the total measurement period, together with all the statistical parameters. The principal advantage of this method is that the raw data is stored. The decision about which acoustic descriptor to apply is deferred until the data has been stored. This new method was considered to be of such importance that the specification of the advanced microprocessor-based instrument was amended to include the Short  $L_{eq}$  facility.

The elemental period selected for the generation of Short  $L_{eq}$  was 125 ms, as this would result in time history data with comparable resolution to a conventional SLM. Requiring the instrument integrator to have only sufficient capacity for this short period eased a number of difficulties which were experienced with the current prototype. However, as the basis of the Short  $L_{eq}$  method is for post-capture processing, it is necessary for the instrument to be able to



respond to an even greater dynamic range of input signals. One application which demands this high dynamic range is unattended airport monitoring, where a very low background may be interrupted by a high level noise event.

To facilitate the increased dynamic span, a further prototype was developed which used three independent integrators. The microprocessor controlled each of the integrators during the elemental period and then selected the data from the most appropriate integrator. For a mid-range signal, one integrator would overload, one would have the correct  $L_{eq}$  and the other would not have acquired sufficient data to resolve accurately the input signal.

Although the microprocessor could balance the three integrators, it had no spare capacity to format and store the data or process keyboard, display and interface routines.

#### 7.5.2 The Final Instrument

The balance between hardware and software processing needed to be optimized. In order to achieve this, the three integrators were replaced by two of the proven switch-back integrators and digital dose store of the hybrid design. As in the hybrid design, the dose data is recovered with a modified R-2R ladder network. Each of the integrators has three possible ladder network taps. The output of the appropriate integrator is selected by a controller, implemented in CMOS random logic. This selected output is then fed to a logarithmic amplifier. Since a reading is only required after the preset elemental period, there is no

need for a signal corresponding to elapsed time. Instead, a fixed current is supplied to the logarithmic amplifier. The value of this current can be varied over a small range to allow for system calibration.

At the end of the elemental period, an analogue to digital conversion is performed on the output of the logarithmic amplifier. This, combined with a three-bit word which specifies which tap was connected to the logarithmic amplifier, provides all the necessary data to the microprocessor. The selected output parameter from the microprocessor is displayed on a 4-digit display as the instrument does not compute sound level.

### 7.5.3 Analogue Refinements

Whilst developing the final prototype, the previously designed analogue stages were also re-examined. Experience gained from "in the field" operation of a number of the designs, coupled with recent component developments showed that the performance could be extended even further.

The majority of the improvements related to the operation of the analogue integrator. This stage had been identified earlier as a possible weak link, due to finite switchback and leakage. The leakage problem was largely eliminated by the adoption of Short  $L_{eq}$  and its implied short measuring duration. Use of an operational amplifier as a comparator in the retrace circuitry was the cause of some of the speed problems. The use of passive components alone to determine the integrator hold-off also led to a reduction in possible

operating speed by having to over design to allow for component tolerancing. The retrace circuitry was therefore re-designed to incorporate a very high speed, yet low current consumption, comparator together with an integrated circuit monostable multivibrator and the latest low impedance FETs. With this new arrangement the retrace and hold-off could be accomplished reliably in only a few microseconds.

A further problem relating to the operation of the integrator was the current wasted in providing the reference current for the antilog stage. Although it is within the antilog stage, this current is used to set the scale of currents into the integrator. This constant reference current is passed through a logging transistor to offset the base of the antilog transistor. By offsetting the base of the logging transistor slightly negative, the current through it can be reduced considerably, yet still maintaining the base of the antilog transistor at its correct value.

A shortcoming of the hybrid instrument which the microprocessor-based instrument was intended to overcome, was the possible loss of dose information during retrace of the integrator. This possibility had been greatly reduced with the upgraded circuitry, but a further improvement was made. This improvement consisted of placing a low value resistor in series with the transistors of the 2log stage. During normal operation, at low signal levels, the voltage drop across the combination of the transistors and resistor

is almost solely determined by the base emitter drop of the transistors. Hence the circuit operation is unchanged. At high signal levels, where loss of dose information is possible, appreciable currents are flowing in the transistor resistor combination. The contribution of the resistor therefore increases and the overall voltage drop is greater than would be expected under normal operation. This increased voltage drop results in a higher integrator current and hence faster sweep speed. If the value of this resistor is selected carefully, its effect is to exactly compensate for the possible loss of dose information during retrace. Without the resistor the integrator sweep speed is slightly slow. Adding the resistor allows the performance at the top of the dynamic span to be improved so that the range of input signals is increased by about 10 dB.

#### 7.5.4 Data Retrieval

The large quantities of data which the instrument was capable of acquiring (256 k) needed to be retrieved for subsequent reprocessing. This was identified as a secondary but nevertheless important task for the microprocessor. In collaboration with the proposers of the Short  $L_{eq}$  concept a protocol for data transfer was proposed, together with the definition of an interface for acoustic applications [15,16,17,18].

Each measurement session which is recorded in the instruments memory is preceded by a header which gives information about the session. This information includes the number of samples within each session, the type of

acquisition and the offsets between headers. This allows for scanning of the headers to determine which, if any of the sessions are to be transferred. A more complete summary of the header format and content is presented in Appendix B.

Complete circuit diagrams of the final instrument are presented in Appendix A. Pseudo-code used in the development of the software is included in Appendix B. Listings of the major programs, including those used to generate the look-up tables, are included in Appendix C.

CHAPTER EIGHT  
EVALUATION PROCEDURES

The assessment of individual circuit performance and that of complete instruments was a necessary and integral part of the study. The findings of such assessments were invaluable in optimizing individual circuit parameters, and in determining the interactive effects of combining these circuits into working instruments.

Special test equipment was constructed so that the full range of the three important  $L_{eq}$  meter parameters could be presented to the instrument. As discussed in Chapter Four, the parameters are: the dynamic span, the exchange rate tolerance and the peak factor capability. Each of these gives additional information about a given circuit design or instrument's suitability to accurately integrate the wide span of possible input signal levels and measurement durations. The method for applying these signals and the method for interpreting the results is also given in Chapter Four.

Tests were carried out on a number of different manufacturers' ISLMs, and the results were compared with those obtained using the hybrid  $L_{eq}$  meter which had been produced as part of this project. The results of these tests were reported at the Institute of Acoustics Spring Conference 1980. A copy of the relevant extract from the proceedings is included in Appendix D. In the table of exchange rate tolerance errors, the ISLM produced as part of this project is instrument number 5.

The assessment procedures used in this work have included both tone burst and single-cycle input signals. A paper discussing the relative merits of the two methodologies was presented at the 12th International Congress on Acoustics, Toronto, 1986 [19]. This paper highlighted the

need for specialized signal sources, and the value of the special interface developed for the advanced microprocessor-based instrument.

The dedicated system developed as part of this work has a signal to noise ratio of greater than 80 dB. This is the limit of the frequency analyser which has been available. The final version of the instrument has a dynamic range in excess of this, and approaching the 110 dB maximum of the control range of the attenuators. It is therefore clear that the evaluation equipment and procedures need constant updating in order to correctly assess the latest instruments.

### 8.1 Instrumentation

The following instrumentation was used during the final assessment stage of the project. This arrangement is representative of the wide range of equipment used throughout the development and earlier assessment stages of the work.

1. Specialized tone burst generator developed as part of this work.
2. 2 x Enertec Programmable Function Generators Type 4431.
3. Marconi MF Attenuator Type TF 2162.
4. Gould Digital Storage Oscilloscope Type 4035.
5. Bruel & Kjaer High Resolution Signal Analyser Type 2033.
6. Hewlett Packard Plotter Type 7470A
7. Farnell Dual Power Supply Type LT 30-1.

The Enertec programmable function generators were used in combination, with one device determining the repetition rate for the

tone burst sequences and the other determining the tone burst duration and signal frequency. Although this was an easy arrangement to control, particularly via the IEEE 488 interface bus, the signal quality and range of signals was not as great as the dedicated system developed as part of this work. This latter system was therefore used for all measurements other than initial evaluations.



## RESULTS

As with any project of this nature, the principal results are the new circuit techniques and applications embodied within the designs which have been presented. The performance of the principal constituent elements has been described within each section. Therefore this chapter will only present results which quantify overall instrument performance or indicate the response of the complete instrument to the test stimuli.

In each of the following figures, the input signal is not shown correctly scaled. This signal was derived from a point before the attenuator, as connecting a probe directly to the sensitive instrument input caused problems of earth loops and increased the background noise.

Figure 9.1 shows the output voltage of the switch-back integrator when subjected to a mid-range constant level on the instrument input.

Figure 9.2 shows the output of the same integrator with a high level input signal. The increase in output due to each half-cycle can be seen clearly. A system phase shift can be detected.

Figure 9.3 shows the output of the switch-back integrator in response to the tone burst test stimulus for the exchange rate test.

The data stored in the advanced microprocessor-based instrument is downloaded to an IBM PC compatible computer for analysis. Figure 9.4 shows the output of data recorded by manually increasing the input signal in 0.1 dB steps.

The overall performance of the instruments and prototypes produced as part of this work is summarised in Table 9.1.

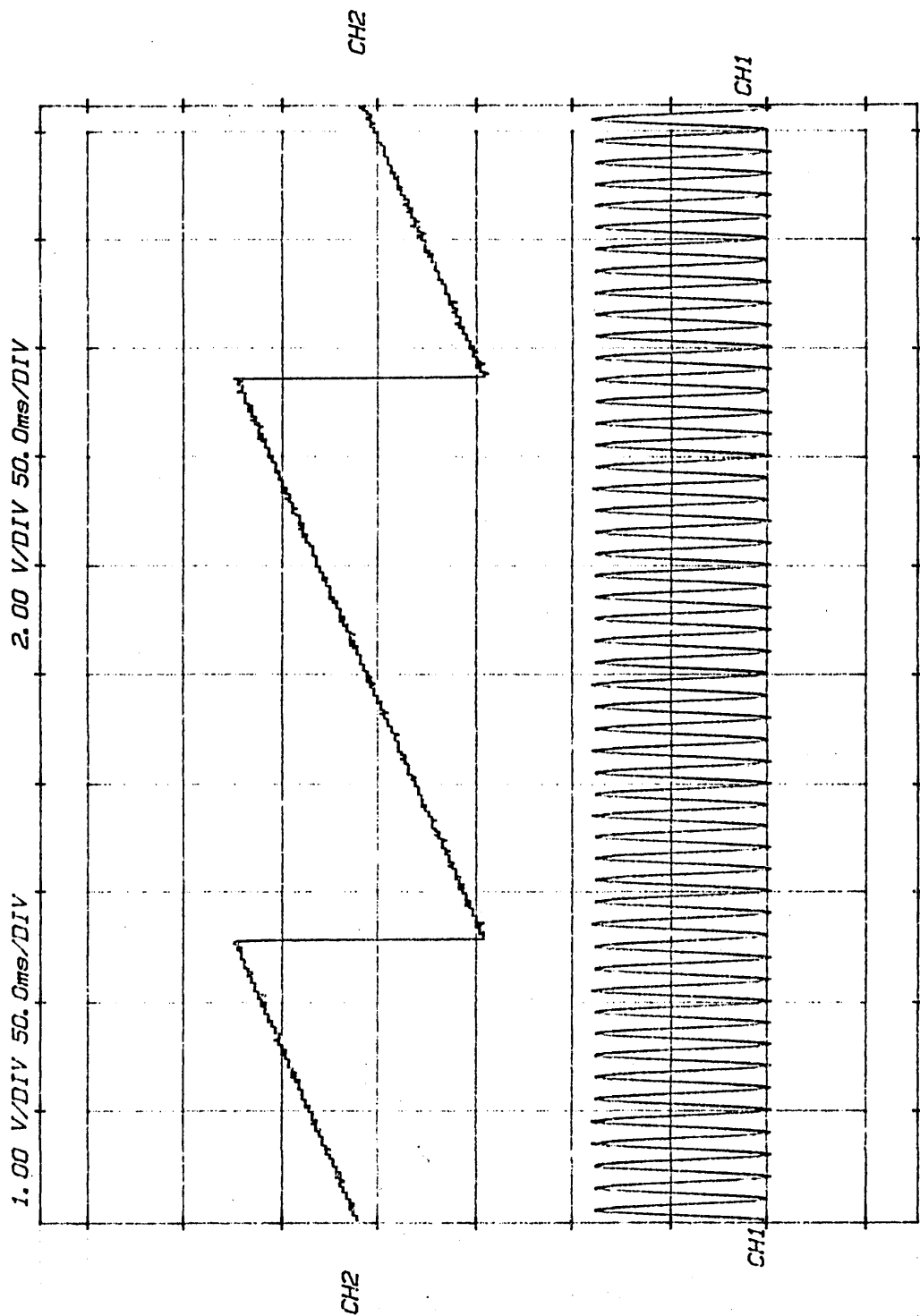


FIGURE 9.1 Switch-back Integrator Output (CH2) with Mid-range Input (CH1)

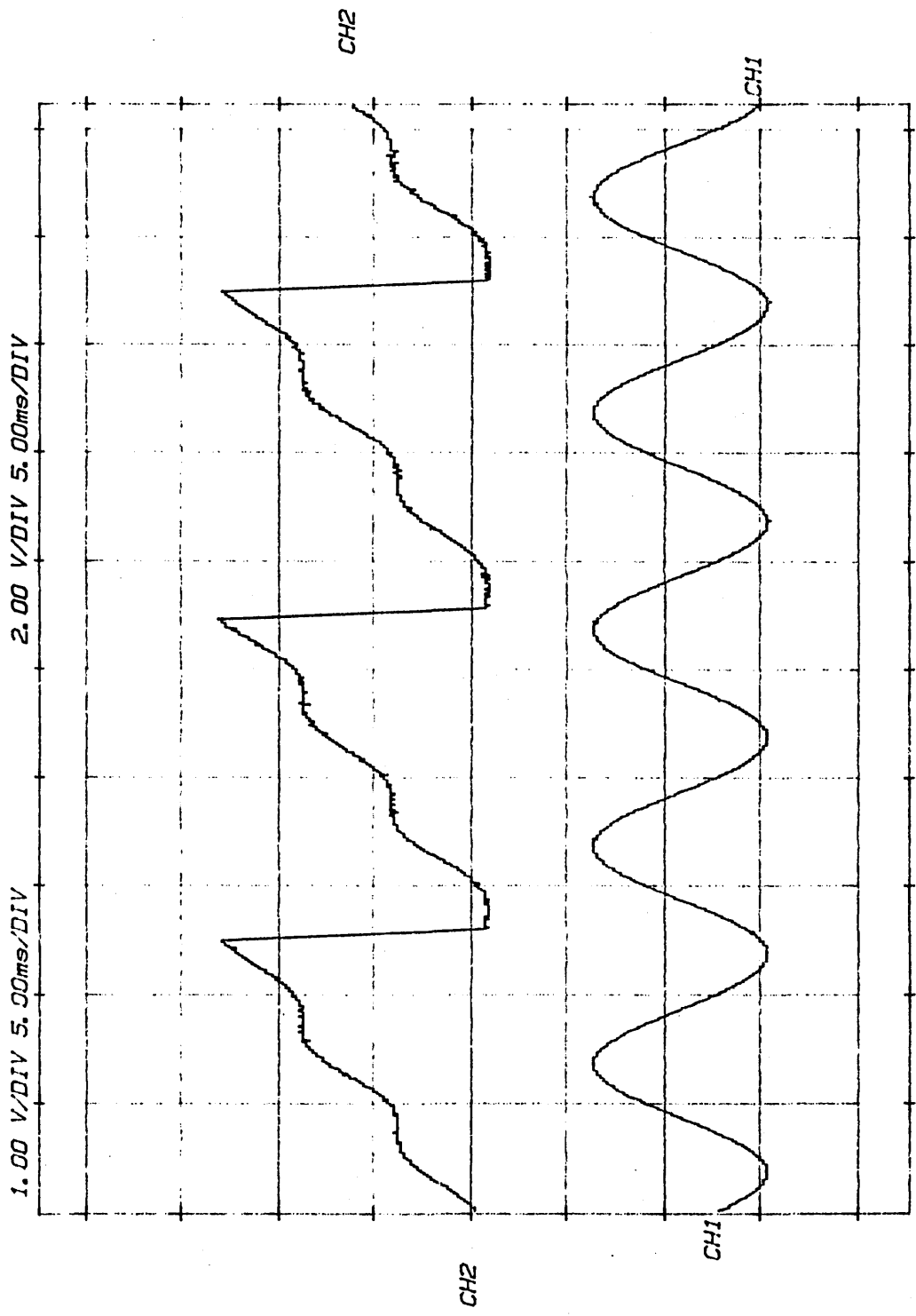


FIGURE 9.2 Switch-back Integrator Output (CH2) with High Level Input Signal (CH1)

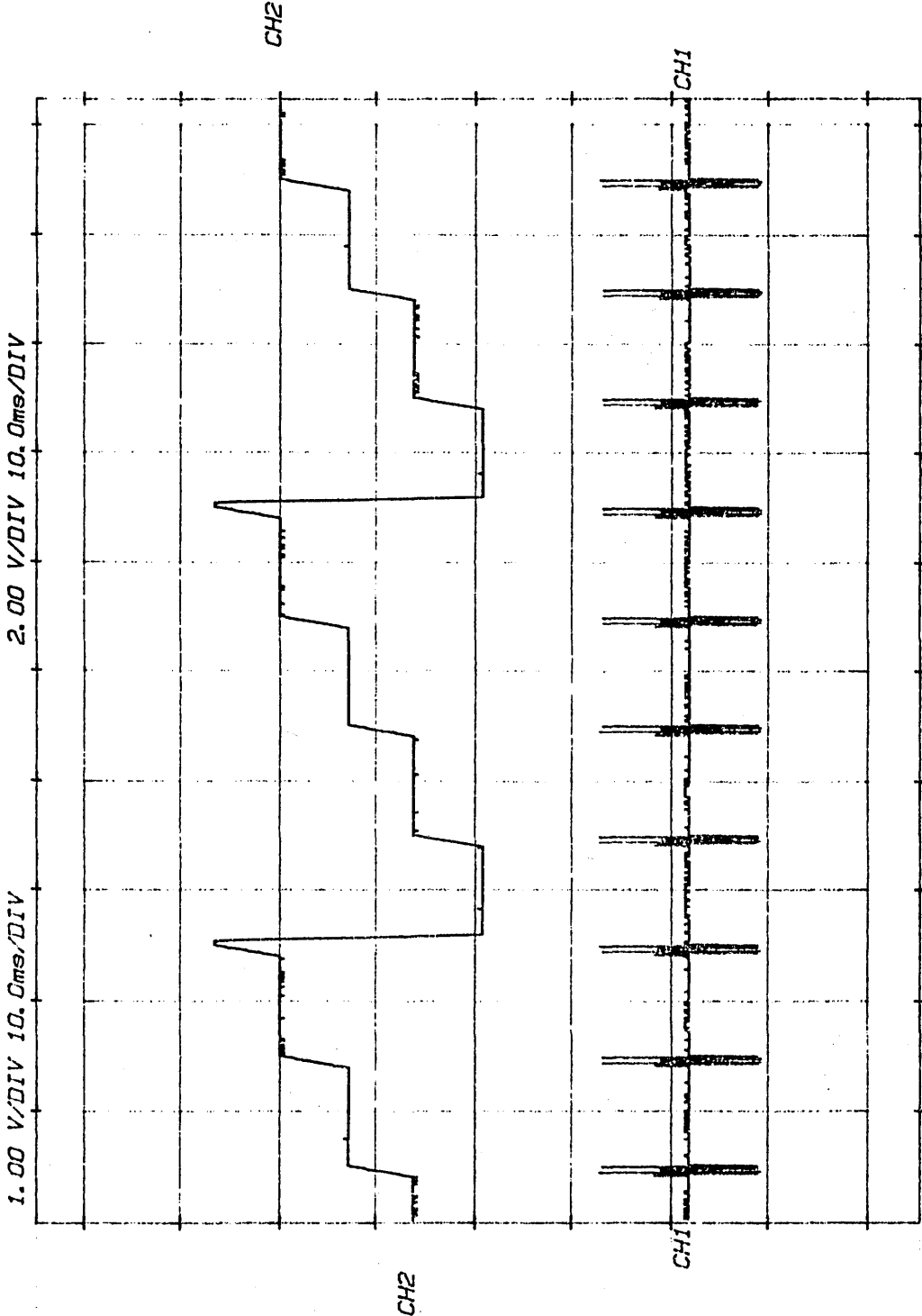


FIGURE 9.3 Switch-back Integrator Output (CH2) with Tone Burst Input (CH1)

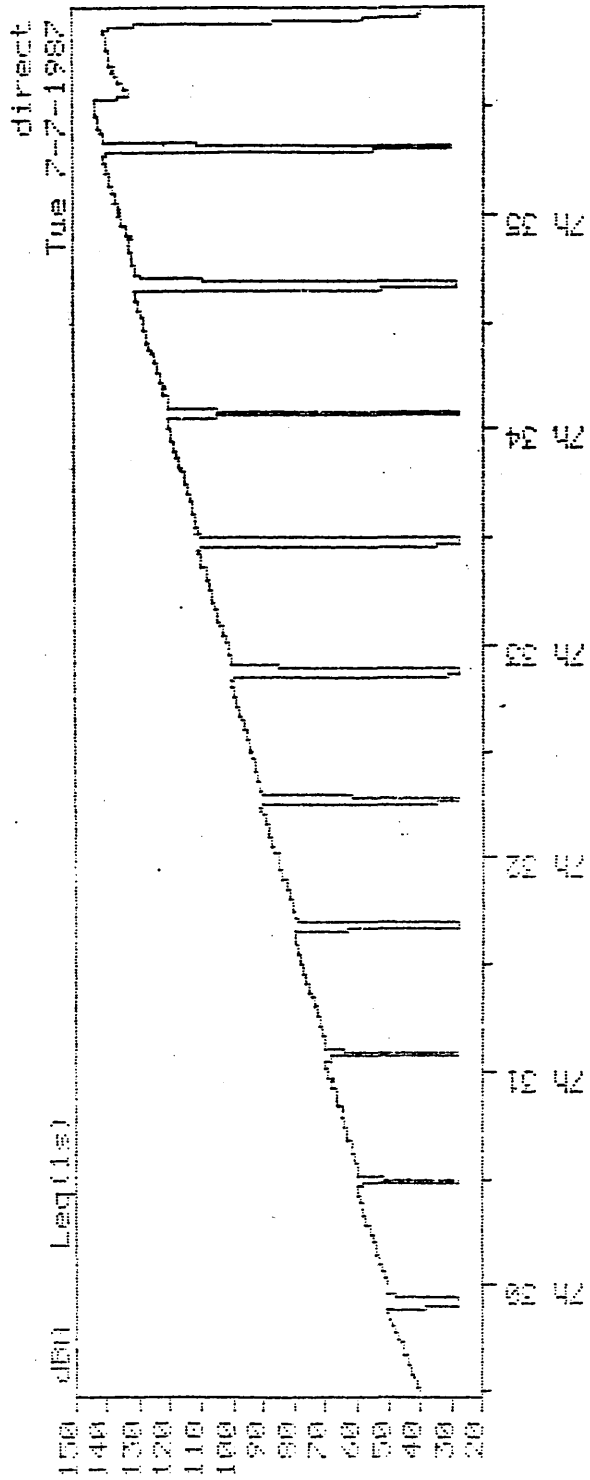


FIGURE 9.4 Data Downloaded from the Advanced Microprocessor-based Instrument

Instrument Number		1	2	3	4
Exchange Rate Error					
Input Signal	Relative Amplitude				
Tone Burst mark/space 1:9	+ 10 dB	0.0	0.0	0.0	0.0
Tone Burst mark/space 1:99	+ 20 dB	0.0	+ 0.1	+ 0.1	- 0.1
Tone Burst mark/space 1:999	+ 30 dB	0.0	+ 0.1	- 0.2	+ 0.2
Tone Burst mark/space 1:9999	+ 40 dB	< 0.1	+ 0.3		+ 0.2
Tone Burst mark/space 1:99999	+ 50 dB				- 0.1
Dynamic Span		65	55	43	~ 110
Peak Factor		68	58	46	> 80
Instrument Type		1	2	3	0

TABLE 9.1 Summary of Complete Instrument Performance

## DISCUSSION OF RESULTS

As expected, the constant input gives rise to a steadily increasing integrator output voltage (Figure 9.1). The quantisation noise evident on the trace is due to the digital storage oscilloscope. One of the major difficulties in assessing the integrator performance of the advanced microprocessor-based instrument is that this form of response only occurs at very low signal levels. At higher signal levels the integrator behaves as a voltage to frequency convertor, with the integrator switching many times within one cycle of the input signal. This makes linearity measurements of the integrator alone very difficult. However, as demonstrated with the final instrument, optimization of the complete instrument is not necessarily achieved by setting the constituent elements in isolation. The level of performance of an instrument is strongly determined by the setting up procedure. A good design should incorporate a repeatable and rapidly convergent adjustment scheme.

Although the input waveform for the tone burst test (Figure 9.3) is not resolved particularly well, it indicates the position of the impulses and serves to highlight the difficulties presented to an ISLM in capturing impulsive signals. The trace for Figure 9.3 was taken from an instrument which had an intentionally slow retrace, but had the compensation resistor fitted in the 2log stage (section 7.5.3). The uniform step size, despite an impulse occurring at switch back, demonstrates the value of this modification.

The software package which produced Figure 9.4 was part of a parallel development programme with the French company Soeur-Anne. Although

developed for combined use with the final instrument as a powerful data acquisition and analysis system, it also provides a convenient tool for assessing the performance of the hardware. The glitches in Figure 9.4 are due to the attenuator passing through its  $-\infty$  position. With the attenuator in this position the noise floor resulting from the limits of the instrumentation system is evident. It is not completely determined whether this is due to the instrument alone or as a result of attenuator breakthrough and other external noise. Under these conditions most of the measurement system is operating at the extreme of its operating limits as the input corresponding to this instrument reading is less than  $4 \mu\text{V}$ .

Although the trace was obtained manually, there is obvious scope to automate instrument evaluation and documentation. This is greatly assisted by the command and data structure associated with the DP37 interface system [17].

At the upper extreme of the trace, the overload condition was not trapped so that the limit of the dynamic range could be readily identified for the purposes of this thesis. A dynamic range of around 110 dB can be identified.

The results presented in Table 9.1 represent four identifiable stages of development of the project. The performance of the earliest hybrid instrument is still a significant achievement, several years after its design. However, it did not fulfil the criterion, discussed earlier in this chapter, that the setting up procedure should not be too critical. The performance of the hybrid instrument outlined in Table 9.1 (instrument number 1) could not be maintained over a wide temperature range. This design was therefore not considered suitable for manufacture.



Instrument number 2 is a hybrid instrument which is a simplified version of the first instrument which was designed to meet the needs of an Open University course. Specifically the major simplification in this instrument is to use a ladder network control strategy which locks the dose and time registers together. Although the earlier, more elegant, design could compute  $L_{eq}$  from a wider range of dose and time information, this increased range of accuracy only applied to readings which could not be displayed due to the meter limitations.

The intended application meant that the instrument had to be reliable and easy to operate as it was to form part of the home experiment kit. In addition to this it had to meet a non-trivial design specification within the restricted budget of the Open University. As is evident from the results from this instrument, its Type 2 classification is due to dynamic span rather than exchange rate errors. Since this is limited by the use of only two batteries, it is probably capable of improvement. This design has been manufactured successfully and is now used by a number of public bodies throughout the world.

Instrument number 3 in Table 9.1 is the microprocessor-based prototype using a charge balancing algorithm described in the early sections of Chapter Seven. It was developed to provide an alternate to the instrument 2 for use by the Open University. The performance of this instrument in computing  $L_{eq}$  is not as good as the previous one, however this instrument offered the additional feature of providing the statistical levels, a feature particularly sought after by the course team. The cost penalty of including a microprocessor embodied within the instrument was a major factor against this unit. The second hybrid instrument was eventually adapted for interface to the analogue to

digital convertors of the BBC model B microcomputer and special software was prepared to facilitate generation of the statistical indices.

The performance of the final instrument is that of instrument 4 in Table 9.1. The exchange rate tolerance errors are well within the limitations imposed by a Type 0 classification. The uncertainties in the dynamic span and peak factor figures are as a result of the limits imposed by the instrumentation system, however they also represent performance which is consistent with a Type 0 classification.

## CONCLUSIONS

Evaluation procedures developed as part of this work and the standards demanded by the allowed tolerances could not be attained by previous instrumentation. These procedures require the use of dedicated hardware to assess fully the important characteristics of integrating sound level meters.

The limitations of earlier instruments' response to impulsive signals has been attributed to both the squaring and integrating stages. These limitations have been assessed and the critical mechanisms have been identified. Techniques have been developed which overcome these limitations. Specifically, these include maximizing the gain-bandwidth and slew rate limit within the absolute value and  $2\log$  stages, together with careful selection of the diodes and transistors.

A novel technique, developed for use in the hybrid instrument, is to combine both analogue and digital elements for storing the dose information. This combines the advantages of the stability of digital storage with the continuous nature of analogue processing.

The optimum configuration for an instrument which attains a high performance against the demanding specification, is formed by the use of analogue techniques for the majority of the signal processing, with a combination of random logic and microprocessor-based techniques for control and data storage.

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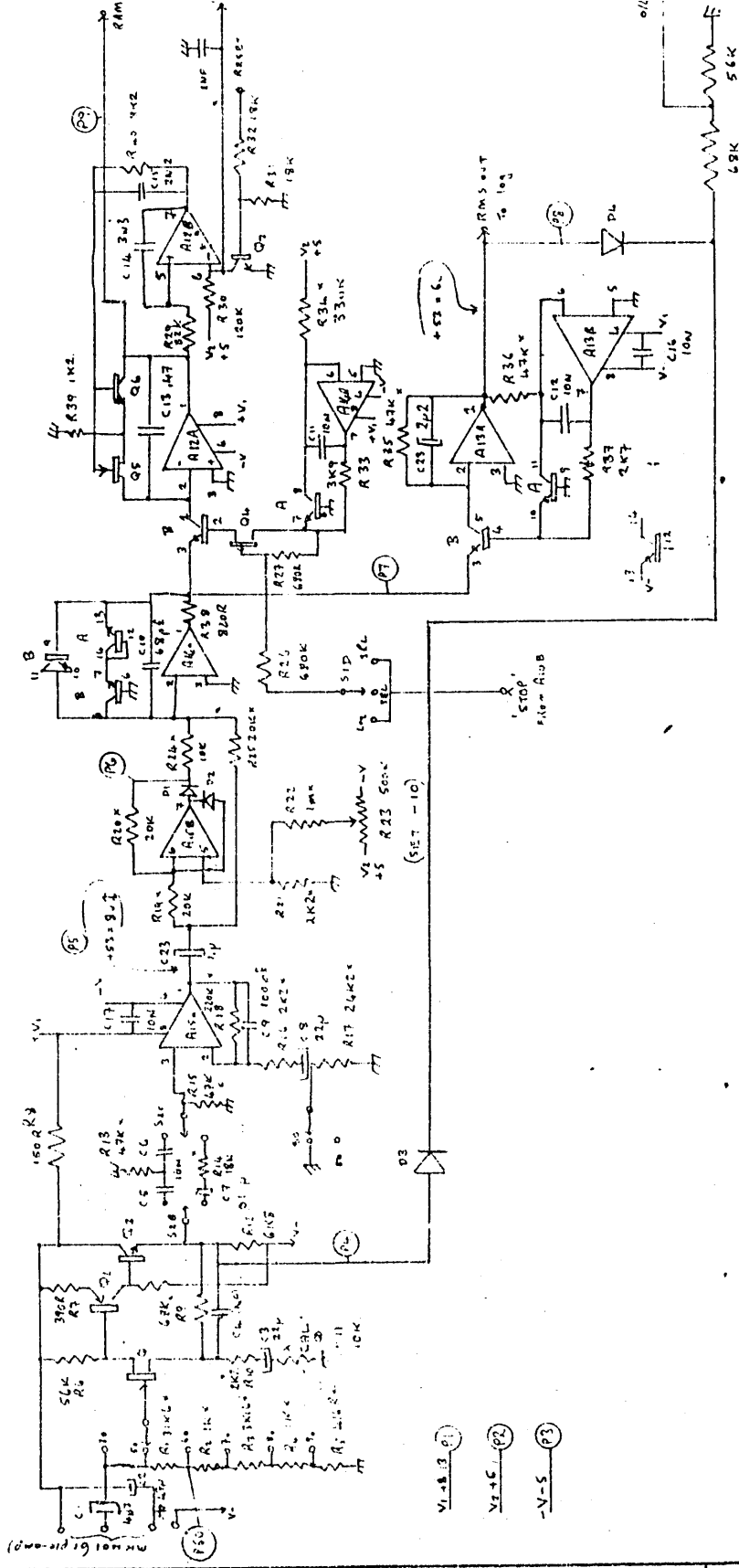
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CD/1031/01/S IA3



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DRAWING NO. CD/1031/01/S

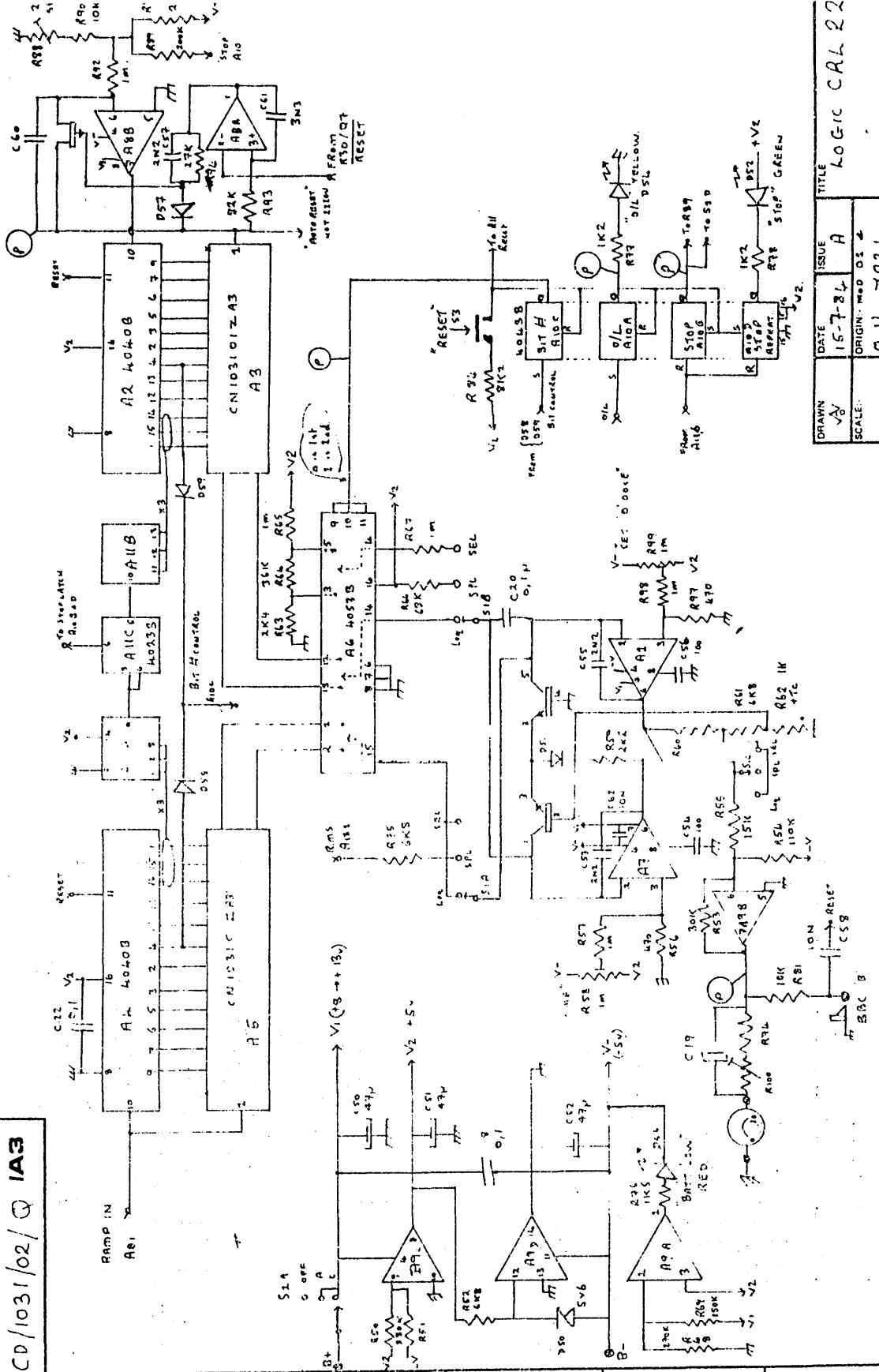
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THIRD ANGLE PROJECTION  
ALL DIMENSIONS IN MM

MATERIAL FINISH:  
THE REC DIVISION OF SCIENTIFIC MEASUREMENTS

MODIFICATION	DATE	ISSUE

H.O.M. HULL & LEEDS

CD/1031/02/Q IA3



DRAWN		DATE	ISSUE	TITLE	
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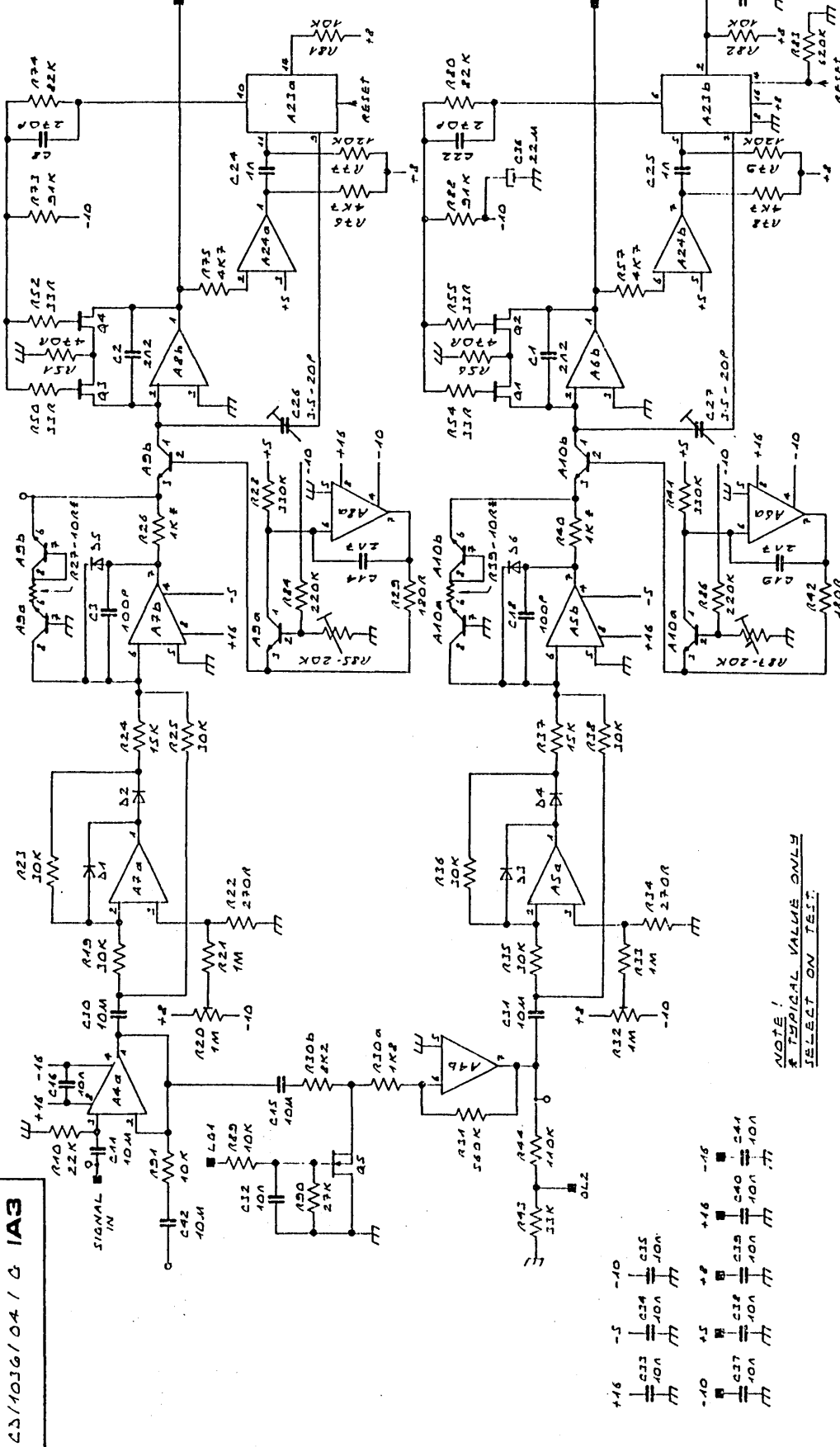
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ALL DIMENSIONS IN MM.

MATERIAL:  
FINISH:  
THE R&D DIVISION OF SCIENTIFIC MEASUREMENTS

MODIFICATION	DATE	ISSUE



CD/1036/04/1 & IAS



NOTE!  
 \* TYPICAL VALUE ONLY  
 \*\* SELECT ON TEST.

- +16 C33 10n
- 5 C34 10n
- 10 C35 10n
- +8 C36 10n
- +16 C37 10n
- +5 C38 10n
- +10 C39 10n
- +16 C40 10n
- +10 C41 10n

DRAWN	DATE	ISSUE	TITLE
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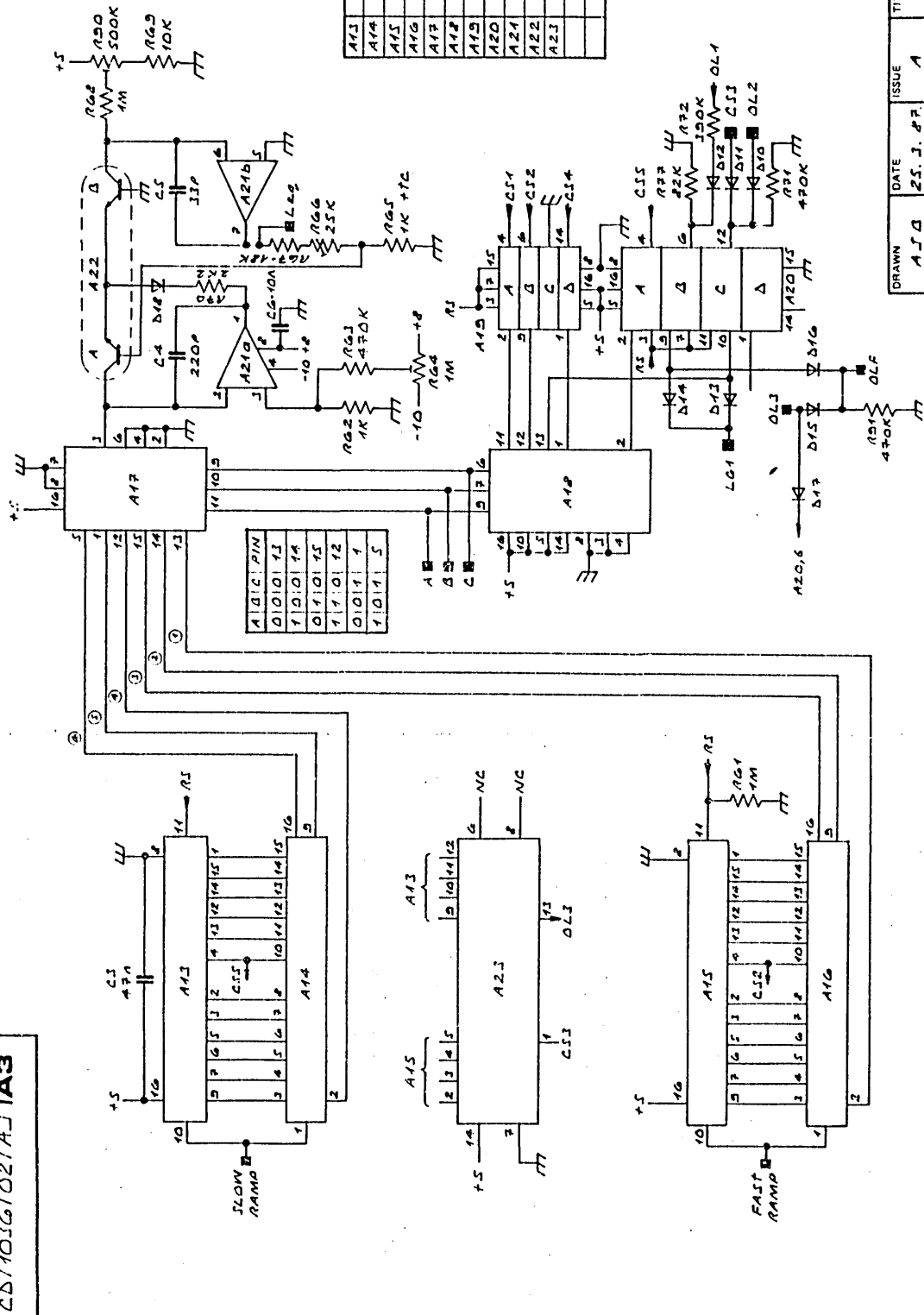


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MODIFICATION	DATE	ISSUE

CD10361021AJ1A3



A13	4040B CMOS
A14	7031-01-Z
A15	4040B CMOS
A16	7031-01-Z
A17	4051A CMOS
A18	4532B CMOS
A19	4043B CMOS
A20	4043B CMOS
A21	AD648 BQ
A22	LM154
A23	4022B CMOS

DRAWN	AJD
DATE	25.3.87
ISSUE	A
TITLE	SAL 236
SCALE	1:1
ORIGIN	CIRCUIT
DIGITAL SELECT	
CIRCUIT DIAGRAM	



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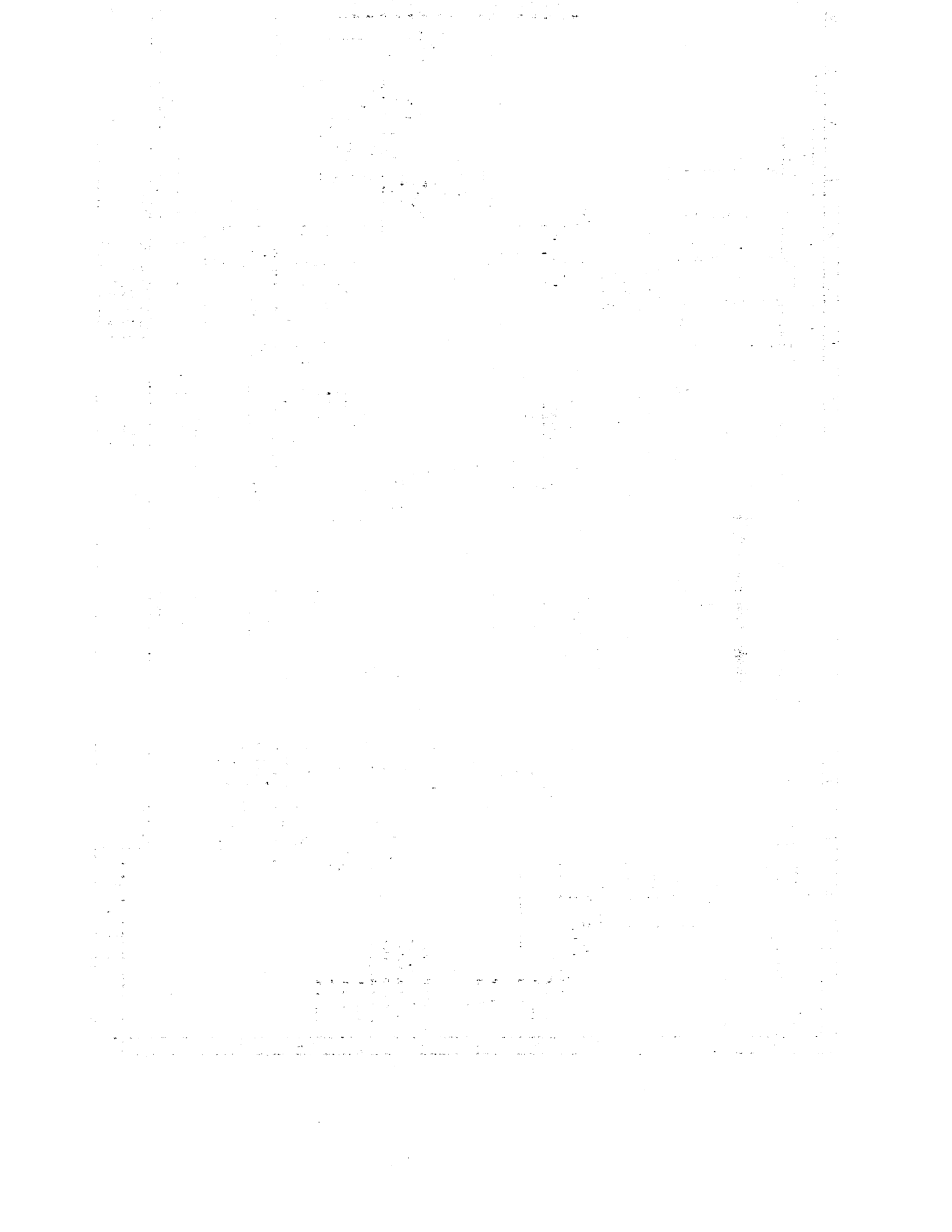
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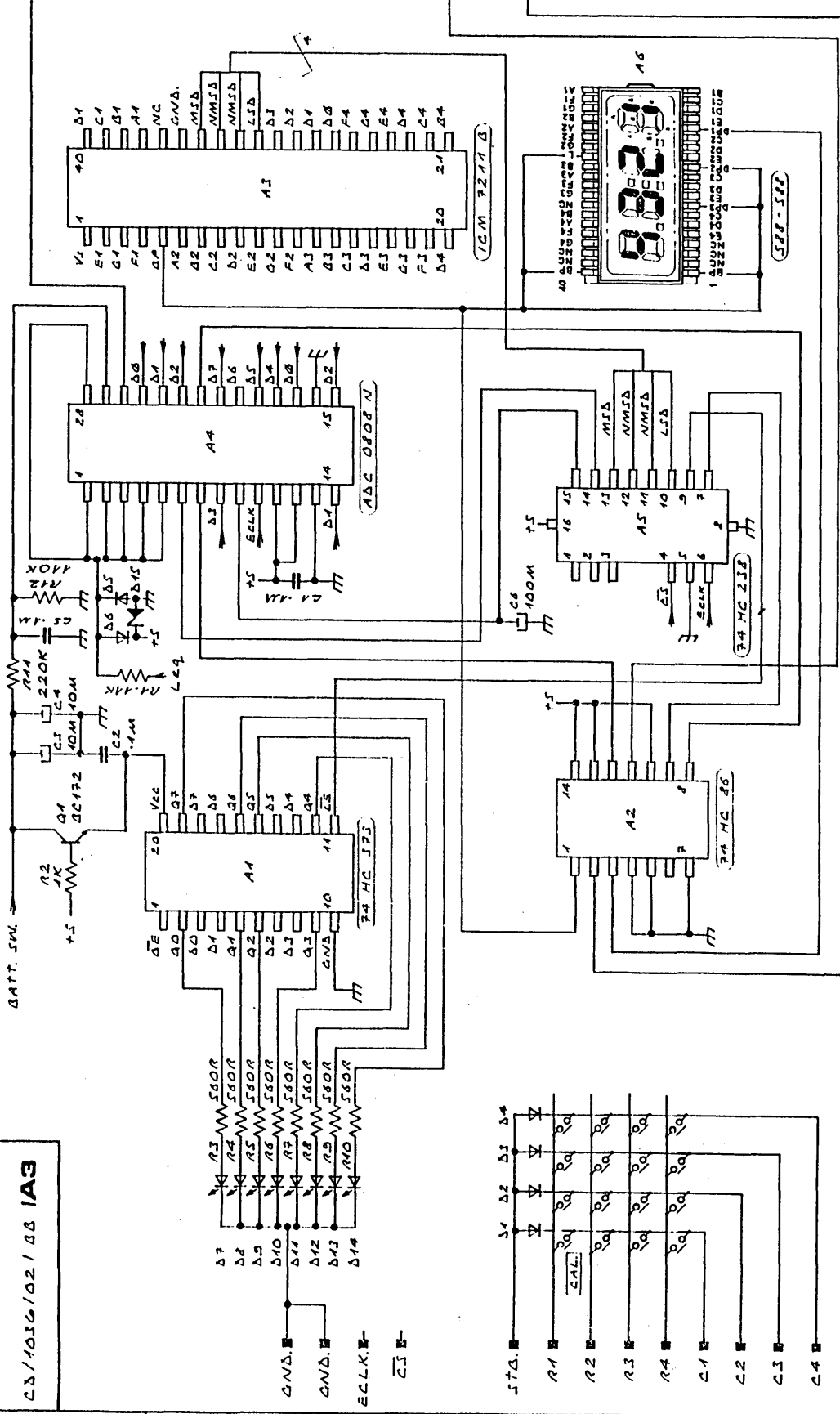
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CS/1036/02/00  
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 XEROBOARD PC  
 CIRCUIT DIAGRAM

DRAWN	DATE	ISSUE	TITLE
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TOLERANCE ± 0.2 UNLESS OTHERWISE NOTED.  
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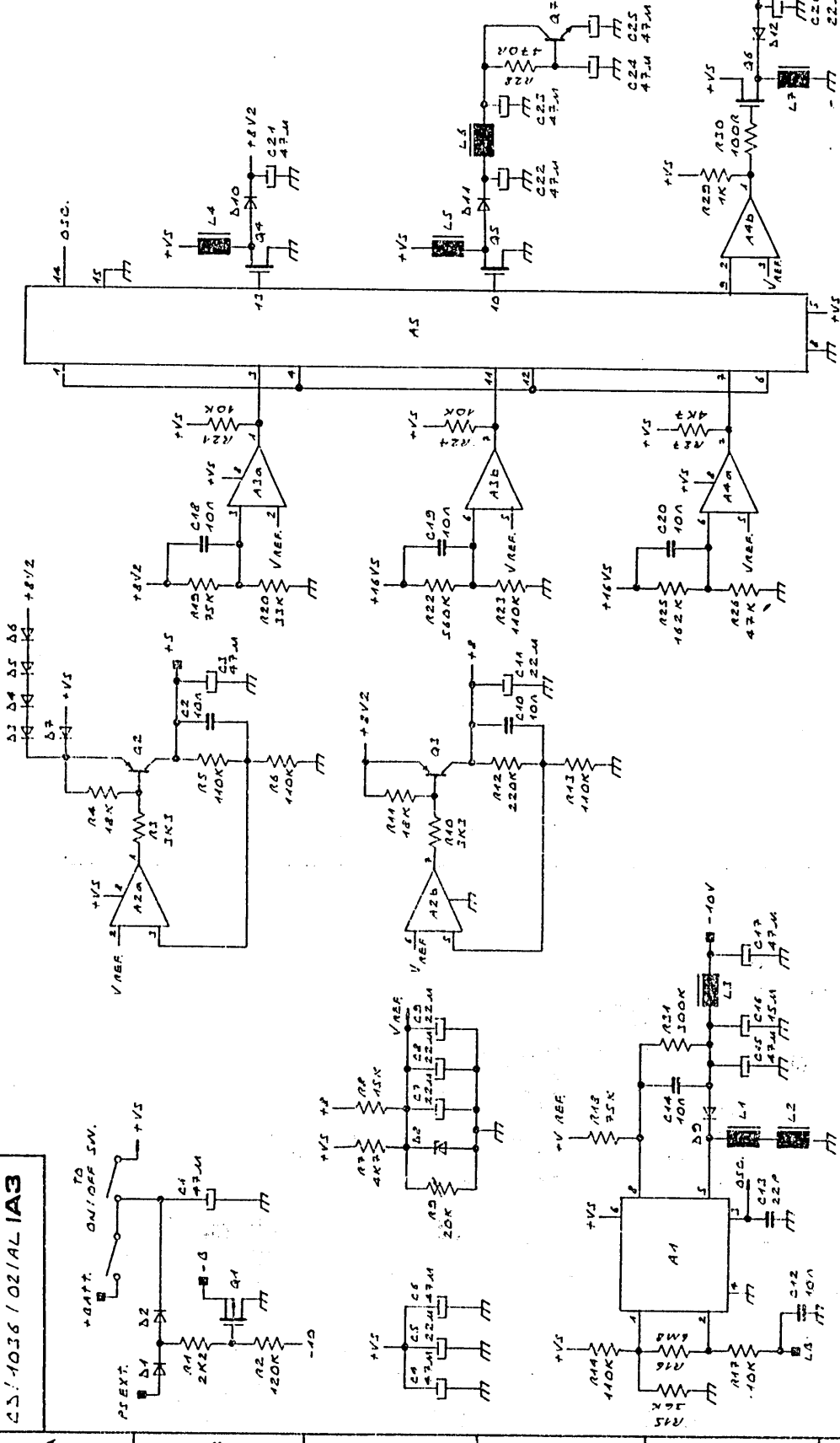
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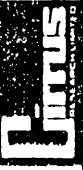
M.S.M. HULL & LEEDS.



CS/1036/02/ALIA3



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SCALE	ORIGIN	DRAWING NO.	
		CS/1036/02/ALIA3	



TOLERANCE ± 0.1 UNLESS OTHERWISE NOTED.  
 THIRD ANGLE PROJECTION.  
 ALL DIMENSIONS IN M.M.

MATERIAL: FINISH:

MODIFICATION	DATE	ISSUE

H.O.M. HULL & LEEDS.

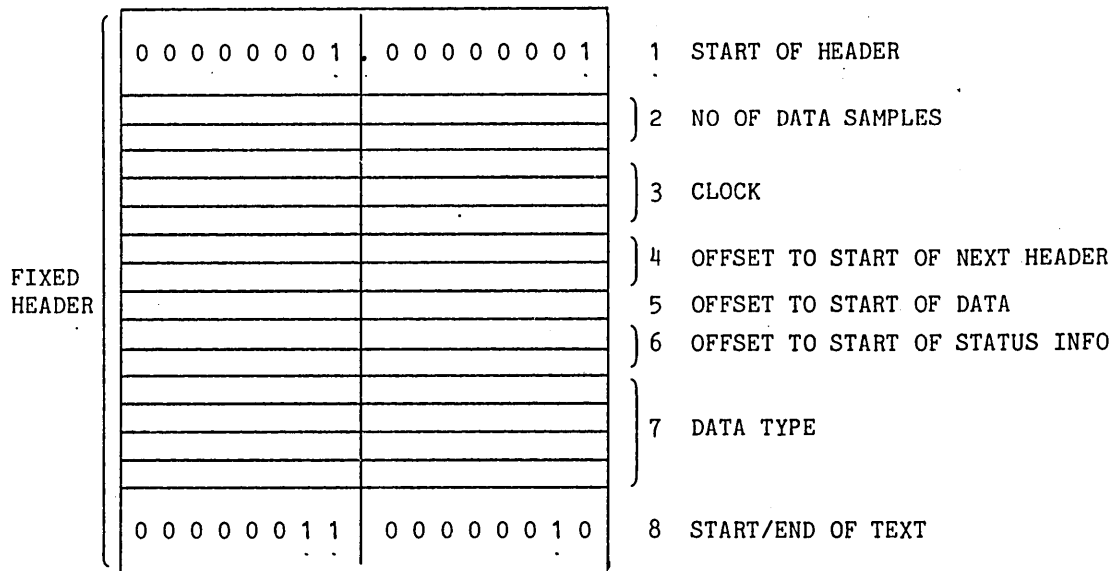


# DATA STRUCTURE FOR DATA FORMAT AND STORAGE

This structure runs within the timer interrupt after a/d conversion and integrator reset.

```
IF ACMODE == 0
THEN RETURN
*** DO A/D ETC HERE ***
PACK TWO BYTES OF DATA INTO DATA WORD
IF DATA WORD > MAX WORD
THEN MAX WORD = DATA WORD
    IF LCD_MAX_UPDATE == 1
    THEN CONVERT MAX WORD TO BCD
LOG ADD DATA WORD TO CUM TOTAL WORD
IF LCD_CUM_UPDATE == 1
THEN CONVERT CUM TOTAL WORD TO BCD
LOG ADD DATA WORD TO RUNNING TOTAL WORD
TOTAL COUNTER
IF TOTAL COUNTER == ACTYPE (EG 80)
THEN TOTAL COUNTER = 0
    IF LCD_LEQ_UPDATE == 1
    THEN CONVERT RUNNING TOTAL WORD TO BCD
    RAM VALUE = RUNNING TOTAL WORD + CODE + ERRORFLAG
    STORE RAM VALUE AT RAM POINTER
    INC RAM POINTER (24 BIT)
    INC DATA COUNTER (24 BIT)
```

HEADER INFORMATION



- 1 Start of header ASCII code x 2.
- 2 No of data samples, NB not including non-data bounded by 0000H, 0000H.
- 3 Clock gives start time in seconds from .....
- 4 Offset to start of next header, from start of this header.
- 5 Offset to start of data, from start of this header.
- 6 Offset to start of status information, from start of this header, 00 = no info
- 7 Basic data type information.

3	2	1	0
7	5	5	4
B	A	9	8
F	E	D	C

NIBBLE 0: Source of data - coded - normally refers to bits 0 -> 10.

- 0 Not in use or not relevant - coding could be in use.
- 1 Sound
- 2 Vibration
- 3 Voltage
- .
- .
- F Go to data type extension for more information

NIBBLE 1: Intentionally left blank.

NIBBLE 2: Frequency weighting.

- 0 Not in use or not relevant
- 1 A weighting
- 2 B weighting
- 3 C weighting
- 4 D weighting
- 5 Lin weighting
- 6 Integral
- 7 Double Integral
- 8 Differential
- .
- .
- F Go to data type extension for more information

NIBBLE 3: Intentionally left blank

NIBBLE 4: Filters

- 0 Not in use or not relevant
- 1 All 8<sup>ve</sup> filters in use, each channel sampled sequentially
- 2 All  $\frac{1}{3}$ 8<sup>ve</sup> filters in use, each channel sampled sequentially
- 3 All 8<sup>ve</sup> filters in use, each channel sampled simultaneously
- 4 All  $\frac{1}{3}$ 8<sup>ve</sup> filters in use, each channel sampled simultaneously
- .
- .
- F Go to data type extension for more information.

NIBBLE 5: Intentionally left blank.

NIBBLE 6: Time response applied

- 0 Not in use or not relevant
- 1 True Integral
- 2 Peak Hold
- 3 Impulse Hold
- 4 Fast Hold
- 5 Slow Hold
- 6 Impulse normal
- 7 Fast normal
- 8 Slow normal
- .
- .
- F Go to data type extension for more information

NIBBLE 7: Intentionally left blank

NIBBLE 8: Code buttons used  $B_3B_2B_1B_0 = C_4C_3C_2C_1$

NIBBLE 9: Intentionally left blank

NIBBLE A: Sample time

- 0 Not in use or not relevant
- 1 100 ms
- .

2 125 ms  
3 1 s  
4 2 s  
5 10 s  
6 60 s

·  
·

F Go to data type extension for more information

NIBBLE B: Intentionally left blank

NIBBLE C:  
Calibration offset

NIBBLE D:

NIBBLE E: Bit 0 set if calibrated since last pause, otherwise cleared

NIBBLE F: Bit 3 signifies if there is another data type (0 = NO, 1 = YES)

8 Delimiters for textual information. Default is START OF TEXT - END OF TEXT.

#### Extended Header

If any of the nibbles in the basic data type is set to 'F', the data type extension is inserted before the text. The data type extensions are placed in the order in which they were called, eg NIBBLE 0, NIBBLE 2, etc. The data type extensions are terminated by a "zero" word. If the data type says that a non-standard form is in use (F), the extension may only consist of the zero word, to say that no further explanation is possible. The number of "zero" words must equal the number of data type extensions requested.

This structure runs within the main loop.

```

GET A KEY VALUE
IF KEY == LED ENABLE
THEN SET LEDS ON FLAG
ELSE IF KEY == SHORT LEQ
THEN LCD_LEQ_UPDATE = 1
LCD_MAX_UPDATE = 0
LCD_CUM_UPDATE = 0
LCD_NO_UPDATE = 0
UPDATE_LEDS BYTE
ELSE IF KEY == MAX LEQ
THEN LCD_LEQ_UPDATE = 0
LCD_MAX_UPDATE = 1
LCD_CUM_UPDATE = 0
LCD_NO_UPDATE = 0
UPDATE_LEDS BYTE
ELSE IF KEY == CUM LEQ
THEN LCD_LEQ_UPDATE = 0
LCD_MAX_UPDATE = 0
LCD_CUM_UPDATE = 1
LCD_NO_UPDATE = 0
UPDATE_LEDS BYTE
ELSE IF KEY == LEQ NO
THEN LCD_LEQ_UPDATE = 0
LCD_MAX_UPDATE = 0
LCD_CUM_UPDATE = 0
LCD_NO_UPDATE = 1
UPDATE_LEDS BYTE
ELSE IF ACMODE == 1
THEN IF KEY == PAUSE
THEN ACMODE = 0
FINISH HEADER
UPDATE_LEDS BYTE
ELSE IF KEY == RESET CUM
THEN CUM VALUE = 0
ELSE IF KEY == RELEASE MAX
THEN MAX VALUE = 0
ELSE IF KEY ROW == CODES ROW
THEN CODE STORE = KEY COLUMN NIBBLE
ELSE (IF ACMODE == 0)
THEN IF KEY == CAL
THEN DO NOTHING
ELSE IF KEY == "1/8" OR KEY == "1" OR KEY == "10"
THEN UPDATE_LEDS BYTE
IF KEY == "1/8"
THEN ACTYPE = 1
ELSE IF KEY == "1"
THEN ACTYPE = 8
ELSE IF KEY == "10"
THEN ACTYPE = 80
ACMODE = 1
ELSE DO NOTHING
IF LCD_NO_UPDATE == 1
THEN CONVERT LCD NO TO DISPLAY FORMAT
ELSE IF LCD_LEQ_UPDATE == 1
THEN CONVERT LEQ VALUE TO DISPLAY FORMAT
DISPLAY DATA SELECTED BY LCD UPDATE FLAGS

```

```

IF INTERRUPT DUE TO TXREADY
THEN  IF TXFLAG !=1
      THEN  RTI
        IF RAMFLAG == 0
        THEN  GET CHAR FROM TXPTR
              PUT CHAR INTO TXD
              CLI
              TXPTR++
              IF TXPTR == TXEND
              THEN  TXFLAG = 0
              RTI
ELSE  SAVE PORT2
      P2.0 = TXBANK
      P2.1 = TXPAGE
      GET CHAR FROM TXPTR
      PUT CHAR INTO TXD
      RESTORE PORT2
      CLI
      IF TXHFLG == 1
      THEN  IF TXBANK == 0
            THEN  IF HDRCTR == 6
                  THEN  OFF2 = CHAR
                  ELSE  IF HDRCTR == 7
                        THEN  OFF4 = CHAR
            ELSE  IF HDRCTR == 6
                  THEN  OFF1 = CHAR
                  ELSE  IF HDRCTR == 7
                        THEN  OFF3 = CHAR

      IF TXBANK == 01
      THEN  TXBANK = 0
            RTI
      ELSE  TXBANK = 1
            TXPTR++
            IF TXPTR == E000
            THEN  TXPTR = RAMSTRT
                  TXPAGE = 1
            IF TXHFLG !=0
            THEN  IF TXPTR == TXEND
                  THEN  IF TXPAGE == TXENDPG
                        THEN  TXFLAG = 0
                  RTI
            ELSE  HDRCTR++
                  IF HDRCTR == 16
                  THEN  IF OFF1 == 0
                        THEN  IF OFF2 == 0
                              THEN  IF OFF3 == 0
                                    THEN  IF OFF4 == 0
                                          THEN  TXFLAG = 0
                                                TXHFLG = 0
                                                    RTI
                  HDRSTRT += OFF2.OFF1 DOUBLE
                  HSTRTPG += OFF3 + CARRY
                  TXPAGE = HSTRTPG
                  TXPTR = HDRSTRT
            RTI
ELSE (IF INTERRUPT DUE TO RXREADY OR OVF)
THEN  READ CHAR
      CLI

```



1. The first part of the document discusses the importance of maintaining accurate records of all transactions. It emphasizes that proper record-keeping is essential for the integrity of the financial system and for the ability to detect and prevent fraud.

2. The second part of the document outlines the specific requirements for record-keeping, including the need to maintain original documents and to keep copies of all transactions. It also discusses the importance of regular audits and the need to report any discrepancies immediately.

3. The third part of the document discusses the consequences of failing to maintain accurate records. It notes that failure to do so can result in severe penalties, including fines and imprisonment. It also discusses the importance of cooperating with investigators and providing all necessary information.

4. The fourth part of the document discusses the importance of transparency and accountability in the financial system. It notes that transparency is essential for the confidence of investors and the public, and that accountability is essential for the integrity of the system.

5. The fifth part of the document discusses the importance of ongoing education and training for all personnel involved in the financial system. It notes that ongoing education is essential for staying up-to-date on the latest developments in the field and for ensuring that all personnel are fully qualified to perform their duties.

6. The sixth part of the document discusses the importance of maintaining a strong ethical culture within the financial system. It notes that a strong ethical culture is essential for the integrity of the system and for the ability to detect and prevent fraud.

7. The seventh part of the document discusses the importance of maintaining a strong relationship with the public. It notes that a strong relationship is essential for the confidence of investors and the public, and for the ability to detect and prevent fraud.

8. The eighth part of the document discusses the importance of maintaining a strong relationship with the government. It notes that a strong relationship is essential for the integrity of the system and for the ability to detect and prevent fraud.

9. The ninth part of the document discusses the importance of maintaining a strong relationship with the media. It notes that a strong relationship is essential for the confidence of investors and the public, and for the ability to detect and prevent fraud.

10. The tenth part of the document discusses the importance of maintaining a strong relationship with the industry. It notes that a strong relationship is essential for the integrity of the system and for the ability to detect and prevent fraud.

```

IF CHAR == ESC
THEN TXPTR = START OF ESC MESSAGE IN ROM
TXPAGE = 0
TXEND = END OF ESC MESSAGE IN ROM + 1
TXENDPG = 0
NUMBER MODE = 0
RAMFLAG = 0
TXHFLG = 0
TXFLAG = 1
RTI
ELSE IF NUMBER MODE == 1
THEN PUT CHAR IN RXPTR
INC RXPTR
IF RXPTR >= RXBUF+20
THEN NUMBER MODE = 0
CALCULATE RAMSTART AND RAMEND FROM 16 DIGITS
FROM RXPTR+2 IE IGNORE THE LG CHARACTERS
TXPTR = CALCULATED RAMSTART
TXPAGE = CALCULATED RAMSTART
TXEND = CALCULATED RAMEND
TXENDPG = CALCULATED RAMEND
TXHFLG = 0
RAMFLAG = 1
TXFLAG = 1
TXBANK = 0
RXPTR = RXBUF
RTI
ELSE PUT CHAR INTO RXPTR
INC RXPTR
IF RXPTR >= RXBUF+4
THEN IF MESSAGE IN RXBUF == PR
THEN TXFLAG = 1
TXHFLG = 1
TXPTR = START OF RAM
HEADER START = TXPTR
HDRCTR = 0
RAMFLAG = 1
TXPAGE = 0
HSTRTPG = 0
TXBANK = 1
RXPTR = RXBUF
NUMBER MODE = 0
RTI
ELSE IF MESSAGE IN RXBUF == ID
THEN TXPTR = START OF ID MESSAGE IN ROM
TXPAGE = 0
TXEND = END OF ID MESSAGE IN ROM + 1
TXENDPG = 0
TXFLAG = 1
TXHFLG = 0
RAMFLAG = 0
TXBANK = 0
RXPTR = RXBUF
NUMBER MODE = 0
RTI
ELSE IF MESSAGE IN RXBUF == LG
THEN NUMBER MODE = 1
RTI

```



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LOC	OBJ	LINE	SOURCE STATEMENT
		1	\$ PAGEWIDTH(80) PAGELENGTH(69) DEBUG
		2	;
		3	;
		4	PROGRAM TO MEASURE DOSE BY CONTROLLING A CHARGE
		5	BALANCING INTEGRATOR WITH TWO SELECTABLE BALANCING
		6	CURRENTS, & TO CALCULATE EITHER LEQ OR SOUND EXPOSURE
		7	FROM THE DOSE & TIME DATA.
		8	THE CURRENT SOUND LEVEL IS SAMPLED EVERY 10MS USING AN
		9	A/D CONVERTER, & A SERIES OF 1DB WIDE BINS ARE USED
		10	TO ACCUMULATE DATA FOR CALCULATION OF TWO
		11	SYMMETRICAL PERCENTILES: L10 & L90.
		12	;
		13	;
0003		14	HITIM EQU 03H ;INITIALIZE VARIABLES
0017		15	LPC10H EQU 17H
0070		16	LPC10L EQU 70H
		17	;
		18	;
0000		19	ORG 00H ;SA=00H
0000	040A	20	JMP RESET ;JUMP TO RESET ROUTINE
000A		21	ORG 0AH
000A	27	22	RESET: CLR A
000B	9A0F	23	ANL P2,#0FH ;CLEAR STOP SIGNAL &
		24	; LO & HI CURRENTS
000D	02	25	OUTL BUS,A ;CLEAR BUS
000E	39	26	OUTL P1,A ;CLEAR PORT 1
000F	B87F	27	MOV RO,#7FH ;CLEAR ALL DATA MEMORY
0011	A0	28	CLEAR: MOV @RO,A
0012	E811	29	DJNZ RO,CLEAR
0014	3614	30	WAIT: JTO WAIT ;WAIT UNTIL CHARGE BALANCING
		31	; IS REQU'D BEFORE STARTING
		32	; TIMER - INTEGRATOR DOES NOT
		33	; RESET PROPERLY
		34	;
		35	;
		36	MAIN PROGRAM FOR CONTROLLING METER FUNCTIONS
0016	D5	37	MAIN: SEL R51 ;INITIALIZE R4 TO TIME
0017	BC20	38	MOV R4,#20H ; LEQ CALCULATIONS
0019	2383	39	STARTT: MOV A,#83H ;INITIALIZE TIMER FOR
001B	62	40	MOV T,A ; 10MS PERIOD
001C	55	41	STRT T
001D	148C	42	CALL SLCONV ;PERFORM SOUND LEVEL CONVERSION
001F	EC31	43	DJNZ R4,LEQINT ;EVERY 320MS UPDATE METER O/P
0021	BC20	44	MOV R4,#20H ;RESET R4 TO TIME LEQ CALCS
0023	341E	45	CALL DOSCON ;CONVERT DOSE VALUE
0025	0A	46	IN A,P2 ;LEQ OR SOUND EXPOSURE?
0026	37	47	CPL A ; (INVERT SWITCH LOGIC)
0027	322F	48	JB1 SEXREQ ; SE, JUMP TO SE ROUTINE
0029	3494	49	CALL TIMCON ; LEQ, CONVERT TIME VALUE
002B	5400	50	CALL LEQCAL ;CALCULATE & O/P LEQ ON BUS
002D	0431	51	JMP LEQINT ;BALANCE THE INTEGRATOR
002F	542D	52	SEXREQ: CALL SEXCAL ;CALCULATE & O/P SE ON BUS
0031	145B	53	LEQINT: CALL LEQDA ;PERFORM CHARGE BALANCING
0033	FC	54	MOV A,R4 ;IS MEASUREMENT TIME FINISHED?
0034	0316	55	ADD A,#16H
0036	9619	56	JNZ STARTT ; NO, RESTART TIMER



LOC	OBJ	LINE	SOURCE STATEMENT
		58 ;	
0038	341E	59	CALL DOSCON ; YES, UPDATE DOSE & TIME
003A	3494	60	CALL TIMCON
003C	FC	61	MOV A, R4
003D	37	62	CPL A
003E	17	63	INC A
003F	6F	64	ADD A, R7
0040	0332	65	ADD A, #32H
0042	B81A	66	MOV RO, #1AH ;STORE UPDATED LEQ VALUE IN
0044	A0	67	MOV @RO, A ; R2, REGISTER BANK 1
0045	14C2	68	CALL L1090 ;CALCULATE L10 & L90
0047	8A4F	69	ORL P2, #4FH ;SIGNAL END OF PERIOD & DATA
		70	; READY FOR PRESENTATION
0049	0A	71	SERREQ: IN A, P2 ;TEST FOR REQUESTED DATA
004A	37	72	CPL A ; (INVERT SWITCH LOGIC)
004B	1253	73	JBO L10OUT ;BIT 0 SET, L10 REQUESTED
004D	3257	74	JB1 L90OUT ;BIT 1 SET, L90 REQUESTED
004F	FA	75	MOV A, R2 ;BIT 2 SET, LEQ REQUESTED
0050	02	76	OUTL BUS, A ;OUTPUT LEQ
0051	0449	77	JMP SERREQ ; & RETURN TO SERVICE REQUESTS
0053	FC	78	L10OUT: MOV A, R4
0054	02	79	OUTL BUS, A ;OUTPUT L10
0055	0449	80	JMP SERREQ ; & RETURN TO SERVICE REQUESTS
0057	FB	81	L90OUT: MOV A, R3
0058	02	82	OUTL BUS, A ;OUPUT L90
0059	0449	83	JMP SERREQ ; & RETURN TO SERVICE REQUESTS
		84 ;	
		85 ;	
		86	;LEQ DATA AQUISITION
005B	C5	87	LEQDA: SEL RBO
005C	35	88	DIS TCNTI ;DISABLE INTERUPTS
005D	15	89	DIS I ;
005E	B903	90	MOV R1, #HITIM ;SET MAX NO OF LORAMP
		91	;BEFORE SELECTING HIRAMP
0060	1686	92	LEQTST: JTF TIMINT ;TEST TIME OVERFLOW FLAG
		93	; BEFORE A COMPLETE
		94	; INTEGRATION CYCLE BEGINS
0062	2666	95	JNTO LOCNT ;TEST INTEGRATOR COMPARATOR
0064	0460	96	JMP LEQTST ; UNTIL BALANCING REQUIRED
0066	E975	97	LOCNT: DJNZ R1, LORAMP ;IF HITIM IS NOT EXCEEDED USE
		98	; LORAMP, OTHERWISE CONTINUE
		99 ;	
		100 ;	
0068	8A20	101	HIRAMP: ORL P2, #20H ;SWITCH ON HI CURRENT
		102	; VIA PORT 2 BIT 5
006A	14BD	103	CALL DELAY ;HI CURRENT ON FOR PREDTERMINED
		104	; PERIOD
006C	9A0F	105	ANL P2, #0FH ;SWITCH OFF HI CURRENT
006E	1E	106	INC R6 ;INCREMENT SECOND BYTE OF
		107	; LEQ COUNT
006F	FE	108	MOV A, R6 ;SECOND BYTE OVERFLOW?
0070	965E	109	JNZ LEQTST-2 ; NO, NEXT INTEGRATION
0072	1F	110	INC R7 ; YES, INCREMENT THIRD BYTE
0073	045E	111	JMP LEQTST-2 ;NEXT INTEGRATION
		112 ;	
		113 ;	
0075	8A10	114	LORAMP: ORL P2, #10H ;SWITCH ON LO CURRENT
		115	; VIA PORT 2 BIT 4

Date	Description	Debit	Credit
1901	Jan 1 Balance		100.00
	Jan 10 Cash	50.00	
	Jan 15 Cash	25.00	
	Jan 20 Cash	10.00	
	Jan 25 Cash	75.00	
	Jan 30 Cash	30.00	
	Feb 1 Cash	15.00	
	Feb 5 Cash	40.00	
	Feb 10 Cash	20.00	
	Feb 15 Cash	60.00	
	Feb 20 Cash	10.00	
	Feb 25 Cash	55.00	
	Feb 30 Cash	35.00	
	Mar 1 Cash	20.00	
	Mar 5 Cash	45.00	
	Mar 10 Cash	15.00	
	Mar 15 Cash	70.00	
	Mar 20 Cash	10.00	
	Mar 25 Cash	50.00	
	Mar 30 Cash	30.00	
	Apr 1 Cash	15.00	
	Apr 5 Cash	40.00	
	Apr 10 Cash	20.00	
	Apr 15 Cash	65.00	
	Apr 20 Cash	10.00	
	Apr 25 Cash	55.00	
	Apr 30 Cash	35.00	
	May 1 Cash	20.00	
	May 5 Cash	45.00	
	May 10 Cash	15.00	
	May 15 Cash	70.00	
	May 20 Cash	10.00	
	May 25 Cash	50.00	
	May 30 Cash	30.00	
	Jun 1 Cash	15.00	
	Jun 5 Cash	40.00	
	Jun 10 Cash	20.00	
	Jun 15 Cash	65.00	
	Jun 20 Cash	10.00	
	Jun 25 Cash	55.00	
	Jun 30 Cash	35.00	
	Jul 1 Cash	20.00	
	Jul 5 Cash	45.00	
	Jul 10 Cash	15.00	
	Jul 15 Cash	70.00	
	Jul 20 Cash	10.00	
	Jul 25 Cash	50.00	
	Jul 30 Cash	30.00	
	Aug 1 Cash	15.00	
	Aug 5 Cash	40.00	
	Aug 10 Cash	20.00	
	Aug 15 Cash	65.00	
	Aug 20 Cash	10.00	
	Aug 25 Cash	55.00	
	Aug 30 Cash	35.00	
	Sep 1 Cash	20.00	
	Sep 5 Cash	45.00	
	Sep 10 Cash	15.00	
	Sep 15 Cash	70.00	
	Sep 20 Cash	10.00	
	Sep 25 Cash	50.00	
	Sep 30 Cash	30.00	
	Oct 1 Cash	15.00	
	Oct 5 Cash	40.00	
	Oct 10 Cash	20.00	
	Oct 15 Cash	65.00	
	Oct 20 Cash	10.00	
	Oct 25 Cash	55.00	
	Oct 30 Cash	35.00	
	Nov 1 Cash	20.00	
	Nov 5 Cash	45.00	
	Nov 10 Cash	15.00	
	Nov 15 Cash	70.00	
	Nov 20 Cash	10.00	
	Nov 25 Cash	50.00	
	Nov 30 Cash	30.00	
	Dec 1 Cash	15.00	
	Dec 5 Cash	40.00	
	Dec 10 Cash	20.00	
	Dec 15 Cash	65.00	
	Dec 20 Cash	10.00	
	Dec 25 Cash	55.00	
	Dec 30 Cash	35.00	
	Total	1000.00	1000.00



LOC	OBJ	LINE	SOURCE STATEMENT
0077	14BD	116	CALL DELAY ;LO CURRENT ON FOR PREDETERMINED
		117	; PERIOD
0079	9A0F	118	ANL P2,#0FH ;SWITCH OFF LO CURRENT
007B	1D	119	INC R5 ;INCREMENT FIRST BYTE OF
		120	; LEQ COUNT
007C	FD	121	MOV A,R5 ;FIRST BYTE OVERFLOW?
007D	9660	122	JNZ LEQTST ; NO, NEXT INTEGRATION
007F	1E	123	INC R6 ; YES, INCREMENT SECOND BYTE
0080	FE	124	MOV A,R6 ;SECOND BYTE OVERFLOW?
0081	9660	125	JNZ LEQTST ; NO, NEXT INTEGRATION
0083	1F	126	INC R7 ; YES, INCREMENT THIRD BYTE
0084	0460	127	JMP LEQTST ;NEXT INTEGRATION
0086	1B	128	TIMINT: INC R3 ;INCREMENT LO BYTE OF TIME STORE
0087	FB	129	MOV A,R3
0088	968B	130	JNZ TIMCNT ; & ON OVERFLOW
008A	1C	131	INC R4 ; INCREMENT HI BYTE
008B	83	132	TIMCNT: RET ;RETURN TO MAIN
		133	;
		134	;
		135	;SOUND LEVEL CONVERSION FOR L10/L90 COMPUTATION
008C	D5	136	SLCONV: SEL RB1 ;SELECT REGISTER BANK 1
008D	35	137	DIS TCNTI ;DISABLE INTERRUPTS
008E	15	138	DIS I
008F	BF06	139	MOV R7,#06H ;COUNTER R7=6
0091	27	140	CLR A ;CLEAR A,R6
0092	AE	141	MOV R6,A
0093	BD40	142	MOV R5,#40H ;SET TEST BIT IN R5
		143	;
		144	;
		145	;6 BIT SUCCESSIVE APPROXIMATION ALGORITHM
0095	FD	146	LOOP: MOV A,R5 ;MOVE TEST BIT RIGHT
0096	77	147	RR A ; FROM MSB TO LSB
0097	AD	148	MOV R5,A
0098	4E	149	ORL A,R5 ;ADD IT TO PRESENT VALUE IN R6
0099	39	150	OUTL P1,A ; AND OUTPUT VIA PORT 1
009A	BA04	151	MOV R2,#04H ;TEMP DELAY FOR TESTING
009C	EA9C	152	TIMDEL: DJNZ R2,TIMDEL
009E	56A1	153	JT1 DROP ;OUTPUT TOO LARGE?
		154	; YES, DROP NEW VALUE
00A0	AE	155	MOV R6,A ; NO, SAVE NEW VALUE
00A1	EF95	156	DROP: DJNZ R7,LOOP ;GO ON TO NEXT BIT
		157	;WITH CONVERTED VALUE IN R6
00A3	23FF	158	MOV A,#0FFH ;SET PORT 1 HI TO FORCE
00A5	39	159	OUTL P1,A ; COMPARATOR HI
		160	;
		161	;
		162	;INCREMENT THE APPROPRIATE BIN
00A6	97	163	CLR C ;CLEAR CARRY BIT
00A7	FE	164	MOV A,R6 ;IS CONVERTED VALUE
00A8	03D8	165	ADD A,#0D8H ; WITHIN 40 DB RANGE?
00AA	F6B8	166	JC OLOAD ; NO, INCREMENT OVERLOAD BIN
00AC	FE	167	MOV A,R6 ; YES, RESTORE VALUE
00AD	6E	168	ADD A,R6 ;FORM ADDRESS OF TWO BYTE BIN
00AE	0320	169	ADD A,#20H ;ADD OFFSET ADDRESS
00B0	A8	170	MOV R0,A ;LOAD ADDRESS TO MEM POINTER
00B1	10	171	INC @R0 ;INCREMENT BIN CONTENTS
00B2	F0	172	OVFLOW: MOV A,@R0 ;HAS LO BYTE OVERFLOWED?
00B3	96B7	173	JNZ SLFIN ; NO, JUMP TO END OF SUBROUTINE



LOC	OBJ	LINE	SOURCE STATEMENT
00B5	18	174	INC R0 ; YES, MOVE MEM POINTER
00B6	10	175	INC @R0 ; & INCREMENT HI BYTE
00B7	83	176	SLFIN: RET ;RETURN TO MAIN
00B8	B870	177	OLOAD: MOV R0,#70H ;FORM ADDRESS OF OVERLOAD
00BA	10	178	INC @R0 ; & INCREMENT LC BYTE
00BB	04B2	179	JMP OVFLOW ;RETURN TO TEST LO BYTE
		180	;
		181	;
00BD	BA9D	182	DELAY: MOV R2,#9DH ;PRESET TIME OF 800US
00BF	EABF	183	CHBTIM: DJNZ R2,CHBTIM ; FOR CHARGE BALANCING
00C1	83	184	RET ;RETURN TO LEQDA
		185	;
		186	;
		187	;L10/L90 COMPUTATION FROM BINNED DATA
		188	;L10 COMPUTATION
00C2	97	189	L1090: CLR C ;CLEAR CARRY BIT
00C3	D5	190	SEL RB1 ;SELECT REGISTER BANK 1
00C4	35	191	DIS TCNTI ;DISABLE INTERRUPTS
00C5	15	192	DIS I
00C6	BE17	193	MOV R6,#LPC10H ;LOAD LPC10 TO R6,R7
00C8	BF70	194	MOV R7,#LPC10L
00CA	B872	195	MOV R0,#72H ;LOAD BIN FINNISH ADDRESS
00CC	C8	196	DECBIN: DEC R0 ; TO MEM POINTER
00CD	C8	197	DEC R0
00CE	F8	198	MOV A,R0 ;IS MEM POINTER IN RANGE?
00CF	03E0	199	ADD A,#0EOH ; YES, CONTINUE
00D1	C6DB	200	JZ STL10 ; NO, STORE THIS VALUE!
00D3	3408	201	CALL DSUB ;SUBTRACT (@R0+1)(@R0)
		202	; FROM R6,R7
00D5	E6DB	203	JNC STL10 ;STORE BIN ADDRESS IF CY=0
00D7	FF	204	MOV A,R7 ;R6,R7=0?
00D8	4E	205	ORL A,R6 ; YES, STORE ADDRESS
00D9	96CC	206	JNZ DECBIN ; NO, TRY NEXT BIN
00DB	2320	207	STL10: MOV A,#20H ;USING TWO'S COMPLEMENT
00DD	37	208	CPL A ; & ADDITION, SUBTRACT
00DE	17	209	INC A ; BIN OFFSET ADDRESS
00DF	68	210	ADD A,R0 ; FROM MEM POINTER
00E0	97	211	CLR C ;CLEAR CARRY BIT
00E1	67	212	RRC A ;DIVIDE ADDRESS BY 2
00E2	E3	213	MOVP3 A,@A ;SCALE & OFFSET USING
		214	; LOOK UP TABLE
00E3	03FA	215	ADD A,#0FAH ;L1090/LEQ BALANCE
00E5	AC	216	MOV R4,A ;STORE L10 IN R4
		217	;L90 COMPUTATION
00E6	97	218	CLR C ;CLEAR CARRY BIT
00E7	BE17	219	MOV R6,#LPC10H ;LOAD LPC10 TO R6,R7
00E9	BF70	220	MOV R7,#LPC10L
00EB	B81E	221	MOV R0,#1EH ;LOAD BIN START ADDRESS
00ED	18	222	INCBIN: INC R0 ; TO MEM POINTER
00EE	18	223	INC R0
00EF	F8	224	MOV A,R0 ;IS MEM POINTER IN RANGE?
00F0	0390	225	ADD A,#90H ; YES, CONTINUE
00F2	C6FC	226	JZ STL90 ; NO, STORE THIS VALUE!
00F4	3408	227	CALL DSUB ;SUBTRACT (@R0+1)(@R0)
		228	; FROM R6,R7
00F6	E6FC	229	JNC STL90 ;STORE BIN ADDRESS IF CY=0
00F8	FF	230	MOV A,R7 ;R6,R7=0?
00F9	4E	231	ORL A,R6 ; YES, STORE ADDRESS

1. Name of the project: [Faint text]

2. Name of the client: [Faint text]

3. Name of the consultant: [Faint text]

4. Name of the project manager: [Faint text]

5. Name of the project sponsor: [Faint text]

6. Name of the project steering committee: [Faint text]

7. Name of the project steering committee chair: [Faint text]

8. Name of the project steering committee members: [Faint text]

9. Name of the project steering committee secretary: [Faint text]

10. Name of the project steering committee treasurer: [Faint text]

11. Name of the project steering committee members: [Faint text]

12. Name of the project steering committee members: [Faint text]

13. Name of the project steering committee members: [Faint text]

14. Name of the project steering committee members: [Faint text]

15. Name of the project steering committee members: [Faint text]

16. Name of the project steering committee members: [Faint text]

17. Name of the project steering committee members: [Faint text]

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25. Name of the project steering committee members: [Faint text]

26. Name of the project steering committee members: [Faint text]

27. Name of the project steering committee members: [Faint text]

28. Name of the project steering committee members: [Faint text]

LOC	OBJ	LINE	SOURCE STATEMENT
00FA	96ED	232	JNZ INCBIN ; NO, TRY NEXT BIN
00FC	2320	233	STL90: MOV A, #20H ; USING TWO'S COMPLEMENT
00FE	37	234	CPL A ; & ADDITION, SUBTRACT
00FF	17	235	INC A ; BIN OFFSET ADDRESS
0100	68	236	ADD A, R0 ; FROM MEM POINTER
0101	97	237	CLR C ; CLEAR CARRY BIT
0102	67	238	RRC A ; DIVIDE ADDRESS BY 2
0103	E3	239	MOVP3 A, @A ; SCALE & OFFSET USING
		240	; LOOK UP TABLE
0104	03FA	241	ADD A, #0FAH ; L1090/LEQ BALANCE
0106	AB	242	MOV R3, A ; STORE L90 IN R3
0107	83	243	RET ; RETURN TO MAIN
		244	;
		245	;
		246	; SUBROUTINE FOR SUBTRACTION OF TWO 16 BIT NUMBERS
0108	FO	247	DSUB: MOV A, @R0 ; FORM TWO'S COMPLEMENT
0109	960C	248	JNZ NONZ1 ; OF LO BYTE
010B	17	249	INC A ; OFFSET ZERO BINS
010C	37	250	NONZ1: CPL A
010D	0301	251	ADD A, #01H
010F	AD	252	MOV R5, A ; TEMP STORE (@R0) COMPLEMENT
0110	18	253	INC R0 ; INCREMENT MEM POINTER
0111	FO	254	MOV A, @R0 ; FORM TWO'S COMPLEMENT
0112	37	255	CPL A ; OF HI BYTE & PICK UP
0113	1300	256	ADDC A, #00H ; OVERFLOW
0115	AB	257	MOV R3, A ; TEMP STORE (@R0+1) COMPLEMENT
0116	FD	258	MOV A, R5 ; BEGIN ADDITION
0117	6F	259	ADD A, R7 ; STORE LO ORDER DIFFERENCE
0118	AF	260	MOV R7, A ; IN R7
0119	FB	261	MOV A, R3
011A	7E	262	ADDC A, R6 ; STORE HI ORDER DIFFERENCE
011B	AE	263	MOV R6, A ; IN R6
011C	C8	264	DEC R0 ; DECREMENT MEM POINTER
011D	83	265	RET ; RETURN TO L1090
		266	;
		267	;
		268	; LEQ COMPUTATION FROM ELAPSED TIME DATA STORED IN R3, R4
		269	; AND DOSE DATA STORED IN R5, R6, R7
011E	C5	270	DOSCON: SEL RBO ; SELECT REGISTER BANK 0
011F	35	271	DIS TCNTI ; DISABLE INTERRUPTS
0120	15	272	DIS I
0121	B879	273	MOV R0, #79H ; TEMP STORE R3-R7 @ LOC 79-7D
0123	FB	274	MOV A, R3
0124	A0	275	MOV @R0, A
0125	18	276	INC R0
0126	FC	277	MOV A, R4
0127	A0	278	MOV @R0, A
0128	18	279	INC R0
0129	FD	280	MOV A, R5
012A	A0	281	MOV @R0, A
012B	18	282	INC R0
012C	FE	283	MOV A, R6
012D	A0	284	MOV @R0, A
012E	18	285	INC R0
012F	FF	286	MOV A, R7
0130	AC	287	MOV @R0, A
0131	FF	288	MOV A, R7 ; IS M S BYTE=0?
0132	963B	289	JNZ THRBYT ; NO, 3 BYTE CONVERSION REQU'D



LOC	OBJ	LINE	SOURCE STATEMENT
0134	FE	290	MOV A,R6 ; YES, IS SECOND BYTE=0?
0135	963F	291	JNZ TWOBYT ; NO, 2 BYTE CONVERSION REQU'D
0137	BA01	292	MOV R2,#01H ; YES, 1 BYTE CONVERSION REQU'D
0139	2441	293	JMP DOSLOG ;LOAD APPROPRIATE NUMBER OF
013B	BA03	294	THRBYT: MOV R2,#03H ; BYTES AND PERFORM LOG
013D	2441	295	JMP DOSLOG ; CONVERSION
013F	BA02	296	TWOBYT: MOV R2,#02H
0141	97	297	DOSLOG: CLR C ;CLEAR CARRY BIT
0142	B901	298	MOV R1,#01H ;SET R1=1
0144	FA	299	MOV A,R2 ;SET MEM POINTER TO
0145	0304	300	ADD A,#04H ; THE M S NON ZERO BYTE
0147	A8	301	MOV RO,A
0148	F0	302	MOV A,@RO ;WHICH IS THE MSB OF THIS
0149	F25E	303	JB7 ROTAT1 ; REGISTER THAT IS SET?
014B	19	304	INC R1 ;USE THIS DATA TO SET
014C	D25E	305	JB6 ROTAT1 ; NUMBER OF REQUIRED
014E	19	306	INC R1 ; ROTATIONS IN R1
014F	B25E	307	JB5 ROTAT1
0151	19	308	INC R1
0152	925E	309	JB4 ROTAT1
0154	19	310	INC R1
0155	725E	311	JB3 ROTAT1
0157	19	312	INC R1
0158	525E	313	JB2 ROTAT1
015A	19	314	INC R1
015B	325E	315	JB1 ROTAT1
015D	19	316	INC R1
015E	B87F	317	ROTAT1: MOV RO,#7FH ;CLEAR MEM LOC 7FH
0160	B000	318	MOV @RO,#00H
0162	B87F	319	ROTAT2: MOV RO,#7FH ;STORE NUMBER OF ROTATIONS
0164	10	320	INC @RO ; PERFORMED+1 @ LOC 7FH
0165	C9	321	DEC R1 ;ARE ANY MORE ROTATIONS
0166	F9	322	MOV A,R1 ; REQU'D?
0167	C675	323	JZ LOOKUP ; NO, LOOK UP LOG OF THIS BYTE
0169	FA	324	MOV A,R2 ; YES, SET NO OF BYTES IN ACC
016A	B804	325	MOV RO,#04H ;SET MEM POINTER TO L S BYTE-1
016C	18	326	INCBYT: INC RO ;INCREMENT MEM POINTER
016D	20	327	XCH A,@RO ;ROTATE BYTE LEFT WITH CARRY
016E	F7	328	RLC A
016F	20	329	XCH A,@RO
0170	07	330	DEC A ;HAVE ALL BYTES BEEN ROTATED?
0171	966C	331	JNZ INCBYT ; NO, ROTATE NEXT BYTE
0173	2462	332	JMP ROTAT2 ; YES, TEST IF MORE ROTATIONS
		333	; ARE NEEDED
0175	FA	334	LOOKUP: MOV A,R2 ;LOAD NUMBER OF BYTES USED FOR
0176	A9	335	MOV R1,A ; CONVERSION INTO R1
0177	2304	336	MOV A,#04H ;LOAD LEFT LEFT HAND JUSTIFIED
0179	6A	337	ADD A,R2 ; M S BYTE INTO ACC
017A	A8	338	MOV RO,A
017B	F0	339	MOV A,@RO
017C	9680	340	JNZ NONZ2 ;IF BYTE=0,
017E	2380	341	MOV A,#80H ; LOAD 80H TO ACC
0180	E3	342	NONZ2: MOV P3 A,@A ;LOOK UP LOG OF THIS BYTE
0181	03B0	343	ADD A,#0BOH
0183	0350	344	BYTMUL: ADD A,#50H ;COMPENSATE FOR NUMBER OF
0185	E983	345	DJNZ R1,BYTMUL ; BYTES USED IN CONVERSION
0187	29	346	XCH A,R1
0188	B87F	347	MOV RO,#7FH

1. The first part of the document discusses the importance of maintaining accurate records of all transactions and activities. It emphasizes the need for transparency and accountability in all financial dealings.

2. The second part of the document outlines the various methods and techniques used to collect and analyze data. It includes a detailed description of the experimental procedures and the tools used for data collection.

3. The third part of the document presents the results of the study, including a comparison of the different methods and techniques used. It also discusses the implications of the findings and the potential for future research.

4. The fourth part of the document discusses the challenges and limitations of the study. It highlights the need for further research to address these issues and improve the accuracy and reliability of the data.

5. The fifth part of the document provides a summary of the key findings and conclusions of the study. It also includes a list of references and a bibliography of the sources used in the research.

6. The sixth part of the document discusses the potential applications of the study and the impact of the findings on the field of research. It also includes a list of references and a bibliography of the sources used in the research.

7. The seventh part of the document discusses the future directions of the study and the potential for further research. It also includes a list of references and a bibliography of the sources used in the research.

8. The eighth part of the document provides a final summary of the study and its findings. It also includes a list of references and a bibliography of the sources used in the research.

9. The ninth part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.

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11. The eleventh part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.

12. The twelfth part of the document provides a final summary of the study and its findings. It also includes a list of references and a bibliography of the sources used in the research.

13. The thirteenth part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.

14. The fourteenth part of the document provides a final summary of the study and its findings. It also includes a list of references and a bibliography of the sources used in the research.

15. The fifteenth part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.

16. The sixteenth part of the document provides a final summary of the study and its findings. It also includes a list of references and a bibliography of the sources used in the research.

17. The seventeenth part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.

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24. The twenty-fourth part of the document provides a final summary of the study and its findings. It also includes a list of references and a bibliography of the sources used in the research.

25. The twenty-fifth part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.

26. The twenty-sixth part of the document provides a final summary of the study and its findings. It also includes a list of references and a bibliography of the sources used in the research.

27. The twenty-seventh part of the document discusses the overall significance of the study and its contribution to the field of research. It also includes a list of references and a bibliography of the sources used in the research.



LOC	OBJ	LINE	SOURCE STATEMENT
018A	FO	348	MOV A,@R0
018B	29	349	XCH A,R1 ;LOAD NUMBER OF ROTATIONS
018C	030A	350	ADD A,#0AH ; PERFORMED IN R1 &
018E	03F6	351 BITMUL: ADD A,#0F6H ; SUBTRACT 10 FROM ACC FOR	
0190	E98E	352	DJNZ R1,BITMUL ; EACH ROTATION PERFORMED
0192	AF	353	MOV R7,A ;STORE CONVERTED VALUE IN R7
0193	83	354	RET ;RETURN TO MAIN
		355 ;	
		356 ;	
0194	FC	357 TIMCON: MOV A,R4 ;IS TIME HI BYTE=0?	
0195	969B	358	JNZ TWOTIM ; NO, 2 BYTE CONVERSION REQU'D
0197	BD01	359	MOV R5,#01H ; YES, 1 BYTE CONVERSION REQU'D
0199	249D	360	JMP TIMLOG ;LOAD NUMBER OF BYTES IN R5
019B	BD02	361 TWOTIM: MOV R5,#02H ; & PERFORM LOG CONVERSION	
019D	B901	362 TIMLOG: MOV R1,#01H ;SET R1=1	
019F	FD	363	MOV A,R5 ;SET MEM POINTER TO THE
01A0	0302	364	ADD A,#02H ; M S NON ZERO BYTE
01A2	A8	365	MOV RO,A
01A3	F0	366	MOV A,@RO ;WHICH IS THE MSB OF THIS
01A4	F2B9	367	JB7 ROTAT3 ; REGISTER THAT IS SET?
01A6	19	368	INC R1 ;USE THIS DATA TO SET NUMBER
01A7	D2B9	369	JB6 ROTAT3 ; OF REQU'D ROTATIONS IN R1
01A9	19	370	INC R1
01AA	B2B9	371	JB5 ROTAT3
01AC	19	372	INC R1
01AD	92B9	373	JB4 ROTAT3
01AF	19	374	INC R1
01B0	72B9	375	JB3 ROTAT3
01B2	19	376	INC R1
01B3	52B9	377	JB2 ROTAT3
01B5	19	378	INC R1
01B6	32B9	379	JB1 ROTAT3
01B8	19	380	INC R1
01B9	B87E	381 ROTAT3: MOV RO,#7EH ;CLEAR MEM LOC 7EH	
01BB	B000	382	MOV @RO,#00H
01BD	B87E	383 ROTAT4: MOV RO,#7EH ;STORE NUMBER OF ROTATIONS	
01BF	10	384	INC @RO ; PERFORMED+1 @ LOC 7EH
01C0	C9	385	DEC R1 ;ARE ANY MORE ROTATIONS REQU'D?
01C1	F9	386	MOV A,R1
01C2	C6D0	387	JZ LUKUP ; NO, LOOK UP LOG OF THIS BYTE
01C4	FD	388	MOV A,R5 ; YES, SET NO OF BYTES IN ACC
01C5	B802	389	MOV RO,#02H ;SET MEM POINTER TO L S BYTE-1
01C7	18	390 INKBYT: INC RO ;INCREMENT MEM POINTER	
01C8	20	391	XCH A,@RO ;ROTATE BYTE LEFT WITH CY
01C9	F7	392	RLC A
01CA	20	393	XCH A,@RO
01CB	07	394	DEC A ;HAVE ALL BYTES BEEN ROTATED?
01CC	96C7	395	JNZ INKBYT ; NO, ROTATE NEXT BYTE
01CE	24BD	396	JMP ROTAT4 ; YES, TEST IF MORE ROTATIONS
		397	; ARE NEEDED
01D0	FD	398 LUKUP: MOV A,R5 ;LOAD NUMBER OF BYTES IN R1	
01D1	A9	399	MOV R1,A
01D2	2302	400	MOV A,#02H ;LOAD LH JUSTIFIED M S BYTE
01D4	6D	401	ADD A,R5 ; INTO ACC
01D5	A8	402	MOV RO,A
01D6	F0	403	MOV A,@RO
01D7	96DB	404	JNZ NONZ3 ;IF BYTE=0,
01D9	2380	405	MOV A,#80H ; LOAD 80H TO ACC

STATE OF CALIFORNIA

IN SENATE  
January 12, 1967.

REPORT  
OF THE  
COMMISSIONERS OF THE  
STATE DEPARTMENT OF  
CORRECTIONS

FOR THE YEAR  
ENDING DECEMBER 31, 1966

PREPARED BY  
THE COMMISSIONERS OF THE  
STATE DEPARTMENT OF  
CORRECTIONS

SAFETY

STATE OF CALIFORNIA  
DEPARTMENT OF CORRECTIONS  
SACRAMENTO, CALIFORNIA  
1967

LOC	OBJ	LINE	SOURCE STATEMENT
01DB	E3	406	NONZ3: MOVP3 A,@A ;LOOK UP LOG OF THIS BYTE
01DC	03B0	407	ADD A,#0B0H
01DE	0350	408	BYTCOM: ADD A,#50H ;COMPENSATE FOR NUMBER OF BYTES
01E0	E9DE	409	DJNZ R1,BYTCOM ; USED IN CONVERSION
01E2	29	410	XCH A,R1
01E3	B87E	411	MOV RO,#7EH
01E5	FO	412	MOV A,@RO
01E6	29	413	XCH A,R1 ;LOAD NUMBER OF ROTATIONS
01E7	030A	414	ADD A,#0AH ; PERFORMED IN R1 &
01E9	03F6	415	BITCOM: ADD A,#0F6H ; SUBTRACT 10 FROM ACC FOR
01EB	E9E9	416	DJNZ R1,BITCOM ; EACH ROTATION PERFORMED
01ED	AC	417	MOV R4,A ;STORE CONVERTED VALUE IN R4
01EE	83	418	RET ;RETURN TO MAIN
		419	;
		420	;
0200		421	ORG 200H ;START LEQCAL AT TOP OF PAGE 2
		422	; TO OBVIATE CROSS PAGE JUMPS
0200	BD00	423	LEQCAL: MOV R5,#00H ;INITIALISE OVERFLOW COUNTER
0202	FC	424	MOV A,R4 ;SUBTRACT TIMLOG FROM DOSLOG
0203	37	425	CPL A
0204	17	426	INC A
0205	6F	427	ADD A,R7
0206	E609	428	JNC OFSET1 ;IF CY=1,
0208	1D	429	INC R5 ; INCR OVERFLOW COUNTER
0209	0332	430	OFSET1: ADD A,#32H ;ADD OFFSET
020B	AF	431	MOV R7,A ;TEMP STORE LEQ IN R7
020C	E60F	432	JNC MAGT1 ;IF CY=1,
020E	1D	433	INC R5 ; INCR OVERFLOW COUNTER
020F	FD	434	MAGT1: MOV A,R5 ;IS LEQ IN CORRECT RANGE?
0210	121A	435	JBO OUT1 ; YES, OUTPUT THIS VALUE
0212	3218	436	JB1 FSCAL1 ; NO, IS LEQ OVER OR UNDER
0214	BF00	437	MOV R7,#00H ; RANGE?
0216	441A	438	JMP OUT1 ; UNDER RANGE, OUTPUT -5DB
0218	BFFF	439	FSCAL1: MOV R7,#0FFH ; OVER RANGE, OUTPUT +68DB
021A	FF	440	OUT1: MOV A,R7 ;RETURN MODIFIED LEQ TO ACC
021B	02	441	OUTL BUS,A ;OUTPUT LEQ VIA BUS
021C	B879	442	MOV RO,#79H ;RESTORE R3-7 FROM LOC 79-7D
021E	FO	443	MOV A,@RO
021F	AB	444	MOV R3,A
0220	18	445	INC RO
0221	FO	446	MOV A,@RO
0222	AC	447	MOV R4,A
0223	18	448	INC RO
0224	FO	449	MOV A,@RO
0225	AD	450	MOV R5,A
0226	18	451	INC RO
0227	FO	452	MOV A,@RO
0228	AE	453	MOV R6,A
0229	18	454	INC RO
022A	FO	455	MOV A,@RO
022B	AF	456	MOV R7,A
022C	83	457	RET ;RETURN TO MAIN
		458	;
		459	;
022D	BD00	460	SEXCAL: MOV R5,#00H ;INITIALISE OVERFLOW COUNTER
022F	239C	461	MOV A,#9CH ;SUBTRACT LOG OF 10 SECONDS
0231	6F	462	ADD A,R7 ; FROM DOSLOG
0232	E635	463	JNC OFSET2 ;IF CY=1,

DESCRIPTION OF WORK	QUANTITY	UNIT	ESTIMATED COST
Excavation for foundation	150	cubic meters	15000
Concrete for foundation	150	cubic meters	30000
Reinforcement for foundation	150	cubic meters	15000
Formwork for foundation	150	cubic meters	15000
Excavation for walls	100	cubic meters	10000
Concrete for walls	100	cubic meters	20000
Reinforcement for walls	100	cubic meters	10000
Formwork for walls	100	cubic meters	10000
Excavation for floor	50	cubic meters	5000
Concrete for floor	50	cubic meters	10000
Reinforcement for floor	50	cubic meters	5000
Formwork for floor	50	cubic meters	5000
Excavation for roof	50	cubic meters	5000
Concrete for roof	50	cubic meters	10000
Reinforcement for roof	50	cubic meters	5000
Formwork for roof	50	cubic meters	5000
Excavation for drainage	50	cubic meters	5000
Concrete for drainage	50	cubic meters	10000
Reinforcement for drainage	50	cubic meters	5000
Formwork for drainage	50	cubic meters	5000
Excavation for site	100	cubic meters	10000
Concrete for site	100	cubic meters	20000
Reinforcement for site	100	cubic meters	10000
Formwork for site	100	cubic meters	10000
Excavation for foundation	150	cubic meters	15000
Concrete for foundation	150	cubic meters	30000
Reinforcement for foundation	150	cubic meters	15000
Formwork for foundation	150	cubic meters	15000
Excavation for walls	100	cubic meters	10000
Concrete for walls	100	cubic meters	20000
Reinforcement for walls	100	cubic meters	10000
Formwork for walls	100	cubic meters	10000
Excavation for floor	50	cubic meters	5000
Concrete for floor	50	cubic meters	10000
Reinforcement for floor	50	cubic meters	5000
Formwork for floor	50	cubic meters	5000
Excavation for roof	50	cubic meters	5000
Concrete for roof	50	cubic meters	10000
Reinforcement for roof	50	cubic meters	5000
Formwork for roof	50	cubic meters	5000
Excavation for drainage	50	cubic meters	5000
Concrete for drainage	50	cubic meters	10000
Reinforcement for drainage	50	cubic meters	5000
Formwork for drainage	50	cubic meters	5000
Excavation for site	100	cubic meters	10000
Concrete for site	100	cubic meters	20000
Reinforcement for site	100	cubic meters	10000
Formwork for site	100	cubic meters	10000

LOC	OBJ	LINE	SOURCE STATEMENT
0234	1D	464	INC R5 ; INCR OVERFLOW COUNTER
0235	0332	465	OFSET2: ADD A, #32H ;ADD OFFSET
0237	AF	466	MOV R7, A ;TEMP STORE SE IN R7
0238	E63B	467	JNC MAGT2 ;IF CY=1,
023A	1D	468	INC R5 ; INCR OVERFLOW COUNTER
023B	FD	469	MAGT2: MOV A, R5 ;IS SE IN CORRECT RANGE?
023C	1246	470	JBO OUT2 ; YES, OUTPUT THIS VALUE
023E	3244	471	JB1 FSCAL2 ; NO, IS SE OVER OR UNDER
0240	BF00	472	MOV R7, #00H ; RANGE?
0242	4446	473	JMP OUT2 ; UNDER RANGE, OUTPUT -5DB
0244	BFFF	474	FSCAL2: MOV R7, #OFFH ; OVER RANGE, OUTPUT +68DB
0246	FF	475	OUT2: MOV A, R7 ;RETURN MODIFIED SE TO ACC
0247	02	476	OUTL BUS, A ;OUTPUT SE VIA BUS
0248	B879	477	MOV RO, #79H ;RESTORE R3-7 FROM LOC 79-7D
024A	FO	478	MOV A, @RO
024B	AB	479	MOV R3, A
024C	18	480	INC RO
024D	FO	481	MOV A, @RO
024E	AC	482	MOV R4, A
024F	18	483	INC RO
0250	FO	484	MOV A, @RO
0251	AD	485	MOV R5, A
0252	18	486	INC RO
0253	FO	487	MOV A, @RO
0254	AE	488	MOV R6, A
0255	18	489	INC RO
0256	FO	490	MOV A, @RO
0257	AF	491	MOV R7, A
0258	83	492	RET ;RETURN TO MAIN
		493	;
		494	;
		495	;LOOK UP TABLE FOR SCALING & OFFSET OF L10 & L90,
		496	; & FOR LOG COVERSION, ON PAGE 3 OF PROG MEM
0300		497	ORG 0300H
0300	11	498	DB 17,20,23,27,30,33,36,40
0301	14		
0302	17		
0303	1B		
0304	1E		
0305	21		
0306	24		
0307	28		
0308	2B	499	DB 43,47,50,53,56,60,63,66
0309	2F		
030A	32		
030B	35		
030C	38		
030D	3C		
030E	3F		
030F	42		
0310	45	500	DB 69,73,76,80,83,86,90,93
0311	49		
0312	4C		
0313	50		
0314	53		
0315	56		
0316	5A		
0317	5D		

PHYSICS 201

PHYSICS 202

PHYSICS 203

PHYSICS 204

PHYSICS 205

PHYSICS 206

PHYSICS 207

PHYSICS 208

PHYSICS 209

PHYSICS 210

PHYSICS 211

PHYSICS 212

PHYSICS 213

PHYSICS 214

PHYSICS 215

PHYSICS 216

PHYSICS 217

PHYSICS 218

PHYSICS 219

PHYSICS 220

LOC	OBJ	LINE	SOURCE STATEMENT
0318	61	501	DB 97,100,103,106,110,113,116,119
0319	64		
031A	67		
031B	6A		
031C	6E		
031D	71		
031E	74		
031F	77		
0320	7B	502	DB 123,126,130,133,136,139,143,146
0321	7E		
0322	82		
0323	85		
0324	88		
0325	8B		
0326	8F		
0327	92		
0328	95	503	DB 149,00,00,00,00,00,00,00
0329	00		
032A	00		
032B	00		
032C	00		
032D	00		
032E	00		
032F	00		
0330	00	504	DB 00,00,00,00,00,00,00,00
0331	00		
0332	00		
0333	00		
0334	00		
0335	00		
0336	00		
0337	00		
0338	00	505	DB 00,00,00,00,00,00,00,00
0339	00		
033A	00		
033B	00		
033C	00		
033D	00		
033E	00		
033F	00		
0340	00	506	DB 00,00,00,00,00,00,00,00
0341	00		
0342	00		
0343	00		
0344	00		
0345	00		
0346	00		
0347	00		
0348	00	507	DB 00,00,00,00,00,00,00,00
0349	00		
034A	00		
034B	00		
034C	00		
034D	00		
034E	00		
034F	00		
0350	00	508	DB 00,00,00,00,00,00,00,00
0351	00		

LOC	OBJ	LINE	SOURCE STATEMENT
0352	00		
0353	00		
0354	00		
0355	00		
0356	00		
0357	00		
0358	00	509	DB 00,00,00,00,00,00,00,00
0359	00		
035A	00		
035B	00		
035C	00		
035D	00		
035E	00		
035F	00		
0360	00	510	DB 00,00,00,00,00,00,00,00
0361	00		
0362	00		
0363	00		
0364	00		
0365	00		
0366	00		
0367	00		
0368	00	511	DB 00,00,00,00,00,00,00,00
0369	00		
036A	00		
036B	00		
036C	00		
036D	00		
036E	00		
036F	00		
0370	00	512	DB 00,00,00,00,00,00,00,00
0371	00		
0372	00		
0373	00		
0374	00		
0375	00		
0376	00		
0377	00		
0378	00	513	DB 00,00,00,00,00,00,00,00
0379	00		
037A	00		
037B	00		
037C	00		
037D	00		
037E	00		
037F	00		
0380	46	514	DB 70,70,70,70,70,71,71,71
0381	46		
0382	46		
0383	46		
0384	46		
0385	47		
0386	47		
0387	47		
0388	47	515	DB 71,71,71,71,71,71,71,72
0389	47		
038A	47		
038B	47		



LOC	OBJ	LINE	SOURCE STATEMENT
038C	47		
038D	47		
038E	47		
038F	48		
0390	48	516	DB 72,72,72,72,72,72,72,72
0391	48		
0392	48		
0393	48		
0394	48		
0395	48		
0396	48		
0397	48		
0398	48	517	DB 72,73,73,73,73,73,73,73
0399	49		
039A	49		
039B	49		
039C	49		
039D	49		
039E	49		
039F	49		
03A0	49	518	DB 73,73,73,73,74,74,74,74
03A1	49		
03A2	49		
03A3	49		
03A4	4A		
03A5	4A		
03A6	4A		
03A7	4A		
03A8	4A	519	DB 74,74,74,74,74,74,74,75
03A9	4A		
03AA	4A		
03AB	4A		
03AC	4A		
03AD	4A		
03AE	4A		
03AF	4B		
03B0	4B	520	DB 75,75,75,75,75,75,75,75
03B1	4B		
03B2	4B		
03B3	4B		
03B4	4B		
03B5	4B		
03B6	4B		
03B7	4B		
03B8	4B	521	DB 75,75,75,75,76,76,76,76
03B9	4B		
03BA	4B		
03BB	4B		
03BC	4C		
03BD	4C		
03BE	4C		
03BF	4C		
03C0	4C	522	DB 76,76,76,76,76,76,76,76
03C1	4C		
03C2	4C		
03C3	4C		
03C4	4C		
03C5	4C		

LOC	OBJ	LINE	SOURCE STATEMENT
03C6	4C		
03C7	4C		
03C8	4C	523	DB 76,77,77,77,77,77,77,77
03C9	4D		
03CA	4D		
03CB	4D		
03CC	4D		
03CD	4D		
03CE	4D		
03CF	4D		
03D0	4D	524	DB 77,77,77,77,77,77,77,77
03D1	4D		
03D2	4D		
03D3	4D		
03D4	4D		
03D5	4D		
03D6	4D		
03D7	4D		
03D8	4D	525	DB 77,78,78,78,78,78,78,78
03D9	4E		
03DA	4E		
03DB	4E		
03DC	4E		
03DD	4E		
03DE	4E		
03DF	4E		
03E0	4E	526	DB 78,78,78,78,78,78,78,79
03E1	4E		
03E2	4E		
03E3	4E		
03E4	4E		
03E5	4E		
03E6	4E		
03E7	4F		
03E8	4F	527	DB 79,79,79,79,79,79,79,79
03E9	4F		
03EA	4F		
03EB	4F		
03EC	4F		
03ED	4F		
03EE	4F		
03EF	4F		
03F0	4F	528	DB 79,79,79,79,79,79,79,79
03F1	4F		
03F2	4F		
03F3	4F		
03F4	4F		
03F5	4F		
03F6	4F		
03F7	4F		
03F8	50	529	DB 80,80,80,80,80,80,80,80
03F9	50		
03FA	50		
03FB	50		
03FC	50		
03FD	50		
03FE	50		
03FF	50		

LOC	OBJ	LINE	SOURCE STATEMENT
		530	END
USER SYMBOLS			
BITCOM	01E9	BITMUL 018E	BYTCOM 01DE BYTMUL 0183 CHBTIM 00BF
CLEAR	0011	DECBIN 00CC	DELAY 00BD DOSCON 011E DOSLOG 0141
DROP	00A1	DSUB 0108	FSCAL1 0218 FSCAL2 0244 HIRAMP 0068
HITIM	0003	INCBIN 00ED	INCBYT 016C INKBYT 01C7 L1090 00C2
L10OUT	0053	L90OUT 0057	LEQCAL 0200 LEQDA 005B LEQINT 0031
LEQTST	0060	LOCNT 0066	LOOKUP 0175 LOOP 0095 LORAMP 0075
LPC10H	0017	LPC10L 0070	LUKUP 01D0 MAGT1 020F MAGT2 023B
MAIN	0016	NONZ1 010C	NONZ2 0180 NONZ3 01DB OFFSET1 0209
OFFSET2	0235	OLOAD 00B8	OUT1 021A OUT2 0246 OVFLOW 00B2
RESET	000A	ROTAT1 015E	ROTAT2 0162 ROTAT3 01B9 ROTAT4 01BD
SERREQ	0049	SEXCAL 022D	SEXREQ 002F SLCONV 008C SLFIN 00B7
STARTT	0019	STL10 00DB	STL90 00FC THRBYT 013B TIMCNT 008B
TIMCON	0194	TIMDEL 009C	TIMINT 0086 TIMLOG 019D TWOBYT 013F
TWOTIM	019B	WAIT 0014	

ASSEMBLY COMPLETE, NO ERRORS

Financial Statement

Account Name	2019	2018	2017	2016
Assets				
Cash	100	100	100	100
Accounts Receivable	200	200	200	200
Inventory	300	300	300	300
Property, Plant, and Equipment	400	400	400	400
Intangible Assets	500	500	500	500
Other Assets	600	600	600	600
Liabilities				
Accounts Payable	100	100	100	100
Long-Term Debt	200	200	200	200
Other Liabilities	300	300	300	300
Equity				
Common Stock	100	100	100	100
Retained Earnings	200	200	200	200
Other Equity	300	300	300	300

```

1 "6805" EXPAND
2 ;TABSET 1 17 24 40 43
3 ;*****
4 ;DEFINE LABELS
5 ;*****
<0000> 6 PORTA EQU 00H ;DEFINE PORT LOC
<0001> 7 PORTB EQU 01H
<0002> 8 PORTC EQU 02H
<0003> 9 PORTD EQU 03H
<0008> 10 TDR EQU 08H ;TIMER DATA REG
<0009> 11 TCR EQU 09H ;TIMER CONTROL REG
<0010> 12 LOTIM EQU 10H ;LOTIM MEM LOC
<0011> 13 MDTIM EQU 11H ;MDTIM MEM LOC
<0012> 14 IN1HB EQU 12H ;INTEGRATOR BYTE LABELS
<0013> 15 IN1MB EQU 13H
<0014> 16 IN1LB EQU 14H
<0015> 17 IN2HB EQU 15H
<0016> 18 IN2MB EQU 16H
<0017> 19 IN2LB EQU 17H
<0018> 20 IN3HB EQU 18H
<0019> 21 IN3MB EQU 19H
<001A> 22 IN3LB EQU 1AH
<001B> 23 CLCAD EQU 1BH ;OUT OF RANGE MEM LOC
<001C> 24 TIMCNT EQU 1CH ;TIMER OVERFLOW COUNTER
<001D> 25 TIMBT1 EQU 1DH ;TIME STORE BYTES
<001E> 26 TIMBT2 EQU 1EH
<001F> 27 TIMBT3 EQU 1FH
<0020> 28 BYTCNT EQU 20H ;BYTE & ROTATION STORES
<0021> 29 ROTCNT EQU 21H
<0022> 30 DOSHB EQU 22H ;DOSE WORD STORES
<0023> 31 DOSLB EQU 23H
<0001> 32 MAXRMP EQU 01H ;DEFINE MAX NO OF RAMP
<0080> 33 TAB EQU 80H ;ADDRESS FOR LOOK UP TABLE
34 ;*****
35 ;PORT ALLOCATIONS
36 ; PORT A PORT B PORT C PORT D
37 ;BIT 0 LEQ LO BYTE LEQ HI BYTE LO - HIGH
38 ;BIT 1 " " MID /
39 ;BIT 2 " " INT 1 \
40 ;BIT 3 " STRT OF LEQ INT 2 >BAL EN
41 ;BIT 4 " TEST LIGHT INT 3 /
42 ;BIT 5 " " INT 1 \
43 ;BIT 6 " " INT 2 >BAL FEQ
44 ;BIT 7 " " INT 3 /
45 ;*****
46 ;
07FE 0100 47 CRG 07FEH ;SET RESET VECT ADDR
48 FDB START
49 ;
0100 3F 07 50 CRG 100H ;SET PROG START ADDR
51 START CLR 07H ;CLEAR PORT CONT REG
52 ; 68705R3 SIM QUIRK
53 ;
0102 3F 00 54 CLR PORTA ;CLEAR PORT A,B,C,D
0104 3F 01 55 CLR PORTB ; DATA REGS
0106 3F 02 56 CLR PORTC
0108 3F 03 57 CLR PORTD

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58 ;
010A AE 14 59 LDX #014H ;CLEAR ALL RAM LOC
010C 6F 0F 60 RAMCLR CLR OFH,X
010E 5A 61 DECX
010F 26 FB 62 BNE RAMCLR
63 ;
0111 A6 FF 64 LDA #OFFH
0113 B7 04 65 STA 04H ;SET PORT A & B FOR OUTPUT
0115 B7 05 66 STA 05H
0117 A6 1F 67 LDA #1FH ;SET PORT C DDR
0119 B7 06 68 STA 06H
69 ;
011B A6 04 70 LDA #04H ;INITIALIZE TIMCNT
011D B7 1C 71 STA TIMCNT
011F A6 F4 72 LDA #0F4H
0121 B7 08 73 STA TDR ;INITIALIZE TDR TO 244
0123 A6 48 74 LDA #48H ;CLEAR PRESCALER
0125 B7 09 75 STA TCR
76 ;
0127 A6 02 77 MAIN LDA #(MAXRMP+1)
0129 B7 11 78 STA MDTIM ;RESTORE MDTIM
012B A6 04 79 LDA #(MAXRMP+3)
012D B7 10 80 STA LOTIM ;RESTORE LOTIM
012F 0F09 18 81 LEQDA BRCLR 7,TCR,INTTST ;TIMER OVERFLOW?
82 ; NO, TEST INTEGRATORS
0132 A6 48 83 LDA #48H ; YES, IS 125 MS UP?
0134 B7 09 84 STA TCR ;(CLEAR PRESCALER & TIMER
0136 3A 1C 85 DEC TIMCNT ; OVERFLOW FLAG)
0138 26 10 86 BNE INTTST ; NO, TEST INTEGRATORS
87 ; YES, UPDATE VALUES & DISPLAY
013A CD 0241 88 JSR TIMINT ;RESET TIMER
013D CD 0260 89 JSR DQSCON ;CONVERT DOSE VALUE
0140 CD 039E 90 JSR OUTPUT ;OUTPUT VALUE
0143 AE 0A 91 LDX #0AH ;CLEAR INTEGRATOR REGISTERS
0145 6F 11 92 RECLR CLR 11H,X ; AND CLOAD
0147 5A 93 DECX
0148 26 FB 94 BNE RECLR
95 ;
014A B6 02 96 INTTST LDA PORTC ;INPUT VIA PORT C
014C A4 ED 97 AND #0EDH ;MASK UNWANTED BITS
98 ;IS CHARGE BALANCING REQU'D?
014E 27 D7 99 BEQ LEQDA-8 ; NO, RETURN & RETEST
0150 44 100 LSRA ; YES, SET APPROPRIATE
0151 44 101 LSRA ; BALANCE CURRENT ENABLES
0152 44 102 LSRA
0153 CC 015A 103 JMP LOCNT ;*****DELETE AFTER TEST
0156 43 104 COMA ;DISREGARD OUT OF RANGE INTEGRATORS
0157 BA 1B 105 CRA CLOAD
0159 43 106 COMA
107 ;
015A 3A 10 108 LOCNT DEC LOTIM ;LO CURRENT?
015C 27 03 109 BEQ MDCNT ; NO, TRY MID CURRENT
015E CC 01EC 110 JMP LORAMP ; YES, JUMP TO LORAMP
111 ;
0161 3A 11 112 MDCNT DEC MDTIM ;MID CURRENT?
0163 27 03 113 BEQ HIRAMP ; NO, USE HI CURRENT
0165 CC 01A7 114 JMP MDRAMP ; YES, JUMP TO MDRAMP

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115 ;
0168 AA 03      116 HIRAMP      CRA #03H      ;SWITCH ON HI CURRENTS VIA
016A B7 02      117              STA PORTC    ; PORT C FOR PRE-DETERMINED
016C CD 0233    118              JSR DELAY    ; PERIOD
119 ;
120 ;
016F 44         121              LSRA         ;TEST IF HI CURRENTS WERE USED
0170 44         122              LSRA         ; ON EACH INTEGRATOR, & IF SO
0171 44         123              LSRA         ; INCREMENT APPROPRIATE MEM LOC
0172 24 0C      124              BCC NOTHI1
0174 97         125              TAX
0175 B6 13      126              LDA IN1MB
0177 AB 40      127              ADD #40H
0179 B7 13      128              STA IN1MB
017B 9F         129              TXA
017C 24 02      130              BCC NOTHI1
017E 3C 12      131              INC IN1HB    ;PICK UP OVERFLOWS
0180 44         132 NOTHI1      LSRA
0181 24 0C      133              BCC NOTHI2
0183 97         134              TAX
0184 B6 16      135              LDA IN2MB
0186 AB 40      136              ADD #40H
0188 B7 16      137              STA IN2MB
018A 9F         138              TXA
018B 24 02      139              BCC NOTHI2
018D 3C 15      140              INC IN2HB
018F 44         141 NOTHI2      LSRA
0190 24 0C      142              BCC NOTHI3
0192 97         143              TAX
0193 B6 19      144              LDA IN3MB
0195 AB 40      145              ADD #40H
0197 B7 19      146              STA IN3MB
0199 9F         147              TXA
019A 24 02      148              BCC NOTHI3
019C 3C 18      149              INC IN3HB
019E A6 04      150 NOTHI3      LDA #(MAXRMP+3) ;RESTORE MDTIM
01A0 B7 11      151              STA MDTIM
01A2 3C 10      152              INC LOTIM    ;PREVENT LOTIM GOING -VE
01A4 CC 012F    153              JMP LEQDA
154 ;
01A7 AA 02     155 MDRAMP      CRA #02H      ;SWITCH ON MID CURRENTS VIA
01A9 B7 02     156              STA PORTC    ; PORT C FOR PRE-DETERMINED
01AB CD 0233    157              JSR DELAY    ; PERIOD
158 ;
159 ;
01AE 44         160              LSRA         ;TEST IF MID CURRENTS WERE USED
01AF 44         161              LSRA         ; ON EACH INTEGRATOR, & IF SO
01B0 44         162              LSRA         ; INCREMENT APPROPRIATE MEM LOC
01B1 24 10      163              BCC NOTMD1
01B3 97         164              TAX
01B4 B6 14      165              LDA IN1LB
01B6 AB 80      166              ADD #80H
01B8 B7 14      167              STA IN1LB
01BA 9F         168              TXA
01BB 24 06      169              BCC NOTMD1
01BD 3C 13      170              INC IN1MB
01BF 26 02      171              BNE NOTMD1

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01C1 3C 12      172      INC      IN1HB      ;PICK UP OVERFLOWS
01C3 44         173 NOTMD1  LSRA
01C4 24 10      174      BCC      NOTMD2
01C6 97         175      TAX
01C7 B6 17      176      LDA      IN2LB
01C9 AB 80      177      ADD      #80H
01CB B7 17      178      STA      IN2LB
01CD 9F         179      TXA
01CE 24 06      180      BCC      NOTMD2
01D0 3C 16      181      INC      IN2MB
01D2 26 02      182      BNE      NOTMD2
01D4 3C 15      183      INC      IN2HB
01D6 44         184 NOTMD2  LSRA
01D7 24 10      185      BCC      NOTMD3
01D9 97         186      TAX
01DA B6 1A      187      LDA      IN3LB
01DC AB 80      188      ADD      #80H
01DE B7 1A      189      STA      IN3LB
01E0 9F         190      TXA
01E1 24 06      191      BCC      NOTMD3
01E3 3C 19      192      INC      IN3MB
01E5 26 02      193      BNE      NOTMD3
01E7 3C 18      194      INC      IN3HB
01E9 CC 012B    195 NOTMD3  JMP      LEQDA-4
196 ;
01EC AA 01      197 LORAMP  CRA      #01H      ;SWITCH ON LO CURRENTS VIA
01EE B7 02      198      STA      PORTC ; PORT C FOR PRE-DETERMINED
01F0 CD 0233    199      JSR      DELAY ; PERIOD
200 ;
201 ;
01F3 44         202      LSRA      ;TEST IF LO CURRENTS WERE USED
01F4 44         203      LSRA      ; ON EACH INTEGRATOR, & IF SO
01F5 44         204      LSRA      ; INCREMENT APPROPRIATE MEM LOC
01F6 24 0A      205      BCC      NOTLO1
01F8 3C 14      206      INC      IN1LB
01FA 26 06      207      BNE      NOTLO1
01FC 3C 13      208      INC      IN1MB      ;PICK UP OVERFLOWS
01FE 26 02      209      BNE      NOTLO1
0200 3C 12      210      INC      IN1HB      ;PICK UP OVERFLOWS OF OVERFLOWS
0202 44         211 NOTLO1  LSRA
0203 24 14      212      BCC      NOTLO2
0205 3C 17      213      INC      IN2LB
0207 26 10      214      BNE      NOTLO2
0209 3C 16      215      INC      IN2MB
020B 97         216      TAX      ;STOP BALANCING INTEGRATOR 1
020C B6 1B      217      LDA      CLOAD
020E AA 04      218      CRA      #04H
0210 B7 1B      219      STA      CLOAD
0212 9F         220      TXA
0213 3D 16      221      TST      IN2MB
0215 26 02      222      BNE      NOTLO2
0217 3C 15      223      INC      IN2HB
0219 44         224 NOTLO2  LSRA
021A 24 14      225      BCC      NOTLO3
021C 3C 1A      226      INC      IN3LB
021E 26 10      227      BNE      NOTLO3
0220 3C 19      228      INC      IN3MB

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0222 97          229          TAX          ;STOP BALANCING INTEGRATOR 2
0223 B6 1B      230          LDA          CLOAD
0225 AA 08      231          CRA          #08H
0227 B7 1B      232          STA          CLOAD
0229 9F          233          TXA
022A 3D 19      234          TST          IN3MB
022C 26 02      235          BNE          NOTLO3
022E 3C 18      236          INC          IN3HB
0230 CC 012F    237 NOTLO3    JMP          LEQDA
                238 ;
                239 ;
0233 AE 14      240 DELAY      LDX          #14H          ;SUBROUTINE TO PROVIDE
0235 5A          241 DELLP      DECX         ; DELAY OF 96 E-6 S (* OAH)
0236 26 FD      242          BNE          DELLP
0238 97          243          TAX
0239 B6 02      244          LDA          PORTC
023B A4 E0      245          AND          #0E0H          ;TURN BALANCE CURRENTS OFF
023D B7 02      246          STA          PORTC
023F 9F          247          TXA
0240 81          248          RTS          ;RETURN TO MAIN
                249 ;
0241 B6 01      250 TIMCNT    LDA          PORTB          ;SIGNAL END OF PERIOD BY SETTING
0243 AA 08      251          ORA          #08H          ; A 1 ON PORT B BIT 3
0245 B7 01      252          STA          PORTB
0247 A6 04      253          LDA          #04H          ;RESET TIMCNT
0249 B7 1C      254          STA          TIMCNT
024B B6 08      255          LDA          TDR          ;FIND TIME SINCE INT WAS FLAGGED
024D AB F4      256          ADD          #0F4H          ; SUBTRACT THIS FROM 244 ...
024F B7 08      257          STA          TDR          ; ... & RESET THE TIMER
0251 A6 48      258          LDA          #48H
0253 B7 09      259          STA          TCR
0255 3C 1D      260          INC          TIMBT1          ;TIME REGISTERS NOT USED ON
0257 26 06      261          BNE          TIMBT2          ; FIRST PROTOTYPE - SHORT LEQ
0259 3C 1E      262          INC          TIMBT2          ; ONLY
025B 26 02      263          BNE          TIMBT3
025D 3C 1F      264          INC          TIMBT3
025F 81          265 TIMBT3    RTS          ;RETURN TO MAIN
                266 ;
0260 041B 03    267 DOSCON    BRSET 2,CLOAD,IN2TST ;INT 1 O/LOAD?
                268          ; YES, TEST INT 2
0263 CC 0266    269          JMP          IN1OK          ; NO, USE INT 1 CR 2
0266 061B 61    270 IN2TST    BRSET 3,CLOAD,IN2OK ;INT2 O/LOAD?
0269 CC 02CA    271          JMP          IN2OK          ; NO, USE INT 2 CR 3
026C 3F 21      272 IN3OK     CLR          ROTCNT          ; YES, USE INT 3
026E 3F 23      273          CLR          DOSLB
0270 3F 22      274          CLR          DOSHB
0272 98          275          CLC
0273 A6 02      276          LDA          #02H          ;INITIALIZE BYTCNT
0275 B7 20      277          STA          BYTCNT
0277 B6 18      278          LDA          IN3HB
0279 26 10      279          BNE          IN33B
027B B6 19      280          LDA          IN3MB
027D 26 0A      281          BNE          IN32B
027F B6 1A      282          LDA          IN3LB
0281 26 04      283          BNE          IN31B          ;IF ALL BYTES ARE ZERO
0283 A6 01      284          LDA          #01H          ; SET IN3LB=1
0285 B7 1A      285          STA          IN3LB

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0287 3A 20      286 IN31B      DEC   BYTCNT      ;STORE NUMBER OF NON-ZERO
0289 3A 20      287 IN32B      DEC   BYTCNT      ; BYTES-1 IN BYTCNT
028B 5F         288 IN33B      CLRX
028C 5C         289 IN3ROT      INCX      ;STORE REQUIRED NUMBER OF
028D 48         290           LSLA      ; ROTATIONS IN X
028E 24 FC      291           BCC   IN3ROT
0290 3C 21      292 ROT3        INC   ROTCNT      ;ROTATE ALL BYTES THE REQUIRED
0292 5A         293           DECX      ; NUMBER OF TIMES
0293 27 09      294           BEQ   LOOK3
0295 38 1A      295           LSL   IN3LB
0297 39 19      296           RCL   IN3MB
0299 39 18      297           RCL   IN3HB
029B CC 0290    298           JMP   ROT3
029E B6 20      299 LOOK3       LDA   BYTCNT
02A0 AB 1A      300           ADD   #IN3LB      ;LOOK-UP THIS BYTE
02A2 97         301           TAX
02A3 FE         302           LDY   X
02A4 F6         303           LDA   X
02A5 AB 1E      304           ADD   #01EH
02A7 A0 1E      305 ROTC3       SUB   #01EH      ;COMPENSATE FOR NUMBER OF
02A9 3A 21      306           DEC   ROTCNT      ; ROTATIONS PERFORMED
02AB 26 FA      307           BNE   ROTC3
02AD 3D 20      308           TST   BYTCNT
02AF 27 0E      309           BEQ   OUP3
02B1 AB F1      310 BYTCM3     ADD   #0F1H      ;COMPENSATE FOR NUMBER OF
02B3 97         311           TAX      ; BYTES USED IN CONVERSION
02B4 B6 22      312           LDA   DOSHB
02B6 A9 00      313           ADC   #00H
02B8 B7 22      314           STA   DOSHB
02BA 9F         315           TXA
02BB 3A 20      316           DEC   BYTCNT
02BD 26 F2      317           BNE   BYTCM3     ;EXITS WITH DOSE DATA IN
02BF AB A8      318 OUP3       ADD   #0A3H      ; DOSHB,DOSLB
02C1 B7 23      319           STA   DOSLB      ;ADD OFFSET BETWEEN INTEGRATORS
02C3 B6 22      320           LDA   DOS1B
02C5 A9 02      321           ADC   #02H
02C7 B7 22      322           STA   DOSHB
02C9 81         323           RTS
02CA 3F 21      324 IN2OK      CLR   ROTCNT      ;RETURN TO MAIN
02CC 3F 23      325           CLR   DOSLB      ;USE INT 2
02CE 3F 22      326           CLR   DOSHB
02D0 98         327           CLC
02D1 A6 02      328           LDA   #02H      ;INITIALIZE BYTCNT
02D3 B7 20      329           STA   BYTCNT
02D5 97         330           TAX
02D6 B6 01      331           LDA   PORTB      ;TEMP LINE FOR DEBUG
02D8 A8 80      332           EOR   #080H      ; TOGGLE BIT 7 PORT B IF IT
02DA B7 01      333           STA   PORTB      ; GETS HERE!
02DC 9F         334           TXA
02DD B6 15      335           LDA   IN2HB
02DF 26 28      336           BNE   IN23B
02E1 97         337           TAX
02E2 B6 01      338           LDA   PORTB      ;TEMP LINE FOR DEBUG
02E4 A8 40      339           EOR   #040H      ; TOGGLE BIT 6 PORT B IF IT
02E6 B7 01      340           STA   PORTB      ; GETS HERE!
02E8 9F         341           TXA
02E9 B6 16      342           LDA   IN2MB

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LOCATION OBJECT CODE LINE SOURCE LINE

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02EB 26 1A      343      BNE    IN22B
02ED 97         344      TAX
02EE B6 01      345      LDA    PCRTB      ;TEMP LINE FOR DEBUG
02FO A8 20      346      EOR    #020H      ; TOGGLE BIT 5 PORT B IF IT
02F2 B7 01      347      STA    PCRTB      ; GETS HERE!
02F4 9F         348      TXA
02F5 B6 17      349      LDA    IN2LB
02F7 26 0C      350      BNE    IN21B      ;IF ALL BYTES ARE ZERO
02F9 A6 01      351      LDA    #01H      ; SET IN2LB=1
02FB B7 17      352      STA    IN2LB
02FD 97         353      TAX
02FE B6 01      354      LDA    PCRTB      ;TEMP LINE FOR DEBUG
0300 A8 10      355      EOR    #010H      ; TOGGLE BIT 4 PORT B IF IT
0302 B7 01      356      STA    PCRTB      ; GETS HERE!
0304 9F         357      TXA
0305 3A 20      358 IN21B  DEC    BYTCNT      ;STORE NUMBER OF NON-ZERO
0307 3A 20      359 IN22B  DEC    BYTCNT      ; BYTES-1 IN BYTCNT
0309 5F         360 IN23B  CLRX
030A 5C         361 IN2ROT INCX                ;STORE REQUIRED NUMBER OF
030B 48         362      LSLA                ; ROTATIONS IN X
030C 24 FC      363      BCC    IN2ROT
030E 3C 21      364 ROT2  INC    ROTCNT      ;ROTATE ALL BYTES THE REQUIRED
0310 5A         365      DECX                ; NUMBER OF TIMES
0311 27 09      366      BEQ    LOOK2
0313 38 17      367      LSL    IN2LB
0315 39 16      368      RCL    IN2MB
0317 39 15      369      RCL    IN2HB
0319 CC 030E    370      JMP    ROT2
031C B6 20      371 LOOK2 LDA    BYTCNT
031E AB 17      372      ADD    #IN2LB
0320 97         373      TAX
0321 FE         374      LDX    X            ;LOOK-UP THIS BYTE
0322 F6         375      LDA    X
0323 AB 1E      376      ADD    #01EH
0325 A0 1E      377 ROTM2  SUB    #01EH      ;COMPENSATE FOR NUMBER OF
0327 3A 21      378      DEC    ROTCNT      ; ROTATIONS PERFORMED
0329 26 FA      379      BNE    ROTM2
032B 3D 20      380      TST    BYTCNT
032D 27 0E      381      BEQ    OUTF2
032F AB F1      382 BYTM2  ADD    #0F1H      ;COMPENSATE FOR NUMBER OF
0331 97         383      TAX                ; BYTES USED IN CONVERSION
0332 B6 22      384      LDA    DOSHB
0334 A9 00      385      ADC    #00H
0336 B7 22      386      STA    DOSHB
0338 9F         387      TXA
0339 3A 20      388      DEC    BYTCNT
033B 26 F2      389      BNE    BYTM2      ;EXITS WITH DOSE DATA IN
033D AB 54      390 OUTF2 ADD    #054H      ; DOSHB,DOSLB
033F B7 23      391      STA    DOSLB      ;ADD OFFSET BETWEEN INTEGRATORS
0341 B6 22      392      LDA    DOSHB
0343 A9 01      393      ADC    #01H
0345 B7 22      394      STA    DOSHB
0347 81         395      RTS                ;RETURN TO MAIN
0348 3F 21      396 INOK  CLR    ROTCNT      ;USE INT 1
034A 3F 23      397      CLR    DOSLB
034C 3F 22      398      CLR    DOSHB
034E 98         399      CLC

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034F A6 02      400      LDA      #02H      ;INITIALIZE BYTCNT
0351 B7 20      401      STA      BYTCNT
0353 B6 12      402      LDA      IN1HB
0355 26 10      403      BNE      IN13B
0357 B6 13      404      LDA      IN1MB
0359 26 0A      405      BNE      IN12B
035B B6 14      406      LDA      IN1LB
035D 26 04      407      BNE      IN11B      ;IF ALL BYTES ARE ZERO
035F A6 01      408      LDA      #01H      ; SET IN1LB=1
0361 B7 14      409      STA      IN1LB
0363 3A 20      410 IN11B      DEC      BYTCNT      ;STORE NUMBER OF NON-ZERO
0365 3A 20      411 IN12B      DEC      BYTCNT      ; BYTES-1 IN BYTCNT
0367 5F         412 IN13B      CLRX
0368 5C         413 IN1ROT      INCX      ;STORE REQUIRED NUMBER OF
0369 48         414          LSLA      ; ROTATIONS IN X
036A 24 FC      415          BCC      IN1ROT
036C 3C 21      416 ROT1      INC      ROTCNT      ;ROTATE ALL BYTES THE REQUIRED
036E 5A         417          DECX      ; NUMBER OF TIMES
036F 27 09      418          BEQ      LOOK1
0371 38 14      419          LSL      IN1LB
0373 39 13      420          RCL      IN1MB
0375 39 12      421          RCL      IN1HB
0377 CC 036C    422          JMP      ROT1
037A B6 20      423 LOOK1      LDA      BYTCNT
037C AB 14      424          ADD      #IN1LB
037E 97         425          TAX
037F FE         426          LDX      X      ;LOOK-UP THIS BYTE
0380 F6         427          LDA      X
0381 AB 1E      428          ADD      #01EH
0383 A0 1E      429 ROTCM1     SUB      #01EH      ;COMPENSATE FOR NUMBER OF
0385 3A 21      430          DEC      ROTCNT      ; ROTATIONS PERFORMED
0387 26 FA      431          BNE      ROTCM1
0389 3D 20      432          TST      BYTCNT
038B 27 0E      433          BEQ      OUTP1
038D AB F1      434 BYTCM1     ADD      #0F1H      ;COMPENSATE FOR NUMBER OF
038F 97         435          TAX      ; BYTES USED IN CONVERSION
0390 B6 22      436          LDA      DOSHB
0392 A9 00      437          ADC      #00H
0394 B7 22      438          STA      DOSHB
0396 9F         439          TXA
0397 3A 20      440          DEC      BYTCNT
0399 26 F2      441          BNE      BYTCM1      ;EXITS WITH DOSE DATA IN
039B B7 23      442 OUTP1      STA      DOSLB      ; DOSHB,DOSLB
039D 81         443          RTS      ;RETURN TO MAIN
444 ;
039E B6 23      445 OUTPUT     LDA      DOSLB      ;OUTPUT VALUE - LO BYTE
03A0 B7 00      446          STA      PORTA      ; VIA PORT A ...
03A2 B6 01      447          LDA      PORTB
03A4 A4 F0      448          AND      #0F0H      ; ... AND HI BYTE VIA PORT B
03A6 BA 22      449          ORA      DOSHB      ; SETTING BIT 3 TO 0 TO SIGNAL
03A8 B7 01      450          STA      PORTB      ; NEW VALUE OUTPUT
03AA 81         451          RTS      ;RETURN TO MAIN
452 ;
453 ;
454 ;DECIDE WHICH INTEGRATOR IS TELLING THE TRUTH
455 ;
456 ;PERFORM LOG CONVERSION ON THE APPROPRIATE DOSE STORES

```

457 ;  
458 ;PERFORM LOG CONVERSION ON THE TIME REGISTERS \*\*\* NOT REQUIRED FOR  
459 ; SHORT LEQ \*\*\*  
460 ;FORM THE CORRECT VALUE OF LEQ  
461 ;  
462 ;OVERALL OR LAST LEQ? \*\*\* SHORT LEQ ONLY FOR FIRST TEST \*\*\*  
463 ;  
464 ;OUTPUT THE CORRECT VALUE OF LEQ

```

466 ;*****
467 ;LOOK-UP TABLE FOR LOG CONVERSION      A ← 100*LOG10(A)
468 ;*****
469          ORG      TAB
0080 D3D3D3D4D4 470          FCB      211,211,211,212,212
0085 D4D5D5D5D6 471          FCB      212,213,213,213,214
008A D6D6D7D7D7 472          FCB      214,214,215,215,215
008F D8D8D8D8D9 473          FCB      216,216,216,216,217
0094 D9D9DADADA 474          FCB      217,217,218,218,218
0099 DADBDBDBDC 475          FCB      218,219,219,219,220
009E DDCDCDDDD 476          FCB      220,220,220,221,221
00A3 DDDDEDEDE 477          FCB      221,221,222,222,222
00A8 DFDFFDFDF 478          FCB      223,223,223,223,224
00AD EDEDEDEE1E1 479          FCB      224,224,224,225,225
00E2 E1E1E2E2E2 480          FCB      225,225,226,226,226
00B7 E2E2E3E3E3 481          FCB      226,226,227,227,227
00BC E3E4E4E4E4 482          FCB      227,228,228,228,228
00C1 E5E5E5E5E5 483          FCB      229,229,229,229,229
00C6 E6E6E6E6E7 484          FCB      230,230,230,230,231
00CB E7E7E7E7E8 485          FCB      231,231,231,231,232
00D0 E8E8E8E8E9 486          FCB      232,232,232,232,233
00D5 E9E9E9E9EA 487          FCB      233,233,233,233,234
00DA EAEAEAEAE 488          FCB      234,234,234,234,235
00DF EBEBEBEBEC 489          FCB      235,235,235,235,236
00E4 ECECECECED 490          FCB      236,236,236,236,237
00E9 EDEDEDEDED 491          FCB      237,237,237,237,237
00EE EEEEEEEEE 492          FCB      238,238,238,238,238
00F3 EFEFEFEFEF 493          FCB      239,239,239,239,239
00F8 FFFOFOF 494          FCB      239,240,240,240,240
00FD FOF 495          FCB      240,240,241
496 ;
497          END

```

Errors= 0

MODULE LIST

- 1 A.LABELS
- 2 A.RESET
- 3 A.RDKEYBD
- 4 A.BCDCONV
- 5 A.MAIN
- 6 A.RDKEYBD
- 7 A.CALMOD
- 8 A.KEYINT
- 9 A.PAUSE
- 10 A.DISPLAY
- 11 A.BCDCONV
- 12 A.BCDCONV
- 13 A.BCDCONV
- 14 A.LCDISP
- 15 A.TIMINT
- 16 A.BCDCONV
- 17 A.BCDCONV
- 18 A.SERIAL
- 19 A.ROMTX
- 20 A.ROMTX
- 21 A.ROMTX
- 22 A.ROMTX
- 23 A.TEST
- 24 A.TABLES
- 25 A.STRING
- 26 A.MONITOR
- 27 A.INTVECT

```

00000001          LIST      ON
                  ;LIST ON ENABLES LISTING AND MAY BE USED BEFORE ONE MOD
                  ULE TO PRINT THAT ONE ONLY. USE LIST OFF TO DISABLE A
                  FTER THE MODULE(S) TO BE LISTED.

                  ;MODULE ON SENDS ANY PRINT OUTPUT TO PRINTER INSTEAD O
                  F THE SCREEN

00000000          HEADER   "CRL 2.36 SHO
00000000          RT Leq DATA A
00000000          QUISITION UNI
00000000          T"
00000001          SYMTAB   ON          symbol table enabled

00000000          EPROM    "      0

00000000          IF      EPROM=1
                  OBSSEND   1,C,0,"236OBJ send object code to disc
                  "
                  OBFORM    1
no load or exec address specified
;          OBSSEND   6,2764,128,0,0
;          OBSSEND   4,7
00000000          ELSE

00000006          OBSSEND   6,2764,128,0,
00000006          0
00000001          OBFORM    1          straight binary (1,0,0,"
00000001          236OBJ")

00000000          ENDIF

                  ;FOR EPROM, STORE OBJECT CODE ON DISK USING OBSSEND 1,0,
                  0,"236OBJ"/OBFORM 2 THEN WHEN THE EPROMER SOFTWARE PRO
                  MPTS FOR FILENAME, GIVE "236OBJ". FOR PORTAL U
                  SE OBSSEND 6,2764,128,C,0 AND OBSSEND 1.

*****

0000E000          ORG      $E000          origin for program code

0000E000          A.LABELS          module to define labels

```



A.LABELS MODULE

;module to define all the labels used in the CRL236 program .....these will be GLOBAL

\*\*\*\*\*

;labels used to refer to HD6303X internal registers

; I/O registers + control

00000001	PORT2DDR	=	\$01	port2 data direction register
00000001				
00000003	PORT2	=	\$03	
00000014	RAMPOR5	=	\$14	internal RAM & port5 control register
00000014				
00000015	PORT5	=	\$15	
00000016	PORT6DDR	=	\$16	port6 data direction register
00000016				
00000017	PORT6	=	\$17	

; timer 1 registers

00000009	FRC	=	\$09	free-running counter (high byte)
00000009				

0000000B	OCR1	=	\$0B	output compare register 1 (high byte)
0000000B				

00000019	OCR2	=	\$19	output compare register 2 (high byte)
00000019				

0000000D	ICR	=	\$0D	input capture register
----------	-----	---	------	------------------------

00000008	TCSR1	=	\$08	timer control/status register 1
00000008				

0000000F	TCSR2	=	\$0F	timer control/status register 2
0000000F				

; timer 2 registers

0000001D	T2CNT	=	\$1D	timer 2 up counter
----------	-------	---	------	--------------------

0000001C	TCONR	=	\$1C	time constant register
----------	-------	---	------	------------------------

0000001B	TCSR3	=	\$1B	timer control/status register
0000001B				

; serial communications interface registers

00000011	TRCSR1	=	\$11	transmit/receive control status register
00000011				

00000010	RMCR	=	\$10	transmit rate/mode control register
00000010				

00000013	TDR	=	\$13	transmit data register
----------	-----	---	------	------------------------

00000012	RDR	=	\$12	receive data register
----------	-----	---	------	-----------------------



```

0000001E      TRCSR2      =      $1E
*****

;labels used to refer to external      peripherals
;A-D start conversion/read location

00000031      ADST        =      $31
00000030      ADRD        =      $30
00000037      ADLOAD     =      $37

;LCD display driver digits

00000032      LCDIG      =      $32
;                $33
;                $34
;                $35

;LED latch

00000036      LEDS       =      $36
*****

;labels used for HD6303X internal RAM locations

;location used to count the number of time loops
00000040      TLOOPCNT   =      $40
;keyboard press storage locations
00000041      KEYVAL     =      $41      row data in low nibble,
00000041      ;                column data in high nibble
00000041      ;                le
00000042      KEYCNT     =      $42      location used to count n
00000042      ;                o of key tests
00000043      KEYTEMP    =      $43      temp store of key press
;LCD display output value location
00000044      LCDWORD    =      $44      low byte location
;                $45
;timer phase flag
00000046      TFLAG      =      $46
;locations for leq computation
00000047      ACTYPE     =      $47
00000048      CODE       =      $48
00000049      CHDSTRT    =      $49
;                $4A
;                $4B
0000004C      CUMBIN     =      $4C
;                $4D
0000004E      CUMBCD     =      $4E
;                $4F
00000050      DATA      =      $50
;                $51
00000052      DATACNT    =      $52
;                $53
;                $54
00000055      ERRFLAG    =      $55

```



```

00000056      HDWCTR      =      $56
00000057      HLPTR       =      $57
;
;                    $58
00000059      LEDSRG     =      $59
0000005A      MAXBIN     =      $5A
;
;                    $5B
0000005C      MAXBCD     =      $5C
;
;                    $5D
0000005E      NOBIN      =      $5E
;
;                    $5F
00000060      RAMPNTR    =      $60
;
;                    $61
00000062      RAMPNTB    =      $62
00000063      RAMPSTR    =      $63
;
;                    $64
00000065      RAMPBSTR   =      $65
00000066      RUNBIN     =      $66
;
;                    $67
;                    $68
00000069      TOTALCNT  =      $69
;operating mode flags
0000006A      ACMODE     =      $6A
0000006B      DBLANKF   =      $6B
0000006C      HDRFLD    =      $6C
0000006D      LCDMAXUP  =      $6D
0000006E      LCDCUMUP  =      $6E
0000006F      LCDLEQUP  =      $6F
00000070      NOTYPE    =      $70

00000071      LCDNOUP   =      $71

00000072      LEDSONF   =      $72
00000073      RAMFULL   =      $73

;communications scratch & buffers
00000074      DSCR7CH   =      $74
;
;                    $75
00000076      HI32VL1   =      $76
;
;                    $77
00000078      LO32VL1   =      $78
;
;                    $79
0000007A      HI32VL2   =      $7A
;
;                    $7B
0000007C      LO32VL2   =      $7C
;
;                    $7D
0000007E      NUMMODE   =      $7E
0000007F      P2SAVE    =      $7F
00000080      RXBUF     =      $80
;RXBUF IS 20H BYTES LONG
000000A0      TXPTR     =      $A0
;
;                    $A1
000000A2      TXEND     =      $A2
;
;                    $A3
000000A4      TXFLAG    =      $A4
000000A5      TXHFLG    =      $A5
000000A6      HDRSTRT   =      $A6
;
;                    $A7
000000A8      HDRCTR    =      $A8
000000A9      RXPTR     =      $A9

```



```

; $AA
000000AB TXBYTE = $AB
000000AC TXBANK = $AC
000000AD TXENDPG = $AD
000000AE RAMFLAG = $AE
000000AF SCRATCH = $AF
000000B0 OFFSET4 = $B0
000000B1 OFFSET3 = $B1
000000B2 OFFSET2 = $B2
000000B3 OFFSET1 = $B3
000000B4 HSTRTPG = $B4
000000B5 BYTCTR = $B5
000000B6 LINCTR = $B6
000000B7 PENDFLG = $B7
000000B8 TXPPEND = $B8
; $B9
000000BA TXPEPEND = $BA
000000BB TXEPEND = $BB
; $BC
000000BD TXEBPEND = $BD
000000BE KENCNT = $BE
000000BF ROTCNT = $BF
000000C0 MONFLG = $C0
000000C1 NOBCD = $C1
; $C2
000000C3 BCDOVF = $C3
000000C4 CODUSE = $C4
000000C5 KENFLG = $C5
000000C6 TOGLCNT = $C6
000000C7 CALFLG = $C7
000000C8 RUNBCD = $C8
; $C9
000000CA DATADIF = $CA
; $CB
000000CC CUMDOSE = $CC
; $CD
; $CE
000000CF CUMTIME = $CF
; $D0
; $D1
000000D2 LOGTIME = $D2
; $D3
; $D4
000000D5 CALOFF = $D5
; $D6
000000D7 ERRSTAT = $D7
000000D8 ERRHOLD = $D8
000000D9 P2BACK = $D9
000000DA CALDNF = $DA
000000DB LINASTR = $DB
000000DC CALVAL = $DC
; $DD
000000DE STAKPTR = $DE
; $DF
000000E0 CALKCNT = $E0
000000E1 MEMLBIN = $E1
; $E2
000000E3 MEMLBCD = $E3
; $E4

```





; \$E5

\*\*\*\*\*

```

;constants
00000000 ADPSU      =      %00000000
00000001 ADLINA    =      %00000001
00000002 ADLEQ     =      %00000010
000000B1 SCALOF    =      177          set instrument scale zer
000000B1                                     o (adj for 10mVrms input
000000B1                                     and 94 dB)
00000140 RAMSTRT   =      $140        ram start address
0000E000 RAMEND     =      $E000       ram end address low word
00000001 RAMENDB   =      1          ram end bank
0000E000 SER NO    ALIAS  "000001"
00000001 CIRRU     =      1
00000001 HD6303Y   =      1
00000001 PARITY    =      1

```

```

;key values
00000011 CAL        =      $11
00000021 LEDENABL   =      $21
00000041 RESETCUM   =      $41
00000081 RELMAX     =      $81
0000012 LEQNO      =      $12
00000022 SHORTLEQ   =      $22
00000042 CUMLEQ     =      $42
00000082 MAXLEQ     =      $82
0000014 EIGHTH     =      $14
00000024 ONESEC     =      $24
00000044 TENSEC    =      $44
00000084 PAUSE     =      $84
00000018 CODE1     =      $18
00000028 CODE2     =      $28
00000048 CODE3     =      $48
00000088 CODE4     =      $88

```

\*\*\*\*\*

0000E000 MEND

0000E000

A.RESET

reset/restart module

A.RESET MODULE  
;module to detect warm/cold start  
;and temporarily to set ports  
RES  
TRAP

0000E000	71E014	AIM	%11100000, RAM	
0000E003			PORT5	
0000E003	724014	OIM	%01000000, RAM	
0000E006			PORT5	
0000E006	7B8014	TIM	%10000000, RAM	if stanby bit is still s
0000E009			PORT5	et batt bak ok
0000E009	2603	BNE	RAMOK	
0000E00B	7EE0C2	JMP	NRAMOK	
0000E00E	716014	RAMOK AIM	%01100000, RAM	
0000E011			PORT5	
0000E011	8600	LDAA	##00000000	
0000E013	9717	STAA	PORT6	
0000E015	860F	LDAA	##00001111	set port 6 for input/out
0000E017				put
0000E017	9716	STAA	PORT6DDR	
0000E019		A.RDKEYBD		

Account Name	Account ID	Account Type	Account Status	Account Balance
Account 1	1000000000	Current	Active	1000.00
Account 2	1000000001	Current	Active	2000.00
Account 3	1000000002	Current	Active	3000.00
Account 4	1000000003	Current	Active	4000.00
Account 5	1000000004	Current	Active	5000.00
Account 6	1000000005	Current	Active	6000.00
Account 7	1000000006	Current	Active	7000.00
Account 8	1000000007	Current	Active	8000.00
Account 9	1000000008	Current	Active	9000.00
Account 10	1000000009	Current	Active	10000.00
Account 11	1000000010	Current	Active	11000.00
Account 12	1000000011	Current	Active	12000.00
Account 13	1000000012	Current	Active	13000.00
Account 14	1000000013	Current	Active	14000.00
Account 15	1000000014	Current	Active	15000.00
Account 16	1000000015	Current	Active	16000.00
Account 17	1000000016	Current	Active	17000.00
Account 18	1000000017	Current	Active	18000.00
Account 19	1000000018	Current	Active	19000.00
Account 20	1000000019	Current	Active	20000.00
Account 21	1000000020	Current	Active	21000.00
Account 22	1000000021	Current	Active	22000.00
Account 23	1000000022	Current	Active	23000.00
Account 24	1000000023	Current	Active	24000.00
Account 25	1000000024	Current	Active	25000.00
Account 26	1000000025	Current	Active	26000.00
Account 27	1000000026	Current	Active	27000.00
Account 28	1000000027	Current	Active	28000.00
Account 29	1000000028	Current	Active	29000.00
Account 30	1000000029	Current	Active	30000.00
Account 31	1000000030	Current	Active	31000.00
Account 32	1000000031	Current	Active	32000.00
Account 33	1000000032	Current	Active	33000.00
Account 34	1000000033	Current	Active	34000.00
Account 35	1000000034	Current	Active	35000.00
Account 36	1000000035	Current	Active	36000.00
Account 37	1000000036	Current	Active	37000.00
Account 38	1000000037	Current	Active	38000.00
Account 39	1000000038	Current	Active	39000.00
Account 40	1000000039	Current	Active	40000.00
Account 41	1000000040	Current	Active	41000.00
Account 42	1000000041	Current	Active	42000.00
Account 43	1000000042	Current	Active	43000.00
Account 44	1000000043	Current	Active	44000.00
Account 45	1000000044	Current	Active	45000.00
Account 46	1000000045	Current	Active	46000.00
Account 47	1000000046	Current	Active	47000.00
Account 48	1000000047	Current	Active	48000.00
Account 49	1000000048	Current	Active	49000.00
Account 50	1000000049	Current	Active	50000.00

```

A.RDKEYBD MODULE
000CE019 LOCAL
*****
;scan keyboard
000CE019 8603          LDAA      #$03          initialise KEYCNT
0000E01B 9742          STAA      KEYCNT
0000E01D 7F0041        CLR       KEYVAL      clear KEYVAL location
0000E020 4F          KEYLOOP  CLRA          clear temp store in acc
0000E021                                A
0000E021 C6F7          LDAB      #$F7          output test bit to row 4
0000E023 D717          STAB      PORT6
0000E025 9617          LDAA      PORT6          read column values
0000E027 43          COMA
0000E028 84F0          ANDA      #%11110000    (mask row data)
0000E02A 2622          BNE      KEYTST        yes, return with values
0000E02C C6FB          LDAB      #$FB          no, output test bit to r
0000E02E                                ow 2 etc....
0000E02E D717          STAB      PORT6
0000E030 9617          LDAA      PORT6
0000E032 43          COMA
0000E033 84F0          ANDA      #%11110000    (mask row data)
0000E035 2617          BNE      KEYTST
0000E037 C6FD          LDAB      #$FD
0000E039 D717          STAB      PORT6
0000E03B 9617          LDAA      PORT6
0000E03D 43          COMA
0000E03E 84F0          ANDA      #%11110000    (mask row data)
0000E040 260C          BNE      KEYTST
0000E042 C6FE          LDAB      #$FE
0000E044 D717          STAB      PORT6
0000E046 9617          LDAA      PORT6
0000E048 43          COMA
0000E049 84F0          ANDA      #%11110000    (mask row data)
0000E04B 2601          BNE      KEYTST
0000E04D 5F          CLR      CLRB
0000E04E 9743          KEYTST  STAA      KEYTEMP    store column data in KEY
0000E050                                TEMP
0000E050 53          COMB
0000E051 DA43          ORAB      KEYTEMP        OR this data into acc B
0000E053 D743          STAB      KEYTEMP        store row and col data i
0000E055                                n KEYTEMP
0000E055 9641          LDAA      KEYVAL        has a key been detected
0000E057                                before?
0000E057 2603          BNE      KEYCOMP        yes, compare with new va
0000E059                                lue
0000E059 D741          STAB      KEYVAL        no, put KEYTEMP in KEYVA
0000E05B                                L
0000E05B 17          TBA          force values to be the s
0000E05C                                ame
0000E05C 10          KEYCOMP  SBA          are values the same?
0000E05D 2705          BEQ      KEYOK          yes, proceed
0000E05F 7F0041        CLR      KEYVAL
0000E062 2005          BRA      KEYRET        don't count this keypres
0000E064                                s
0000E064 7A0042        KEYOK   DEC      KEYCNT    debounce using KEYCNT
0000E067 26B7          BNE      KEYLOOP
0000E069 7F0017        KEYRET  CLR      PORT6      return port6 to initial
0000E06C                                value

```

\*\*\*\*\*

0000E06C

MEND

```

0000E06C 9641          LDAA    KEYVAL
0000E06E 81C1          CMPA    #RESETCUM BOR
0000E070              #RELMAX
0000E070 2750          BEQ    NRAMOK
0000E072 9EDE          LDS    STAKPTR
0000E074 96D9          LDAA    P2BACK          set dec pt and SIO rec'v
0000E076              e line
0000E076 9703          STAA   PORT2
0000E078 86FF          LDAA    #11111111      set port 2 for output
0000E07A 9701          STAA   PORT2DDR
0000E07C 8600          LDAA    #00000000
0000E07E 9717          STAA   PORT6
0000E080 860F          LDAA    #00001111      set port 6 for input/out
0000E082              put
0000E082 9716          STAA   PORT6DDR
0000E084 8602          LDAA    #2            set timer 2 baud rate
0000E086 971C          STAA   TCONR          9600
0000E088          IF    HD6303Y=1
0000E088 8624          LDAA    #00100100
0000E08A 9710          STAA   RMCR
0000E08C 861A          LDAA    #00011010
0000E08E 9711          STAA   TRCSR1
0000E090          IF    PARITY=1
0000E090 8604          LDAA    #00000100
0000E092 971E          STAA   TRCSR2
0000E094          ELSE
0000E094          LDAA    #00000001
0000E094          STAA   TRCSR2
0000E094          ENDIF
0000E094          ELSE
0000E094          LDAA    #01110100
0000E094          STAA   RMCR
0000E094          LDAA    #00011010
0000E094          STAA   TRCSR1
0000E094          ENDIF
0000E094 8610          LDAA    #00010000
0000E096 971B          STAA   TCSR3
0000E098 8604          LDAA    #00000100
0000E09A 9708          STAA   TCSR1
0000E09C 8601          LDAA    #1
0000E09E 9772          STAA   LEDSONF
0000E0A0 7D00C7        TST    CALFLG
0000E0A3 2712          BEQ    OLDCAL
0000E0A5 CCFBEC        LDD    #FFBEC
0000E0A8 DD05          STD    CALOFF
0000E0AA 4F          CLRA
0000E0AB 97DA          STAA   CALDNF
0000E0AD 97C7          STAA   CALFLG
0000E0AF 30          TSX
0000E0B0 C607          LDAB   #7
0000E0B2 3A          ABX
0000E0B3 35          TXS
0000E0B4 7EE1AF        JMP    START
0000E0B7 8684          LDAA    #PAUSE
0000E0B9 9741          STAA   KEYVAL
0000E0BB C00000        LDD    #0000
0000E0BE DD09          STD    FRC
0000E0C0 0E          CLI
0000E0C1 3B          RTI

```

```

0000E0C2 8E013F   NRAMOK   LDS     #013F      set stack pointer
0000E0C5 CE0040           LDX     #040
0000E0C8 4F           CLRA
0000E0C9 A700   RAMCLR   STAA    0,X
0000E0CB 08           INX
0000E0CC 8C0140           CPX     #0140
0000E0CF 26F8           BNE     RAMCLR
0000E0D1 86A8           LDAA   #01010100  set dec pt and SIO rec'v
0000E0D3           LDD    e line
0000E0D3 9703           STAA   PORT2
0000E0D5 86FF           LDAA   #011111111  set port 2 for output
0000E0D7 9701           STAA   PORT2DDR
0000E0D9 8600           LDAA   #00000000
0000E0DB 9717           STAA   PORT6
0000E0DD 860F           LDAA   #00001111  set port 6 for input/out
0000E0DF           LDD    put
0000E0DF 9716           STAA   PORT6DDR
0000E0E1 8602           LDAA   #02        set timer 2 baud rate
0000E0E3 971C           STAA   TCONR      9600
0000E0E5           IF     HD6303Y=1
0000E0E5 8624           LDAA   #00100100
0000E0E7 9710           STAA   RMCR
0000E0E9 861A           LDAA   #00011010
0000E0EB 9711           STAA   TRCSR1
0000E0ED           IF     PARITY=1
0000E0ED 8604           LDAA   #00000100
0000E0EF 971E           STAA   TRCSR2
0000E0F1           ELSE
0000E0F1           LDAA   #00000001
0000E0F1           STAA   TRCSR2

0000E0F1           ENDIF
0000E0F1           ELSE
0000E0F1           LDAA   #01110100
0000E0F1           STAA   RMCR
0000E0F1           LDAA   #00011010
0000E0F1           STAA   TRCSR1

0000E0F1           ENDIF
0000E0F1 8610           LDAA   #00010000
0000E0F3 971B           STAA   TCSR3
0000E0F5 8604           LDAA   #00000100
0000E0F7 9708           STAA   TCSR1
0000E0F9 4F           CLRA
0000E0FA 9747           STAA   ACTYPE
0000E0FC 97C7           STAA   CALFLG
0000E0FE 97DA           STAA   CALDNF
0000E100 4C           INCA
0000E101 976B           STAA   DBLANKF
0000E103 9772           STAA   LEDSONF
0000E105 976F           STAA   LCDLEQUP
0000E107 97BE           STAA   KENCNT
0000E109 9770           STAA   NOTYPE
0000E10B 9746           STAA   TFLAG
0000E10D 976A           STAA   ACMODE
0000E10F 97C6           STAA   TOGLCNT
0000E111 CCE000           LDD    #RAMEND
0000E114 830140           SUBD   #RAMSTRT
0000E117 DDE1           STD    MEMLBIN
0000E119           A.BCDCONV MEMLBIN;MEMLB
0000E119           CD+1

```





A.BCDCONV MACRO BINVAL;BCDVAL  
;macro to convert values stored in parameter BINVAL  
to bcd values in parameter BCDVAL .....bcd digits 4+  
5 are also placed in BCDOVF.....BINVAL & BCDVAL 16-bit  
registers (CCR contents destroyed)

\*\*\*\*\*

```

0000E119 36          PSHA          temp store accumulator A
0000E11A 4F          CLRA
0000E11B 97C3        STAA          BCDOVF
;units
0000E11D 96E2        LDAA          MEMLBIN+1
0000E11F 840F        ANDA          #$0F
0000E121 810A        CMPA          #$0A
0000E123 2502        BCS          LOSTR
0000E125 8B06        ADDA          #$06
0000E127 97E5        LOSTR        STAA          MEMLBIN+1
;multiples of 16
0000E129 D6E2        LDAB          MEMLBIN+1
0000E12B C4F0        ANDB          #$FO
0000E12D 54          LSRB
0000E12E 54          LSRB
0000E12F 54          LSRB
0000E130 CEF15D      LOMIDST      LDX          #BCDTAB1
0000E133 3A          ABX
0000E134 EC00        LDD          0,X
0000E136 36          PSHA
0000E137 17          TBA
0000E138 33          PULB
0000E139 9BE5        ADDA          MEMLBIN+1
0000E13B 19          DAA
0000E13C 97E5        STAA          MEMLBIN+1
0000E13E 36          PSHA
0000E13F 17          TBA
0000E140 33          PULB
0000E141 8900        ADCA          #$00
0000E143 19          DAA
0000E144 97E4        STAA          MEMLBIN+1
;multiples of 256
0000E146 D6E1        LDAB          MEMLBIN
0000E148 C40F        ANDB          #$0F
0000E14A 58          ASLB
0000E14B CEF17D      HIMIDST      LDX          #BCDTAB2
0000E14E 3A          ABX
0000E14F EC00        LDD          0,X
0000E151 36          PSHA
0000E152 17          TBA
0000E153 33          PULB
0000E154 9BE5        ADDA          MEMLBIN+1
0000E156 19          DAA
0000E157 97E5        STAA          MEMLBIN+1
0000E159 36          PSHA
0000E15A 17          TBA
0000E15B 33          PULB
0000E15C 99E4        ADCA          MEMLBIN+1
0000E15E 19          DAA
0000E15F 97E4        STAA          MEMLBIN+1
;multiples of 4096 (4 dig only)

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0000E161 D6E1 LDAB MEMLBIN
0000E163 C4F0 ANDB # $FO
0000E165 54 LSRB
0000E166 54 LSRB
0000E167 54 LSRB
0000E168 CEF19D HIST LDX #BCDTAB3
0000E16B 3A ABX
0000E16C EC00 LDD O,X
0000E16E 36 PSHA
0000E16F 17 TBA
0000E170 33 PULB
0000E171 9BE5 ADDA MEMLB CD+1+1
0000E173 19 DAA
0000E174 97E5 STAA MEMLB CD+1+1
0000E176 36 PSHA
0000E177 17 TBA
0000E178 33 PULB
0000E179 99E4 ADCA MEMLB CD+1
0000E17B 19 DAA
0000E17C 97E4 STAA MEMLB CD+1
0000E17E 96C3 LDAA BCDOVF
0000E180 8900 ADCA # $00
0000E182 97C3 STAA BCDOVF
;other dig of 4096 multiple
0000E184 D6E1 LDAB MEMLBIN
0000E186 C4F0 ANDB # $FO
0000E188 54 LSRB
0000E189 54 LSRB
0000E18A 54 LSRB
0000E18B 54 LSRB
0000E18C CEF1BD LDX #BCDTAB4
0000E18F 3A ABX
0000E190 A600 LDAA O,X
0000E192 9BC3 ADDA BCDOVF
0000E194 19 DAA
0000E195 97C3 STAA BCDOVF
0000E197 32 PULA

```

\*\*\*\*\*

```

0000E198 MEND
0000E198 96C3 LDAA BCDOVF
0000E19A 97E3 STAA MEMLB CD
0000E19C CCFBFC LDD # $FFBC
0000E19F DDD5 STD CALOFF
0000E1A1 8612 LDAA # %0010010
0000E1A3 9759 STAA LEDSRG
0000E1A5 CE0080 LDX #RXBUF
0000E1A8 DFA9 STX RXPTR
0000E1AA CE014G LDX #RAMSTR
0000E1AD DF60 STX RAMPNTR
0000E1AF 8684 START LDAA #PAUSE
0000E1B1 9741 STAA KEYVAL pause
0000E1B3 724003 OIM #01000000, POR
0000E1B6 T2
0000E1B6 71BF03 AIM #10111111, POR
0000E1B9 T2
0000E1B9 CC0000 LDD # $0000
0000E1BC DD09 STD FRC

```

0000E1BE 0E  
0000E1BF

CLI  
MEND

0000E1BF

A.MAIN

A.MAIN MODULE

;main module

\*\*\*\*\*

MLOOP

0000E1BF 1A		SLP	
0000E1C0 7D00C0		TST	MONFLG
0000E1C3 2706		BEQ	NMON
0000E1C5 7F00C0		CLR	MONFLG
0000E1C8 7EF90A		JMP	MONITA
	NMON		
0000E1CB 7A00BE		DEC	KENCNT
0000E1CE 2608		BNE	NKEYEN
0000E1D0 8610		LDAA	#\$10
0000E1D2 97BE		STAA	KENCNT
0000E1D4 4F		CLRA	
0000E1D5 4C		INCA	
0000E1D6 97C5		STAA	KENFLG
	NKEYEN		
0000E1D8 9641		LDAA	KEYVAL
0000E1DA 2703		BEQ	TRYREAD
0000E1DC 7EE315		JMP	INTRPRT
0000E1DF 7DC072	TRYREAD	TST	LEDSONF
0000E1E2 2603		BNE	ROW3OK
0000E1E4 720417		OIM	%00000100, POR
0000E1E7			T6
0000E1E7 9615	ROW3OK	LDAA	PORT5
0000E1E9 8401		ANDA	##%00000001
0000E1EB 2653		BNE	NOKEY
0000E1ED		A.RDKEYBD	

poll keyboard  
if no key...  
...go back to sleep

Category	2010-2011	2009-2010	2008-2009	2007-2008
Total	1,234,567	1,123,456	1,012,345	901,234
Academic Affairs	456,789	432,109	408,765	385,432
Student Services	234,567	221,098	208,765	195,432
Administrative Services	189,012	176,543	164,321	152,109
Faculty & Staff	123,456	112,345	101,234	90,123
Capital Construction	98,765	87,654	76,543	65,432
Financial Services	76,543	65,432	54,321	43,210
Information Technology	65,432	54,321	43,210	32,109
Legal & Compliance	54,321	43,210	32,109	21,098
Physical Plant	43,210	32,109	21,098	10,987
Public Affairs	32,109	21,098	10,987	0,876
Research & Innovation	21,098	10,987	0,876	-0,765
Special Programs	10,987	0,876	-0,765	-1,654
Unallocated	0,876	-0,765	-1,654	-2,543

```

A.RDKEYBD MODULE
LOCAL
*****
;scan keyboard
0000E1ED 8603          LDAA      #$03          initialise KEYCNT
0000E1EF 9742          STAA      KEYCNT
0000E1F1 7F0041         CLR       KEYVAL       clear KEYVAL location
0000E1F4 4F          KEYLOOP   CLRA        clear temp store in acc
0000E1F5                                A
0000E1F5 C6F7          LDAB      #$F7          output test bit to row 4
0000E1F7 D717          STAB      PORT6
0000E1F9 9617          LDAA      PORT6        read column values
0000E1FB 43          COMA
0000E1FC 84F0          ANDA      #%11110000   (mask row data)
0000E1FE 2622          BNE      KEYTST       yes, return with values
0000E200 C6FB          LDAB      #$FB        no, output test bit to r
0000E202                                ow 2 etc....
0000E202 D717          STAB      PORT6
0000E204 9617          LDAA      PORT6
0000E206 43          COMA
0000E207 84F0          ANDA      #%11110000   (mask row data)
0000E209 2617          BNE      KEYTST
0000E20B C6FD          LDAB      #$FD
0000E20D D717          STAB      PORT6
0000E20F 9617          LDAA      PORT6
0000E211 43          COMA
0000E212 84F0          ANDA      #%11110000   (mask row data)
0000E214 260C          BNE      KEYTST
0000E216 C6FE          LDAB      #$FE
0000E218 D717          STAB      PORT6
0000E21A 9617          LDAA      PORT6
0000E21C 43          COMA
0000E21D 84F0          ANDA      #%11110000   (mask row data)
0000E21F 2601          BNE      KEYTST
0000E221 5F          CLR      CLRB
0000E222 9743          KEYTST   STAA      KEYTEMP   store column data in KEY
0000E224                                TEMP
0000E224 53          COMB
0000E225 DA43          ORAB      KEYTEMP      OR this data into acc B
0000E227 D743          STAB      KEYTEMP      store row and col data i
0000E229                                n KEYTEMP
0000E229 9641          LDAA      KEYVAL       has a key been detected
0000E22B                                before?
0000E22B 2603          BNE      KEYCOMP      yes, compare with new va
0000E22D                                lue
0000E22D D741          STAB      KEYVAL       no, put KEYTEMP in KEYVA
0000E22F                                L
0000E22F 17          TBA        force values to be the s
0000E230                                ame
0000E230 10          KEYCOMP   SBA        are values the same?
0000E231 2705          BEQ      KEYOK        yes, proceed
0000E233 7F0041         CLR      KEYVAL
0000E236 2005          BRA      KEYRET       don't count this keypres
0000E238                                s
0000E238 7A0042         KEYOK   DEC      KEYCNT   debounce using KEYCNT
0000E23B 26B7          BNE      KEYLOOP
0000E23D 7F0017         KEYRET   CLR      PORT6   return port6 to initial
0000E240                                value

```



\*\*\*\*\*

0000E240

MEND

NOKEY

0000E240	7D00C7		TST	CALFLG
0000E243	2603		BNE	CALPH
0000E245	7EE30E		JMP	NCALMOD
0000E248	7B0146	CALPH	TIM	\$1,TFLAG
0000E24B	2606		BNE	CALMOD
0000E24D	7F0041		CLR	KEYVAL
0000E250	7EE30E		JMP	NCALMOD
0000E253		CALMOD	A.CALMOD	

Particulars	Dr	Cr
Goodwill	120,000	
Identifiable Intangible Assets	200,000	
Trade Debtors	100,000	
Trade Creditors		100,000
Share Capital		200,000
Reserves		120,000
Net Assets	420,000	420,000

A.CALMOD	MODULE	
0000E253 9641	LDAA	KEYVAL
0000E255 81F8	CMPA	#\$F8
0000E257 2617	BNE	NCALCLR
0000E259 4F	CLRA	
0000E25A 97C7	STAA	CALFLG
0000E25C 97DA	STAA	CALDNF
0000E25E CCFFBC	LDD	\$\$FFBC
0000E261 DDD5	STD	CALOFF
0000E263 71BFD7	AIM	%10111111,ERR
0000E266		STAT
0000E266 71F259	AIM	%11110010,LED
0000E269		SREG
0000E269 8622	LDAA	#SHORTLEQ
0000E26B 9741	STAA	KEYVAL
0000E26D 7EE30E	JMP	CALEND
	NCALCLR	
0000E270 8114	CMPA	#EIGHTH
0000E272 2607	BNE	N94DB
0000E274 CC03AC	LDD	#\$03AC
0000E277 DDDC	STD	CALVAL
0000E279 205D	BRA	TSTOFF
0000E27B 8124	N94DB CMPA	#ONESEC
0000E27D 2607	BNE	N104DB
0000E27F CC0410	LDD	#\$0410
0000E282 DDDC	STD	CALVAL
0000E284 2052	BRA	TSTOFF
0000E286 8144	N104DB CMPA	#TENSEC
0000E288 2607	BNE	N117DB
0000E28A CC0492	LDD	#\$0492
0000E28D DDDC	STD	CALVAL
0000E28F 2047	BRA	TSTOFF
0000E291 8184	N117DB CMPA	#PAUSE
0000E293 2605	BNE	N124DB
0000E295 CC04D8	LDD	#\$04D8
0000E298 DDDC	STD	CALVAL
0000E29A D6E0	N124DB LDAB	CALCNT
0000E29C 5C	INCB	
0000E29D D7E0	STAB	CALCNT
0000E29F C108	CMPB	#8
0000E2A1 2635	BNE	TSTOFF
0000E2A3 5F	CLRB	
0000E2A4 D7E0	STAB	CALCNT
0000E2A6 8118	CMPA	#CODE1
0000E2A8 2609	BNE	NUP1DB
0000E2AA DCDC	LDD	CALVAL
0000E2AC C3000A	ADDD	#10
0000E2AF DDDC	STD	CALVAL
0000E2B1 2025	BRA	TSTOFF
0000E2B3 8128	NUP1DB CMPA	#CODE2
0000E2B5 260B	BNE	NDN1DB
0000E2B7 DCDC	LDD	CALVAL
0000E2B9 271D	BEQ	TSTOFF
0000E2BB 83000A	SUBD	#10
0000E2BE DDDC	STD	CALVAL
0000E2C0 2016	BRA	TSTOFF
0000E2C2 8148	NDN1DB CMPA	#CODE3
0000E2C4 2607	BNE	NUPPT1DB
0000E2C6 DEDC	LDX	CALVAL

No.	Date	Particulars	Amount
1000	1950	...	...
1001	1950	...	...
1002	1950	...	...
1003	1950	...	...
1004	1950	...	...
1005	1950	...	...
1006	1950	...	...
1007	1950	...	...
1008	1950	...	...
1009	1950	...	...
1010	1950	...	...
1011	1950	...	...
1012	1950	...	...
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1015	1950	...	...
1016	1950	...	...
1017	1950	...	...
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1020	1950	...	...
1021	1950	...	...
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1098	1950	...	...
1099	1950	...	...
1100	1950	...	...

0000E2C8 08		INX	
0000E2C9 DFDC		STX	CALVAL
0000E2CB 200B		BRA	TSTOFF
0000E2CD 8188	NUPPT1 DB	CMPA	#CODE4
0000E2CF 2607		BNE	TSTOFF
0000E2D1 DEDC		LDX	CALVAL
0000E2D3 2703		BEQ	TSTOFF
0000E2D5 09		DEX	
0000E2D6 DFDC		STX	CALVAL
0000E2D8 DED5	TSTOFF	LDX	CALOFF
0000E2DA 8C007F		CPX	#\$007F
0000E2DD 230E		BLS	CALOK
0000E2DF 8CFF80		CPX	#\$FF80
0000E2E2 2209		BHI	CALOK
0000E2E4 8601		LDAA	#\$01
0000E2E6 9755		STAA	ERRFLAG
0000E2E8 7240D7		OIM	%01000000,ERR
0000E2EB			STAT
0000E2EB 2016		BRA	DOCAL
	CALOK		
0000E2ED 71BFD7		AIM	%10111111,ERR
0000E2F0			STAT
0000E2F0 81C1		CMPA	#RESETCUM BOR
0000E2F2			#RELMAX
0000E2F2 260F		BNE	DOCAL
0000E2F4 4F		CLRA	
0000E2F5 97C7		STAA	CALFLG
0000E2F7 4C		INCA	
0000E2F8 97DA		STAA	CALDNF
0000E2FA 71F259		AIM	%11110010,LED
0000E2FD			SREG
0000E2FD 8622		LDAA	#SHORTLEQ
0000E2FF 9741		STAA	KEYVAL
0000E301 200B		BRA	CALEND
	DOCAL		
0000E303 DC50		LDD	DATA
0000E305 D3D5		ADDD	CALOFF
0000E307 93DC		SUBD	CALVAL
0000E309 DDD5		STD	CALOFF
0000E30B 7F0041		CLR	KEYVAL
	CALEND		
0000E30E		MEND	

	NCALMOD		
0000E30E 9641		LDAA	KEYVAL
0000E310 2603		BNE	INTRPRT
0000E312 7EE6CD		JMP	NINTRPRT
0000E315	INTRPRT	A.KEYINT	

Exhibit 1

Exhibit 2

Account Name	Account Number	Balance	Account Name	Account Number	Balance
AAA	123456789	100.00	AAA	123456789	100.00
AAA	123456789	200.00	AAA	123456789	200.00
AAA	123456789	300.00	AAA	123456789	300.00
AAA	123456789	400.00	AAA	123456789	400.00
AAA	123456789	500.00	AAA	123456789	500.00
AAA	123456789	600.00	AAA	123456789	600.00
AAA	123456789	700.00	AAA	123456789	700.00
AAA	123456789	800.00	AAA	123456789	800.00
AAA	123456789	900.00	AAA	123456789	900.00
AAA	123456789	1000.00	AAA	123456789	1000.00
AAA	123456789	1100.00	AAA	123456789	1100.00
AAA	123456789	1200.00	AAA	123456789	1200.00
AAA	123456789	1300.00	AAA	123456789	1300.00
AAA	123456789	1400.00	AAA	123456789	1400.00
AAA	123456789	1500.00	AAA	123456789	1500.00
AAA	123456789	1600.00	AAA	123456789	1600.00
AAA	123456789	1700.00	AAA	123456789	1700.00
AAA	123456789	1800.00	AAA	123456789	1800.00
AAA	123456789	1900.00	AAA	123456789	1900.00
AAA	123456789	2000.00	AAA	123456789	2000.00
AAA	123456789	2100.00	AAA	123456789	2100.00
AAA	123456789	2200.00	AAA	123456789	2200.00
AAA	123456789	2300.00	AAA	123456789	2300.00
AAA	123456789	2400.00	AAA	123456789	2400.00
AAA	123456789	2500.00	AAA	123456789	2500.00
AAA	123456789	2600.00	AAA	123456789	2600.00
AAA	123456789	2700.00	AAA	123456789	2700.00
AAA	123456789	2800.00	AAA	123456789	2800.00
AAA	123456789	2900.00	AAA	123456789	2900.00
AAA	123456789	3000.00	AAA	123456789	3000.00



A.KEYINT	MODULE		
0000E315 8121	CMPA	#LEDENABL	LEDENABLE
0000E317 2612	BNE	NLEDKEY	
0000E319 7D00C5	TST	KENFLG	
0000E31C 270D	BEQ	NLEDKEY	
0000E31E 4F	CLRA		
0000E31F 97C5	STAA	KENFLG	
0000E321 8610	LDA	#\$10	
0000E323 97BE	STAA	KENCNT	
0000E325 750172	EIM	\$01, LEDSONF	
0000E328 7EE6C7	JMP	NSTRT	
0000E32B 8122	NLEDKEY CMPA	#SHORTLEQ	
0000E32D 2618	BNE	NSHRTLEQ	
0000E32F 4F	CLRA		
0000E330 976D	STAA	LCDMAXUP	
0000E332 976E	STAA	LDCUMUP	
0000E334 9771	STAA	LCDNOUP	
0000E336 9770	STAA	NOTYPE	
0000E338 4C	INCA		
0000E339 976F	STAA	LCDLEQUP	
0000E33B 728003	OIM	%10000000, POR	
0000E33E		T2	
0000E33E 71F059	AIM	%11110000, LED	
0000E341		SREG	
0000E341 720259	OIM	%0000010, LED	
0000E344		SREG	
0000E344 7EE6C7	JMP	NSTRT	
	NSHRTLEQ		
0000E347 8182	CMPA	#MAXLEQ	
0000E349 2618	BNE	NMAXLEQ	
0000E34B 4F	CLRA		
0000E34C 976F	STAA	LCDLEQUP	
0000E34E 976E	STAA	LDCUMUP	
0000E350 9771	STAA	LCDNOUP	
0000E352 9770	STAA	NOTYPE	
0000E354 4C	INCA		
0000E355 976D	STAA	LCDMAXUP	
0000E357 728003	OIM	%10000000, POR set dec pt	
0000E35A		T2	
0000E35A 71F059	AIM	%11110000, LED	
0000E35D		SREG	
0000E35D 720859	OIM	%00001000, LED	
0000E360		SREG	
0000E360 7EE6C7	JMP	NSTRT	
	NMAXLEQ		
0000E363 8142	CMPA	#CUMLEQ	
0000E365 2618	BNE	NCUMLEQ	
0000E367 4F	CLRA		
0000E368 976D	STAA	LCDMAXUP	
0000E36A 976F	STAA	LCDLEQUP	
0000E36C 9771	STAA	LCDNOUP	
0000E36E 9770	STAA	NOTYPE	
0000E370 4C	INCA		
0000E371 976E	STAA	LDCUMUP	
0000E373 728003	OIM	%10000000, POR set dec pt	
0000E376		T2	
0000E376 71F059	AIM	%11110000, LED	
0000E379		SREG	
0000E379 720459	OIM	%00000100, LED	

100-100000-100000

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100-100000-100000

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100-100000-100000

0000E37C			SREG
0000E37C 7EE6C7		JMP	NSTRT
	NCUMLEQ		
0000E37F 8112		CMPA	#LEQNO
0000E381 2626		BNE	NLEQNO
0000E383 7D00C5		TST	KENFLG
0000E386 2721		BEQ	NLEQNO
0000E388 4F		CLRA	
0000E389 97C5		STAA	KENFLG
0000E38B 976D		STAA	LCDMAXUP
0000E38D 976E		STAA	LCD CUMUP
0000E38F 976F		STAA	LCDLEQUP
0000E391 4C		INCA	
0000E392 9771		STAA	LCDNOUP
0000E394 8610		LDAA	#\$10
0000E396 97BE		STAA	KENCNT
0000E398 717F03		AIM	%01111111,POR set three dots
0000E39B			T2
0000E39B 9670		LDAA	NOTYPE
0000E39D 8401		ANDA	#!00000001
0000E39F 8801		EORA	#!00000001
0000E3A1 9770		STAA	NOTYPE
0000E3A3 717F059		AIM	%11110000,LED
0000E3A6			SREG
0000E3A6 7EE6C7		JMP	NSTRT
0000E3A9 7D006A	NLEQNO	TST	ACMODE
0000E3AC 2603		BNE	RUNKEYS
0000E3AE 7EE5C3		JMP	NRUNKEYS
0000E3B1 8184	RUNKEYS	CMPA	#PAUSE
0000E3B3 2703		BEQ	DOPAUSE
0000E3B5 7EE58F		JMP	NPAUSE
0000E3B8	DOPAUSE	A. PAUSE	

项目	2019年12月31日	2019年12月31日	2019年12月31日
流动资产	1,234,567	1,234,567	1,234,567
货币资金	100,000	100,000	100,000
应收账款	200,000	200,000	200,000
预付款项	50,000	50,000	50,000
其他流动资产	834,567	834,567	834,567
非流动资产	3,456,789	3,456,789	3,456,789
固定资产	2,000,000	2,000,000	2,000,000
无形资产	500,000	500,000	500,000
其他非流动资产	956,789	956,789	956,789
负债	2,345,678	2,345,678	2,345,678
短期借款	1,000,000	1,000,000	1,000,000
应付账款	500,000	500,000	500,000
其他负债	845,678	845,678	845,678
所有者权益	3,456,789	3,456,789	3,456,789
实收资本	1,000,000	1,000,000	1,000,000
留存收益	2,456,789	2,456,789	2,456,789

	A.PAUSE	MODULE	
0000E3B8 7F006A		CLR	ACMODE
		;was the 2.36 running?	
0000E3BB 9647		LDAA	ACTYPE
0000E3BD 2713		BEQ	CONVCMP
		;was there 1 complete conversion?	
0000E3BF DC60		LDD	RAMPNTR
0000E3C1			prevents endless empty h
0000E3C1 830010		SUBD	eaders if
0000E3C4			a conversion is interrup
0000E3C4 18		XGDX	ted before
0000E3C5 9C4A		CPX	the first data is stored
0000E3C7 2609		BNE	CHDSTR+1
0000E3C9 9662		LDAA	CONVCMP
0000E3CB 9149		CMPA	RAMPNTB
0000E3CD 2603		BNE	CHDSTR
0000E3CF 7EE578		JMP	CONVCMP
			NLASTEND
	CONVCMP		
	;build new header		
0000E3D2 7F006C		CLR	HDRFLD
0000E3D5 7F0056		CLR	HDWCTR
0000E3D8 CEF1CD		LDX	#HLOOK
0000E3DB DF57		STX	HLPTR
0000E3DD 9603		LDAA	PORT2
0000E3DF 8402		ANDA	;%00000010
0000E3E1 44		LSRA	
0000E3E2 9762		STAA	RAMPNTB
0000E3E4 DE60		LDX	RAMPNTR
0000E3E6 DF63		STX	RAMPSTR
0000E3E8 9662		LDAA	RAMPNTB
0000E3EA 9765		STAA	RAMPBSTR
0000E3EC 7D0073	NXEMPTY	TST	RAMFULL
0000E3EF 2706		BEQ	NFULL1
0000E3F1 8601		LDAA	#\$01
0000E3F3 976C		STAA	HDRFLD
0000E3F5 204E		BRA	DOLAST
0000E3F7 DE60	NFULL1	LDX	RAMPNTR
0000E3F9 8CE000		CPX	#RAMEND
0000E3FC 2625		BNE	DOWRT
0000E3FE 7D0062		TST	RAMPNTB
0000E401 2708		BEQ	OTHRPG
0000E403 8601		LDAA	#\$01
0000E405 976C		STAA	HDRFLD
0000E407 9773		STAA	RAMFULL
0000E409 203A		BRA	DOLAST
0000E40B 8601	OTHRPG	LDAA	#RAMENDB
0000E40D 2608		BNE	TOGL1
0000E40F 8601		LDAA	#\$01
0000E411 976C		STAA	HDRFLD
0000E413 9773		STAA	RAMFULL
0000E415 202E		BRA	DOLAST
0000E417 8601	TOGL1	LDAA	#\$01
0000E419 9762		STAA	RAMPNTB
0000E41B 720203		OIM	%00000010,POR
0000E41E			T2
0000E41E CE0140		LDX	#RAMSTR
0000E421 DF60		STX	RAMPNTR
0000E423 9656	DOWRT	LDAA	HDWCTR
0000E425 4C		INCA	

NAME	RESIDENCE	DATE	AMOUNT
ALBANY	ALBANY	1890	100.00
ALBANY	ALBANY	1891	100.00
ALBANY	ALBANY	1892	100.00
ALBANY	ALBANY	1893	100.00
ALBANY	ALBANY	1894	100.00
ALBANY	ALBANY	1895	100.00
ALBANY	ALBANY	1896	100.00
ALBANY	ALBANY	1897	100.00
ALBANY	ALBANY	1898	100.00
ALBANY	ALBANY	1899	100.00
ALBANY	ALBANY	1900	100.00
ALBANY	ALBANY	1901	100.00
ALBANY	ALBANY	1902	100.00
ALBANY	ALBANY	1903	100.00
ALBANY	ALBANY	1904	100.00
ALBANY	ALBANY	1905	100.00
ALBANY	ALBANY	1906	100.00
ALBANY	ALBANY	1907	100.00
ALBANY	ALBANY	1908	100.00
ALBANY	ALBANY	1909	100.00
ALBANY	ALBANY	1910	100.00
ALBANY	ALBANY	1911	100.00
ALBANY	ALBANY	1912	100.00
ALBANY	ALBANY	1913	100.00
ALBANY	ALBANY	1914	100.00
ALBANY	ALBANY	1915	100.00
ALBANY	ALBANY	1916	100.00
ALBANY	ALBANY	1917	100.00
ALBANY	ALBANY	1918	100.00
ALBANY	ALBANY	1919	100.00
ALBANY	ALBANY	1920	100.00
ALBANY	ALBANY	1921	100.00
ALBANY	ALBANY	1922	100.00
ALBANY	ALBANY	1923	100.00
ALBANY	ALBANY	1924	100.00
ALBANY	ALBANY	1925	100.00
ALBANY	ALBANY	1926	100.00
ALBANY	ALBANY	1927	100.00
ALBANY	ALBANY	1928	100.00
ALBANY	ALBANY	1929	100.00
ALBANY	ALBANY	1930	100.00
ALBANY	ALBANY	1931	100.00
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ALBANY	ALBANY	1933	100.00
ALBANY	ALBANY	1934	100.00
ALBANY	ALBANY	1935	100.00
ALBANY	ALBANY	1936	100.00
ALBANY	ALBANY	1937	100.00
ALBANY	ALBANY	1938	100.00
ALBANY	ALBANY	1939	100.00
ALBANY	ALBANY	1940	100.00
ALBANY	ALBANY	1941	100.00
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ALBANY	ALBANY	1946	100.00
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ALBANY	ALBANY	1952	100.00
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ALBANY	ALBANY	1954	100.00
ALBANY	ALBANY	1955	100.00
ALBANY	ALBANY	1956	100.00
ALBANY	ALBANY	1957	100.00
ALBANY	ALBANY	1958	100.00
ALBANY	ALBANY	1959	100.00
ALBANY	ALBANY	1960	100.00
ALBANY	ALBANY	1961	100.00
ALBANY	ALBANY	1962	100.00
ALBANY	ALBANY	1963	100.00
ALBANY	ALBANY	1964	100.00
ALBANY	ALBANY	1965	100.00
ALBANY	ALBANY	1966	100.00
ALBANY	ALBANY	1967	100.00
ALBANY	ALBANY	1968	100.00
ALBANY	ALBANY	1969	100.00
ALBANY	ALBANY	1970	100.00
ALBANY	ALBANY	1971	100.00
ALBANY	ALBANY	1972	100.00
ALBANY	ALBANY	1973	100.00
ALBANY	ALBANY	1974	100.00
ALBANY	ALBANY	1975	100.00
ALBANY	ALBANY	1976	100.00
ALBANY	ALBANY	1977	100.00
ALBANY	ALBANY	1978	100.00
ALBANY	ALBANY	1979	100.00
ALBANY	ALBANY	1980	100.00
ALBANY	ALBANY	1981	100.00
ALBANY	ALBANY	1982	100.00
ALBANY	ALBANY	1983	100.00
ALBANY	ALBANY	1984	100.00
ALBANY	ALBANY	1985	100.00
ALBANY	ALBANY	1986	100.00
ALBANY	ALBANY	1987	100.00
ALBANY	ALBANY	1988	100.00
ALBANY	ALBANY	1989	100.00
ALBANY	ALBANY	1990	100.00
ALBANY	ALBANY	1991	100.00
ALBANY	ALBANY	1992	100.00
ALBANY	ALBANY	1993	100.00
ALBANY	ALBANY	1994	100.00
ALBANY	ALBANY	1995	100.00
ALBANY	ALBANY	1996	100.00
ALBANY	ALBANY	1997	100.00
ALBANY	ALBANY	1998	100.00
ALBANY	ALBANY	1999	100.00
ALBANY	ALBANY	2000	100.00

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0000E426 9756          STAA      HDWCTR
0000E428 8111          CMPA      # $11
0000E42A 2719          BEQ      DOLAST
0000E42C DE57          LDX      HLPTR
0000E42E 71FE03         AIM      %11111110,POR
0000E431                T2
0000E431 EC00          LDD      0,X
0000E433 08            INX
0000E434 08            INX
0000E435 DF57          STX      HLPTR
0000E437 DE60          LDX      RAMPNTR
0000E439 E700          STAB     0,X
0000E43B 720103        OIM      %00000001,POR
0000E43E                T2
0000E43E A700          STAA     0,X
0000E440 08            INX
0000E441 DF60          STX      RAMPNTR
0000E443 20A7          BRA      NXEMPTY

DOLAST
;finish last header if there was one
0000E445 DE60          LDX      RAMPNTR
0000E447 8C0150         CPX      #RAMSTR+16
0000E44A 260F          BNE      DOLAST1
0000E44C 9662          LDAA     RAMPNTB
0000E44E 260B          BNE      DOLAST1
0000E450 CE0140        LDX      #RAMSTR
0000E453 DF4A          STX      CHDSTR+1
0000E455 4F            CLRA
0000E456 9749          STAA     CHDSTR
0000E458 7EE578         JMP      NLASTEND
0000E45B 9649          LDAA     CHDSTR
0000E45D 2605          BNE      CHDB1
0000E45F 71FD03         AIM      %11111101,POR
0000E462                T2
0000E462 2003          BRA      CHDBDN
0000E464 720203        CHDB1    OIM      %00000010,POR
0000E467                T2

CHDBDN
0000E467 DE4A          LDX      CHDSTR+1
0000E469 08            INX
0000E46A 8CE000         CPX      # $E000
0000E46D 2606          BNE      NHDOVF1
0000E46F CE0140        LDX      #RAMSTR
0000E472 720203        OIM      %00000010,POR
0000E475                T2

NHDOVF1
0000E475 DC53          LDD      DATAcnt+1
0000E477 71FE03         AIM      %11111110,POR
0000E47A                T2
0000E47A E700          STAB     #0,X          no of data samples
0000E47C 720103        OIM      %00000001,POR
0000E47F                T2
0000E47F A700          STAA     #0,X
0000E481 9652          LDAA     DATAcnt
0000E483 71FE03         AIM      %11111110,POR
0000E486                T2
0000E486 08            INX
0000E487 8CE000         CPX      # $E000
0000E48A 2606          BNE      NHDOVF2

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0000E48C	CE0140		LDX	#RAMSTRT	
0000E48F	720203		OIM	%00000010, POR	
0000E492				T2	
		NHDOVF2			
0000E492	A700		STAA	0,X	no of data samples hi wo
0000E494					rd
0000E494	08		INX		
0000E495	08		INX		
0000E496	08		INX		
0000E497	08		INX		
0000E498	8CE000		CPX	#\$E000	
0000E49B	250B		BCS	NHDOVF3	
0000E49D	18		XGDY		
0000E49E	83E000		SUBD	#\$E000	
0000E4A1	CE0140		LDX	#RAMSTRT	
0000E4A4	3A		ABX		
0000E4A5	720203		OIM	%00000010, POR	
0000E4A8				T2	
0000E4A8	5F	NHDOVF3	CLRB		
0000E4A9	9649		LDAA	CHDSTRT	
0000E4AB	9865		EORA	RAMPBSTR	
0000E4AD	2706		BEQ	NPCHNG	
0000E4AF	CC2000		LDD	#\$2000	fudge....offset to start
0000E4B2					of next
0000E4B2	C30140		ADDD	#RAMSTRT	
0000E4B5	C30010	NPCHNG	ADDD	#\$10	allows for prog gap but
0000E4B8	D353		ADDD	DATAcnt+1	extended headers
0000E4BA	DD53		STD	DATAcnt+1	not catered for
0000E4BC	9652		LDAA	DATAcnt	
0000E4BE	8900		ADCA	#0	
0000E4C0	9752		STAA	DATAcnt	
0000E4C2	7D006C		TST	HDRFLD	
0000E4C5	2707		BEQ	NNULL	
0000E4C7	4F		CLRA		
0000E4C8	9752		STAA	DATAcnt	
0000E4CA	9753		STAA	DATAcnt+1	
0000E4CC	9754		STAA	DATAcnt+2	
0000E4CE	DC53	NNULL	LDD	DATAcnt+1	
0000E4D0	71FE03		AIM	%11111110, POR	
0000E4D3				T2	
0000E4D3	E700		STAB	0,X	
0000E4D5	720103		OIM	%00000001, POR	
0000E4D8				T2	
0000E4D8	A700		STAA	0,X	
0000E4DA	9652		LDAA	DATAcnt	
0000E4DC	71FE03		AIM	%11111110, POR	
0000E4DF				T2	
0000E4DF	08		INX		
0000E4E0	8CE000		CPX	#\$E000	
0000E4E3	2606		BNE	NHDOVF4	
0000E4E5	CE0140		LDX	#RAMSTRT	
0000E4E8	720203		OIM	%00000010, POR	
0000E4EB				T2	
		NHDOVF4			
0000E4EB	A700		STAA	0,X	
0000E4ED	08		INX		
0000E4EE	08		INX		
0000E4EF	08		INX		



Section	Acres	Remarks
1	1.00	...
2	1.00	...
3	1.00	...
4	1.00	...
5	1.00	...
6	1.00	...
7	1.00	...
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14	1.00	...
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36	1.00	...
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41	1.00	...
42	1.00	...
43	1.00	...
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62	1.00	...
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69	1.00	...
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74	1.00	...
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89	1.00	...
90	1.00	...
91	1.00	...
92	1.00	...
93	1.00	...
94	1.00	...
95	1.00	...
96	1.00	...
97	1.00	...
98	1.00	...
99	1.00	...
100	1.00	...

0000E4F0	08		INX	
0000E4F1	8CE000		CPX	#\$E000
0000E4F4	250B		BCS	NHDOVF5
0000E4F6	18		XGDY	
0000E4F7	83E000		SUBD	#\$E000
0000E4FA	CE0140		LDX	#RAMSTRT
0000E4FD	3A		ABX	
0000E4FE	720203		OIM	%00000010,POR
0000E501				T2
0000E501	720103	NHDOVF5	OIM	%00000001,POR
0000E504				T2
0000E504	96DB		LDAA	LINASTR
0000E506	A700		STAA	0,X
0000E508	08		INX	
0000E509	8CE000		CPX	#\$E000
0000E50C	2506		BCS	NHDOVF6
0000E50E	CE0140		LDX	#RAMSTRT
0000E511	720203		OIM	%00000010,POR
0000E514				T2
0000E514	08	NHDCVF6	INX	
0000E515	8CE000		CPX	#\$E000
0000E518	2606		BNE	NHDOVF7
0000E51A	CE0140		LDX	#RAMSTRT
0000E51D	720203		OIM	%00000010,POR
0000E520				T2
0000E520	71FE03	NHDOVF7	AIM	%11111110,POR
0000E523				T2
0000E523	96C4		LDAA	CODUSE
0000E525	44		LSRA	
0000E526	44		LSRA	
0000E527	44		LSRA	
0000E528	A700		STAA	0,X
0000E52A	720103		OIM	%00000001,POR
0000E52D				T2
0000E52D	9647		LDAA	ACTYPE
0000E52F	8101		CMPA	#1
0000E531	2606		BNE	N18
0000E533	8602		LDAA	#2
0000E535	A700		STAA	0,X
0000E537	200E		BRA	DCALWRT
0000E539	8108	N18	CMPA	#8
0000E53B	2606		BNE	N1
0000E53D	8603		LDAA	#3
0000E53F	A700		STAA	0,X
0000E541	2004		BRA	DCALWRT
0000E543	8605	N1	LDAA	#5
0000E545	A700		STAA	0,X
		DCALWRT		
0000E547	08		INX	
0000E548	8CE000		CPX	#\$E000
0000E54B	2606		BNE	NHDOVF8
0000E54D	CE0140		LDX	#RAMSTRT
0000E550	720203		OIM	%00000010,POR
0000E553				T2
0000E553	71FE03	NHDOVF8	AIM	%11111110,POR
0000E556				T2
0000E556	96D6		LDAA	CALOFF+1
0000E558	A700		STAA	0,X
0000E55A	720103		OIM	%00000001,POR

0000E55D			T2
0000E55D 96DA		LDAA	CALDNF
0000E55F A700		STAA	O,X
0000E561 71FE03	NEWDST	AIM	%11111110,POR
0000E564			T2
0000E564 DC63		LDD	RAMPSTR
0000E566 DD4A		STD	CHDSTR+1
0000E568 9665		LDAA	RAMPBSTR
0000E56A 9749		STAA	CHDSTR
0000E56C 9662		LDAA	RAMPNTB
0000E56E 2705		BEQ	SETP2
0000E570 720203		OIM	%00000010,POR
0000E573			T2
0000E573 2003		BRA	NLASTEND
0000E575 71FD03	SETP2	AIM	%11111101,POR
0000E578			T2

;EXTENDED HEADERS NOT ACCOMMODATED

NLASTEND

0000E578 710F59		AIM	%00001111,LED
0000E57B			SREG
0000E57B 721059		OIM	%00010000,LED
0000E57E			SREG
0000E57E 728003		OIM	%10000000,POR
0000E581			T2
0000E581 4F		CLRA	
0000E582 97DA		STAA	CALDNF
0000E584 9752		STAA	DATAcnt
0000E586 9753		STAA	DATAcnt+1
0000E588 9754		STAA	DATAcnt+2
0000E58A 97C4		STAA	CODUSE
0000E58C		MEND	

Account	2023	2022
Balance b/f	1000	1000
Revenue	1000	1000
Cost of sales	(500)	(500)
Profit	500	500
Dividends	(200)	(200)
Retained profit	300	300
Balance c/f	1300	1300

```

0000E58C 7EE6C7      JMP      NSTRT
                    NPAUSE
0000E58F 8141      CMPA    #RESETCUM
0000E591 2614      BNE     NRSTCUM
0000E593 4F        CLRA
0000E594 974C      STAA   CUMBIN
0000E596 974D      STAA   CUMBIN+1
0000E598 97CC      STAA   CUMDOSE
0000E59A 97CD      STAA   CUMDOSE+1
0000E59C 97CE      STAA   CUMDOSE+2
0000E59E 97CF      STAA   CUMTIME
0000E5A0 97D0      STAA   CUMTIME+1
0000E5A2 97D1      STAA   CUMTIME+2
0000E5A4 7EE6C7      JMP      NSTRT
0000E5A7 8181      NRSTCUM CMPA    #RELMAX
0000E5A9 2609      BNE     NRELMAX
0000E5AB 7F005A    CLR     MAXBIN
0000E5AE 7F005B    CLR     MAXBIN+1
0000E5B1 7EE6C7      JMP      NSTRT
0000E5B4 7B0841    NRELMAX TIM     %00001000,KEY
0000E5B7      VAL
0000E5B7 2707      BEQ     NCODE
;NOTE!! ONLY THE MOST RECENT VALID CODE IS STORED
0000E5B9 9641      LDAA   KEYVAL
0000E5BB 84F0      ANDA   #$FO
0000E5BD 44        LSRA
0000E5BE 9748      STAA   CODE
                    NCODE
0000E5C0 7EE6C7      JMP      NSTRT
                    NRUNKEYS
0000E5C3 8111      CMPA    #CAL
0000E5C5 2625      BNE     NCAL
0000E5C7 4F        CLRA
0000E5C8 97D5      STAA   CALOFF
0000E5CA 97D6      STAA   CALOFF+1
0000E5CC 97E0      STAA   CALCNT
0000E5CE 976D      STAA   LCDMAXUP
0000E5D0 976E      STAA   LCDCUMUP
0000E5D2 9771      STAA   LCDNOUP
0000E5D4 9770      STAA   NOTYPE
0000E5D6 4C        INCA
0000E5D7 976F      STAA   LCDLEQP
0000E5D9 97C7      STAA   CALFLG
0000E5DB CC03AC    LDD    #03AC
0000E5DE DDDC      STD    CALVAL
0000E5E0 728003    OIM    %10000000,POR set dec pt
0000E5E3      T2
0000E5E3 71F059    AIM    %11110000,LED
0000E5E6      SREG
0000E5E6 720159    OIM    %00000001,LED
0000E5E9      SREG
0000E5E9 7EE6C7      JMP      NSTRT
0000E5EC 7D0073    NCAL   TST    RAMFULL
0000E5EF 2703      BEQ     NFULL2
0000E5F1 7EE6C7      JMP      NSTRT
0000E5F4 8114      NFULL2 CMPA    #EIGHTH
0000E5F6 2642      BNE     NEIGHTH
0000E5F8 710F59    AIM    %00001111,LED

```

0000E5FB			SREG
0000E5FB 728059		OIM	%10000000, LED
0000E5FE			SREG
0000E5FE 4F		CLRA	
0000E5FF 974C		STAA	CUMBIN
0000E601 974D		STAA	CUMBIN+1
0000E603 97CC		STAA	CUMDOSE
0000E605 97CD		STAA	CUMDOSE+1
0000E607 97CE		STAA	CUMDOSE+2
0000E609 97CF		STAA	CUMTIME
0000E60B 97D0		STAA	CUMTIME+1
0000E60D 97D1		STAA	CUMTIME+2
0000E60F 975A		STAA	MAXBIN
0000E611 975B		STAA	MAXBIN+1
0000E613 9766		STAA	RUNBIN
0000E615 9767		STAA	RUNBIN+1
0000E617 9768		STAA	RUNBIN+2
0000E619 4C		INCA	
0000E61A 976A		STAA	ACMODE
0000E61C 9747		STAA	ACTYPE
0000E61E 9769		STAA	TOTALCNT
0000E620 9615	ADWAIT2	LDAA	PORT5
0000E622 8402		ANDA	##00000010
0000E624 26FA		BNE	ADWAIT2
0000E626 9630		LDAA	ADDR
0000E628 817F		CMPA	#\$7F
0000E62A 2207		BHI	LINPOS1
0000E62C 8601		LDAA	#\$01
0000E62E 97DB		STAA	LINASTR
0000E630 7EE6C7		JMP	NSTR
0000E633 8605	LINPOS1	LDAA	#\$05
0000E635 97DB		STAA	LINASTR
0000E637 7EE6C7		JMP	NSTR
0000E63A 8124	NEIGTH	CMPA	#ONESEC
0000E63C 2644		BNE	NOHESEC
0000E63E 710F59		AIM	%00001111, LED
0000E641			SREG
0000E641 724059		OIM	%01000000, LED
0000E644			SREG
0000E644 4F		CLRA	
0000E645 974C		STAA	CUMBIN
0000E647 974D		STAA	CUMBIN+1
0000E649 97CC		STAA	CUMDOSE
0000E64B 97CD		STAA	CUMDOSE+1
0000E64D 97CE		STAA	CUMDOSE+2
0000E64F 97CF		STAA	CUMTIME
0000E651 97D0		STAA	CUMTIME+1
0000E653 97D1		STAA	CUMTIME+2
0000E655 975A		STAA	MAXBIN
0000E657 975B		STAA	MAXBIN+1
0000E659 9766		STAA	RUNBIN
0000E65B 9767		STAA	RUNBIN+1
0000E65D 9768		STAA	RUNBIN+2
0000E65F 4C		INCA	
0000E660 976A		STAA	ACMODE
0000E662 8608		LDAA	#\$8
0000E664 9747		STAA	ACTYPE
0000E666 9769		STAA	TOTALCNT
0000E668 9615	ADWAIT3	LDAA	PORT5

0000E66A	8402		ANDA	##00000010
0000E66C	26FA		BNE	ADWA IT3
0000E66E	9630		LDAA	ADR D
0000E670	817F		CMPA	#\$7F
0000E672	2207		BHI	LINPOS2
0000E674	8601		LDAA	#\$01
0000E676	97DB		STAA	LINASTR
0000E678	7EE6C7		JMP	NS TRT
0000E67B	8605	LINPOS2	LDAA	#\$05
0000E67D	97DB		STAA	LINASTR
0000E67F	7EE6C7		JMP	NS TRT
0000E682	8144	NONESEC	CMPA	#TENSEC
0000E684	2641		BNE	NTENSEC
0000E686	710F59		AIM	%00001111,LED
0000E689				SREG
0000E689	722059		OIM	%00100000,LED
0000E68C				SREG
0000E68C	4F		CLRA	
0000E68D	974C		STAA	CUMBIN
0000E68F	974D		STAA	CUMBIN+1
0000E691	97CC		STAA	CUMDOSE
0000E693	97CD		STAA	CUMDOSE+1
0000E695	97CE		STAA	CUMDOSE+2
0000E697	97CF		STAA	CUMTIME
0000E699	97D0		STAA	CUMTIME+1
0000E69B	97D1		STAA	CUMTIME+2
0000E69D	975A		STAA	MAXBIN
0000E69F	975B		STAA	MAXBIN+1
0000E6A1	9766		STAA	RUNBIN
0000E6A3	9767		STAA	RUNBIN+1
0000E6A5	9768		STAA	RUNBIN+2
0000E6A7	4C		INCA	
0000E6A8	976A		STAA	ACMODE
0000E6AA	8650		LDAA	#\$50
0000E6AC	9747		STAA	ACTYPE
0000E6AE	9769		STAA	TOTALCNT
0000E6B0	9615	ADWA IT4	LDAA	PORT5
0000E6B2	8402		ANDA	##00000010
0000E6B4	26FA		BNE	ADWA IT4
0000E6B6	9630		LDAA	ADR D
0000E6B8	817F		CMPA	#\$7F
0000E6BA	2207		BHI	LINPOS3
0000E6BC	8601		LDAA	#\$01
0000E6BE	97DB		STAA	LINASTR
0000E6C0	7EE6C7		JMP	NS TRT
0000E6C3	8605	LINPOS3	LDAA	#\$05
0000E6C5	97DB		STAA	LINASTR
		NTENSEC		
0000E6C7	7F0041	NS TRT	CLR	KEYVAL
0000E6CA	7F0017		CLR	PORT6
0000E6CD			MEND	

0000E6CD NINTRPRT A.DISPLAY





```

A.DISPLAY MODULE
0000E6CD 5F          CLR B
0000E6CE 9672        LDAA LEDSONF
0000E6D0 2702        BEQ  NLEDS
0000E6D2 D659        LDAB LEDSREG
0000E6D4 D736        NLEDS STAB  LEDS
0000E6D6 7B0171      TIM   $01,LCDNOUP
0000E6D9 2603        BNE  NOUP
0000E6DB 7EE7A7      JMP  NONOUP

NOUP
0000E6DE DC60        LDD  RAMPNTR
0000E6E0 830140      SUBD #RAMSTR
0000E6E3 DD5E        STD  NOBIN
0000E6E5          A.BCDCONV NOBIN;NOBCD

```

```

A.BCDCONV MACRO BINVAL;BCDVAL
;macro to convert values stored in parameter BINVAL
to bcd values in parameter BCDVAL .....bcd digits 4+
5 are also placed in BCDOVF.....BINVAL & BCDVAL 16-bit
registers (CCR contents destroyed)

```

\*\*\*\*\*

```

0000E6E5 36          PSHA          temp store accumulator A
0000E6E6 4F          CLRA
0000E6E7 97C3        STAA BCDOVF

;units
0000E6E9 965F        LDAA NOBIN+1
0000E6EB 840F        ANDA #0F
0000E6ED 810A        CMPA #0A
0000E6EF 2502        BCS  LOSTR
0000E6F1 8B06        ADDA #06
0000E6F3 97C2        LOSTR STAA NOBCD+1
;multiples of 16
0000E6F5 D65F        LDAB NOBIN+1
0000E6F7 C4F0        ANDB #0F0
0000E6F9 54          LSRB
0000E6FA 54          LSRB
0000E6FB 54          LSRB
0000E6FC CEF15D      LOMIDST LDX #BCDTAB1
0000E6FF 3A          ABX
0000E700 EC00        LDD  0,X
0000E702 36          PSHA
0000E703 17          TBA
0000E704 33          PULB
0000E705 9BC2        ADDA NOBCD+1
0000E707 19          DAA
0000E708 97C2        STAA NOBCD+1
0000E70A 36          PSHA
0000E70B 17          TBA
0000E70C 33          PULB
0000E70D 8900        ADCA #00
0000E70F 19          DAA
0000E710 97C1        STAA NOBCD
;multiples of 256
0000E712 D65E        LDAB NOBIN
0000E714 C40F        ANDB #0F
0000E716 58          ASLB
0000E717 CEF17D      HIMIDST LDX #BCDTAB2
0000E71A 3A          ABX

```

```

0000E71B EC00      LDD      0,X
0000E71D 36       PSHA
0000E71E 17       TBA
0000E71F 33       PULB
0000E720 9BC2     ADDA      NOBCD+1
0000E722 19       DAA
0000E723 97C2     STAA      NOBCD+1
0000E725 36       PSHA
0000E726 17       TBA
0000E727 33       PULB
0000E728 99C1     ADCA      NOBCD
0000E72A 19       DAA
0000E72B 97C1     STAA      NOBCD
                ;multiples of 4096 (4 dig only)
0000E72D D65E     LDAB      NOBIN
0000E72F C4F0     ANDB      # $FO
0000E731 54       LSRB
0000E732 54       LSRB
0000E733 54       LSRB
0000E734 CEF19D   HIST     LDX      #BCDTAB3
0000E737 3A       ABX
0000E738 EC00      LDD      0,X
0000E73A 36       PSHA
0000E73B 17       TBA
0000E73C 33       PULB
0000E73D 9BC2     ADDA      NOBCD+1
0000E73F 19       DAA
0000E740 97C2     STAA      NOBCD+1
0000E742 36       PSHA
0000E743 17       TBA
0000E744 33       PULB
0000E745 99C1     ADCA      NOBCD
0000E747 19       DAA
0000E748 97C1     STAA      NOBCD
0000E74A 96C3     LDAA      BCDOVF
0000E74C 8900     ADCA      # $00
0000E74E 97C3     STAA      BCDOVF
                ;other dig of 4096 multiple
0000E750 D65E     LDAB      NOBIN
0000E752 C4F0     ANDB      # $FO
0000E754 54       LSRB
0000E755 54       LSRB
0000E756 54       LSRB
0000E757 54       LSRB
0000E758 CEF1BD   HIST     LDX      #BCDTAB4
0000E75B 3A       ABX
0000E75C A600     LDAA      0,X
0000E75E 9BC3     ADDA      BCDOVF
0000E760 19       DAA
0000E761 97C3     STAA      BCDOVF
0000E763 32       PULA

```

\*\*\*\*\*

```

0000E764          MEND
0000E764 9603     LDAA      PORT2
0000E766 8402     ANDA      #%00000010
0000E768 2603     BNE       PGCORR
0000E76A 7EE782   JMP       NPGCORR

```

Item No.	Description	Quantity	Unit Price	Total Price
1	...	...	...	...
2	...	...	...	...
3	...	...	...	...
4	...	...	...	...
5	...	...	...	...
6	...	...	...	...
7	...	...	...	...
8	...	...	...	...
9	...	...	...	...
10	...	...	...	...
11	...	...	...	...
12	...	...	...	...
13	...	...	...	...
14	...	...	...	...
15	...	...	...	...
16	...	...	...	...
17	...	...	...	...
18	...	...	...	...
19	...	...	...	...
20	...	...	...	...
21	...	...	...	...
22	...	...	...	...
23	...	...	...	...
24	...	...	...	...
25	...	...	...	...
26	...	...	...	...
27	...	...	...	...
28	...	...	...	...
29	...	...	...	...
30	...	...	...	...
31	...	...	...	...
32	...	...	...	...
33	...	...	...	...
34	...	...	...	...
35	...	...	...	...
36	...	...	...	...
37	...	...	...	...
38	...	...	...	...
39	...	...	...	...
40	...	...	...	...
41	...	...	...	...
42	...	...	...	...
43	...	...	...	...
44	...	...	...	...
45	...	...	...	...
46	...	...	...	...
47	...	...	...	...
48	...	...	...	...
49	...	...	...	...
50	...	...	...	...
51	...	...	...	...
52	...	...	...	...
53	...	...	...	...
54	...	...	...	...
55	...	...	...	...
56	...	...	...	...
57	...	...	...	...
58	...	...	...	...
59	...	...	...	...
60	...	...	...	...
61	...	...	...	...
62	...	...	...	...
63	...	...	...	...
64	...	...	...	...
65	...	...	...	...
66	...	...	...	...
67	...	...	...	...
68	...	...	...	...
69	...	...	...	...
70	...	...	...	...
71	...	...	...	...
72	...	...	...	...
73	...	...	...	...
74	...	...	...	...
75	...	...	...	...
76	...	...	...	...
77	...	...	...	...
78	...	...	...	...
79	...	...	...	...
80	...	...	...	...
81	...	...	...	...
82	...	...	...	...
83	...	...	...	...
84	...	...	...	...
85	...	...	...	...
86	...	...	...	...
87	...	...	...	...
88	...	...	...	...
89	...	...	...	...
90	...	...	...	...
91	...	...	...	...
92	...	...	...	...
93	...	...	...	...
94	...	...	...	...
95	...	...	...	...
96	...	...	...	...
97	...	...	...	...
98	...	...	...	...
99	...	...	...	...
100	...	...	...	...

```

0000E76D 96C2      PGCORR   LDAA    NOBCD+1
                ;ADD RAMEND-RAMSTRT
0000E76F 9BE5      ADDA     MEMLBCD+2
0000E771 19        DAA
0000E772 97C2      STAA    NOBCD+1
0000E774 96C1      LDAA    NOBCD
0000E776 99E4      ADCA    MEMLBCD+1
0000E778 19        DAA
0000E779 97C1      STAA    NOBCD
0000E77B 96C3      LDAA    BCDOVF
0000E77D 99E3      ADCA    MEMLBCD
0000E77F 19        DAA
0000E780 97C3      STAA    BCDOVF

                NPGCORR
0000E782 9670      LDAA    NOTYPE
0000E784 270B      BEQ     PAGEUP
0000E786 96C1      LDAA    NOBCD
0000E788 840F      ANDA    #$0F
0000E78A 8AD0      ORAA    #$D0
0000E78C 97C1      STAA    NOBCD
0000E78E 7EE79D     JMP     DONOUP

                PAGEUP
0000E791 96C3      LDAA    BCDOVF
0000E793 D6C1      LDAB    NOBCD
0000E795 04        LSRD
0000E796 04        LSRD
0000E797 04        LSRD
0000E798 04        LSRD
0000E799 8AEO      ORAA    #$EO
0000E79B DDC1      STD     NOBCD
0000E79D DCC1      DONOUP LDD     NOBCD
0000E79F DD44      STD     LCDWORD
0000E7A1 717FO3     AIM    %01111111,POR
0000E7A4      T2
0000E7A4 7EE8E9     JMP     DOLCD

                NONOUP
0000E7A7 7D006D     TST    LCDMAXUP
0000E7AA 2603      BNE    DOMAXUP
0000E7AC 7EE842     JMP     NMAXUP

                DOMAXUP
0000E7AF DC5A      LDD     MAXBIN
0000E7B1 2705      BEQ    ZERMAX
0000E7B3 7F006B     CLR    DBLANKF
0000E7B6 2004      BRA    NZMAX
0000E7B8 8601      ZERMAX LDAA    #$01
0000E7BA 976E      STAA   DBLANKF
0000E7BC      NZMAX  A.BCDCONV MAXBIN;MAXBCD
                A.BCDCONV MACRO  BINVAL;BCDVAL
                ;macro to convert values stored in      parameter BINVAL
                to bcd values in parameter BCDVAL .....bcd digits 4+
                5 are also placed in BCDOVF.....BINVAL & BCDVAL 16-bit
                registers (CCR contents destroyed)

```

\*\*\*\*\*

```

0000E7BC 36      PSHA           temp store accumulator A
0000E7BD 4F      CLRA
0000E7BE 97C3     STAA    BCDOVF

                ;units

```

0000E7C0	965B		LDAA	MAXBIN+1
0000E7C2	840F		ANDA	#\$0F
0000E7C4	810A		CMPA	#\$0A
0000E7C6	2502		BCS	LOSTR
0000E7C8	8B06		ADDA	#\$06
0000E7CA	975D	LOSTR	STAA	MAXBCD+1
		;multiples of 16		
0000E7CC	D65B		LDAB	MAXBIN+1
0000E7CE	C4F0		ANDB	#\$FO
0000E7D0	54		LSRB	
0000E7D1	54		LSRB	
0000E7D2	54		LSRB	
0000E7D3	CEF15D	LOMIDST	LDX	#BCDTAB1
0000E7D6	3A		ABX	
0000E7D7	EC00		LDD	0,X
0000E7D9	36		PSHA	
0000E7DA	17		TBA	
0000E7DB	33		PULB	
0000E7DC	9B5D		ADDA	MAXBCD+1
0000E7DE	19		DAA	
0000E7DF	975D		STAA	MAXBCD+1
0000E7E1	36		PSHA	
0000E7E2	17		TBA	
0000E7E3	33		PULB	
0000E7E4	8900		ADCA	#\$00
0000E7E6	19		DAA	
0000E7E7	975C		STAA	MAXBCD
		;multiples of 256		
0000E7E9	D65A		LDAB	MAXBIN
0000E7EB	C40F		ANDB	#\$0F
0000E7ED	58		ASLB	
0000E7EE	CEF17D	HIMIDST	LDX	#BCDTAB2
0000E7F1	3A		ABX	
0000E7F2	EC00		LDD	0,X
0000E7F4	36		PSHA	
0000E7F5	17		TBA	
0000E7F6	33		PULB	
0000E7F7	9B5D		ADDA	MAXBCD+1
0000E7F9	19		DAA	
0000E7FA	975D		STAA	MAXBCD+1
0000E7FC	36		PSHA	
0000E7FD	17		TBA	
0000E7FE	33		PULB	
0000E7FF	995C		ADCA	MAXBCD
0000E801	19		DAA	
0000E802	975C		STAA	MAXBCD
		;multiples of 4096 (4 dig only)		
0000E804	D65A		LDAB	MAXBIN
0000E806	C4F0		ANDB	#\$FO
0000E808	54		LSRB	
0000E809	54		LSRB	
0000E80A	54		LSRB	
0000E80B	CEF19D	HIST	LDX	#BCDTAB3
0000E80E	3A		ABX	
0000E80F	EC00		LDD	0,X
0000E811	36		PSHA	
0000E812	17		TBA	
0000E813	33		PULB	
0000E814	9B5D		ADDA	MAXBCD+1

```

0000E816 19          DAA
0000E817 975D       STAA          MAXBCD+1
0000E819 36         PSHA
0000E81A 17         TBA
0000E81B 33         PULB
0000E81C 995C       ADCA          MAXBCD
0000E81E 19          DAA
0000E81F 975C       STAA          MAXBCD
0000E821 96C3       LDAA          BCDOVF
0000E823 8900       ADCA          #$00
0000E825 97C3       STAA          BCDOVF
;other dig of 4096 multiple
0000E827 D65A       LDAB          MAXBIN
0000E829 C4F0       ANDB          #$FO
0000E82B 54         LSRB
0000E82C 54         LSRB
0000E82D 54         LSRB
0000E82E 54         LSRB
0000E82F CEF1BD     LDX           #BCDTAB4
0000E832 3A         ABX
0000E833 A600       LDAA          0,X
0000E835 9BC3       ADDA          BCDOVF
0000E837 19          DAA
0000E838 97C3       STAA          BCDOVF
0000E83A 32         PULA

```

\*\*\*\*\*

```

0000E83B          MEND
0000E83B DC5C       LDD           MAXBCD
0000E83D DD44       STD           LCDWORD
0000E83F 7EE8E9     JMP           DOLCD
NMAXUP
0000E842 7D006E     TST           LCDCUMJUP
0000E845 2603       BNE           DOCUMUP
0000E847 7EE8DD     JMP           NCUMUP
DOCUMUP
0000E84A DC4C       LDD           CUMBIN
0000E84C 2705       BEQ           ZERCUM
0000E84E 7F006B     CLR           DBLANKF
0000E851 2004       BRA           NZERCUM
0000E853 8601       ZERCUM       LDAA          #$01
0000E855 976B       ZERCUM       STAA          DBLANKF
0000E857          NZERCUM     A.BCDCONV CUMBIN;CUMBCD
A.BCDCONV MACRO BINVAL;BCDVAL

```

;macro to convert values stored in parameter BINVAL  
to bcd values in parameter BCDVAL .....bcd digits 4+  
5 are also placed in BCDOVF.....BINVAL & BCDVAL 16-bit  
registers (CCR contents destroyed)

\*\*\*\*\*

```

0000E857 36         PSHA          temp store accumulator A
0000E858 4F         CLRA
0000E859 97C3       STAA          BCDOVF
;units
0000E85B 964D       LDAA          CUMBIN+1
0000E85D 840F       ANDA          #$0F
0000E85F 810A       CMPA          #$0A

```

0000E861	2502		BCS	LOSTR
0000E863	8B06		ADDA	#\$06
0000E865	974F	LOSTR	STAA	CUMBCD+1
		;multiples of 16		
0000E867	D64D		LDAB	CUMBIN+1
0000E869	C4FO		ANDB	#\$FO
0000E86B	54		LSRB	
0000E86C	54		LSRB	
0000E86D	54		LSRB	
0000E86E	CEF15D	LOMIDST	LDX	#BCDTAB1
0000E871	3A		ABX	
0000E872	EC00		LDD	0,X
0000E874	36		PSHA	
0000E875	17		TBA	
0000E876	33		PULB	
0000E877	9B4F		ADDA	CUMBCD+1
0000E879	19		DAA	
0000E87A	974F		STAA	CUMBCD+1
0000E87C	36		PSHA	
0000E87D	17		TBA	
0000E87E	33		PULB	
0000E87F	8900		ADCA	#\$00
0000E881	19		DAA	
0000E882	974E		STAA	CUMBCD
		;multiples of 256		
0000E884	D64C		LDAB	CUMBIN
0000E886	C40F		ANDB	#\$0F
0000E888	58		ASLB	
0000E889	CEF17D	HIMIDST	LDX	#BCDTAB2
0000E88C	3A		ABX	
0000E88D	EC00		LDD	0,X
0000E88F	36		PSHA	
0000E890	17		TBA	
0000E891	33		PULB	
0000E892	9B4F		ADDA	CUMBCD+1
0000E894	19		DAA	
0000E895	974F		STAA	CUMBCD+1
0000E897	36		PSHA	
0000E898	17		TBA	
0000E899	33		PULB	
0000E89A	994E		ADCA	CUMBCD
0000E89C	19		DAA	
0000E89D	974E		STAA	CUMBCD
		;multiples of 4096 (4 dig only)		
0000E89F	D64C		LDAB	CUMBIN
0000E8A1	C4FO		ANDB	#\$FO
0000E8A3	54		LSRB	
0000E8A4	54		LSRB	
0000E8A5	54		LSRB	
0000E8A6	CEF19D	HIST	LDX	#BCDTAB3
0000E8A9	3A		ABX	
0000E8AA	EC00		LDD	0,X
0000E8AC	36		PSHA	
0000E8AD	17		TBA	
0000E8AE	33		PULB	
0000E8AF	9B4F		ADDA	CUMBCD+1
0000E8B1	19		DAA	
0000E8B2	974F		STAA	CUMBCD+1
0000E8B4	36		PSHA	



```

0000E8B5 17          TBA
0000E8B6 33          PULB
0000E8B7 994E        ADCA      CUMBCD
0000E8B9 19          DAA
0000E8BA 974E        STAA     CUMBCD
0000E8BC 96C3        LDAA    BCDOVF
0000E8BE 8900        ADCA    #$00
0000E8C0 97C3        STAA    BCDOVF
                ;other dig of 4096 multiple
0000E8C2 D64C        LDAB    CUMBIN
0000E8C4 C4F0        ANDB    #$FO
0000E8C6 54          LSRB
0000E8C7 54          LSRB
0000E8C8 54          LSRB
0000E8C9 54          LSRB
0000E8CA CEF1BD       LDX     #BCDTAB4
0000E8CD 3A          ABX
0000E8CE A600        LDAA    O,X
0000E8D0 9BC3        ADDA    BCDOVF
0000E8D2 19          DAA
0000E8D3 97C3        STAA    BCDOVF
0000E8D5 32          PULA

```

\*\*\*\*\*

```

0000E8D6          MEND
0000E8D6 DC4E        LDD     CUMBCD
0000E8D8 DD44        STD     LCDWORD
0000E8DA 7EE8E9       JMP     DOLCD
                NCUMUP
0000E8DD 7D006F       TST     LCDLEQUP
0000E8E0 2603        BNE    DOLEQUP
0000E8E2 7EE8E9       JMP     NLEQUP
                DOLEQUP
0000E8E5 DCC8          LDD     RUNBCD
0000E8E7 DD44        STD     LCDWORD
                NLEQUP
                DOLCD

```

```

0000E8E9          A.LCDISP          output value to display
                A.LCDISP MACRO
                ;macro to output values stored in parameter LCDWORD
                to locations LCDIG,LCDIG+1,LCDIG+2,LCDIG+3 (CCR cont
                ents destroyed)

```

\*\*\*\*\*

```

0000E8E9          IF          CIRRUS=1
0000E8E9          LOBATW    ALIAS    #$DOFE    LO P
0000E8E9          ELSE
0000E8E9          LOBATW    ALIAS    #$E1DB    P1LE
0000E8E9          ENDF

```

```

0000E8E9 36          PSHA          temp store accumulator A
0000E8EA 9655        LDAA    ERRFLAG
0000E8EC 2747        BEQ     NERDISP
0000E8EE 96D7        LDAA    ERRSTAT
0000E8F0 2727        BEQ     NERRDET
0000E8F2 7F00D8       CLR     ERRHOLD
0000E8F5 717F03       AIM    %01111111,POR

```

资产类别	账面余额	减值准备	账面价值
货币资金	100,000,000.00		100,000,000.00
应收账款	200,000,000.00	20,000,000.00	180,000,000.00
其他应收款	50,000,000.00	5,000,000.00	45,000,000.00
存货	300,000,000.00	30,000,000.00	270,000,000.00
固定资产	400,000,000.00	40,000,000.00	360,000,000.00
无形资产	100,000,000.00		100,000,000.00
长期股权投资	200,000,000.00	20,000,000.00	180,000,000.00
其他权益工具投资	50,000,000.00		50,000,000.00
其他非流动资产	100,000,000.00		100,000,000.00
流动资产合计	1,000,000,000.00	75,000,000.00	925,000,000.00
非流动资产合计	800,000,000.00	60,000,000.00	740,000,000.00
资产总计	1,800,000,000.00	135,000,000.00	1,665,000,000.00
短期借款	100,000,000.00		100,000,000.00
应付账款	200,000,000.00		200,000,000.00
其他应付款	50,000,000.00		50,000,000.00
预收账款	300,000,000.00		300,000,000.00
应付职工薪酬	100,000,000.00		100,000,000.00
应交税费	50,000,000.00		50,000,000.00
其他流动负债	100,000,000.00		100,000,000.00
流动负债合计	1,000,000,000.00		1,000,000,000.00
长期借款	200,000,000.00		200,000,000.00
应付债券	100,000,000.00		100,000,000.00
其他非流动负债	50,000,000.00		50,000,000.00
非流动负债合计	350,000,000.00		350,000,000.00
负债合计	1,350,000,000.00		1,350,000,000.00
所有者权益合计	450,000,000.00		315,000,000.00
股本	100,000,000.00		100,000,000.00
资本公积	200,000,000.00		200,000,000.00
盈余公积	100,000,000.00		100,000,000.00
未分配利润	50,000,000.00		15,000,000.00

0000E8F8			T2	
0000E8F8 8580		BITA	##10000000	
0000E8FA 2707		BEQ	NOVLERR	
0000E8FC CCOADF		LDD	#\$0ADF	O-L
0000E8FF DD44		STD	LCDWORD	
0000E901 2052		BRA	NLEDZER	
0000E903 8540	NOVLERR	BITA	##01000000	
0000E905 2707		BEQ	NCALERR	
0000E907 CCBF01		LDD	##BF01	E 01
0000E90A DD44		STD	LCDWORD	
0000E90C 2047		BRA	NLEDZER	
0000E90E 8520	NCALERR	BITA	##00100000	
0000E910 2707		BEQ	NBATTLO	
0000E912 CCD0FE		LDD	##\$0FE	
0000E915 DD44		STD	LCDWORD	
0000E917 203C		BRA	NLEDZER	
	NBATTLO			
	NERRDET			
0000E919 4F		CLRA		
0000E91A 9755		STAA	ERRFLAG	
0000E91C 4C		INCA		
0000E91D 976B		STAA	DBLANKF	
0000E91F 717F03		AIM	%01111111,POR	
0000E922			T2	
0000E922 2011		BRA	NERDISP	
0000E924 717F03		AIM	%01111111,POR	
0000E927			T2	
0000E927 96D8		LDAA	ERRHOLD	
0000E929 4C		INCA		
0000E92A 97D8		STAA	ERRHOLD	
0000E92C 8108		CMPA	##\$8	
0000E92E 2639		BNE	NUPDATE	
0000E930 4F		CLRA		
0000E931 9755		STAA	ERRFLAG	
0000E933 97D8		STAA	ERRHOLD	
	NERDISP			
0000E935 7B0171		TIM	\$01,LCDNOUP	
0000E938 261B		BNE	NLEDZER	
0000E93A 7B016B		TIM	\$01,DBLANKF	
0000E93D 2708		BEQ	NDBLANK	
0000E93F 86AA		LDAA	##\$AA	
0000E941 9744		STAA	LCDWORD	
0000E943 9745		STAA	LCDWORD+1	
0000E945 200E		BRA	NLEDZER	
0000E947 9644	NDBLANK	LDAA	LCDWORD	suppress leading zero
0000E949 84FO		ANDA	##\$FO	
0000E94B 2608		BNE	NLEDZER	
0000E94D 9644		LDAA	LCDWORD	
0000E94F 840F		ANDA	##\$0F	
0000E951 8AFO		ORAA	##\$FO	
0000E953 9744		STAA	LCDWORD	
	NLEDZER			load high byte to accumulator A
0000E955 9644		LDAA	LCDWORD	
0000E957 9733		STAA	LCDIG+1	output low nibble of high byte
0000E959				shuffle accumulator
0000E959 44		LSRA		
0000E95A 44		LSRA		
0000E95B 44		LSRA		

```

0000E95C 44          LSRA
0000E95D 9732       STAA          LCDIG          output high nibble of high byte
0000E95F

0000E95F 9645       LDAA          LCDWORD+1      load low byte to accumulator A
0000E961
0000E961 9735       STAA          LCDIG+3        output low nibble of low byte
0000E963
0000E963 44          LSRA          shuffle accumulator
0000E964 44          LSRA
0000E965 44          LSRA
0000E966 44          LSRA
0000E967 9734       STAA          LCDIG+2        output high nibble of low byte
0000E969

NUPDATE
0000E969 32          PULA          restore accumulator A

*****
0000E96A          MEND
0000E96A          MEND
0000E96A 7EE1BF      JMP          MLOOP

*****

NMI
0000E96D 9FDE          STS          STAKPTR
0000E96F 9603          LDAA          PORT2
0000E971 97D9          STAA          P2BACK
0000E973 728014       OIM          %10000000, RAM
0000E976
0000E976 71BF14       AIM          %10111111, RAM
0000E979
0000E979 86FF          LDAA          #$$FF
0000E97B C6FF          LDAB          #$$FF
0000E97D 5A          SELF1        DECB
0000E97D 5A          SELF2
0000E97E 26FD          BNE          SELF2
0000E980 4A          DECA
0000E981 26F8          BNE          SELF1

IRQ2
CMI
ICI
OCI
IRQ1

0000E983 0E          CLI
0000E984 3B          RTI

0000E985          MEND

0000E985          A.TIMINT      timer interrupt service routines
0000E985

```

A.TIMINT MODULE  
\*\*\*\*\*

;timer interrupt routines  
TOI

0000E985	9646		LDA	TFLAG	
0000E987	270F		BEQ	PHASE2	
0000E989	710046		AIM	0, TFLAG	
0000E98C	8600		LDAA	#ADPSU	
0000E98E	9737		STAA	ADLOAD	
0000E990	9731		STAA	ADST	
0000E992	9608		LDAA	TCSR1	
0000E994	9609		LDAA	FRC	
0000E996	0E		CLI		
0000E997	3B		RTI		
0000E998	720146	PHASE2	OIM	1, TFLAG	
		:	#\$4B2F		
0000E99B	CC4B2F		LDD	#\$4B2F	
0000E99E	DD09		STD	FRC	
0000E9A0	9630		LDAA	ADRD	
0000E9A2	8153		CMPA	#83	WITH 2:1 RESISTORS 83=4.
0000E9A4					9V
0000E9A4	2305		BLS	BATTLOW	
0000E9A6	71DFD7		AIM	%11011111, ERR	
0000E9A9				STAT	
0000E9A9	2007		BRA	DOCONV	
0000E9AB	8601	BATTLOW	LDAA	#\$1	
0000E9AD	9755		STAA	ERRFLAG	
0000E9AF	7220D7		OIM	%00100000, ERR	
0000E9B2				STAT	
0000E9B2	9615	DOCONV	LDAA	PORT5	
0000E9B4	8470		ANDA	##01110000	
0000E9B6	9750		STAA	DATA	
0000E9B8	8602	ADSTRT	LDAA	#ADLEQ	
0000E9BA	9737		STAA	ADLOAD	
0000E9BC	9731		STAA	ADST	
0000E9BE	9615	ADWAIT	LDAA	PORT5	
0000E9C0	8402		ANDA	##00000010	
0000E9C2	26FA		BNE	ADWAIT	
0000E9C4	9630	ADMISS	LDAA	ADRD	
0000E9C6	9751		STAA	DATA+1	
0000E9C8	9615		LDAA	PORT5	
0000E9CA	8470		ANDA	##01110000	
0000E9CC	9150		CMPA	DATA	
0000E9CE	2709		BEQ	NOCHNGE	
0000E9D0	9750		STAA	DATA	
0000E9D2	C603		LDAB	#\$03	
0000E9D4	5A	TDEL1	DECB		
0000E9D5	26FD		BNE	TDEL1	
0000E9D7	20DF		BRA	ADSTRT	
0000E9D9	9615	NOCHNGE	LDAA	PORT5	
0000E9DB	8480		ANDA	##10000000	
0000E9DD	270A		BEQ	NOLOAD	
0000E9DF	9AD7		ORAA	ERRSTAT	
0000E9E1	97D7		STAA	ERRSTAT	
0000E9E3	8601		LDAA	#\$01	
0000E9E5	9755		STAA	ERRFLAG	
0000E9E7	2003		BRA	INTRES	
0000E9E9	717FD7	NOLOAD	AIM	%01111111, ERR	

```

0000E9EC          STAT
0000E9EC 724003  INTRES  OIM  %01000000,POR
0000E9EF          T2
0000E9EF 71BF03  AIM  %10111111,POR
0000E9F2          T2
0000E9F2 8601          LDAA  #ADLINA
0000E9F4 9737          STAA  ADLOAD
0000E9F6 9731          STAA  ADST
0000E9F8 D650          LDAB  DATA
0000E9FA 54          LSRB
0000E9FB 54          LSRB
0000E9FC 54          LSRB
0000E9FD CEF14D  LDX  #INTOF
0000EA00 3A          ABX
0000EA01 EC00          LDD  O,X
0000EA03 DB51          ADDB  DATA+1
0000EA05 2401          BCC  NDATOVF
0000EA07 4C          INCA
0000EA08 18          NDATOVF XGDX
0000EA09 9603          LDAA  PORT2
0000EA0B 8420          ANDA  #%00100000
0000EA0D 2603          BNE  NGCOMP
0000EA0F C6C9          LDAB  #C9
0000EA11 3A          ABX
          NGCOMP
0000EA12 7D00C7  TST  CALFLG
0000EA15 2705          BEQ  TSTAUTO
0000EA17 71DF03  AIM  %11011111,POR
0000EA1A          T2
0000EA1A 2017          BRA  RUNTST
          TSTAUTO
0000EA1C 7B2003  TIM  %00100000,POR
0000EA1F          T2
0000EA1F 270A          BEQ  LOGAIN
0000EA21 8C0467  CPX  #SCALOF+950
0000EA24 2D0D          BLT  RUNTST
0000EA26 71DF03  AIM  %11011111,POR
0000EA29          T2
0000EA29 2008          BRA  RUNTST
0000EA2B 8C01AB  LOGAIN CPX  #SCALOF+250
0000EA2E 2203          BHI  RUNTST
0000EA30 722003  OIM  %00100000,POR
0000EA33          T2
          RUNTST
0000EA33 18          XGDX
0000EA34 93D5          SUBD  CALOFF
0000EA36 18          XGDX
0000EA37 DF50          STX  DATA
0000EA39 7D006A  TST  ACMODE
0000EA3C 2703          BEQ  NRUNING
0000EA3E 7EEACE  JMP  RUNNING
          NRUNING
0000EA41 DF66          STX  RUNBIN
0000EA43 7F006B  CLR  DBLANKF
0000EA46          A.BCDCONV RUNBIN;RUNBCD
          A.BCDCONV MACRO BINVAL;BCDVAL

```

parameter BINVAL  
to bcd values in parameter BCDVAL .....bcd digits 4+  
5 are also placed in BCDOVF.....BINVAL & BCDVAL 16-bi

t registers (CCR contents destroyed)

\*\*\*\*\*

0000EA46	36		PSHA		temp store accumulator A
0000EA47	4F		CLRA		
0000EA48	97C3		STAA	BCDOVF	
		;units			
0000EA4A	9667		LDAA	RUNBIN+1	
0000EA4C	840F		ANDA	#\$0F	
0000EA4E	810A		CMPA	#\$0A	
0000EA50	2502		BCS	LOSTR	
0000EA52	8B06		ADDA	#\$06	
0000EA54	97C9	LOSTR	STAA	RUNBCD+1	
		;multiples of 16			
0000EA56	D667		LDAB	RUNBIN+1	
0000EA58	C4F0		ANDB	#\$F0	
0000EA5A	54		LSRB		
0000EA5B	54		LSRB		
0000EA5C	54		LSRB		
0000EA5D	CEF15D	LOMIDST	LDX	#BCDTAB1	
0000EA60	3A		ABX		
0000EA61	EC00		LDD	O,X	
0000EA63	36		PSHA		
0000EA64	17		TBA		
0000EA65	33		PULB		
0000EA66	9BC9		ADDA	RUNBCD+1	
0000EA68	19		DAA		
0000EA69	97C9		STAA	RUNBCD+1	
0000EA6B	36		PSHA		
0000EA6C	17		TBA		
0000EA6D	33		PULB		
0000EA6E	8900		ADCA	#\$00	
0000EA70	19		DAA		
0000EA71	97C8		STAA	RUNBCD	
		;multiples of 256			
0000EA73	D666		LDAB	RUNBIN	
0000EA75	C40F		ANDB	#\$0F	
0000EA77	58		ASLB		
0000EA78	CEF17D	HIMIDST	LDX	#BCDTAB2	
0000EA7B	3A		ABX		
0000EA7C	EC00		LDD	O,X	
0000EA7E	36		PSHA		
0000EA7F	17		TBA		
0000EA80	33		PULB		
0000EA81	9BC9		ADDA	RUNBCD+1	
0000EA83	19		DAA		
0000EA84	97C9		STAA	RUNBCD+1	
0000EA86	36		PSHA		
0000EA87	17		TBA		
0000EA88	33		PULB		
0000EA89	99C8		ADCA	RUNBCD	
0000EA8B	19		DAA		
0000EA8C	97C8		STAA	RUNBCD	
		;multiples of 4096 (4 dig only)			
0000EA8E	D666		LDAB	RUNBIN	
0000EA90	C4F0		ANDB	#\$F0	
0000EA92	54		LSRB		
0000EA93	54		LSRB		

```

0000EA94 54          LSRB
0000EA95 CEF19D     HIST  LDX      #BCDTAB3
0000EA98 3A          ABX
0000EA99 EC00       LDD      0,X
0000EA9B 36          PSHA
0000EA9C 17          TBA
0000EA9D 33          PULB
0000EA9E 9BC9       ADDA     RUNBCD+1
0000EAA0 19          DAA
0000EAA1 97C9       STAA    RUNBCD+1
0000EAA3 36          PSHA
0000EAA4 17          TBA
0000EAA5 33          PULB
0000EAA6 99C8       ADCA     RUNBCD
0000EAA8 19          DAA
0000EAA9 97C8       STAA    RUNBCD
0000EAAB 96C3       LDAA    BCDOVF
0000EAAD 8900       ADCA    #00
0000EAAF 97C3       STAA    BCDOVF
;other dig of 4096 multiple
0000EAB1 D666       LDAB    RUNBIN
0000EAB3 C4F0       ANDB    #0F0
0000EAB5 54          LSRB
0000EAB6 54          LSRB
0000EAB7 54          LSRB
0000EAB8 54          LSRB
0000EAB9 CEF1BD     LDX      #BCDTAB4
0000EABC 3A          ABX
0000EABD A600       LDAA    0,X
0000EABF 9BC3       ADDA    BCDOVF
0000EAC1 19          DAA
0000EAC2 97C3       STAA    BCDOVF
0000EAC4 32          PULA

```

```

*****
0000EAC5          MEND
0000EAC5 728003    OIM      %10000000,POR
0000EAC8          T2
0000EAC8 9608     LDAA    TCSR1
0000EACA 9609     LDAA    FRC
0000EACC 0E       CLI
0000EACD 3B       RTI

```

```

*****
RUNNING
0000EACE 9C5A     CPX      MAXBIN
0000EAD0 2502     BCS      MAXOK
0000EAD2 DF5A     STX      MAXBIN
MAXOK
0000EAD4 9669     LDAA    TOTALCNT
0000EAD6 9147     CMPA    ACTYPE
0000EAD8 2609     BNE     NRUNCLR
0000EADA 7F0066    CLR     RUNBIN
0000EADD 7F0067    CLR     RUNBIN+1
0000EAE0 7F0068    CLR     RUNBIN+2
NRUNCLR

```



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\*\*\*\*\*

;log add data to cumulative dose

0000EAE3	DECC	LDX	CUMDOSE	
0000EAE5	9C50	CPX	DATA	
0000EAE7	251E	BCS	BIGDAT1	
0000EAE9	18	XGDX		
0000EAEA	9350	SUBD	DATA	
0000EAEC	8101	CMPA	#\$01	
0000EAEE	2304	BLS	SMDATA1	difference = 255
0000EAF0	8601	LDAA	#\$01	
0000EAF2	C6FF	LDAB	#\$FF	
0000EAF4	05	SMDATA1	ASLD	
0000EAF5	C3F1ED	ADDD	#LOGTAB1	
0000EAF8	18	XGDX		
0000EAF9	EC00	LDD	0,X	
0000EAFB	D3CD	ADDD	CUMDOSE+1	
0000EAFD	DDCD	STD	CUMDOSE+1	
0000EAFF	96CC	LDAA	CUMDCGE	
0000EB01	8900	ADCA	#\$00	
0000EB03	97CC	STAA	CUMDOSE	
0000EB05	2023	BRA	CUMCNEND	
0000EB07	DC50	BIGDAT1	LDD	DATA
0000EB09	93CC	SUBD	CUMDOSE	
0000EB0B	DDCA	STD	DATADIF	
0000EB0D	2304	BLS	SMCUM	
0000EB0F	8601	LDAA	#\$01	
0000EB11	C6FF	LDAB	#\$FF	
0000EB13	05	SMCUM	ASLD	
0000EB14	C3F1ED	ADDD	#LOGTAB1	
0000EB17	18	XGDX		
0000EB18	EC00	LDD	0,X	
0000EB1A	D3CD	ADDD	CUMDCGE+1	
0000EB1C	DDCD	STD	CUMDOSE+1	
0000EB1E	96CC	LDAA	CUMDOSE	
0000EB20	8900	ADCA	#\$00	
0000EB22	97CC	STAA	CUMDCGE	
0000EB24	DCCC	LDD	CUMDCGE	
0000EB26	D3CA	ADDD	DATADIF	
0000EB28	DDCC	STD	CUMDOSE	

CUMCNEND

\*\*\*\*\*

;increment cumulative time

0000EB2A	DCD0	LDD	CUMTIME+1	
0000EB2C	C30001	ADDD	#\$01	
0000EB2F	DDDD	STD	CUMTIME+1	
0000EB31	DCCF	LDD	CUMTIME	
0000EB33	8900	ADCA	#\$00	
0000EB35	97CF	STAA	CUMTIME	

;log convert cumulative time

0000EB37	DCCF	LDD	CUMTIME	
0000EB39	4D	TSTA		
0000EB3A	272B	BEQ	NTHREEB	
0000EB3C	7F00BF	CLR	ROTCNT	
0000EB3F	7C00BF	NXTROT1	INC	ROTCNT
0000EB42	05	ASLD		
0000EB43	24FA	BCC	NXTROT1	
0000EB45	04	LSRD		
0000EB46	8A80	ORAA	##10000000	
0000EB48	7A00BF	DEC	ROTCNT	

```

0000EB4B 16          TAB
0000EB4C C080       SUBB      #$80
0000EB4E 58          ASLB
0000EB4F CEF5ED     LDX      #LOGTAB2
0000EB52 3A          ABX
0000EB53 EC00       LDD      0,X
0000EB55 DDD3       STD      LOGTIME+1
0000EB57 CEF6ED     LDX      #ROTOFF
0000EB5A D6BF       LDAB     ROTCNT
0000EB5C 58          ASLB
0000EB5D 3A          ABX
0000EB5E 16          TAB
0000EB5F 4F          CLRA
0000EB60 E300       ADDD     0,X
0000EB62 DDD2       STD      LOGTIME
0000EB64 7EEB96     JMP      DTIMCMP

```

NTHREEB

```

0000EB67 7F006B     CLR      DBLANKF
0000EB6A DC00       LDD      CUMTIME+1
0000EB6C 7F00BF     CLR      ROTCNT
0000EB6F 7C00BF     INC      ROTCNT
0000EB72 05          ASLD
0000EB73 24FA       BCC      NXTROT2
0000EB75 04          LSRD
0000EB76 8A80       ORAA     #%10000000
0000EB78 7A00BF     DEC      ROTCNT
0000EB7B 16          TAB
0000EB7C C080       SUBB     #$80
0000EB7E 58          ASLB
0000EB7F CEF5ED     LDX      #LOGTAB2
0000EB82 3A          ABX
0000EB83 EC00       LDD      0,X
0000EB85 DDD3       STD      LOGTIME+1
0000EB87 CEF6ED     LDX      #ROTOFF
0000EB8A D6BF       LDAB     ROTCNT
0000EB8C CB08       ADDB     #$08
0000EB8E 58          ASLB
0000EB8F 3A          ABX
0000EB90 16          TAB
0000EB91 4F          CLRA
0000EB92 E300       ADDD     0,X
0000EB94 DDD2       STD      LOGTIME

```

ONLY1

DTIMCMP

```

0000EB96 DCCD       LDD      CUMDOSE+1
0000EB98 93D3       SUBD     LOGTIME+1
0000EB9A 16          TAB
0000EB9B 96CC       LDAA     CUMDOSE
0000EB9D 92D2       SBCA     LOGTIME
0000EB9F DD4C       STD      CUMBIN

```

\*\*\*\*\*  
;log add data word to running total  
RUNCONV

```

0000EBA1 DE66       LDX      RUNBIN
0000EBA3 9C50       CPX      DATA
0000EBA5 251E       BCS      BIGDAT2
0000EBA7 18          XGDX
0000EBA8 9350       SUBD     DATA

```

0000EBAA 8101		CMPA	#\$01	
0000EBAC 2304		BLS	SMDATA2	difference = 255
0000EBAE 8601		LDAA	#\$01	
0000EBB0 C6FF		LDAB	#\$FF	
0000EBB2 05	SMDATA2	ASLD		
0000EBB3 C3F1ED		ADDD	#LOGTAB1	
0000EBB6 18		XGDX		
0000EBB7 EC00		LDD	O,X	
0000EBB9 D367		ADDD	RUNBIN+1	
0000EBBB DD67		STD	RUNBIN+1	
0000EBBD 9666		LDAA	RUNBIN	
0000EBBF 8900		ADCA	#\$00	
0000EBC1 9766		STAA	RUNBIN	
0000EBC3 2023		BRA	RCONVEND	
0000EBC5 DC50	BIGDAT2	LDD	DATA	
0000EBC7 9366		SUBD	RUNBIN	
0000EBC9 DDCA		STD	DATADIF	
0000EBCB 2304		BLS	SMRUN	
0000EBCD 8601		LDAA	#\$01	
0000EBCF C6FF		LDAB	#\$FF	
0000EBD1 05	SMRUN	ASLD		
0000EBD2 C3F1ED		ADDD	#LOGTAB1	
0000EBD5 18		XGDX		
0000EBD6 EC00		LDD	O,X	
0000EBD8 D367		ADDD	RUNBIN+1	
0000EBDA DD67		STD	RUNBIN+1	
0000EBDC 9666		LDAA	RUNBIN	
0000EBDE 8900		ADCA	#\$00	
0000EBE0 9766		STAA	RUNBIN	
0000EBE2 DC66		LDD	RUNBIN	
0000EBE4 D3CA		ADDD	DATADIF	
0000EBE6 DD66		STD	RUNBIN	

RCONVEND  
 \*\*\*\*\*

0000EBE8 7A00C6		DEC	TOGLCNT	
0000EBEB 2607		BNE	NTOGL	
0000EBED 8604		LDAA	#\$4	
0000EBEF 97C6		STAA	TOGLCNT	
0000EBF1 758003		EIM	%10000000,POR	
0000EBF4			T2	

	NTOGL			
0000EBF4 7A0069		DEC	TOTALCNT	
0000EBF7 2703		BEQ	STORE	
0000EBF9 7EECF4		JMP	NSTORE	
0000EBFC 9647	STORE	LDAA	ACTYPE	
0000EBFE 9769		STAA	TOTALCNT	
0000EC00 8101		CMPA	#\$1	
0000EC02 2714		BEQ	TCOMP DN	
0000EC04 8108		CMPA	#\$8	
0000EC06 2609		BNE	TENSCMP	
0000EC08 DC66		LDD	RUNBIN	
0000EC0A 83005A		SUBD	#\$5A	
0000EC0D DD66		STD	RUNBIN	
0000EC0F 2007		BRA	TCOMP DN	
0000EC11 DC66	TENSCMP	LDD	RUNBIN	
0000EC13 8300BE		SUBD	#\$BE	
0000EC16 DD66		STD	RUNBIN	
	TCOMP DN			

```

0000EC18 DC66          LDD      RUNBIN
0000EC1A C30064       ADDD     #100
0000EC1D 18           XGDY
0000EC1E 96D7         LDAA     ERRSTAT
0000EC20 8480         ANDA     #%10000000
0000EC22 9A48         ORAA     CODE
0000EC24 9748         STAA     CODE
0000EC26 18           XGDY
0000EC27 9A48         ORAA     CODE
0000EC29 DE60         LDY      RAMPNTR
0000EC2B 71FE03       AIM      %11111110,POR
0000EC2E              T2
0000EC2E E700         STAB     0,X
0000EC30 720103       OIM      %00000001,POR
0000EC33              T2
0000EC33 A700         STAA     0,X
0000EC35 DE53         LDY      DATACNT+1
0000EC37 08           INX
0000EC38 DF53         STX      DATACNT+1
0000EC3A 2603         BNE      NDTAOVF
0000EC3C 7C0052       INC      DATACNT

```

NDTAOVF

```

0000EC3F DE60         LDY      RAMPNTR
0000EC41 08           INX
0000EC42 8CE000       CPX      #RAMEND
0000EC45 2626         BNE      NRAMOVF
0000EC47 8601         LDAA     #RAMENDB
0000EC49 2706         BEQ      FULL
0000EC4B 9603         LDAA     PORT2
0000EC4D 8402         ANDA     #%00000010
0000EC4F 2712         BEQ      NFULL
0000EC51 8601         LDAA     #1
0000EC53 9773         STAA     RAMFULL
0000EC55 8684         LDAA     #PAUSE
0000EC57 9741         STAA     KEYVAL
0000EC59 860F         LDAA     #%00001111
0000EC5B 9717         STAA     PORT6
0000EC5D 9608         LDAA     TCSR1
0000EC5F 9609         LDAA     FRC
0000EC61 0E           CLI
0000EC62 3B           RTI
0000EC63 CE0140       NFULL   LDY      #RAMSTRT
0000EC66 8601         LDAA     #1
0000EC68 9762         STAA     RAMPNTB
0000EC6A 720203       OIM      %00000010,POR
0000EC6D              T2
0000EC6D DF60         NRAMOVF STX      RAMPNTR
0000EC6F 7F006B       CLR      DBLANKF
0000EC72              A.BCDCONV RUNBIN;RUNBCD

```

A.BCDCONV MACRO BINVAL;BCDVAL  
;macro to convert values stored in ..... parameter BINVAL  
to bcd values in parameter BCDVAL .....bcd digits 4+  
5 are also placed in BCDOVF.....BINVAL & BCDVAL 16-bit  
registers (CCR contents destroyed)

\*\*\*\*\*

```

0000EC72 36           PSHA     temp store accumulator A
0000EC73 4F           CLRA

```

```

0000EC74 97C3          STAA      BCDOVF
                        ;units
0000EC76 9667          LDAA      RUNBIN+1
0000EC78 840F          ANDA      #$0F
0000EC7A 810A          CMPA      #$0A
0000EC7C 2502          BCS      LOSTR
0000EC7E 8B06          ADDA      #$06
0000EC80 97C9          LOSTR    STAA      RUNBCD+1
                        ;multiples of 16
0000EC82 D667          LDAB      RUNBIN+1
0000EC84 C4F0          ANDB     #$F0
0000EC86 54          LSRB
0000EC87 54          LSRB
0000EC88 54          LSRB
0000EC89 CEF15D        LOMIDST  LDX      #BCDTAB1
0000EC8C 3A          ABX
0000EC8D EC00          LDD      0,X
0000EC8F 36          PSHA
0000EC90 17          TBA
0000EC91 33          PULB
0000EC92 9BC9          ADDA      RUNBCD+1
0000EC94 19          DAA
0000EC95 97C9          STAA      RUNBCD+1
0000EC97 36          PSHA
0000EC98 17          TBA
0000EC99 33          PULB
0000EC9A 8900          ADCA     #$00
0000EC9C 19          DAA
0000EC9D 97C8          STAA      RUNBCD
                        ;multiples of 256
0000EC9F D666          LDAB      RUNBIN
0000ECA1 C40F          ANDB     #$0F
0000ECA3 58          ASLB
0000ECA4 CEF17D        HIMIDST  LDX      #BCDTAB2
0000ECA7 3A          ABX
0000ECA8 EC00          LDD      0,X
0000ECAA 36          PSHA
0000ECAB 17          TBA
0000ECAC 33          PULB
0000ECAD 9BC9          ADDA      RUNBCD+1
0000ECAE 19          DAA
0000ECB0 97C9          STAA      RUNBCD+1
0000ECB2 36          PSHA
0000ECB3 17          TBA
0000ECB4 33          PULB
0000ECB5 99C8          ADCA      RUNBCD
0000ECB7 19          DAA
0000ECB8 97C8          STAA      RUNBCD
                        ;multiples of 4096 (4 dig only)
0000ECBA D666          LDAB      RUNBIN
0000ECBC C4F0          ANDB     #$F0
0000ECBE 54          LSRB
0000ECBF 54          LSRB
0000ECC0 54          LSRB
0000ECC1 CEF19D        HIST     LDX      #BCDTAB3
0000ECC4 3A          ABX
0000ECC5 EC00          LDD      0,X
0000ECC7 36          PSHA
0000ECC8 17          TBA

```



0000ECC9	33	PULB	
0000ECCA	9BC9	ADDA	RUNBCD+1
0000ECCC	19	DAA	
0000ECCD	97C9	STAA	RUNBCD+1
0000ECCF	36	PSHA	
0000ECD0	17	TBA	
0000ECD1	33	PULB	
0000ECD2	99C8	ADCA	RUNBCD
0000ECD4	19	DAA	
0000ECD5	97C8	STAA	RUNBCD
0000ECD7	96C3	LDAA	BCDOVF
0000ECD9	8900	ADCA	#\$00
0000ECDB	97C3	STAA	BCDOVF
		;other dig of 4096 multiple	
0000ECDD	D666	LDAB	RUNBIN
0000ECDF	C4FO	ANDB	#\$FO
0000ECE1	54	LSRB	
0000ECE2	54	LSRB	
0000ECE3	54	LSRB	
0000ECE4	54	LSRB	
0000ECE5	CEF1BD	LDX	#BCDTAB4
0000ECE8	3A	ABX	
0000ECE9	A600	LDAA	O,X
0000ECEB	9BC3	ADDA	BCDOVF
0000ECED	19	DAA	
0000ECEE	97C3	STAA	BCDOVF
0000ECFO	32	PULA	

\*\*\*\*\*

0000ECF1		MEND	
0000ECF1	96C4	LDAA	CODUSE
0000ECF3	9A48	ORAA	CODE
0000ECF5	97C4	STAA	CODUSE
0000ECF7	7F0048	CLR	CCDE
		NSTORE	
		FIDLST	
		ADWAIT1	
0000ECFA	9615	LDAA	PORT5
0000ECFC	8402	ANDA	#\$00000010
0000ECFE	26FA	BNE	ADWAIT1
0000ED00	9630	LDAA	ADR
0000ED02	817F	CMPA	#\$7F
0000ED04	2208	BHI	LINPOS
0000ED06	96DB	LDAA	LINASTR
0000ED08	8101	CMPA	#\$1
0000EDA0	2710	BEQ	NFIDDLE
0000ED0C	2006	BRA	FIDDLE
0000ED0E	96DB	LDAA	LINASTR
0000ED10	8105	CMPA	#\$5
0000ED12	2708	BEQ	NFIDDLE
0000ED14	8684	LDAA	#PAUSE
0000ED16	9741	STAA	KEYVAL
0000ED18	8601	LDAA	#\$01
0000ED1A	9772	STAA	LEDSONF
0000ED1C	9608	LDAA	TCSR1
0000ED1E	9609	LDAA	FRC
0000ED20	0E	CLI	
0000ED21	3B	RTI	
0000ED22		MEND	



00000001  
0000ED22

LIST ON  
A.SERIAL



	A.SERIAL	MODULE	
0000ED22	9611	SIO	LDAA TRCSR1
0000ED24	84C0		ANDA #11000000
0000ED26	2603		BNE DORX
0000ED28	7EEFA3		JMP DOTX
0000ED2B	9610	DORX	LDAA RMCR
0000ED2D	9612		LDAA RDR
0000ED2F	811B		CMPA #1B
0000ED31	2704		BEQ DOESC
0000ED33	8107		CMPA #07
0000ED35	2627		BNE NOTESC
0000ED37		DOESC	A.ROMTX ESCSTR
		ROMTX	MACRO ROMSTRG
0000ED37	CEF71D		LDX #ESCSTR
0000ED3A	E600		LDAB 0,X
0000ED3C	08		INX
0000ED3D	DFA0		STX TXPTR
0000ED3F	3A		ABX
0000ED40	DFA2		STX TXEND
0000ED42	5F		CLRB
0000ED43	D7AC		STAB TXBANK
0000ED45	D7AB		STAB TXBYTE
0000ED47	D77E		STAB NUMMODE
0000ED49	D7A5		STAB TXHFLG
0000ED4B	D7AD		STAB TXENDPG
0000ED4D	D7AE		STAB RAMFLAG
0000ED4F	D7B7		STAB PENDFLG
0000ED51	5C		INCB
0000ED52	D7A4		STAB TXFLAG
0000ED54	720411		OIM %0000100,TRC
0000ED57			SRI
0000ED57	CE0080		LDX #RXBUF
0000ED5A	DFA9		STX RXPTR
0000ED5C	0E		CLI
0000ED5D	3B		RTI
0000ED5E			MEND
0000ED5E	8113	NOTESC	CMPA #13
0000ED60	260A		BNE NCTRLS
0000ED62	CE0080		LDX #RXBUF
0000ED65	DFA9		STX RXPTR
0000ED67	71FB11		AIM %11111011,TRC
0000ED6A			SRI
0000ED6A	0E		CLI
0000ED6B	3B		RTI
0000ED6C	8111	NCTRLS	CMPA #11
0000ED6E	260A		BNE NCTRLQ
0000ED70	CE0080		LDX #RXBUF
0000ED73	DFA9		STX RXPTR
0000ED75	720411		OIM %0000100,TRC
0000ED78			SRI
0000ED78	0E		CLI
0000ED79	3B		RTI
0000ED7A	0E	NCTRLQ	CLI
0000ED7B	D67E		LDAB NUMMODE
0000ED7D	2603		BNE DONUM
0000ED7F	7EEE9E		JMP NOTNUM
0000ED82	DEA9	DONUM	LDX RXPTR
0000ED84	A700		STAA 0,X

0000ED86	08		INX	
0000ED87	DFA9		STX	RXPTR
0000ED89	CE008C		LDX	#RXBUF
0000ED8C	C614		LDAB	#20
0000ED8E	3A		ABX	
0000ED9F	9CA9		CPX	RXPTR
0000ED91	2701		BEQ	DODIGS
0000ED93	3B		RTI	
0000ED94	5F	DOBIGS	CLRB	
0000ED95	D77E		STAB	NUMMODE
0000ED97	D7A5		STAB	TXHFLG
0000ED99	D7AB		STAB	TXBYTE
0000ED9B	D7AE		STAB	RAMFLAG
0000ED9D	D7AC		STAB	TXBANK
0000ED9F	D7AD		STAB	TXENDPG
0000EDA1	5C		INCB	
0000EDA2	D7B7		STAB	PENDFLG
0000EDA4	D7A4		STAB	TXFLAG
0000EDA6	CEF738		LDX	#WELCOME
0000EDA9	E600		LDAB	0,X
0000EDAB	08		INX	
0000EDAC	DFA0		STX	TXPTR
0000EDAE	3A		ABX	
0000EDAF	DFA2		STX	TXEND
0000EDB1	CE0080		LDX	#RXBUF
0000EDB4	DFA9		STX	RXPTR
0000EDB6	CE0000		LDX	#0
0000EDB9	DF78		STX	LO32VL1
0000EDBB	DF76		STX	HI32VL1
0000EDBD	DF7C		STX	LO32VL2
0000EDBF	DF7A		STX	HI32VL2
0000EDC1	5F		CLRB	
0000EDC2	37	NXTDIG1	PSHB	
0000EDC3	CE0080		LDX	#RXBUF
0000EDC6	3A		ABX	
0000EDC7	37		PSHB	
0000EDC8	E602		LDAB	2,X
0000EDCA	C030		SUBB	#\$30
0000EDCC	D7AF		STAB	SCRATCH
0000EDCE	860A		LDAA	#10
0000EDE0	33		PULB	
0000EDD1	3D		MUL	
0000EDD2	DBAF		ADDB	SCRATCH
0000EDD4	8900		ADCA	#0
0000EDD6	05		ASLD	
0000EDD7	05		ASLD	
0000EDD8	C3F7AC		ADDD	#HEXTBL
0000EDDB	DD74		STD	DSCRATCH
0000EDDD	DE74		LDX	DSCRATCH
0000EDDF	E000		LDD	0,X
0000EDE1	D378		ADDD	LO32VL1
0000EDE3	DD78		STD	LO32VL1
0000EDE5	2407		BCC	NO32CR1
0000EDE7	3C		PSHX	
0000EDE8	DE76		LDX	HI32VL1
0000EDEA	08		INX	
0000EDEB	DF76		STX	HI32VL1
0000EDED	38		PULX	
0000EDEE	DC76	NO32CR1	LDD	HI32VL1



0000EDFO	E302		ADDD	2,X
0000EDF2	DD76		STD	HI32VL1
0000EDF4	33		PULB	
0000EDF5	5C		INCB	
0000EDF6	C108		CMPB	#8
0000EDF8	26C8		BNE	NXTDIG1
0000EDFA	5F		CLRB	
0000EDFB	37	NXTDIG2	PSHB	
0000EDFC	CE0080		LDX	#RXBUF
0000EDFF	3A		ABX	
0000EE00	37		PSHB	
0000EE01	E60A		LDAB	10,X
0000EE03	C030		SUBB	#\$30
0000EE05	D7AF		STAB	SCRATCH
0000EE07	860A		LDAA	#'0
0000EE09	33		PULB	
0000EE0A	3D		MUL	
0000EE0B	DBAF		ADDB	SCRATCH
0000EE0D	8900		ADCA	#0
0000EE0F	05		ASLD	
0000EE10	05		ASLD	
0000EE11	C3F7AC		ADDD	#HEXTBL
0000EE14	DD74		STD	DSCRTCH
0000EE16	DE74		LDX	DSCRTCH
0000EE18	DC7C		LDD	LO32VL2
0000EE1A	E300		ADDD	0,X
0000EE1C	DD7C		STD	LO32VL2
0000EE1E	2407		BCC	NO32CR2
0000EE20	3C		PSHX	
0000EE21	DE7A		LDX	HI32VL2
0000EE23	08		INX	
0000EE24	DF7A		STX	HI32VL2
0000EE26	38		PULX	
0000EE27	DC7A	NO32CR2	LDD	HI32VL2
0000EE29	E302		ADDD	2,X
0000EE2B	DD7A		STD	HI32VL2
0000EE2D	33		PULB	
0000EE2E	5C		INCB	
0000EE2F	C108		CMPB	#8
0000EE31	26C8		BNE	NXTDIG2
0000EE33	DC78		LDD	LO32VL1
0000EE35	C30140		ADDD	#RAMSTR1
0000EE38	DD78		STD	LO32VL1
0000EE3A	2405		BCC	NO32CR3
0000EE3C	DE76		LDX	HI32VL1
0000EE3E	08		INX	
0000EE3F	DF76		STX	HI32VL1
0000EE41	CEE000	NO32CR3	LDX	#\$E000
0000EE44	9C78		CPX	LO32VL1
0000EE46	220F		BHI	NPGJMP
0000EE48	DC78		LDD	LO32VL1
0000EE4A	C32000		ADDD	#\$2000
0000EE4D	C30140		ADDD	#RAMSTR1
0000EE50	DD78		STD	LO32VL1
0000EE52	DE76		LDX	HI32VL1
0000EE54	08		INX	
0000EE55	DF76		STX	HI32VL1
0000EE57	DC78	NPGJMP	LDD	LO32VL1
0000EE59	DDB8		STD	TXPPEND

1. The first part of the document discusses the general principles of the theory of relativity, including the special theory of relativity and the general theory of relativity. It covers topics such as the equivalence principle, the curvature of spacetime, and the effects of gravity on the motion of objects.

2. The second part of the document focuses on the application of these principles to various physical phenomena, such as the bending of light by gravity, the precession of the perihelion of Mercury, and the gravitational redshift of light. It also discusses the role of relativity in modern physics, particularly in the context of quantum field theory and cosmology.

3. The third part of the document provides a detailed analysis of the experimental evidence that supports the theory of relativity. This includes discussions of the Michelson-Morley experiment, the Eddington experiment on the bending of light, and the Pound-Rebka experiment on gravitational redshift.

4. The fourth part of the document explores the philosophical implications of relativity, particularly the concept of spacetime and the nature of time. It discusses how relativity challenges our intuitive notions of space and time, and how it has influenced our understanding of the universe.

5. The fifth part of the document concludes with a summary of the key findings and a discussion of the future directions of research in this field. It highlights the ongoing efforts to unify general relativity with quantum mechanics and the potential for new discoveries in the years ahead.

0000EE5B	4F		CLRA	
0000EE5C	DE76		LDX	HI32VL1
0000EE5E	2701		BEQ	NOPAGE
0000EE60	4C		JNCA	
0000EE61	97BA	NOPAGE	STAA	TXBPEND
0000EE63	DC78		LDD	L032VL1
0000EE65	D37C		ADDD	L032VL2
0000EE67	DDBB		STD	TXEPEND
0000EE69	2405		BCC	NOENDP1
0000EE6B	DE76		LDX	HI32VL1
0000EE6D	08		INX	
0000EE6E	DF76		STX	HI32VL1
0000EE70	CEE000	NOENDP1	LDX	#\$E000
0000EE73	9CBB		CPX	TXEPEND
0000EE75	220F		BHI	NOENDP2
0000EE77	DCBB		LDD	TXEPEND
0000EE79	C32000		ADDD	#\$2000
0000EE7C	C30140		ADDD	#RAMSTR
0000EE7F	DDEB		STD	TXEPEND
0000EE81	DE76		LDX	HI32VL1
0000EE83	08		INX	
0000EE84	DD76		STD	HI32VL1
0000EE86	DC76	NOENDP2	LDD	HI32VL1
0000EE88	D37A		ADDD	HI32VL2
0000EE8A	2706		BEQ	NOENDP3
0000EE8C	8601		LDAA	#1
0000EE8E	97BD		STAA	TXEBPEND
0000EE90	2003		BRA	ENDPG
0000EE92	4F	NOENDP3	CLRA	
0000EE93	97BD		STAA	TXEBPEND
		ENDPG		
		DORTI		
0000EE95	CE0080		LDX	#RXBUF
0000EE98	DFA9		STX	RXPTR
0000EE9A	720411		OLM	\$00000100,TRC
0000EE9D				SR1
0000EE9D	3B		RTI	
		NOTNUM		
0000EE9E	DEA9		LDX	RXPTR
0000EEA0	A700		STAA	0,X
0000EEA2	08		INX	
0000EEA3	DFA9		STX	RXPTR
0000EEA5	CE0080		LDX	#RXBUF
0000EEA8	C604		LDAB	#4
0000EEAA	3A		ABX	
0000EEAB	9CA9		CPX	RXPTR
0000EEAD	2701		BEQ	DOMESS
0000EEAF	3B		RTI	
		DOMESS		
0000EEB0	CE0080		LDX	#RXBUF
0000EEB3	A600		LDAA	0,X
0000EEB5	8150		CMPA	#'P'
0000EEB7	263A		BNE	NOTPR
0000EEB9	A601		LDAA	1,X
0000EEBB	8152		CMPA	#'R'
0000EEBD	2703		BEQ	MESSOKO
0000EEBF	7EEF7C		JMP	BADMESS
0000EEC2	4F	MESSOKO	CLRA	



1. The first part of the document discusses the importance of maintaining accurate records of all transactions and activities. It emphasizes that this is crucial for ensuring transparency and accountability in the organization's operations.

2. The second part of the document outlines the specific procedures and protocols that must be followed to ensure that all records are properly maintained and updated. This includes details on how data should be collected, stored, and reviewed.

3. The third part of the document addresses the role of management in overseeing the record-keeping process. It highlights the need for regular communication and reporting to ensure that the system remains effective and compliant with all relevant regulations.

4. The fourth part of the document discusses the importance of training and education for all staff members involved in the record-keeping process. It stresses that everyone must understand their responsibilities and the consequences of non-compliance.

5. The fifth part of the document provides a summary of the key points discussed and offers recommendations for further improvement and ongoing monitoring of the record-keeping system.

6. The sixth part of the document details the various methods and tools used to collect and analyze data, ensuring that the information is reliable and actionable.

7. The seventh part of the document discusses the challenges and risks associated with maintaining a comprehensive record-keeping system, such as data loss, security breaches, and human error.

8. The eighth part of the document provides a detailed overview of the current state of the organization's record-keeping practices and identifies areas for immediate attention.

9. The ninth part of the document outlines the long-term goals and objectives for the record-keeping system, including the implementation of new technologies and the establishment of a robust governance framework.

10. The tenth part of the document concludes with a final statement on the commitment to excellence in record-keeping and the ongoing effort to improve the organization's operational efficiency and compliance.

0000EEC3	977E	STAA	NUMMODE
0000EEC5	97AB	STAA	TXBYTE
0000EEC7	97AC	STAA	TXBANK
0000EEC9	97A8	STAA	HDRCTR
0000EECB	97B4	STAA	HSTRTPG
0000EECD	97AE	STAA	RAMFLAG
0000EECF	97BA	STAA	TXPBPEND
0000EED1	4C	INCA	
0000EED2	97A4	STAA	TXFLAG
0000EED4	97B7	STAA	PENDFLG
0000EED6	97A5	STAA	TXHFLG
0000EED8	CE0140	LDX	#RAMSTRT
0000EEDB	DFB8	STX	TXPPEND
0000EEDD	DFA6	STX	HDRSTRT
0000EEDF	CE0080	LDX	#RXBUF
0000EEE2	DFA9	STX	RXPTR
0000EEE4	CEF738	LDX	#WELCOME
0000EEE7	E600	LDAB	O,X
0000EEE9	08	INX	
0000EEEA	DFA0	STX	TXPTR
0000EEEC	3A	ABX	
0000EEED	DFA2	STX	TXEND
0000EEEF	720411	OIM	%00000100,TRC
0000EEF2			SR1
0000EEF2	3B	RTI	
	NOTPR		
0000EEF3	8149	CMPA	#'I'
0000EEF5	2630	BNE	NOTID
0000EEF7	A601	LDAA	1,X
0000EEF9	8144	CMPA	#'D'
0000EEFB	2703	BEQ	MESSOK1
0000EEFD	7EEF2D	JMP	NOTID1
0000EF00	MESSOK1	A.ROMTX	IDMESS
	ROMTX	MACRO	ROMSTRG
0000EF00	CEF74D	LDX	#IDMESS
0000EF03	E600	LDAB	O,X
0000EF05	08	INX	
0000EF06	DFA0	STX	TXPTR
0000EF08	3A	ABX	
0000EF09	DFA2	STX	TXEND
0000EF0B	5F	CLRB	
0000EF0C	D7AC	STAB	TXBANK
0000EF0E	D7AB	STAB	TXBYTE
0000EF10	D77E	STAB	NUMMODE
0000EF12	D7A5	STAB	TXHFLG
0000EF14	D7AD	STAB	TXENDPG
0000EF16	D7AE	STAB	RAMFLAG
0000EF18	D7B7	STAB	PENDFLG
0000EF1A	5C	INCB	
0000EF1B	D7A4	STAB	TXFLAG
0000EF1D	720411	OIM	%00000100,TRC
0000EF20			SR1
0000EF20	CE0080	LDX	#RXBUF
0000EF23	DFA9	STX	RXPTR
0000EF25	0E	CLI	
0000EF26	3B	RTI	
0000EF27		MEND	
	NOTID		
0000EF27	8149	CMPA	#'I'

Item	Description	Quantity	Unit Price	Total Price
1	...	...	...	...
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100	...	...	...	...

0000EF29 2630		BNE	NOTIT
0000EF2B A601		LDAA	1,X
0000EF2D 8154	NOTID1	CMPA	#'T'
0000EF2F 2703		BEQ	MESSOK2
0000EF31 7EEF7C		JMP	BADMESS
0000EF34	MESSOK2	A.ROMTX	ITMESS
	ROMTX	MACRO	ROMSTRG
0000EF34 CEF77A		LDX	#ITMESS
0000EF37 E600		LDAB	0,X
0000EF39 08		INX	
0000EF3A DFA0		STX	TXPTR
0000EF3C 3A		ABX	
0000EF3D DFA2		STX	TXEND
0000EF3F 5F		CLRB	
0000EF40 D7AC		STAB	TXBANK
0000EF42 D7AB		STAB	TXBYTE
0000EF44 D77E		STAB	NUMMODE
0000EF46 D7A5		STAB	TXHFLG
0000EF48 D7AD		STAB	TXENDPG
0000EF4A D7AE		STAB	RAMFLAG
0000EF4C D7B7		STAB	PENDFLG
0000EF4E 5C		INCB	
0000EF4F D7A4		STAB	TXFLAG
0000EF51 720411		OIM	%00000100,TRC
0000EF54			SRI
0000EF54 CE0080		LDX	#RXBUF
0000EF57 DFA9		STX	RXPTR
0000EF59 0E		CLI	
0000EF5A 3B		RTI	
0000EF5B		MEND	
	NOTIT		
0000EF5B 814C		CMPA	#'L'
0000EF5D 260E		BNE	NOTLG
0000EF5F A601		LDAA	1,X
0000EF61 8147		CMPA	#'G'
0000EF63 2703		BEQ	MESSOK3
0000EF65 7EEF7C		JMP	BADMESS
0000EF68 8601	MESSOK3	LDAA	#1
0000EF6A 977E		STAA	NUMMODE
0000EF6C 3B		RTI	
	NOTLG		
0000EF6D 814D		CMPA	#'M'
0000EF6F 260B		BNE	BADMESS
0000EF71 A601		LDAA	1,X
0000EF73 814F		CMPA	#'C'
0000EF75 2605		BNE	BADMESS
0000EF77 8601		LDAA	#1
0000EF79 97C0		STAA	MONFLG
0000EF7B 3B		RTI	
	BADMESS		
0000EF7C		A.ROMTX	ERMESS
	ROMTX	MACRO	ROMSTRG
0000EF7C CEF797		LDX	#ERMESS
0000EF7F E600		LDAB	0,X
0000EF81 08		INX	
0000EF82 DFA0		STX	TXPTR
0000EF84 3A		ABX	
0000EF85 DFA2		STX	TXEND
0000EF87 5F		CLRB	

Account Number	FY2024 Request	FY2025 Request	Description
100-1000-1000	1000	1000	General Fund
100-1000-1001	2000	2000	Public Safety
100-1000-1002	3000	3000	Public Works
100-1000-1003	4000	4000	Public Health
100-1000-1004	5000	5000	Public Administration
100-1000-1005	6000	6000	Public Utilities
100-1000-1006	7000	7000	Public Housing
100-1000-1007	8000	8000	Public Transportation
100-1000-1008	9000	9000	Public Safety
100-1000-1009	10000	10000	Public Works
100-1000-1010	11000	11000	Public Health
100-1000-1011	12000	12000	Public Administration
100-1000-1012	13000	13000	Public Utilities
100-1000-1013	14000	14000	Public Housing
100-1000-1014	15000	15000	Public Transportation
100-1000-1015	16000	16000	Public Safety
100-1000-1016	17000	17000	Public Works
100-1000-1017	18000	18000	Public Health
100-1000-1018	19000	19000	Public Administration
100-1000-1019	20000	20000	Public Utilities
100-1000-1020	21000	21000	Public Housing
100-1000-1021	22000	22000	Public Transportation
100-1000-1022	23000	23000	Public Safety
100-1000-1023	24000	24000	Public Works
100-1000-1024	25000	25000	Public Health
100-1000-1025	26000	26000	Public Administration
100-1000-1026	27000	27000	Public Utilities
100-1000-1027	28000	28000	Public Housing
100-1000-1028	29000	29000	Public Transportation
100-1000-1029	30000	30000	Public Safety
100-1000-1030	31000	31000	Public Works
100-1000-1031	32000	32000	Public Health
100-1000-1032	33000	33000	Public Administration
100-1000-1033	34000	34000	Public Utilities
100-1000-1034	35000	35000	Public Housing
100-1000-1035	36000	36000	Public Transportation
100-1000-1036	37000	37000	Public Safety
100-1000-1037	38000	38000	Public Works
100-1000-1038	39000	39000	Public Health
100-1000-1039	40000	40000	Public Administration
100-1000-1040	41000	41000	Public Utilities
100-1000-1041	42000	42000	Public Housing
100-1000-1042	43000	43000	Public Transportation
100-1000-1043	44000	44000	Public Safety
100-1000-1044	45000	45000	Public Works
100-1000-1045	46000	46000	Public Health
100-1000-1046	47000	47000	Public Administration
100-1000-1047	48000	48000	Public Utilities
100-1000-1048	49000	49000	Public Housing
100-1000-1049	50000	50000	Public Transportation
100-1000-1050	51000	51000	Public Safety
100-1000-1051	52000	52000	Public Works
100-1000-1052	53000	53000	Public Health
100-1000-1053	54000	54000	Public Administration
100-1000-1054	55000	55000	Public Utilities
100-1000-1055	56000	56000	Public Housing
100-1000-1056	57000	57000	Public Transportation
100-1000-1057	58000	58000	Public Safety
100-1000-1058	59000	59000	Public Works
100-1000-1059	60000	60000	Public Health
100-1000-1060	61000	61000	Public Administration
100-1000-1061	62000	62000	Public Utilities
100-1000-1062	63000	63000	Public Housing
100-1000-1063	64000	64000	Public Transportation
100-1000-1064	65000	65000	Public Safety
100-1000-1065	66000	66000	Public Works
100-1000-1066	67000	67000	Public Health
100-1000-1067	68000	68000	Public Administration
100-1000-1068	69000	69000	Public Utilities
100-1000-1069	70000	70000	Public Housing
100-1000-1070	71000	71000	Public Transportation
100-1000-1071	72000	72000	Public Safety
100-1000-1072	73000	73000	Public Works
100-1000-1073	74000	74000	Public Health
100-1000-1074	75000	75000	Public Administration
100-1000-1075	76000	76000	Public Utilities
100-1000-1076	77000	77000	Public Housing
100-1000-1077	78000	78000	Public Transportation
100-1000-1078	79000	79000	Public Safety
100-1000-1079	80000	80000	Public Works
100-1000-1080	81000	81000	Public Health
100-1000-1081	82000	82000	Public Administration
100-1000-1082	83000	83000	Public Utilities
100-1000-1083	84000	84000	Public Housing
100-1000-1084	85000	85000	Public Transportation
100-1000-1085	86000	86000	Public Safety
100-1000-1086	87000	87000	Public Works
100-1000-1087	88000	88000	Public Health
100-1000-1088	89000	89000	Public Administration
100-1000-1089	90000	90000	Public Utilities
100-1000-1090	91000	91000	Public Housing
100-1000-1091	92000	92000	Public Transportation
100-1000-1092	93000	93000	Public Safety
100-1000-1093	94000	94000	Public Works
100-1000-1094	95000	95000	Public Health
100-1000-1095	96000	96000	Public Administration
100-1000-1096	97000	97000	Public Utilities
100-1000-1097	98000	98000	Public Housing
100-1000-1098	99000	99000	Public Transportation
100-1000-1099	100000	100000	Public Safety

0000EF88	D7AC		STAB	TXBANK
0000EF8A	D7AB		STAB	TXBYTE
0000EF8C	D77E		STAB	NUMMODE
0000EF8E	D7A5		STAB	TXHFLG
0000EF90	D7AD		STAB	TXENDPG
0000EF92	D7AE		STAB	RAMFLAG
0000EF94	D7B7		STAB	PENDFLG
0000EF96	5C		INCB	
0000EF97	D7A4		STAB	TXFLAG
0000EF99	720411		OJM	%00000100,TRC
0000EF9C				SR1
0000EF9C	CE0080		LDX	#RXBUF
0000EF9F	DFA9		STX	RXPTR
0000EFA1	0E		CLI	
0000EFA2	3B		RTI	
0000EFA3			MEND	
0000EFA3	96A4	DOTX	LDAA	TXFLAG
0000EFA5	2605		BNE	DOTX1
0000EFA7	71FB11		AIM	%11111011,TRC
0000EFAA				SR1
0000EFAA	0E		CLI	
0000EFAB	3B		RTI	
0000EFAC	8601	DOTX1	LDAA	#\$1
0000EFAE	4A	TRWAIT	DECA	
0000EFAF	26FD		BNE	TRWAIT
0000EFB1			IF	HD6303Y=1
0000EFB1			ELSE	
			LDAA	RMCR
			ORAA	/%01000000
			STAA	RMCR
0000EFB1			ENDIF	
0000EFB1	96AE		LDAA	RAMFLAG
0000EFB3	262E		BNE	DO16BIT
0000EFB5	DEA0		LDX	TXPTR
0000EFB7	A600		LDAA	O,X
0000EFB9	9713		STAA	TDR
0000EFBB	0E		CLI	
0000EFBC	08		INX	
0000EFBD	DFA0		STX	TXPTR
0000EFBF	9CA2		CPX	TXEND
0000EFC1	261F		BNE	MOREMES
0000EFC3	96B7		LDAA	PENDFLG
0000EFC5	2715		BEQ	NOPEND
0000EFC7	8501		LDAA	#1
0000EFC9	97AE		STAA	RAMFLAG
0000EFCB	DEB8		LDX	TXPPEND
0000EFCD	DFA0		STX	TXPTR
0000EFCF	96BA		LDAA	TXBPEND
0000EFD1	97AC		STAA	TXBANK
0000EFD3	96BD		LDAA	TXEBPEND
0000EFD5	97AD		STAA	TXENDPG
0000EFD7	DEBB		LDX	TXEPEND
0000EFD9	DFA2		STX	TXEND
0000EFD E	3B		RTI	
0000EFD C	4F	NOPEND	CLRA	
0000EFD D	97A4		STAA	TXFLAG
0000EFD F	71FB11		AIM	%11111011,TRC
0000EFE2				SR1

1900

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1902

Year	Month	Day	Time
1900	Jan	1	10:00
1901	Jan	1	10:00
1902	Jan	1	10:00
1900	Feb	1	10:00
1901	Feb	1	10:00
1902	Feb	1	10:00
1900	Mar	1	10:00
1901	Mar	1	10:00
1902	Mar	1	10:00
1900	Apr	1	10:00
1901	Apr	1	10:00
1902	Apr	1	10:00
1900	May	1	10:00
1901	May	1	10:00
1902	May	1	10:00
1900	Jun	1	10:00
1901	Jun	1	10:00
1902	Jun	1	10:00
1900	Jul	1	10:00
1901	Jul	1	10:00
1902	Jul	1	10:00
1900	Aug	1	10:00
1901	Aug	1	10:00
1902	Aug	1	10:00
1900	Sep	1	10:00
1901	Sep	1	10:00
1902	Sep	1	10:00
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1902	Oct	1	10:00
1900	Nov	1	10:00
1901	Nov	1	10:00
1902	Nov	1	10:00
1900	Dec	1	10:00
1901	Dec	1	10:00
1902	Dec	1	10:00

0000EFE2	3B	MOREMES	RTI	
		DO16BIT		
0000EFE3	9603		LDAA	PORT2
0000EFE5	977F		STAA	P2SAVE
0000EFE7	96AB		LDAA	TXBYTE
0000EFE9	2705		BEQ	NOBANK
0000EFEB	720103		OIM	%00000001,POR
0000EFEE				T2
0000EFEE	2003		BRA	BNKDONE
0000EFF0	71FE03	NOBANK	AIM	%11111110,POR
0000EFF3				T2
0000EFF3	96AC	BNKDONE	LDAA	TXBANK
0000EFF5	2705		BEQ	NOPGE
0000EFF7	720203		OIM	%00000010,POR
0000EFFA				T2
0000EFFA	2003		BRA	PGDONE
0000EFFC	71FD03	NOPGE	AIM	%11111101,POR
0000EFFF				T2
0000EFFF	DEA0	PGDONE	LDX	TXPTR
0000F001	A600		LDAA	O,X
0000F003	9713		STAA	TDR
0000F005	97AF		STAA	SCRATCH
0000F007	967F		LDAA	P2SAVE
0000F009	9703		STAA	PORT2
0000F00B	0E		CLI	
0000F00C	96A5		LDAA	TXHFLG
0000F00E	272E		BEQ	NOTHDR1
0000F010	96AB		LDAA	TXBYTE
0000F012	2615		BNE	HDRBNK1
0000F014	96A8		LDAA	HDRCTR
0000F016	8106		CMPA	#6
0000F018	2606		BNE	NOT6
0000F01A	96AF		LDAA	SCRATCH
0000F01C	97B3		STAA	OFFSET1
0000F01E	201E		BRA	NOTHDR1
0000F020	8107	NOT6	CMPA	#7
0000F022	261A		BNE	NOTHDR1
0000F024	96AF		LDAA	SCRATCH
0000F026	97B1		STAA	OFFSET3
0000F028	2018		BRA	NOTHDR1
0000F02A	96A8	HDRBNK1	LDAA	HDRCTR
0000F02C	8106		CMPA	#6
0000F02E	2606		BNE	NOT16
0000F030	96AF		LDAA	SCRATCH
0000F032	97B2		STAA	OFFSET2
0000F034	2008		BRA	NOTHDR1
0000F036	8107	NOT16	CMPA	#7
0000F038	2604		BNE	NOTHDR1
0000F03A	96AF		LDAA	SCRATCH
0000F03C	97B0		STAA	OFFSET4
0000F03E	96AB	NOTHDR1	LDAA	TXBYTE
0000F040	2604		BNE	DOBNKO
0000F042	4C		INCA	
0000F043	97AB		STAA	TXBYTE
0000F045	3B		RTI	
0000F046	4F	DOBNKO	CLRRA	
0000F047	97AB		STAA	TXBYTE
0000F049	DEA0		LDX	TXPTR
0000F04E	08		INX	



Main body of the document containing several columns of text, possibly representing a list or data table. The text is very faint and difficult to read.

0000F04C	DFA0		STX	TXPTR
0000F04E	8CE000		CPX	#\$E000
0000F051	260F		BNE	NOFLIP
0000F053	96AC		LDAA	TXBANK
0000F055	8101		CMPA	#RAMENDB
0000F057	2719		BEQ	DATADN
0000F059	CE0140		LDX	#RAMSTRT
0000F05C	DFA0		STX	TXPTR
0000F05E	8601		LDAA	#1
0000F060	97AC		STAA	TXBANK
0000F062	96A5	NOFLIP	LDAA	TXHFLG
0000F064	2613		BNE	DOHDR
0000F066	9CA2		CPX	TXEND
0000F068	2701		BEQ	TESTPG
0000F06A	3B		RTI	
0000F06B	96AC	TESTPG	LDAA	TXBANK
0000F06D	91AD		CMPA	TXENDPG
0000F06F	2701		BEQ	DATADN
0000F071	3B		RTI	
0000F072	4F	DATADN	CLRA	
0000F073	97A4		STAA	TXFLAG
0000F075	71FB11		AIM	%11111011,TRC
0000F078				SR1
0000F078	3B		RTI	
0000F079	96A8	DOHDR	LDAA	HDRCTR
0000F07B	4C		INCA	
0000F07C	97A8		STAA	HDRCTR
0000F07E	8110		CMPA	#16
0000F080	2701		BEQ	NXTHDR
0000F082	3B		RTI	
0000F083	4F	NXTHDR	CLRA	
0000F084	97A5		STAA	HDRCTR
0000F086	96B3		LDAA	OFFSET1
0000F088	2615		BNE	NXTHDR1
0000F08A	96B2		LDAA	OFFSET2
0000F08C	2611		BNE	NXTHDR1
0000F08E	96B1		LDAA	OFFSET3
0000F090	260D		BNE	NXTHDR1
0000F092	96B0		LDAA	OFFSET4
0000F094	2609		BNE	NXTHDR1
0000F096	4F		CLRA	
0000F097	97A4		STAA	TXFLAG
0000F099	71FB11		AIM	%11111011,TRC
0000F09C				SR1
0000F09C	97A5		STAA	TXHFLG
0000F09E	3B		RTI	
0000F09F	DCB2	NXTHDR1	LDD	OFFSET2
0000FA01	D3A6		ADDD	HDRSTRT
0000FA03	DDA6		STD	HDRSTRT
0000FA05	DDA0		STD	TXPTR
0000FA07	96B4		LDAA	HSTRTPG
0000FA09	99B1		ADCA	OFFSET3
0000FA0B	97B4		STAA	HSTRTPG
0000FA0D	97AC		STAA	TXBANK
0000FA0F	3B		RTI	
0000F0B0			MEND	
0000F0B0			A. TEST	

	A. TEST	MODULE	
0000FOB0 FE0100	RAMDUMP	LDX	DMPSTRT
0000FOB3 BDFOB9		JSR	TEST
0000FOB6 7EF913		JMP	MONITA+9
	TEST		
	;SEI		
0000FOB9 3C		PSHX	
0000FOBA 4F		CLRA	
0000FOBB 97B6	NXTLIN	STAA	LINCTR
0000FOBD 4F		CLRA	
0000FOBE 97B5	NXTBYT	STAA	BYTCTR
0000FOC0 9611	TXWT1	LDAA	TRCSR1
0000FOC2 8420		ANDA	##00100000
0000FOC4 27FA		BEQ	TXWT1
0000FOC6 9610		LDAA	RMCR
0000FOC8 8A40		ORAA	##01000000
0000FOCA 9710		STAA	RMCR
0000FOCC A600		LDAA	0,X
0000FOCE 84FO		ANDA	##11110000
0000FODO 44		LSRA	
0000FOD1 44		LSRA	
0000FOD2 44		LSRA	
0000FOD3 44		LSRA	
0000FOD4 8109		CMPA	#9
0000FOD6 2304		BLS	NOTASC1
0000FOD8 8B37		ADDA	#55
0000FODA 2002		BRA	ASCDN1
0000FODC 8B30	NOTASC1	ADDA	#48
0000FODE 9713	ASCDN1	STAA	TDR
0000FOEO 9611	TXWT2	LDAA	TRCSR1
0000FOE2 8420		ANDA	##00100000
0000FOE4 27FA		BEQ	TXWT2
0000FOE6 9610		LDAA	RMCR
0000FOE8 8A40		ORAA	##01000000
0000FOEA 9710		STAA	RMCR
0000FOEC A600		LDAA	0,X
0000FOEE 840F		ANDA	##00001111
0000FOFO 8109		CMPA	#9
0000FOF2 2304		BLS	NOTASC2
0000FOF4 8B37		ADDA	#55
0000FOF6 2002		BRA	ASCDN2
0000FOF8 8B30	NOTASC2	ADDA	#48
0000FOFA 9713	ASCDN2	STAA	TDR
0000FOFC 08		INX	
0000FOFD 9611	TXWT3	LDAA	TRCSR1
0000FOFF 8420		ANDA	##00100000
0000F101 27FA		BEQ	TXWT3
0000F103 9610		LDAA	RMCR
0000F105 8A40		ORAA	##01000000
0000F107 9710		STAA	RMCR
0000F109 8620		LDAA	#\$20
0000F10B 9713		STAA	TDR
0000F10D 96B5		LDAA	BYTCTR
0000F10F 4C		INCA	
0000F110 8108		CMPA	#8
0000F112 26AA		BNE	NXTBYT
0000F114 9611	TXWT4	LDAA	TRCSR1
0000F116 8420		ANDA	##00100000



```

0000F118 27FA      BEQ      TXWT4
0000F11A 9610      LDAA     RMCR
0000F11C 8A40      ORAA     #01000000
0000F11E 9710      STAA     RMCR
0000F120 860D      LDAA     #0D
0000F122 9713      STAA     TDR
0000F124 9611      LDAA     TRCSR1
0000F126 8420      ANDA     #00100000
0000F128 27FA      BEQ      TXWT5
0000F12A 9610      LDAA     RMCR
0000F12C 8A40      ORAA     #01000000
0000F12E 9710      STAA     RMCR
0000F130 860A      LDAA     #0A
0000F132 9713      STAA     TDR
0000F134 96B6      LDAA     LINCTR
0000F136 4C        INCA
0000F137 810A      CMPA     #10
0000F139 2680      BNE     NXTLIN
0000F13B 9611      LDAA     TRCSR1
0000F13D 8420      ANDA     #00100000
0000F13F 27FA      BEQ      TXWT6
0000F141 9610      LDAA     RMCR
0000F143 8A40      ORAA     #01000000
0000F145 9710      STAA     RMCR
0000F147 860A      LDAA     #0A
0000F149 9713      STAA     TDR
0000F14B 38        PULX

;CLI

0000F14C 39        RTS

0000F14D      MEND

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0000F14D

A. TABLES

10/10/2017 10:10:10 AM 10/10/2017 10:10:10 AM 10/10/2017 10:10:10 AM

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A.TABLES MODULE

;module to define all the tables used in the CRL236 program

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0000F14D	00B10166	INTOF	FDB	SCALOF,SCALOF
0000F151	021A0238			+181,SCALOF+3
0000F155	02ED03A1			61,SCALOF+391
0000F159	00000000			,SCALOF+572,S
0000F15D				CALOF+752,0,0

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0000F15D	00000016	BCDTAB1	FDB	\$0000,\$0016,\$
0000F161	00320048			0032,\$0048,\$0
0000F165	00640080			064,\$0080,\$00
0000F169	00960112			96,\$0112,\$012
0000F16D	01280144			8,\$0144,\$0160
0000F171	01600176			,\$0176,\$0192,
0000F175	01920208			\$0208,\$0224,\$
0000F179	02240240			0240
0000F17D	00000256	BCDTAB2	FDB	\$0000,\$0256,\$
0000F181	05120768			0512,\$0768,\$1
0000F185	10241280			024,\$1280,\$15
0000F189	15361792			36,\$1792,\$204
0000F18D	20482304			8,\$2304,\$2560
0000F191	25602816			,\$2816,\$3072,
0000F195	30723328			\$3328,\$3584,\$
0000F199	35843840			3840
0000F19D	00004096	BCDTAB3	FDB	\$0000,\$4096,\$
0000F1A1	81922288			8192,\$2288,\$6
0000F1A5	63840480			384,\$0480,\$45
0000F1A9	45768672			76,\$8672,\$276
0000F1AD	27686864			8,\$6864,\$0960
0000F1B1	09605056			,\$5056,\$9152,
0000F1B5	91523248			\$3248,\$7344,\$
0000F1B9	73441440			1440
0000F1BD	00000001	BCDTAB4	FCB	\$00,\$00,\$00,\$
0000F1C1	01020202			01,\$01,\$02,\$0
0000F1C5	03030404			2,\$02,\$03,\$03
0000F1C9	04050506			,\$04,\$04,\$04,
0000F1CD				\$05,\$05,\$06

\*\*\*\*\*

0000F1CD	01010000	HLOOK	FDB	\$0101,\$0000,\$
0000F1D1	00000000			0000,\$0000,\$0
0000F1D5	00000000			000,\$0000,\$00
0000F1D9	00000000			00,\$0000,\$001
0000F1DD	00100000			0,\$0000,\$0000
0000F1E1	00000001			,\$0001,\$0100,
0000F1E5	01000000			\$0000,\$0000,\$
0000F1E9	00000302			0302

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0000F1ED		LOGTAB1	LOAD	A.ADDLOG
0000F5ED		LOGTAB2	LOAD	A.TIMLOG



0000F6ED	010F012D	ROTOFF	FDB	\$010F,\$012D,\$
0000F6F1	014B0169			014B,\$0169,\$0
0000F6F5	018701A5			187,\$01A5,\$01
0000F6F9	01C401E2			C4,\$01E2
0000F6FD	00F100D3		FDB	\$00F1,\$00D3,\$
0000F701	00B50097			00B5,\$0097,\$0
0000F705	0078005A			078,\$005A,\$00
0000F709	003C001E			3C,\$001E,\$000
0000F70D	0000FFE2			0,\$FFE2,\$FFC4
0000F711	FFC4FFA6			,\$FFA6,\$FF88,
0000F715	FF88FF69			\$FF69,\$FF4B,\$
0000F719	FF4BFF2D			FF2D

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0000F71D MEND

0000F71D

A.STRING

Polymerization System	Temperature (°C)	Decomposition Product(s)
ZnO / AlR <sub>3</sub>	100	AlR <sub>3</sub>
	150	AlR <sub>3</sub>
	200	AlR <sub>3</sub>
	250	AlR <sub>3</sub>
	300	AlR <sub>3</sub>
	350	AlR <sub>3</sub>
	400	AlR <sub>3</sub>
	450	AlR <sub>3</sub>
	500	AlR <sub>3</sub>
	550	AlR <sub>3</sub>
ZnO / AlR <sub>3</sub> / ZnEt <sub>2</sub>	100	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	150	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	200	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	250	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	300	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	350	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	400	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	450	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	500	AlR <sub>3</sub> , ZnEt <sub>2</sub>
	550	AlR <sub>3</sub> , ZnEt <sub>2</sub>
ZnO / AlR <sub>3</sub> / ZnEt <sub>2</sub> / ZnMe <sub>2</sub>	100	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	150	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	200	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	250	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	300	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	350	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	400	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	450	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	500	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
	550	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub>
ZnO / AlR <sub>3</sub> / ZnEt <sub>2</sub> / ZnMe <sub>2</sub> / ZnPh <sub>2</sub>	100	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	150	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	200	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	250	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	300	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	350	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	400	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	450	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	500	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>
	550	AlR <sub>3</sub> , ZnEt <sub>2</sub> , ZnMe <sub>2</sub> , ZnPh <sub>2</sub>

	A.STRING	MODULE	
0000F71D		IF	CIRRUS=1
0000F71D	INSTYPE	ALIAS	"CRL 2.36 "
0000F71D		ELSE	
	INSTYPE	ALIAS	"SA 11.40 "
0000F71D		ENDIF	
0000F71D 1A	ESCSTR	EQUB	26
0000F71E 43524C20		EQUB	"CRL 2.36 "
0000F722 322E3336			
0000F726 2020			
0000F728 30303030		EQUB	"000001"
0000F72C 3031			
0000F72E 0D0A0D0A		EQUB	13,10,13,10
0000F732 39363030		EQUB	"9600"
0000F736 0D0A		EQUB	13,10
0000F738 14	WELCOME	EQUB	20
0000F739 43524C20		EQUB	"CRL 2.36 "
0000F73D 322E3336			
0000F741 2020			
0000F743 30303030		EQUB	"000001"
0000F747 3031			
0000F749 0D0A0D0A		EQUB	13,10,13,10
0000F74D 2C	IDMESS	EQUB	44
0000F74E 43524C20		EQUB	"CRL 2.36 "
0000F752 322E3336			
0000F756 2020			
0000F758 73657220		EQUB	"ser #"
0000F75C 23			
0000F75D 30303030		EQUB	"000001"
0000F761 3031			
0000F763 20524F4D		EQUB	" ROM ver 1.0
0000F767 20766572			0 rev 0"
0000F76B 20312E30			
0000F76F 30207265			
0000F773 762030			
0000F776 0D0A0D0A		EQUB	13,10,13,10
0000F77A 1C	ITMESS	EQUB	28
0000F77B 43524C20		EQUB	"CRL 2.36 "
0000F77F 322E3336			
0000F783 2020			
0000F785 30303030		EQUB	"000001"
0000F789 3031			
0000F78B 0D0A0D0A		EQUB	13,10,13,10
0000F78F 30303031		EQUB	"000100"
0000F793 3030			
0000F795 0D0A		EQUB	13,10
0000F797 14	ERMESS	EQUB	20
0000F798 43524C20		EQUB	"CRL 2.36 "
0000F79C 322E3336			
0000F7A0 2020			
0000F7A2 30303030		EQUB	"000001"
0000F7A6 3031			
0000F7A8 2424		EQUB	"\$\$"
0000F7AA 0D0A		EQUB	13,10

Item No.	Description	Quantity	Unit	Remarks
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0000F7B0	96800098		FDB	\$9680,\$0098,	;10000000
0000F7B4	2D000131		FDB	\$2D00,\$0131,	;20000000
0000F7B8	C38001C9		FDB	\$C380,\$01C9,	;30000000
0000F7BC	5A000262		FDB	\$5A00,\$0262,	;40000000
0000F7C0	F08002FA		FDB	\$F080,\$02FA,	;50000000
0000F7C4	87000393		FDB	\$8700,\$0393,	;60000000
0000F7C8	1D80042C		FDB	\$1D80,\$042C,	;70000000
0000F7CC	B40004C4		FDB	\$B400,\$04C4,	;80000000
0000F7D0	4A80055D		FDB	\$4A80,\$055D,	;90000000
0000F7D4	00000000		FDB	\$0000,\$0000,	;00000000
0000F7D8	4240000F		FDB	\$4240,\$000F,	;01000000
0000F7DC	8480001E		FDB	\$8480,\$001E,	;02000000
0000F7E0	C6C0002D		FDB	\$C6C0,\$002D,	;03000000
0000F7E4	0090003D		FDB	\$0090,\$003D,	;04000000
0000F7E8	4640004C		FDB	\$4640,\$004C,	;05000000
0000F7EC	8D80005B		FDB	\$8D80,\$005B,	;06000000
0000F7F0	CF00006A		FDB	\$CF00,\$006A,	;07000000
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0000F7F8	54400089		FDB	\$5440,\$0089,	;09000000
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0000F800	86A00001		FDB	\$86A0,\$0001,	;00100000
0000F804	0D400003		FDB	\$0D40,\$0003,	;00200000
0000F808	93E00004		FDB	\$93E0,\$0004,	;00300000
0000F80C	1A800006		FDB	\$1A80,\$0006,	;00400000
0000F810	A1200007		FDB	\$A120,\$0007,	;00500000
0000F814	27C00009		FDB	\$27C0,\$0009,	;00600000
0000F818	AE60000A		FDB	\$AE60,\$000A,	;00700000
0000F81C	3500000C		FDB	\$3500,\$000C,	;00800000
0000F820	BBE0000D		FDB	\$BBE0,\$000D,	;00900000
0000F824	00000000		FDB	\$0000,\$0000,	;00000000
0000F828	27100000		FDB	\$2710,\$0000,	;00010000
0000F82C	4E200000		FDB	\$4E20,\$0000,	;00020000
0000F830	75300000		FDB	\$7530,\$0000,	;00030000
0000F834	9C400000		FDB	\$9C40,\$0000,	;00040000
0000F838	C3500000		FDB	\$C350,\$0000,	;00050000
0000F83C	EA600000		FDB	\$EA60,\$0000,	;00060000
0000F840	11700001		FDB	\$1170,\$0001,	;00070000
0000F844	38800001		FDB	\$3880,\$0001,	;00080000
0000F848	5F900001		FDB	\$5F90,\$0001,	;00090000
0000F84C	00000000		FDB	\$0000,\$0000,	;00000000
0000F850	03E80000		FDB	\$03E8,\$0000,	;00001000
0000F854	07D00000		FDB	\$07D0,\$0000,	;00002000
0000F858	0BE80000		FDB	\$0BE8,\$0000,	;00003000
0000F85C	0FA00000		FDB	\$0FA0,\$0000,	;00004000
0000F860	13880000		FDB	\$1388,\$0000,	;00005000
0000F864	17700000		FDB	\$1770,\$0000,	;00006000
0000F868	1B580000		FDB	\$1B58,\$0000,	;00007000
0000F86C	1F400000		FDB	\$1F40,\$0000,	;00008000
0000F870	23280000		FDB	\$2328,\$0000,	;00009000
0000F874	00000000		FDB	\$0000,\$0000,	;00000000
0000F878	00640000		FDB	\$0064,\$0000,	;00000100
0000F87C	00C80000		FDB	\$00C8,\$0000,	;00000200
0000F880	012C0000		FDB	\$012C,\$0000,	;00000300
0000F884	01900000		FDB	\$0190,\$0000,	;00000400
0000F888	01F40000		FDB	\$01F4,\$0000,	;00000500
0000F88C	02580000		FDB	\$0258,\$0000,	;00000600
0000F890	02BC0000		FDB	\$02BC,\$0000,	;00000700

0000F894	03200000	FDB	\$0320,\$0000,	;00000800
0000F898	03840000	FDB	\$0384,\$0000,	;00000900
0000F89C	00000000	FDB	\$0000,\$0000,	;00000000
0000F8A0	000A0000	FDB	\$000A,\$0000,	;00000010
0000F8A4	00140000	FDB	\$0014,\$0000,	;00000020
0000F8A8	001E0000	FDB	\$001E,\$0000,	;00000030
0000F8AC	00280000	FDB	\$0028,\$0000,	;00000040
0000F8B0	00320000	FDB	\$0032,\$0000,	;00000050
0000F8B4	003C0000	FDB	\$003C,\$0000,	;00000060
0000F8B8	00460000	FDB	\$0046,\$0000,	;00000070
0000F8BC	00500000	FDB	\$0050,\$0000,	;00000080
0000F8C0	005A0000	FDB	\$005A,\$0000,	;00000090
0000F8C4	00000000	FDB	\$0000,\$0000,	;00000000
0000F8C8	00010000	FDB	\$0001,\$0000,	;00000001
0000F8CC	00020000	FDB	\$0002,\$0000,	;00000002
0000F8D0	00030000	FDB	\$0003,\$0000,	;00000003
0000F8D4	00040000	FDB	\$0004,\$0000,	;00000004
0000F8D8	00050000	FDB	\$0005,\$0000,	;00000005
0000F8DC	00060000	FDB	\$0006,\$0000,	;00000006
0000F8E0	00070000	FDB	\$0007,\$0000,	;00000007
0000F8E4	00080000	FDB	\$0008,\$0000,	;00000008
0000F8E8	00090000	FDB	\$0009,\$0000,	;00000009

0000F8EC MEND

0000F8EC

A.MONITOR



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... ..

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... ..

A.MONITOR MODULE

;this module provides a way to "look into" a 68XX target system from the "Serial Communicator" part of META. It 's almost entirely LOCAL since it may need to be included in any 68XX program.

;the routines CSEND and CGET are specialised to this particular 6303 system: they send and await Chars on the RS232 link with the BBC, vis through the DP-37 connector.

;MONITOR program assembled at current ORG

0000F8EC

LOCAL 100

\*\*\*\*\*

0000F8EC  
0000F8EC

OTEMP EQU \* make a copy of current ORG

00000100  
00000100

ORG \$0100 define constants/storage area in RAM

00000100

.DMPSTRT DS.W  
ACCA DS.B storage for accumulator A

00000102

00000102

ACCB DS.B storage for accumulator B

00000103

00000103

XREG DS.W storage for X index  
PC DS.W storage for Program Counter

00000104

00000106

00000106

CCR DS.B storage for Condition Code Register

00000108

00000108

CUR DS.W "cursor" position

00000109

0000010B

COUNT DS.B

0000010C

XTEMP DS.W temporary storage

0000010E

TEMPW DS.W temporary storage

00000110

STACK DS.W storage for stack pointer

00000110

0000F8EC

ORG OTEMP back to where we left off..

0000F8EC

\*\*\*\*\*

CSEND

;send the character in ACCA down RS232 port: preserve A, B,X

0000F8EC 37

PSHB

0000F8ED 3C

PSHX

0000F8EE D611

TXWAIT1

LDAB

TRCSR1

0000F8F0 C420

ANDB

#\$00100000

0000F8F2 27FA

BEQ

TXWAIT1

0000F8F4

IF

HD6303Y=1

0000F8F4

ELSE

OIM \$01000000,RMC

R

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64
65	66	67	68
69	70	71	72
73	74	75	76
77	78	79	80
81	82	83	84
85	86	87	88
89	90	91	92
93	94	95	96
97	98	99	100

\*\*\*\*\*

101	102	103	104
105	106	107	108
109	110	111	112
113	114	115	116
117	118	119	120
121	122	123	124
125	126	127	128
129	130	131	132
133	134	135	136
137	138	139	140
141	142	143	144
145	146	147	148
149	150	151	152
153	154	155	156
157	158	159	160
161	162	163	164
165	166	167	168
169	170	171	172
173	174	175	176
177	178	179	180
181	182	183	184
185	186	187	188
189	190	191	192
193	194	195	196
197	198	199	200

201	202	203	204
205	206	207	208
209	210	211	212
213	214	215	216
217	218	219	220
221	222	223	224
225	226	227	228
229	230	231	232
233	234	235	236
237	238	239	240
241	242	243	244
245	246	247	248
249	250	251	252
253	254	255	256
257	258	259	260
261	262	263	264
265	266	267	268
269	270	271	272
273	274	275	276
277	278	279	280
281	282	283	284
285	286	287	288
289	290	291	292
293	294	295	296
297	298	299	300

\*\*\*\*\*

```

0000F8F4                ENDIF
0000F8F4 9713           STAA      TDR
0000F8F6 D611           TXWAIT2   LDAB      TRCSR1
0000F8F8 C420           ANDB     #%0010G000
0000F8FA 27FA           BEQ      TXWAIT2
0000F8FC 38             PULX
0000F8FD 33             PULB
0000F8FE 39             RTS

```

```

CGET
;"get" a character routine; loops until character received.
Exit with character in Acc A, X preserved.

```

```

0000F8FF 3C             PSHX
0000F900 D611           RXWAIT1  LDAB      #%10000000
0000F904 27FA           BEQ      RXWAIT1
0000F906 9612           LDAA     RDR
0000F908 38             PULX
0000F909 39             RTS

```

\*\*\*\*\*

```

;RESET entry point
.MONITA

```

```

0000F90A 71EF11         AIM      %11101111,TRC
0000F90D                SR1
0000F90D BF0110         STS      STACK
0000F910 CEF91C         LDX      #SSTRING
0000F913 BDFB86         JSR      MSG
0000F916 BDFA24         JSR      REGDISP
0000F919 7EFA7E         JMP      PROMPT

```

\*\*\*\*\*

```

;start-up string

```

```

0000F91C 0C             SSTRING  EQUB      12
0000F91D 2D2D2D2D         EQUUS    "---- 6303 MO
0000F921 20363330         NITOR   ----"
0000F925 33204D4F
0000F929 4E49544F
0000F92D 52202D2D
0000F931 2D2D
0000F933 0D0A             EQUB      13,10
0000F935 28432920         EQUUS    "(C) JOHN HOL
0000F939 4A4F484E         DING 1986"
0000F93D 20484F4C
0000F941 44494E47
0000F945 20313938
0000F949 36
0000F94A 0D0A             EQUB      13,10
0000F94C 00             EQUB      0

```

```

;"help" message string

```

FY 2020 BUDGET REQUEST

POSITION TITLE

POSITION CLASSIFICATION

POSITION NUMBER

POSITION DESCRIPTION

POSITION DUTIES

POSITION QUALIFICATIONS

POSITION STATUS

POSITION LOCATION

POSITION TYPE

POSITION GRADE

POSITION SALARY

POSITION BENEFITS

POSITION TOTAL

POSITION TOTAL (BUDGET)

POSITION TOTAL (TOTAL)

POSITION TOTAL (NET)

POSITION TOTAL (GROSS)

POSITION TOTAL (NET)

```

0000F94D 0DOA      HSTRING  EQUB   13,10
0000F94F 3C52544E      EQUUS  "<RTN>  Next
0000F953 3E202020          Byte"
0000F957 4E657874
0000F95B 20427974
0000F95F 65
0000F960 0DOA      EQUB   13,10
0000F962 2D202020      EQUUS  "-      Back
0000F966 20202020          one byte"
0000F96A 4261636B
0000F96E 206F6E65
0000F972 20627974
0000F976 65
0000F977 0DOA      EQUB   13,10
0000F979 3C58583E      EQUUS  "<XX>  Stor
0000F97D 20202020          e XX into cur
0000F981 53746F72          rent pos."
0000F985 65205858
0000F989 20596E74
0000F98D 6F206375
0000F991 7272656E
0000F995 7420706F
0000F999 732E
0000F99B 0DOA      EQUB   13,10
0000F99D 52202020      EQUUS  "R      Redi
0000F9A1 20202020          splay Regs"
0000F9A5 52656469
0000F9A9 73706C61
0000F9AD 79205265
0000F9B1 6773
0000F9B3 0DOA      EQUB   13,10
0000F9B5 473C5858      EQUUS  "G<XXXX> Move
0000F9B9 58583E20          pos to XXXX"
0000F9BD 4D6F7665
0000F9C1 20706F73
0000F9C5 20746F20
0000F9C9 58585858
0000F9CD 0DOA      EQUB   13,10
0000F9CF 58202020      EQUUS  "X      Exec
0000F9D3 20202020          ute from curr
0000F9D7 45786563          ent pos"
0000F9DB 75746520
0000F9DF 66726F6D
0000F9E3 20637572
0000F9E7 72656E74
0000F9EB 20706F73
0000F9EF 0DOA00      EQUB   13,10,0

;register headings

0000F9F2 0DOA      RSTRING EQUB   13,10
0000F9F4 20504320      EQUUS  " PC  ACCA AC
0000F9F8 20414343          GB XREG CCR
0000F9FC 41204143          SP"
0000FA00 43422058
0000FA04 52454720
0000FA08 43435220

```

REPORT OF THE CHIEF OF STAFF ON THE INVESTIGATION

ON THE SUBJECT OF THE... (text is faint)

... (text is faint)

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... (text is faint)

```
0000FA0C 205350
0000FA0F 0D0A00          EQUB      13,10,0
```

;command keys list

```
0000FA12 0D          COMLIST  EQUB      13
0000FA13 47582D52     EQUB      "GX-RH"
0000FA17 48
```

;jump table for each of the commands above

```
0000FA18 FB29     COMVEC  FDB      INPC      ;move on one byte
0000FA1A FB52     FDB      GOTO      ;"GOTO" a new address
0000FA1C FB43     FDB      EXEC      ;"EXECUTE" from current
0000FA1E          FDB      address
0000FA1E FB33     FDB      DECPC     ;move back a byte
0000FA20 FB3D     FDB      REPRG    ;repeat register values
0000FA22          FDB      from last SWI
0000FA22 FB20     FDB      HELP     ;print up the "HELP" lis
0000FA24          FDB      t
```

\*\*\*\*\*

;display register values as recorded on entry into mon  
itor

```
0000FA24 CEF9F2     REGDISP LDX      #RSTRING
0000FA27 BDFB86     JSR      MSG
0000FA2A B60106     LDAA     PC
0000FA2D BDFBAE     JSR      HEX
0000FA30 B60107     LDAA     PC+1
0000FA33 BDFBAE     JSR      HEX
0000FA36 BDFBA8     JSR      SPACE2
0000FA39 B60102     LDAA     ACCA
0000FA3C BDFBAE     JSR      HEX
0000FA3F BDFBA5     JSR      SPACE3
0000FA42 B60103     LDAA     ACCB
0000FA45 BDFBAE     JSR      HEX
0000FA48 BDFBA8     JSR      SPACE2
0000FA4B B60104     LDAA     XREG
0000FA4E BDFBAE     JSR      HEX
0000FA51 B60105     LDAA     XREG+1
0000FA54 BDFBAE     JSR      HEX
0000FA57 BDFBA8     JSR      SPACE2
0000FA5A B60108     LDAA     CCR
0000FA5D BDFBAE     JSR      HEX
0000FA60 BDFBA0     JSR      SPACE1
0000FA63 B60110     LDAA     STACK
0000FA66 BDFBAE     JSR      HEX
0000FA69 B60111     LDAA     STACK+1
0000FA6C BDFBAE     JSR      HEX
0000FA6F 860D     LDAA     #13
0000FA71 BDF8EC     JSR      CSEND
0000FA74 860A     LDAA     #10
0000FA76 7EF8EC     JMP      CSEND
0000FA79 860A     LDA      #10
0000FA7B 7EF8EC     JMP      CSEND
```



Statement of Assets and Liabilities

Assets	Liabilities	Equity
Real Estate	Accounts Payable	Capital
Loans	Deposits	Reserves
Investments	Notes	Surplus
Other Assets	Other Liabilities	
Total	Total	Total

Continued on next page

See page 10 for details

;main prompt routine

```

0000FA7E 860D      PROMPT   LDAA    #13
0000FA80 BDF8EC      JSR     CSEND
0000FA83 860A      LDAA    #10
0000FA85 BDF8EC      JSR     CSEND
0000FA88 B60109      PROMPT1 LDAA    CUR
0000FA8B BDFBAE      JSR     HEX
0000FA8E B6010A      LDAA    CUR+1
0000FA91 BDFBAE      JSR     HEX
0000FA94 BDFBA0      JSR     SPACE1
0000FA97 FE0109      LDX     CUR
0000FA9A A600      LDAA    O,X
0000FA9C 847F      ANDA    #%01111111
0000FA9E 8120      CMPA    #' '
0000FAA0 2F04      BLE     DOT
0000FAA2 817F      CMPA    #%01111111
0000FAA4 2602      BNE     DOT1
0000FAA6 862E      DOT     LDAA    #'.'
0000FAA8 BDF8EC      DOT1   JSR     CSEND
0000FAAB BDFBA0      JSR     SPACE1
0000FAAE FE0109      LDX     CUR
0000FAB1 A600      LDAA    O,X
0000FAB3 BDFBAE      JSR     HEX
0000FAB6 863A      LDAA    #'.'
0000FAB8 BDF8EC      JSR     CSEND
0000FABB BDF8FF      IGNORE JSR     CGET      strip out line feeds
0000FABE 810A      CMPA    # $0A
0000FAC0 27F9      BEQ     IGNORE
0000FAC2 CEFA12      LDX     #COMLIST
0000FAC5 C600      LDAB    #0
0000FAC7 A100      PRO     CMPA    O,X
0000FAC9 272E      BEQ     PRI
0000FACB 08      INX
0000FACC 5C      INCB
0000FACD 5C      INCB
0000FACE C10C      CMPB    #12
0000FAD0 26F5      BNE     PRO
0000FAD2 8130      CMPA    #'0'
0000FAD4 2D0C      BLT     NOTHEX
0000FAD6 8146      CMPA    #'F'
0000FAD8 2E08      BGT     NOTHEX
0000FADA 8139      CMPA    #'9'
0000FADC 2F07      BLE     ISHEX
0000FADE 8141      CMPA    #'A'
0000FAE0 2C03      BGE     ISHEX
0000FAE2 7EFA7E      NOTHEX JMP     PROMPT
0000FAE5 CE0000      ISHEX  LDX     #0
0000FAE8 FF010E      STX     TEMPW
0000FAEB BDFBCE      JSR     GH1A
0000FAEE B6010F      LDAA    TEMPW+1
0000FAF1 FE0109      LDX     CUR
0000FAF4 A700      STAA   O,X
0000FAF6 7EFB29      JMP     INCPC

0000FAF9 CEFA18      PRI     LDX     #COMVEC
0000FAFC FF010E      STX     TEMPW

```

```

0000FAFF 0C          CLC
0000FB00 F9010F     ADCB      TEMPW+1
0000FB03 F7010F     STAB      TEMPW+1
0000FB06 F6010E     LDAB      TEMPW
0000FB09 C900       ADCB      #0
0000FB0B F7010E     STAB      TEMPW
0000FB0E FE010E     LDX       TEMPW
0000FB11 A600       LDAA      0,X
0000FB13 B7010C     STAA      XTEMP
0000FB16 A601       LDAA      1,X
0000FB18 B7010D     STAA      XTEMP+1
0000FB1B FE010C     LDX       XTEMP
0000FB1E 6E00       JMP       0,X

```

;display help list

```

0000FB20 CEF94D     HELP     LDX      #HSTRING
0000FB23 BDFB86     JSR      MSG
0000FB26 7EFA7E     JMP      PROMPT

```

;move on a byte

```

0000FB29 FE0109     INPC     LDX      CUR
0000FB2C 08         INX
0000FB2D FF0109     STX      CUR
0000FB30 7EFA88     JMP      PROMPT1

```

;move back a byte

```

0000FB33 FE0109     DECPC    LDX      CUR
0000FB36 09         DEX
0000FB37 FF0109     STX      CUR
0000FB3A 7EFA7E     JMP      PROMPT

```

;repeat list of registers

```

0000FB3D BDF824     REPRG    JSR      REGDISP
0000FB40 7EFA7E     JMP      PROMPT

```

;execute from current address

```

0000FB43 FE0109     EXEC     LDX      CUR
0000FB46 721011     OIM      %00010000,TRC ;RECEIVE INT NOT RE ENAB
0000FB49          SR1      LED
0000FB49 0E         CLI
0000FB4A AD00       JSR      0,X
0000FB4C 71EF11     AIM      %11101111,TRC
0000FB4F          SR1
0000FB4F 7EFB61     JMP      MONITB

```

;GOTO new address

```

0000FB52 BDFB86     GOTO     JSR      GETHEX
0000FB55 FE010E     LDX      TEMPW
0000FB58 FF0109     STX      CUR
0000FB5B 7EFA7E     JMP      PROMPT

```

\*\*\*\*\*

;SWI entry point

.SWI

0000FB5E	71EF11		AIM	%11101111,TRC
0000FB61				SR1
0000FB61	B70102	.MONITB	STAA	ACCA
0000FB64	32		PULA	
0000FB65	B70108		STAA	CCR
0000FB68	F70103		STAB	ACCB
0000FB6B	FF0104		STX	XREG
0000FB6E	32		PULA	
0000FB6F	32		PULA	
0000FB70	32		PULA	
0000FB71	32		PULA	
0000FB72	32		PULA	
0000FB73	B70106		STAA	PC
0000FB76	B70109		STAA	CUR
0000FB79	32		PULA	
0000FB7A	B70107		STAA	PC+1
0000FB7D	B7010A		STAA	CUR+1
0000FB80	BF0110		STS	STACK
0000FB83	7EF90A		JMP	
0000FBA0	8620	SPACE1	LDAA	#32
0000FBA2	7EF8EC		JMP	CSEND
0000FBA5	BDFBA0	SPACE3	JSR	SPACE1
0000FBA8	BDFBA0	SPACE2	JSR	SPACE1
0000FBAB	7EFBA0		JMP	SPACE1

\*\*\*\*\*

;display binary value in Acc A as two hex ASCII digits

```

0000FBAE 36      HEX      PSHA
0000FBAF 47      ASRA
0000FBB0 47      ASRA
0000FBB1 47      ASRA
0000FBB2 47      ASRA
0000FBB3 BDFBB7   JSR      HEX1
0000FBB6 32      PULA
0000FBB7 840F   HEX1    ANDA    #%00001111
0000FBB9 8A30   ORAA    #'0'
0000FBBB 813A   CMPA    #' ':'
0000FBBD 2D03   BLT     HEX2
0000FBBF 0C      CLC
0000FBC0 8907   ADCA    #7
0000FBC2 7EF8EC  HEX2    JMP     CSEND

```

\*\*\*\*\*

;await an incoming hex number terminated by CR (\$D). Ma  
y be any number of digits, but only last four returned i  
n the 2-byte result store "TEMPW".

```

0000FBC5 CE0000  GETHEX  LDX     #0
0000FBC8 FF010E  STX     TEMPW
0000FBCB BDF8FF   GH1     JSR     CGET
0000FBCE 810D   GH1A    CMPA    #13
0000FBD0 2604   BNE     GH2
0000FBD2 BDF8FF   JSR     CGET
0000FBD5 39      RTS
0000FBD6 8130   GH2     CMPA    #'0'
0000FBD8 2D0C   BLT     GH3
0000FBDA 8146   CMPA    #'F'
0000FBDC 2E08   BGT     GH3
0000FBDE 8141   CMPA    #'A'
0000FBE0 2C0C   BGE     GH4
0000FBE2 8139   CMPA    #'9'
0000FBE4 2F0B   BLE     GH5
0000FBE6 8607   GH3     LDAA    #7
0000FBE8 BDF8EC   JSR     CSEND
0000FBEB 7EF8EC   JMP     GH1
0000FBEE 0D      GH4     SEC
0000BEF 8206   SBCA    #'A'-'0'+11]
0000FBF1 0D      GH5     SEC
0000FBF2 8230   SBCA    #'0'
0000FBF4 4C      INCA
0000FBF5 48      ASLA
0000FBF6 48      ASLA
0000FBF7 48      ASLA
0000FBF8 48      ASLA

0000FBF9 0C      CLC
0000FBFA 48      ASLA
0000FBFB 79010F  ROL     TEMPW+1
0000FBFE 79010E  ROL     TEMPW
0000FC01 0C      CLC

```

0000FC02 48	ASLA	
0000FC03 79010F	ROL	TEMPW+1
0000FC06 79010E	ROL	TEMPW
0000FC09 0C	CLC	
0000FC0A 48	ASLA	
0000FC0B 79010F	ROL	TEMPW+1
0000FC0E 79010E	ROL	TEMPW
0000FC11 0C	CLC	
0000FC12 48	ASLA	
0000FC13 79010F	ROL	TEMPW+1
0000FC16 79010E	ROL	TEMPW
0000FC19 7EFBCB	JMP	GH1

\*\*\*\*\*

0000FC1C MEND

TO : DIRECTOR, FBI (100-441100)  
FROM : SAC, NEW YORK (100-100000)  
SUBJECT: [REDACTED]

RE: [REDACTED]

DATE: [REDACTED]

CLASSIFICATION: [REDACTED]

REASON FOR EXTENSION: [REDACTED]

DATE OF REVIEW: [REDACTED]

REVIEWER: [REDACTED]

APPROVAL: [REDACTED]

DATE OF APPROVAL: [REDACTED]

REASON FOR DENIAL: [REDACTED]

DATE OF DENIAL: [REDACTED]

REVIEWER: [REDACTED]

APPROVAL: [REDACTED]

DATE OF APPROVAL: [REDACTED]

000GFC1C SKIP \$FFEA-\*, \$FF fill with FF for eprom p  
0000FC1C programmer

\*\*\*\*\*

0000FFEA ORG \$FFEA interrupt vector label i  
0000FFEA nitialization

0000FFEA A.INTVECT initialize processor reg  
0000FFEA isters



A.INTVECT MODULE

;module to write interrupt vectoring locations  
\*\*\*\*\*

0000FFEA E983	FDB	IRQ2	interrupt request 2
0000FFEC E983	FDB	CMI	timer 2 counter match
0000FFEE E000	FDB	TRAP	undefined opcode/illegal address
0000FFF0 ED22	FDB	SIO	serial I/O (RDRF+ORFE+TD RE)
0000FFF2 E985	FDB	TOI	timer 1 overflow
0000FFF4 E983	FDB	OCI	timer 1 output compare 1 ,2
0000FFF6 E983	FDB	ICI	timer 1 input capture
0000FFF8 E983	FDB	IRQ1	interrupt request 1
0000FFFA FB5E	FDB	SWI	software interrupt
0000FFFC E96D	FDB	NMI	non-maskable interrupt
0000FFFE E000	FDB	RES	reset program start vect or
00010000			

\*\*\*\*\*

00010000 MEND

00010000

\*\*\*\*\*

END

The first part of the document is a list of names and titles, including 'The Hon. Mr. Justice G. D. Young, Chief Justice of the Supreme Court of the Province of Ontario' and 'The Hon. Mr. Justice G. D. Young, Chief Justice of the Supreme Court of the Province of Ontario'.

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Symbol Table:

ADST.....GBL .....31	ADRD.....GBL .....30	ADLOAD...GBL .....37
ACTYPE...GBL .....47	ACMODE...GBL .....6A	ADPSU...GBL .....0
ADLINA...GBL .....1	ADLEQ...GBL .....2	ADWAIT2..GBL ....E620
ADWAIT3..GBL ....E668	ADWAIT4..GBL ....E6B0	ADSTRT...GBL ....E9B8
ADWAIT...GBL ....E9BE	ADMISS...GBL ....E9C4	ADWAIT1..GBL ....ECFA
ASCDN1...GBL ....F0DE	ASCDN2...GBL ....F0FA	ACCA.....100 .....102
ACCB.....100 .....103	BYTCTR...GBL .....E5	BCDOVF...GBL .....C3
BATTLOW..GBL ....E9AB	BIGDAT1..GBL ....EBO7	BIGDAT2..GBL ....EBC5
BADMESS..GBL ....EF7C	BNKDONE..GBL ....EFF3	BCDTAB1..GBL ....F15D
BCDTAB2..GBL ....F17D	BCDTAB3..GBL ....F19D	BCDTAB4..GBL ....F1BD
CODE.....GBL .....48	CHDSTRT..GBL .....49	CUMBIN...GBL .....4C
CUMBCD...GBL .....4E	CODUSE...GBL .....C4	CALFLG...GBL .....C7
CUMDOSE..GBL .....CC	CUMTIME..GBL .....CF	CALOFF...GBL .....D5
CALDNF...GBL .....DA	CAIVAL...GBL .....DC	CALCNT...GBL .....E0
CIRRUS...GBL .....1	CAL.....GBL .....11	CUMLEQ...GBL .....42
CODE1...GBL .....18	CODE2...GBL .....28	CODE3...GBL .....48
CODE4...GBL .....88	CALPH...GBL ....E248	CALMOD...GBL ....E253
CALOK...GBL ....E2ED	CALEND...GBL ....E30E	CONVCMP..GBL ....E3D2
CHDB1...GBL ....E464	CHDBDN...GBL ....E467	CMI.....GBL ....E983
CUMCNEND..GBL ....EB2A	CCR.....100 .....108	CUR.....100 .....109
COUNT...100 .....10B	CSEND...100 ....F8EC	CGET...100 ....F8FF
COMLIST..100 ....FA12	COMVEC...100 ....FA18	DATA.....GBL .....50
DATAcnt..GBL .....52	DBLANKF..GBL .....6B	DSCRICH..GBL .....74
DATADIF..GBL .....CA	DOCAL...GBL ....E303	DOPAUSE..GBL ....E3B8
DOWRT...GBL ....E423	DOLAST...GBL ....E445	DOLAST1..GBL ....E45B
DCALWRT..GBL ....E547	DONOUP...GBL ....E79D	DOMAXUP..GBL ....E7AF
DOCUMUP..GBL ....E84A	DOLEQUP..GBL ....E8E5	DOLCD...GBL ....E8E9
DOCONV...GBL ....E9B2	DTIMCMP..GBL ....EB96	DORX.....GBL ....ED2B
DOESC...GBL ....ED37	DONUM...GBL ....ED82	DODIGS...GBL ....ED94
DORTI...GBL ....EE95	DOMESS...GBL ....EEB0	DOTX.....GBL ....EFA3
DOTX1...GBL ....EFAC	DO16BIT..GBL ....EFE3	DOBNKO...GBL ....FO46
DATADN...GBL ....F072	DOHDR...GBL ....F079	DMPSTRT..GBL .....100
DOT...100 ....FAA6	DOT1...100 ....FAA8	DECPC...100 ....FB33
EPROM...GBL .....0	ERRFLAG..GBL .....55	ERRSTAT..GBL .....D7
ERRHOLD..GBL .....D8	EIGHTH...GBL .....14	ENDPG...GBL ....EE95
ESCSTR...GBL ....F71D	ERMESS...GBL ....F797	EXEC...100 ....FB43
FRC.....GBL .....9	FULL.....GBL ....EC51	FIDLTST..GBL ....ECFA
FIDDLE...GBL ....ED14	GOTO...100 ....FB52	GETHEX...100 ....FBC5
GH1.....100 ....FBCE	GH1A...100 ....FBCE	GH2.....100 ....FBD6
GH3.....100 ....FBE6	GH4.....100 ....FBEE	GH5.....100 ....FBF1
HDWCTR...GBL .....56	HLPTR...GBL .....57	HDRFLD...GBL .....6C
HI32VL1..GBL .....76	HI32VL2..GBL .....7A	HDRSTRT..GBL .....A6
HDRCTR...GBL .....A8	HSTRIPG..GBL .....B4	HD6303Y..GBL .....1
HIMIDST.. 4 ....E14B	HIST..... 4 ....E168	HIMIDST.. 11 ....E717
HIST..... 11 ....E734	HIMIDST.. 12 ....E7EE	HIST..... 12 ....E80B
HIMIDST.. 13 ....E889	HIST..... 13 ....E8A6	HIMIDST.. 16 ....EA78
HIST..... 16 ....EA95	HIMIDST.. 17 ....ECA4	HIST..... 17 ....ECC1
HDRBNK1..GBL ....F02A	HLOOK...GBL ....F1CD	HEXTBL...GBL ....F7AC
HSTRING..100 ....F94D	HELP...100 ....FB20	HEX...100 ....FBAE
HEX1...100 ....FBB7	HEX2...100 ....FBC2	ICR.....GBL .....D
INTRPRT..GBL ....E315	IRQ2...GBL ....E983	ICI.....GBL ....E983
IRQ1...GBL ....E983	INTRES...GBL ....E9EC	INTOF...GBL ....F14D
IDMESS...GBL ....F74D	ITMESS...GBL ....F77A	IGNORE...100 ....FABB
ISHEX...100 ....FAE5	INCPG...100 ....FB29	KEYVAL...GBL .....41
KEYCNT...GBL .....42	KEYTEMP..GBL .....43	KENCNT...GBL .....BE

1. The first part of the document discusses the importance of maintaining accurate records of all transactions. It emphasizes that proper record-keeping is essential for the integrity of the financial system and for the ability to detect and prevent fraud. The text outlines the various types of records that should be maintained, including receipts, invoices, and bank statements, and provides guidance on how to organize and store these records effectively.

2. The second part of the document focuses on the role of internal controls in ensuring the accuracy and reliability of financial information. It describes the various types of internal controls, such as segregation of duties, authorization requirements, and independent verification, and explains how these controls can be used to identify and prevent errors and fraud. The text also discusses the importance of regularly reviewing and updating internal controls to reflect changes in the organization's operations and the external environment.

3. The third part of the document discusses the importance of transparency and accountability in financial reporting. It emphasizes that financial statements should be prepared and presented in a clear, concise, and understandable manner, and that they should be subject to independent audit and review. The text also discusses the importance of disclosing all material information that could affect the financial statements, and provides guidance on how to prepare and present financial statements in accordance with applicable accounting standards.

4. The fourth part of the document discusses the importance of maintaining accurate records of all transactions. It emphasizes that proper record-keeping is essential for the integrity of the financial system and for the ability to detect and prevent fraud. The text outlines the various types of records that should be maintained, including receipts, invoices, and bank statements, and provides guidance on how to organize and store these records effectively.

KENFLG...GBL	.....C5	KEYLOOP..	3 ....E020	KEYTST...	3 ....E04E
KEYCOMP..	3 ....E05C	KEYOK....	3 ....E064	KEYRET...	3 ....E069
KEYLOOP..	6 ....E1F4	KEYTST...	6 ....E222	KEYCOMP..	6 ....E230
KEYOK....	6 ....E238	KEYRET...	6 ....E23D	LCDIG....GBL	.....32
LEDS.....GBL	.....36	LCDWORD..GBL	.....44	LEDSREG..GBL	.....59
LCDMAXUP..GBL	.....6D	LDCUMUP..GBL	.....6E	LCDLEQUP..GBL	.....6F
LCDNOUP..GBL	.....71	LEDSONF..GBL	.....72	LO32VL1..GBL	.....78
LO32VL2..GBL	.....7C	LINCTR...GBL	.....B6	LOGTIME..GBL	.....D2
LINASTR...GBL	.....DB	LEDENABL..GBL	.....21	LEQNO....GBL	.....12
LOSTR....	4 ....E127	LOMIDST..	4 ....E130	LINPOS1..GBL	....E633
LINPOS2..GBL	....E67B	LINPOS3..GBL	....E6C3	LOSTR....	11 ....E6F3
LOMIDST..	11 ....E6FC	LOSTR....	12 ....E7CA	LOMIDST..	12 ....E7D3
LOSTR....	13 ....E865	LOMIDST..	13 ....E86E	LOGAIN...GBL	....EA2B
LOSTR....	16 ....EA54	LOMIDST..	16 ....EA5D	LOSTR....	17 ....EC80
LOMIDST..	17 ....EC89	LINPOS...GBL	....ED0E	LOGTAB1..GBL	....F1ED
LOGTAB2..GBL	....F5ED	MAXBIN...GBL	.....5A	MAXBCD...GBL	.....5C
MONFLG...GBL	.....CO	MEMLBIN..GBL	.....E1	MEMLBCD..GBL	.....E3
MAXLEQ...GBL	.....82	MLOOP...GBL	....E1BF	MAXOK...GBL	....EAD4
MESSOK0..GBL	....EC2	MESSOK1..GBL	....EF00	MESSOK2..GBL	....EF34
MESSOK3..GBL	....EF68	MOREMES..GBL	....EFE2	MONITA...GBL	....F90A
MONITB...GBL	....FB61	MSG.....	100 ....FB86	MESSG...100	....FB86
MSG3.....	100 ....FB92	MSG1.....	100 ....FB9F	NOBIN...GBL	.....5E
NOTYPE...GBL	.....70	NUMMODE..GBL	.....7E	NOBCD...GBL	.....C1
NRAMOK...GBL	....E0C2	NMON....GBL	....E1CB	NKEYEN...GBL	....E1D8
NOKEY...GBL	....E240	NCALCLR..GBL	....E270	N94DB...GBL	....E27B
N104DB...GBL	....E286	N117DB...GBL	....E291	N124DB...GBL	....E29A
NUP1DB...GBL	....E2B3	NDN1DB...GBL	....E2C2	NUPPT1DB..GBL	....E2CD
NCALMOD..GBL	....E30E	NLEDKEY..GBL	....E32B	NSHRTLQ..GBL	....E347
NMAXLEQ..GBL	....E363	NCUMLEQ..GBL	....E37F	NLEQNO...GBL	....E3A9
NXEMPTY..GBL	....E3EC	NFULL1...GBL	....E3F7	NHDOVF1...GBL	....E475
NHDOVF2..GBL	....E492	NHDOVF3...GBL	....E4A8	NPGCHNG..GBL	....E4B5
NNULL...GBL	....E4CE	NHDOVF4...GBL	....E4EB	NHDOVF5...GBL	....E501
NHDOVF6..GBL	....E514	NHDOVF7...GBL	....E520	N18.....GBL	....E539
N1.....GBL	....E543	NHDOVF8...GBL	....E553	NEWHDST..GBL	....E561
NLASTEND..GBL	....E578	NPAUSE...GBL	....E58F	NRSTCUM..GBL	....E5A7
NRELMAX..GBL	....E5B4	NCODE...GBL	....E5C0	NRUNKEYS..GBL	....E5C3
NCAL...GBL	....E5EC	NFULL2...GBL	....E5F4	NEIGHTH..GBL	....E63A
NONESEC..GBL	....E682	NTENSEC..GBL	....E6C7	NSTRT...GBL	....E6C7
NINTRPRT..GBL	....E6CD	NLEDS...GBL	....E6D4	NOUP...GBL	....E6DE
NPGCORR..GBL	....E782	NONOUP...GBL	....E7A7	NZMAX...GBL	....E7BC
NMAXUP...GBL	....E842	NZERCUM..GBL	....E857	NCUMUP...GBL	....E8DD
NLEQUP...GBL	....E8E9	NOVLERR..	14 ....E903	NCALERR..	14 ....E90E
NBATL0...14	....E919	NERRDET..	14 ....E919	NERDISP..	14 ....E935
NDELANK...14	....E947	NLEDZER..	14 ....E955	NUPDATE..	14 ....E969
NMI.....GBL	....E96D	NOCHNGE..GBL	....E9D9	NOLOAD...GBL	....E9E9
NDAOVF...GBL	....EA08	NCCOMP...GBL	....EA12	NRUNING..GBL	....EA41
NRUNCLR..GBL	....EAE3	NXTROT1..GBL	....EB3F	NTHREEB..GBL	....EB67
NXTROT2..GBL	....EB6F	NTOGL...GBL	....EBF4	NDTAOVF..GBL	....EC3F
NFULL...GBL	....EC63	NRAMOVF..GBL	....EC6D	NSTORE...GBL	....ECFA
NFIDDLE..GBL	....ED1C	NOTESC...GBL	....ED5E	NCTRLS...GBL	....ED6C
NCTRLQ...GBL	....ED7A	NXTDIG1..GBL	....EDC2	NO32CR1..GBL	....EDEE
NXTDIG2..GBL	....EDFB	NO32CR2..GBL	....EE27	NO32CR3..GBL	....EE41
NPGJMP...GBL	....EE57	NOPAGE...GBL	....EE61	NOENDP1..GBL	....EE70
NOENDP2..GBL	....EE86	NOENDP3..GBL	....EE92	NOTNUM...GBL	....EE9E
NOTPR...GBL	....EEF3	NOTID...GBL	....EF27	NOTID1...GBL	....EF2D
NOTIT...GBL	....EF5B	NOTLG...GBL	....EF6D	NOPEN...GBL	....EFDC
NOBANK...GBL	....EFF0	NOPGE...GBL	....EFFC	NOT6...GBL	....F020
NOT16...GBL	....F036	NOTHDR1..GBL	....F03E	NOFLIP...GBL	....F062
NXTHDR...GBL	....F083	NXTHDR1..GBL	....F09F	NXTLIN...GBL	....FOBB

1. The first part of the document discusses the importance of maintaining accurate records of all transactions. It emphasizes that proper record-keeping is essential for the integrity of the financial system and for the ability to detect and prevent fraud. The text notes that without reliable records, it would be difficult to track the flow of funds and identify any irregularities.

2. The second part of the document outlines the specific procedures for recording transactions. It details the steps involved in entering data into the system, including the use of standardized codes and the requirement for double-checking entries. The text also discusses the importance of regular audits and reconciliations to ensure that the records are up-to-date and accurate. It mentions that any discrepancies should be investigated immediately and reported to the appropriate authorities.

3. The third part of the document addresses the issue of data security and access control. It stresses that sensitive financial information must be protected from unauthorized access and disclosure. The text describes the implementation of strict access policies and the use of secure communication channels. It also highlights the need for regular security updates and the training of staff on best practices for handling sensitive data. The document concludes by stating that a strong security posture is critical for maintaining the trust of stakeholders and the overall stability of the organization.

NXTBYT...GBL	....FOBE	NOTASC1..GBL	....FODC	NOTASC2..GBL	....FOF8
NOTHEX...100	....FAE2	OCR1.....GBL	.....B	OCR2.....GBL	.....19
OFFSET4..GBL	.....B0	OFFSET3..GBL	.....B1	OFFSET2..GBL	.....B2
OFFSET1..GBL	.....B3	ONESEC...GBL	.....24	OLDCAL...GBL	....E0B7
OTHRPG...GBL	....E40B	OCI.....GBL	....E983	ONLY1...:GBL	....EB96
OTEMP...:100	....F8EC	PORT2DDR.GBL	.....1	PORT2...:GBL	.....3
PORT5...:GBL	.....15	PORT6DDR.GBL	.....16	PORT6...:GBL	.....17
P2SAVE...GBL	.....7F	PENDFLG..GBL	.....B7	P2BACK...GBL	.....D9
PARITY...GBL	.....1	PAUSE...:GBL	.....84	PGCORR...GBL	....E76D
PAGEUP...GBL	....E791	PHASE2...GBL	....E998	PGDONE...GBL	....EFFF
PC.....:100	....106	PROMPT...100	....FA7E	PROMPT1...100	....FA88
PRO.....:100	....FAC7	PR1.....:100	....FAF9	RAMPOR5..GBL	.....14
RMCR.....GBL	.....10	RDR.....:GBL	.....12	RAMPNTR..GBL	.....60
RAMPNTB..GBL	.....62	RAMPSTR..GBL	.....63	RAMPBSTR..GBL	.....65
RUNBIN...:GBL	.....66	RAMFULL..GBL	.....73	RXBUF...:GBL	.....80
RXPTR...:GBL	.....A9	RAMFLAG..GBL	.....AE	ROTCNT...GBL	.....BF
RUNBCD...GBL	.....C8	RAMSTRT..GBL	....140	RAMEND...GBL	....E000
RAMENDB..GBL	.....1	RESETCUM.GBL	.....41	RELMAX...GBL	.....81
RES.....:GBL	....E000	RAMOK...:GBL	....E00E	RAMCLR...GBL	....E0C9
ROW3OK...GBL	....E1E7	RUNKEYS..GBL	....E3B1	RUNTST...GBL	....EA33
RUNNING..GBL	....EACE	RUNCONV..GBL	....EBA1	RCONVEND.GBL	....EBE8
RAMDUMP..GBL	....F0B0	ROTOFF...GBL	....F6ED	RXWAIT1...100	....F900
RSTRING..:100	....F9F2	REGDISP..100	....FA24	REPREG...:100	....FB3D
SCRATCH..GBL	.....AF	STAKPTR..GBL	.....DE	SCALQF...GBL	.....B1
SHORTLEQ.GBL	.....22	START...:GBL	....E1AF	SETP2...:GBL	....E575
SELF1...:GBL	....E97B	SELF2...:GBL	....E97D	SMDATA1..GBL	....EAF4
SMCUM...:GBL	....EB13	SMDATA2..GBL	....EBB2	SMRUN...:GBL	....EBD1
STORE...:GBL	....EBFC	SIO.....:GBL	....ED22	STACK...:100	....110
SSTRING..100	....F91C	SWI.....:GBL	....FB5E	SPACE1...:100	....FBA0
SPACE3...100	....FBA5	SPACE2...100	....FBA8	TCSR1...:GBL	.....8
TCSR2...:GBL	.....F	T2CNT...:GBL	.....1D	TCONR...:GBL	.....1C
TCSR3...:GBL	.....1E	TRCSR1...GBL	.....11	TDR.....:GBL	.....13
TRCSR2...GBL	.....1E	TLOOPCNT.GBL	.....40	TFLAG...:GBL	.....46
TOTALCNT.GBL	.....69	TXPTR...:GBL	.....A0	TXEND...:GBL	.....A2
TXFLAG...GBL	.....A4	TXHFLG...GBL	.....A5	TXBYTE...GBL	.....AB
TXBANK...GBL	.....AC	TXENDPG..GBL	.....AD	TXPPEND..GBL	.....B8
TXBPEND.GBL	.....BA	TXEPEND..GBL	.....BB	TXEBPEND.GBL	.....BD
TOGLCNT..GBL	....C6	TENSEC...GBL	.....44	TRAP...:GBL	....E000
TRYREAD..GBL	....E1DF	TSTOFF...GBL	....E2D8	TOGL1...:GBL	....E417
TOI.....:GBL	....E985	TDEL1...:GBL	....E9D4	TSTAUTO..GBL	....EA1C
TENSCMP..GBL	....EC11	TCOMPDN..GBL	....EC18	TRWAIT...GBL	....EFAE
TESTPG...GBL	....F06B	TEST...:GBL	....F0B9	TXWT1...:GBL	....FOC0
TXWT2...:GBL	....F0E0	TXWT3...:GBL	....F0FD	TXWT4...:GBL	....F114
TXWT5...:GBL	....F124	TXWT6...:GBL	....F13B	TEMPW...:100	....10E
TXWAIT1...100	....F8EE	TXWAIT2...100	....F8F6	WELCOME..GBL	....F738
XREG...:100	....104	XTEMP...:100	....10C	ZERMAX...GBL	....E7B8
ZERCUM...:GBL	....E853				

Labels used: 481





MODULE LIST

- 1 A.LABELS
- 2 R:RESET
- 3 A.TEST
- 4 A.MONITOR
- 5 A.INTVECT

00000001

LIST ON

;LIST ON ENABLES LISTING AND MAY BE USED BEFORE ONE MODULE TO PRINT THAT ONE ONLY. USE LIST OFF TO DISABLE AFTER THE MODULE(S) TO BE LISTED.

;MODULE ON SENDS ANY PRINT OUTPUT TO PRINTER INSTEAD OF THE SCREEN

00000000

HEADER "CRL 2.36 SHORT Leq DATA ACQUISITION UNIT, 6303Y PROCESSOR"

00000000

00000000

00000000

00000000

00000000

SYMTAB OFF symbol table enabled

00000000

EPROM = 0

00000000

IF EPROM=1  
 OBSEND 1,0,0,"236OBJ send object code to disc"

OBFORM 1

no load or exec address specified

; OBSEND 6,2764,128,0,0

; OBSEND 4,7

00000000

ELSE

00000006

OBSEND 6,2764,128,0,

00000006

0

00000001

OBFORM 1 straight binary (1,0,0,"236OBJ")

00000001

00000000

ENDIF

;FOR EPROM, STORE OBJECT CODE ON DISK USING OBSEND 1,0,0,"236OBJ"/OBFORM 2 THEN WHEN THE EPROMER SOFTWARE PROMPTS FOR FILENAME, GIVE "236OBJ". FOR PORTAL USE OBSEND 6,2764,128,0,0 AND OBSEND 1.

\*\*\*\*\*

0000E000

ORG \$E000 origin for program code

00000001

LIST ON

0000E000

R.RESET reset/restart module



```
R.RESET MODULE
;module to detect warm/cold start
;and temporarily to set ports
IRQ2
IRQ1
ICI
OCI
TOI
CMI
NMI
SIO
RES
TRAP
```

```
0000E000 71E014 AIM %11100000,RAM
0000E003 PORT5
0000E003 724014 OIM %01000000,RAM
0000E006 PORT5
0000E006 8E00FF LDS #$00FF set stack pointer
0000E009 CE0040 LDX #$40
0000E00C 4F CLRA
0000E00D A700 RAMCLR STAA 0,X
0000E00F 08 INX
0000E010 8C0100 CPX #$100
0000E013 26F8 BNE RAMCLR
0000E015 86A8 LDAA #%10101000 set dec pt and SIO rec'v
0000E017 e line
0000E017 9703 STAA PORT2
0000E019 86FF LDAA #%11111111 set port 2 for output
0000E01B 9701 STAA PORT2DDR
0000E01D 8600 LDAA #%00000000
0000E01F 9717 STAA PORT6
0000E021 860F LDAA #%00001111 set port 6 for input/out
0000E023 put
0000E023 9716 STAA PORT6DDR
0000E025 8602 LDAA #$2 set timer 2 baud rate
0000E027 971C STAA TCONR 9600
0000E029 IF
0000E029 8624 LDAA #%00100100
0000E02B 9710 STAA RMCR
0000E02D 861A LDAA #%00011010
0000E02F 9711 STAA TRCSR1
0000E031 8601 LDAA #%00000001
0000E033 971E STAA TRCSR2
0000E035 ELSE
LDAA #%01110100
STAA RMCR
LDAA #%00011010
STAA TRCSR1
0000E035 ENDIF
0000E035 8610 LDAA #%00010000
0000E037 971B STAA TCSR3
0000E039 0E CLI
0000E03A CE0140 LDX #RAMSTRT
0000E03D FF0100 STX DMPSTRT
0000E040 71FC03 AIM %11111100,POR
0000E043 T2
0000E043 FEC100 NEXT LDX DMPSTRT
```



```

0000E046 86FF      TSLP1      LDAA      #%11111111
0000E048 A700              STAA      0,X
0000E04A A100              CMPA      0,X
0000E04C 264B              BNE       WRNGRAM
0000E04E 08                INX
0000E04F 8CE000           CPX       #RAMEND
0000E052 26F2              BNE       TSLP1
0000E054 7C0003           INC       PORT2
    
```

```

0000E057 CE0140           LDX       #RAMSTRT
0000E05A 86FF      TSLP2      LDAA      #%11111111
0000E05C A700              STAA      0,X
0000E05E A100              CMPA      0,X
0000E060 2637              BNE       WRNGRAM
0000E062 08                INX
0000E063 8CE000           CPX       #RAMEND
0000E065 26F2              BNE       TSLP2
0000E068 7C0003           INC       PORT2
    
```

```

0000E06B CE0140           LDX       #RAMSTRT
0000E06E 86FF      TSLP3      LDAA      #%11111111
0000E070 A700              STAA      0,X
0000E072 A100              CMPA      0,X
0000E074 2623              BNE       WRNGRAM
0000E076 08                INX
0000E077 8CE000           CPX       #RAMEND
0000E07A 26F2              BNE       TSLP3
0000E07C 7C0003           INC       PORT2
    
```

```

0000E07F CE0140           LDX       #RAMSTRT
0000E082 86FF      TSLP4      LDAA      #%11111111
0000E084 A700              STAA      0,X
0000E086 A100              CMPA      0,X
0000E088 260F              BNE       WRNGRAM
0000E08A 08                INX
0000E08B 8CE000           CPX       #RAMEND
0000E08E 26F2              BNE       TSLP4
0000E090 7C0003           INC       PORT2
    
```

```

0000E093 CE0000           LDX       #0000
0000E096 8500              LDAA      #0
0000E098 3F                SWI
    
```

```

0000E099 9603      WRNGRAM    LDAA      PORT2
0000E09B 8403              ANDA      #3
0000E09D 3F                SWI
0000E09E              MEND
    
```

```

L.
10 REM: SAVE"L.LOGGEN"
20 X=OPENOUT("A.ADDLOG")
30 PRINT"Difference in levels          Add          hi_byte  lo_byte"
40 FOR A= 0 TO 5.11 STEP 0.01
50   B=10^A :REM A=10LOG(B)  O=10LOG(1)
60   C=B+1
70   D=LOG(C)
80   E=10*D :REM E=10LOG(1+B)
90   F=10*A :REM F=10LOG(B) ie dB's
100  G=E-F  :REM G=10LOG(1+B)/B
110  H=G*2560 :REM H IS IN 0.00039dB MULTIPLES
120  I=INT(H/256)
125  J=INT((H-(I*256))+0.5)
130  PRINTTAB(9); F;TAB(24);G,~I,~J
140  BPUT# X,I
145  BPUT# X,J
150 NEXT A
160 CLOSE# X
170 END
>

```

&gt;RUN

Difference in levels	Add	hi_byte	lo_byte
0	3.01029996	1E	1A
0.1	2.96058778	1D	9B
0.2	2.91145115	1D	1D
0.3	2.86288985	1C	A1
0.4	2.8149035	1C	26
0.5	2.76749157	1B	AD
0.6	2.72065336	1B	35
0.7	2.67438805	1A	BE
0.8	2.62869465	1A	49
0.9	2.58357203	19	D6
1	2.53901891	19	64
1.1	2.49503386	18	F3
1.2	2.45161531	18	84
1.3	2.40876154	18	16
1.4	2.36647071	17	AA
1.5	2.32474081	17	3F
1.6	2.28356971	16	D6
1.7	2.24295515	16	6E
1.8	2.20289472	16	7
1.9	2.1633859	15	A2
2	2.12442603	15	3F
2.1	2.08601232	14	DC
2.2	2.04814186	14	7B
2.3	2.01081164	14	1C
2.4	1.9740185	13	BD
2.5	1.9377592	13	61
2.6	1.90203037	13	5
2.7	1.86682852	12	AB
2.8	1.83215008	12	52
2.9	1.79799137	11	FB
3	1.76434862	11	A5
3.1	1.73121796	11	50
3.2	1.69859541	10	FC
3.3	1.66647692	10	AA
3.4	1.63485838	10	59
3.5	1.60373556	10	A
3.6	1.57310417	F	BB
3.7	1.54295985	F	6E
3.8	1.51329816	F	22
3.9	1.48411461	E	D7
4	1.45540463	E	8E
4.1	1.42716361	E	46
4.2	1.39938687	D	FE
4.3	1.37206968	D	B8
4.4	1.34520726	D	74
4.5	1.3187948	D	30
4.6	1.29282744	C	EE
4.7	1.26730028	C	AC
4.8	1.24220837	C	6C
4.9	1.21754677	C	2D
5	1.19331048	B	EF
5.1	1.16949448	B	B2
5.2	1.14609374	B	76
5.3	1.1231032	B	3B
5.4	1.10051779	B	1
5.5	1.07833242	A	C9
5.6	1.05654201	A	91
5.7	1.03514145	A	5A
5.8	1.01412566	A	24
5.9	0.993489517	9	EF
6	0.973227937	9	BB
6.1	0.95333582	9	89
6.2	0.933808079	9	57
6.3	0.914639637	9	25



6.4	0.895825423	8	F5
6.5	0.877360394	8	C6
6.6	0.859239517	8	98
6.7	0.841457769	8	6A
6.8	0.82401016	8	3D
6.9	0.806891721	8	12
7	0.790097499	7	E7
7.1	0.773622578	7	BC
7.2	0.757462062	7	93
7.3	0.741611101	7	6B
7.4	0.726064855	7	43
7.5	0.710818527	7	1C
7.6	0.69586736	6	F5
7.7	0.681206627	6	D0
7.8	0.666831642	6	AB
7.9	0.65273775	6	87
8	0.638920344	6	64
8.1	0.625374854	6	41
8.2	0.612096757	6	1F
8.3	0.599081568	5	FE
8.4	0.586324845	5	DD
8.5	0.573822197	5	BD
8.6	0.561569266	5	9E
8.7	0.549561758	5	7F
8.8	0.537795413	5	61
8.9	0.52626602	5	43
9.0	0.51496942	5	26
9.1	0.503901504	5	A
9.2	0.493058205	4	EE
9.3	0.482435506	4	D3
9.4	0.472029448	4	B8
9.5	0.461836115	4	9E
9.6	0.451851644	4	85
9.7	0.44207222	4	6C
9.8	0.432494074	4	53
9.9	0.423113514	4	3B
10	0.413926855	4	24
10.1	0.404930498	4	D
10.2	0.396120884	3	F6
10.3	0.387494501	3	E0
10.4	0.379047893	3	CA
10.5	0.370777652	3	B5
10.6	0.362680417	3	A0
10.7	0.354752887	3	8C
10.8	0.346991803	3	78
10.9	0.339393966	3	65
11	0.331956204	3	52
11.1	0.32467543	3	3F
11.2	0.317548562	3	2D
11.3	0.310572609	3	1B
11.4	0.30374461	3	A
11.5	0.297061644	2	F8
11.6	0.290520847	2	E8
11.7	0.284119412	2	D7
11.8	0.277854558	2	C7
11.9	0.271723568	2	B8
12	0.265723761	2	A8
12.1	0.259852514	2	99
12.2	0.254107226	2	8B
12.3	0.248485368	2	7C
12.4	0.24298444	2	6E
12.5	0.237601984	2	60
12.6	0.232335597	2	53
12.7	0.227182914	2	46
12.8	0.222141605	2	39
12.9	0.217209384	2	2C

13.0	0.212384026	2	20
13.1	0.207663316	2	14
13.2	0.203045104	2	8
13.3	0.198527258	1	FC
13.4	0.194107715	1	F1
13.5	0.189784419	1	E6
13.6	0.185555376	1	DB
13.7	0.181418601	1	DO
13.8	0.177372191	1	C6
13.9	0.173414242	1	BC
14.0	0.169542897	1	B2
14.1	0.165756341	1	A8
14.2	0.162052784	1	9F
14.3	0.158430476	1	96
14.4	0.154887699	1	8D
14.5	0.151422773	1	84
14.6	0.148034044	1	7B
14.7	0.144719895	1	72
14.8	0.141478747	1	6A
14.9	0.138309028	1	62
15.0	0.135209225	1	5A
15.1	0.132177848	1	52
15.2	0.12921343	1	4B
15.3	0.126314532	1	43
15.4	0.12347975	1	3C
15.5	0.120707702	1	35
15.6	0.117997043	1	2E
15.7	0.115346454	1	27
15.8	0.112754639	1	21
15.9	0.110220321	1	1A
16.0	0.107742269	1	14
16.1	0.105319247	1	E
16.2	0.102950074	1	8
16.3	0.100633584	1	2
16.4	9.83686224E-2	0	FC
16.5	9.61540937E-2	0	F6
16.6	9.39888731E-2	0	F1
16.7	9.18718874E-2	0	EB
16.8	8.98021013E-2	0	E6
16.9	8.77784789E-2	0	E1
17.0	8.57999995E-2	0	DC
17.1	8.38656947E-2	0	D7
17.2	8.1974566E-2	0	D2
17.3	8.01257119E-2	0	CD
17.4	7.83181712E-2	0	C8
17.5	7.65510499E-2	0	C4
17.6	7.48234615E-2	0	C0
17.7	7.31345341E-2	0	BB
17.8	7.14834109E-2	0	B7
17.9	6.98692724E-2	0	B3
18.0	6.82912841E-2	0	AF
18.1	6.67486787E-2	0	AB
18.2	6.52406439E-2	0	A7
18.3	6.37664348E-2	0	A3
18.4	6.23252988E-2	0	A0
18.5	6.09165058E-2	0	9C
18.6	5.95393404E-2	0	98
18.7	5.8193095E-2	0	95
18.8	5.68770841E-2	0	92
18.9	5.55906668E-2	0	8E
19.0	5.43331429E-2	0	8B
19.1	5.31039089E-2	0	88
19.2	5.19023091E-2	0	85
19.3	5.07277399E-2	0	82
19.4	4.9579598E-2	0	7F
19.5	4.84573022E-2	0	7C

19.6	4.73602712E-2	0	79
19.7	4.62879539E-2	0	76
19.8	4.52397689E-2	0	74
19.9	4.42152172E-2	0	71
20.0	4.321374E-2	0	6F
20.1	4.22348529E-2	0	6C
20.2	4.1278027E-2	0	6A
20.3	4.03427705E-2	0	67
20.4	3.94286141E-2	0	65
20.5	3.85350734E-2	0	63
20.6	3.76617014E-2	0	60
20.7	3.68080437E-2	0	5E
20.8	3.59736532E-2	0	5C
20.9	3.51580903E-2	0	5A
21.0	3.43609527E-2	0	58
21.1	3.35818157E-2	0	56
21.2	3.28202918E-2	0	54
21.3	3.20759565E-2	0	52
21.4	3.1348452E-2	0	50
21.5	3.06373835E-2	0	4E
21.6	2.99423933E-2	0	4D
21.7	2.92631015E-2	0	4B
21.8	2.85991877E-2	0	49
21.9	2.79502869E-2	0	48
22.0	2.73160487E-2	0	46
22.1	2.66961679E-2	0	44
22.2	2.60903165E-2	0	43
22.3	2.54981667E-2	0	41
22.4	2.49194205E-2	0	40
22.5	2.4353765E-2	0	3E
22.6	2.38009319E-2	0	3D
22.7	2.32606009E-2	0	3C
22.8	2.27325037E-2	0	3A
22.9	2.22163722E-2	0	39
23.0	2.17119381E-2	0	38
23.1	2.12189108E-2	0	36
23.2	2.07370669E-2	0	35
23.3	2.02661231E-2	0	34
23.4	1.98058635E-2	0	33
23.5	1.93560272E-2	0	32
23.6	1.89163908E-2	0	30
23.7	1.84867233E-2	0	2F
23.8	1.80667862E-2	0	2E
23.9	1.76563635E-2	0	2D
24.0	1.72552615E-2	0	2C
24.1	1.68632418E-2	0	2B
24.2	1.6480118E-2	0	2A
24.3	1.61056742E-2	0	29
24.4	1.57397389E-2	0	28
24.5	1.53820887E-2	0	27
24.6	1.50325522E-2	0	26
24.7	1.46909505E-2	0	26
24.8	1.435709E-2	0	25
24.9	1.40308067E-2	0	24
25.0	1.37119368E-2	0	23
25.1	1.34002939E-2	0	22
25.2	1.30957291E-2	0	22
25.3	1.27980635E-2	0	21
25.4	1.25071779E-2	0	20
25.5	1.22228712E-2	0	1F
25.6	1.19450316E-2	0	1F
25.7	1.16734952E-2	0	1E
25.8	1.14081129E-2	0	1D
25.9	1.11487657E-2	0	1D
26.0	1.08953118E-2	0	1C
26.1	1.06476173E-2	0	1B

26.2	1.0405533E-2	0	1B
26.3	1.01689398E-2	0	1A
26.4	9.93774831E-3	0	19
26.5	9.71177965E-3	0	19
26.6	9.49095935E-3	0	18
26.7	9.27515328E-3	0	18
26.8	9.06424224E-3	0	17
26.9	8.85812193E-3	0	17
27.0	8.65668803E-3	0	16
27.1	8.45982134E-3	0	16
27.2	8.26744735E-3	0	15
27.3	8.0794245E-3	0	15
27.4	7.89568573E-3	0	14
27.5	7.71610439E-3	0	14
27.6	7.54062831E-3	0	13
27.7	7.3691383E-3	0	13
27.8	7.20153004E-3	0	12
27.9	7.03772902E-3	0	12
28.0	6.87766075E-3	0	12
28.1	6.72122091E-3	0	11
28.2	6.56835735E-3	0	11
28.3	6.41894341E-3	0	10
28.4	6.27294183E-3	0	10
28.5	6.13025576E-3	0	10
28.6	5.99081069E-3	0	F
28.7	5.85453212E-3	0	F
28.8	5.72134554E-3	0	F
28.9	5.59120625E-3	0	E
29.0	5.46401739E-3	0	E
29.1	5.3397119E-3	0	E
29.2	5.21823764E-3	0	D
29.3	5.09952754E-3	0	D
29.4	4.9835071E-3	0	D
29.5	4.87014651E-3	0	C
29.6	4.75934148E-3	0	C
29.7	4.65106219E-3	0	C
29.8	4.5452565E-3	0	C
29.9	4.44184244E-3	0	B
30.0	4.34078276E-3	0	B
30.1	4.24202532E-3	0	B
30.2	4.14550304E-3	0	B
30.3	4.05118614E-3	0	A
30.4	3.95901501E-3	0	A
30.5	3.86893749E-3	0	A
30.6	3.78090888E-3	0	A
30.7	3.69487703E-3	0	9
30.8	3.61081213E-3	0	9
30.9	3.52864712E-3	0	9
31.0	3.44835967E-3	0	9
31.1	3.3698976E-3	0	9
31.2	3.29322368E-3	0	8
31.3	3.21828574E-3	0	8
31.4	3.14506143E-3	0	8
31.5	3.07348371E-3	0	8
31.6	3.00355256E-3	0	8
31.7	2.93520093E-3	0	8
31.8	2.86842138E-3	0	7
31.9	2.80314684E-3	0	7
32.0	2.73936242E-3	0	7
32.1	2.67702341E-3	0	7
32.2	2.61610746E-3	0	7
32.3	2.55657732E-3	0	7
32.4	2.49838829E-3	0	6
32.5	2.44154036E-3	0	6
32.6	2.38597393E-3	0	6
32.7	2.331689E-3	0	6

32.8	2.27861106E-3	0	6
32.9	2.22675502E-3	0	6
33.0	2.17609107E-3	0	6
33.1	2.12657452E-3	0	5
33.2	2.07817554E-3	0	5
33.3	2.03087926E-3	0	5
33.4	1.98467076E-3	0	5
33.5	1.93950534E-3	0	5
33.6	1.8953532E-3	0	5
33.7	1.85222924E-3	0	5
33.8	1.81007385E-3	0	5
33.9	1.76888704E-3	0	5
34.0	1.72862411E-3	0	4
34.1	1.68928504E-3	0	4
34.2	1.65084004E-3	0	4
34.3	1.61327422E-3	0	4
34.4	1.57654285E-3	0	4
34.5	1.54066086E-3	0	4
34.6	1.50561333E-3	0	4
34.7	1.47134066E-3	0	4
34.8	1.43784285E-3	0	4
34.9	1.4051199E-3	0	4
35.0	1.373142E-3	0	4
35.1	1.34190917E-3	0	3
35.2	1.31134689E-3	0	3
35.3	1.28151476E-3	0	3
35.4	1.25233829E-3	0	3
35.5	1.22384727E-3	0	3
35.6	1.1959821E-3	0	3
35.7	1.16875768E-3	0	3
35.8	1.14217401E-3	0	3
35.9	1.11618638E-3	0	3
36.0	1.090765E-3	0	3
36.1	1.06593966E-3	0	3
36.2	1.04169548E-3	0	3
36.3	1.01798773E-3	0	3
36.4	9.94801521E-4	0	3
36.5	9.72151756E-4	0	2
36.6	9.50038433E-4	0	2
36.7	9.28416848E-4	0	2
36.8	9.07287002E-4	0	2
36.9	8.86633992E-4	0	2
37.0	8.6645782E-4	0	2
37.1	8.46728683E-4	0	2
37.2	8.27461481E-4	0	2
37.3	8.08641315E-4	0	2
37.4	7.90223479E-4	0	2
37.5	7.72252679E-4	0	2
37.6	7.54654408E-4	0	2
37.7	7.37473369E-4	0	2
37.8	7.20694661E-4	0	2
37.9	7.04288483E-4	0	2
38.0	6.88254833E-4	0	2
38.1	6.72593713E-4	0	2
38.2	6.5729022E-4	0	2
38.3	6.42329454E-4	0	2
38.4	6.27696514E-4	0	2
38.5	6.13406301E-4	0	2
38.6	5.99458814E-4	0	2
38.7	5.8580935E-4	0	1
38.8	5.72472811E-4	0	1
38.9	5.59449196E-4	0	1
39.0	5.46723604E-4	0	1
39.1	5.34266233E-4	0	1
39.2	5.22091985E-4	0	1
39.3	5.10215759E-4	0	1

39.4	4.98607755E-4	0	1
39.5	4.87267971E-4	0	1
39.6	4.76151705E-4	0	1
39.7	4.65318561E-4	0	1
39.8	4.54738736E-4	0	1
39.9	4.4439733E-4	0	1
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40.2	4.14714217E-4	0	1
40.3	4.05296683E-4	0	1
40.4	3.96057963E-4	0	1
40.5	3.87042761E-4	0	1
40.6	3.78236175E-4	0	1
40.7	3.69638205E-4	0	1
40.8	3.61219048E-4	0	1
40.9	3.53008509E-4	0	1
41.0	3.44976783E-4	0	1
41.1	3.37123871E-4	0	1
41.2	3.29434872E-4	0	1
41.3	3.2196939E-4	0	1
41.4	3.14608216E-4	0	1
41.5	3.0747056E-4	0	1
41.6	3.00467014E-4	0	1
41.7	2.9361248E-4	0	1
41.8	2.8693676E-4	0	1
41.9	2.80410051E-4	0	1
42.0	2.74017453E-4	0	1
42.1	2.67773867E-4	0	1
42.2	2.61679292E-4	0	1
42.3	2.5574863E-4	0	1
42.4	2.49907374E-4	0	1
42.5	2.44230032E-4	0	1
42.6	2.38671899E-4	0	1
42.7	2.33232975E-4	0	1
42.8	2.2791326E-4	0	1
42.9	2.22742558E-4	0	1
43.0	2.17661262E-4	0	1
43.1	2.12714076E-4	0	1
43.2	2.07871199E-4	0	1
43.3	2.03132629E-4	0	1
43.4	1.98498368E-4	0	1
43.5	1.93998218E-4	0	0
43.6	1.89587474E-4	0	0
43.7	1.85281038E-4	0	0
43.8	1.8106401E-4	0	0
43.9	1.76936388E-4	0	0
44.0	1.72913074E-4	0	0
44.1	1.68979168E-4	0	0
44.2	1.65119767E-4	0	0
44.3	1.61364675E-4	0	0
44.4	1.57698989E-4	0	0
44.5	1.5412271E-4	0	0
44.6	1.50606036E-4	0	0
44.7	1.47163868E-4	0	0
44.8	1.43811107E-4	0	0
44.9	1.40532851E-4	0	0
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45.2	1.31189823E-4	0	0
45.3	1.2819469E-4	0	0
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45.5	1.2242794E-4	0	0
45.6	1.19641423E-4	0	0
45.7	1.16884708E-4	0	0
45.8	1.14247203E-4	0	0
45.9	1.11669302E-4	0	0

46.0	1.09121203E-4	0	0
46.1	1.0663271E-4	0	0
46.2	1.04188919E-4	0	0
46.3	1.01834536E-4	0	0
46.4	9.95099545E-5	0	0
46.5	9.7244978E-5	0	0
46.6	9.50247049E-5	0	0
46.7	9.28491354E-5	0	0
46.8	9.07480717E-5	0	0
46.9	8.87066126E-5	0	0
47.0	8.66502523E-5	0	0
47.1	8.46982002E-5	0	0
47.2	8.27759504E-5	0	0
47.3	8.08686018E-5	0	0
47.4	7.90506601E-5	0	0
47.5	7.72476196E-5	0	0
47.6	7.54743814E-5	0	0
47.7	7.37905502E-5	0	0
47.8	7.20769167E-5	0	0
47.9	7.0437789E-5	0	0
48.0	6.88433647E-5	0	0
48.1	6.72638416E-5	0	0
48.2	6.5729022E-5	0	0
48.3	6.42389059E-5	0	0
48.4	6.27934933E-5	0	0
48.5	6.13629818E-5	0	0
48.6	5.99473715E-5	0	0
48.7	5.8606267E-5	0	0
48.8	5.72651625E-5	0	0
48.9	5.59389591E-5	0	0
49.0	5.46872616E-5	0	0
49.1	5.3435564E-5	0	0
49.2	5.222857E-5	0	0
49.3	5.10513783E-5	0	0
49.4	4.98592854E-5	0	0
49.5	4.87416983E-5	0	0
49.6	4.76390123E-5	0	0
49.7	4.65363264E-5	0	0
49.8	4.5478344E-5	0	0
49.9	4.44352627E-5	0	0
50.0	4.34368849E-5	0	0
50.1	4.24534082E-5	0	0
50.2	4.14699316E-5	0	0
50.3	4.05311584E-5	0	0
50.4	3.96072865E-5	0	0
50.5	3.86983156E-5	0	0
50.6	3.78191471E-5	0	0
50.7	3.69697809E-5	0	0
50.8	3.61353159E-5	0	0
50.9	3.53008509E-5	0	0
51.0	3.45110893E-5	0	0
51.1	3.37362289E-5	0	0

&gt;

```
L.  
10 CLOSE#0  
20 REM SAVE"L.TIMLGEN"  
30 X=OPENOUT("A.TIMLOG")  
40 Y=1.0232929922:REM 10**(0.01)  
50 Z=LOG(Y)  
60 PRINT"   Difference hi_byte  lo_byte"  
70 PRINT"     in levels"  
80 FOR A= 128 TO 255 STEP 1  
90   B=256*LOG(A)/Z  
100  I=INT(B/256)  
110  J=INT((B-(I*256))+0.5)  
120  BPUT# X,I  
130  BPUT# X,J  
140  PRINT A,~I,~J  
150 NEXT A  
160 CLOSE# X  
170 END  
>
```



&gt;RUN

Difference in levels	hi_byte	lo_byte
128	D2	B9
129	D3	F
130	D3	65
131	D3	BA
132	D4	F
133	D4	63
134	D4	B6
135	D5	9
136	D5	5B
137	D5	AC
138	D5	FD
139	D6	4D
140	D6	9D
141	D6	EC
142	D7	3B
143	D7	89
144	D7	D6
145	D8	23
146	D8	6F
147	D8	BB
148	D9	7
149	D9	52
150	D9	9C
151	D9	E6
152	DA	2F
153	DA	78
154	DA	C1
155	DB	8
156	DB	50
157	DB	97
158	DB	DE
159	DC	24
160	DC	69
161	DC	AF
162	DC	F4
163	DD	38
164	DD	7C
165	DD	C0
166	DE	3
167	DE	46
168	DE	88
169	DE	CA
170	DF	B
171	DF	4D
172	DF	8E
173	DF	CE
174	EO	E
175	EO	4E
176	EO	8D
177	EO	CC
178	E1	B
179	E1	49
180	E1	87
181	E1	C5
182	E2	2
183	E2	3F
184	E2	7B
185	E2	B8
186	E2	F4
187	E3	2F
188	E3	6A
189	E3	A5
190	E3	E0

191	E4	1A
192	E4	55
193	E4	8E
194	E4	C8
195	E5	1
196	E5	3A
197	E5	72
198	E5	AB
199	E5	E3
200	E6	1A
201	E6	52
202	E6	89
203	E6	C0
204	E6	F7
205	E7	2D
206	E7	63
207	E7	99
208	E7	CE
209	E8	4
210	E8	39
211	E8	6E
212	E8	A2
213	E8	D7
214	E9	B
215	E9	3E
216	E9	72
217	E9	A5
218	E9	D8
219	EA	B
220	EA	3E
221	EA	70
222	EA	A3
223	EA	D5
224	EB	6
225	EB	38
226	EB	69
227	EB	9A
228	EB	CB
229	EB	FC
230	EC	2C
231	EC	5C
232	EC	8C
233	EC	BC
234	EC	EC
235	ED	1B
236	ED	4B
237	ED	7A
238	ED	A8
239	ED	D7
240	EE	5
241	EE	34
242	EE	62
243	EE	90
244	EE	BD
245	EE	EB
246	EF	18
247	EF	45
248	EF	72
249	EF	9F
250	EF	CB
251	EF	F8
252	FO	24
253	FO	50
254	FO	7C
255	FO	A7

&gt;

## Proceedings of The Institute of Acoustics

## EVALUATION OF LOUDNESS EQUIVALENT METERS

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Evaluation of Leq MetersIntroduction

Leq meters are almost exclusively calibrated using a continuous input signal. This calibration only confirms that the Leq meter can measure sound pressure level, but tells nothing about the Leq meters ability to measure impulsive signals. The Health & Safety Executive have produced a much needed draft standard for Leq meters which, it is expected, will form the basis of an international standard. The work presented here describes the use of a tone-burst generator which has been developed in order to investigate certain aspects of the draft standard, with reference to specific Leq measuring systems.

Tests

The type of input signal which most readily distinguishes between sound level meters and the different grades of Leq meters proposed in the draft standard is that which consists of high amplitude impulses; the maximum amplitude and mark:space ratio of these impulses being different for each grade of instrument. The output of the tone-burst generator, which has been developed in order to produce such impulses, consists of integral cycles of 6KHz sinusoid with a variable, but pre-determined, mark:space ratio; each cycle starting and ending at a zero-crossing. The tone-burst generator also produces these impulses in the presence of a completely variable level of background signal of identical frequency which is phase-locked to the pulses.

A continuous sinusoidal signal at 6KHz is applied to the Leq meter to be tested, and the level of the input is adjusted to give a reading of approximately 10 dB above the bottom of the indicator range. A series of tone-bursts is then substituted for the continuous signal and the level of the input is increased to give an identical Leq, ie if the number of pulses in a given period is reduced by a factor of 10, the level of the pulses must be increased by 10dB to maintain the same Leq. The permissible error for different combinations of mark:space ratio and signal amplitude is specified in the draft standard as the Exchange Rate Tolerance. Although such a test does measure the exchange rate, it is also a measure of the instruments ability to handle impulsive signals, however, this is of no serious consequence since the main reason for using an Leq meter in place of a sound level meter is to accurately integrate high level transients.

A further test is specified in the draft standard which measures the maximum impulse which the Leq meter can measure, to within a certain tolerance of the error allowed by linearity tests performed using a continuous signal. This impulse is presented to the meter in the presence of a continuous background signal which is set at a level corresponding the bottom end of the dynamic

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### EVALUATION OF LOUDNESS EQUIVALENT METERS

span. The result of this test is called the Peak Factor capability and is expressed as the ratio of the peak value of the impulse to the rms level of continuous background signal.

To have any confidence in the results in any of the above tests, there must be complete confidence in all of the testing equipment. An important part of this work was to conduct a thorough examination of the signal sources used and to consider any possible irregularities in measurements due to properties of the signal, or of the measuring equipment. A transient recorder was used to check that the tone-bursts started and stopped at zero and several spectrum analyzers were used to check the frequency content of the signal source.

#### Results

Instrument	Input Signal Mark:Space Ratio/Level			
	1:9/+10dB	1:99/+20dB	1:999/+30dB	1:9999/+40dB
1	0.4, 0.2	7.5, 5.8	=, 9.8	=, =
2	0.2, 0.3	0.9, 1.1	5.5, 3.5	=, 3.8
3	0.0, 0.0	0.3, 0.3	3.4, 1.9	=, 2.7
Reference Standard	0.2 (0.5)	0.4 (0.5)	0.6 (1.0)	1.0 (1.0)
4	0.0	0.0	0.0	0.3
5	0.0	0.0	0.0	<0.1

Fig.1 Exchange Rate Error for some of the meters which were tested.

The results of the exchange rate test are shown in Fig.1. The input signal levels shown are relative to the continuous signal which is applied to the meter as the reference level. The errors shown in the table are the difference between the reading with the reference level applied and the reading with the specified mark:space ratio and level, expressed in decibels.

Initially the test was carried out using only a single cycle in the tone-burst. Where an instrument failed to meet a certain standard, which is shown as in the table, the test was repeated using a series of ten cycles in each tone-burst and a correspondingly larger gap between bursts. This accounts for the readings where two errors are given for each input signal mark:space ratio and level; the first reading corresponding to the single cycle test, and the second, to the ten cycle test.

#### Discussion

The five instruments whose exchange rate errors appear in Fig.1 are all instruments which are described by their manufacturers as precision grade. Therefore, the reference standard included in the table corresponds to a Type 1

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### EVALUATION OF LOUDNESS EQUIVALENT METERS

peak instrument as specified by the Health & Safety Executive in their draft standard which was supplied to instrument manufacturers for a competitive tender. Since that time the exchange rate tolerance has been increased, and the current proposed tolerances are shown in brackets for comparison. It can be seen, however, that this does not affect the ranking.

The draft standard allows for instruments with a reduced peak factor capability. This restricts the range of mark:space ratios over which the instrument must measure and also increases the permissible error. On the basis of the above results, instrument no.3 may be considered as a type 1 non-peak instrument under both the original and the relaxed specifications, and instrument no.2 may be considered as marginal for type 1 non-peak under the relaxed specification only.

It is interesting to note that instruments 1-3 calculate  $L_{eq}$  from a rectified signal, ie from sound pressure level, whereas instruments 4 and 5 calculate  $L_{eq}$  directly, ie from sound pressure. Instruments 1-4 have a digital display and presumably digital processing, whereas instrument 5 has an analogue display and analogue processing. This information suggests that optimum accuracy cannot be achieved by calculating  $L_{eq}$  from sound pressure level and contradicts a popularly held view that digital instruments are inherently more accurate.

#### Conclusion

The results of this work emphasize the great disparity between instruments which nominally measure the same parameter. The proposed standard is obviously much needed in order to help both the prospective customer and the instrument manufacturer.

# inter-noise

Honolulu, USA  
1984 December 3-5

# 84

## A METHOD OF GENERATING "SHORT LEQ"

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The concept of short Leq was originally developed by the LNE in France as a method of time compressing data without losing any of the basic energy information. In essence the object is to take a series of elemental Leqs one after the other with no break. The time of each elemental Leq can vary between 125mS which equates to the Fast time constant, up to an acquisition period of several minutes. In practical systems, where the number of elemental Leq are limited by storage space, the fastest acquisition rate is used consistent with the total measurement time. Table 1 shows the total measurement times for a 64K store (65536 words).

Table 1.

Acquisition time	64K storage time
125mS	2hr 16min
1sec	18.2hr
1min	45 days
10min	1yr 3mths

In any system of short Leq there are certain essential specification points to permit the system to operate to agreed international specifications such as IEC 651 and the proposed IEC Integrating Sound Level Meter standard. As, however the current proposals do not include short Leq, there are many points which need specially defining.

The first and most vital part of the specification is that each elemental Leq shall individually meet at least the full specification of normal Leq. The only exception to this would be that the normal 10sec or so to allow the reading to stabilise is too long and in the design specification we have required that at the end of the elemental Leq the reading shall be within 0,1dB of the nominal "final" reading over the prime range and 0,2dB over the whole dynamic span of the unit.

The second specification point is that the time between elemental Leq shall be small in relation to the Leq time. In the original concept 'lost' times of about half a millisecond were considered acceptable. However, in the current realisation lost time is down to about 20 microseconds, i.e. about 2 parts in  $10^4$  at the fastest acquisition rate. Thus the lost data is insignificant in any practical situation.

The third vital point concerns the total measuring range. If the unit is to be used over a 7 day period there are many situations where the instantaneous level will vary between the noise floor, which could be of the order of 20dBA, and levels in the low hundreds say 120dBA. A dynamic span of 100dB is to say the least difficult unless auto-ranging is employed. 100dB may not seem a vast range, but for a 50mV/Pa microphone it is a voltage range from 10 microvolts rms to 3V peak to peak. If auto-ranging is used there is the classic problem of how and when to switch ranges. Clearly, with a microcomputer unit the decision is eased, but the time over which range switching occurs must be of a similar order to the dead time. However, practical sound level meters in the recent past which incorporated auto-ranging have usually not been a success usually because of settling time or computation error. In the new concept of short Leq it has been pre-supposed that auto-ranging is not acceptable and thus the present realisation has no auto-ranging. Instead 3 manual ranges are fitted each of 100dB. While there must be many situations where this dynamic span is exceeded, there are fortunately many more where a 100dB span is adequate.

When the elemental Leq has been computed it is stored in a CMOS RAM. This is organised into 2 parts: the Leq itself and other data bits. The actual Leq which has a resolution of 0.1dB requires an 11 bit word to allow for longer dynamic spans than the current 100. Bits 12 through 16 gives a 5 bit code with 32 possibilities. The precise codes are in the main established although some of the 32 have been left undefined to allow for system extensions. At this time the 5 bit coding is not being published not only for reasons of software copyright but also for reasons of contractual agreement. However, the principles involved in the coding are of interest.

Firstly one code must indicate that the reading is indeed an Leq. This way seems redundant but in fact the system can acquire other data in the environmental analyser: For example, vehicle count, temperature, humidity, windspeed in non-acoustic terms and also the peak value or an octave band level in the acoustic domain.

Also, some of the 2048 possible levels far exceed the required coding for Leq alone. If we assume a

maximum range of say 0dB to 164dB, that requires 1640 to give 0,1dB resolution leaving over 400 to be used in complex programming for other purposes. Some high Leq codes are used where the elemental Leq may be in error and thus is not recorded. Examples of this would be a routine microphone calibration, power drop out, operating of controls during an elemental Leq etc. At this time 7 error codes are fully defined all of these replacing an Leq.

Some of the other 400 non Leq values are assigned to test and data function which are stored while the current Leq is being calculated. For example, in one realisation of short Leq 10 parallel channels of 9 octaves plus dBA are measured at the same time. This requires special test and timing routines which are stored and coded in the 400 'false' Leq values.

One bit of the 16 is used as an overload flag. Thus if any elemental Leq exceeds the dynamic span the Leq is stored but the overload is flagged and thus the software can take account of this. Other vital data which must be recorded is generated at each use of 'Pause' or even switch-on. For example, the real time is first recorded followed by a test sequence. Thus, if a handheld unit such as the CRL 2.36 is in use, the operator merely has to record his physical position at each time pause or switch-on. The unit itself records the time and calibration data. This function which involves a real time clock is, like the memory, backed up by a separate battery which has a working life of over one year after the main battery is totally discharged. This back-up is automatically float charged from the main battery during normal use.

As turning the unit off does not destroy data some means have to be provided for resetting the memory. Normally this is never done in the field and thus it is a software function which occurs only after readout of memory. However, to enable the full store to be used at any time, a keyboard routine is built into the CRL 2.36 to enable reset to be achieved only by a multiple keystroke.

The first long term monitor unit having short Leq, the CRL 2.40, has instead a locked hard reset. We consider that an outdoor monitor is less likely to be put to 'pause' and thus does not usually make several measurements on one reset.

The next part of the chain after data acquisition is data readout and for this an interface is required. Clearly if this can be to some defined standard this will naturally increase the number of access units available.

In 1980 Cirrus Research proposed the DP15 analogue bus and the L3M microphone input interface. Now we propose a new digital interface the DP37. This like the DP15 and L3M is based on a connector available



internationally from many sources.

The CRL 2.36 has the new DP37 digital bus which has already had over a years field trials. Included in the DP37 is a full RS432 type serial interface with all the standard commands together with the IEEE 488 Purpose Interface Bus (GP1B). This allows the acquisition unit to function both as a talker/listener "on line" to a micro but when not connected to a computer system, it takes over the function of bus controller, allowing control of intelligent peripherals. Extra connections are codified for filter drive and power supply so that plug-in units can be developed to modify the acquisition function of the units. For example, one of the first new units is a  $\frac{1}{3}$ rd octave filter which operates via the DP15 analogue bus but can be software controlled via the DP37 digital bus in real time.

The provision of both parallel and serial interfaces may seem excessive but this is a system requirement. The RS432 is needed for MODEM use wick includes the use of the acquisition unit as a monitor at the end of a telephone line. If the CRL 2.40 is connected to a phone line it can be interrogated from anywhere in the world on a routine basis to output the data to a local computer and if required reset the memory for the next period's acquisition. Imagine a city with a series of units like the CRL 2.40. Each acquiring short Leq on a 1 sec basis. Twice a day the unit is automatically interrogated by the main computer and the data dumped onto disc. The noise foot-print of a small town can be mapped on a second by second basis using very little manpower. If telephone line installation is too expensive, as would be the case for short events such as a Pop Festival, the unit can be read back by dumping down to a standard cassette recorder. Naturally this needs a visit twice a day but that is a small price to pay for the amount of data that is acquired.

Software for the CRL 2.36 and CRL 2.40 is a vital part of the package and currently work is underway on using several microcomputers as the basic processor via an international operating system as well as in some machine codes.

#### SUMMARY

The concept of short Leq has allowed the realisation of a new generation of data acquiring sound level meters both handheld and as monitors. These units have a potential production cost far lower than current generation units together with storage capacities an order higher than current units. Raw data is time compressed into units which lose little basic information and in many cases obviate the need for tape recording noise data for subsequent analysis.

## INDUSTRIAL NOISE ASSESSMENT VIA SHORT LEQ

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The value of Leq in assessing time varying and, particularly, impulsive noises lies in its extended integration period when compared with the conventional sound level meter responses. The integration period for an Leq meter is equal to the measurement duration. Equal weighting is given to all noises, independently of their position in the time history of the measurement. These properties make Leq a better indicator than SPL when assessing hearing damage risk and noise nuisance due to impulsive noises. Having identified a potentially hazardous environment, a more detailed analysis is required to ensure that effective noise control measures can be adopted.

The method chosen for this detailed analysis is dependent on the type of noise source encountered. If the noise is varying, but with a restricted pulse range and rise/fall time, a level recorder can be used to generate a permanent record of the time history for later analysis. This analysis could consist of identifying the major peaks by correlation with a tape recorder or by notes written on the trace during recording. The response speed of the level recorder would preclude any accurate prediction of the overall Leq if a major noise source were attenuated due to some proposed noise control measure. If the noise is highly impulsive, with a large pulse range, an integrating sound level meter with the capability of measuring sound exposure level (SEL) can be used. This allows comparison of the energy content of individual impulses, but loses the time history value of a level recorder and may not allow separation of sources whose energy contributions overlap in time. Short Leq, originally proposed by researchers at LNE in France, combines all the attributes of an Leq meter with the analytical capabilities of the SLM/level recorder and SEL techniques.

Short Leq is generated by taking individual or elemental Leqs over a constant, pre-determined period, and storing them for later analysis on a computer. The number of different integration periods, the number of elemental Leqs which can be stored and the storage medium would depend on the particular instrument in use. At present, two basic types have been produced: one with the integration period set by the instrument front panel controls and containing internal memory, the other having its integration period controlled by an external microcomputer and utilising the mass storage of the computer for retaining the elemental Leqs. Further instruments which can be configured as intelligent

## INDUSTRIAL NOISE ASSESSMENT VIA SHORT LEQ

peripherals on a large data acquisition system are already proposed.

The choice of integration period for the elemental Leq depends on the resolution which is envisaged at the analysis stage. If the total memory capacity is not a limitation, then the shortest integration period should be chosen. For extended monitoring applications, the integration period need only be short enough to resolve the expected noise sources, e.g. the passing of an aeroplane, motor vehicle or train. If however, only one important noise source is expected, and the background noise is sufficiently low, the integration period need only be short enough to resolve the time between occurrences of the noise. With an integration period of 10 minutes and a fairly modest store of 64K words, data could be acquired for in excess of one year.

An integrating sound level meter is primarily intended for measuring impulsive noises. It is therefore essential that a short Leq acquisition unit should accurately integrate all incoming signals, and should not misrepresent large impulses which occur on an overlap between two successive elemental Leqs. The time lost between Leqs must be small enough such that an instantaneous impulse at the upper limit of the dynamic range, which overlapped two elemental periods, should not result in an error greater than the tolerance allowed for the elemental Leqs individually. The contiguous nature of the elemental Leqs is what transforms them from a simple sequence of values to a versatile representation of the raw data, from which many acoustic parameters can be derived.

If the elemental Leq period was correctly chosen, complete flexibility exists in the later treatment of the data. The elemental values can be recombined to form an overall or global Leq for any period within the total measurement. If a large period is to be represented when a very short elemental period was used during the acquisition, groups of short Leq can be combined to give a time history with any desired resolution in time. At the analysis stage, different noise events can be identified so that their contribution to the overall Leq, and the percentage of the measurement period for which each occurred, can be calculated.

Data from a number of acquisition units can be inserted into a common file, so that concurrent data from a number of measurement positions can be processed. Possible applications of an array of units include identifying and measuring transmission paths, quantifying the performance of sound barriers or simply to provide a convenient means of displaying multi-channel monitoring data.

## INDUSTRIAL NOISE ASSESSMENT VIA SHORT LEQ

The ability to recombine the elemental Leqs, identify and separate various noise sources and operate on multi-channel data are all new and powerful analysis tools; they are not, however, made available at the expense of more familiar acoustic measures.

A level recorder type trace can be produced which shows the time history of the measurement period. Such a graphic representation is often useful to demonstrate noise duration and repetition rate. Parameters which have historically, and empirically, been derived from level recorder traces can also be synthesized using short Leq, without the need for a dedicated measuring instrument. The most common of these are the Ln values, statistical parameters based on the level which was exceeded for n percent of the measurement time. A combination of at least two of these parameters is usually used to represent the variability of a particular noise environment. The flexibility of short Leq allows the choice of the appropriate percentage levels to be made at the analysis stage, rather than having to preset instrument controls.

The representation of the energy content of individual noise events by SEL is also supported by short Leq. Since all the raw data is recorded, the exact duration of an event can be defined with the aid of an examination of the time history. The definition of the time at which an event appears out of the background and returns back into it can be varied to determine precisely what uncertainty exists in the SEL. Performing this function at the analysis stage allows much greater flexibility than either relying on preset thresholds or on the mechanical pressing of buttons by an operator in real time.

Short Leq has shown itself to be a versatile tool for acoustic analysis. The existing software is being continually updated and expanded; to run on more powerful computers with more capable acquisition units, as more of the potential of short Leq is realized. An apparently conventional integrating sound level meter can now be interfaced with a popular home computer to provide a powerful analysis package at a much lower cost than existing dedicated hardware.

### Summary

Short Leq provides a new measurement concept which draws together and enhances existing acoustic parameters rather than trying to replace them. Its principal value lies in the retention of the raw data to allow flexibility at the analysis stage. These facilities can be incorporated into a hand-held instrument which can be used for short Leq or as a stand-alone instrument, as required.

DP37 - A DIGITAL ACOUSTIC INTERFACE

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INTRODUCTION

Advances in the availability of highly integrated computing power has led to a dilemma in the design of hand-held acoustic instrumentation. This arises from the designer being able to offer the instrument user a wide range of measurement options, including acquisition of large quantities of data, but at the same time not wishing to confuse the user with the presentation or volume of data. The simple solution is of course to leave the arduous analysis task to an office or home computer, where programming power and sophisticated, multi-colour graphics aid in presentation and interpretation. There are problems, however, in the transfer of data between the acquisition unit and the computer. This paper addresses these problems in an attempt to establish an internationally agreed hardware and software protocol for data transfer.

Interface Requirements

The functional requirements of the interface determine the best form of implementation. Care must therefore be exercised in the specification of the possible functions. Cirrus Research have gained much experience from the design and use, over a number of years, of both the L3M microphone input interface and the DP15 analogue interface which is used for external plug-in units. The value of investing time in making these interfaces as universal as possible has allowed expansion to applications which could not have been foreseen when the individual connector pins were assigned.

The original requirement was to transfer data from some acquisition unit to a microcomputer for subsequent analysis. For secure and controlled data transfer, some form of two-way communication is needed to allow a handshaking sequence to take place. The basic form of interface need consist of no more than a uni-directional data channel between the acquisition unit and the computer, together with a couple of control lines to conduct the handshaking sequence.

To limit the interface to this simple implementation is, however,

unnecessarily restrictive. The principal impetus which encouraged Cirrus Research to investigate communication interfaces suitable for instrumentation systems was the advent of the acoustic parameter short  $L_{eq}$ , which is described more fully in an accompanying paper. In essence, the time history of an acoustic signal is described by a series of  $L_{eq}$  values, each taken with a short integration period, which are contiguous in time. The concept allows for versatile and powerful interpretation of these elemental  $L_{eq}$  to reveal much information about the acoustic signal, and possible relationships with other concurrent data. A consequence of this is that an acquisition unit will often contain many data, possibly taken at different times or from a number of different measuring positions. A very useful feature to be incorporated in the interface is therefore the possibility of sending data from the computer which the acquisition unit can interpret as commands to control the volume and format of the  $L_{eq}$  data in the opposite direction.

Having established that two-way communication is a desirable feature of the interface, it is necessary to decide whether the handshaking protocol should allow simultaneous or sequential exchange of data, in established computer jargon - full-duplex or half-duplex. The advantages of full-duplex being increased transfer rate when two-way exchange is required and easier interruption when an erroneous data stream is being transmitted. These are attained at the expense of having to provide two independent data channels. A valued judgement between these alternatives can best be made by consideration of specific hardware options.

#### Serial or Parallel?

Many issues are raised by consideration of whether the data transfer should be bit serial or bit parallel, however, by confining attention to the number of data channels, one seems to be suited to each of the possible alternatives. The use of a second channel with serial data exchange requires only one extra wire, whereas with bit parallel transfer the number of extra wires is equal to width of the byte, typically 8-bit. It is no accident, therefore, that these correspond to versions of the two most popular and commonly implemented interface standards: RS232C and IEEE488.

The RS232C interface standard defines a number of signal lines but no connector. By common use, the DP25 connector works as an effective standard. Most of the 25 pins are assigned, but few are usually used in practice. This arises from the origin of the RS232C system, which was developed to enable data transfer between devices via some communication equipment, typically a pair of modems together with a telephone line. RS232C defines how the device interfaces with the communication equipment, however direct connection is not envisaged. The often used direct connection must therefore gloss over this inconsistency with the standard. This is usually achieved by simply ignoring many of the available signal lines. Use of RS232C type interfaces do enable simple, reliable communication links over relatively long distance, including, of course, via modems and telephone lines.

The IEEE488, in contrast, is primarily designed for local communication within intelligent instrumentation systems. If the system is restricted to a controller, the computer, and one peripheral, the acquisition unit, then the maximum separation is 2 metres. The limitation on cable length and the specification of line drive capabilities ensures that IEEE488 system can be used for extremely high data rates, up to 1 Mbyte per second. The IEEE488 standard does specify a stackable, 24-pin connector, however, the situation has been confused by the issuing of an almost identical IEC standard which specifies a 25-pin D-type connector. The use of a 3-wire handshaking protocol controls whichever of the instruments is putting data onto the common 8-bit bus, each instrument having a unique address code to enable it to distinguish which of the data on the bus are intended for it. The system must contain a single controller which is usually programmable and often a microcomputer. In the context of acoustic instrumentation, a complete system might comprise several acquisition units transferring data periodically to a central computer. An alternate system could have the acquisition unit acting as system controller, supervising a number of peripherals which might include a microphone multiplexer, a filter unit or even other forms of environmental monitoring.

The major disadvantage of the IEEE488 system is that of the cable length restriction. A bus extender, which converts from parallel to serial and vice versa, can be used where long distance communication is essential. Such a solution is only viable where a heavy commitment to the IEEE488 system has already been made, and the added complexity of the bus extenders can be justified.

#### The DP37 Solution

The proposed DP37 digital interface aims to draw together the useful features of both the RS232C and IEEE488 systems. To ensure complete compatibility with all IEEE488 systems, all of the 24 defined pins need to be implemented. For the reasons outlined earlier, only a further 5 or 6 pins need to be reserved to ensure compatibility with a majority of RS232C type interfaces. This leaves sufficient pins free for duplication of the standard power supply voltages and other signals which have proved useful on the DP15 analogue interface.

The DP37 uses an internationally available, multi-sourced connector. Different cables can be used to adapt to whichever of two standard interfaces is most appropriate for the system in use. Although the DP37 interface is fully specified, it is not expected that every instrument which has a DP37 connector supports all the possible interface functions. For example, a basic instrument might be a hand-held acquisition unit. The basic unit size is little more than the width of the connector and the interface is only capable of serial transfer of its memory contents upon request. More sophisticated units can form part of a distributed instrumentation system whose task would currently be performed by an environmental noise analyser. The advantage of a distributed system is the design flexibility and ease of system extension and upgrade.

The data formats which have already been used with the DP37 interface

are also intended to be flexible. The serial transfer is accomplished using the asynchronous serial protocol of 1 start bit, 8 data bits, 1 parity bit (even) and 1 stop bit. All the commands sent to the acquisition unit have so far been in ASCII code, an extensive list of commands already exist. The 8-bit data format allows response in ASCII, which eases the formatting task of the computer, or in binary. The binary option is used where large data blocks are to be transferred. The parallel transfer using the IEEE488 component of the interface is naturally 8-bit, which therefore can also be in ASCII or binary. Different commands are used to elicit the two formats of data. Although single byte parity checks are performed on the serial data no attempt has been made to perform parity checks across blocks of data, eg by checksums. This is because such a requirement would unnecessarily increase the computing requirement of the acquisition unit. We have not experienced any problems as a result of not including such a feature.

#### The Limits of Imagination

In summary, the purpose of the DP37 digital interface is to provide a versatile system for transferring data from the increasingly powerful acquisition units to microcomputer systems which operate sophisticated analysis packages. A major objective was to ensure that the specification of the interface did not limit its future use.



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CONSIDERATION OF ACOUSTIC ACCURACY OF COMPUTER METHODS

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Most scientists and engineers will be familiar with the use of specialist computer packages to process and analyze large volumes of data. This paper offers some observations about the use of conventional acoustic measuring hardware in conjunction with data processing software packages.

PROBLEMS OF COMPUTERS

A computer at the end of an acoustic signal processing chain replicates the function normally performed by the meter. The resolution of the display unit should be consistent with the tolerances on the data. Use of clever software should not detract from the acoustic accuracy. As an example, claims have been made for 0.1 dB resolution over a 60 dB span when employing an 8-bit analogue to digital converter. The differing presentations of analogue, digital and computer-based displays are all the same thing - man-machine interfaces. If the data present in the computer have a gaussian distribution, a combination of such data would statistically yield a result of greater accuracy than the basic data. After combining many Short  $L_{eq}$ , the apparent resolution is greater than that of each individual sample. The separate samples must therefore be to the full accuracy or the resolution is meaningless. This is evident since although such resolution improvement would be correctly gained for background noises, many industrial and environmental noise nuisances are impulsive, or at least intermittent.

DATA DISPLAY

The great value of analogue data presentation is that it can show important information about trends. Digital presentation is, however, much better for steady-state signals as the readings can be resolved better by humans. Computer displays

can utilize the advantages of both, but software errors can easily devalue the display. For example, the use of monitors with different numbers of pixels can cause problems if the screen display is addressed directly. A good design goal is to have easily transportable software. Such software should either overcome these difficulties or indicate possible limitations. Even the very simplest computers can also recombine Short  $L_{eq}$  to give any acoustic index, within the limitation of the acquired data, and can easily cope with data from several sources. This makes it possible to calculate and display differences in space, time and frequency or, given three microphones, plot probable noise sources.

#### FREQUENCY ANALYSIS

Simple signal processing, together with a simple computer can simulate a digital filter in quasi real-time. Semi-conductor manufacturers offer specialized integrated circuits which allow the construction of a number of parallel channels. If the FAST rms time constant is applied, microsecond differences will occur which will lead to minimal errors. Upon logarithmic conversion of the rms signal, a 50 dB dynamic range can be achieved using a 9-bit converter to yield 0.1 dB resolution. The games port of a simple computer usually has an 8-bit conversion accuracy - this would give 0.2 dB resolution. Such developments enable the rapid generation and synthesis of new indices. A combination of the 63 Hz, 125 Hz and 250 Hz octave-bands can be used to assess noise nuisance from discos. The transmission characteristics of buildings can be simulated to worn system controllers or limit the level. Realistic assessment of the nuisance due to industrial noise or rock festivals is facilitated in a way which was not previously possible.

#### TIME HISTORY

Desk top and home computers are generally programmed in a high-level language. This often has the effect of complicating input/output processes. The net result of this is that the control of data acquisition through its input ports is at "arms length" and necessarily has poor resolution in time. Some computers have the ability to include machine code subroutines within high-level language programs, but for ease of software portability, reliance on external hardware for signal conditioning and data capture is more profitable. Experience has shown that when the acquisition is controlled directly by the computer, a minimum resolution of about one second is consistent with amplitude resolution normally required.

The advent of instruments which can acquire Short  $L_{eq}$  data has provided an ideal complement for the modern desktop and home computer. Dedicated hardware can provide the optimum accuracy in both amplitude and time resolution. Standards are already in existence which specify the dynamic, time-averaging capabilities and the pre-set measurement time resolution

required of such instruments. This highlights the major difficulty in making comparisons between results produced from different software packages; there is no standard for performance. There should be no degradation of the data during transfer into the computer. The software package should therefore recognize the resolution of the data presented to it, and not allow the user to ascribe unrealistic accuracy to any derived results. A sample output from a typical software package is shown in Figure 1.

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Serial Number	2985
L <sub>eq</sub> period	1 sec
Range	30 dB
Date of readings	21 January 1986
Time of readings	10:50.08
Mode	L <sub>eq</sub>

NOTES: Demonstration of Indices for Inter-Noise 86

L values

L1 = 77.1  
 L10 = 58.3  
 L50 = 53.6  
 L90 = 52.7  
 L99 = 50.8

Overall L<sub>eq</sub> is: 55.2

FIGURE 1: Sample Output from Typical Software Package

The employment of the Short L<sub>eq</sub> methodology, with its constant measurement interval, allows graphical and tabulated presentation of the time history with the data combined in any multiple of the elemental period. This allows the software user to concentrate on either extreme of time resolution. When the data are combined into large multiples of the elemental period, long-term trends can be observed without distraction from fine detail. Lower multiples, down to the elemental period itself, enable examination of this fine detail. This is extremely useful in attempting to identify which of a number of possible sources, each with a recognizable signature, is providing the major contribution to the overall measured level.

Earlier reference was made to the ease with which computers can combine and analyze data from a number of sources. The additional data which is afforded by a multi-channel system enhances the ability of software to identify sources, though there is a natural limit on the localization possible, determined by the elemental Short L<sub>eq</sub> period. Utilization can also be made of the value of the multi-channel facility in readily assessing transmission loss from acoustic source to a number of observation locations. This is particularly useful where there is a restriction on the available time for acquisition. For instance, where the source being analyzed is of a transient nature, data

obtained from a series of sequential tests may contain masking which arises from usual experimental variation. Simultaneous data capture overcomes this problem, there being the added advantage of alignment of measured data by the software through a synchronizing signal such as a starting pistol shot.

#### SUMMARY

A number of software packages have been evaluated. Attention has been drawn to the necessary precautions to be taken before placing reliance on processed data from computers. The available software packages are extremely powerful analysis tools, enabled varied presentation in terms of time history, the  $L_n$  values and  $L_{eq}$ . The calculated values can be determined from any subset within the total measurement period, and at least one package can calculate the above in the octave bands.

## SINE BURST TESTING OF INTEGRATING SOUND LEVEL METERS

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## INTRODUCTION

Over the past decade there has been a continuing discussion as to the performance characteristics required of integrating sound level meters. Discussion has centred on quantifying the limits and tolerances of important parameters, however, a significant portion of the debate has been concerned with testing methodology and its relevance to practical acoustics. The aim of this paper is to review the various procedures which have been proposed for evaluating the transient response of instruments, and to report on developments in instrumentation required for such evaluation.

## TRANSIENT RESPONSE

The acceptable performance of acoustic instrumentation is often a compromise between practical requirements and technical feasibility. With integrating sound level meters, the current differences are small. There is fairly general agreement as to whether a specific instrument meets the acceptable standard, but divergence as to how the evaluation should be performed. For the steady-state testing, which is highly derived from conventional sound level meter standards, only the numbers are subject to debate. It is in the testing of dynamic behaviour or transient response where the divergence occurs.

Multi-cycle Testing

The use of tonebursts of integral cycles of sinewaves is accepted in IEC 804 as being an appropriate method of determining the linearity of the instrument outside the display range. The duty factor and tone burst duration are chosen to allow on scale readings to be taken without causing limitations due to the pulse range.

The pulse range, as defined in IEC 804, is determined by superimposing an in-phase tone burst on to a low level signal. The amplitude of the fixed frequency tone burst and its duration are varied in order to investigate the dynamic performance. A minimum pulse range is specified for each grade of instrument. This quantifies the ratio of the peak of the tone burst to the rms value of the low level background over which the instrument will integrate within given tolerances. The expectation is normally that the tolerance will only be approached at the higher peak levels, but the variation in tone burst amplitude allows investigation of mid-range non-linearities.

The use of the low level background performs a couple of useful functions. It provides a defined signal during the tone bursts "off" period, giving a minimum signal to noise ratio for the signal generator. Secondly, it provides what can arguably be described as a realistic representation of an acoustic signal, being an impulse rising out of a background level.

Single-cycle Testing

The use of single-cycle sine bursts of various frequencies to evaluate the "dynamic frequency weighting" was central to several drafts of the American National Standard for integrating sound level meters. As the frequency of the sinusoid is varied, the effective toneburst duration also varies. The instrument's response is most easily determined if it measures and displays sound exposure level. The reading on sound exposure level is stable after the single cycle has been applied. The actual meter reading is compared with a calculated value of sound exposure level which is based on both signal amplitude and frequency. If the instrument does not display sound exposure level, the calculation of theoretical meter reading is further complicated by having to compensate for the measurement duration. In addition, if the instrument has no provision for short term, fixed-period measurement, the meter reading will be falling constantly after the application of the impulse. The meter reading during the IEC 804 pulse factor test is also time variant, but as the input is repetitive the reading converges to a specific value.

The relevance of single-cycle sine bursts to the majority of acoustic signals is questionable. Low frequency single-cycles are reasonable simulations of shock waves, but a larger number of industrial noises are repetitive with considerable mid-frequency energy.

There is an argument that a single-cycle sine burst is a more efficient signal for stimulating the transient response than a multi-cycle tone burst. This could lead to the adoption of a dc step input as signal source, with the Impulse Response Function as the sole arbiter of acceptable dynamic performance. This may have interesting possibilities, but is even more difficult to relate to practical sound sources.

Independently, however, of any technical discussion as to the relative merits of these or any other evaluation methods, an international standard is now in existence. It is hoped that this can be universally accepted so as to remove the uncertainties about required performance which have existed since the construction of the first dedicated integrating sound level meter. Future debate on the testing of integrating sound level meters would most profitably centre on the tolerances of the various tests, with a view to the issuing of a future revised IEC 804.

## PRACTICAL IMPLEMENTATION

The authors have had experience over the last eight years in the design and use of instrumentation specifically designed for evaluating the transient performance of integrating sound level meters. The equipment which has been used has always had capabilities in excess of the performance required of the instruments, but the precise effect of shortcomings in the signal source is not fully understood. For example, whilst conducting a multi-cycle tone burst test as per IEC 804, the signal source was intentionally adjusted so as to start and stop at other than zero crossing. The resulting spectrum was virtually indistinguishable from that of the correctly adjusted waveform, the extra steps adding little to the already broadband spectrum. The instrument under test gave identical readings with both signals, within normal experimental uncertainty.

In a current exercise to further upgrade our existing testing facility, a number of commercial signal generators have been examined. Recognizing the role which computer assisted testing has to play, this included "intelligent" instrumentation designed for use via the IEEE 488 interface bus. One particular example, a programmable waveform generator, with the facility of remotely setting sinusoidal tone bursts with integral number of cycles, starting and stopping at zero crossing, with the ability to generate ISO preferred frequencies to 1 part in  $10^6$ , could only manage a signal to noise ratio of 62 dB and produced a less than orderly completion of the tone burst sequence.

Attention has therefore focussed on the development of specialized signal sources "in house". An interface has been constructed which allows control over signal level and frequency, tone burst duration and level of in-phase background signal for IEC 804 tests. Additional provision includes the facility for automatic logging of instrument performance, particularly of the latest generation of instruments which have the DP37 - digital acoustic interface.

The necessary software development to accompany this programmable hardware has resulted in a pseudo-language which enables quick setting up of a particular test schedule. Some knowledge of structured programming is all that is needed to modify the parameters which are passed to the procedures.

#### SUMMARY

The two commonly used methods of determining the ability of an integrating sound level meter to measure accurately impulsive signals have been discussed. It is suggested that, as the two methods would not result in significantly different instrumentation, the duality of evaluation procedures is avoided and the existing IEC 804 is universally adopted.

Attention has been drawn to the lack of quantified specification for signal sources. This has led to the development of dedicated hardware and software to aid in instrument evaluation.