Electrically active defects in novel group IV semiconductors

A thesis submitted in partial fulfilment of the requirements of Sheffield Hallam University for the degree of Doctor of Philosophy by:

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To all my family, brothers and sisters

and to the souls of my parents

Declaration

The work described in this thesis was carried out by the author in the Materials and Engineering Research Institute, Sheffield Hallam University. The author declares that this work has not been submitted for any other degree. The work is original except where acknowledged by reference.

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Abstract

This thesis presents the electrical characterisation of defects in novel group IV semiconducting materials: semiconducting diamond and silicon germanium (SiGe) virtual substrates. Several methods to clean diamond surfaces are introduced, which lead to the fabrication of a diamond Schottky diode with acceptable characteristics. Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements were carried out to study the electrical properties of both the diamond and SiGe Schottky diodes. Deep level transient spectroscopy (DLTS) and Laplace DLTS were then carried out to investigate the deep electronic states in these devices. Scanning Electron Microscopy (SEM) was also used to investigate defects in the diamond samples.

For the diamond Schottky diodes, I-V and C-V measurements confirmed the quality of the fabricated Schottky diode; the measured phase angle between capacitance and voltage was close to 90° for temperatures greater than 300K and frequencies above 200 kHz and the device clearly exhibited rectification. DLTS and LDLTS measurements of the diamond did not show any signatures that could be attributed to isolated point defects. This could be due to the fact that it was necessary to take the samples to higher temperatures in order to fully ionize the boron in the sample. The boron acceptor is at 0.37 eV above the valence band and therefore only about 5% is ionised at room temperature. During the major part of the study at Manchester, there was no access to a high temperature cryostat. However, a clear capacitance transient was observed at lower temperatures and it is proposed that this is due to emission of holes from boron. Deep traps will be located deeper in the band gap than the boron. An additional problem was that the sample was of polycrystalline structure and is full of grain boundaries, which appear to be implicated in the leakage currents present in our devices.

I-V, C-V, DLTS and LDLTS were also used to investigate the deep states in the SiGe virtual substrate. I-V and C-V measurements showed that the SiGe Schottky diode showed some leakage (reported by the suppliers) but nevertheless the diode exhibited rectification. Analysis of the DLTS data showed the presence of a defect in the SiGe samples which could be a structural defect, probably dislocation-related. However, the low background doping meant that a considerable depth below the surface was being measured in DLTS and depth profiling was not possible.

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Chapter 1

Introduction

1.1 General introduction/statement of the problem

This research is centred around two novel and emerging technologies in electronic devices, namely new materials for power electronics, and the need for new designs to enable complementary metal oxide semiconductor (CMOS) scaling.

Silicon diodes presently used in power electronics are approaching their theoretical limits in that they lack both the high voltage capacity and power handling capabilities needed for high efficiency power electronic converters and systems. Progress is hampered by the nature of the materials used [Benjamin, 1997].

Strained silicon has higher carrier mobility than bulk silicon but needs to be grown on a substrate with a different lattice constant. One solution is to grow a graded SiGe layer and deposit Si on the top where the Ge can be as high as 30%.

Graded silicon germanium layers, usually called 'virtual substrates', are one industrial approach to producing strained silicon, but they are associated with higher-than-acceptable leakage currents. They often contain threading dislocations, because the layer progressively relaxes as growth continues.

Among other semiconducting materials, diamond has the widest band gap (5.5 eV) with considerable potential for high power throughput at high operating temperatures. However, it is only since about 1990 that the Chemical Vapour Deposition technique (particularly microwave plasma CVD) of growing diamond wafers on semiconductor substrates (e. g., silicon) has opened the door to practical applications of thin film

semiconducting diamond. Progress in the synthesis of high quality diamond films has made them a promising material for many specialised electronic device applications [Buckley-Golder and Collins, 1992; Ralchenko *et al*, 1999]. It is hoped that devices capable of operating at voltages in excess of 10,000 volts and at higher temperatures than other semiconductor materials may soon be available. This thesis is concerned with the fabrication of a working Schottky diode on semiconducting diamond and the testing of its properties for future commercial use.

1.2 Rationale for research

Diamond exhibits a rare combination of physical, optical and thermal properties that make it a very attractive material for many electronic applications. It is extremely hard, it is electrically insulating but can be made conducting, has the highest thermal conductivity at room temperature of any semiconducting material, and is transparent to electromagnetic waves from about 225nm to beyond the infra-red region. Because of these advantages this research attempts to develop a Schottky diode on thin film diamond, and studies the defects that are in the diamond by Deep Level Transient Spectroscopy (DLTS).

We illustrate the properties of diamond and discuss the different methods used for the production of synthetic diamond and conclude that the presence of defects in a diamond sample will have a great effect on the electronic behaviour of a device.

1.3 Research Aims and Objectives

The major aims of this research are two-fold:

(i) to fabricate a working diamond Schottky diode with acceptable characteristics, and

(ii) to study the defects in a strained silicon Schottky diode fabricated on a virtual substrate.

The objectives of the research programme are:

- To study certain novel group IV semiconductors and their applications.
- To study those defects in diamond that could have a significant effect on the electronic behaviour of the diamond, and to develop an analytical explanation of the behaviour of defects and the subsequent behaviour of the Schottky diode
- To study defects in virtual substrates.

- On the basis of the investigation conducted, to provide useful information to guide future research in this field.

1.4 Organisation of the thesis

This work is organized as follows:

Chapter 2 is concerned with the investigation of diamond growth and properties, and present a survey of different material systems used in power electronic devices.

Chapter 3 consists of a discussion and analysis of defects in diamond. It also illustrates the use of different techniques (such as temperature dependent current-voltage (I-V) characteristics and DLTS) for the investigation of the electronic behaviour of defects and traps in diamond.

Chapter 4 gives a brief account of defects in silicon and their consequences for the behaviour of silicon devices, as comparison.

Chapter 5 discusses briefly the metals used to fabricate a Schottky diode and illustrates how a Schottky diode is created when a metal is deposited on the surface of a semiconductor. It also introduces techniques for characterising a Schottky diode.

Chapter 6 gives a survey of the experimental techniques, including Laplace DLTS, used in investigating the electronic behaviour of the traps in semiconductors using a Schottky diode.

Chapter 7 introduces the fabrication of a Schottky diode on diamond.

Chapter 8 shows the experimental results obtained from the I-V and capacitance-voltage (C-V) measurements carried out on the fabricated diamond Schottky diode. The results of DLTS measurements are introduced in order to fully electrically characterise the fabricated diamond Schottky diode.

In chapter 9 we introduce a SiGe Schottky diode. We report its excellent characteristics and the experimental results. At the end of this chapter we introduce a comparison between a diamond Schottky diode and a SiGe Schottky diode from the point of view of the C-V measurements.

Finally, conclusions and suggestions for future work are given in Chapter 10.

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Chapter 2

Properties and growth of diamond

2.1 Introduction

Silicon diodes have been used in power electronics for many years and their properties and characteristics have been studied in great detail. The increasing proportion of electricity generated by power electronic converters in motor drives, high voltage dc systems, distributed energy resource interfaces, and flexible ac transmission, makes the efficiency and reliability of these converters of the utmost importance. Several of these applications require voltage-blocking capabilities in the tens and hundreds of kV and thus need series connection of many silicon-based power electronic devices to achieve the necessary voltage rating. Power electronic converters may process gigawatts of power between where that power is generated and where it is ultimately utilized, emphasizing the need for highly efficient power electronic converters and systems. All commercial power electronic devices (diodes, thyristors, etc.) are presently silicon-based, but the performance of these systems is approaching its theoretical limit. The development of new power electronic devices based on wide bandgap semiconductor materials would give substantial improvements in the performance of power electronics converter systems in terms of higher blocking voltages, efficiency and reliability as well as reduced thermal requirements [Ozpineci *et al*, 2002].

Modern power electronic devices have reached the point where progress is hampered by the nature of the materials themselves. For a given size, silicon transistors can only switch so fast, and new materials are needed for high speed switching applications. Similarly, silicon is a poor conductor and so thermally produced carriers

can cause conduction problems. In many high power, high frequency applications vacuum tubes are required, but these are bulky, inefficient and much more prone to failure than semiconductors. It would thus be advantageous to replace such tubes with semiconductors wherever possible and so new semiconductor materials for power device applications are needed [Benjamin, 1997].

Wide bandgap semiconductors like silicon carbide (SiC), gallium nitride (GaN), zinc oxide (ZnO), and diamond, with their superior electrical properties, are candidates likely to meet the enhanced requirements [Tolbert *et al*, 2003]. These materials are very attractive for certain applications, having many remarkable properties, such as high-temperature capabilities and higher threshold voltages, which make them very promising semiconductor materials for power electronics. However, the large-scale manufacturing of electronic devices requires continuous production of good quality wafers, which is currently a problem. For example, in silicon carbide growth there are still some basic problems that limit the commercial utilisation of the material [Raback, 1999] although recently much larger wafers of SiC have become commercially available.

So what are the advantages of wide bandgap materials? A bandgap is the amount of energy required for an electron to jump from the valence band to the conduction band. Wide bandgap materials have a bandgap energy of, typically, between 3-6 eV. A high bandgap energy gives a higher breakdown voltage, which in turn leads to higher power operation. Threshold voltages are greatly increased and there is a high output impedance because of high resistivity. Although wide bandgap semiconductor-based power devices have these advantages compared with silicon, manufacturing difficulties and other disadvantages limit their widespread use. These disadvantages include: low processing yield because of defects in SiC, processing problems with GaN and single crystal diamond, high cost and limited availability. Only SiC Schottky diodes of relatively low power are commercially available [Ozpineci, 2003].

Wide bandgap semiconductor materials have better electronic characteristics than silicon [see table 2-1 for some characteristics of the most popular wide bandgap semiconductors]. Among these diamond has the widest band gap. Because semiconductors with wide bandgaps can operate at higher temperatures, diamond power devices, potentially, have the capability to operate at higher ambient temperatures than

the other materials. Additionally, a higher electric breakdown field results in power devices with higher breakdown voltages. The breakdown voltage of a diode is expressed as [Raback, 1999, Ozpineci, 2003]:

$$V_B \approx \frac{\varepsilon_r E_C^2}{2qN_D} \qquad 2.1$$

where q is the charge of an electron, N_D is the doping density, ε_r is the dielectric constant and E_C is the electric breakdown field.

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.54
Dielectric constant, ε_r	11.9	13.1	9.66	10.1	9	5.5
Electric Breakdown Field, E_C (kV/cm)	300	400	2500	2200	2000	10000
Electron Mobility, μ_n (cm^2.V.s)	1500	8500	500	1000	1250	2200
Hole Mobility, μ_p(cm^2.V.s)	600	400	101	115	850	850
Thermal conductivity, λ(W/cm. K)	1.5	0.46	4.9	4.9	1.3	22
Theoretical breakdown voltage of material normalized to a silicon diode, using eqn 2.1 (same doping assumed)			56	46	34	514
Saturated Electron Drift Velocity, V_{sat} (x10^7cm/s)	1	1	2	2	2.2	2.7

$\varepsilon=\varepsilon_r\varepsilon_o$ where $\varepsilon_o = 8.85 \times 10^{-12}$ F/m, ε_r = relative permittivity.

Table 2-1 Physical characteristics of silicon and common wide bandgap semiconductors [Raback, 1999, Ozpineci, 2003].

Using equation 2.1, the breakdown voltages of diodes made of the materials in table 2-1 were calculated assuming the same doping density, and the results are shown normalized to the breakdown voltage of a silicon diode. The theoretical breakdown voltages for 6 H-SiC, 4H-SiC, and GaN are respectively 56, 46, and 34 times that of a silicon diode; but for diamond it is 514 times greater. Tolbert *et al,* [2003] have noted that with higher electric breakdown fields, a greater doping density can be introduced in the material than in silicon. This will further increase the breakdown field of the wide bandgap semiconductor diodes.

Another consequence of the higher breakdown field and higher doping density is a width reduction in the drift region of the devices. The required width of the drift region can be expressed as [Raback, 1999, Ozpineci, 2003];

$$w(V_B) \approx \frac{2V_B}{E_C} \qquad 2.2$$

A plot of the drift region width versus the breakdown voltages for different types of semiconductors can be seen in figure 2-1 for a breakdown voltage range of 100 to 10,000 V. Diamond, as expected, requires the minimum width while 6H-SiC, 4H-SiC, and GaN follow diamond in order of increasing width. Compared to these, silicon requires approximately a 10 times thicker drift region [Tolbert *et al*, 2003].

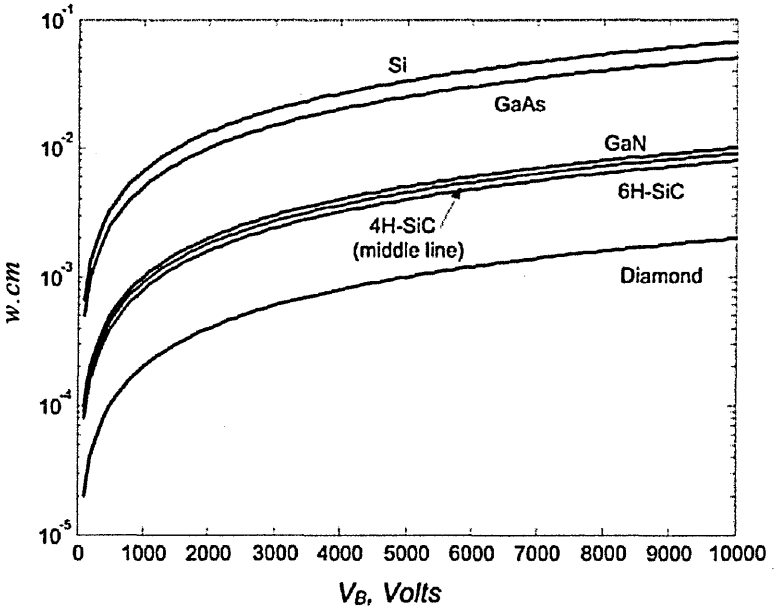

Figure 2-1 Width of the drift region for several common materials at different breakdown voltages [Ozpineci *et al*, 2002].

Silicon carbide, gallium nitride, zinc oxide and diamond will be discussed in the following sections.

2.1.1 Silicon carbide

Silicon carbide (SiC) is a wide bandgap semiconductor currently of interest to the semiconductor device industry for use in high temperature, high power voltage, and high frequency devices and sensors [Silly *et al*, 2004]. In particular it possesses an

electrical field strength one order of magnitude larger than that of silicon, a bandgap of 2.9 eV, and a high thermal conductivity. Silicon carbide is hard, has high heat resistance, strong oxidisation and a small thermal coefficient, which makes it favoured for many technical applications [Werhiet and Schwetz, 2004]. Silicon carbide is also very resistant to radiation damage [Cheng *et al*, 2002. Silly *et al*, 2004]. Silicon carbide occurs in many different crystal structures; more than 200 different polytypes. SiC-4H and SiC-6H have the same basic parameters including their crystal structures (Wurtzite (Hexagonal)), melting point (3103 ± 40 K at 35 atm), and density (3219 gcm^{-3} at 300 K) [de Mesquita 1967; Harris and Weiner, 1989]. SiC exhibits a higher value of thermal conductivity (3 to 13 times), critical electric field (4 to 20 times), and saturated carrier velocity (2 to 2.5 times) compared to conventional semiconductor materials such as silicon, germanium and gallium arsenide [Lee, 2002].

Schottky diodes constructed from silicon carbide are stable to high temperatures, but there are still a number of factors that limit device performance. One of the most important and critical factors is the formation of low resistivity Ohmic contacts [Lee, 2002]. For applications in silicon-compatible technology, a new process at a lower temperature is required. Furthermore, SiC has a large lattice mismatch to silicon, making it difficult to achieve good performance from heteroepitaxial growth [Kiuchi *et al*, 2004].

2.1.2 Gallium nitride

Gallium nitride (GaN) has some of the advantages of SiC; a direct wide bandgap, high thermal conductivity, and relatively good high frequency performance, so applications of GaN devices have mainly focused on short wavelength optoelectronics and radio frequency uses. GaN and SiC Schottky diodes show similar performance advantages (at similar blocking voltages) compared to Si pn junction diodes. There is a negligible reverse recovery current and consequently a lower switching loss that is independent of the operating temperature. The switching speed and losses of GaN Schottky diodes have been shown to be slightly better than similarly rated SiC diodes. On the other hand, because of its wider bandgap, the forward voltage drop of a GaN Schottky diode is much higher than both Si and SiC Schottky diodes [Ozpineci *et al*, 2002].

GaN does have some disadvantages compared to SiC; for example, it does not have a native oxide, which is required for MOS devices. Studies are underway to find a suitable oxide since without it GaN MOS devices are not possible. Also, with present technology, GaN boules are difficult to grow, so pure GaN wafers are not available; instead GaN wafers are grown on sapphire or even SiC. Even then, thick substrates are not commercially available. As a consequence, GaN wafers are more expensive than SiC wafers [Ozpineci *et al*, 2002]. Another disadvantage compared to SiC is its thermal conductivity, which is almost one quarter of that of SiC. This property is crucial in high power, high temperature operation because the heat generated inside the device needs to be dissipated as quickly as possible. The higher the thermal conductivity, the quicker the heat is dissipated. Growing GaN on SiC wafers increases the overall thermal conductivity but it still does not reach the performance of SiC [Ozpineci *et al*, 2002]. Undesired screw dislocations are observed in gallium nitride films, although they are reduced by growing on a vicinal surface [Goorsky, 2002; Wulfhekel *et al*, 2004].

Bandgap engineering, through alloying and heteroepitaxial annealing has enabled systems with a broad range of applications. High breakdown electric field and electron saturation velocities make the system suitable for high power applications, as does its overall thermal robustness. Applications, however, require the use of GaN substrates because heat dissipation is a problem when sapphire substrates are used [Arulkumaran *et al*, 2002, Goorsky, 2002]. Finally, GaN and SiC wafers are, relatively, very expensive.

2.1.3 Zinc oxide

Zinc oxide (ZnO) has a wide bandgap (3.4 eV) but it has not received the same attention as SiC and GaN, probably because this material has been perceived as being useful only in its polycrystalline form in such diverse areas as facial powders and sun cream. Recently, however, large area bulk growth has been achieved, and furthermore, several epitaxial methods have produced excellent material. Also, quantum wells have been successfully grown, by alloying with other materials. Thus ZnO is now being proposed for the same applications as those listed above for GaN, SiC, and diamond. In fact, ZnO recently exhibited several fundamental advantages over its chief competitor; renewed interest in ZnO culminated in the first international Workshop on ZnO in 2000 [Look, 2001]. In general, the electrical properties of bulk ZnO are excellent, as might

have been expected from the low background impurity concentrations. However, good electrical properties also demand low point defect and dislocation concentrations, and bulk ZnO also excels in these aspects. So far, it has proved difficult to dope ZnO p-type, although thin film results look promising [Look, 2001].

2.1.4 Diamond

Diamond is a metastable form of carbon in which each carbon atom is tetrahedrally sp3 bonded to its four nearest neighbours. This strong bonding is responsible for a number of unique physical and chemical properties [Field, 1992, Prawer and Kalish, 1994].

Diamond shows the best theoretical performance, with several times the improvement in every power electronics category compared with every other wide bandgap semiconductor. However, its processing problems have not been solved yet. SiC also still has processing problems, even after years of research, because of the high temperatures required in the process; diamond is a mechanically harder material, needing even higher temperatures for processing, and much research has yet to be done on its processing before it can be used commercially [Ozpineci *et al*, 2002].

Diamond has amazing properties: because of its fundamental material parameters such as critical field for avalanche breakdown, it has potentially high power throughput and high operational temperature. Also many of its properties are extreme, such as being the hardest solid and the best thermal conductor at room temperature, but, as yet, the electronic applications have been quite limited. Because of diamond's corrosion and radiation resistance, and its stability at high temperatures and pressures, a variety of applications are possible [Mainwood, 2000].

The ability to synthesise diamond from methane and other hydrocarbons (i.e., by Chemical Vapour Deposition) and to deposit the diamond on semiconductor substrates (e. g., silicon) opens many technological applications. Semiconducting diamond exhibits a unique combination of electrical, optical, and physical properties, e. g., low thermal impedance, low dielectric constant, high strength, excellent corrosion resistance, high breakdown voltage, radiation hardness, high saturated carrier velocities at high electric fields, and optical transparency over a wide frequency range [Moazed *et*

al, 1988; Geis *et al*, 1987]. These properties have led to considerable interest in the use of this material for high power and high temperature electronics [Chan *et al*, 1995; Gildenblat *et al*, 1991; Shenai *et al*, 1989]. In addition, the wide band gap should also make diamond significantly immune to the effects of ionising radiation as compared to other common semiconductors. Successful operation of active electronic devices at elevated temperatures as high as 400 °C indicates the potential of this material. Diamond is an ideal substrate material for electronic packaging because of its properties outlined above [Menon and Dutta, 1996, Pickrell *et al*, 1993]. However, diamond is difficult to metallize for two reasons:

1. The surface of diamond is relatively inert, making it difficult for common, non-carbide forming, metallisation with high electrical conductivity.
2. Its thermal expansion coefficient is very small (~ 1-2× 10^{-6} /K), resulting in large interfacial residual stresses between the substrate and the metallisation [Menon and Dutta, 1996].

Electrical contacts, especially Ohmic contacts, are an essential topic to be studied for the application of diamond films for electronic devices [Wang *et al*, 2002]. The metallization is used to ensure good Ohmic contacts to electrically active areas on the diamond sample. For all cases the adhesion of the metallization on the sample surface has to be very good. To fulfil all these conditions a three layer metal system is used. At first a titanium layer is deposited by sputtering. Titanium shows good adhesion to diamond because of the formation of a carbide layer at elevated temperatures. To avoid oxidation of the titanium layer a platinum layer is deposited on the top of the titanium layer which acts as a diffusion barrier. Lastly, to make soldering and, later, bonding feasible a gold layer is deposited on top of the platinum.

The thermal conductivity of diamond is two to three times better than copper or silver [Ono *et al*, 1986], which makes diamond films extremely attractive candidates for use as dielectrics in conjunction with common semiconductors [Narayan *et al*, 1988]. By far the most successful method for depositing diamond films is Chemical Vapour Deposition (CVD) [Jones *et al*, 2003]. Moreover, CVD diamond films show very interesting properties, including negative electron affinity (NEA) and extreme mechanical strength [Van der Weide *et al*, 1994].

Although high-quality polycrystalline diamond has many properties that approach those of the best natural diamonds now commercially available, the presence of grain boundaries impedes electronic performance, so that the only option for the most demanding electronic applications is single-crystal CVD diamond. The best material suitable for electronic applications that has been reported is thin-layers (typically <<100 μm) with electronic properties, such as carrier mobility and lifetime, similar to those measured in specially selected natural type IIa diamond [Isberg *et al*, 2002]. In homoepitaxial boron-doped CVD diamond, Yamanaka *et al*, [1999] have measured a Hall hole mobility of 1840 cm^2/Vs. Improvement in electronic properties such as carrier mobility and lifetime can be directly related to enhanced crystalline quality and reduced defect (point and extended) concentration, because the carrier mobility is limited by defect-scattering mechanisms [Isberg *et al*, 2002].

Because diamond has a high breakdown voltage, high thermal conductivity, and high carrier saturation velocity, its low dielectric constant makes it useful for fast switching operation, and diamond's high resistivity makes it possible to apply a high dc bias field to a device. Natural diamond exhibits electrical resistivities of the order 10^{16} Ω cm before doping [Landstrass and Ravi, 1989], whereas diamond films, synthesised by CVD techniques, display relatively low resistivities, of the order of 10^6 Ω cm, in the as-synthesised condition as a result of hydrogen passivation of deep traps in the films. The resistivity of these films can be increased by several orders of magnitude by annealing the films in a neutral ambient to expel the hydrogen [Landstrass and Ravi, 1989]. In the case of diamond films, hydrogen passivation is a natural consequence of the synthesis process since the presence of atomic hydrogen in the plasma ambient is a necessary requirement for the promotion of diamond (sp3) bonding and the suppression of graphitic (sp2) bonding in these films [Deragin *et al*, 1969; Spitsyn *et al*, 1981; Landstrass and Ravi, 1989]. In 1997 Watabanabe *et al*, successfully synthesised high-quality diamond films with an atomically flat surface using a low CH_4 concentration in a mixture of CH_4/H_2 gas [Watabanabe *et al*, 1997; Okushi, 2001].

Progress in the synthesis of high quality diamond films by CVD makes diamond films a promising material for many specialised electronic device applications [Buckley-Golder and Collins, 1992; Ralchenko *et al*, 1999], and semiconductor diamond is also considered as a key material in the field of Schottky barrier theory [Davies, 1979]. While homoepitaxial diamond films can facilitate the development of

electronic devices, the high cost and limited availability of large-area natural or synthetic single-crystal diamond substrates would make commercialisation of such structures difficult. Unfortunately most CVD diamond films currently grown on economical, non-diamond substrates are polycrystalline [Polyakov *et al*, 2001]. Until the beginning of 1980, natural or high-pressure high temperature (HPHT) synthesized diamond, especially the rare type IIb diamond, was used for investigations of semiconductor properties [Gies *et al*, 1987], however, the success of CVD diamond has opened up study of this field [Spitsyn *et al*, 1981; Hicks *et al*, 1989; Kawarada *et al*, 1994].

The electronic transport of CVD diamond films is affected by both the surface and the bulk electronic properties. Surface-related electronic properties can be changed by hydrogen termination of the films, the conductance drastically increases (typically to 10^{-4} S) [Landstrass and Ravi, 1989; Albin and Watkins, 1990; Looi *et al*, 1999], and the surface itself exhibits p-type conduction [Mijto *et al*, 1991]. Surface effects are further discussed later in this chapter. The films can be doped with boron to behave as (bulk) p-type semiconductors. Ongoing investigations indicated that n-type doping might be possible with phosphorus [Koizumi *et al*, 1998; Cannaerts *et al*, 2002].

Because diamond was the material chosen for investigation in this project, the following section discusses properties and classification of diamond, and discusses different techniques for growing diamond films.

2.2 Classification of diamonds

Diamonds are defined as either natural or synthetic, natural diamond can be found in the earth's crust while synthetic is grown in a laboratory by different techniques and for different applications.

2.2.1 Natural diamonds

Natural diamond is formed deep under ground by heating carbon to high temperatures under extreme pressure. This process forms the basis of the so-called HPHT growth technique [Field, 1992], which has been used to produce 'industrial diamond' for several decades. The diamond crystals produced using HPHT are used for a wide range of industrial processes, which use the hardness and wear resistance

properties of diamond in mechanical components, and for polishing and grinding in optics [May, 2000].

Natural diamond does not contain any hydrogen. Consequently, if the observed high resistivity of natural diamond is a result of traps resident deep in the band gap of the material, then hydrogen passivation of these traps should lead to a reduction of the resistivity of the crystals as in the case of hydrogenated films synthesised by plasma-enhanced chemical vapour deposition (PECVD) techniques [Landstrass and Ravi, 1989].

Natural diamond is classified by the type and level of impurities found within it:

1. Type Ia diamond- Nearly 99.9 % of diamonds occurring naturally are Ia. These have high concentrations of nitrogen (up to 0.3 %), which is concentrated in various aggregates in the crystal.

2. Type Ib diamond is rare, only about 0.1 % of diamonds occurring naturally are this type. However, most synthetic (industrial) diamonds are of this type, having an even distribution of nitrogen atoms substituted for carbon atoms in the lattice. The concentration of nitrogen is up to 500 ppm (0.05 %).

3. Type IIa diamond is very rare in nature. There is very little nitrogen in these diamonds ($<10^{18}$ cm^{-3}), and the nitrogen is not easily detected by the usual infrared (IR) or ultra-violet (UV) absorption measurements because the concentration is so low.

4. Type IIb diamond is also extremely rare in nature. The concentration of nitrogen is very low (even lower than type IIa) and the crystal may be a p-type semiconductor because it can contain uncompensated boron acceptor impurities to a level of about 10^{17} cm^{-3}.

While types IIa and IIb are very rare in nature, they can be synthesized industrially.

2.2.2 Synthetic industrial diamonds

There are no substantial differences between natural and synthetic diamond in terms of their thermal or electrical conductivity. Type Ia diamond has a thermal conductivity about twice that of copper, type IIa diamond has a thermal conductivity about 5 times greater than that of copper, while type IIb diamond can exhibit significant electrical conductivity, passing currents of many mA through 1 mm Schottky diodes.

There is much effort underway to develop new applications that utilise diamond's properties, including use as an active semiconductor material in electronic devices. Typically, for thin film semiconductors, diamond films are produced by the CVD process which offers the possibility of producing a high purity, single crystal diamond that is economically suitable for industrial applications. Single crystal diamonds for industrial applications should be at least 0.25 mm thick, while a thickness of 0.5 mm and 1.00 mm allows for broader application [Linaress and Doering, 1999].

Natural IIb diamond contains small amounts of boron in substitutional sites that cause it to become a p-type semiconductor. In a similar manner, boron can be incorporated into a CVD single crystal diamond by the addition of a gaseous boron compound into the growth chamber. Because the growth conditions are highly controlled, the boron can be incorporated over a wide range of values and predictable electrical properties obtained. Presently it is possible to grow structures that contain layers of differing electrical properties, which makes possible the production of unique semiconductor and industrial devices, for example diodes whose electrical resistivity can be varied from less than 1Ω cm to over 1000 Ωcm, while maintaining good crystal quality. Methods of producing synthetic diamond will now be explained.

2.3 Methods for production of synthetic diamond

There are many CVD techniques used to synthesise diamond including: Hot Filament, Microwave Plasma, dc Plasma, and rf Plasma. The two classes of methods currently used are HPHT, and CVD. Diamond films grown by hot-filament or plasma-assisted CVD are of most interest to this thesis [Grot *et al*, 1991; May, 2000].

2.3.1 High-Pressure-High-Temperature growth

Synthetic diamond has been produced for the past 50 years using HPHT technology. HPHT subjects graphite to conditions similar to those under which natural diamonds are formed in the earth's mantle. Most large gem quality synthetic diamonds are grown using variants of this method. The most successful technique involves growing the diamonds in a 'flux' of molten alloy. Natural diamond crystals most often grows on octahedral {111} faces, though growth on cubic {100} faces is also seen. Synthetic diamonds for industrial use have been made since the early 1950's, by the HPHT process. In this process, graphite is put into a large hydraulic press, to be compressed to tens of thousands of atmospheres, heated to over 2000 K in the presence of a suitable metal catalyst which converts graphite to diamond over a period of a few hours. The diamond crystals that are produced by this method are typically a few mm in size. However, they are extremely useful as hard wearing edges on cutting tools and drill-bits. The drawback of the HPHT method is that it produces diamond in the form of small crystals ranging in size from nanometres to millimetres, and this limits the range of applications for which it can be used. What is required is methods to produce diamond in a form that can allow many more of its superlative properties to be exploited, in other words, as diamond thin film [Bundy, 1980; Field, 1992, May, 2000]. Figure 2-2 shows the conditions of pressure and temperature where diamond and graphite will be a stable form of carbon.

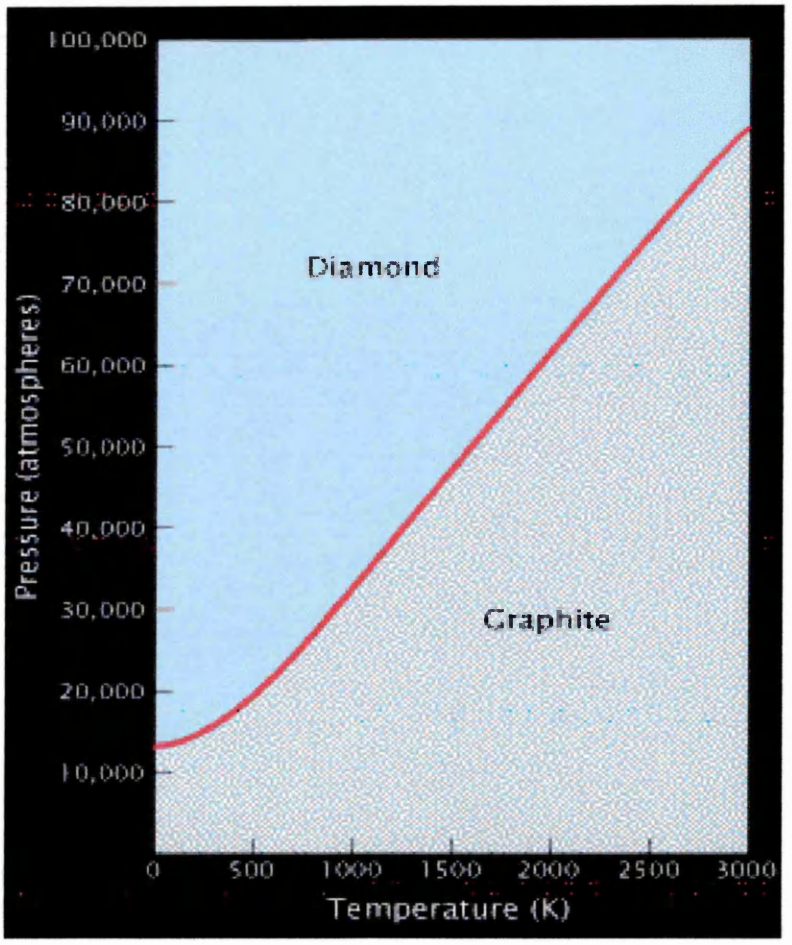

Figure 2-2 The conditions of pressure and temperature required to form diamond and graphite from carbon [American Museum of Natural History, 2004].

2.3.2 Chemical Vapour Deposition

CVD produces thin films of diamond which were originally used for optical windows but recent applications include developing novel power electronic devices, as the layers can be heavily doped with boron. The complex chemical and physical processes which occur during diamond CVD have several different but interrelated features. The process gases first mix in the chamber before diffusing toward the substrate surface, see figure 2-3. En route, they pass through an activation region such as a hot filament or electrical discharge (dc or rf) causing microwave plasmas, or a combustion flame such as an oxyacetylene or plasma torch, which provides energy to the gaseous species. As a result, molecules are fragmented into reactive radicals and atoms, creating ions and electrons and heat the gas up to temperatures approaching a few hundred Kelvin. Beyond the activation region, these reactive fragments continue to mix and undergo a complex set of chemical reactions until they strike the substrate surface. Two things could happen at this point: firstly; the species may adsorb then react

with the surface, subsequently desorbing again back into the gas phase, or secondly, diffuse around close to the surface until an appropriate reaction site is found. If a surface reaction occurs, one possible outcome, if all the conditions are suitable, is diamond [May, 2000].

This technique of CVD growth involves the deposition of layers of carbon onto a given substrate and is particularly useful as the only limitation on the size of crystal is the substrate, and dopants may be introduced with relative ease. The growth of single crystal diamond is possible if a homoepitaxial technique is applied, although polycrystalline crystal growth is the most understood and commonly used method [Wotherspoon *et al*, 2002].

Figure 2-3 shows some reactors which are used for deposition of synthetic diamonds. Features are shared by the most commonly used experimental methods but they differ in detail. Growth of diamond (rather than graphite) normally requires that the principal gas (usually methane, CH_4) is diluted with an excess of hydrogen, typically with a ratio of 1% by volume of CH_4, and the temperature of the substrate is usually more than 973 K [May, 2000].

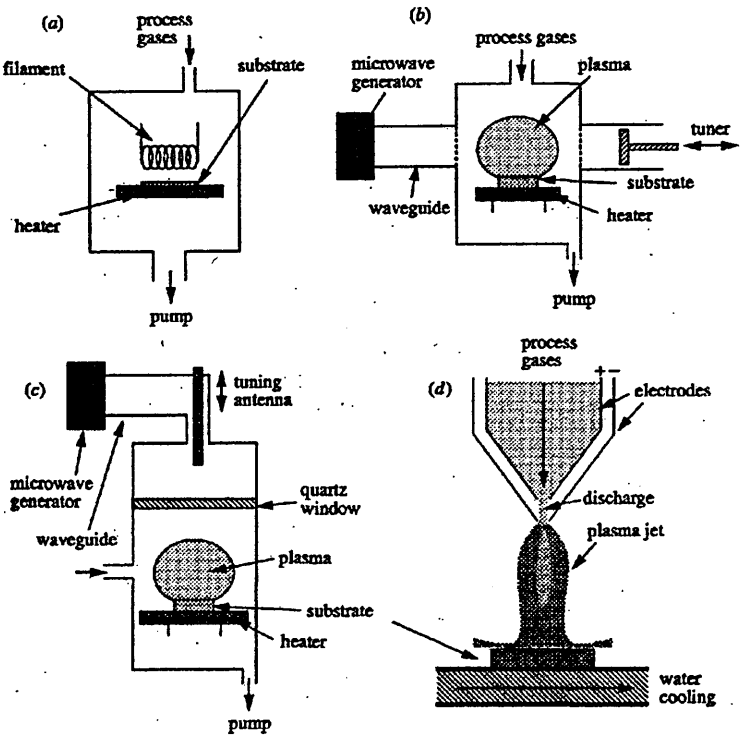

Figure 2-3 Examples of the more popular types of low pressure CVD diamond reactors; a- Hot filament, b- National institute for research in inorganic materials "NIRIM-type" microwave plasma reactor, c- Applied science and technology exchange "ASTEX-type" microwave plasma reactor, d- dc arc (plasma torch) [May, 2000].

Figure 2-3 (a) shows CVD using a hot filament reactor. A rotary pump is used to continuously pump the chamber to a pressure of, typically, between 20-30 Torr. The process gases are introduced at carefully controlled rates of a few hundred sccm. The temperature of the substrate (e.g. a slice of silicon) to be coated can be raised from 973 to 1173 K using throttle valves.

This system is cheap and easy to use and operate, to produce reasonable quality polycrystalline diamond films, depending upon exact deposition conditions. It is particularly sensitive to oxidising or corrosive gases, which limit the variety of gas mixtures which can be employed, and it is very difficult to avoid contamination of the diamond films with filament material. Metallic impurities at the tens of ppm level are unacceptable for electronic applications but it can be used in mechanical applications [May, 2000].

Figure 2-3 (b) shows a microwave plasma CVD NIRIM reactor which uses similar conditions to the hot filament CVD. In this reactor, a quartz discharge tube is inserted through the side of the principle mode rectangular tuned wave-guide appropriate for the propagation of 2.45 GHz microwaves. The maximum electric field is arranged to be centred in the middle of the discharge tube, where stable plasma is created. The substrate is introduced from the bottom of the discharge tube. This method is more expensive, but it is among the most widely used techniques for diamond growth.

Figure 2-3 (c) shows a microwave CVD that uses an ASTEX-type reactor, which is the most common type. Through a quartz window, microwaves are coupled with a water-cooled metal cavity. The inner chamber diameter is chosen so that only one microwave radial mode can be sustained in the cavity at 2.45 GHz. Positioned on a heated stage beneath the plasma ball, substrates as wide as 10cm in diameter can be coated. The advantages of a microwave system are high power and high growth rates and they can also use a wide variety of gas mixtures, including mixtures with high oxygen contents or ones containing chlorinated or fluorinated gases [May, 2000].

In figure 2-3 (d) a plasma jet is used in plasma CVD. The direct current arc jet drives high currents through the ionised flowing process gases. Plasma jet, arc jet or plasma torch methods are promising alternatives to the more conventional low-pressure high frequency and microwave systems. In the plasma jet, gas at relatively high flow rates passes through a high-power electrical discharge and forms a jet of ionised particles, atoms and radicals, which then expand into a secondary chamber to strike a substrate at high velocity. The pressure within the secondary chamber usually distinguishes plasma jets, which can be 100 torr to 1 atm. The high growth rate of diamond that can be achieved is the main advantage of the plasma jet system. It has produced the highest diamond growth rates, reported greater than 900 μh^{-1} [Othake and Yoshikawa, 1990; May, 2000], which is nearly three orders of magnitude higher than most CVD techniques [May, 2000].

There are other techniques of depositing of diamond which have been used to grow diamond films with variety degrees of success, including pulsed laser deposition, hydrothermal growth, and laser-assisted CVD [Dischler and Wild, 1998; May, 2000].

Under growth conditions of low CH_4 partial pressure and low substrate temperature, most of the CVD diamond films reported to date have been grown on single crystal silicon wafers, but this is by no means the only possible substrate material. Of course the substrate must have a melting point higher than the temperature window (1000-1400 K) required for diamond growth [Spear and Dismukes, 1994; May, 2000].

The addition of oxygen to the reactant gases, as either O_2 or alcohols, has a large effect on the quality and growth rates of CVD diamond films. Depending on its concentration, O_2 can either increase or decrease the diamond growth rate. The effects of O_2 on diamond growth have been attributed to any or all of four phenomena [Belton and Schmieg, 1991]:

a- Destruction of gas phase pyrocarbon-forming species.
b- Formation of different radicals in the gas phase.
c- Enhanced etching of non-diamond carbon on the surface.
d- Creation of different or more active surface species.

Experiments by Harris and Weiner [1989] examined the effects of oxygen on the concentration profiles of the gas phase reactants, which arrive at the growing diamond surface. Using a combination of mass spectrometry, gas chromatography, and a chemical kinetics model, it was concluded [Belton and Schmieg, 1991]:

a- Hydrocarbon species (likely to form pyrocarbons and/or diamond) are reduced somewhat by oxygen addition.
b- Oxygen has a relatively small effect on the mole fractions of radical species such as hydrogen H and CH_3.
c- OH is formed at concentrations sufficient to remove non-diamond carbon at rates comparable to the rate of diamond growth.

2.4 Negative electron affinity effects on the diamond surface

Negative-electron-affinity (NEA) surfaces are semiconductor surfaces that have a work function such that the vacuum level lies below the conduction-band edge. Electrons present in the conduction band can therefore readily escape the surface. NEA surfaces are utilized in a number of important applications, such as photocathodes,

secondary electron emitters and cold-cathode emitters. In general, wide-band-gap semiconductors are particularly suitable candidates for NEA emitters, since the conduction-band minimum is likely to be close to the vacuum level. Figure 2-4 shows the electron affinity of the first 20 elements in the periodic table [Emsely, 1988].

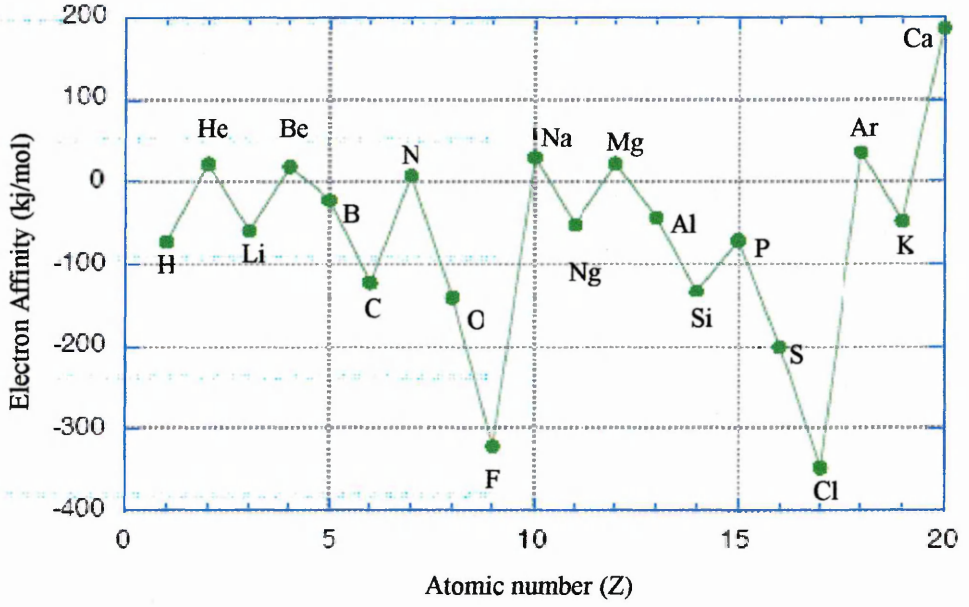

Figure 2-4 Electron affinity values for the first 20 elements [Emsely, 1988].

NEA surfaces of semiconductors are attracting renewed interest because they impact a broad class of important optoelectronic devices including field emitters and photometers. When band gap radiation excites electron-hole pairs near the surface, the electron can be emitted spontaneously from a NEA surface, resulting in a directed electron beam that is readily controlled with applied fields. Experimentally, NEA behaviour means simply that electrons at the bulk conduction band minimum are emitted from the surface. More often, NEA surfaces result from organic solids or form semiconductor surfaces covered by molecules or metals [Rei Vilar *et al*, 1988; Pickett, 1994].

Photoemission is a highly sensitive tool to determine the presence of NEA. Excited electrons from the valence band into various conduction band energy levels lose energy through inelastic collision processes and accumulate in levels at the conduction band minimum. At a NEA surface, the vacuum level lies below the conduction band

and the electrons accumulated at the conduction-band are emitted into the vacuum. These electrons appear in the photoemission spectra as a sharp peak at low electron energies. The position of the peak can be correlated with other features in the photoemission spectra to verify that the emission originates from the conduction band minimum.

A NEA has been demonstrated for the diamond {111} surface [Himpsel *et al*, 1979], and theoretical calculation associate this with the presence of hydrogen bonded to the surface [Pate, 1986; Pate *et al*, 1982; Van der Weide *et al*, 1994]. Moreover, PEA was obtained on the diamond {100} surface by annealing a polished and chemically cleaned surface at 10~100°C. This resulted in desorption of oxygen. It was found to be possible to prepare a NEA on a CVD grown diamond {100} surface without high temperature annealing, and it was suggested that the surface might exhibit a NEA during or immediately after growth. Many more NEA emitters are likely to be found as the methods for CVD growth of wide band gap semiconductors are improved. Photoemission experiments provide unambiguous evidence of the existence of NEA in diamond, and can be used both to calibrate the theoretical findings and to verify the actual occurrence of NEA [Van der Weide *et al*, 1994].

Surface band bending is another important aspect that affects electron emission from diamond surfaces. Depending on the sign and magnitude, the surface potential can, for example, effectively suppress the diffusion of electrons or holes to the surface. This surface potential is the difference between the Fermi level position at the surface and in the bulk of the sample. The latter is determined by doping and compensation of the material, and it is thus the energy at which the Fermi level is fixed at the surface potential. The reported values of the surface Fermi level position (E_F - E_V), where E_V is the valence band, for diamond is scattered between 0.2 and 0.8 eV for as-polished or hydrogen-plasma-treated surfaces and between 0.8 and 1.6 eV for hydrogen-free reconstructed surfaces [Bandis and Pate, 1995]. There is a general agreement that annealing the sample at high temperature results in a large change in band bending accompanying the hydrogen desorption and surface reconstruction [Cui *et al*, 1999].

The typical band scheme of a semiconductor surface is shown in figure 2-5 (a) where the vacuum level lies above the conduction band minimum creating an energy barrier. If the vacuum level lies below the conduction band minimum energy at the

surface, a NEA surface is produced, as shown in figure 2-5 (b). This reduction in the electron affinity together with a short characteristic band bending length (due to heavy p-doping) results in an effective negative electron affinity surface. A NEA semiconductor surface makes it possible for bulk conduction band electrons with kinetic energies as low as the conduction band minimum to escape into the vacuum [Bandis and Pate, 1995].

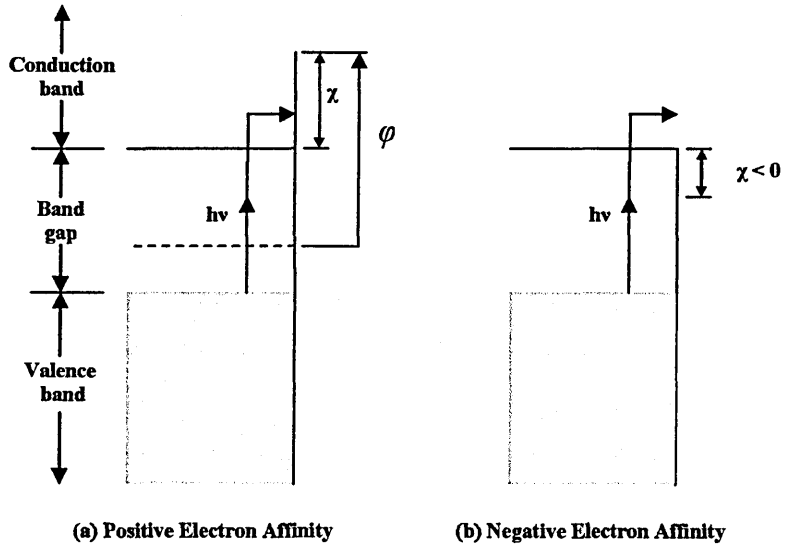

Figure 2-5 Shows the electron affinity band diagram; (a) PEA, (b) NEA [Bandis and Pate, 1995].

In principle, the relationship between the electron affinity, (χ), the work function of the material (φ), and the surface Fermi level position, (E_F), can be expressed as:

$$\chi = \varphi - (E_c - E_F) = \varphi + (E_F - E_V) - E_g \qquad 2.3$$

Where E_g is the band-gap energy of diamond, and E_V and E_C are the energies of the valence and conduction band edge respectively. If the values of the work function, (φ), and Fermi level position are known, the electron affinity, χ, can be determined via Equation 2.3. *hv* is the energy of the photon.

Eimori *et al*, [1994] reported that the electron affinities of hydrogen and oxygen adsorbed diamond surfaces were negative and positive respectively, from the result of photoyield spectra using ultraviolet synchrotron radiation light. Moreover, Van der Weide and Nemanich, [1993] reported that the diamond surface has positive electron

affinity after removing hydrogen atoms from the surface by argon plasma exposure. These reports indicate that the affinity of the diamond surface is governed by the species of adsorbed atoms. Therefore, it is necessary to terminate the diamond surface with hydrogen atoms for electron emission [Show *et al*, 1998].

Experimental results of Garrido *et al*, [2002] have shown that carbon-hydrogen dipoles formed at the diamond surface by hydrogenation treatment give rise to a NEA of –1.3 eV. This NEA together with the presence of a surface adsorbate layer which provides empty acceptor states for valence band electrons gives rise to an electron transfer from the diamond into the adsorbate layers [Maier *et al*, 2000]. As a consequence, an upward band bending is induced at the hydrogen-terminated diamond surface, and a narrow hole accumulation layer is created directly at the surface [Nebel *et al*, 2001], with a Fermi level position (E_F) about 0.9 eV below the valence band maximum (VBM) [Garrido *et al*, 2002]. This situation is completely changed when aluminium is deposited on the hydrogen-terminated surface. Garrido *et al*, [2002] established that the NEA is still present due to the carbon-hydrogen surface bonds, but no electron transfer from the valence band is expected since there are no empty states in the aluminium. Using published values for the work function of aluminium (4.28eV) [Petrosyan and Shik, 1989], and taking into account a NEA of 1.3 eV [Maier *et al*, 2000], it is possible to estimate the position of Fermi level at the aluminium/diamond interface to be just at or slightly below the valence band maximum of diamond. In this situation no hole accumulation is generated at the surface [Garrido *et al*, 2002].

2.5 Summary

In summary, this chapter is concerned with the investigation of diamond growth and the properties of diamond. The chapter can be broken down into four parts: the first part gave an introduction to the different materials used in power electronic devices, such as; SiC, GaN, ZnO and diamond, in the second part the properties and classification of diamond are discussed, the third part illustrates the different methods used for the production of synthetic diamond and, due to its effects on the diamond surface, NEA was extensively discussed in the final part.

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Chapter 3

Impurities and defects in diamond

3.1 Introduction

Following the development of techniques for the growth of good quality diamond films, diamond has the potential to become an important material for electronic devices. However, since heterogeneous growth of diamond films using CVD techniques results in various impurities and defects being incorporated in the films, so there has been a consequent growth of interest in the effect of impurities in diamond. The understanding of the behaviour of such impurities is essential in the search for a possible n-type dopant, which is essential for device applications.

More than 30 years of research on defects in natural and HPHT synthetic diamond has helped to characterise diamond produced by CVD. Nitrogen is the most common impurity in natural diamond, but hydrogen and boron are also detected. In HPHT diamond, nickel or cobalt complexes are also seen. Some native defects can be identified through irradiation which produces self interstitials and vacancies which are seen close to the growth surfaces of particularly good quality CVD diamonds, although they are not present in the bulk of the diamond [Mainwood, 1999].

3.2 Defects in semiconducting diamond

A defect can be defined as any configuration which rises to an electronic state near the Fermi level [Robertson, 1986; Robertson and Oreilly, 1987]. In a fully sp3 bonded network, the defects can be regarded as isolated sp3 sites or 'dangling bonds' [Robertson, 2001]. In the case of dopants, a small percentage of foreign atoms are added

into the regular crystal lattice of diamond which produces dramatic changes in its electrical properties. The main electrically active impurities in diamond are nitrogen and boron [Vavilov, 1997]. Nitrogen in diamond forms very deep (E_C - 1.7 eV and E_C - 4.0 eV) donor levels, and for this reason diamond doped with nitrogen is not of much interest for electronic applications. The most suitable impurity to control the conductivity of diamond is boron, which forms a rather shallow (E_V - 0.37 eV [Bezrukov, 1970]) acceptor centre in this semiconductor.

The self-interstitial and the vacancy in the group IV semiconductors also have unique properties among defects in crystals in which are composed entirely of atoms of one atomic species [Davies *et al*, 2001]. A major challenge in large gap semiconductors lies in improving the knowledge of the defects and their electrical effects. Either point defects such as foreign atoms, vacancies and their complexes, or extended defects such as those found at interfaces, generally have a detrimental effect on the electronic properties of the semiconductor. Most of them appear as deep levels in the forbidden band gap [Muret *et al*, 1999].

Because many defects are electrically active, behaving as trapping or recombination centres, detailed information about the defect states (including deep levels) is needed in order to fully understand the behaviour of semiconducting diamond devices. A dominant trap level is obtained from the temperature dependence of diamond film current-voltage (I-V) characteristics [Nath and Wilson, 1996], but further studies of trap levels, which have a strong influence on electrical properties, are necessary in addition to I-V measurements. These can be pursued by optical absorption or luminescence spectroscopy as well as by further electrical measurements. For example, DLTS has already been used extensively to study the electronic behaviour of the deep levels in other, more conventional semiconductors. There are other techniques which are used to study defect levels including the analysis of space-charge-limited current (SCLC), capacitance-voltage (C-V) measurements, isothermal current transient spectroscopy (ICTS), photoinduced current transient spectroscopy (PICTS) and frequency-dependent (ac) conductivity measurements [Nath and Wilson, 1996].

Charge-based Deep Level Transient Spectroscopy (Q-DLTS) was applied by Polyakov *et al*, [2001], to study impurity-induced defects. Their density and energy distribution were in a band 0.01 eV $\leq E\text{-}E_V \leq$ 1.1 eV above the valence band. It was

shown that differential C-V and Hall Effect measurements combined with DLTS data can be used to determine the degree of acceptor compensation, and the concentration of compensating donors (mostly the positively charged single-substitutional nitrogen (N^+)) in p-type CVD polycrystalline diamond films. It was found that incorporated boron atoms induce three levels of electrically active defects;. two of them have concentrations of (2-3) $\times 10^{16}$ cm^{-3} and activation energies of 0.36 and 0.25 eV with capture cross-sections of 1.3 $\times 10^{-13}$ and 4.5 $\times 10^{-19}$ cm^2, respectively. The third type of defect has an activation energy of 0.02 eV and a capture cross-section of 3×10^{-20} cm^2, this shallow trap may will be a general provider of holes in low-doped films [Polyakov *et al*, 2001].

The constant photocurrent method (CPM), Electron Paramagnetic Resonance (EPR), and Infrared absorption Fourier Transform (FTIR) techniques have been used to study characteristic defects in the gap of free-standing optical-quality CVD diamond [Nesladek *et al*, 1999]. It has been shown that the density of states in the gap is very sensitive to oxidation, hydrogenation and annealing treatments [Nesladek *et al*, 1998]. At room temperature EPR and CPM measurements reveal a well-defined single substitutional nitrogen defect [Nesladek *et al*, 1998; Rosa *et al*, 1999]. Although it was originally suggested that CVD diamond could not be of the Ib type, the CPM spectra clearly show that substitutional nitrogen is also a fundamental bulk defect present in CVD diamond.

Photocurrent yield measurements of CVD diamond show two main electron emission features, one at about 4.2 eV, and a second one at about 2.1 eV below the conduction band minimum, denoted as D1 and D2, respectively [Riestein *et al*, 1997]. The numerical fitting of data of Nesladek *et al*, [1998], places the D1 level at photon energy of about 1.3 eV. This is in good agreement with the photoelectron yield data (D1 was placed about 4.2 eV from the conduction band, hence about 1.3 eV from the top of the valence band) [Riestein *et al*, 1997]. Nesladek *et al*, [1998] observed two dominant features in the photocurrent data in optical-quality CVD diamond samples; a clear photocurrent shoulder with an onset at about 2.2 eV (denoted as D2). This value agrees with the photoexcitation of a single substitutional nitrogen defect.

The best understood defect caused by electron irradiation in diamond is the vacancy due to the removal of a carbon atom from its lattice site. This process is known

to be orientation dependent, with the smallest displacement energies in the {100} direction. The dislodged carbon atom moves through the crystal and relocates itself, usually sitting between lattice sites as an interstitial. The vacancy creates four 'dangling bond' sp3 orbitals of the nearest neighbour atoms which no longer experience the same periodic potential. This results in ground and excited electronic states in the band gap of diamond. The neutral vacancy in diamond is responsible for a luminescence centre known as GR1. Its ground state lies approximately mid gap in diamond [Lowther, 1993], and it has a doubly excited state some 1.67 eV above this. Wotherspoon *et al*, [2002] found two zero phonon lines (ZPLs) associated with the GR1 vacancy, at 741 and 745 nm. The vacancy in diamond is also known to exist in the negative charge state. Although the negative vacancy in diamond might not be expected to generate a signal because the excited state of the defect lies in the conduction band of the material, it has been seen a couple of times in Wotherspoon's work [Wotherspoon *et al*, 2002]. Steeds [2000] suggests that the positive vacancy has been observed in boron-doped diamond.

As carbon atoms move from their lattice sites they begin to create more complex defects. For example, if two interstitials are located between adjacent lattice sites then it is a di-interstitial [Hunt *et al*, 2000], and so on. The introduction of a nitrogen dopant further complicates the picture; nitrogen impurities can be located next to vacancies creating nitrogen – vacancy complexes [Vlasov, 2000]. These complexes exist in the neutral $(NV)^{0}$ and negative $(NV)^{-}$ charge states. Nitrogen may also aggregate in the lattice. The simplest form, the aggregate, consists of two nearest neighbour substitutional N atoms. In CVD grown diamond the low temperature of growth is below the onset for nitrogen aggregation.

With many different centres existing after electron irradiation, photoluminesince (PL) spectra consist of many lines competing with one another for excitation. The intensity of a given peak will depend upon the quantity of that centre in the diamond, as well as its capture cross-section and upon the energy of the incident laser light. The position of the Fermi level and the charge state of the centre also determine the intensity of the observed luminescence [Wotherspoon *et al*, 2002].

Although donor and acceptor levels (labelled (0/+) and (-/0)) of point defects in a range of materials like silicon, germanium and III-V materials have been extensively studied using theoretical and experimental methods, the situation is somewhat different

for diamond. The importance of defects as deep traps for carriers or as non-radiative recombination centres is significant now that diamond is becoming a viable electronic material [Isberg *et al*, 2002]. For narrow-gap semiconductor materials the deep electrical levels possess the ability to trap free carriers, and zero bias measurements indicate the charge state that a defect will adopt for a given Fermi level in the material. However, for diamond (an insulator) the concept of a Fermi level is perhaps less relevant, and it has been suggested that the proximity of defects to dopants is crucial [Collins, 2002]. For inhomogeneous, e.g. polycrystalline, samples the Fermi level has to be interpreted with great care. In a small number of instances the electrical levels of impurities and lattice defects have been obtained experimentally, predominantly for impurities such as substitutional nitrogen, phosphorus, boron and other optically and magnetically active centres. The defects present in the samples depend on the history of the material and in particular whether it is natural or synthetic. CVD diamond commonly contains isolated impurity defects including nitrogen, silicon and boron, and it has recently become clear that hydrogen plays a role in the formation of electrically active defects. HPHT synthetic diamonds may contain isolated substitutional nitrogen if getters have not been employed, and where nickel is present as part of the solvent-catalyst, a range of nickel-related defects have also been found, many of which are predicted to be electrically active [Goss *et al*, 2004].

In diamond, the vacancy, because of its high activation energy, only becomes mobile at about 973 K. CVD diamond films are commonly grown at temperatures between 973-1473 K, and so the neutral vacancy is mobile and will migrate to grain boundaries or trapping centres [Davies *et al*, 1992]. Since material further into the bulk will have spent longer at high temperatures than material near the surface, the concentration of vacancies would be expected to decay with distance into the film if the vacancies originally grew in the surface of the sample.

Studies of natural diamond [Davies *et al*, 1992], and CVD diamond, shows that the vacancies may be trapped at defects or form divacancies [Allers and Mainwood 1998]. In other semiconductor materials, the temperature at which vacancies migrate is much lower than the growth temperature, so any vacancies which are created in the growth process will rapidly migrate to the surface, be trapped or aggregate into clusters [Allers and Mainwood, 1998].

Structural defects also exist, such as twins or dislocations. According to Harlman's model [Zhang, 1981], the bonds in the two parts of a twinned crystal are identical with each other, with different intermediate layers only. This difference is the deformation which probably happened when the bond chains went through the twin boundary. Energy theory predicts that the smaller the deformation, the easier is the formation of the twin crystal. When a crystal grows in the quasi-equilibrium condition, all the atoms that form the surface of the crystal will be at the positions where their free energy is lowest. Thus single crystals are formed. However, if the conditions slightly deviate from these, there is probability that the atoms could form the twin crystal. In this case, the two bodies of the twin crystal are the same size while the orientation near the twin boundary agrees with the reflection symmetric relation [Qizhi *et al*, 1993]. The type of dislocation in CVD diamond and their characteristic quantities and distributions are determined by a projection analysis of the dislocations [Xu and Feng, 1987; Qizhi *et al*, 1993]. Twin crystal and dislocation defects are described and illustrated in Chapter 4 on defects in semiconductors.

3.3 Defect state measurements

Potential applications of diamond to semiconducting devices have been extensively studied since the successful growth of thin CVD diamond films. In many of these studies emphasis was on the procedure for sample preparation and subsequent characterisation rather than the actual properties of a device. For electronic device applications, it is important to understand the electrical properties and conduction mechanisms as well as the junction properties of these films [Nath and Wilson, 1996].

DLTS has been used at a fixed voltage bias over the temperature range 100 - 450K on an aluminium Schottky contact on polycrystalline diamond, prepared on a silicon substrate by PACVD [Nath and Wilson, 1996]. A good signal to noise ratio and clear peaks in the DLTS spectra were observed by Srikanth *et al*, [1990]. The activation energies, the cross-sections and concentrations of the traps present in diamond were obtained. C-V characteristics at 1 MHz can also be analysed to determine the dopant concentration and subsequently the trap concentration from the capacitance transient [Nath and Wilson, 1996]. Since diamond samples are usually highly resistive, caution must be taken not to exceed the frequency limit imposed by the measurement.

3.4 Treatment of the diamond surface

The grown surface of undoped (nominally p-type) CVD films, which is fully hydrogen-terminated, is deeply accumulated, hence holes form a conducting surface layer, while an oxygenated surface shows downward band bending to form a depletion layer for holes. Measurements of electrical conduction along the surface on samples with different surface conditions suggest the existence of an accumulated or a depleted surface for holes depending on whether it is hydrogenated or oxygenated respectively [Shirafuji and Sugino, 1996]. Furthermore, Kelvin probe measurement [Sugino *et al*, 1994] and X-ray photoelectron spectroscopy (XPS) analysis [Sugino *et al*, 1994: Shirafuji *et al*, 1995] give direct evidence implying the occurrence of band bending related to adsorption of hydrogen or oxygen atoms. The work function estimated from the measurement of contact potential difference (CPD) may include a surface dipole effect due to the added atoms. The order of electronegativity is H<C<O, suggesting that hydrogen adsorption will reduce the work function while oxygen adsorption will produce the opposite effect. CVD diamond films are usually deposited under conditions deviating from thermal equilibrium in an environment filled with high energy particles such as electrons, hydrogen ions, ionized source gas molecules and their fragments. These high energy particles can introduce various kinds of structural defects at and near the surface as well as promoting the occurrence of hydrogen termination of surface dangling bonds. Such defects can act as Fermi level pinning centres. However, surface structural defects, which may not be directly associated with adsorbates, may also be responsible for band bending [Shirafuji and Sugino, 1996].

The position of the Fermi-level at a diamond film surface and the band bending or internal (built-in) electrical field plays an important role in determining its electrical and photoelectrical properties, including surface electron emission [Bandis and Pate, 1995; Pate *et al*, 1995]. Various surface treatments can change the band bending and even induce a NEA on the diamond surfaces [Baumann *et al*, 1996; Van der Weide *et al*, 1994; Bandis and Pate, 1995]. Such treatments include either annealing at elevated temperatures, or plasma treatments in various gas environments. For example, it has been demonstrated that hydrogen termination can form downward band bending and induce NEA on monocrystalline diamond surfaces [Tachibana *et al*, 1993; Bandis and Pate, 1995; Pate *et al*, 1995]. The hydrogen termination is assumed to create a surface dipole that causes a shift of the conduction band minimum on the diamond surface with respect to the vacuum level. In contrast, as–prepared oxygen-treated diamond surfaces

often exhibit upward bending and positive electron affinity [Van der Wide *et al*, 1994; Bandis and Pate, 1995; Pate *et al*, 1995; Kiyota *et al*, 1995]. However, an oxygen-terminated diamond surface (treated by plasma) can react with caesium and form a surface with NEA, enhancing field electron emission [Pickett, 1994; Geis *et al*, 1995].

An alternative surface treatment that can be employed to change the diamond surface properties is to coat the film surface with a thin layer of metal. Deposition of a few monolayers of a metal such as titanium, nickel, cobalt, aluminium or gold on a diamond surface can change the band bending, induce NEA and cause field enhanced electron emission [Nemanich *et al*, 1995; Baumann *et al*, 1996]. The type of defects formed on treated diamond surfaces can include vacancies, second phases such as graphite and amorphous carbon impurities [Polyakov *et al*, 1998]. Moreover, the assumption that electrons can be emitted directly into a vacuum from these surface states can explain emission from the undoped diamond at low electrical fields [Huang *et al*, 1994; Zhu *et al*, 1995].

Concerning the experiments involving the annealing of the films, another puzzle is that the I-V characteristics can change after annealing under UHV conditions at very low temperatures. Even annealing for 30 minutes at 323K influences the (surface) conductance and the I-V curves. Landstrass and Ravi [1989], Looi *et al*, [1999], Maier *et al*, [2000] and Szameitat *et al*, [2000] all observed a similar loss of the surface conductance after annealing at relatively low temperatures. It has been shown that the p-type surface conductance is hydrogen-related (since it was also observed on perfectly reconstructed diamond) [Kawarada *et al*, 1995]. Consequently, three possible explanations can be given for the disappearance of the conductance. One explanation for the observed behaviour is oxidation of the sample, but this can be ruled out as the experiments were performed in high vacuum. A second involves subsurface hydrogen. Experiments by Cannaerts *et al*, [2001], confirmed that the morphology of the reconstructed surface does not change significantly after low temperature annealing. The third possible explanation is proposed by Maier *et al*, [2000] and Szameitat *et al*, [2000] who observed a reduction in conductance after annealing at low temperatures, and a subsequent reappearance of the conductance by simply exposing the samples to atmosphere for a few hours. They argue that chemisorbed hydrogen is a necessary condition for the high conductance, but that other adsorbed species such as a water layer [Maier *et al*, 2000] or a CO group [Szameitat *et al*, 2000] are also required.

Consequently, rather than a redistribution of subsurface hydrogen, it is desorption of adsorbates from the surface which causes the lowering of the surface conductance [Cannaerts *et al*, 2002].

Exposing diamond to a hydrogen plasma yields a surface conductive layer with p-type carriers of low activation energies [Kawarda *et al*, 1995; Mackey *et al*, 1995; Looi *et al*, 1998; Sauerer *et al*, 2001; Williams *et al*, 2001; Look and Molnar, 1997; Hayashi *et al*, 1997; Maier *et al*, 2000]. This phenomenon has been utilised to fabricate diodes and field effect transistors on the surface of homoepitaxial and polycrystalline films, which display excellent characteristics at room temperature [Gluche *et al*, 1997; Hokazon *et al*, 1997; Looi *et al*, 1998]. However they are not particularly stable. Various models have been proposed to explain this effect involving adsorbed species (including but not limited to hydrogen) and hydrogen within the bulk of the diamond [Hayashi *et al*, 1997; Gi *et al*, 1995]. However, all current models require the termination of the surface of diamond by hydrogen [Williams *et al*, 2002].

Hydrogenated diamond films exhibit different features in both their electrical and optical properties compared to those of oxidized diamond films. From Hall effect measurements, Hayashi *et al*, [1997], found that the carrier (holes) concentration per unit area of all the as-deposited films is four to five orders of magnitude larger than that of the oxidized boron doped film at room temperature and is nearly constant in the temperature range between 120 and 400K, while the number of carriers per unit area for the oxidized boron-doped film shows a strong temperature dependence with an activation energy 0.38 eV. The Hall mobility of all the as-deposited films was found to be one to two orders of magnitude smaller than that of the oxidized boron-doped film and increased with increasing temperature, while that of the oxidized boron-doped film decreased [Hayashi *et al*, 1997].

3.5 Impurities in diamond

There are many elements (≈ more than 50) that exist naturally in diamonds. Nitrogen, hydrogen, boron, phosphorus, lithium, and oxygen are the dominant impurity species. Boron and nitrogen can exist as substitutes for carbon in the crystal lattice, but other impurities can exist as small inclusions. Synthetic diamonds do not contain many of the naturally occurring impurities, although the walls of the synthetic vessel may

introduce the presence of boron and nitrogen in significant amounts. The role and properties of some important impurities are given below.

Impurities can be introduced into diamond during CVD or HPHT growth. Some of the layers grown thus may exhibit electrical conductivity related to the presence of the foreign atoms. In order to be certain that doping actually took place, the effects related to undesirable impurities or defects, in particular those decorating grain boundaries in CVD-grown polycrystalline material, must be eliminated. Studying single-crystal diamond obtained by homo-epitaxial growth in presence of the required dopants is the best manner of achieving this.

Several impurities are candidates to act as donors in diamond when occurring in the proper lattice site: group I elements (lithium, sodium) on interstitial sites, or group V elements (nitrogen, phosphorus, arsenide), when singly ionized, on substitutional sites, group VI elements (oxygen, sulphur) can also donate electrons for conduction when no substitutional sites exist and when in the singly ionized charge state. In principle, defect complexes, such as impurity-vacancy, impurity-hydrogen, or more complicated structures can also possess suitable donor energy levels. Native defects in diamond give rise to well known levels within the forbidden gap. In particular, many experiments indicate that vacancies, such as those created during electron irradiation or ion implantation, can yield donor-related conduction, mostly determined by conductivity measurements [Kalish, 2001].

As in silicon and germanium, group III and V substitutional impurities are expected to behave as shallow acceptors and donors respectively in diamond [Ramdas and Rodrigues, 1981]. It is interesting to note that the Hall effect and resistivity measurements performed on the extremely rare p-type naturally occurring diamonds (the so-called nitrogen free type IIb specimens) as a function of temperature, yielded impressive hole mobilities and acceptor ionisation energy [Kim *et al*, 2000].

Diamond is not easy to dope since it is difficult to get non-carbon atoms to occupy substitutional sites within the dense crystal lattice. Boron and nitrogen are the only widely demonstrated dopant species, forming acceptor and donor states, respectively, but both require high levels of thermal activation to release free carriers (0.37 eV for boron, much more than nitrogen (1.7 eV)) [Gildenblat *et al*, 1991; Collins, 1994].

Phosphorus and sulphur have been considered for the formation of n-type diamond, with some suggestions of success [Koizumi *et al*, 1997; Koizumi *et al*, 1998; Zhang *et al*, 1996; Casanova *et al*, 2001; Kalish *et al*, 2000; Saada *et al*, 2000; Miyazaki and Okushi, 2001], but again very deep donor levels are formed.

In the case of sulphur it has been claimed that a donor level was formed with activation energy of 0.19-0.33 eV, and a p-n junction was formed using a boron-doped substrate [Hasegawa *et al*, 1999]. Nitrogen incorporation by ion-implantation has also been shown to increase the n-type character of diamond films used for field emission applications [Kalish *et al*, 1997; Kalish, 2001]. A few reports exist on the use of Q-DLTS to explore the defect structure within diamond films [Ermakova *et al*, 1993; Botev *et al*, 1993; Pimenov *et al*, 1997; Polyakov *et al*, 1997; Polyakov *et al*, 2001; Gaudin *et al*, 2001].

It is well known that boron atoms induce electrically active deep level defects in single-crystal diamond with an activation energy for moderately doped samples of approximately 0.35-0.37 eV [Collins and Lightowlers, 1979; Wynands *et al*, 1994; Malta *et al*, 1995; Von Windheim *et al*, 1993]. Nitrogen atoms that are incorporated at substitutional sites of diamond films form deep donors with a much higher activation energy of approximately 1.6-1.7 eV, which is dependent on temperature, as determined by resistivity measurements [Collins, 1999; Polyakov *et al*, 2001].

The concentration of boron and nitrogen atoms incorporated in diamond films can be detected by chemical, optical or electrical methods [Wynands *et al*, 1994; Malta *et al*, 1995; Von Windheim *et al*, 1993; Chen and Chen, 1995; Locher *et al*, 1995; De Cesare *et al*, 1995; Rohrer *et al*, 1998; Erz *et al*, 1995; Gheeraert *et al*, 1998; Fox *et al*, 1995; Nistor *et al*, 2000]. As a rule, secondary-ion mass spectroscopy (SIMS) has been used for the measurements of the total boron and nitrogen concentration, N_B and N_N respectively. However, in diamond films only a proportion of the boron and nitrogen is incorporated at substitutional sites of the diamond lattice and can therefore act as acceptors or donors. A substantial fraction of the boron and nitrogen atoms are located at the interstitial and clustering sites, or at the grain boundaries and are electrically inactive. Thus, the total concentrations N_B and N_N tend to be much higher than the uncompensated acceptor (or donor) concentration $|N_A\text{-}N_D|$, where N_A is the total

acceptor concentration and N_D is the total donor concentration. The SIMS measurements are unaffected by compensation [Polyakov *et al*, 2001].

As a rule, the quantitative evaluation of the uncompensated acceptor concentration $|N_A - N_D|$ of p-type (boron-doped) diamond films is determined from non-destructive electrical measurements, such as Hall effect and C-V measurements [Wynands *et al*, 1994; Malta *et al*, 1995; Von Windheim *et al*, 1993], or DLTS directly to obtain quantitative information about native and extrinsic defects [Lang, 1974; Nath and Wilson, 1996]. DLTS was applied previously to investigate the defect distribution in IIb synthetic diamond and thin CVD polycrystalline diamond films at silicon and metal substrates [Ermakova *et al*, 1993; Kiyota *et al*, 1993; Polyakov *et al*, 1997; Polyakov *et al*, 1998; Zeisel *et al*, 1998; Zeisel *et al*, 1999; Polyakov *et al*, 2000; Muret *et al*, 2000].

3.5.1 Nitrogen in diamond

Nitrogen is always present at different concentrations in natural diamond and it can also be introduced into diamond during CVD and HPHT synthesis. Nitrogen-containing diamonds are electrically insulating at room temperature due to the deep level associated with this impurity. Photoconductivity, optical absorption, cathodoluminescence (CL) and Electron Paramagnetic Resonance (EPR) techniques are suitable for studying nitrogen in diamond. The various defect complexes which nitrogen forms in the crystal have been identified, and the amount of nitrogen incorporated in substitutional sites and the nitrogen bonding configurations in diamond have been investigated [Kalish, 2001]. The energy level associated with an interstitial nitrogen in diamond is found to lie at 1.7 eV below the conduction band minimum [Kalish, 2001]. Hence, doping diamond with nitrogen is not expected to yield useful conductivities at room temperature. The amazingly strong field emission observed by Okano *et al*, [1996] in nitrogen-doped CVD diamond at room temperature can not thus be directly attributed to the availability of electrons for emission, due to their rather deep energetic location inside the diamond.

The PL spectra of flame-grown layers are usually dominated by two vibrational systems that have been attributed to nitrogen-vacancy pairs, with their zero phonon lines at 2.16 eV and 1.95 eV [Janssen *et al*, 1991; Freitas *et al*, 1994]. The spectra reveal an

extremely low density of luminescent defects with a marginal presence of the 2.16 eV (indicated by nitrogen-V) system and almost no sign of the other nitrogen-related system mentioned above. It has been suggested that, under certain growth conditions, nitrogen may be incorporated as nitrogen-vacancy pairs in the crystal from the ambient nitrogen in the atmosphere [Schermer *et al*, 1995].

3.5.2 Hydrogen in diamond

Generally, hydrogen can be incorporated into diamond in one of three electronic states, H^-, H^0 or H^+ depending on the position of the Fermi level (E_F). For the case in which E_F is at approximately mid-band gap (i.e. between the acceptor and donor level energies of hydrogen), hydrogen is expected to be in the neutral charge state. In p-type diamond, the stable form of hydrogen will be H^+, and in n-type diamond, it will be H^-. The migration energy of H^0 has been calculated to be approximately 1.9 eV while that of H^+ is much smaller, approximately 0.2 eV, and that of H^- is 2.5 eV. H^+ will, thus, be a fast diffuser while H^- and H^0 are predicted to be very slow diffusers [Uzan-Saguy *et al*, 2002]. The hydrogen dimer, H_2, is a neutral defect predicted to be readily formed when the concentration of H^0 is high [Uzan-Saguy *et al*, 2002]. The H_2 dimers have a relatively high binding energy (2.5eV) and a high migration energy (3.5 eV) and are expected to be stable and immobile up to very high temperatures. Furthermore, it is expected that hydrogen atoms will strongly interact with dislocation cores where they may diffuse rapidly and form complexes with other hydrogen atoms. The binding energy of such hydrogen complexes to the dislocation core was calculated to be 4 eV [Uzan-Saguy *et al*, 2002], making this defect particularly stable. The stability of hydrogen in diamond is, as in other semiconductors, very low in pure crystal and significantly increased by the interaction of hydrogen with dopants and point / extended defects. In CVD grown diamond layers of reasonable quality, the concentration of hydrogen is approximately 1×10^{19} cm^{-3} due to the inherent presence of H in the carrier gas.

In the case of phosphorus, the donor level (E_C – 0.6) eV is well above the hydrogen acceptor level ($\approx E_C$ – 2) eV. Therefore, hydrogen will compensate the phosphorus donors giving rise to H^- and possibly to phosphorus-hydrogen complexes as a result of the trapping of H^- by positively-charged phosphorus donors. The hydrogen acceptor level ($\approx E_C$ –2) eV is probably close to the nitrogen donor level (mentioned

above) and a charge transfer giving rise to H^- and N^+ donors is also possible [Chevallier *et al*, 2002]. However, the calculated theoretical migration energy of H^- is quite high (2 – 2.5) eV [Mehandru and Anderson, 1994]. As a consequence, diffusion of hydrogen in n-type is much lower than in p-type diamond where the migration energy of protons is only 0.1– 0.2 eV [Goss *et al*, 2001].

It has been shown [Chevallier *et al*, 1998; Zeisel *et al*, 1999; Uzan-Saguy *et al*, 2001], that hydrogen may be trapped by boron impurities and its presence in the crystal next to boron acceptors passivates the latter. Both C-V and Hall effect measurements have clearly demonstrated electrical passivation of boron acceptors by hydrogen following deuteration at 820K [Zeisel *et al*, 1999; Uzan-Saguy *et al*, 2001].

The role of oxygen in CVD grown diamonds is to reduce the concentration of hydrogen-carbon complexes such as CH_3 by forming CO [Goodwin *et al*, 1997]. This is stable and thereby removes excess carbon. Trace amounts of OH and O present in the plasma react with sp^2 impurities far more readily than does atomic hydrogen. Oxygen therefore helps to remove sp^2 defects to give a purer CVD crystal. Natural diamond surfaces have been studied using X-ray photoelectron spectroscopy and Rutherford back scattering spectroscopy (RBS) and a submonolayer of oxygen has been found [Hansen *et al*, 1989; Rebuli *et al*, 1999].

Atomic hydrogen is necessary during the CVD growth process to remove the graphitic phase and to stabilize the diamond phase. Therefore, in contrast to natural diamond, all CVD films will inevitably contain after deposition, to a certain extent, hydrogen at the surface as well as in the bulk [Landstrass and Ravi, 1989]. Hydrogen can be removed from CVD diamond surfaces by annealing the films at temperatures that typically range between 873 and 1273K [Chua *et al*, 1994], depending on the annealing conditions. On the other hand, CVD films can be rehydrogenated by annealing them in hydrogen plasma [Cannaerts *et al*, 2002].

Boron is a well-established dopant, that controls the (p-type) electrical conductivity of diamonds. Its use has enabled the production of a variety of electronic devices, sensors and electrodes. The uptake of the boron during growth has been found to rely on surface facet orientation and on the presence of oxygen in the growth chamber. Charles *et al*, [2002] indicates that there may be boron depletion at grain

boundaries or a grain size or boundary dependence on the uptake. The study of point defects is facilitated by their introduction via irradiation, usually done with electrons. When irradiating with electrons, simple point defects are formed, mainly interstitials and vacancies. Boron-doped diamonds have an abundance of holes and could be a candidate to find the elusive positive vacancy (V^+) in diamond. To study these defects, microscopic photoluminescence (PL) is carried out, which enables local studies of the spectra, and hence boron levels, in different regions of the diamond [Charles *et al*, 2002].

3.5.3 Boron in diamond

Boron is the only element known to be an effective mass acceptor in diamond giving p-type semiconductor behaviour. Boron-doped CVD diamond with different acceptor concentrations can be easily grown, and because of its technical importance, many studies of the electrical and optical properties have been carried out [Collins and Lightowlers 1979; Gheeraert *et al*, 1998; Pruvost *et al*, 2000; Mamin and Inushima, 2001; Piccirillo *et al*, 2002].

The presence of substitutional boron, whether occurring naturally (type IIb diamonds), via ion implantation, or introduced into chemically vapour deposited films during growth creates an acceptor level at 0.37 eV above the valence band leading to p-type conduction [Walker *et al*, 1997]. A convenient gaseous form of boron to dope CVD diamond films at room temperature is diborane B_2H_6 [Harper *et al*, 1991; Fujimori *et al*, 1990; Miyati *et al*, 1993; Butler *et al*, 2002]. Extensive research has been conducted in the synthesis and characterization of boron doped p-type semiconducting diamond [Fujimori *et al*, 1990; Gildenblat *et al*, 1991; Visser *et al*, 1992; Borst *et al*, 1994], and some electronic devices have been tested [Gildenblat *et al*, 1991; Geis *et al*, 1988].

Measurements of the temperature dependence of resistivity reported by Collins and Williams *et al*, [1970] showed that values of activation energy for the boron impurity were much smaller than those of the acceptor levels of boron impurity in natural diamonds as determined by photoabsorbtion (0.35 eV) [Collins and Williams, 1970]. C-V and DLTS experiments have been used to explore various properties of

boron-doped type IIb-HPHT diamond and of homoepitaxially grown boron doped (CVD) diamond including [Nebel *et al*, 2001]:

- Properties of Schottky contacts.
- Acceptor densities and hydrogen-boron interactions.
- Energy distributions and densities of compensating defects.

Due to the low dielectric constant of diamond the Bohr radius for holes in diamond is small (approximately 3Å) and the formation of an impurity band is observed for rather high boron concentrations (above $10^{19}cm^{-3}$), while the Mott insulator-metal transition is predicted to be around $2x10^{20}cm^{-3}$ for boron [Williams *et al*, 1970; Visser *et al*, 1992]. At room temperature nearly all boron atoms (more than 99 %) are not ionised [Gono *et al*, 1995]. At low carrier concentrations the activation energy approaches 0.37 eV, and at approximately $10^{21}cm^{-3}$ the activation energy can be extrapolated to be zero at which point the diamond becomes a perfect degenerate semiconductor. Vishnevskii *et al*, [1981] and Nishimura *et al*, [1991] have reported that synthetic semiconducting diamonds become "degenerate semiconductors" at approximately $7\times10^{20}cm^{-3}$ of boron.

The effective activation energy for boron in polycrystalline diamond is higher than that reported for single crystal diamond [Shin *et al*, 1995]. The possible reasons for the higher value reported by different workers and by various techniques may be due to the barrier height across the grain boundaries or to the existence of point defects such as vacancies. One possible cause of very low activation energy when doping heavily by boron implantation may be due to the difficulty of annealing diamond without conversion to graphite [Nath and Wilson, 1996]. Hydrogen is believed to bind chemically to the boron atoms removing boron's electrical activity [Butler *et al*, 2002].

3.5.4 Phosphorous in diamond

The further development of diamond-based electronic devices is hindered mainly due to the inability of making n-type semiconducting diamond with a shallow donor level. Theoretical calculations [Kajihara *et al*, 1991; Kajihara *et al*, 1990], using the plane wave pseudoptential method, suggest that phosphorus should be a shallow donor in diamond, at a level of 0.2 eV relative to the bottom of the conduction band, despite the large positive formation energy and the very small equilibrium solubility in

diamond. Prins [1994] has implanted diamond with phosphorus at low concentration and determined the phosphorus donor level to be 0.1 eV [Cao *et al*, 1995].

The phosphorus-doped samples grown by NIRIM (National Institute for Research in Inorganic Materials) have been subjected to a wide variety of experimental tests. The results of all these studies confirmed the existence of a level, associated with the presence of substitutional phosphorus in the diamond crystal, located at approximately 0.5 eV within the gap. The early findings of the NIRIM group, that phosphorus introduced into diamond during CVD growth does indeed act as donor, provides a guideline for the search for phosphorus doping of diamond also by ion implantation [Koizumi *et al*, 1997; Koizumi *et al*, 1998].

So far phosphorus is the only element found to be an unequivocally successful n-type dopant for diamond [Koizumi *et al*, 1997] with a thermal activation energy equal to 0.6 eV [Neslandek *et al*, 1999; Gheeraert *et al*, 1999] for a sample doped with about $10^{18}cm^{-3}$ [Koizumi *et al*, 2002]. Fourier transform infrared spectroscopy, cathodoluminesence, and Hall effect were employed to characterize a set of phosphorus-doped diamond films grown under similar conditions by CVD with different phosphine concentrations in the reactant gas ([P]/[C]) = 250 to 500 ppm). The activation energy of the conductivity shows a good agreement with the value for the phosphorus-doped sample (about 0.6 eV). Infrared measurements show the characteristic absorption peaks related to neutral substitutional phosphorus. Hall effect measurements clearly indicate n-type conductivity with mobility equal to $40cm^2/Vs$ at room temperature and a phosphorus concentration in the film of about 10^{18} cm^{-3}. Cathodoluminescence measurements showed the free excitons and bound exciton peaks related to phosphorus; bound-exciton recombination without phonon emission has also been observed [Tajani *et al*, 2002]. These results were obtained by different analytical methods on a set of phosphorus-doped diamond films. Fourier transform infrared spectra, obtained at 4K showed two peaks at 0.525 and 0.564 eV, and Hall effect measurements indicated clear n-type conductivity, with an activation energy of the electron concentration of about 0.6 eV. The two peaks correspond to the transitions between the ground level of the phosphorus bound electron and its first and second excited states, respectively.

A quasi-steady photocurrent method was used to study phosphorus-doped CVD films of differing qualities. High resistivity samples showed the presence of two defects,

Xp_1, with a photoionisation offset E_1 of about 0.59 eV, and Xp_2, with an E_1 of 0.81 eV. The fact that Xp_2 is not detectable in high conductivity samples indicates that Xp_2 is probably acting as a compensation or neutralisation centre. But the exact nature of the defect remains unclear. Good agreement between the activation energy E_A of the charge carrier concentration (0.55-0.6 eV) and the optical ionisation energy E_1 (PC: 0.59 eV; FTIR: 0.6 eV) of the Xp_1 level has been found. The detection of oscillatory photoconductivity and photothermal ionisation spectroscopy (PTIS) spectra at different temperatures (4.2K to 170K) yields information about the electronic structure. Three excited states from the phosphorus level were clearly detected; respectively 0.515 eV, 0.565 eV and 0.58 eV, above the Xp_1 ground level. The second excited state was also 0.565 eV [Haenen *et al*, 2000].

The location of ion-implanted phosphorus in diamond has been determined by both PIXE (particle induced x-ray emission) [Braunstein and Kalish, 1981] and electron-emission channelling techniques [Hoffsass *et al*, 1997]. Recently, EPR measurements were performed by Casanova *et al*, [2001], on type-IIa diamond implanted with phosphorus at increasing doses using the CIRA (cold implantation and rapid thermal annealing) procedure. A peak in the EPR spectra, associated with phosphorus, was observed after implantation/annealing. 1673K for 10 min. However, both EPR and channelling measurement show that a substantial fraction (~50%) of implanted phosphorus occupies substitutional sites [Casanova *et al*, 2001]. It can be speculated that the introduction of the large phosphorus atom into the tight diamond crystal induces strain, which is likely to attract defects that form electrically inactive complexes with the phosphorus.

3.5.5 Lithium in diamond

Following the theoretical prediction that lithium may be a donor in diamond when residing in an interstitial, non-bonding site [Kajihara *et al*, 1991], attempts were made to grow CVD diamond in the presence of lithium-containing vapours [Srenschulte *et al*, 2000]. Some indications for the presence of lithium in diamond were published by Nesladek *et al*, [1996]. It should be noted that there are some indirect indications that lithium may be ionised in diamond to yield a positively charged ion, which can be driven into the diamond crystal by electric field-forced diffusion [Popovici and Prelas, 1995]. However, diamond samples into which lithium has been driven by this method

did not show any conductivity, even at elevated temperatures (873K); hence, even if some lithium was incorporated into the diamond, its usefulness as an n-type dopant is in doubt [Kalish, 2001]. Lithium and carbon implantation doping attempts were also carried out by Prawer *et al*, [1993] at low temperatures. Lithium and carbon (as a control non-dopant ion) were implanted into type-IIa diamonds at doses below and above the threshold for graphitisation. For the low-dose implanted samples, no significant electrical signature could be detected. The high-dose implanted sample, following annealing at 1673K for 10 min and graphite removal, did show some electrical conductivity. From the temperature dependence of the resistivity, an activation energy of 0.22 eV over the temperature range 400 to 700K was found.

High-dose lithium implantations were performed by Job *et al*, [1996] into diamond heated to 1123K and subsequently annealed at 1173K. As expected, no radiation-induced graphitisation was observed as instantaneous annealing occurs for such hot implantations. n-type conductivity could be verified by hot-probe measurements only and an activation energy of 0.23 eV was deduced from room temperature measurements [Job *et al*, 1996].

3.5.6 Other impurities in diamond

Reports on n-type feature impurities (arsenic, antimony) in diamond appear in the early literature. However, there is no clear proof, based on detailed electrical measurements, which unambiguously shows that the measured features are directly due to the chemical doping. The suitability of large foreign atoms to serve as substitutional dopants in diamond is questionable as the large physical strain expected to accompany their substitutional presence in the diamond crystal may be the cause of the measured effects [Kalish, 2001].

Oxygen has been implanted by Prins [1994] into type-IIa diamond, and some indications are presented that conduction due to the presence of the implanted oxygen is observed. Results on the implantation of silicon into heated (673K) undoped and boron-doped homo-epitaxial diamond layers have been published [Hasegawa *et al*, 1999]. While no clear Hall effect could be measured, a variety of activation energies (0.19 - 0.33 eV) were deduced from room temperature measurements for the undoped sample following silicon implantation. The authors of that work indirectly conclude that silicon

acts as a donor in diamond by observing rectifying features for the silicon implanted into p-type diamond. In light of the donor-like nature of implantation-related damage in diamond, the p-n junction found by Buckley-Golder *et al*, [1991] in hot lithium-implanted p-type diamond could explain some of the results of Hasegawa *et al*, [1999]. It would be most desirable to confirm the findings of that work.

3.6 Grain boundaries

Grain boundaries occur in most materials and "crystalline" solids usually do not consist of a large single crystal but of many randomly orientated small crystallites which are called grains. Every grain in the solid crystal has a different orientation, shape, and volume. The boundaries separating them are called grain boundaries, which mark mismatches in the rows and planes in two adjoining crystallites. Each grain in itself is however a single crystal, and can contain point, line, planar and 3D defects.

The grain boundary blocks the movement of dislocations by providing an effective edge to the crystal where, of course, movement must stop. It is well known that polycrystalline materials are invariably more resistant to fracture than single crystals of the same material, which can be important in the structure of Schottky diodes [Rudden, 1993]. However, these grain boundaries also tend to resist the motion of electrons, and this may increase the electrical resistance of the material, which reduces its conductivity in a 'transverse' motion across the boundaries. It is possible that there is conduction parallel to the grain boundaries. It has been found that semiconducting diamond films have complicated conductivity behaviour, depending on the dopant level [Nath and Wilson, 1996]. By comparing the resistivity and hole mobility data obtained from polycrystalline films with those for bulk diamonds it appears that grain boundaries do not affect the transport properties significantly for heavily doped films. The grain boundary effects were expected to be much more important for lightly doped films [Huang *et al*, 1994].

Investigations of electrical transport in undoped plasma assisted CVD (PACVD) diamond films showed that current flows predominantly along grain boundaries in polycrystalline samples [Fiegl *et al*, 1994; Nath and Wilson, 1996]. Ermakova *et al*, [1993] studied the charge transport mechanism of diamond polycrystalline films obtained by the chemical crystallization method from an electrically activated gas phase. These authors concluded that three carrier transport mechanisms are possible in

polycrystalline diamond films, each of them being dominant in different temperature regions. For temperatures above 600K the grain boundary limited the conductivity, for intermediate temperatures (300-500K) the conductivity was greatest along the disordered intercrystalline boundaries and in the low temperature region, less than 250K, conduction is dominated by hopping between localised states of the intercrystalline boundaries near the Fermi level.

More definitive work has been done by quantifying the differences in the electrical properties of similarly grown boron-doped, homoepitaxial, and polycrystalline CVD diamond films by examining hole transport [Malta *et al*, 1995]. This group reported that grain-boundary trapping and scattering models, which were applicable to polycrystalline silicon, did not generally describe the carrier transport in polycrystalline CVD diamond [Han and Wagner, 1996].

The effects of the grain boundary have also been examined by using a fully penetrating excitation source to minimize any surface effects and by fabricating undoped polycrystalline CVD diamond film into metal-semiconductor-metal (MSM) devices in two different geometries: one with electric field normal (NG) and the other parallel (PG) to the grain growth direction. Free carriers generated with the excitation source in the NG geometry interact with grain boundaries whereas the interaction is minimal in the PG geometry. The quantitative effect of grain boundary is examined by deducing mean-free-carrier drift distance. Two device geometries were used to probe the grain boundary effects on the carrier transport see figure 3-1. The rate of saturation is much greater in normal grain geometries compared to the parallel grain [Han and Wagner, 1996].

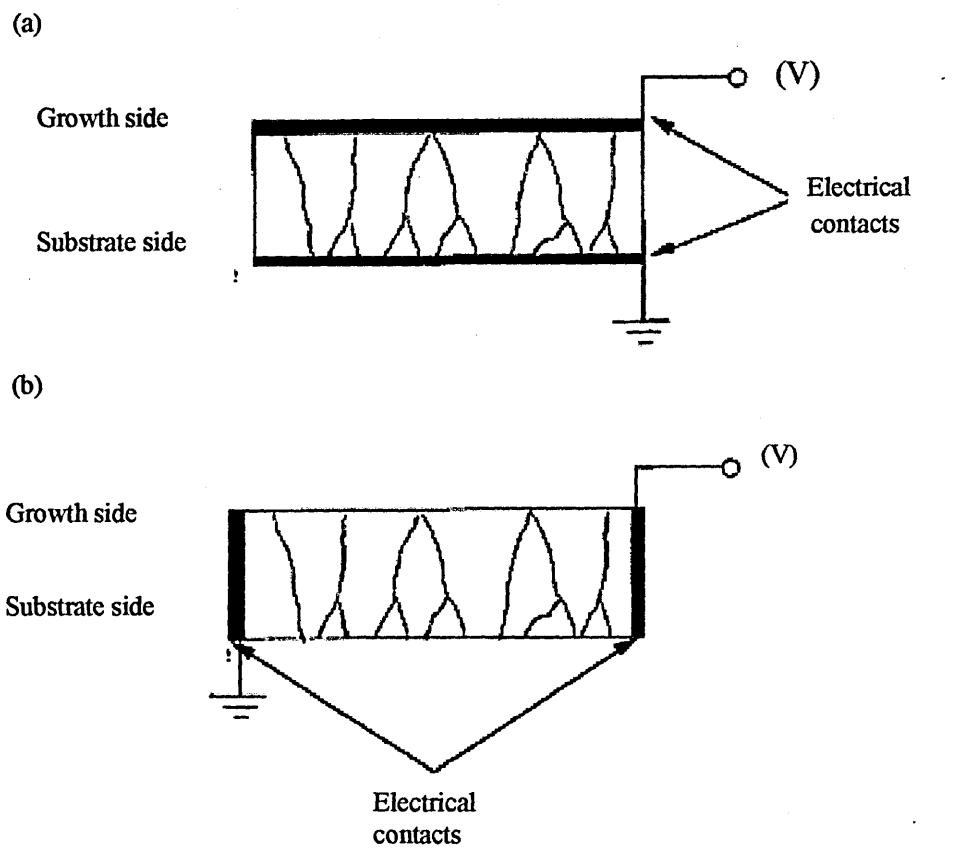

Figure 3-1 Schematic of the device geometries for measurements of grain boundary effect: a- applied electric field parallel to the crystallite growth direction; b- applied electric field normal to the crystallite growth direction [Han and Wagner, 1996].

Grain boundary effects on carrier transport properties have been examined using a hard x-ray excitation source [Han and Wagner, 1996]. The magnitude of the degradation in the transport properties has been measured to be approximately a factor of 2 at 10 kV/cm. In order to see the effect of grain boundary on the transport properties clearly, the qualities of the film needs to increase further. At a mean-carrier drift distance of approximately a factor of 3 greater than the mean-grain size, about 95% of all free carriers created from intrinsic excitation will interact with grain boundaries. This should clearly show the extent of carrier scattering and trapping at the boundaries [Han and Wagner, 1996].

Grain boundaries with a high density of defects can act as sinks for impurity atoms [Malta *et al*, 1995; Von Windheim *et al*, 1993], so an enhanced boron

concentration (compared to the bulk of the crystallites) might be present at the grain boundaries in the polycrystalline diamond films. Furthermore, it is highly probable that boron atoms incorporated at the grain boundaries do not sit substitutionally. This could result in a different apparent defect level in the forbidden gap of CVD polycrystalline diamond films with different activation energies and capture cross-section and/or an increase in the concentration of any intrinsic CVD diamond defects [Polyakov *et al*, 2001].

Most of CVD grown diamond is polycrystalline. The grains in this material are columnar being smallest on the substrate side and increasing in size approximately linearly with film thickness. Han and Wagner [1996] show that the grain boundaries degrade the detection properties in particle detectors by a factor of two to three when interdigitated electrodes are used, where carriers are more likely to drift across grain boundaries and become trapped or scattered [Mainwood, 1999]. Diamond grown by CVD produces columnar microstructures with mixtures of grain orientations, typically with a large variation of size and different shape, such as in figure 3-2 [Drory *et al*, 1995].

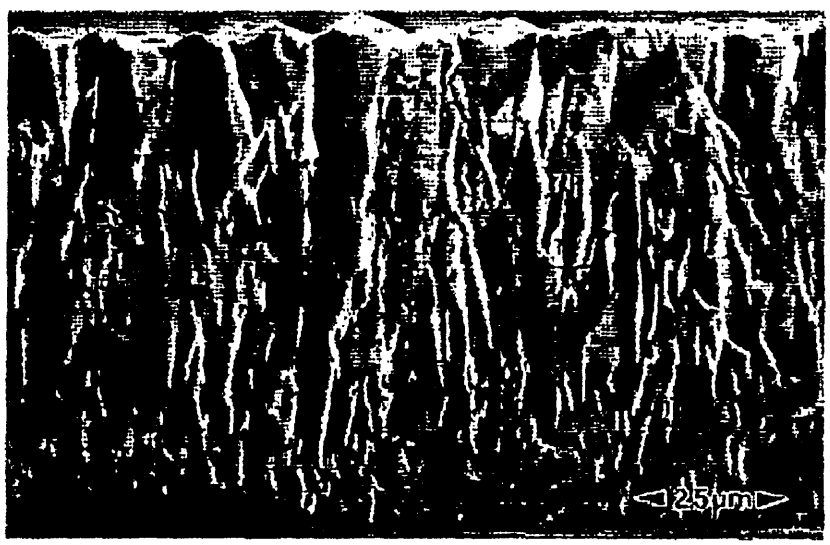

Figure 3-2: SEM micrograph of a cross section of a CVD diamond sample, showing the columnar microstructure with a very wide range of grain size from <<1µm on the nucleation surface to ~20 µm on the growth surface [Drory *et al*, 1995].

3.7 Summary

This chapter has focused on the defects that can be found in diamond. Many of these defects are electrically active, hence they can be investigated using several experimental techniques. Temperature dependence of diamond film I-V characteristics can give information about the trap level. Optical observation or luminescence spectroscopy can be used to study traps in diamond films. On the other hand, DLTS measurement is a powerful tool used to study the electronic behaviour of the deep levels in conventional semiconductors and use of DLTS to study the electronic behaviour of the deep levels in diamond films will be briefly discussed in Chapter 6. As the treatment of the diamond surface plays an important role in fabricating effective devices, we have illustrated different processes used for diamond surface treatment. Impurities can be introduced into diamond during the growth process, the control of the introduction of impurities is essential if the intention is to fabricate active semiconductor devices from diamond substrate. Different types of impurities used as dopants for diamond, have been discussed, for example, nitrogen, hydrogen, phosphorus and, particularly, boron which has been used to dope the samples investigated in this research. Other types of defects have been briefly discussed in Section 3.6. The next chapter will discuss defects in silicon as a comparison, as they are much better understood.

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Chapter 4

General properties of defects in semiconductors

4.1 Introduction

All semiconductor materials are insulators when pure or when at a temperature of 0 K. The resistivity of a semiconductor is strongly influenced by the presence of impurities called dopants and most semiconductors used today have values of resistivity around 10^{-4} - 10^{4} Ωcm at room temperature [Whitaker, 2000; Comer, 1968]. There are three important semiconductor materials, germanium, silicon, and gallium arsenide, of band gaps approximately 0.66, 1.1, and 1.43 eV respectively at 300K. Most of today's semiconductor devices contain one or more of these materials. The rest of this chapter is dedicated to a discussion of the formation and properties of defects in silicon. This is because (1) it remains the most industrially important semiconductor and (2) because the defects are not further compensated by considerations of low symmetry structures or ionicity of the crystal lattice.

As a result of the thermal energy present in a pure or intrinsic semiconductor material, valence electrons may gain sufficient energy to become free electrons, able to move through the solid as current carriers. These electrons leave behind an electron vacancy in the material, called a hole. Another electron from one of the neighbouring atoms can easily move to an adjacent bond to fill this hole. In this way the hole can move from one covalent bond to an adjacent bond and the hole can appear to move through the material. These holes contribute in almost the same way as electrons to electrical conductivity so, in a semiconductor, there are two types of mobile electrical

charge carriers that can contribute to the electrical conductivity [Cooke, 1990; Sparkes, 1987]. Thus the electric conduction in a semiconductor is caused by free electrons in conduction band and free holes in the valence band, which are known as charge carriers [Alley and Atwood, 1971].

Intrinsic semiconductors are carefully refined to reduce the impurities to a very low level. In case of the extrinsic or doped semiconductor, impurities are intentionally added to modify its electronic characteristics. The choice of the proper impurity and its effect can be estimated from an examination of table 4-1, which is a section of the periodic table of elements, including some of those belonging to Groups III, and VI, and which also includes the total number of electrons for each element shown. For example, if a dopant atom with five valence electrons (pentavalent) in the outer electron shell (such as phosphorus, antimony or arsenic), substitutes for an atom of the semiconductor material (e.g. silicon or germanium) which is quadravalent, four of the five valence electrons of the dopant atom will be held in covalent bonds. The fifth valence electron will not be in a covalent bond, and is bound only very weakly to its parent atom. Only a small amount of energy is required to make this fifth electron mobile, about 0.01 eV compared to the 0.75 eV required to generate mobile electrons in pure germanium or 1.1 eV in pure silicon. Materials which donate free electrons to the semiconductor are called donors and in a semiconductor doped in this way there are more electrons than holes. This is called an n-type semiconductor, electrons are the majority carrier and holes are the minority carrier. For more detailed information see, for example, Alley and Atwood, [1971], Cooke [1990], Lenert [1968], Sparkes [1987] and Sze [1985].

Group II	GROUP III	Group IV	Group V	Group VI
	5 B (boron)	6 C (carbon)	7 N (nitrogen)	
	13 Al (aluminium)	14 Si (silicon)	15 P (phosphorus)	16 S (sulphur)
30 Zn (zinc)	31 Ga (gallium)	32 Ge (germanium)	33 As (arsenic)	34 Se (selenium)
48 Cd (cadmium)	49 In (indium)	50 Sn (tin)	51 Sb (antimony)	52 Te (tellurium)

Table 4-1 A section of the periodic table of elements [Bar-lev, 1984].

In the same way, if an impurity or dopant atom with a valency of three, such as boron, aluminium, gallium or indium, is substituted for a silicon or germanium atom, three electrons will be held in covalent bonds, and one covalent bond will be missing an

electron, thereby creating an electron vacancy or hole, so an electron from a neighbouring atom can easily jump into this electron vacancy. Semiconductors doped with atoms that accept free electrons are called p-type semiconductors; here holes are the majority carrier and electrons are the minority carrier. The crystal is now a p-type extrinsic semiconductor in which the acceptor atoms have become bound negative ions, whilst the free carriers are nearly all holes [Waston, 1977; Zanger, 1984].

These dopants atoms will create levels, donor or acceptor, in the forbidden band gap. A shallow donor is an atom with enough outer electrons to bind its nearest neighbours with an extra electron loosely bound to the impurity. Similarly, a shallow acceptor has a loosely bound hole. These are typically less than 0.1 eV from the relevant band edge in silicon.

In contrast, foreign atoms not belonging to a neighbouring periodic group will create impurity levels further from the corresponding band edge, or deeper than its linked hydrogenic states; such levels are so-called deep levels. These deep level defects introduce energy levels deeper in the band gap at a position denoted E_T. Typically the deep levels lie between 0.1 eV and mid band gap. Usually the deep levels that locate above mid band gap are acceptor-like (-/0), i.e., they are negatively charged when occupied and neutral when empty. This is referred to as a deep acceptor level or electron trap (n_t). Those below the mid band gap are normally donor-like (+/0), i.e., positively charged when empty and neutral when full of electrons;. an alternative view is that they are positively charged when hole-filled and neutral when the hole is emitted. These are referred to as deep donor level hole traps (p_t). Such deep levels can also be introduced by point defects. For example, an atom missing from a lattice site (vacancy), or self interstitial may be introduced during the growth process, or by damage caused by irradiation or ion implantation. A certain equilibrium of vacancies and self interstitials will always exist in a real crystal at temperatures above 0K. Both these defects introduce deep levels in silicon.

Deep levels may behave as carrier traps or as generation-recombination centres. The classification will be determined by the respective capture and emission rates of electrons and/or holes. If a captured carrier stays at a deep level until re-emission into the originating band gap the deep level is classified as a trap. In contrast, if a carrier of opposite type is also captured at the same deep level before the re-emission of the first

carrier, then this level is a recombination centre as electron-hole recombination [Bourgion and Lanoo, 1983].

Whether as traps or recombination centres, deep levels are vital to semiconductor technology. As traps they can capture free carriers supplied by shallow levels, in this way serving to compensate a reduction in doping density, but the resulting increase in material resistivity could be harmful to the device. Where they function as recombination centres, deep levels may have advantageous or disadvantageous effects. Recombination centres may be used to optimise the turn-off time/forward drop trade-off in some commercial power devices. Deep levels are deleterious to LED and laser structures as they introduce a non-radiative recombination path which reduces the number of carriers available for radiative recombination [Ahmed, 1998].

4.2 Definition of a trap or recombination centre

A full definition of a trap or recombination centre is given in terms of the capture rates in a neutral region within a semiconductor, and the thermal emission rates in the depletion region of a Schottky barrier or p-n junction. First, in a neutral semiconductor, a deep level is said to be a recombination centre if the capture rates for electrons and holes are large and comparable. A deep level is referred to as an electron trap, for example, if its electron capture rate is at least an order of magnitude greater than its hole capture rate, that is $C_n >> C_p$. These definitions are summarized in figure 4-1 (a), (b). In general the recombination rate depends on the defect (or the recombination centre) density, the free carrier concentration, the electron and hole capture cross section and the energy level position.

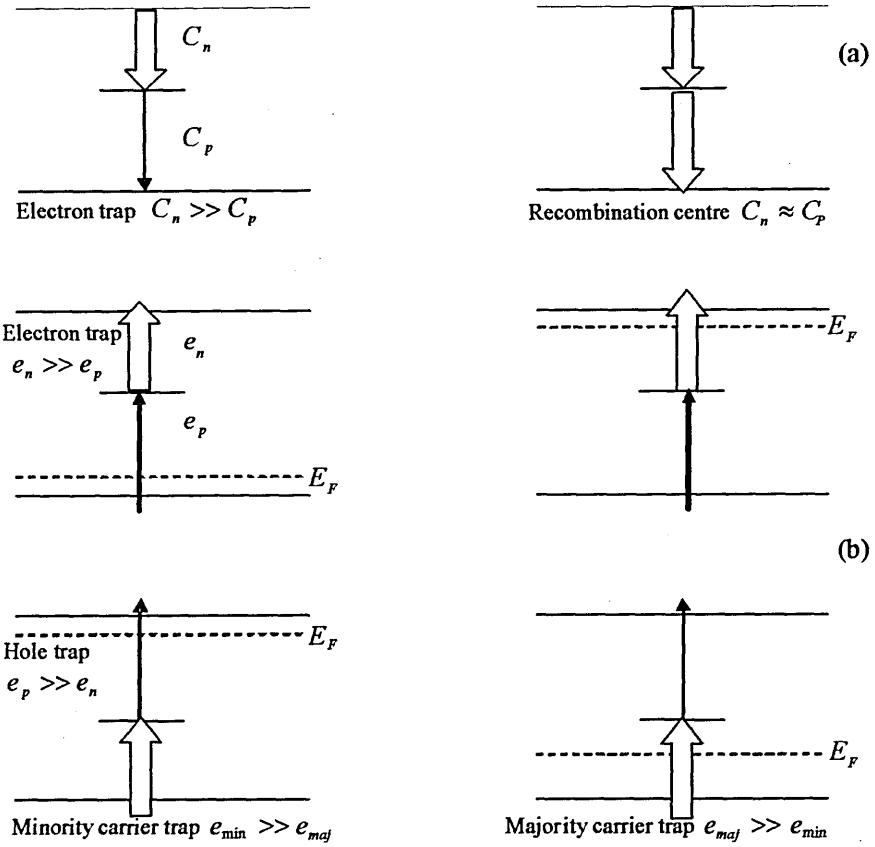


Figure 4-1 (a) Definition of the terms of electron traps and recombination centres by means of the relative magnitudes of the capture coefficients as indicated by the widths of the arrows. (b) Definition of the terms majority carrier trap and minority trap (columns) and electron trap and hole trap (rows), the relative magnitudes of the carrier emission coefficients are indicated by the widths of the arrows [Miller *et al*, 1977].

Where the electron density n, and the hole density p, are near zero in a depletion region, the thermal emission rate is more useful than the capture rate for characterising the behaviour of deep levels. If a deep level has comparable (and large) emission rates for electrons and holes then it is referred to as a generation centre, equivalent to a recombination centre in a neutral region [Sah *et al*, 1957]. For traps it is also useful to differentiate between minority and majority traps. A majority trap has a much larger capture rate for majority carriers than for minority carriers. For example an electron trap is a majority trap in an n-type semiconductor and a minority trap in a p-type semiconductor.

The Fermi level controls the occupation of traps and shallow levels. It is therefore useful to clarify the charge state of electron and hole traps in relation to their Fermi level position. Another definition given by Miller *et al*, [1977]: "An electron trap is full (of electrons) and is therefore neutral when below the electron quasi Fermi level E_{Fn}, and it is empty (of electrons) and therefore positively charged when it is above Fermi level E_{Fp}". Similarly a hole trap is full of holes and therefore neutral when it is above the hole quasi Fermi level (E_{Ff}) and empty of holes where it is negatively charged and below (E_{Ff}).

4.3 Crystal structure and band structure of Si

In a solid material, the ions are arranged in a periodic manner and each electron interacts with the surrounding ion lattice and with the other electrons in the crystal lattice. The electron energy states are determined by solving the Schrödinger equation with an effective one-electron potential representing these interactions. The solution yields a set of continuous functions ε_n (k) which from the band structure of the solid may be derived. For a semiconductor, all energy bands are either completely filled or completely empty in the ground states. Thus, the definition of the band gap (E_g) is the energy difference between the minimum E_C of the conduction band (the lowest empty band) and the maximum E_V of the valance band (the highest filled band). The conduction electrons and valence holes can be described as free particles with effective masses controlled by an effective mass tensor.

Completely filled and completely empty energy bands are electrically inert, consequently, the electrical properties of a semiconductor are mainly determined by the density of conduction electrons n_c and the density of valence holes p_V. These values are obtained from the densities of energy states in the bands and the Fermi-Dirac probability of their occupancy. The Fermi-Dirac distribution function is given by

$$F(E)=\left(1+\exp\left(\frac{E-E_F}{kT}\right)\right)^{-1} \qquad 4.1$$

where E_F is the Fermi level of the semiconductor, (E-E_F) is the distance from the Fermi level, k Boltzmann's constant, and T is the absolute temperature.

For a non-degenerate semiconductor, n_C and p_V are given by;

$$n_C = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) \quad 4.2$$

$$p_V = N_V \exp\left(-\frac{E_F - E_V}{KT}\right) \quad 4.3$$

where N_C and N_V are the effective densities of states in the bands and E_F is the semiconductor Fermi energy.

Silicon and germanium have the same lattice structure as diamond where each silicon atom is surrounded by four neighbouring atoms forming a regular tetrahedron structure, figure 4-2. At room temperature the band gap energy of silicon is E_g = 1.12 eV, and the effective densities of states in the bands are N_C = 2.86x10^{19} cm^{-3}, and N_V = 3.1x10^{19} cm^{-3} [Green, 1990].

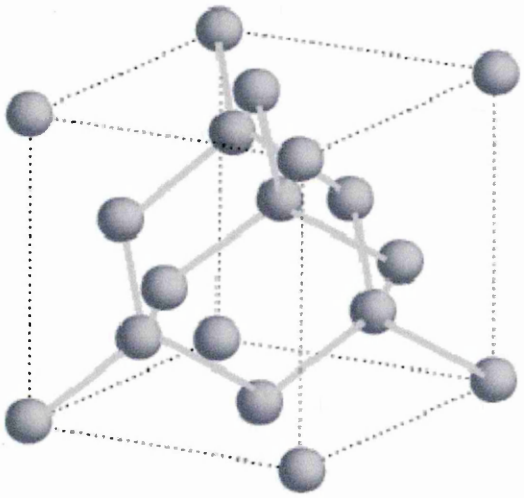


Figure 4-2 Silicon, germanium and diamond crystal structure [Sze, 1985].

4.4 Crystal defects

All real crystal lattices have imperfections in the arrangement of their atoms. For example, there are numerous crystallographic defects that may occur during the growth and subsequent processing of crystalline semiconductors. Such defects arise in many ways; implantation of host atoms, irradiation of the crystal, or adding doping elements to the melt before the crystals are grown. Additionally, a real crystal (such as a silicon wafer) may differ from the ideal crystal in important ways not only because of the

presence of lattice defects, but also because of thermal vibration of lattice atoms around their equilibrium positions.

Defects play a very important role in semiconductor devices as they have considerable influence on material properties such as resistivity and dielectric strength. Many electronic devices are essentially based on the controlled introduction of defects in the crystal. The perfect single crystal semiconductor has a band diagram which consists of a valence band (E_V), and a conduction band (E_C) separated by the band gap (E_g). When the periodicity of the single crystal is perturbed by foreign atoms or crystal defects the resulting lattice imperfections distort the electronic potential and may result in the introduction of discrete energy levels into the band gap, see also Section 3.2.

The defect energy levels are usually categorized as either shallow or deep. The addition of a substitutional group V/III impurity can be represented as a fixed charge +e/-e on top of a host atom along with an additional electron / hole. Dopants from group V (e.g., phosphorus with ionization energy 0.044 eV) and group III (e.g., boron with ionization energy 0.046 eV) are labelled donors and acceptors, respectively. A semiconductor doped with donors/acceptors is called n-type/p-type due to the excess of conduction electrons/valence holes in comparison to the carrier type. The other defects form a stronger electronic potential that binds the carriers more efficiently. These deep level defects/traps introduce energy levels deeper in the band gap at a position denoted E_t. In thermodynamic terms, the band structure represents Gibbs free energies. Thus, the ionisation energy (E-E_F) is correctly interpreted as the change ΔG_n in Gibbs energy by the excitation of an electron from a deep level to the conduction band, i.e., the Gibbs energy difference between (1) the empty centre and the conduction electron and (2) the centre with a trapped electron it is temperature dependent. Thus;

$$E_c(T) - E_t(T) = \Delta G_n(T) = \Delta H_n - T\Delta S_n \qquad 4.4$$

where ΔH_n, and ΔS_n are corresponding changes in enthalpy and entropy, respectively. A similar result applies to the hole ionisation energy E-E_F. Figure 4-3 shows the donor (E_D) and acceptor (E_A) levels in the conduction band.

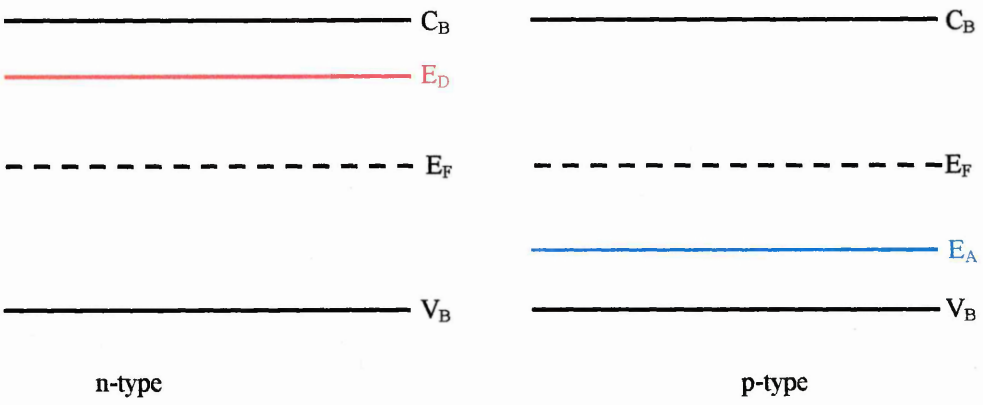


Figure 4-3 The donor and acceptor levels in the conduction band

4.4.1 Shallow level defects

As we have mentioned before in Section 4.1, shallow level defects are formed by introducing a new atom as a dopant which replaces the original atom (i.e. it is substitutional). Atoms from group III (e.g. boron) and group V (e.g. phosphorus) are shallow impurities for group IV elements (silicon or germanium). They are known as either donors or acceptors depending on whether they contribute electrons or holes. They are fully ionised at room temperature, so they increase the conductivity of the material.

4.4.2 Deep level defects

For silicon, germanium and gallium arsenide deep level defects are typically metallic impurities, e.g. iron, gold or copper. Deep levels are also introduced by crystal imperfections, such as dislocations, which introduce energy levels near the middle of the energy gap and can have substantial impact on the performance of electronic devices. Such energy levels are typically within the range from 0.1eV below the conduction band to 0.1 eV above the valence band [Sze, 1990]. Deep level defects have an effect upon carrier behaviour in semiconductors; as they may enable lattice constituents to have a much greater mobility than that predicated in an ideal crystal since the diffusion can progress stepwise from vacancy to vacancy [Wolf, 1971] or can be interstitial-assisted. Antimony (Sb) diffuses by a vacancy-mediated mechanisms, whereas boron and phosphorous both have interstitial-assisted diffusion.

Unlike shallow dopants, deep level defects can often exist in more than two charge states. As a result of Coulomb interaction between the carrier and the charged centre, an electron is more strongly bound to a positively charged centre than to a neutral or negatively charged centre. This natural sequence of levels is illustrated in figure 4-4.

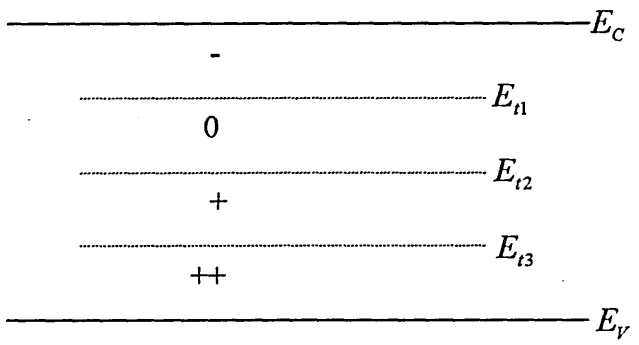


Figure 4-4 Deep energy levels of an arbitrary defect centre, which can exist in four charge states. The absolute state of the defect is dependent on the position of the Fermi level.

The charge state of a deep energy level is labelled in accordance with the absolute charge states of the defect before and after the carrier emission. A transition from a negatively charged defect to one that is neutrally, by electron emission, is labelled (-/0) and is also called a single acceptor level, while a transition from a positively charged defect to one that is neutrally, by hole emission, is labelled (+/0) and also called a single donor level.

4.4.3 Extended defects

Defects in semiconductors may be classified according to their dimensions, e.g. point defects are zero dimensional defects. Self-interstitials and vacancies count for most defects within this classification. Impurity atoms on interstitial and substitutional sites and small complexes of impurities, sometimes in conjunction with interstitials or vacancies are also denoted as point defects. Dislocations are one-dimensional defects, while stacking faults, twin and grain boundaries are two dimensional defects. Precipitates of impurity atoms may form three-dimensional defects in semiconductor materials.

Twins, dislocations and stacking faults are the three most important types of extended defects in epitaxial films [Mahajan and Harsha, 1999]. Twinning, see figure 4-5 is a gross defect which occurs when part of the crystal transforms into the mirror image of the other across the twin plane. It may occur during crystal growth or may be produced by mechanical shear of successive planes of atoms.

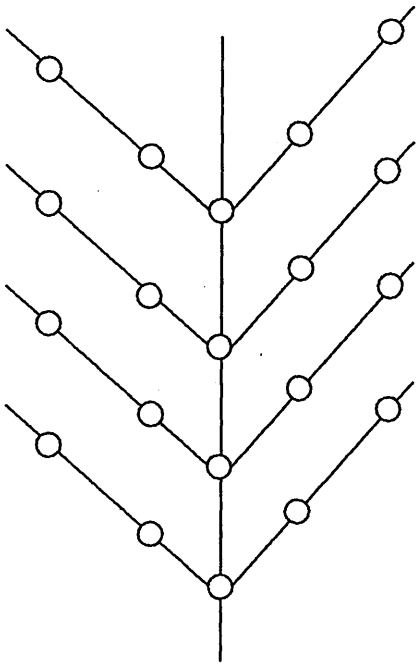
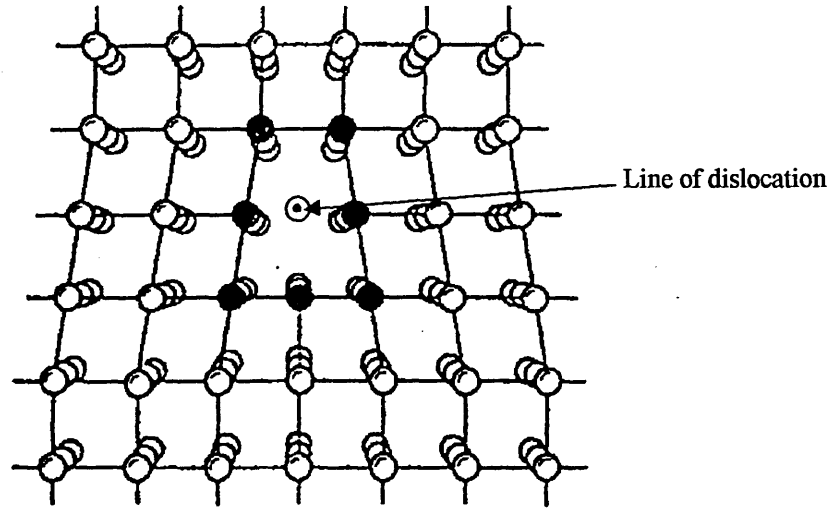


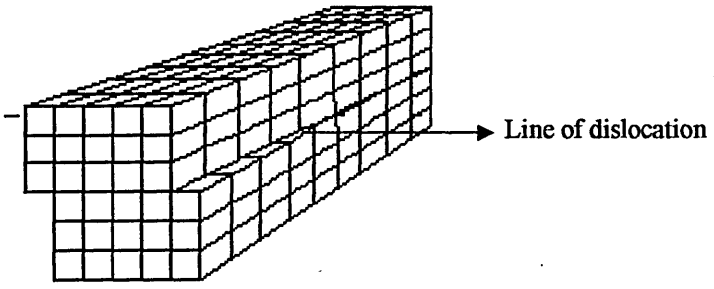
Figure 4-5 Two-dimensional representation of a twinned crystal [Tyagi, 1991]

Grain boundaries occur as inclusion defects. Sometimes small particles of metal, dielectric or refractory materials get incorporated into the crystal during its growth, and these particles form a precipitate near dislocation sites or vacancies.

There are two main dislocation types [Friedel, 1964]; edge and screw dislocations. Dislocations are types of line defects, as shown in figure 4-6. They result when one part of the crystal slips relative to another part within the crystal. These are dynamic defects, which can move under applied stress, dissociate into partial dislocations, or interact with other dislocations. Dislocations may be introduced by thermal stress on the silicon wafer during processing or by the introduction of an excessive concentration of an impurity atom, such as the end-of-range damage in implanted material which consists of dislocation loops.



(a)



(b)

Figure 4-6 (a) Schematic diagram of a crystal containing an edge dislocation. (b) Geometry of a screw-type dislocation [Tyagi, 1991].

Smith [1995] discusses how, in epitaxial films, dislocations are generated in several ways: distortion of the surface structure, e.g., particles on the substrate surface may result in the formation of dislocations when the crystal grows over them; the stress resulting from mismatch of lattice SiGe between substrate and film may be reduced by the formation of dislocations; any dislocation that is present in the substrate will be continued in the epitaxial film.

At dislocations, the distorted lattice structure represents a preferred gettering site for impurities. Dislocation core states (dangling bonds), as well as decoration of dislocations with impurities might result in electronic defect levels in the band gap with a high recombination activity [Weber, 1994].

Stacking faults represent an irregularity in the stacking sequence of the crystal lattice. No broken bonds remain at a stacking fault. Nevertheless, stacking faults might be associated with shallow electronic levels in the band gap [Weber and Alexander, 1983; Letho, 1997]. For epitaxial growth, the formation of stacking faults has an enormous impact on the crystalline quality.

4.5 Effects of defects

When the regularity of the crystalline lattice is disturbed, caused by bulk damage, new energy levels in the forbidden energy gap occur. Macroscopic evidence for this is available from changes in the bulk electrical characteristics as will be discussed in the following sub-sections..

4.5.1 Leakage currents

In the depletion region of a silicon device, a small leakage current can arise from the thermal generation of electron - hole pairs as some electrons gain sufficient energy to move from the valence band into the conduction band, leaving a hole in the valence band and an electron in the conduction band. A large leakage current will arise from the presence of mid band gap defects. The generation process may be considered in terms of the defect centre simultaneously emitting a hole into the valence band and an electron into the conduction band. In practice, deep levels can interact with leakage related to carriers in the conduction band or valence band [Chen *et al*, 1984; Kyu *et al*, 1990]. In many cases the majority carrier capture rate when a leakage current is present cannot be neglected in comparison with the majority carrier emission rate. In such cases the leakage current has a very serious influence on the DLTS spectra and therefore on deep level parameter determination [Chen *et al*, 1984; Kyu *et al*, 1990]. It can thus lead to an incorrect interpretation of experimental results. In spite of this no practical method to analyse DLTS spectra has been proposed which allows one to obtain the real values of the deep level parameters in Schottky diodes with non-negligible leakage currents.

During DLTS measurements, the peak amplitude decreases much more strongly with a slower rate window than expected (as shown in Chapter Five). This has been attributed to competition between carrier capture due to leakage current and thermal emission [Schroder, 1998].

4.5.2 Lifetime shortening

Charge carrier lifetime is an important parameter for many kinds of silicon devices and control of the charge carrier lifetime is a key factor in optimisation of device performance. Carrier lifetimes may be defined as the mean times spent by excess electrons and holes in the conduction and valence band respectively. Consider a disturbance of electron density added to a thermal equilibrium level of n_o electrons cm^{-3}. When the source of the disturbance is cut off, the semiconductor returns to equilibrium under the influence of a recombination process and thermal generation process [Rein *et al*, 2002]. The mean carrier lifetime, τ_n, is the time for the disturbance to reduce to $1/e_n$ of its original value where e_n is electron emission rate [Milnes, 1973]. Carrier lifetime is very sensitive to the presence of electrically active defects. It is important to have short values of lifetime to obtain fast switching, but necessary to have long lifetimes for devices such as detectors.

Although DLTS is accepted as one of the most sensitive methods to detect and analyse small concentrations of electrically active defects, defect concentrations below its detection limit can still significantly affect carrier recombination lifetime [Lang, 1974]. Due to this high sensitivity of carrier lifetime to electrically active defects, lifetime measurements can be used to characterize material quality. Apart from detecting the presence of recombination active defects, lifetime measurements can be used for direct identification of defects if the temperature and injection dependence of carrier lifetime are known [Rein *et al*, 2002].

At a constant temperature, in equilibrium, the recombination rate of electron - hole pairs will balance the thermal generation rate. This recombination occurs during the transition of an electron from the conduction band into a vacancy in the valence band. The energy thus released is roughly equal to the energy gap, E_g and may be expressed either as a photon, or as vibration in the crystal lattice (phonon). The recombination mechanism itself will decide the photon / phonon outcome. Photon release is known as radiative recombination, while the non-radiative process results in the creation of a lattice phonon.

Recombination takes place in two ways; band-to-band and defect assisted. In the band-to-band process, figure 4-7 (a) there is a direct electron jump from the conduction to valence band, where it recombines with a hole. In the defect centre process, it is only

at a defect that recombination can take place [Wilson and Hawkes, 1989]. The nature and energy level of the defect centre will determine the exact mechanism of a defect centre recombination event. One such process is illustrated in figure 4-7 (b) where as a first step (i) an electron is trapped by a recombination centre which subsequently captures a hole. When both of these events have occurred the net result is the annihilation of an electron-hole pair (ii), leaving the centre primed for another recombination event. The energy released (iii) is given to the lattice as a phonon [Wilson and Hawkes, 1989].

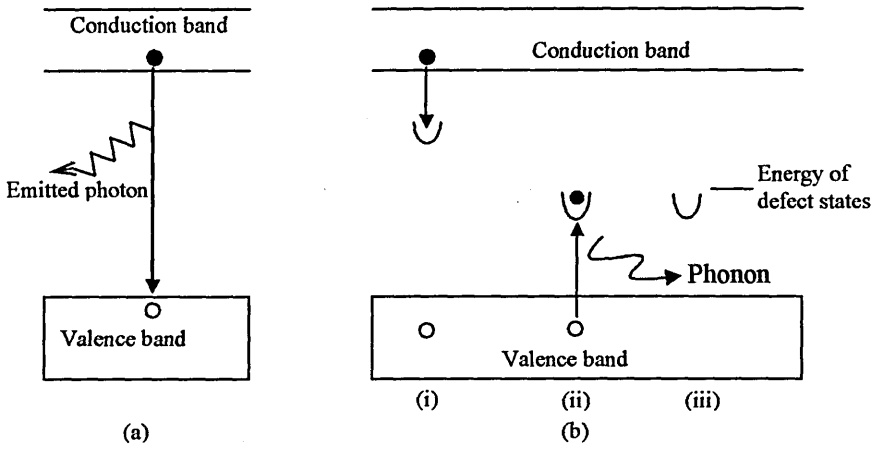


Figure 4-7 (a) Band to band recombination (b) recombination via a defect centre. The first step in (b) is (i) the trapping of an electron followed by (ii) hole capture. This result in the annihilation of an electron hole pair and emission of a phonon, leaving the centre ready to participate in another recombination (iii) [Wilson and Hawkes, 1989].

4.5.3 Transient enhanced diffusion

Ion implantation of, for example, boron for doping will require one or more annealing treatments in order to activate the dopant and to remove the primary crystalline defects generated by ion bombardment. Nevertheless, the possibility also exists of excess interstitials combining with dopant atoms to induce transient enhanced diffusion (TED) during subsequent thermal processing [Stolk *et al*, 1995; Tamura *et al*, 1987]. This TED of all atoms that diffuse via an interstitial mechanism is an inevitable result of annealing after ion implantation as, on average, one excess interstitial is created for every ion implanted. The result is that the diffusion rate during the first few

seconds of annealing is much greater than usual. TED will thus broaden the profile of all affected implants both high and low dose.

4.6 Interactions of defects with the conduction and valence bands

4.6.1 The rate equation

Consider a trap of volume density N_t which introduces a deep energy level into the band gap at a position E_t. The level can interact with the conduction band and the valence band through emission and capture of electrons and holes. Thus the following four processes need to be considered, see figure 4-8:

1. Emission of electrons to the conduction band, with emission rate e_n.
2. Emission of holes to the valence band, with emission rate e_p.
3. Capture of electrons from the conduction band, with capture rate C_n.
4. Capture of holes from the valence band, with capture rate C_p.

The volume of density n_t of filled traps is determined by the competition of these four processes. The emission of electrons and capture of holes takes place from the n_t filled traps, while the emission of holes and the capture of electrons takes place from the (N_t-n_t) empty traps. Thus, the interactions are described by the rate equations;

$$\frac{dn_t}{dt} = -(e_n + C_p)n_t + (C_n + e_p)(N_t - n_t) \qquad 4.5$$

Equation 4.5 form the basis for mapping deep levels by DLTS. The steady state occupancy ratio of the trap is determined by the condition $dn_t/dt = 0$ as;

$$\frac{n_t(\infty)}{N_t} = \frac{C_n + e_p}{e_n + C_n + e_p + C_p} \qquad 4.6$$

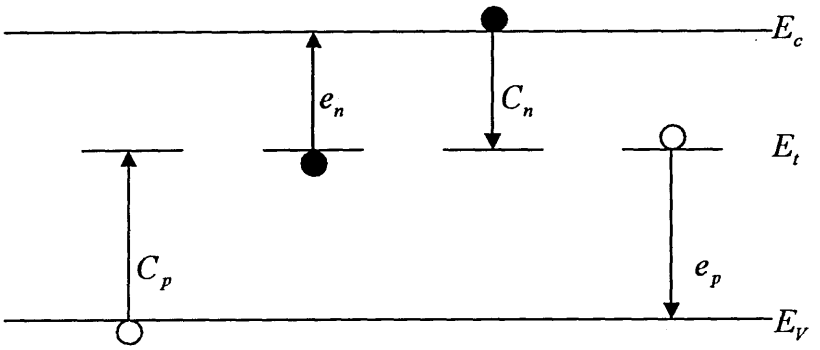


Figure 4-8 Interactions between a deep energy level and the two bands. Electrons and holes are represented by filled and open symbols, respectively.

In n-type material [this description is for electrons in n-type materials, but an analogous description can be gives for holes in p-type material] consider the special cases where (1) all traps are initially empty and electron capture is the dominant process (2) and all the traps are initially filled and electron emission the dominant process. In these two cases, the solution to equation 4.5 is given, respectively by;

$$n_t(t) = N_t(1 - \exp(-C_n t)) \qquad n_t(0) = 0, \quad C_n >> e_n, e_p, C_p \qquad 4.7$$

$$n_t(t) = N_t \exp(-e_n t) \qquad n_t(0) = N_t, \quad e_n >> C_n, e_p, C_p \qquad 4.8$$

Thus the volume density n_t of filled traps relaxes exponentially towards the steady state values nt (∞) = N_t for the capture process and nt (∞) = 0, for the emission process. The time constants for the processes are given by the inverse capture rate C_n^{-1} and the inverse emission rate e_n^{-1} respectively.

4.6.2 The capture process

The electronic capture rate C_n is proportional to the flux of conduction electrons (electrons per unit area per unit time) that pass the defect. Thus;

$$C_n = \sigma_n \langle v_n \rangle n_c \qquad 4.9$$

where

$$\langle v_n \rangle = \sqrt{\frac{3kT}{m_c^*}} \qquad 4.10$$

$\langle v_n \rangle$ is the average thermal velocity of conduction electrons and the proportionality constant σ_n is the electron capture cross section and has units of area (cm^2). The value of the capture cross section is of the order of atomic dimensions and describes the effectiveness of the centre in capturing electrons. The product $\sigma_n \langle v_n \rangle$ is known as the capture coefficient (units of $cm^3 s^{-1}$). The capture cross section can be independent of temperature or can be thermally dependent. In the latter case, the cross section is usually found to follow the behaviour;

$$\sigma_n(T) = \sigma_n^{\infty} \exp\left(-\frac{E_{\sigma_n}}{kT}\right) \qquad 4.11$$

where E_{σ_n} is the energy barrier for capture of electrons and σ_n^{∞} is the electron capture cross section in the limit $T \rightarrow \infty$ [Henry and Lang, 1977]. In most cases, the value of the carrier capture cross section can indicate the charge state of the defect centres, the carrier capture cross section is expected to be $\geq 10^{-14}$ cm^2 for the attractive centre, in the range $10^{-16} - 10^{-14}$ cm^2 for a neutral centre, and in the range $\leq 10^{-17}$ cm^2 for a repulsive centre.

4.6.3 The emission process

In thermodynamic equilibrium, the principle of detailed balance applies. This principle states the exchange of electrons between the deep level and the conduction band and the exchange of electrons between the deep level and the valence band are both balanced, i.e., $e_n n_t = C_n(N_T - n_t)$ and $e_p(N_T - n_t) = C_p n_t$. Combining this principle with Fermi - Dirac statistics yields the electron emission rate;

$$e_n = \sigma_n \langle v_n \rangle \frac{g_0}{g_1} N_c \exp\left(-\frac{E_c - E_t}{kT}\right) \qquad 4.12$$

where g_0 and g_1 are the degeneracies of the empty and filled energy levels, respectively. The temperature dependence of the electron emission rate is determined

from the temperature dependencies of the thermal velocity (see equation 4.10), the electron capture cross section (see equation 4.11), the ionisation (see equation 4.4), and the effective density of states ($N_C \propto T^{3/2}$) [Green, 1990]. The result is;

$$e_n(T) = \gamma_n T^2 \sigma_n^2 \exp\left(-\frac{E_n^a}{kT}\right) \qquad 4.13$$

where

$$E_n^a = \Delta H_n + E_{\sigma_n}, \qquad 4.14$$

$$\sigma_n^a = \frac{g_0}{g_1}\sigma_n^\infty \exp(\Delta S_n/k) \qquad 4.15$$

and γ_n is a constant.

Thus, a plot of $\ln[e_n(T)/T^2]$ versus inverse temperature (T^{-1}) (an Arrhenius plot) gives a straight line with gradient E_n^a/k and intercept of $\ln(\gamma_n \sigma_n^2)$ on the e_n/T^2 axis characterised by the activation energy E_n^a and the apparent electron capture cross section σ_n^a, respectively. This however does not directly determine the ionization energy, E_c-E_t, or the true electron capture cross section, σ_n. In some cases of temperature independent electron capture, the activation energy, E_n^a, equals the enthalpy change ΔH_n for the emission process.

The emission rate, e_p, for emission of holes to the valence band is described by expressions equivalent to equations 4.12, and 4.13. For Coulomb attractive centres, the enhancement of the emission rate is often caused by a lowering of the Poole-Frenkel effect, an explanation originally developed by Frenkel and later extended to a three dimensional model by Hartke [1968]. For an electron attracted to a singly positively charged centre and under the influence of a uniform electric field ε, the ratio between the emission rate $e_n(\varepsilon)$ in the electric field and the zero field emission rate e_n (0) is given by;

$$\frac{e_n(\varepsilon)}{e_n(0)} = w^{-2}\left[1+(w-1)\exp(w)\right]+\frac{1}{2} \qquad 4.16$$

where k is Boltzmann's constant, the field parameter $w = \frac{\sqrt{e^3\varepsilon/\pi\varepsilon_s}}{kT}$ and ε_s is the semiconductor dielectric constant [Hartke, 1968].

Thus, the observation of a Poole-Frenkel effect can be indicative of a charged defect centre. However, an enhancement of the emission rate in an electric field must be interpreted with care as other mechanisms (e.g., tunnelling and impact ionization) can produce a similar effect for neutral as well as charged centres. Recently, the problem of distinction between these effects was considered by Ganichev *et al*, [2000]. It was concluded that, for coulombically attractive centres, the Poole-Frenkel effect is the dominant effect at relatively low electric field strengths. At larger field strengths, the stimulation of the emission process is dominated by phonon assisted tunnelling, which enhances the emission rate exponentially with the square of the electric field strength. For neutral centres, phonon assisted tunnelling is the dominant effect even at small fields.

4.7 Summary

Because silicon still dominates the semiconductor market, a brief overview of its defects has been introduced. A definition for the trap or recombination centre has been given, and in Section 4.3 a brief examination of the crystal and band structure of silicon and germanium has been made. The following Section, 4.4, defined the crystal defects and introduced three common crystal defects: shallow level defects. In Section 4.5 the effects of defects on the behaviour of the silicon semiconductor were introduced. These can be divided into an effect on leakage currents, lifetime shortening and transient enhanced diffusion. Finally, interactions with the conduction and valence bands are introduced. In the next chapter a review of Schottky diode, its fabrication and characteristics will be given.

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Chapter 5

Schottky diode

5.1 Introduction

This chapter introduces the Schottky diode and its operation. The simplest method of producing a working semiconductor device is to fabricate an interface where a metal and either an n-layer or p-layer of material are in contact. While the point contact diode was the first application of this type of junction, nowadays the Schottky diode can be formed by plating, evaporating or sputtering a variety of metals onto a semiconductor [Ahmed, 1998]. The metal-semiconductor properties of nearly all semiconductors in contact with a variety of metals have been investigated in one form or another [Cirovic, 1971; Whitaker, 2000].

The properties of forward-biased Schottky diodes are determined by majority carrier phenomena, whereas in p-n junction diodes the properties are mainly determined by minority carriers. As a result, the Schottky diode can be switched rapidly from forward to reverse bias without minority carrier storage effects. The typical current versus voltage curve of a Schottky barrier diode resembles that of a p-n junction; however, the reverse breakdown is lower and the leakage higher than in a p-n junction diode using the same resistivity n-type material, and the forward voltage at a specific forward current level is generally lower for a Schottky diode than for a p-n junction.

Figure 5-1 shows the energy band diagram of a Schottky barrier of a metal and a p-type semiconductor. Figure 5-1 (a) shows the situation before contact and figure 5-1 (b) shows the resulting Schottky barrier after contact. At equilibrium, in absence of

externally applied voltages, the Fermi level must be constant throughout the sample, since otherwise a current would flow [Stallinga, 2000].

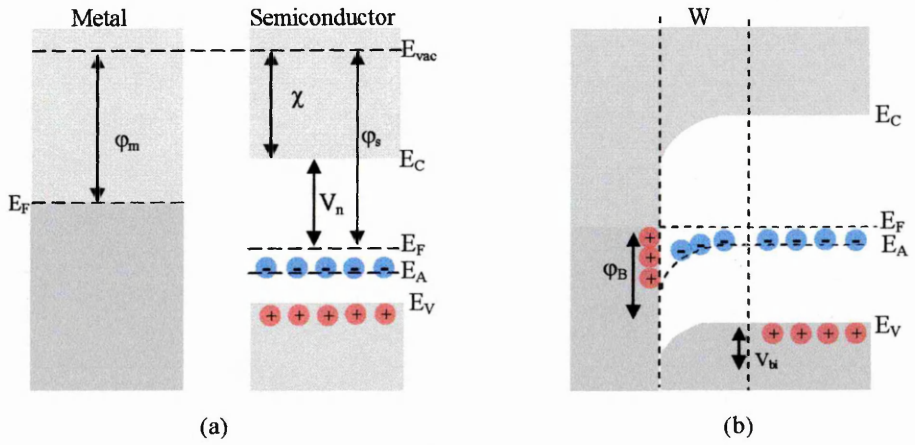

Figure 5-1 (a) A metal and a semiconductor before contact. (b) A Schottky barrier formed after contact between metal and semiconductor. A region of uncompensated charged acceptors results. This causes a voltage drop at the interface [Stallinga, 2000].

The conduction properties of metal-semiconductor junctions depend on whether the semiconductor is p-type or n-type and on the relative magnitudes of φ_s and φ_m, where φ_s, and φ_m are the work functions of the semiconductor and metal respectively. The work function is the energy required to transfer an electron from the Fermi level to the vacuum level (well away from the atom), and the electron affinity (χ_s) is the energy difference between the bottom of the conduction band and the vacuum level [Sparkes, 1987; Schroder, 1998; Sze, 1981]. If $\varphi_m > \varphi_s$ for n-type silicon, or $\varphi_m < \varphi_s$ for p-type silicon, the redistribution of charge at formation creates non-linear conduction properties whereby the junction conducts well in one direction but poorly in the opposite direction [Brennan, 1999]. This called a Schottky diode contact. Therefore, when putting a metal next to a semiconductor either a Schottky contact or an Ohmic contact is formed, depending on the concentration, the interface properties, and the difference between the work functions of the metal and semiconductor. The work functions of a number of common substrates are given in table 5-1 [Cooke, 1990; Sparkes, 1987, Sze, 1981].

Material	Work functions (φ) eV
Aluminium	4.1
Caesium	1.9
Carbon	4.8
Copper	4.3
Gold	4.8
Iron	4.6
Platinum	6.3
Silver	4.7
Thorium	3.5
Tungsten	4.5

Table 5-1 Work functions of common substances [Cooke, 1990].

Schottky barrier diodes based on the rectifying properties of the Schottky barrier have some advantages over p-n diodes including;

1. The most important advantage is their dynamic behaviour. In a Schottky diode carriers are injected into the metal but cannot be stored there as an excess charge, thus there is no delay in the reverse recovery phase of the diode unlike p-n diodes. The Schottky diode responds more quickly when the current is reversed.

2. Metal-semiconductor contacts have a depletion region at the interface. The current in such a diode is determined mainly by thermal emission of majority carriers from the semiconductor into the metal across a potential barrier (ΔV_B).

5.2 Energy band diagrams for metal-n-type semiconductor

The energy band diagrams for a metal-n-type semiconductor are shown in figure 5-2. Figure 5-2 (a) shows the two materials separately, in order to compare the relevant energy levels within and between the two solids. In an extrinsic semiconductor, the location of the Fermi level (E_F) is determined by the degree of doping of the semiconductor. Therefore the Fermi level is not fixed with respect to the conduction and valence bands.

In figure 5-2 (b), if $\varphi_m < \varphi_s$ then the electrons in the metal have an average total energy that is higher than those in the semiconductor. If $\varphi_m > \varphi_s$, the electrons in the semiconductor have an average total energy greater than those in the metal. At the point of contact, since the Fermi level of the semiconductor is higher than that of the metal, electrons will transfer from the semiconductor into the metal until equilibrium is reached and the Fermi levels realigned [Bar-Lev, 1984; Mouthaan, 1999].

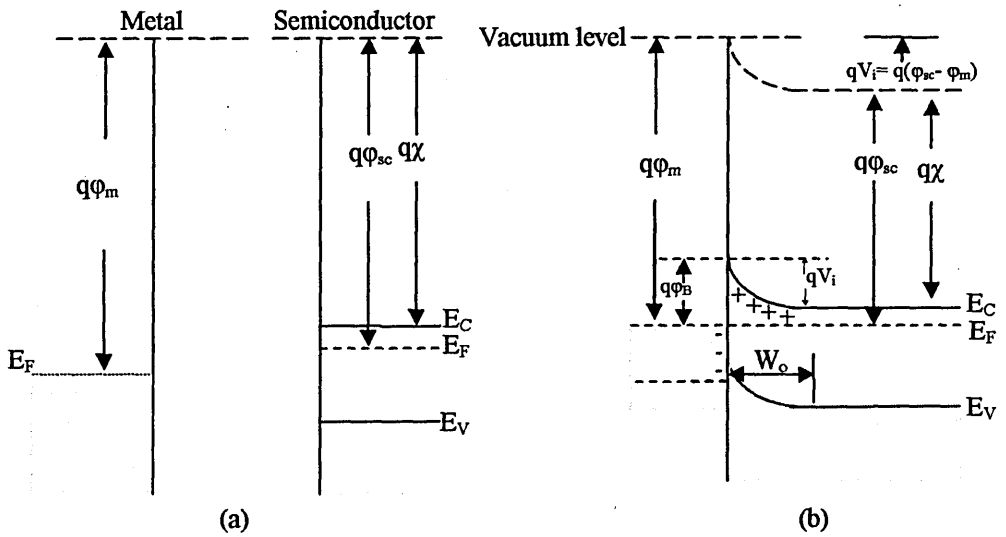

Figure 5-2 Energy band diagrams of metal-n-type semiconductor contact (a) two materials isolated from each other, (b) thermal equilibrium situation after the contact is made [Tyagi, 1991].

As a result of the flow of electrons from the n-type semiconductor to the metal, a depletion region is established in the semiconductor surface consisting of positively ionised donor atoms. An electric field between the semiconductor and the metal is thus built and a potential barrier is established. As a result the conduction band and the valence band in the semiconductor in the region of the depletion layer are bent, as shown in figure 5-2 (b). The bending of the conduction band is accompanied by an identical bending of the vacuum level of the semiconductor. In both the semiconductor and metal the vacuum level, E_o, is still the energy level at which an electron is no longer bound to an atom. The derivative of the conduction band shape of the semiconductor is greatest where the semiconductor is in contact with metal, where the electric field is largest. Since the Fermi energy level is fixed, the increase in the energy difference

between the conduction band and the Fermi level ($E_C - E_F$) in the semiconductor near the surface results in a reduced electron density at the surface in contact with the metal. After contact formation, the distribution of the density of electrons above the bottom of the semiconductor conduction band is identical in both the metal and semiconductor [Dimiterijev, 2000].

After contact, an energy barrier, qV_i, is formed in the semiconductor at the surface in contact with the metal. There is no depletion region or layer and no voltage drop in the metal. This is because the metal is assumed to be a perfect conductor with zero resistance, which does not permit the formation of an electric field and the sustaining of a voltage drop. The barrier for electrons in the metal is known as a Schottky barrier. One of the important characteristics of a Schottky barrier is its height $q\varphi_B$, which is the energy difference between the aligned Fermi levels and semiconductor band edge at the surface with the metal. The Schottky barrier represents the energy barrier that electrons in the metal must overcome to move into the semiconductor, assuming ideal contact

$$q\varphi_B = q(\varphi_m - \chi). \qquad 5.1$$

where $q\chi$ is the electron affinity of semiconductor, the difference in the energy between the vacuum level, E_o, and the bottom of the conduction band E_C at the contact surface . The barrier which prevents electrons that are in the contact region of the semiconductor from moving into the metal is qV_i and given by

$$qV_i = q(\varphi_m - \varphi_{sc}) \qquad 5.2$$

Since the built-in voltage at equilibrium appears only in the semiconductor and as the metal cannot sustain a voltage difference, any voltage that is applied appears entirely in the semiconductor and the barrier height in the metal, the Fermi level and the conduction band edge of the semiconductor at the surface will be unchanged. As a consequence, the density of electrons in the metal that have energies greater than this barrier is unchanged from its equilibrium value.

An applied voltage causes a change in the degree of bending of the bands in the semiconductor and a corresponding change in the electric field in the semiconductor at the junction with the metal. The barrier in the semiconductor is reduced when a forward

bias is applied. This bias reduces the electric field and degree of bending of the bands. As the barrier is reduced more electrons (in n-type), compared to thermal equilibrium, cross from the semiconductor to the metal. On the other hand, the number of electrons that cross from the metal to semiconductor is unchanged from the number that cross at thermal equilibrium because the barrier height, $q\varphi_B$, is unaffected by the applied voltage and unchanged from its thermal equilibrium value of $q(\varphi_m - \chi_s)$.

As the reverse bias increases the barrier height in the semiconductor increases, and the electron current, which crosses from the semiconductor to the metal, is reduced compared to that at thermal equilibrium.

5.3 Energy band diagrams for metal-p-type semiconductor

At a contact between a metal and a p-type semiconductor where $\varphi_m < \varphi_s$, see figure 5-3, electrons move from the metal into the semiconductor and the Fermi levels are aligned. The electrons that move into the semiconductor recombine with the holes in the semiconductor, leaving negatively charged uncompensated acceptor ions in the semiconductor to form a depletion layer whose width depends upon the doping of the semiconductor. On the metal side, a layer of positive charge is formed at the interface with the semiconductor. There is thus an electric field directed from the metal to the semiconductor, a downward bending of the energy bands in the semiconductor occurs, see figure 5-3, and an energy barrier is formed. The downward bending of the energy bands in the semiconductor corresponds to an upwards bending of the potential, and the built-in voltage (V_i) in the semiconductor is equal to φ_m - φ_s. The contact is rectifying and the barrier from the metal to the semiconductor valence band ($q\varphi_B$) is ($q\chi_s + E_g$ - $q\varphi_m$). This energy separation is between the aligned Fermi levels at the surface of the valence band in the semiconductor, in contact with the metal. Here the electrostatic potential barrier to hole motion is opposite to the direction of the barrier in the electron energy band diagram. Therefore, the highest energy level of a hole in the semiconductor is at the surface where the valence band curve meets the metal surface. While holes at that surface have the highest energy, they are not numerous. This is because of the large separation of this level from the Fermi level compared to the separation experienced by holes in the bulk of the semiconductor.

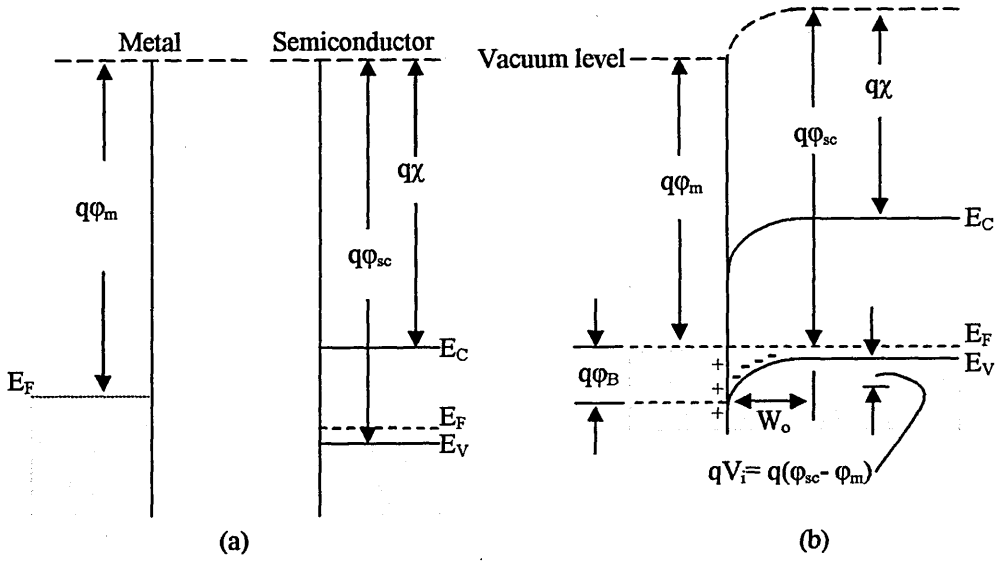

Figure 5-3 Energy band diagrams of a metal-p-type semiconductor contact with $\varphi_m < \varphi_s$. (a) Materials isolated from each other, (b) situation after the contact is made and thermal equilibrium is reached [Tyagi, 1991].

When a forward voltage (Va), is applied the barrier to hole flow from the semiconductor to the metal is reduced. But, when the bias is reversed, the barrier to hole flow from the semiconductor to the metal is increased, so the current is negligibly small.

It is important to note that in both the metal-n-type semiconductor rectifying contact and the metal-p type semiconductor rectifying contact, the forward current is due to the motion of majority carriers from the semiconductor to the metal

5.4 Schottky barrier diode

The ideal value of barrier height of φ_{Bo}, is approached when the diode is strongly forward biased. The actual barrier height φ_B is less than φ_{Bo}. The built-in potential is V_{bi} (see figure 5-1 (b)) and V_o is the potential of the semiconductor Fermi level with respect to the conduction band. The current-voltage relationship of a Schottky barrier diode, neglecting series and shunt/ parallel resistance, is given by

$$I = I_s\left(\exp\left(\frac{qV}{nkT}\right)-1\right) \qquad 5.3$$

where I_s the saturation current, and n the ideality factor of the diode [Karadeniz *et al*, 2004, Cetin and Ayyildiz, 2005].

$$I_s = AA^*T^2 \exp\left(\frac{-q\varphi_B}{kT}\right) = I_{s1} \exp\left(\frac{-q\varphi_B}{kT}\right) \qquad 5.4$$

A is the diode area, A^* is the effective Richardson's constant, $I_{s1} = A\,A^*\,T^2$ and $A^* = 4\pi qk^2m^*/h^3 = 120(m^*/m)A/cm^2$, where k is Boltzmann's constant, and φ_B the effective barrier height. A^* does not always follow the value predicted by this relationship even when quantum mechanical reflection at the interface and phonon scattering is considered [Schroder, 1998], for example, a Schottky diode is unlikely to be uniform over its entire area. The ideality factor n incorporates all these unknown effects which make the device non-ideal. This leads to $n > 1$ and also explains other effects such as n decreasing with temperature and with increasing reverse bias. The maximum value of n is 2.2, with an ideal value of 1.2 for diamond. Equation 5.3 is sometimes expressed as [Schoder 1990];

$$I = I_s \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right] \qquad 5.5$$

For I-V methods, the barrier height is most commonly calculated from the current I_s, determined by an extrapolation of the log(I) versus V curve to V= 0. I_s is found from the intercept of the straight line on the log (I) axis. The barrier height φ_B is calculated from I_s in equation 5.4 according to

$$\varphi_B = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_s}\right) \qquad 5.6$$

The barrier height φ_B is found for zero bias. The most difficult to determine of the parameters in equation 5.6 is A^*, rendering this method only as accurate as knowledge of A^* [Schroder, 1998].

5.5 Depletion region capacitance

A change in the voltage across the Schottky barrier junction causes a change in the depletion region, and hence causes a change in the junction capacitance [Burford and Verner, 1965]. The depletion region capacitance can be written as [Sharma, 1984, Singh 1994],

$$C = A\left[\frac{q\varepsilon N_d}{2\left[V_i - \left(kT/q\right) - V_{app}\right]}\right]^{\frac{1}{2}} \qquad 5.7$$

where the term (kT/q) is the contribution of electrons to the space charge. When this term is omitted the capacitance can be expressed as:

$$C = A\left[\frac{q\varepsilon N_d}{2(V_i - V_{app})}\right]^{\frac{1}{2}} \qquad 5.8$$

$$C = A\frac{\varepsilon}{w} \qquad 5.9$$

This relation shows that the Schottky barrier junction capacitance can be regarded as the capacitance of a parallel plate capacitor with separation distance equal to the depletion region width (w). For a Schottky junction which contains deep traps, the energy level of the traps varies with respect to the (constant) Fermi level as do the other bands which are bent in the depletion region of the barrier (see figure 5.3). The occupation of the level (and hence its state of charge) will also vary, i.e. the electron traps which lie below the Fermi level (E_F) will be occupied and those which lie above it will be empty. Because the degree of band bending depends on the application of the bias voltage, the state of charge of the trap will depend on the bias and as a result the capacitance will be affected. The effect of traps on the capacitance of a Schottky barrier affords a very convenient method of detecting and characterising an extremely low concentration of defects. This leads to the idea of DLTS, discussed in Chapter 6.

5.6 Typical current-voltage characteristics

I-V tests may be used to determine the quality of the diode. In this technique the diode current (I) is measured as a function of the forward bias. In forward bias the diffusion current is initially much smaller than the generation-recombination term. However, as the forward bias is increased there will come a point at which the diffusion current will start to dominate. As the reverse bias is increased, the depletion region increases [Lenert, 1968].

Figure 5-4 shows the current-voltage characteristic of a typical n-type silicon – metal (gold) junction diode. The curve is not linear, and the diode will only begin to conduct well after a few tenths of a volt (typically 0.3V) are applied across it. This is the voltage needed to remove the depletion region. The curve shows some reverse current I_R. This leakage current is caused by minority carriers, but it is usually very small and consequently the (I_R) axis is sometimes calibrated in microamperes (μA) or nanoamps (nA). Reverse current is not significant until there is a large reverse bias across the diode and for this reason the V_R axis is sometimes calibrated in tens or hundreds of volts. However, if a certain critical value of V_R is reached the silicon diode will show a rapid increase in reverse current. This is known as the reverse breakdown point.

Ideally, when a forward voltage is applied, the resistance of the diode would be zero, and forward current flow which would be limited only by the external circuitry. On the other hand, the resistance of the diode would be infinite for reverse voltage with no current flow [Watson and White, 1977] (more explanation of I-V measurements will be given in Chapter 6).

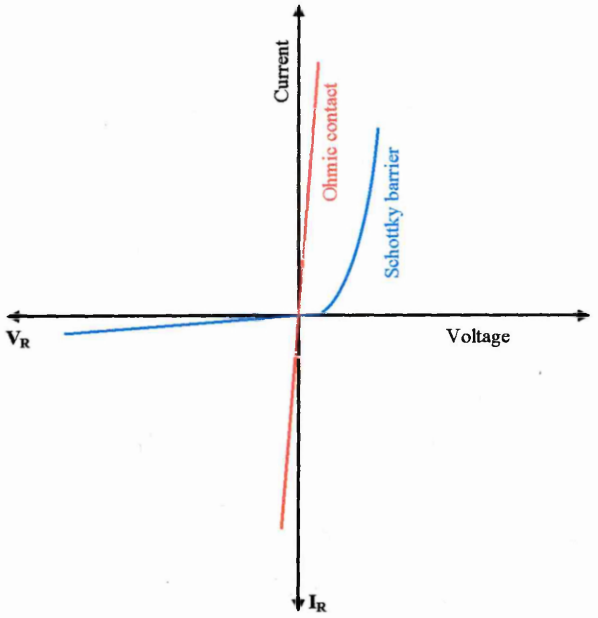

Figure 5-4 The current-voltage characteristics of Schottky diode and Ohmic contact on silicon [Shur, 1990].

5.7 Typical capacitance-voltage characteristics

C-V tests provide information on whether the diode has a high series resistance and the value of the phase angle. The depth profile indicates the concentration of carriers with depth, and also shows the variation of depletion region depth under different reverse-bias voltages. In C-V measurements the diode is reverse biased and the C-V measurements are made for a number of different dc bias voltages.

This measurement can determine the height of the barrier (φ_B), and gives the relation between the voltage and the impurity concentration N_d (m^{-3}), and the relation between depth and N_d. It is discussed in detail in the next chapter.

5.8 Summary

In this chapter we have illustrated how a Schottky diode functions. The energy band diagrams for metal-n-type and p-type semiconductor were presented and briefly discussed. In Sections 5-2, 5-3 the Schottky barrier diode that results from depositing a metal on the surface of a semiconductor was investigated. Mathematical equations that describe the current-voltage relationship of a Schottky barrier diode were given. Based on these equations it is possible to determine the factors that affect the behaviour of the Schottky diode. Finally, in Sections 5-6 and 5-7 the tools for characterising a Schottky diode have been introduced: particularly I-V and C-V characteristics.

In the following chapter the experimental techniques used to fully characterise the Schottky diode are given and described.

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Chapter 6

Experimental techniques

6.1 Introduction

This chapter describes the experimental techniques used in this work. I-V and C-V measurements of the fabricated diodes provide the electrical characterisation needed for DLTS and LDLTS measurements. Scanning electron microscopy measurements used to observe the grain boundaries in the semiconductor materials are described very briefly, and other experimental techniques such as admittance and impedance spectroscopy are discussed.

The thermally stimulated current (TSC) or capacitance (TSCAP) [Buehler and Phillips, 1972], and DLTS [Lang and Kimerling, 1979] techniques have had considerable success over many years in identifying and studying the dynamic response of deep states in crystalline semiconductors. Admittance measurements, first in the form of C-V, and later as functions of frequency and temperature, have been made for many years on p-n junctions, Schottky barriers, or metal-oxide-semiconductor (MOS) structures [Cohen and Lang, 1982].

6.2 Current-voltage and capacitance-voltage measurements

I-V and C-V characteristics are normally the first measurements to be carried out because they give information about the reverse leakage current and the series or parallel resistance of the junction diode prior to DLTS and LDLTS measurements. I-V measurements verify that the device being tested does indeed behave as a diode, and that its characteristics do allow it to be considered as a working device.

The C-V technique relies on the fact that the width (w) of the space charge region in a reversed biased semiconductor junction device depends on the applied voltage. This means that the capacitance also depends on the applied voltage, since width and capacitance, C, are related as shown in equation 6.1.

$$w = \left(\varepsilon_r \varepsilon_o A\right)/C \qquad 6.1$$

The depletion capacitance (C) of the Schottky diode on p-type material is given equation 6.2 [Singh 1994]

$$C = \left[\frac{q\varepsilon_r \varepsilon_o N_D}{2\left(V_{bi} - V_{app}\right)}\right]^{1/2} \qquad 6.2$$

where ε_r is the relative permittivity of the semiconductor material, ε_o is the permittivity of free space = 8.85×10^{-12} $C^2N^{-1}m^{-2}$, A is the surface area of the diode, C is the capacitance of the diode, V_{bi} is the potential barrier of the diode and V_{app} is the voltage applied across the diode. The characteristics of a Schottky junction may be used to obtain the carrier concentration profiles, and the width of the depletion region (w) is given by equation 6.3 (obtained by combining equation 6.1 and 6.2) [Singh 1994]

$$w = \left[\frac{2\varepsilon_r \varepsilon_o \left(V_{bi} - V_{app}\right)}{qN_D}\right]^{1/2} \qquad 6.3$$

The depletion region width of the Schottky diode can be varied by application of forward or reverse voltages. Switching the diode after a filling pulse into reverse bias gives rise to a capacitance transient which can be recorded via a digitised oscilloscope.

Equation 6.2 indicates that a plot of ($1/C^2$) against applied voltage should be expected to be linear, provided N_D is uniform, with a gradient equal to $2/q\varepsilon_r\varepsilon_o N_D$. A non-uniform N_D will be detected by the non-linearity of this plot. In this case, N_D may still be extracted from the data.

The spatial doping profile can be determined from the following equation:

$$N(w) = \frac{-C^3}{A^2 q \varepsilon_r \varepsilon_o \left(\frac{dC}{dV}\right)^{-1}} \qquad 6.4$$

In our work, a Hewlett-Packard model 4192 impedance analyser is utilised for these measurements.

6.3 Description of DLTS technique

About thirty years ago Kukimoto *et al*, [1973] used photocapacitance, Sah and Walker [1973] used TSCAP and Davies and Roosild [1971] used thermally stimulated current to study traps in semiconductors. In 1974 Lang [1974] described a powerful technique called Deep Level Transient Spectroscopy which had many advantages over methods then current, including:

1- relatively easy and quick to use,
2- much greater sensitivity,
3- a greater range of observable trap depth, and
4- it gave a spectroscopic-type output with universal signatures.

DLTS gives great sensitivity and covers traps over the widest range of the band gap. With such advantages DLTS has replaced thermally stimulated current and capacitance methods, and is now the most common deep level characterisation technique, allowing the precise electrical properties of some defects to be found in semiconductors.

This method of measurement is based on capacitance change with reverse bias when deep levels emit their carriers after a forward bias pulse has filled them. The emission rate is temperature dependent and characteristic for each type of defect. From the temperature dependence of the emission rate, the activation energy of a deep level (the energy required for the charge carrier to escape) can be deduced. With DLTS, it is also possible to measure the capture cross-section of a deep level since varying the pulse length varies the signal amplitude and this allows the capture cross-section to be deduced. As a high-frequency capacitance thermal scanning method, DLTS is useful for observing a wide range of traps in semiconductors. The presence of a peak is an indication that a carrier trap exists in the bandgap and the sign of the peak indicates

whether it is a majority or minority carrier trap. The height of the peak is proportional to the trap concentration while the position of the peak is uniquely determined by the thermal emission properties of the trap and depends on temperature. Thus traps of majority-carrier and/or minority-carrier types can be distinguished by this technique and such features as concentration, energy levels and capture rates can also be determined. It is possible for DLTS to characterise defects at a range of depths [Schroder, 1990].

Both impurities and intrinsic defects have been found at deep levels between E_C - 0.1eV and the mid-band gap in n-type materials, E_V-0.1 eV and the mid band gap in p-type materials. The intrinsic defects originate from crystal imperfections, whilst the impurities may have several sources: dopant atoms misplaced substitutionally or interstitially, intrinsic, anti-site intrinsic defects (where host atoms are wrongly sited in compound semiconductors), or Frank damage inflicted during ion implantation or electron irradiation. In the mid-band gap region deep levels can function as carrier traps or generation-recombination centres, thus distorting the design behaviour of the device concerned. As traps capturing free carriers, they can cause a gain in the resistivity (p) of the material, and may even induce intrinsic-like properties. As generation-recombination centres, they can all too easily provide a path for e-h pairs across the entire band-gap i.e., leakage current, an effect that can be both harmful to performance and, sometimes, beneficial [Henry *et al*, 1973].

DLTS can also be used to measure the emission of carriers from deep traps under thermal excitation, by applying a zero or forward bias to the diode, and then observing the transient after the diode is switched into reverse bias. The degree of capture and emission of carriers is recorded as a change in capacitance, which may be measured using a Schottky diode. This technique is very useful for observing a wide variety of deep levels in semiconductors, even though it is a survey technique with the main draw-back being that it is not precise and open to misinterpretation.

Deep levels may be characterised by three properties; activation energy (E_T) which is related to the position of the level in the band gap, trap concentration (N_T) and capture cross section (σ) which provides a measure of the ability of the deep level to trap carriers. DLTS allows measurement of all these properties directly.

The emission and capture processes which characterise a particular trap are summarised in figure 6-1. The symbol e represents the emission rate and σ_T the capture

rate; the subscripts p and n indicate a hole process and an electron process respectively. (i) represents carrier generation; (ii) electron trapping and re-emission; (iii) hole trapping and re-emission and (iv) recombination.

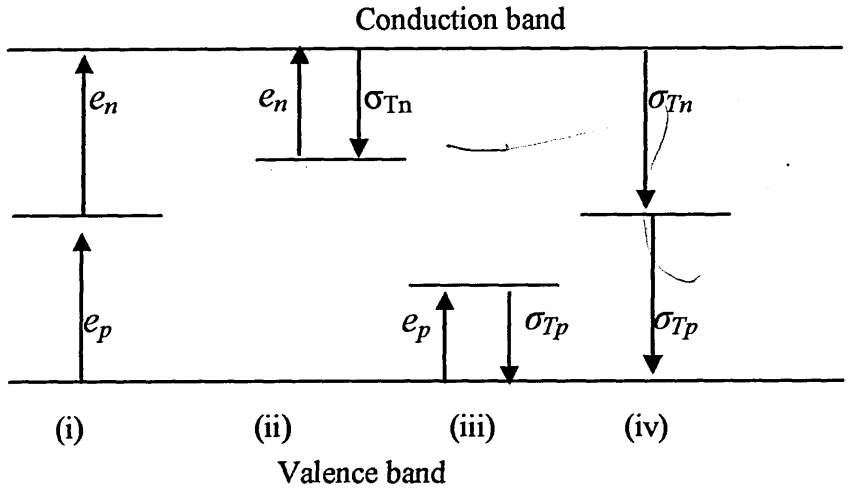


Figure 6-1 The principal charge mechanisms associated with deep states [Peaker and Brozel, 1999].

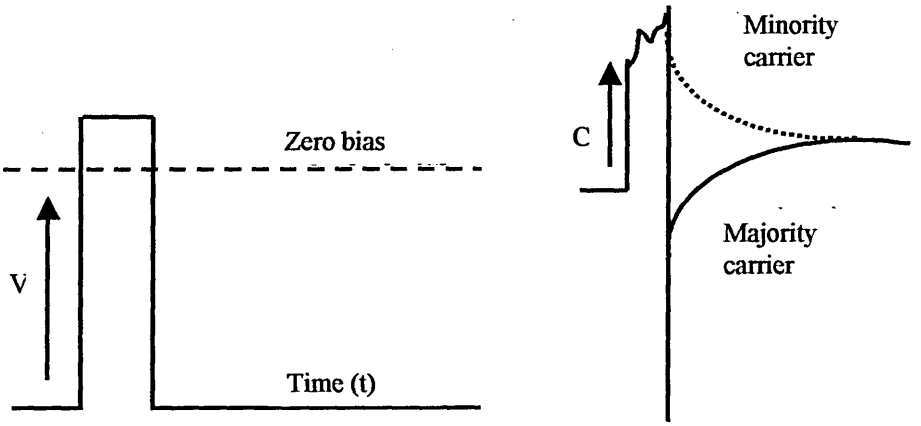
6.4 DLTS measurements

The measurement of deep states can be regarded as having three stages [Peaker and Brozel, 1999];

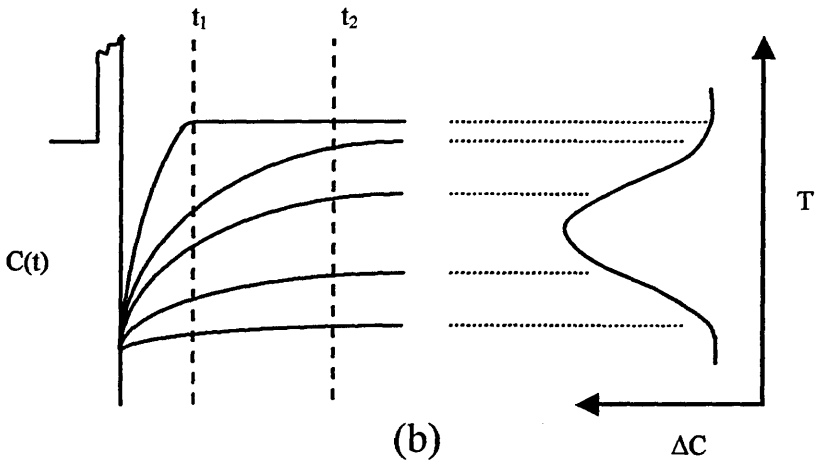
a- the occupancy of the deep electronic state is set,
b- the occupancy is perturbed, and
c- the change in occupancy is measured.

In DLTS the traps are filled with carriers by applying a zero or small forward bias voltage pulse to the device. The capacitance transient is then observed after the device is switched into reverse bias, usually between 2V and 10V. In figure 6-2 (a), a forward bias is applied to the device for a short period of time (typically 1ms). This collapses the depletion region, thus allowing the majority carriers to fill the traps. When the voltage is switched into reverse bias, the measured capacitance is lower because the majority carriers captured in the trap reduce the depletion region. If the temperature is high enough these majority carriers are emitted to the carrier band, and the depletion region increases, which is detected as an increase in capacitance, and appears as a DLTS peak. Minority carriers could theoretically be injected if a fill pulse is applied, but their

concentration will always be less than that of the majority carriers. However, a minority carrier transient may be observed if the minority carrier capture cross section is similar to or larger than the majority carrier cross section.



(a)



(b)

Figure 6-2 (a) The capacitance transient resulting from applying a voltage pulse to diode containing deep states. (b) The use of test pulses at t_1 and t_2 to extract ΔC.

For a single emission rate, the change of capacitance is exponential, as shown in figure 6-2 (b), and is sampled at times t_1 and t_2, after the application of the reverse bias. If the exponential rise is very slow, no difference exists between the signal measured at t_1 and t_2, and so the system output $(\Delta C_{(t)} = C_{t_1} - C_{t_2})$ is effectively zero. If the exponential rise is very fast so that $C_{(t)}$ effectively reaches a plateau before t_1, then again no difference is discernible. At intermediate values there will be a time constant for which $(\Delta C_{(t)} = C_{t_1} - C_{t_2})$ is a maximum. The scanning of the temperature causes a

change in the signal due to the thermal dependence of the electron emission rate. The capacitance is sampled at two different times $t_2 > t_1$ during the emission process the DLTS signal ΔC is defined as the capacitance difference between t_2-t_1. The electron emission rate e_n [lang, 1974];

$$\Delta C = C(t_2) - C(t_1) = \Delta C_o(\exp(-e_n t_1) - \exp(-e_n t_2)) \qquad 6.5$$

Figure 6-2b at temperature T_1 ΔC equals maximum. By differentiating equation 5.5 with respect to τ_n and setting the result equal zero, we obtain $\tau_{n,max}$ at ΔC_{max} as [lang, 1974, Davidson and Evans-Freeman 1997];

$$\tau_{n,max} = e_{n,max}^{-1} = \tau = \frac{(t_1 - t_2)}{\ln\left(t_1/t_2\right)} \qquad 6.6$$

The value of $e_{n,max}$, defined by the setting of t_1 and t_2, is denoted the rate window of the measurement (typically, $e_{n,max} \sim$ 1-1000 S^{-1}).

Traps with different characteristics will produce peaks at different temperatures and hence if there are a number of traps in the sample, they may be recognised by their temperature 'fingerprints'.

For Schottky diodes, DLTS can only measure majority carrier traps (centres which trap electrons in n-type or holes in p-type material). Using p-n junctions minority carrier traps can also be seen but it is difficult to quantify the results. A valuable alternative is minority carrier transient spectroscopy (MCTS). This was developed at UMIST (Manchester) and employs a laser pulse of around band-gap energy to create minority carriers which may then fill the minority carrier traps [Davidson and Evans-Freeman 1997].

A series of transients with a constant repetition rate (forming a signal) is obtained by applying a repetitive bias pulse to the sample. By changing the temperature (T) of the sample, the time constant of the transients will vary exponentially with ($1/T$) as illustrated in figure 6-3. The capacitance-time (C-t) transient, according to Miller *et al*, [1977] and Lang and Kimerling [1979] follows an exponential time dependence;

$$C = C_0[1 - \frac{n_T(0)}{2N_D}\exp(-\frac{t}{\tau_e})] \qquad 6.7$$

where C_o is the capacitance without any deep levels, N_D is the donor doping concentration (cm^{-3}), and τ_e is the electron emission time constant given by:

$$\tau_e = \frac{\exp[(E_C - E_T)/kT]}{\gamma_n \sigma_n T^2} \qquad 6.8$$

where $\gamma_n = (V_{th}/T^{1/2})(N_C/T^{3/2})$, V_{th} is electron thermal velocity and N_C is the effective density of states in the conduction band. The γ_n value for n-type silicon is 1.07 x10^{12} (cm^{-2} s^{-1} K^{-2}) [Martin *et al*, 1977].

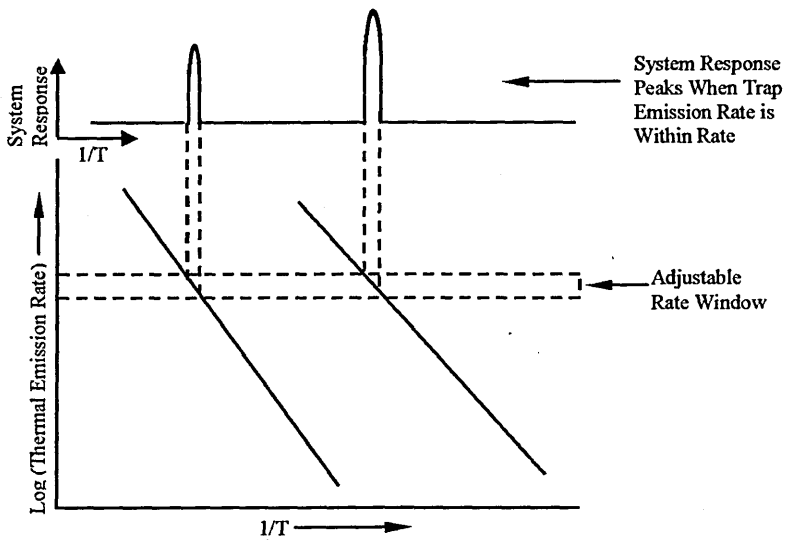


Figure 6-3 Shows the rate widow concept, which is the basis of the DLTS method [Miller *et al*, 1977; Lang and Kimerling, 1979].

6.5 Determination of trap parameters

6.5.1 Trap activation energy, E_A

DLTS peaks can only be observed at temperatures where the trap emission rate is within an emission rate window. As it will be seen later, the emission rate of a trap varies with varying sample temperature, so the instrument will show a response peak at the temperature where emission rates are within the window. The emission rate is given by;

$$e = \frac{N_C \sigma V_{th}}{g} \exp\left(-\Delta E / kT\right) \qquad 6.9$$

where N_C is the effective density of states, σ is the capture cross section, V_{th} is the thermal velocity of the carrier and g is the degeneracy of level. If σ is independent of temperature, then the thermal activation energy E_A of the deep defects can be obtained from the slope of the plot of $\ln(e/T^2)$ against $1/T$, (since $N_C V_{th}$ is assumed to vary with T^2) [Kan 2001].

6.5.2 Trap concentration, N_T

The trap concentration is given by;

$$N_T = \frac{2\Delta C}{C}(N_D) \qquad 6.10$$

where ΔC is the capacitance change due to a saturating injection pulse (i.e., data from a DLTS measurement), C is the capacitance of the diode under quiescent reverse biased conditions at the measurement voltage, and N_D is the net donor concentration when the trap is observed. This relationship is accurate only when:

1. The trap and doping density are uniformly distributed, with a field independent emission rate,
2. A single emission process occurs at a deep level, and
3. $N_T << N_D$.

6.5.3 Capture cross section, σ_T

Point defects can be considered to have a circular cross sectional area centred on the trap; this area is chosen such that if any carrier passes through it, it is "captured". In DLTS the majority traps are filled with a pulse to zero bias, which enables them to capture carriers from the bulk population. If the pulse is very short, it is possible that the traps will not have time to fill completely. In fact, if electron traps are considered, the extent to which they fill will depend on the trap cross section σ_n, the pulse length, t, and the majority carrier population, n:

$$\frac{\Delta C_\infty - \Delta C_t}{\Delta C_\infty} = \exp\left(-\sigma_n V_{th} n\right) t \qquad 6.11$$

where the thermal velocity $V_{th} = \left(3kT/m^*\right)^{1/2} \approx 10^7$ cm.s^{-1} at room temperature, m^* is the effective mass, ΔC_∞ is the capacitance transient when the particular trap is completely filled (at longest fill pulse) and ΔC_t is the capacitance transient at time t. As the fill pulse length is reduced, a point is reached where the trap fails to fill completely and the DLTS peak height is reduced. The usual procedure is to set the temperature so that the DLTS output is at a peak and then change the fill pulse width in known steps. If ln $[(\Delta C_\infty - \Delta C_t)/ \Delta C_\infty]$ is plotted as a function of t, the slope is equal to τ, where $\tau = (\sigma_n V_{th} n)^{-1}$ and the value of σ_n can be determined. In this method the capture is from the bulk, i.e., in a field free region, whereas the emission is observed in the space charge layer. These calculations do not account for the Debye tail (i.e., the distribution of free carriers near the edge of the space charge region) [Pons, 1984]. This region is never abrupt and the defects present there have different emission characteristics. The Debye tail calculations are tedious and an experimental technique to eliminate the need for them has been developed. Double DLTS subtracts the DLTS signals obtained from consecutive transients with slightly different filling pulses, essentially subtracting the Debye tail effects [Lefevre and Schulz, 1977]. Unfortunately, it is often not possible to make the pulse length as short as required, but if the value of carrier concentration (n) is reduced, a smaller σ_n can be measured (equation 6.11).

The influence of the Debye region in capacitance measurements is of major importance. The Debye region occurs at the depletion edge, where the free carrier density of carriers diffuses in the depletion region. Hence the depletion region edge tends not to be a well-defined boundary, and the carriers spill over in a tail (i.e. the distribution of free carriers near the edge of the space charge region is non-uniform).

Capture cross sections in the range of $10^{-24} \sim 10^{-13}$ cm^2 are typically observed for defects in silicon. Extremely small σ_n are measured at repulsive deep level centres, in the range of 10^{-24} to 10^{-21} cm^2 [Kan 2001]. Neutral deep levels have σ_n in the range of 10^{-17} to 10^{-15} cm^2. It is assumed that an attractive potential can be provided by the polarisation of the centre. It is not as strong as a charged defect state potential, and decreases rapidly with increasing distance away from the defect. Attractive centres have

cross sections that may be 10^{-14} cm^2, or larger. It is thought that these indicate the presence of a doubly charged defect state, which will act as a trapping centre rather than a recombination centre.

6.6 Emission and capture from deep levels

Deep levels typically reside at energy levels of more than E_C - 0.1eV from the band edge. The capture and thermal emission rates for majority carriers (i.e. electrons for n-type semiconductor) are c_n and e_n respectively. The capture and thermal rates for minority carriers (holes) are c_p and e_p respectively. The electron emission process depends on the concentration of deep traps occupied by electrons and the rate of emission, while the capture process depends on electron concentration in the conduction band, the concentration of deep traps occupied by holes, and the capture rate which includes the thermal velocity. Figure 6-4 shows four trapping processes of which the deep level is assumed to be capable of:

c_n, electron capture from the conduction band edge E_C to neutralise an unoccupied centre.

e_n, electron emission from an occupied state centre to E_C.

c_p, hole capture from E_V by an occupied centre.

e_p, hole emission from an unoccupied centre to E_V.

Whether the deep level acts as a trap or generation-recombination centre depends on the temperature, the majority and minority capture cross sections of the deep level and the position of the Fermi level in the band gap.

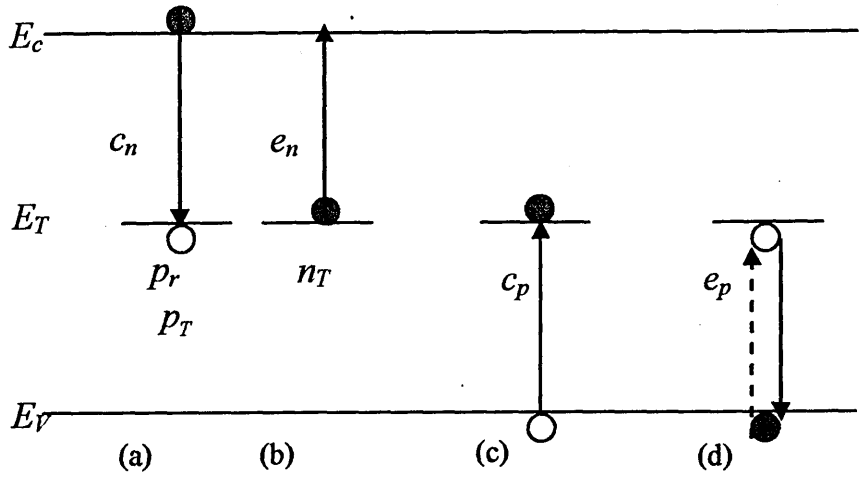


Figure 6-4 Various carrier transitions between deep level and band edge [Schroder, 1990]

The deep levels located near the mid-gap behave as generation-recombination centres, but in the upper half of the band gap the electron emission rate is much higher than the hole emission rate. In the lower half of the band gap the electron emission rate is lower than the hole emission rate. Otherwise the deep levels near the edge tend to act as traps. When the deep levels are occupied by holes (p), they are in the p_T state, and when they are occupied by electrons, they are in the n_T state.

It follows that $N_T = n_T + p_T$, where N_T is the total concentration of deep levels. [Schroder, 1990]. In an n-type semiconductor, n_T is given by

$$n_T(t) = n_T(0)e^{-t/\tau} + \frac{e_p + c_n n}{e_n + c_n n + e_p} N_T(1 - e^{-t/\tau}) \qquad 6.12$$

where c_n is the electron capture coefficient, e_n electron emission rate, e_p hole emission rate, $n_T(0)$ is the concentration of the deep levels occupied by electrons at zero time, the transient time constant, $\tau = 1/(e_n + c_n + e_p)$, and the steady-state deep level concentration n_T is [Schroder, 1990]

$$n_T = \frac{e_p + c_n n}{e_n + c_n n + e_p} N_T \qquad 6.13$$

When a reverse bias is applied, n_T the $C_n n = 0$, becomes

$$n_T = \frac{e_p}{e_n + e_p} N_T \qquad 6.14$$

6.7 Transient capacitance

The capacitance of a Schottky diode is a measurement of the static charge in the space charge region. The presence of deep traps in the depletion region of a Schottky diode causes a change in the junction capacitance because any variation in the charge state of the deep traps due to a change in the concentration of carriers trapped by them causes a change in the capacitance. These traps, which capture or emit carriers, can be monitored by observing the corresponding change in the capacitance. The trapping process can be controlled by changing the voltage applied to the junction using the biasing pulse technique. The trapped carriers may be majority carriers depending on the applied pulse type where there are two types of biasing pulses [Lang, 1974], the majority carrier pulse and the injection pulse. The majority carrier pulse, in which voltage bias is pulsed from reverse voltage to zero voltage, momentarily reduces the diode bias and introduces only majority carriers into the region of observation. The injection pulse is applied either by forward biasing the device for a very short interval or by an optical pulse which injects both minority carrier and majority carriers into the depletion region where the voltage bias can be pulsed from a reverse voltage to a forward voltage. The latter technique is not used often as the results are difficult to understand.

6.8 Majority carrier emission

At a Schottky junction, which is initially reverse biased, as shown in figure 6-5 (a), all the traps below the Fermi level, E_F, are occupied by electrons, and the traps above E_F are empty. In this case, the junction has a certain capacitance $C_1(V=V_R)$. When the voltage is increased momentarily to zero, the width of the depletion region decreases rapidly, as shown in figure 6-5 (b), and hence the capacitance increases $C_2(V= 0)$. At the same time the deep traps may capture electrons to fill the empty traps that have fallen below E_F. When again subjected to reverse bias, the width of the depletion region increases figure 6-5 (c). As a result, the capacitance decreases to a value C_3 $(V=V_3)$ which is less than its original value, due to the trapped electrons in the deep traps within the depletion region. At a certain temperature where the necessary

thermal excitation energy is available, these trapped electrons will be emitted by thermal emission, figure 6-5 (d,e). As result, the electron-occupied trap concentration within the depletion region decreases as a function of time according to:

$$n_T = N_T \exp\left(-t/t_e\right) \qquad 6.15$$

This will produce an exponentially increasing capacitance transient, shown as C_4 in figure 6-5 (f), which reaches the original value C_1.

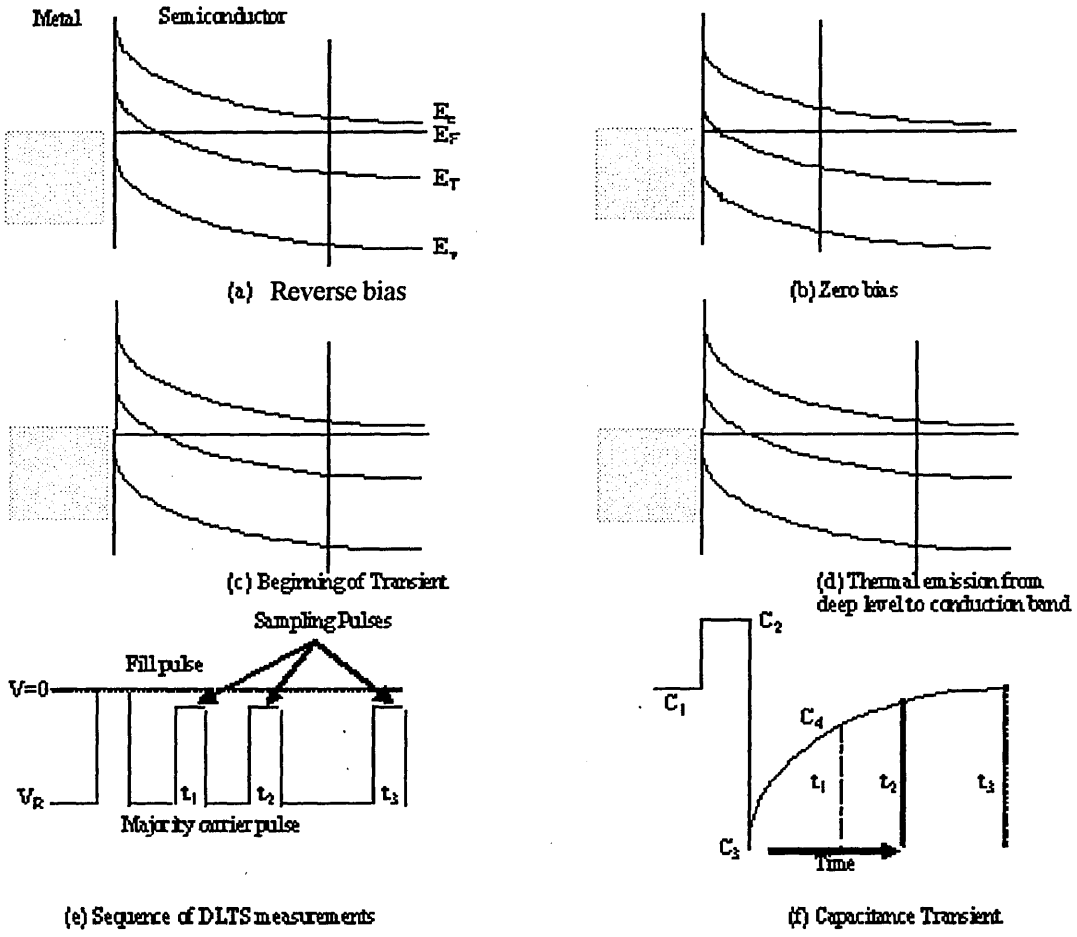


Figure 6-5 Variation of capacitance with the filling and thermal emission of a majority carrier trap.

6.9 Principles of DLTS

Capacitance transients have long been used for the study of deep traps in semiconductors [Williams, 1966]. Information about the presence of impurity levels in

the depletion region of a Schottky barrier can be obtained by observing the capacitance transient that results from a return to thermal equilibrium of trap occupancy after an initial non-equilibrium condition. The sequence of events that occur in a majority carrier trap during an observation of the emission transient in the depletion region can be explained with the aid of figure 6-6, which illustrates the band diagram of a Schottky contact on an n-type semiconductor before, during and after a bias pulse that acts as the non-equilibrium condition.

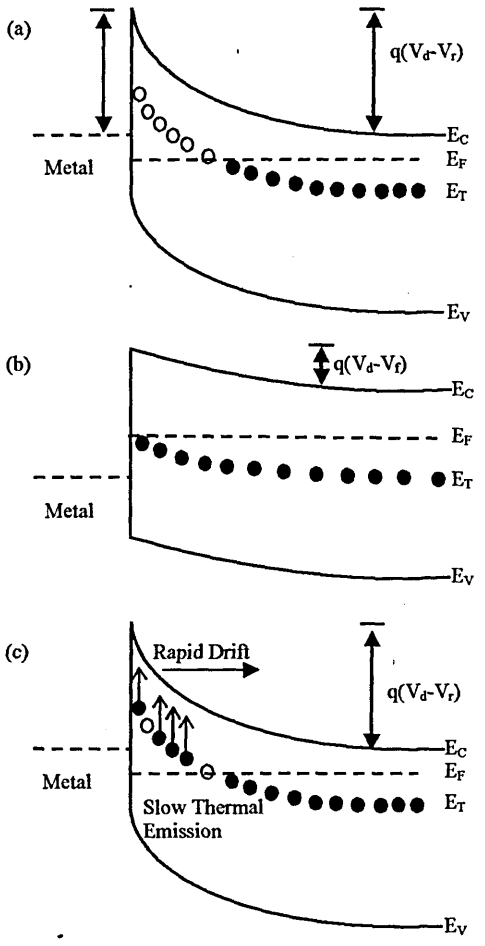


Figure 6-6 The band diagram of the Schottky barrier. (a) At quiescent reverse bias with all deep levels empty. (b) Filling pulse, all deep levels full (c) The deep levels emit the trapped electrons with a characteristic emission rate [Williams, 1966]

In figure 6-6 (a) the traps are within the depletion region, and in the equilibrium state of the system the diode is reverse biased. The position of the Fermi level determines whether or not the traps are occupied. In figure 6-6 (b), when the majority carrier fill pulse is applied, the traps in the neutral region are filled due to the capture rates exceeding the emission rates and because the Fermi level has risen. After the bias

is returned to the quiescent reverse value, figure 6-6 (c), the capture process is turned off and the traps empty of carriers by thermal emission, with a characteristic emission rate, which is given by the principle of detailed balance [Williams, 1966].

Any change in the concentration of carriers trapped in deep levels as a result of carrier emission causes a change in the capacitance of the diode [Sah *et al*, 1970; Yau, and Sah 1971; Lang, 1974]. After the fill pulse the deep levels are again within the space charge layer where the capture rate is zero. As a result of the captured carriers, the capacitance of the diode will have changed, and as these carriers are thermally emitted a capacitance transient will be produced as shown in figure 6-7 [Lang, 1974].

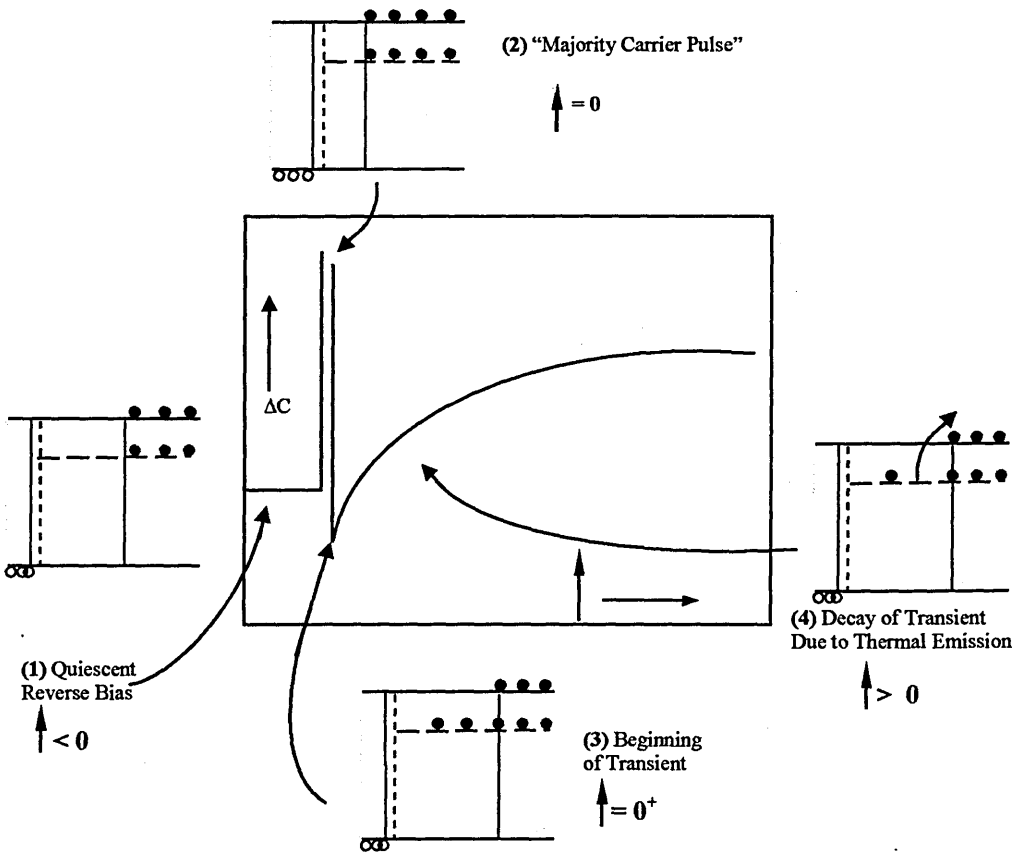


Figure 6-7 Isothermal capacitances transient for thermal emission from a majority carrier trap [Lang, 1974].

The field rapidly sweeps the emitted carriers out of the depletion region and this causes an increase in the positive space charge density. The resulting rise in capacitance, caused by a decrease in depletion region width, can then be analysed to provide quantitative information about the particular trap. The capacitance transient response is given by

$$\Delta C(t) = C_q \frac{N_T}{2N_d} \exp(-e_n t) \qquad 6.16$$

This shows how the transient's time constant gives the emission rate of the trap, and information about the trap concentration is provided by the amplitude of the transient $\Delta C(0)/C_q$. The type of trap under observation is known from the fact that the transient response of a majority trap is opposite to that of a minority carrier trap. A minority carrier pulse (or injection pulse) may be generated by using an optical pulse, which requires Schottky diodes with a very thin metallic contact (i.e., semitransparent).

6.10 Laplace DLTS

A considerable amount of work has been carried out to overcome the limitations of DLTS, using peak de-convolution methods with fixed filters to produce an output proportional to the amount of signal seen within a particular time constant range. So far these methods have not been particularly successful in improving the resolution of the original DLTS technique.

LDLTS is an isothermal technique developed at UMIST (Manchester), which is carried out at a particular temperature, usually the temperature that produces the maximum in the DLTS peaks. The system uses a high stability cryostat, accurate to better than 0.5K. The sample is allowed to come to thermal equilibrium at the chosen temperature and then the transient is sampled.

Several thousand capacitance transients are taken and then digitally averaged. This is expected to give a signal to noise ratio (S/N) better than 1000. This S/N ratio is necessary to separate transients with closely spaced emission rates. In general, this means that the concentration of the defect must be above 1% of the shallow doping level but below 10%. LDLTS applies three mathematical procedures, based on Tikhonov regularisation routines, to obtain the emission rate from the capacitance transients. A true exponential transient will give only one peak in the LDLTS spectrum from these three calculations (i.e., the three calculations coincide). The area under each sharp peak is proportional to the trap concentration.

LDLTS is fairly a new technique, which has not yet been applied intensively, but already there is evidence showing that many problems related to defects in high purity silicon and its alloys can be usefully investigated using this technique. LDLTS can be used to observe the influence of small disturbances on the process of carrier thermal emission and it becomes possible to distinguish defects with slightly different emission characteristics, which provides a new insight into defect microscopy.

Dobaczewki *et al*, [1994] applied this technique to very complicated centres, such as the DX centre related to group IV (silicon) and group VI (Te) atoms in AlGaAs (DX is explained by Dobaczewki). They observed in each case that standard DLTS gave featureless peaks, while the LDLTS spectra revealed the existence of a fine structure in the thermal emission process. i.e., each of the defects has its characteristic signature. Deixler *et al*, [1998] studied the Au-H complex in silicon by LDLTS. They separated the signals from the Au-acceptor and the G4 (Si: Au-H) centres by measuring the emission rate, activation energy and electron σ_n. Alloy splitting in Si-Ge has also been investigated by Dobaczewki *et al*, [1999] using LDLTS. In semiconductor alloys, the spatial fluctuations in local alloy composition may cause variations in the thermal emission rates of carriers from the defect, and the thermal emission is sensitive to the lattice relaxation that may accompany the electronic transition. Provided that the alloy is macroscopically homogeneous, the fine structure observed in the defect spectra is a manifestation of spatial fluctuations in the alloy composition on the microscopic scale. By applying LDLTS, Dobaczewki *et al*, [1999] were able to show that the outer two shells of germanium atoms surrounding the impurity perturb the electronic properties of the Au and Pt acceptor defects.

To find a quantitative description it is common to assume that the non-exponentionality exhibited by some capacitance transients can be characterised by a spectrum of emission rates and that a mathematical representation of the transients is given by the Laplace transform of the spectral density function

$$f(t) = \int_{o}^{\infty} F(s)e^{-st}ds \qquad 6.17$$

where $f(t)$ is the recorded transient. Performing the inverse Laplace transform of the signal $f(t)$ will then give the spectrum of emission rates present in the transient. This results in a spectrum of δ-like peaks representing single and multiple exponential

transients, and a broad DLTS spectrum if there is no general continuous distribution. The problem now arises that there is no general solution for all possible functions *f(t)* in equation 6.16, and when this signal is superimposed with system noise the number of possible solution becomes infinite. Therefore the LDLTS technique uses a number of advanced regularisation algorithms in order to find the best estimate for *f(s)*. It is then a matter of using previous knowledge of the system to examine only those solutions that reveal the least new information not already known or expected.

The present system used to obtain Laplace DLTS is Version 2.04 which allows 1-30000 scans to be performed each comprising 10-30000 samples taken at rates between 10 Hz and 100 kHz. Once the transient has been captured primary analysis of the transient can be carried out by using either simple one-exponential fitting or multiple-exponential fitting using a statistical approach.

A database is used to store and compare the results at different temperatures from which information about the particular trap under observation can be deduced. One extreme examples of the structure observed in the emission process has been reproduced in figure 6-8 which shows a comparison between DLTS and LDLTS signals and the increase in resolution which can be achieved by use of the latter technique.

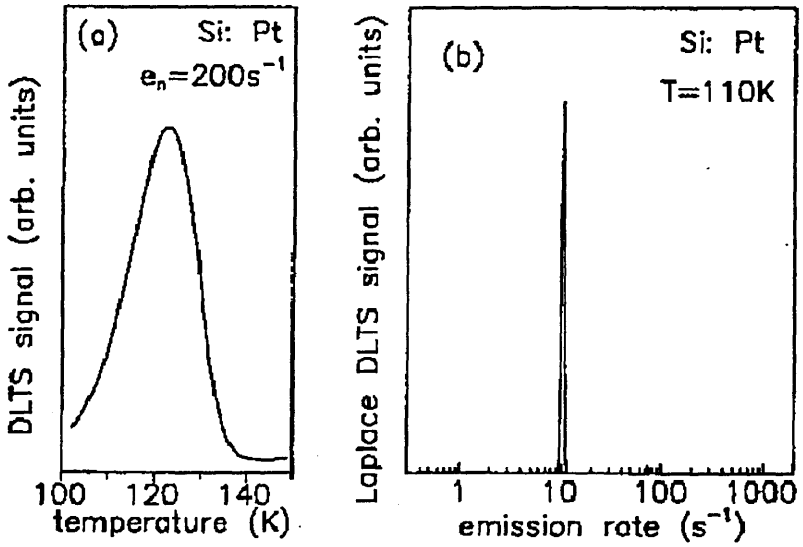


Figure 6-8 Comparison between conventional and LDLTS spectra. These show a platinum related defect in silicon [Dobaczewski *et al*, 1995].

6.11 Scanning electron microscopy

This section gives a brief description of some of the advantages and disadvantages of SEM compared to optical microscopy. Table 6-1 shows some differences between optical microscopy and SEM

Optical microscopy	Scanning electron microscopy
polychromatic white light	monochromatic electrons
Maximum magnification 1000 x	sub-nanometre resolution possible.
small depth of field	large depth of field
air	vacuum (in general)
wavelength information (colour)	SE image not specific
non-conducting	need best semiconducting surface

Table 6-1 Differences between optical microscopy and scanning electron microscopy.

Many other signals are generated by the interaction of the electron beam with the specimen (see figure 6-9). These can be used to give additional information such as an energy dispersive X ray analysis, the crystal structure and orientation, electron backscattered diffraction spectrum, any information on electrically and optically active defects in semiconductors, electron beam induced current and cathodoluminesence.

In this section the fundamentals of scanning electron microscopy and the information that can be gained from this technique are introduced. Conventional microscopes use a series of glass lenses to bend light waves and create a magnified image, with a maximum useful magnification of about 1000x. Modern field emission gun SEMs are capable of image resolution on atomic scale. The energetic electrons strike the sample and various reactions can occur as shown in figure 6-9. The electron beam interacts with the atoms, molecules and other components of the specimen to produce backscattered electrons, secondary electrons, X-rays, and photons.

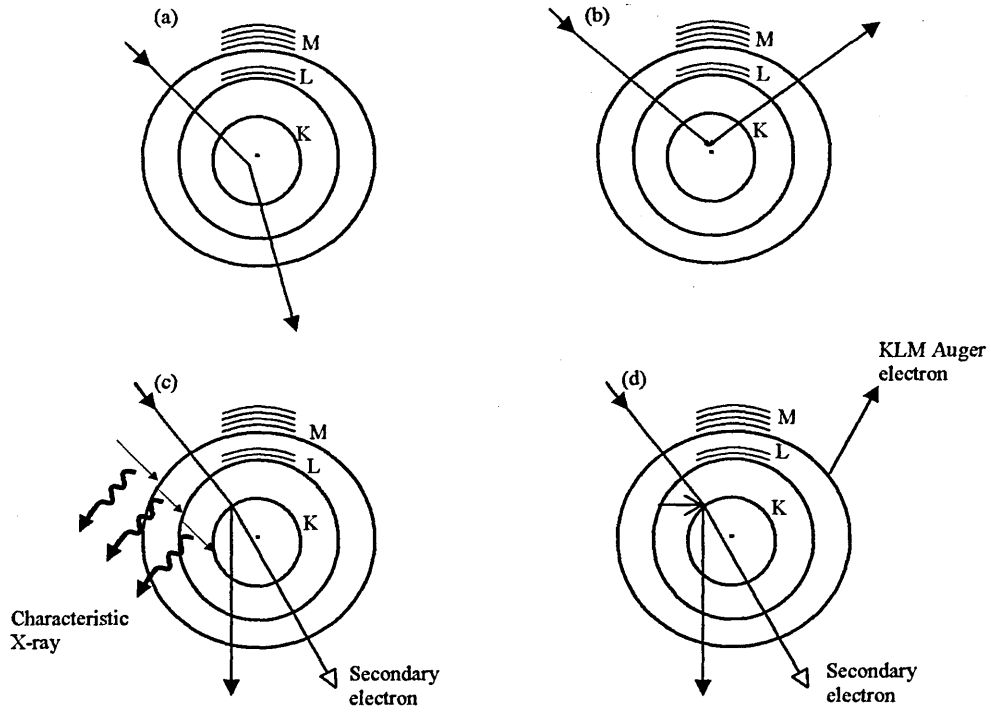


Figure 6-9 Atom-high energy electron interactions. The inner electron shells of atoms are labelled according to standard notation (the innermost states K, L etc). The incident particle is arrowed. a- Low-angle scattering – electrons scattered in this way pass to the next layer of the atoms with very little loss of energy; b- Back (or high angle) scattering; c- Emission of a secondary electron and characteristic X-ray; d- Emission of a secondary electron and an Auger electron [Vernon-Parry, 2000].

SEM can provide information on surface topography, crystalline structure, chemical composition and electrical behaviour of the top 1 μm or so of a specimen. A variety of imaging techniques exist with resolutions in the range 1μm to 0.5 nm, depending on the microscope and the signal used to form the image. Information about electrically active defects can be obtained using techniques such as electron beam induced current, and cathodoluminescence, and this data can be correlated with the micro-structure obtained in secondary electron images. For semiconductors, no special specimen preparation is required. The surface to be examined is mounted on a special SEM stub with electrically conducting pads. If the specimen is mounted on an insulator then to prevent the specimen from charging (which distorts the image) a conduction path to ground is required, this is usually a fine line of Ag paste from the sample to the stubs.

6.12 Summary

One of the main goals of this chapter was to illustrate the different characterisation methods which were used to study fabricated diodes. I-V and C-V measurements provide the electrical characteristics of the diodes and also used to study its behaviour.

Using information obtained from those measurements, DLTS and LDLTS measurements can be carried out. The principle and advantages of the DLTS technique were introduced, and DLTS measurements were discussed.

In the fifth section of this chapter the determination of traps and their parameters was briefly discussed. Due to the limitations of DLTS, UMIST (Manchester) developed the high resolution Laplace DLTS technique. The idea and principle of LDLTS measurements were introduced indicating the various advantages of this technique. In the last section we have discussed Scanning Electron Microscopy which can provide information on the surface topography and crystalline structure of the sample.

In the following chapter, diamond Schottky diodes will be discussed and the experimental techniques introduced in this chapter will be used to characterise the fabricated diamond Schottky diodes.

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Chapter 7

Schottky diode fabrication

7.1 Introduction to diamond for devices

Diamond has been successfully doped with boron, to become a semiconductor with a wide band gap of 5.54 eV. This, combined with its unique physical and chemical properties, makes its application desirable in a range of high power devices operating to high temperatures, and in harsh environments. A prerequisite to making such applications possible is a knowledge of the properties of the defect states in diamond. Cathodoluminescence, photoluminescence and photoconductivity measurements have been widely used to determine and characterise the relevant properties of diamond [Gildenblat *et al*, 1991; May and Trans, 2000]. Since the realization of n-type doping by phosphorus [Koizumi *et al*, 1997] and the improvement of the structural properties of CVD diamond, increased attention has been focused on the production of diamond-based electronic devices [Zeisel *et al*, 1998].

A large number of researchers including Collins *et al*, [1970], Moazed *et al*, [1988], Moazed *et al*, [1990], Fang *et al*, [1989] and Prins [1989] have used various methods for fabricating and studying Ohmic and Schottky contacts on semiconducting diamond. It is important to carefully prepare the diamond surface since the surface condition critically influences the properties of the device. Prior to metallization, an early procedure was to rub the surface of type-IIa single crystals with olive oil to produce a hydrogen terminated surface. The surfaces were subsequently rinsed with acetone and methanol prior to introduction into a vacuum system.

Tachibana *et al*, [1993] have examined the effect of interface chemistry by comparing the chemical reactivity of gold, aluminium and titanium on diamond; gold

being a non-reactive metal, aluminium a weak carbide-forming metal, and titanium a strong carbide former. They found that when titanium was used as a backing material it reacted with the diamond on annealing at 703K to form titanium carbide at the interface. Tachibana and Co-Workers [1992,1993] have confirmed that aluminium does not form a carbide layer on an undamaged diamond surface. Au contacts on polycrystalline diamond did not show any evidence of chemical reaction at the interface [Tachibana *et al*, 1993].

Consequently a choice has been made to use pure titanium to form the Schottky barrier. Titanium is widely used in metallisation systems due to its excellent adhesion to silicon and silicon oxide. It is one of the few metals which have been shown to have a higher Schottky barrier with p-type silicon than with n-type silicon. The barrier height on p-silicon is reported to be in the 0.6 eV range [Butler *et al*, 2002].

Butler *et al*, [2002] have shown diamond Schottky diodes to have the highest voltage breakdown of all Schottky diodes, but with large forward resistances, typically 300 Ω. This large resistance is the result of a combination of poor Ohmic contacts, non-optimum device geometry and hydrogen electrically compensating the boron. Under optimum conditions the theoretical forward resistance [Geis and Twichell, 1997] is between 0.01 and 0.1 Ωcm^{-2} for diodes with a breakdown voltage of 10 kV. Similar diodes formed in silicon would have a resistance of 30 Ωcm^{-2} [Sze, 1981].

The breakdown voltage of a diode depends upon the fundamental properties of the semiconductor and the minimum controllable doping density, which is limited by growth technology. The breakdown voltage of diamond, SiC [Dmitriev *et al*, 1983, Harris, 1995] and silicon [Sze, 1981] is a function of doping density. The breakdown voltage for diamond was obtained from equation 7.1 below, which empirically predicts the breakdown voltage of semiconductors [Sze, 1981].

$$V_{max} = k_d / N^{3/4} \qquad 7.1$$

where V_{max} is the maximum breakdown voltage of the diode, N is the doping density in cm^{-3} and k_d is an experimentally determined constant. Landstrass *et al*, [1983] showed that at higher doping levels, $k_d = 1.9 \times 10^{16}$ $Vcm^{-9/4}$, the breakdown voltage

determined by Butler *et al*, [2002] for diamond Schottky diodes is higher than that for silicon carbide and silicon, at the same doping level.

Rodrigues *et al*, [1999] prepared two Schottky barrier devices by depositing the rectifying aluminium contact either on the smooth or rough surface of the semiconducting diamond. Gold was used for the other electrode. Rodrigues *et al*, [1999] have clearly shown that the diode with the depletion layer established on the smooth surface has a lower capacitance, as would be expected for a larger depletion layer width. The rough, doped surface must be used as a highly conductive region, i. e, for the Ohmic contact, and the smooth surface must be used to establish a rectifying contact with metals [Rodrigues *et al*, 1999].

It is important to prepare the diamond surface carefully. Bell and Leivo [1958] suggested, based on point contact work, that rectification on the diamond surface was dominated by surface-state pinning. Alternatively, Mori *et al*, [1991] have observed that the I-V characteristics of point contacts to diamond depend on the electro-negativity of the metals. Tachibana *et al*, [1992] have reported that diamond cleaning procedures significantly affect the electrical characteristics. A similar effect of surface pre-treatment was observed by Gort *et al*, [1990].

Diamond is an insulator in its undoped state and yet it exhibits a pronounced p-type surface conductivity provided the surface is terminated by hydrogen [Landstrass and Ravi, 1989]. The surface conductivity reaches values as high as 10^{-5} S cm^{-1}, independent of whether the diamond is in the form of single crystals or polycrystalline films prepared by chemical vapour deposition. This surface conductivity is unique among all semiconductors and insulators and it has already been utilized for a variety of device applications such as Schottky diodes [Hokazono, 1997], field effect transistors [Hokazono, 1997; Kohn, 2001], and sensors [Muller, 2002]. The phenomenon is based on a near-surface hole layer that has a concentration of the order of 10^{12}-10^{13} cm^{-2} which shows little temperature dependence and thus requires acceptors that are very shallow, or even degenerate with the valence band [Hayashi *et al*, 1996; Yamanaka, 1996; Takeuchi *et al*, 2003].

7.2 Diamond Schottky diode

Schottky diodes on p-type diamond show a barrier height (φ_B) >1.5 eV and a low ideality factor (n = 1.1), thus making them attractive for high temperature applications. However, at low (e.g. room) temperature, injection mechanisms other than thermionic emission become apparent and contribute to the current transport. The ideality factor increases with decreasing temperature and current paths other than thermionic emission become apparent. This may point towards small area defects contributing to the excess current flow, leading to a reduction in effective I-V barrier height [Vescan *et al*, 1995].

Therefore, although the forward I-V characteristics are widely in agreement with thermionic emission, the reverse characteristics are less clear. Theoretically, the high barrier should result in immeasurably low reverse current levels and high breakdown voltages, and in natural diamond, such a behaviour is observed [Geis *et al*, 1993; Humphreys *et al*, 1991]. However, technically relevant diodes on epitaxial layers show high reverse currents, which are thermally activated and do not saturate at high reverse bias [Ebert *et al*, 1994; Shiomi *et al*, 1990; Vescan *et al*, 1995]. The I-V Schottky barrier height, as determined from the high temperature region of the characteristics (where the ideality factor is low), is φ_B I-V $\approx$ 1.5 eV. From reverse bias C-V measurements, a barrier height of φ_B (C-V) $\approx$ 1.7 eV is extrapolated, which is nearly independent of temperature.

Diamond can be doped with boron to make it p-type, with an acceptor energy of 0.37 eV [Smith and Taylor, 1962]. Diamond, having a larger band gap (5.54 eV) than SiC (3.4 eV), GaN (3.2 eV), and Si (1.1 eV) [Sze, 1981], should enable the fabrication of diodes with larger breakdown voltages than those exhibited by diodes formed using other semiconductor materials. Because of the inability to control the level of impurities, diamond diodes and transistors have not yet exhibited breakdown voltages in excess of 500V, while diodes formed in other semiconductors exhibit significantly higher breakdown voltage [Geis *et al*, 1987; Gluche *et al*, 1997; Vescan *et al*, 1998; Yamanaka *et al*, 2000; Butler *et al*, 2002]. However, the development of diamond electronics has also been hampered by other problems such as lack of shallow donors and low quality, inconsistent synthetic material. Nevertheless, interesting devices have been made; for example, Koizumi and co-workers have recently realized an ultraviolet light-emitting p-n diode using diamond [Koizumi *et al*, 2001].

Generally, for use in commercial electronic devices, high-quality semiconductors with atomically flat surface, low defect density, and low residual impurity levels are required. Among the wide-gap semiconductors, diamond is the best material in terms of superior physical and electrical properties. In particular, a problem of high density of structural defects, which occurs in compound semiconductors, can be automatically removed in diamond, because it is a one-element tetrahedral semiconductor. However, to date, diamond has proved one of the most difficult materials to synthesise as a semiconductor. Many studies in terms of semiconductor and device processes have been reported with natural, HPHT synthesised and polycrystalline CVD diamonds [Pan and Kania, 1995; Walker, 1979]. Okushi [2001] points out, however, that there are few papers reporting cases where such diamonds have been found to be of sufficiently high quality to be applied in electronic devices, and that this strongly suggests that single-crystalline CVD diamond films prepared by homo- and/or hetero-epitaxial growth are required to realise high-quality diamond.

There are many possible factors that can play an important role in determining the Schottky barrier height at a metal-semiconductor interface. Such factors include the work function and/or electronegativity of the metals, densities of surface (interface) states, and interface chemistry such as the heat of condensation of the metal and the heat of the reaction between the metal and semiconductor constituents [Tachibana *et al*, 1992; Tachibana and Glass, 1992]. Ihm *et al*, [1978], Pepper [1982], Pate [1986] and Derry *et al*, [1986] amongst others point out that it is both interesting and useful to study the Schottky barrier height of metal contacts on diamond because diamond is both fully covalent and a wide-band-gap semiconductor.

Diodes for technical applications need to show high blocking voltages and a low forward loss, i.e. a low series resistance [Okano *et al*, 1990; Okano *et al*, 1991]. Therefore, undoped diamond p-n diodes are not technologically relevant for such applications. However, lightly boron-doped ($N_A \leq 10^{17}$ cm^{-3}) Schottky diamond diodes (with Al being the Schottky metal) on oxygen-terminated diamond surfaces show good performance at high temperatures, i.e. acceptable forward currents and high breakdown voltages at reverse bias [Aleksov *et al*, 2003].

7.3 Ohmic contacts

A metal-semiconductor contact is defined as Ohmic where the contact has a negligible resistance relative to the bulk or spreading resistance of the semiconductor. A satisfactory Ohmic contact should not significantly perturb device performance, and while an Ohmic contact will tend to have linear or quasi-linear I-V characteristics it is more important that the contact must be able to pass the necessary device current. Also the voltage drop across the contact should be very small compared to the voltage drops across the active regions. This implies that Ohmic contacts frequently function as regions of high recombination. It also implies that highly damaged regions should serve as good Ohmic contacts.

An Ohmic contact should not degrade the device to any significant extent, and it should not inject minority carriers. In addition, one should be able to make such contacts in a reproducible manner. Ohmic contacts must be able to withstand the operating conditions, such as high temperatures, for which diamond devices are intended. Ideally, the contacts would be compatible with conventional device processing techniques, and finally, they should strongly adhere to the diamond surfaces [Hewett and Zeidler, 1993].

Ohmic contacts with low specific contact resistivities on diamond have been achieved by a number of researchers [Das *et al*, 1994]. These authors employed a carbide-forming metal such as titanium and molybdenum (Mo), capped by a protective layer of, for example, gold, to obtain acceptable Ohmic contacts on diamond. In the as-deposited state these contacts will act to rectify the current, but when annealed at over 673K will become Ohmic contacts. Some investigations on Au/Ta (tantalum)/p-diamond and Au/Mo/p-diamond contacts have also been reported [Nakanishi *et al*, 1994; Muret *et al*, 1999; Zhen *et al*, 2002].

Titanium tends to react with diamond to form TiC, which can not only lower the barrier height but also produce strong adhesion between the metal and diamond. The gold capping layer can prevent oxidation of the underlying titanium. Following the methods of Wang *et al*, [2002], instead of using a conventional evaporation method, Ti/Au bilayer metals were fabricated on boron-doped diamond films using radio frequency sputtering.

Various methods to fabricate Ohmic and/or Schottky contacts on semiconducting diamond have been studied [Moazed *et al*, 1990; Moazed *et al*, 1988; Prins, 1989; Gort *et al*, 1990; Collins *et al*, 1970; Humphreys *et al*, 1991; Fang *et al*, 1989]. A number of excellent reviews are available [Moazed *et al*, 1990; Okano *et al*, 1991; Gildenblat *et al*, 1991; Geis, 1991; Das *et al*, 1994].

The surface band bending (SBB) after deposition of non-reactive metals (gold and aluminium) increases after annealing at 703K. Tachibana *et al*, [1992] have shown (i) that gold contacts on polycrystalline diamond did not show any evidence of chemical reaction at the interface whereas titanium deposited on an as-grown diamond surface formed a carbide at the interface upon annealing at 703K, (ii) titanium on an Ar^+-sputtered diamond surface reacted to form the carbide at an even lower annealing temperature (413K). (iii) Aluminium, which is thermodynamically a weak carbide former, did not react with an as-grown polycrystalline diamond even after annealing up to 703K, but did form a carbide on the Ar^+-sputtered surface. (iv) That a substantially damaged diamond surface and/or higher annealing temperatures are necessary for aluminium to react with diamond. Thus the observations reported here, of reactive Titanium-diamond interfaces and non-reactive gold- and aluminium-diamond interfaces are consistent with previously reported results for polycrystalline diamond.

Tachibana *et al*, [1993] observed that it is necessary to have a more severely damaged and open diamond structure than just the small geometric strain introduced during the reconstruction for a weak carbide forming metal such as aluminium to react chemically at the interface. A similar result, the decrease of the Schottky barrier height (SBH) of aluminium after annealing, has been observed previously by Himpsel *et al*, [1980]. Tachibana *et al*, [1993] suggested that this might be attributed to the agglomeration of metal clusters by the annealing process, which in turn decreases the effect of the charge transfer from the metal.

7.4 Sample preparation

A variety of p-type diamond semiconductor samples have been investigated in this work. The total number of samples was fourteen, divided as follows;

1- Eight samples were supplied by Diamond Trading Company (now called Element 6, a subsidiary of de Beers), all of them had same dimensions, and there were two different doping levels.

2- Six samples were supplied by the National Research Laboratories in Washington, these samples were of different dimensions but had the same doping level.

All the samples required suitable cleaning procedures prior to fabrication of the Schottky diodes. They were first cleaned by wet cleaning procedures, and then by a dry cleaning procedure to passivate their surfaces. Each of the following processing procedures were used during this research to fabricate Schottky diodes which showed good rectifying qualities and low leakage currents despite the different doping levels of the samples.

The processing procedure can be divided into three steps:

(1) For the Schottky diode the sample surface is first cleaned using different methods as will be described below. (2) The Ohmic contact is formed by depositing metal on the rear of the sample. (3) Metal is deposited on the front side of the cleaned sample to form the Schottky contact.

Researchers have used different methods to achieve a clean surface for Schottky diode fabrication. Due to the importance of the cleaning process, the following section will discuss the cleaning procedures relevant to this research work.

7.4.1 Surface cleaning

The surfaces of homoepitaxial diamond films and the electrical characteristics of metal-homoepitaxial diamond contacts are sensitive to the various surface treatments. Proper cleaning of boron doped homoepitaxial diamond film is necessary for the fabrication of reliable high-temperature Schottky diodes [Gort *et al*, 1990]. For completeness, different methods and procedures used by some researchers to clean the diamond surfaces to enable it to work as a Schottky diode were tested in this research work. We have tried different methods of cleaning, which we will be discussed later.

Mori *et al*, [1992] have reported that as-deposited diamond films prepared by CVD have a highly conductive p-type semiconducting layer near the surface, and that

this can be removed by oxidation using acid solutions or oxygen ambient annealing. Gort *et al*, [1990] also pointed out that the measured sheet resistance of as-deposited diamond films was almost the same regardless of the doping. Hayashi *et al*, [1997] demonstrated that the near surface p-type high-conductivity layer which is usually observed on as-deposited diamond films disappeared after chemical cleaning using a saturated solution of CrO_3 + H_2SO_4, but this exposure of the diamond film to a hydrogen plasma resulted in recovery of the high conductivity layer. In order to remove graphitic surface layers, their diamond samples were heated for 1 hour at 453K in a CrO_3 + H_2SO_4 solution prior to the hydrogen treatment. Once a clean oxidized surface was obtained, the samples were hydrogenated in a microwave plasma for 30 minutes at 1123K. The film surface was prepared for Schottky diode fabrication by immersing the sample in CrO_3+H_2SO_4 at 443K for 3 minutes, and then rinsing in a 1:1 boiling solution of H_2O_2 (30 %) and NH_4OH (70 %). This cleaning is effective in removing the conductive layer and any non diamond carbon existing on the surface of as-deposited homoepitaxial diamond films [Gort *et al*, 1990; Gildenblat *et al*, 1990]. These cleaning procedures are critical to fabrication of high performance diamond Schottky diodes [Landstrass and Ravi, 1989].

Four kinds of surface treatment have been carried out by Mori *et al*, [1991]; treatment A, boiling in a saturated solution of CrO_3 at 473K following by a rinse in a solution of H_2O_2 (30 %) and NH_4OH (70 %) at 363K, treatment B, boiling in a pure H_2SO_4 solution at 473K, treatment C, exposing to an O_2 plasma for a few minutes, and treatment D, exposing to a H_2 plasma for 5 minutes [Geis *et al*, 1987; Gildenblat, 1988; Gort *et al*, 1990; Mori *et al*, 1991].

Treatment A is popular in cleaning diamond surfaces and has been reported extensively in the literature [see, e.g., Gies *et al*, 1987, Gildenblat *et al*, 1988, Gort *et al*, 1990]. The effects of treatment A and treatment D on the electrical properties have been previously reported by Gort *et al*, [1990] and by Mori *et al*, [1991].

Metal	φ_m (eV)	χ_m (eV)	As-grown	After treatment A	After treatment C
Platinum	5.65	2.2	Ohmic	Schottky	Schottky
Nickel	5.15	1.8	Schottky	Schottky	Schottky
Gold	5.10	2.4	Ohmic	Schottky	Schottky
Cu	4.65	1.9	Ohmic	Schottky	Schottky
Tin	4.42	1.8	Schottky	Schottky	Schottky
Zn	4.33	1.6	Schottky	Schottky	Schottky
Titanium	4.33	1.5		Schottky	Schottky
Aluminium	4.28	1.5	Schottky	Schottky	Schottky
Silver	4.26	1.9	Ohmic	Schottky	Schottky
Ta	4.25	1.5	Schottky	Schottky	Schottky
Indium	4.12	1.7	Schottky	Schottky	Schottky

Table 7-1 Relationship between work function (φ_m) and electronegativity (χ_m) of metals, and their contact properties with CVD diamond before (as-grown) and after treatment A or C

Table 7-1 shows the effects of treatments A and C on I-V characteristics obtained from point-contact interfaces between CVD diamond films and 11 metals. The I-V characteristics obtained from as-grown diamond films depend on the metal, especially its electronegativity [Mori *et al*, 1990]. After surface treatment, whether by A or C, these dependences disappear and all interfaces show Schottky properties. These changes are due to changes in the surface conditions [Mori *et al*, 1991]. Also shown is relationship between work function (φ_m) and electronegativity (χ_m) of metals, and their contact properties with CVD diamond before (as-grown) and after treatment A or C [Mori *et al*, 1991].

Thus, the effects of treatment C on the I-V characteristics may be considered the same as treatment A. However, treatment with boron has no effect on the I-V characteristics, because it cannot oxidize diamond, and a strong oxidisation ability is essential for the chemical adsorption of oxygen onto diamond surfaces. Treatment D removes oxygen from the oxidized diamond surfaces. When the as-grown diamond films have first been subjected to treatment A, and then to treatment D, their I-V characteristics using Pt, Au, and Al as contact materials were almost the same as those of the as-grown diamond films. From these results, it can be seen that the adsorption of oxygen has a very important role in changing the electrical surface structure related to

Schottky barriers of metal/diamond interfaces. Oxygen adsorbed onto diamond surfaces is stable as even after annealing at 1173K for 1 hour after treatment A; Mori *et al*, [1991] have observed oxygen on surface using x-ray photoelectron spectroscopy (XPS). One possible explanation is that the surface states induced by oxygen adsorption pin the Fermi level [Mori *et al*, 1991].

To hydrogenate diamond films, Baral *et al*, [1996] first immersed them in a boiling ammonium persulphate/sulphuric acid mixture which is known to result in a contaminant-free oxidised surface. Hydrogenation was performed using an atomic hydrogen plasma generated within a standard microwave plasma enhanced CVD chamber (sample temperature 773 K, power 800 W, pressure 40 Torr, duration of 5 minutes) [Williams and Jackman, 2002].

Hayashi *et al*, [1997] cleaned a sample oxidized by an H_2SO_4 and HNO_3 acid solution at 473K for 15 minutes. The aluminium was evaporated to make Ohmic contact, then thermally annealed at 673K for 30 minutes in a nitrogen atmosphere in order to achieve good Ohmic contacts to the oxidized boron doped diamond surface as well as to ensure oxidation of the surface. The oxidized samples are called 'oxidized-boron-doped sample' diamond. After annealing, the sample was ultrasonically cleaned in acetone and methanol, and rinsed with de-ionised water, after which Al-Schottky contacts were deposited.

The following procedures were carried out in UMIST (Manchester). The diamond samples were already cut into small samples of areas 2.25, 8.64, and 22.66 mm^2, each with thickness 0.42 mm. The surface was cleaned before the fabrication of Schottky diodes. Surface cleaning is necessary to ensure an impurity-free surface prior to any processing because the processes of packing and holding leaves the surface of the wafers with considerable amounts of contaminants. These contaminants can diffuse deep into the sample introducing unwanted centres or stay on the surface and affect the device performance.

Wet chemical cleaning was used to clean the sample (which is usually used in UMIST for silicon cleaning) according to the following steps:

1- Contamination was removed from the surface of the samples in a degreasing process according to the following procedure:
   - the sample is rinsed in de-ionised (DI) water,
   - the sample was de-greased using three different solvents; trichloroethylene, acetone and methanol (in that order), and in each solvent the sample was agitated ultrasonically for 3-5 minutes, and
   - the sample is rinsed again in DI water.

2- To remove the metallic impurities, the samples were immersed for 10 minutes in a 70°C solution consisting of NH_4OH, H_2O_2 and DI (H_2O) in the ratio 1:1:5, and then rinsed in DI water.

3- To remove organic impurities, the samples were immersed for 10 minutes in a 70°C solution consisting of HCL, H_2O_2 and DI (H_2O) in the ratio 1:1:6, and then rinsed in DI water.

Samples were always rinsed in DI water not only to wash the diamond samples surfaces but to avoid the mixing of the different chemical solutions. The samples were blown dry using nitrogen gas after each rinse and were kept in methanol prior to the next step. The temperature at steps 2 and 3 must be between 60 and 70 °C. After the wet chemical cleaning was finished, the sample was subjected to oxygen plasma to clean and passivate the surface, and then fabrication of the Schottky diode was carried out. The procedure is to allow the samples to remain in an oxygen plasma chamber for twenty minutes at a pressure of 600 mTorr.

It is acknowledged that this method is far from ideal, but we were hampered by lack of access to all the chemicals used by previous workers. Nevertheless we were able to produce working devices.

7.4.2 Plasma cleaning (passivation)

Each carbon atom in diamond shares four electrons with its neighbours. At the surface the carbon atoms share only three electrons with their neighbours. The surface is passivated by using oxygen plasma, and this stops current leakage across the surface.

After the wet cleaning, passivation was carried out to remove the hydrogen from the surface. The chemical treatment reagents used to clean the sample (see Section 7.4.1) affect only properties of the sample surface, and etching of the diamond is not observed nor expected. This suggests that the conduction mechanism of the as-deposited samples is limited to the surface. However, previous work by Landstrass *et al*, [1989] and Gort *et al*, [1990] has shown that bulk conduction of polycrystalline diamond films is increased by incorporation of hydrogen.

Although a significant number of studies have been carried out on diamond surfaces [e.g. Pate, 1986; Lander and Morrison, 1966; Thomas *et al*, 1992; Matsumoto *et al*, 1981; Mitsuda *et al*, 1991; Tsuno *et al*, 1991] a basic question remains unsolved: what structure or what species exist on the as-grown surfaces. It is now well established by low-energy electron diffraction [Pate, 1986; Lander and Morrison, 1966] and thermal-desorption [Aizawa *et al*, 1993; Thomas *et al*, 1992; Matsumoto *et al*, 1981] studies that hydrogen plays an important role in the reconstruction of diamond surfaces.

The treatment of the external diamond surface surrounding the diode by an oxygen plasma or by heating the sample in air is an essential step for attaining good rectification ratios. This fact indicates that the passivating properties of the oxygenated surfaces are very useful in achieving good diode characteristics [Muret and Saby, 2002].

The {100} surfaces of homoepitaxial diamond layers display very different electronic properties according to the presence of hydrogen or oxygen on them. Hydrogenated surfaces become conductive in air although they exhibit a downward bending of 0.3 eV in UHV. The band bending increases to 0.9 eV for the free surface when the diamond is boron doped. Oxygenated surfaces are highly insulating and strongly improve the Schottky diode characteristics by lowering leakage currents at the diode periphery.

The position of the Fermi level on a diamond film surface, and the band bending, or internal (built-in) electrical field, play an important role in determining electrical and photoelectrical properties, including the yield of electron emission [Bandis and Pate, 1995; Pate *et al*, 1995]. Various surface treatments can change the band bending and even induce a NEA on the diamond surfaces [Bandis and Pate, 1995; Pate *et al*, 1995; Van der Weide *et al*, 1994; Nemanich *et al*, 1995]. Such treatments include either

annealing at elevated temperatures or plasma treatments in various gas environments. For example, it has been demonstrated that hydrogen termination can produce downward band bending and induce NEA on mono-crystalline diamond surfaces [Bandis and Pate, 1995; Pate *et al*, 1995; Nemanich *et al*, 1995; Tachibana *et al*, 1993]. Hydrogen termination is assumed to create the surface dipole that causes a shift in the conduction band level. In contrast, as-prepared or oxygen treated diamond surfaces often exhibit upward band bending and positive electron affinity [Bandis and Pate, 1995; Pate *et al*, 1995; Van der Weide *et al*, 1994; Nemanich *et al*, 1995; Tachibana *et al*, 1993]. However, diamond surfaces treated by oxygen plasma can react with caesium to form a surface with NEA, enhancing field electron emission [Pickett, 1994; Geis *et al*, 1995].

Mori *et al*, 1991 investigated the effects of oxidation of the surface of CVD diamond films on the electrical characteristics of Schottky diodes. I-V characteristics obtained from CVD diamond films without oxygen on their surfaces depend on the metals, especially their electronegativities, but when oxygen is adsorbed onto the diamond surfaces, this dependence vanishes [Mori *et al*, 1991]. It is well known that as-grown CVD diamond films have relatively high-conductivity layers near the surface [Hayashi *et al*, 1997]. The hydrochloric acid (HCL) has p-type conduction, which disappears after oxidation and reappears on exposure to the hydrogen plasma [Hayashi *et al*, 1997; Okushi, 2001].

Landstrass and Ravi [1989] discovered a surface conductivity in as-grown diamond of the order 10^{-5} - 10^{-4} Scm^{-1} at room temperature. It is assumed that (i) either shallow hydrogen-related acceptor states close to the valence band maximum or (ii) band bending caused by hydrogen termination of the surface give rise to a hole accumulation layer [Kawarada, 1996]. Models which assume transport at the diamond surface [Ri-Sung *et al*, 1999; Tsugawa *et al*, 1999], conductive surface layers extending 10 nm into below the diamond surface [Hayashi *et al*, 1997] and transfer doping [Maier *et al*, 2000; Nebel *et al*, 2002] has been proposed.

Vescan [1995], made a comparison between two typical diamond diodes on different layer configurations, with areas of 8×10^{-5} cm^2 (passivated) and 5×10^{-4} cm^2 (non-passivated). The leakage current was reduced below the resolution limit (10 pA). However, the exponential temperature-activated nature of hydrogen still seems to be

present, therefore the reduction in value can be interpreted as a reduction in defect density. Thus the plasma treatment has acted to passivate a substantial number of defect centres. Initial passivation experiments indicate that the defects are native defects generated during growth. However, it seems that the defect-induced nature of the remaining leakage current is preserved. An exponential increase with reverse bias and thermal activation are still evident. The reduction in defect density seems critical to obtain diodes which can operate at high reverse bias and high temperature [Vescan *et al*, 1995].

It has been reported that the resistivity of diamond can be reduced by several orders of magnitude by hydrogen plasma treatment [Landstrass *et al*, 1989]. While this may be beneficial to some electronic devices, the increased surface conductivity will lead to large leakage currents which will hinder device performance [Shenia *et al*, 1989]. The rate of hydrogenation seems to be independent of plasma power and hydrogen pressure. Grain boundaries in polycrystalline films are passivated by hydrogen, and deep traps in bulk diamond are passivated. Controlled hydrogenation can reveal subtle changes in the I-V characteristics of diamond samples [Albins and Watkins, 1990].

7.4.3 Sputtering deposition

In sputtering deposition, the target material is bombarded by energetic ions to release atoms which then condense on the substrate to form the required surface film of the materials. Sputtering has long been observed as a result of glow discharges between two electrodes in vacuum when a film of cathode material was observed on the wall of the cathode crucible. Basically a sputtering system is composed of a vacuum chamber containing cathode and anode plates connected to a voltage source. The chamber is filled by an inert gas (argon in the UMIST system) and the pressure is reduced to an appropriate level using an oil diffusion pump.

Sputtering processes are highly controllable and are generally applicable to metals, alloys, semiconductors, and insulators. Sputtering is a widely used metal deposition technique in microelectronics technology, the advantages are:

- better step coverage than thermal evaporation,
- far less radiation damage than electron beam evaporation,

- much better than either thermal or electron beam evaporation at producing layers of compound materials and alloys, and
- easy monitoring and control of deposition rate and thickness.

Radio frequency and dc sputtering can be used to sputter metals. In sputtering a plasma is created in the chamber by filling it with the inert gas at low pressure and by applying a voltage to the electrodes (~100-150 V for radio frequency sputtering). In this configuration plasma ions are accelerated toward the negative cathode and, when they strike it can release secondary electrons which may collide with the neutral plasma and either ionise or excite the argon gas. The cathode is composed of a copper back plate which is completely covered by a layer of the target material. The terminal is water-cooled and a thermally conductive paste enhances thermal contact between the terminal and the target.

A Dressler Cesar RF136 (13.56 MHz, 600W) generator attached to an Edward 306 vacuum machine was used for the metallisation procedures. Figure 7-1 is a schematic of the sputtering system; the sample is held on the anode and the material of the cathode is used for the metallisation. During diode fabrication, the rear Ohmic contact was formed by sputtering, in turn, 20 nm of titanium, 30 nm of platinum and 300 nm of gold onto the rear surface of the sample. The chamber evaporation pressure was 10^{-6} Torr

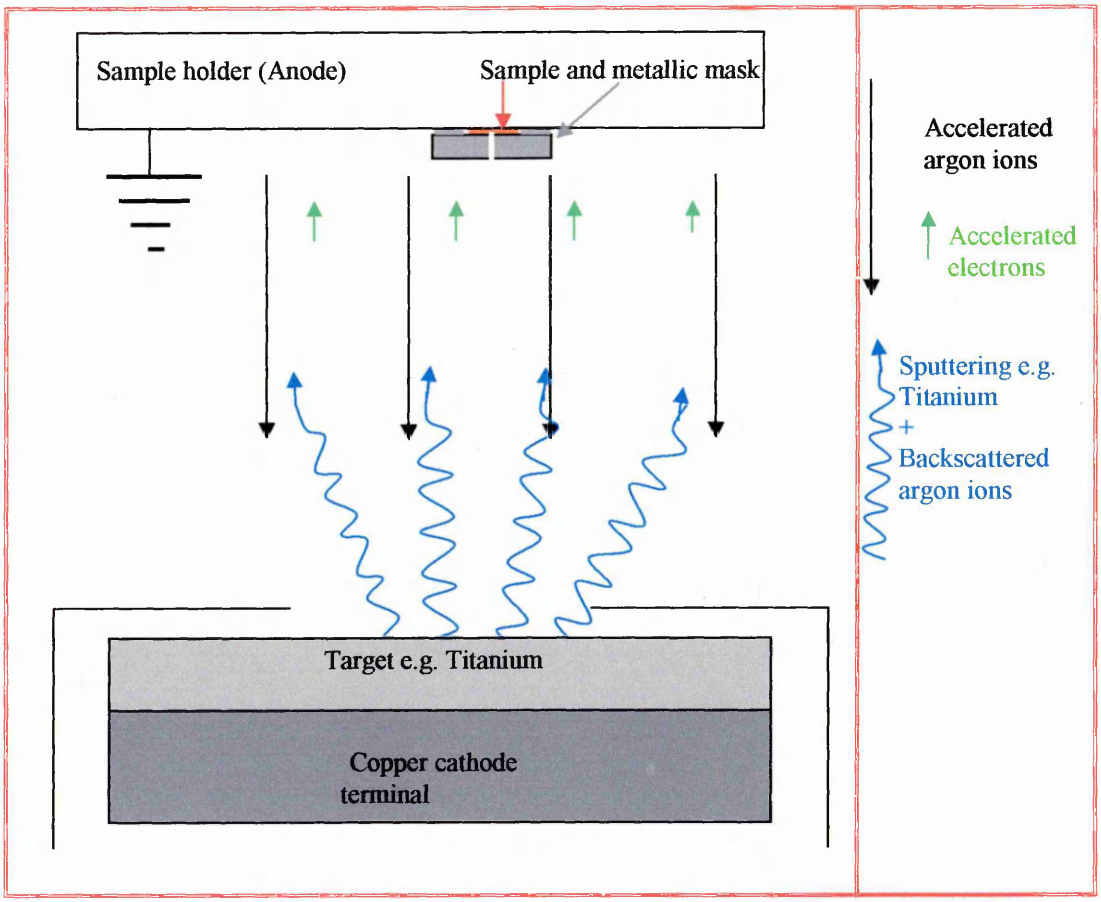

Figure 7-1 Schematic of the sputtering system.

7.4.4 Sample annealing

A number of authors have suggested different procedures for the annealing processes. For example, Gildenblat *et al*, [1990], suggested that the contacts should be annealed in air by heating the sample from room temperature to 1123K over a 20 minutes period, allowing the temperature to stay at 1123K for 5 minutes, and then cooling the sample to room temperature in 10 minutes. This annealing process changes the I-V characteristics of a Au/Ti sandwich contact from rectifying to linear, with a drastic increase in reverse current. However, annealing had virtually no effect on the rectifying I-V characteristics of gold contacts on the same film surface.

Hayashi *et al*, [1997], suggested an alternative procedure, which we have used in this research. After the deposition of the Ti / Pt / Au contact, the samples were annealed at 673K for 20 minutes in a nitrogen atmosphere in order to achieve good Ohmic contacts to the diamond surface as well as to ensure oxidation of the surface.

Immediately afterwards, the samples were ultrasonically cleaned in acetone and methanol, and rinsed with de-ionized water.

7.4.5 Evaporation

Deposition of the aluminium on the front surface of the p-type diamond samples, which was used to fabricate Schottky diodes, was carried out in the evaporation chamber of a standard vacuum coater. A thick tungsten filament was used to hold and heat the Al during the evaporation process. To eliminate any contamination, the filament was first heated by passing a suitable current through it to eliminate any impurities that might be found on the Al surface. Also the aluminium was melted onto the filament in the chamber in the absence of samples to further reduce any contamination adsorbed on the surface of the Al. The aluminium was then evaporated onto the sample's surface at a pressure of $< 10^{-5}$ Torr by passing a suitable current through the filament. The same procedure was used to evaporate aluminium through a metal mask with a series of 0.78 mm^2 area holes to deposit dots of aluminium on the front of the samples, to form Schottky diodes.

Using aluminium to form Schottky contacts should yield a barrier height of 0.8-0.9 eV, making use of the surface potential dependence on work function difference [Kawarada, 1996; Aleksov *et al*, 2003]. Figure 7-2 illustrates a schematic of the thermal evaporation system.

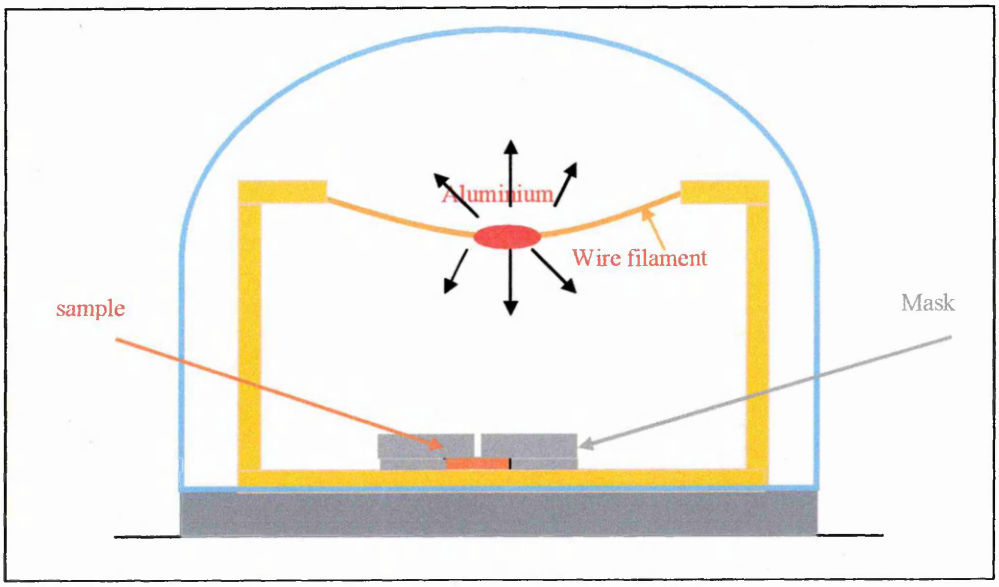

Figure 7-2 Schematic of the thermal evaporation system

7.4.6 Bonding

The samples were mounted onto a ceramic plate which contained gold fingers using silver paint. The silver paint makes a contact between the Ohmic back contact and some of the gold fingers. The samples were then left in an oven for 5 minutes at a temperature < 373 K to remove all solvents from the silver paint. The front contact pad of each diode was gold wire bonded to a gold finger using a West Bond 5400 Motorized Ultrasonic Wire Bonder. This enables probes to be attached to the gold finger for subsequent measurements, eliminating the risk of damage to the diode structure.

7.5 Structure of the diamond Schottky diode

The Schottky diode consists of diamond of 1.5 mm × 1.5 mm, and 2.94 mm × 2.94 mm supplied by Natural Laval Research Laboratory in Washington, and other samples 4.76 mm × 4.76 mm supplied by Element 6. All the samples were of thickness ≈ 0.42 mm, the back surface was sputtered with titanium (layer thickness 20 nm), platinum (layer thickness 30 nm) and gold (layer thickness 300 nm), the total thickness was 350 nm. Aluminium was then evaporated onto the other side of the diamond film to make a Schottky diode with area 0.78 mm^2 as shown in figure 7-3 below, and the Schottky contact shown in figure 7-4.

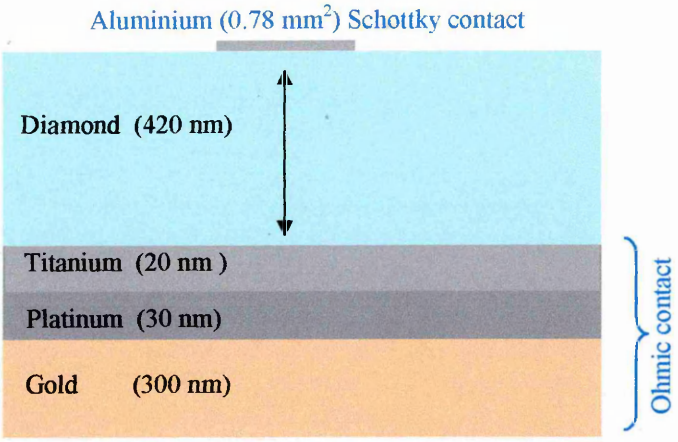

Figure 7-3 Cross-section schematic of the fabricated diode

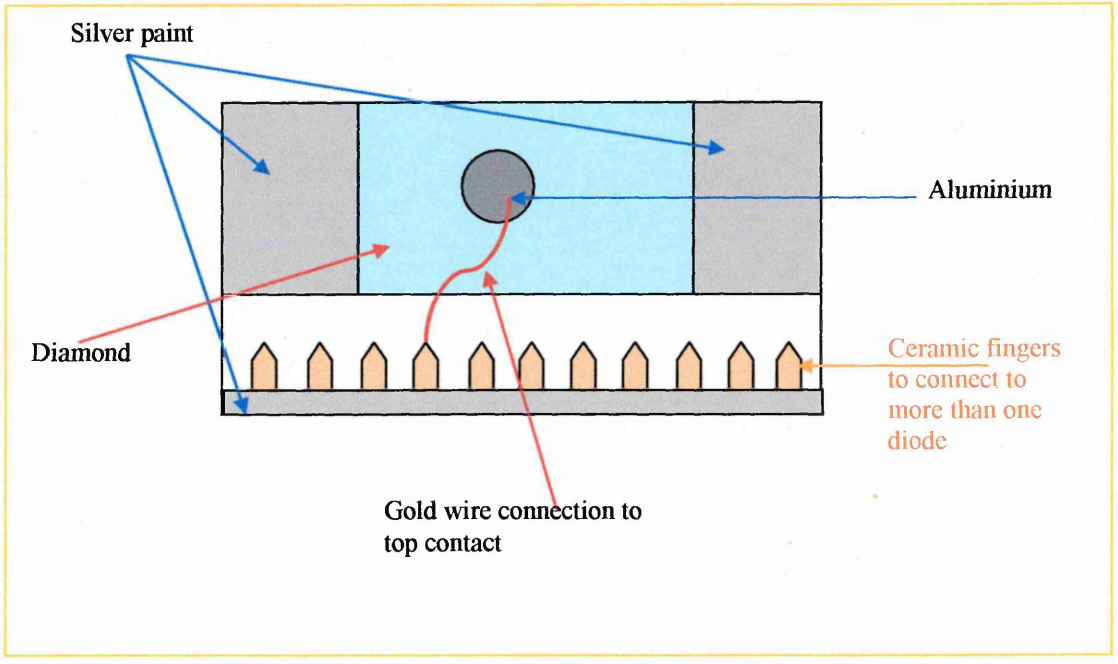

Figure 7-4 Bird's eye view of the Schottky diode mounted on the ceramic substrate

It should be noted that the fabrication process of the diamond Schottky diode (cleaning, sputtering with Ti, Pt, and Au, evaporation of Al) was also carried out on silicon germanium, producing a SiGe Schottky diode which is discussed later in this thesis, Chapter 9.

7.6 Silicon-germanium diode fabrication

The structure of the sample consisted of a virtual SiGe (30%) substrate with thickness of 1500 nm (with Ge mole fraction graded from 0 % to 30 %) grown on top of a pure silicon substrate, on top of that layer, a layer of SiGe (30 %) was grown, then a pure Si layer (on which the Ti Schottky metal is sputtered) is grown. Figure 7-5 illustrates schematic diagram of the SiGe Schottky diode.

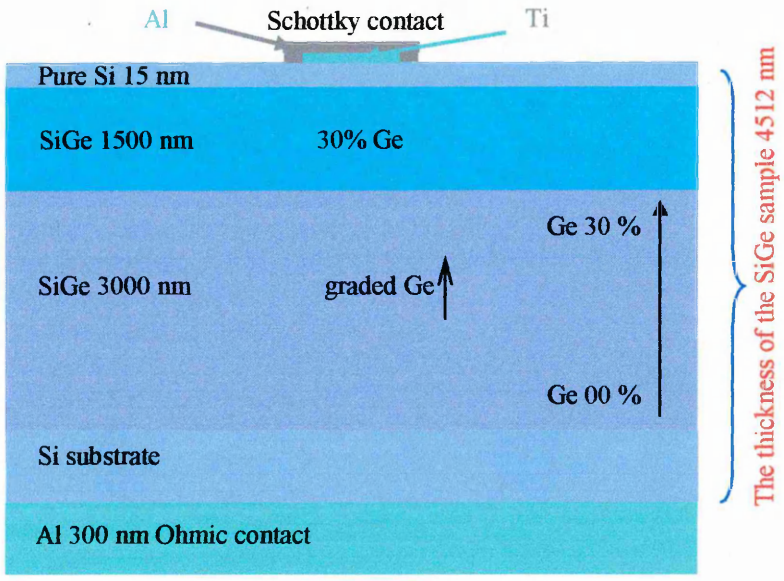

Figure 7-5 Schematic of the SiGe Schottky diode.

Fabricating good quality Schottky diodes on p-type silicon was a difficult task. Due to the small built-in Schottky barrier, the choice of the deposited metal is crucial as is the clean surface quality. Several materials have been assessed during this study (Ag, Al, Pt,...), even though the most widely used in research laboratories is aluminium. In Volpi [2002], experiments with evaporated aluminium showed very high leakage current densities (~ 1A/cm^2 at -1V at room temperature) probably related to poor interface quality. Industrial laboratories usually use a titanium tungsten alloy (Ti-W) but such a compound could not be deposited with the UMIST equipment.

Consequently a choice was made to use pure titanium as this is widely used in metallisation systems due to its excellent adhesion to silicon and silicon dioxide. Titanium is one of the few metals which have been shown to have a higher Schottky barrier in p-type than in n-type silicon [Ng, 1987]. The barrier height on p-Si is reported

to be in the 0.6 eV range [Cowley, 1970; Aboelfotoh and Tu, 1986; Taubentlatt *et al*, 1984]. After several attempts, sputtering led to very good and reproducible diode quality. As we will see in Chapter 9 the SiGe diodes have very low leakage reverse currents and good forward characteristics.

The same procedures used to fabricate diamond Schottky diodes were also used to fabricate SiGe Schottky diodes, starting with cutting the samples, wet cleaning and the fabrication of the Schottky diodes. It should be noted that there were significant new problems in sticking the samples onto the sample mask and holder in the sputtering system.

Figure 7-5 illustrates the fabricated SiGe Schottky diode. It shows the layer structure of the diode: a top layer of pure silicon 15 nm thick (smooth front surface), a second layer of silicon germanium 30 % Ge, 1500 nm thick, a third layer of silicon germanium graded started from 0 % Ge at the bottom to 30 % in the top, 3000 nm thick, and the (fourth) substrate surface which is pure silicon. More details will be given in Chapter 9. At the top of the Schottky diode is a dot of metal which may be either titanium or gold. At the bottom is the aluminium Ohmic contact. The fabrication was carried out many times using many different ways for sputtering the Schottky diode, to get acceptable quality diodes.

With the SiGe samples the cleaning procedures described above were used. The rear was covered with evaporated aluminium as the Ohmic contact, then the Schottky contact was sputtered onto the face. The titanium did not bond well for all diodes, and a number of samples had to be fabricated to make sure that the quality of the final diode was satisfactory. In an attempt to avoid this problem we changed the metal and instead of Ti we tried silver, gold, ... etc, but when the I-V and C-V measurements were made it was found that the flow of the current was very low, the reverse bias was very high and the phase angle was not more than 60° for all the measurements and materials used. We also tried diffusion of boron into the rear surface of the SiGe samples to improve the Ohmic contact, before sputtering the Ti, Au or Al front contact.

The major problem was found to be the manner in which the mask was used. By holding the mask fixed in one position when sputtering and avoiding leakage under the shadow mask, acceptable quality diodes were fabricated by sputtering Ti and Au as a

Schottky contact. Subsequent measurement of I-V and C-V characteristics showed the leakage the current to be very small (~10^{-6} A), and the phase angle 85° -89°, which means the diodes were suitable for use in other measurements. Chapter 9 will give more details about the silicon germanium structures.

7.7 Summary

In this chapter the properties of Schottky diodes are discussed and the fabrication of a diamond Schottky diode is reported. It is demonstrated that using aluminium as the Schottky contact allows the production of a good Schottky barrier diode. All the steps carried out to prepare the samples for Schottky diode fabrication are described, though only briefly. Finally, the preparation and fabrication of SiGe Schottky diodes, including the layer structure of the fabricated SiGe diode is presented.

The following chapter will discuss the I-V and C-V characteristics of the fabricated Schottky diodes (diamond and silicon-germanium, and DLTS, LDLTS measurements.

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Chapter 8

Electrical characterisation of Schottky diode on diamond

8.1 Introduction

In this chapter, methods of electrical characterisation of semiconducting diamond, including I-V and C-V measurements, are presented. Problems associated with the C-V technique are discussed. DLTS and LDLTS results are also presented.

The aims of the work described in this chapter were to: (i) establish that the depletion region width in the thin semiconducting p-type diamond samples could be manipulated by the application of a reverse voltage, and that the geometric depletion region had not been reached; (ii) to examine the series resistance of a p-type diamond Schottky diode by studying the phase angle between current and voltage as a function of the applied voltage, and capacitance as function of temperature of the device and frequency of the signal; (iii) to investigate the ability to detect deep electrically active defects in diamond Schottky diodes.

A preliminary study of the quality of Schottky diodes on boron doped CVD diamond is presented. It is demonstrated that the depletion region width can be varied by the applied voltage even in a thin sample. Moreover, it is shown that the phase angle is sufficient for capacitance DLTS to be carried out. The variation of the phase angle with voltage is consistent with a slightly varying series resistance as the depletion region increases. This is analogous to similar tests carried out on silicon. This chapter paves the way for a high temperature study by DLTS of deep levels in the material.

The samples used in this work were supplied by two companies. They have different dimensions and doping. Table 8-1 below shows the description of those samples. It should be noted that, the carrier concentration in the samples was experimentally measured as the suppliers did not enclose any data about doping in the samples.

Supplier	Diamond Trading Company (Element 6)		Natural Laval Research Laboratory, Washington	
Number of samples	2	2	4	4
Sample colour	blue	Light blue	Light blue	Light blue
Sample dimensions (mm)	4.76×4.76×0.42	4.76×4.76×0.42	1.5×1.5×0.42	2.94×2.94×0.42
Capacitance at 0V and 300K temperature (pF)	102.46	31.5	70	72
Measured carrier concentration (cm^{-3})	1.78×10^{18}	1.6×10^{17}	2×10^{16}	2.3×10^{16}

Table 8-1 Description of the samples used in this work

We had no information about the boron concentration but was assumed to be of the order of 18^{18}-10^{19} cm^{-3} from the colours.

8.2 Energy band diagram of diamond Schottky diode

Figure 8-1 (a), shows the variation of the depletion region width for boron doped (w_2) and undoped (w_1) diamond. Figure 8-1 (b) shows the equivalent circuit diagram.

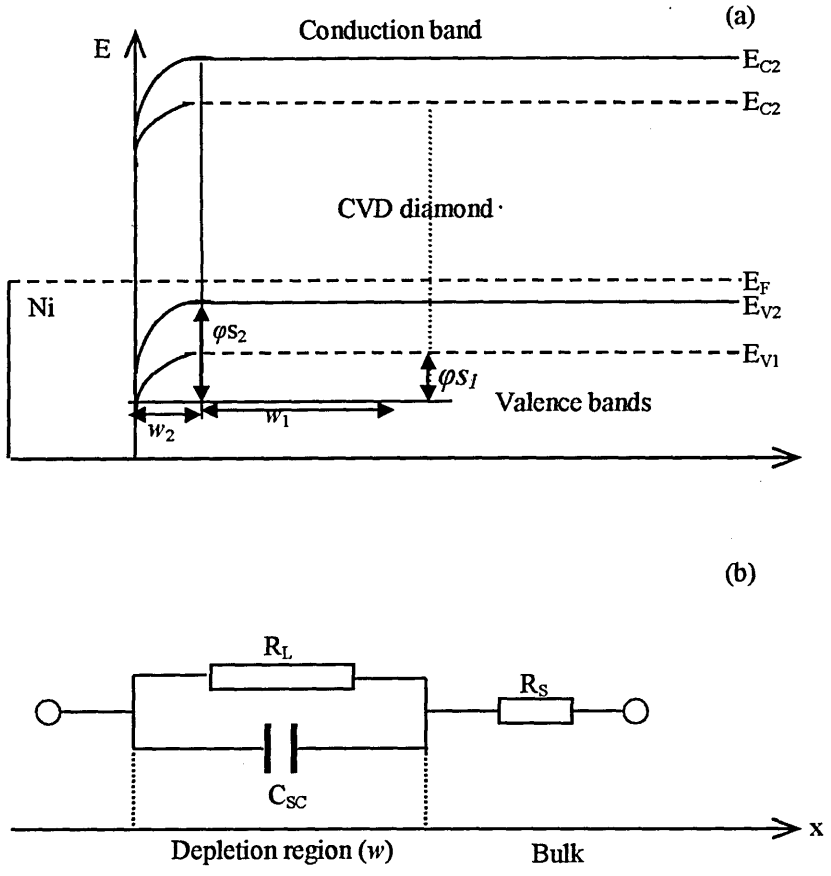

Figure 8-1 (a) and (b) shows a schematic view of the energy band diagram for B-doped and undoped diamond films and the equivalent circuit respectively: R_S is the bulk resistance of diamond; C_{SC} is the capacitance of the depletion region or space charge region, R_L is the resistance determining the leakage current of the Schottky contact [Polyakov *et al*, 2001].

Boron forms an acceptor in diamond with an ionisation energy of 0.37 eV. Boron is present in the very rare type IIb natural diamonds [Mainwood, 1999, Kajihara *et al*, 1993, Werner and Locher, 1998]. If the boron concentration is 1.6×10^{17} cm^{-3}, such natural diamonds are semiconducting at room temperature [Collins, 2002]. If for example $N_A = 8\times10^{15}$ cm^{-3} one can calculate the Fermi level in a p-type Schottky diode as $E_V-E_F = kT/q[\ln (N_A/N_V)]$,where $N_V = 1 \times 10^{19}$ cm^{-3} and $kT/q = 0.026$ V. With these values it is found that the Fermi level position is 120 meV above the valence band, but this assumes total boron ionisation at room temperature. This is very unlikely to be the case.

Figure 8-2 illustrates the Fermi level position when the diamond is extrinsic and when doped, where V_B is the bottom of the band gap, E_{Fi} the intrinsic Fermi level, E_A the acceptor level, E_F the Fermi level when the diamond is doped with boron and the ionised boron concentration is 8×10^{15} cm^{-3}, and C_B is the upper conduction band of the diamond diode. In reality, because of compensation by nitrogen, the Fermi level will be nearer mid-gap than this at room temperature.

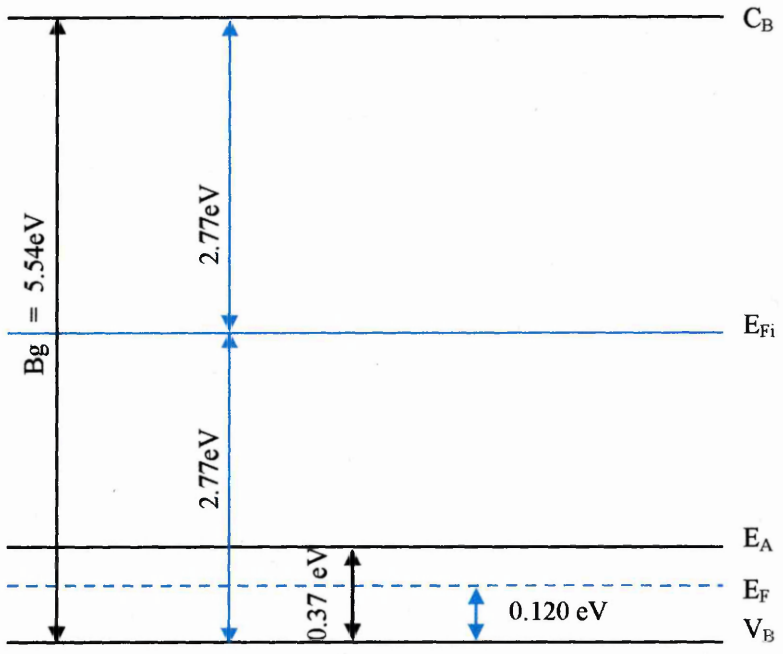

Figure 8-2 Band diagram of the Schottky diamond diode

8.3 Electrical characterisation

I-V and C-V characteristics are very important because they give valuable information about the diodes under test; I-V measurements are also needed to be sure that the diodes have the rectification necessary for DLTS, LDLTS and other measurements. It is also important to have information about the reverse leakage current of a junction diode before the DLTS and LDLTS measurements are carried out.

I-V measurements were performed to determine the leakage current of each diode. Low-leakage Schottky contacts are required for C-V characterisation. The C-V measurements were performed as a function of bias for frequencies as high as 1MHz.

The quality of the C-V data was determined by analysing the phase angle, which should be nearly 90° for an ideal diode.

C-V measurements made on boron-doped diamond are helpful to explore the acceptor density and contact properties. In the case of CVD diamond, where the quality of the layers has improved significantly over recent years, this technique has distinct advantages compared to Hall effect measurements [Nebel *et al*, 1999]. C-V measurements are concentrated on the depletion layer below the rectifying or blocking contact. Since the acceptors in the depletion layer are not ionised at all temperatures, the measurement of acceptor concentration (N_A) and the donor concentration (N_D) from C-V characteristic would require full thermal ionisation [Polyakov *et al*, 2001], because C-V measures carrier concentrations. The depth profile indicates the carrier concentrations at various depths, and shows depth variation with reverse-bias voltages.

8.3.1 Current-voltage characteristics

I-V curves are the most commonly used characterisation tool for semiconductor devices. The dc characterisation set-up essentially consists of a Hewlett-Packard HP4140B Semiconductor Parameter Analyser (SPA) and a PC. The current is typically measured for voltages in the range ~ -15 to 5 V, steps of ~ 0.1 V. The measurements are controlled by UMIST software (see Chapter 5). Typical experimental values of the current are in the range 10^{-6} to 10^{-8} A at room temperature for diodes on diamond with area 0.78 mm^2. The forward branch of the I-V characteristic is dominated by the diode series resistance, which is exponentially dependent on temperature. When the diode is forward biased the current follows the relationship given by equation (5.3).

In figure 8-3, the section of the curve to the right of the current axis shows the electrical characteristics of a typical diode in the forward biased region where the above equation applies; current flows easily because the diode has a certain amount of resistance, and a voltage drop occurs as current flows through the diode. A typical diode causes a voltage drop of about 0.6 to 1 V according to the forward region.

When the forward current becomes very large the current saturates, and $exp(qV/kT)>>1$, $n=1$, and

$$I \approx I_s \, exp\,(qV/kT) \qquad 8.1$$

At room temperature ($T = 300$K), q/kT is about $40V^{-1}$, and the forward bias current may be approximated as

$$I = I_s \exp(40V) \qquad 8.2$$

The gradient of the I-V curve at any point gives the resistance of the forward bias junction. Here $\frac{dI}{dV} = 40I_s \exp(40V) = 40I$, hence $\frac{dV}{dI} = \frac{1}{40I} = r$, where r is the dynamic resistance of the forward biased junction. When I is expressed in mA, $r \cong 25/I$.

When the voltage is applied in the reverse direction, there will be greater resistance to current flow. The leakage current should be typically a few nA in diamond, but is found to be much higher. (as $I \approx -I_s$ when the exponential component is near zero).

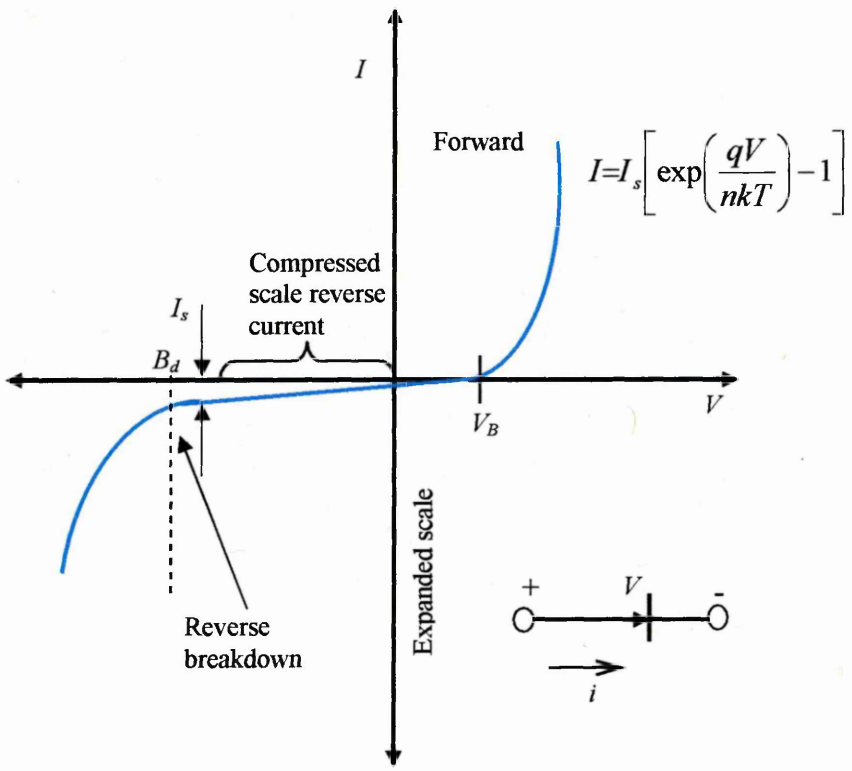

Figure 8-3 Diode I-V relationship with some scales expanded and other compressed in order to reveal details.

All the I-V measurements on the samples were undertaken at room temperature with the bias voltage varying from -15 to 5 volts, and the maximum detectable current was 15 mA. The fabricated diodes were placed on the holder and were held by a sprung gold pin to ensure good contact. Before carrying on the measurements, the diode is checked for polarity, i.e., the reverse bias connection was checked Figure 8-4 and figure 8-5 illustrate the I-V curves for low and high boron doped diamond Schottky diodes. At low applied forward bias, very little current is observed, until the potential difference reaches the barrier potential (~1 V for diamond), when holes start crossing the junction in ever increasing numbers and a rapid increase in current results. The point at which the increase is observed is called the "Knee", "offset voltage" or built-in potential (V_B).

In the forward biased region, when $V > 0$, the current flowing through the highly boron doped diode, and the low boron doped diode is very small ($< 10^{-6}$, $< 10^{-7}$ A respectively). However, once the applied voltage exceeds the barrier voltage, free electrons or holes (depending on whether the material is n-type or p-type), begin crossing the junction in large numbers causing an exponential increase in the current. When the voltage across the diode is reversed, the diode current is extremely small ($< 10^{-7}$ A). As mentioned earlier, this is the reverse saturation current or the leakage current (I_s). There is practically no increase in the leakage current until the applied voltage reaches the breakdown voltage. Note that both the voltage and current scales are presented in such a way as to show an extremely small reverse current and a relative large breakdown voltage. The breakdown voltage depends upon the level of doping. Therefore, the breakdown voltage for diodes can vary anywhere from a few volts to a few kilovolts. As soon as the applied voltage exceeds the breakdown voltage, the diode begins to conduct heavily readily.

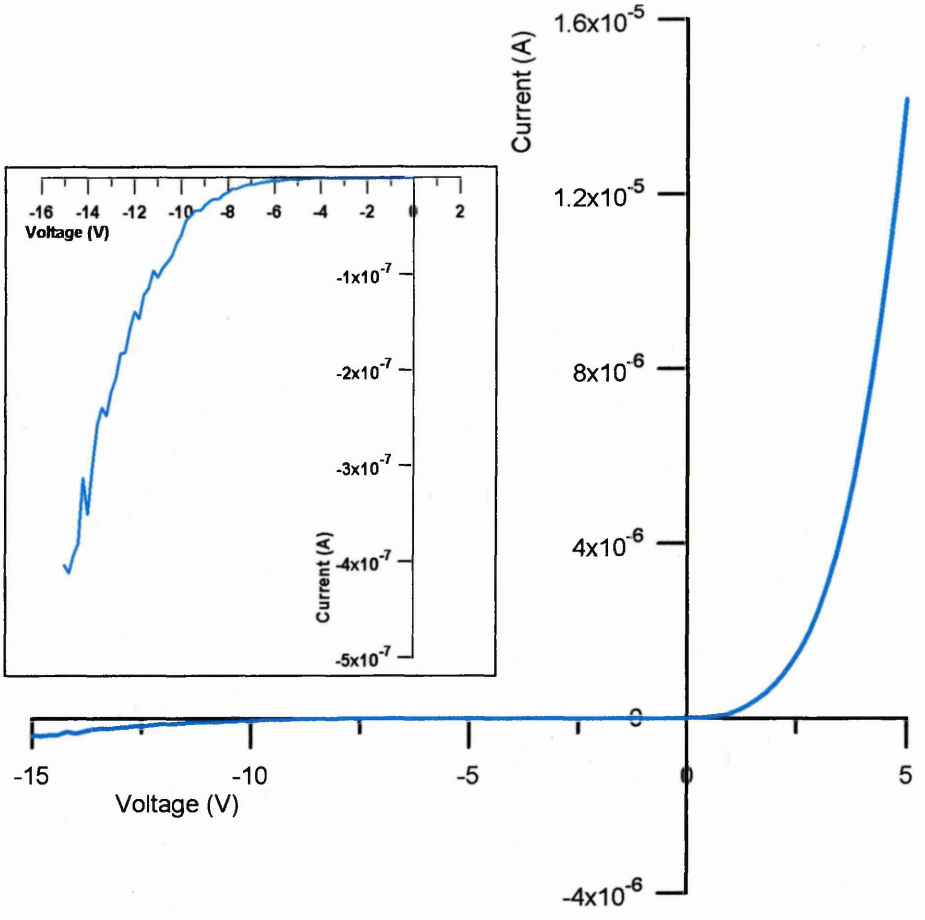

Figure 8-4: I-V measurement of a low boron doped diamond sample. The window shows reveres biased I-V curve for the same sample with an expanded current scale over the range –16 to 2V.

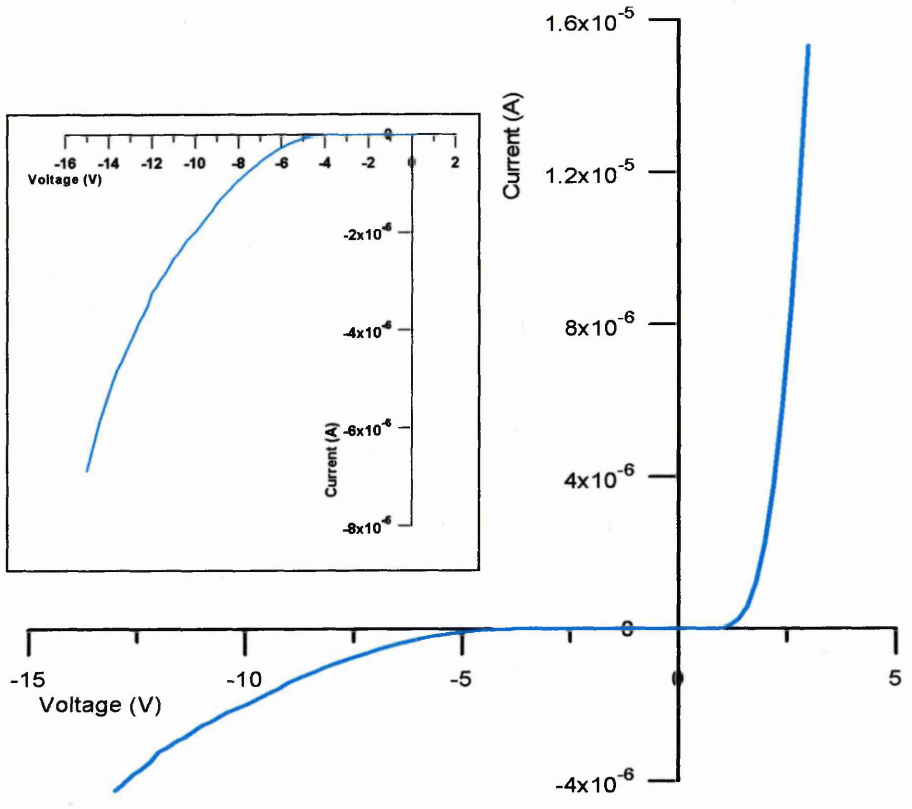

Figure 8-5: I-V measurement of high boron doped diamond sample. The window shows reveres biased I-V curve for the same sample with an expanded current scale over the range –16 to 2V.

It can be seen that the high boron doped sample suffers higher leakage reverse current (2.54×10^{-6}A) than the low boron doped sample (1×10^{-7}A) at a reverse bias of -11V. When the diode is forward biased, the high boron doped sample exhibits better characteristics than the low boron doped sample – nearly 7.58×10^{-7}A for low doped boron compared to 2.24×10^{-6} A in case of high boron doped samples. Figures 8-4 and 8-5 show that the higher the doping level, the lower the resistance of the diode in both forward and reverse bias.

In polycrystalline diamond films the grain boundaries may act as a conduction channel which could transport holes to the surface as a leakage current [Huang *et al*, 1994]. The grain boundaries are readily seen when scanning electron microscopy is performed on the samples (see section 8.7). However, at low voltages the diodes rectify and are therefore suitable for C-V profiling. This would indicate that our cleaning process was suitable and all the fabrication procedures were correct.

8.3.2 Forward-bias I-V characteristics as a function of temperature

Metal-semiconductor contacts are important components of semiconductor devices. The electronic properties of such a contact (Schottky barrier diodes-SBDs) are characterised by its barrier height (BH) and ideality factor. Song *et al*, [1986] reported that barrier height differences over the contact area occur because of variations in the interface layer thickness and/or composition and also due to interfacial charges in a real Schottky barrier. Sullivan *et al*, [1991] have confirmed that the current across the metal-semiconductor contact may be greatly influenced by the existence of SBD inhomogeneity. Numerical simulations indicate that regions of low SBH are often pinched-off when the size of these regions is less than the average depletion width. Cetin *et al*, [2004] have shown that the parameters of SBDs vary from diode to diode even if they are identically prepared [Cetin *et al*, 2004]. For Schottky diodes operating at room temperature, the dominant transport mechanism is thermionic emission of majority carriers from the semiconductor over the potential barrier into the metal [Sze, 2002].

Analysis of the I-V characteristics of the Schottky barrier measured only at room temperature does not give detailed information about the conduction process and the nature of barrier formation at the metal semiconductor interface. The temperature dependence of the I-V characteristics allows us to understand different aspects of conduction measurements. Extrapolation of the linear portion of the forward I-V curve to V = 0V gives us experimental values for n and, from I_s and equation 8.2 we can obtain the BH [Sze, 2002]. A detailed knowledge of the conduction process involved is essential to extract barrier parameters, namely the barrier height and ideality factor. Moreover, Schottky diodes with low BH have found applications in devices operating at cryogenic temperatures; infrared detectors and sensors in thermal imaging [Rhoderick and Williams, 1988; Horvath, 1996; Werner and Guttler, 1991; Song *et al*, 1986; Schmitsdorf *et al*, 1995; Sullivan *et al*, 1991; Tung, 1991; Monch, 1999; Zhu *et al*, 2000; Chand and Kumar, 1995; Karadeniz *et al*, 2004; Tugluoglu *et al*, 2004]. So, information about electrical characteristics at low temperatures is vital for a better understanding which will enable us to tailor the devices to particular requirements.

The current through a SBD at a forward bias V, based on thermionic emission theory, is given by Rhoderick and Williams, [1988], from, which one can find the Schottky BH of the p-type diamond diode (φ_B) using the following equation:

$$\varphi_B = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_s}\right) \qquad 8.3$$

where I_s is the saturation current derived from the straight line intercept of the log I-V plot at V = 0, and the symbols are as defined in Section 5.4. The SBHs are found to be 1.25 eV for the Aluminium contact, assuming that A^* is 84 A $cm^{-2}k^{-2}$ using an effective mass of 0.7 m_o [Kiyota *et al*, 1996]. Also Schottky diodes on p-type diamond show a barrier height of $\varphi_B > 1.5$ eV and low ideality factor of $n = 1.1$ [Vescan *et al*, 1995], thus making them attractive for high temperature application. Theoretically, the high barrier should result in an immeasurably low reverse current levels and high breakdown voltages. Indeed, on natural diamond, such behaviour is observed [Vescan *et al*, 1995; Geis *et al*, 1993; Humphreys *et al*, 1991]. The ideality factor n is given by

$$n = \frac{q}{kT}\frac{\Delta V}{\Delta \log I_s} \qquad 8.4$$

The value of n estimated by Kiyota *et al*, [1996] ranges from 1.2 to 1.8. The smallest value, of 1.2, is the nearest to unity ever reported for oxidized diamond. In this work I-V measurements were performed in the temperature range between 200 and 400K. The measured I-V plots of the p-type Schottky barrier diodes in the temperature range of 200-400K are shown in figure 8-6. From least-squares fits of equation 5.5 to the linear part of the measured I-V plots the experimental values of n and φ_B were determined. Once I_o is known, the zero bias BH can be computed with the help of equation 8.3. The n and φ_B determined from semilog-forward I-V plots were found to be a strong function of temperature; the ideality factor n was found to increase, while the barrier height φ_B decreased with decreasing temperature. However since current transport across the metal semiconductor interface is a temperature-activated process, holes at low temperatures are able only to surmount the lower barrier and therefore current transport will be dominated by current flowing through the regions with a lower SBH and a larger ideality factor, as explained in [Sullivan *et al*, 1991; Tung, 1991; Monch, 1999; Zhu *et al*, 2000; Chand and Kumar, 1995; Karadeniz *et al*, 2004; Tugluoglu *et al*, 2004]. As the temperature increases, more and more holes have sufficient energy to surmount the regions of higher barrier. As a result, more current flows at lower bias at higher temperatures. An apparent increase in the ideality factor is

caused possibly by other effects such as inhomogeneities of thickness and non-uniformity of the interfacial charges. This gives rise to an extra current that remains consistent with the thermal emission process [Chand and Kumar, 1995; Karadeniz *et al*, 2004; Tugluoglu *et al*, 2004]. This result is attributed to inhomogeneous interfaces and BHs because of the inverse proportional linear relationship between the BH and ideality factor as shown in figure 8-10. For evaluation and determination of the BH in another way, one may also make use of the Richardson plot of the saturation current [Tugluoglu *et al*, 2004]. Equation 8.4 can be rewritten as

$$\ln\left(I_s/T^2\right) = \ln\left(AA^*\right) - \frac{q\varphi_B}{kT} \qquad 8.5$$

In this research, for the first time, we study the forward bias current-voltage characteristics and barrier parameters in p-type diamond Schottky diodes in the temperature range 200-400K, by using a temperature-controlled cryostat. The temperature dependence of the barrier height and the ideality factor are discussed using the thermal emission theory with a Gaussian distribution of the barrier heights around a mean value due to the barrier height inhomogeneities prevailing at the metal-semiconductor interface.

By carrying out the I-V measurements at different temperatures, the barrier height will change. Figure 8-6 illustrates that the barrier height of diamond doped with a low proportion of boron decreases with increasing temperature.

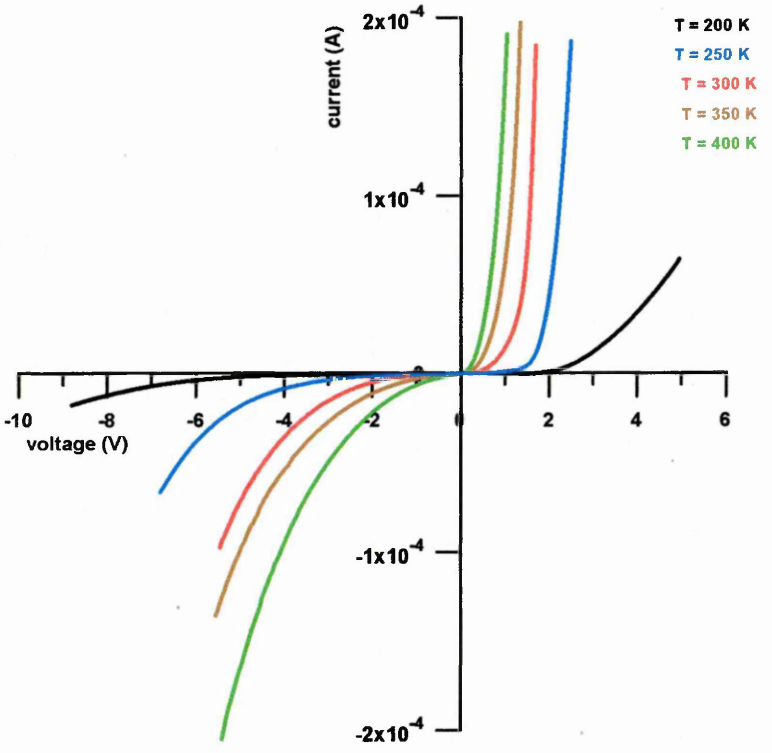

Figure 8-6 Variation of the current and barrier height with temperature of a diamond Schottky diode doped with a low proportion of boron.

At room temperature there is a gradual rise in current at low forward bias, which is contrary to what is expected for an ideal diode. This is likely to be caused by the large series resistance of the diamond films, and the lack of total ionisation of the boron.

Figure 8-6 shows the temperature variation of the I-V curves from 200 to 400 K. The leakage current increases with increasing temperature and rectification decreases until the rectification disappears at temperatures above 400K and Ohmic behaviour is obtained. This effect is probably due to the presence of a high density of electrically active defects at the interface between diamond and metal contributing to a large generation current at higher temperatures. As explained by Nishimura *et al*, [1991] the resistivity decreases with increasing temperature, increasing the current flow, which suggests impurity levels are deep and not activated at room temperature. Figure 8-7 shows the I-V characteristics and change of the barrier BH quality silicon of Schottky diode for comparison.

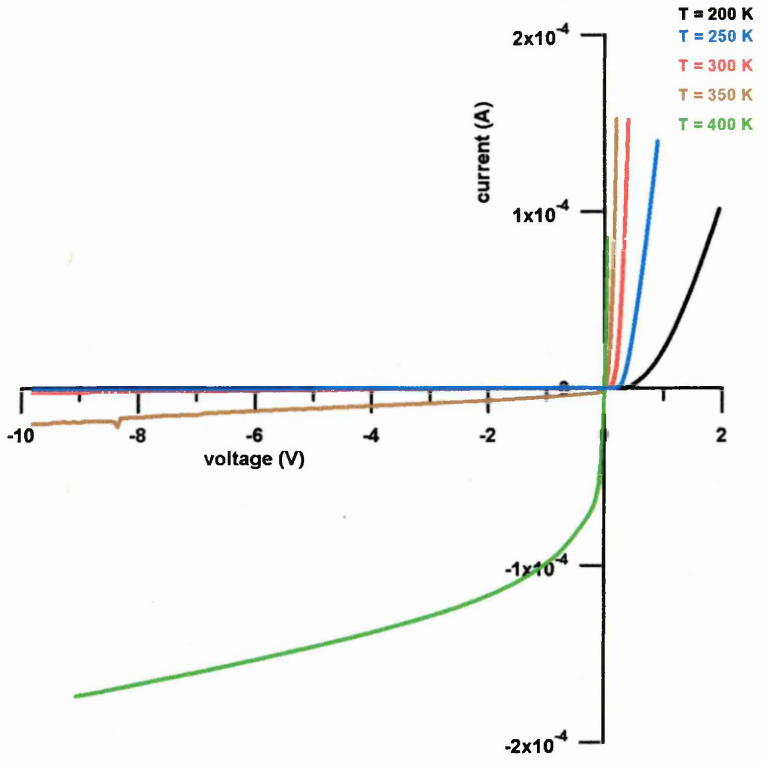

Figure 8-7 Variation of current and barrier height of a silicon Schottky diode with change of temperature

From figure 8-6 and figure 8-7 it can be seen that the behaviour of the diamond Schottky diode and silicon Schottky diode are very similar, but the BH is essentially nearly zero when the temperature reaches 400K in the silicon diode and it appears to behave like a resistor. From the two figures the SBH (φ_B) increases with a increasing in temperature, and the leakage current increases with reverse bias, which agrees with the results of Ru *et al*, [2003]. A useful property of Schottky diodes on diamond is that the forward voltage drop is higher than the voltage drop of a Schottky barrier on silicon.

By applying equation 8.4 we can find the barrier height of the p-type diamond Schottky diode from figure 8-4 by plotting ln (I_s) vs V. Here k is the Boltzmann constant (1.38×10^{-23} J.K^{-1}), T is the temperature at the time the I-V measurement was made, q is the electronic charge (1.6×10^{-19} C), A is the area of the Schottky diode (0.78×10^{-2} cm^2), I_s is the saturation current which is determined from figure 8-8, for every temperature, A^* is the effective Richardson constant calculated from equation 8.7 [Kiyota *et al*, 1996]

$$A^* = 4\pi q m^* k^2/h^3 \qquad 8.6$$

Where, m^* is the mass of hole in aluminium which equal $0.7m_o$, $m_o = 9.1\times10^{-28}$ kg, h is the Planck's constant (6.6×10^{-34} J s). By applying equation 8.4 for the SBH and equation 8.4 for the ideality factor (n) to every temperature the result for I_s as a function of temperature and voltage are as shown in table 8-2, and figure 8-8.

T(K)	I_s (A)	φ_B (eV)	n	$1/T$	$1000/T$	$ln(I_s/T^2)$
200	1.4×10^{-8}	0.794	2	0.005	5	28.68
250	6×10^{-8}	0.971	1.7	0.004	4	27.67
300	2.8×10^{-7}	1.135	1.5	3.33×10^{-3}	3.3333	26.5
350	7×10^{-7}	1.306	1.2	2.86×10^{-3}	2.872	25.89
400	2×10^{-6}	1.466	1	0.0025	2.5	25.11

Table 8-2 The ideality factor and barrier height of lower doping p-type diamond Schottky diode.

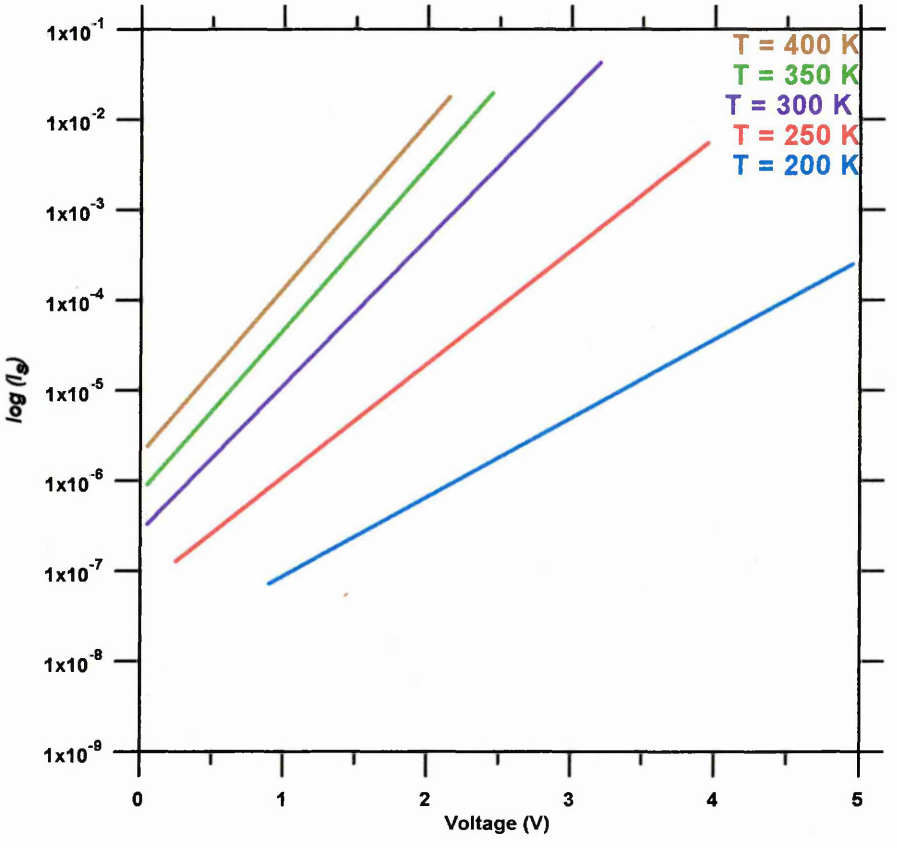

Figure 8-8 Derivation of the derived saturation current (I_s) with the voltage for the lower doped diamond

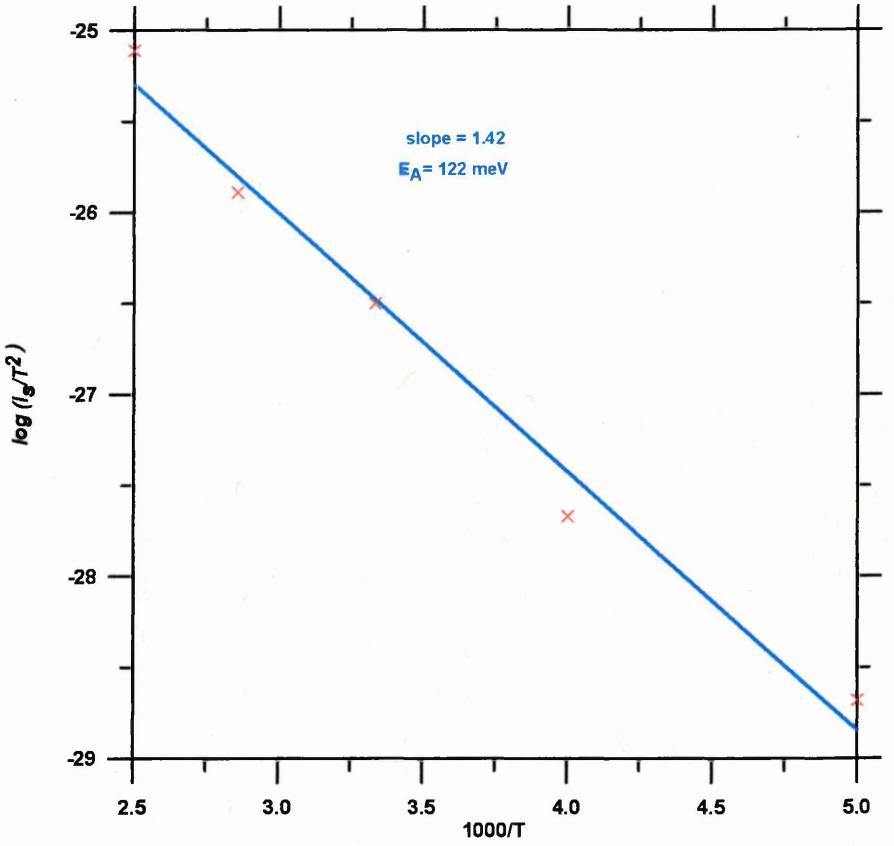

Figure 8-9 Arrhenius plot of ln (I_s/T^2) against $10^3/T$ for the lower doped diamond

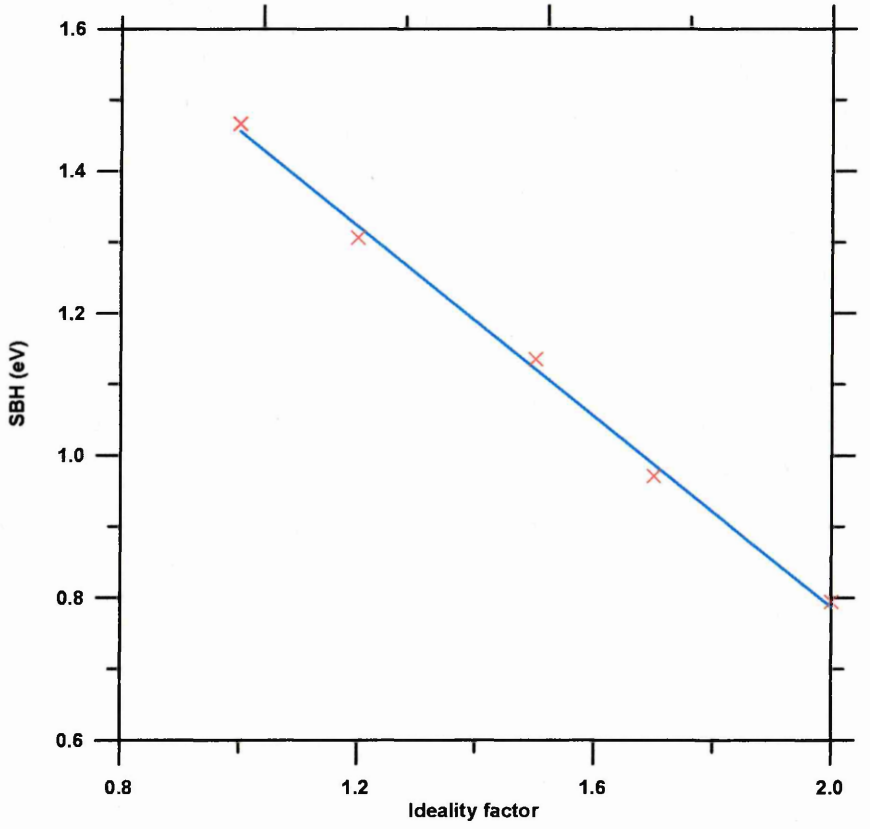

Figure 8-10 Relation between the SBH and the ideality factor for the lower doped diamond.

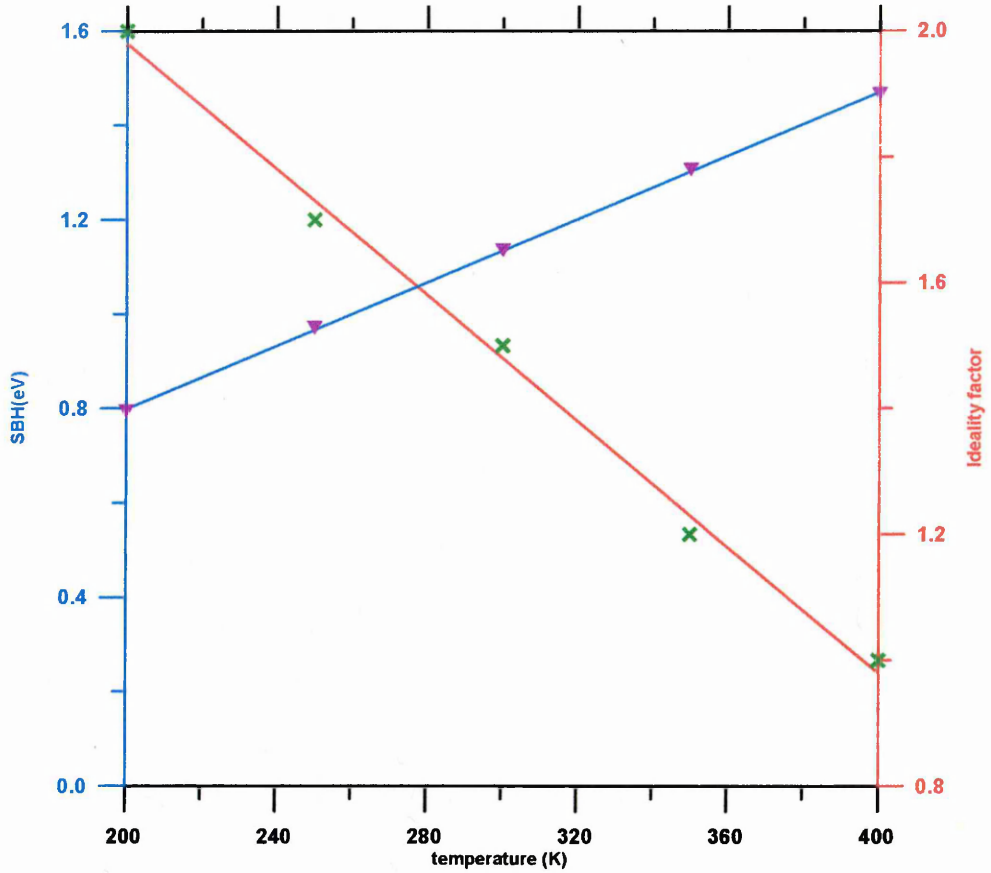

Figure 8-11 Variation of SBH and n with temperature for lower doped diamond.

Figure 8-9 shows the Arrhenius plot of ln (I_s/T^2) against $1000/T$. The dependence of ln (I_s/T^2) on $10^3/T$ is found to be nearly linear in the temperature range used as shown by equation (8.5). The non-linearity in the conventional ln (I_s/T^2) versus $10^3/T$ is caused by the temperature dependence of the BH and ideality factor. Similar results have also been found by several authors [Zhu *et al*, 2000; Chand and Kumar, 1995; Karadeniz *et al*, 2004]. Moreover, in figure 8-9 the slope of the line gives an activation energy of 122 meV. The activation energy of the device is the energy required to transfer the carriers between the Fermi level and valence band or conduction banpd. The deviation in the Richardson plots may be due to the spatial inhomogeneous BHs and potential fluctuations at the interface that consists of low and high barrier areas [Werner and Gutter, 1991; Zhu *et al*, 2000; Chand and Kumar, 1995; Karadeniz *et al*, 2004; Tugluoglu *et al*, 2004]. In other words, the current of the diode will flow preferentially through the lower barriers in the potential distribution. As was explained by Horvath [1996], the A^* values obtained from the temperature dependence of the I-V characteristics may be affected by the lateral inhomogeneity of the barrier, and the fact that it is different from the theoretical value which may be connected to a value of the real effective mass that is different from that calculated.

The BH was extracted from a Richardson plot (taking the points with low ideality factors) by Vescan *et al*, [1998] giving φ_B = 1.9 eV. In the high temperature limit the ideality factors approach unity at high current levels. The forward current is limited by the series resistance, which is a function of temperature. The activation energy in the low temperature range is 0.25 eV, dominated by the resistance of the low-doped epitaxial layer. With increasing temperature there is a slight deviation from the exponential behaviour which indicates an increasing contribution of the substrate resistance (which shows typical activation energies of 0.1 eV [Vescan *et al*, 1998]).

If one observes a change in capacitance due to the change in a material's resistivity (rather than an experimental artefact), then one should observe an associated change in the current through the diode as the temperature is reduced; figure 8-12 shows that this is indeed the case. Figure 8-12 shows the forward current measured at different temperatures and different forward biases at one frequency (1 MHz). The current increases with increasing temperature and at the same time the current increases with increasing voltage. At a voltage of 2 V the current is increasing very quickly. The relation between the current and voltage can be clearly seen in figures 8-4 and 8-5.

Figure 8-12 shows that the current decreases significantly with temperature and we note the change in capacitance, attributed to carrier freeze out.

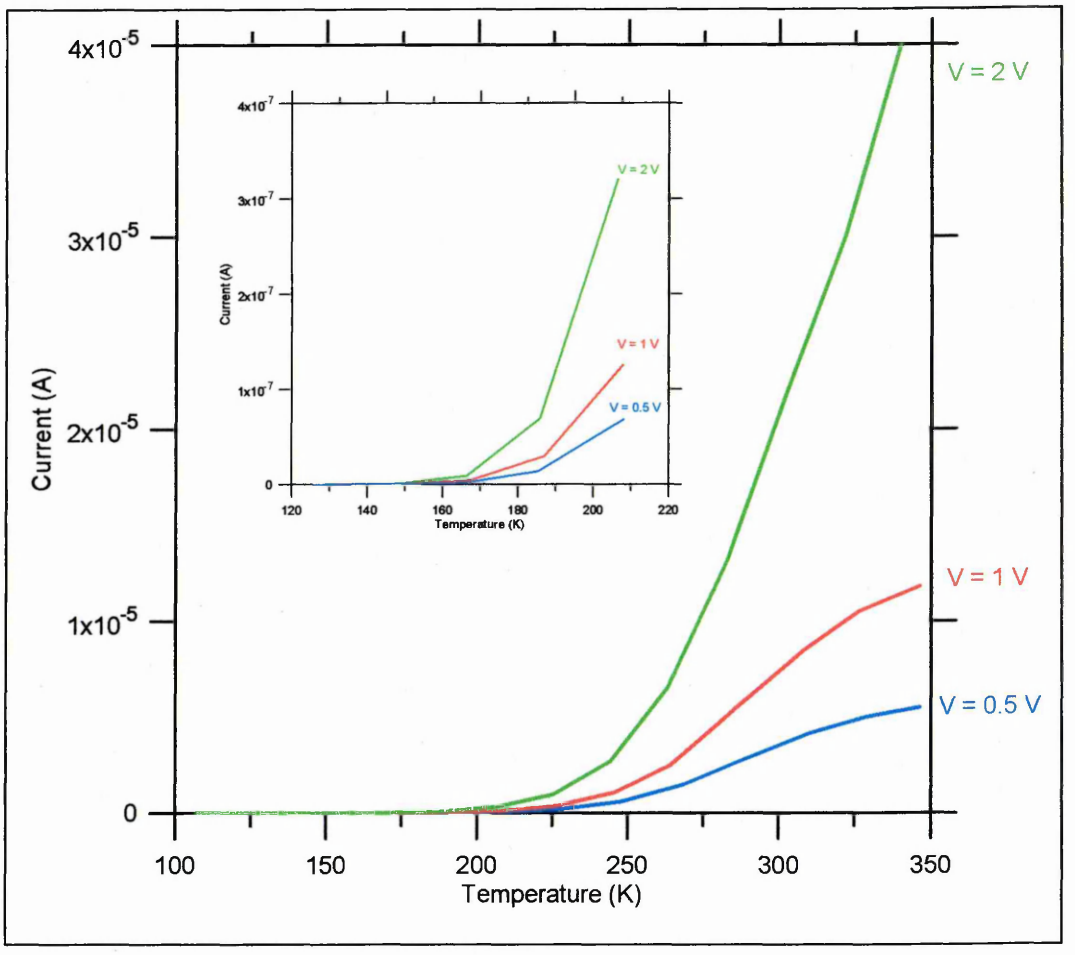

Figure 8-12 Forward bias current through the lower resistivity diode as a function of temperature for three different voltages. Inset is a high resolution plot of the carrier freeze out region.

8.3.3 Capacitance-voltage characteristics

C-V measurements can be used to study the most basic properties of semiconductor rectifying junctions. In addition to obtaining simple capacitance values at a given bias, which may be important for circuit simulation, the data can be manipulated to yield a number of other parameters such as the built-in potential, V_{bi}, the doping profile as a function of depth [Hilibrand and Gold, 1960, Iniewski *et al*, 1994] and barrier height [Goodman, 1963]. C-V measurements also form the basis for more advanced analysis techniques such as DLTS [Palmer, 1990]. Some of the more basic techniques will now be discussed in greater detail [Shabbir, 1998].

Firstly, I-V measurements were performed to determine the leakage currents for each diode, because low leakage currents are required for C-V characterisation. The C-

V measurement gives information on capacitance as a function of applied voltage and is used to determine the quality of the diode as it allows the phase angle to be measured. A good diode should have an infinite parallel resistance and have a phase angle of nearly 90°. Also, C-V profile can show the variation of carrier concentrations with depletion region depth and the change of depletion region depth with reverse bias. Typical plots of C-V and C^{-2} - V at 1 MHz for a boron doped film are shown in Figures 8-13 and 8-15 respectively. The linearity of the C^{-2}-V plot over the entire bias range shows the homogeneity of the acceptor concentration within the depletion region.

In practice, measurements of this type are performed using a high frequency capacitance bridge circuit. In this work, C-V measurements were carried out at room temperature using the HP 4192B Impedance Analyzer (5Hz-13MHz). The capacitance is measured at different reverse bias values by superimposing a small-amplitude ac voltage on the dc voltage. The reverse bias (V_R) is typically varied in the range 0 V to -10 V in steps of 0.1 V - 0.3 V. The capacitance was measured at a frequency of 1 MHz, the diode area was 0.78 mm^2, and the amplitude and frequency are controlled by UMIST software which not only plots the C-V curve but also calculates all the other parameters.

Figure 8-13 shows the capacitance and phase angle as a function of voltage for low boron doped diode. It can be seen that the phase angle is slightly more than 86° for all reverse biases in the studied range, which indicates that the diode is of acceptable quality. Also from the figure it is clear that capacitance is decreased by increasing the reverse bias which again indicates that the diode has a very good quality.

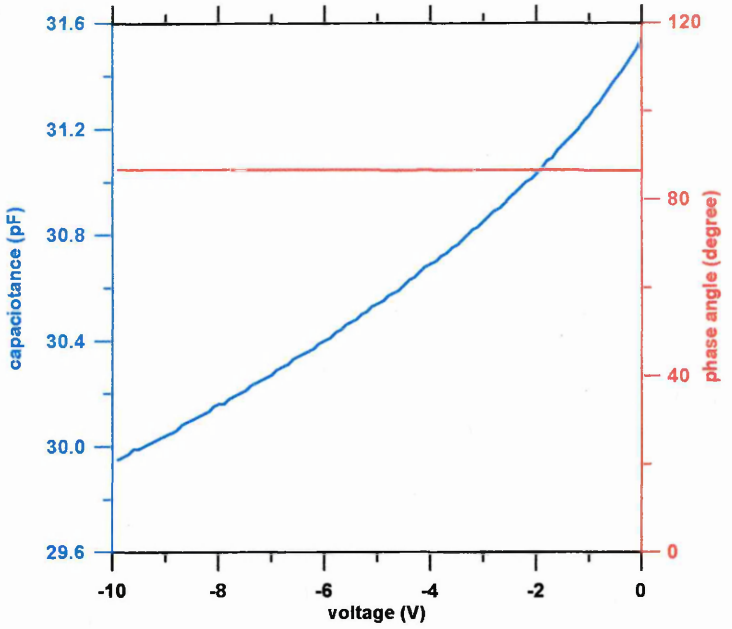

Figure 8-13 C-V measurement for low boron doped diode diamond.

By studying the phase angle as a function of voltage we can examine the resistance of the p-type diamond. Figure 8-14 is a higher resolution version of figure 8-13 which shows that the phase angle slightly decreases with the decrease in the reverse bias. The change in the phase angle is very small from 86.5° to 86.8°, a range of only 0.3°, over a reverse bias range of 0 to -10 volts, at room temperature. These results support the use of the diodes for DLTS and LDLTS measurements over the given reverse bias range, until the breakdown voltage is reached. It should be noted that the measured phase angle at zero voltage and at room temperature (300K) was, on average, 87.5° for all the diodes; this is deemed to present an acceptable diode quality. The variation of the phase angle is due to the variation of the depletion region width while the rest of the device (the bulk section) has a significant series resistance.

It is also noted that figure 8-13 shows that the capacitance varies from 29.9 pF to 31.6 pF over a reverse bias range from 0 to -10 V, that means, the capacitance variation (ΔC) is 1.7 pF over 10V . This change in the value of the capacitance is very small (and difficult to determine).

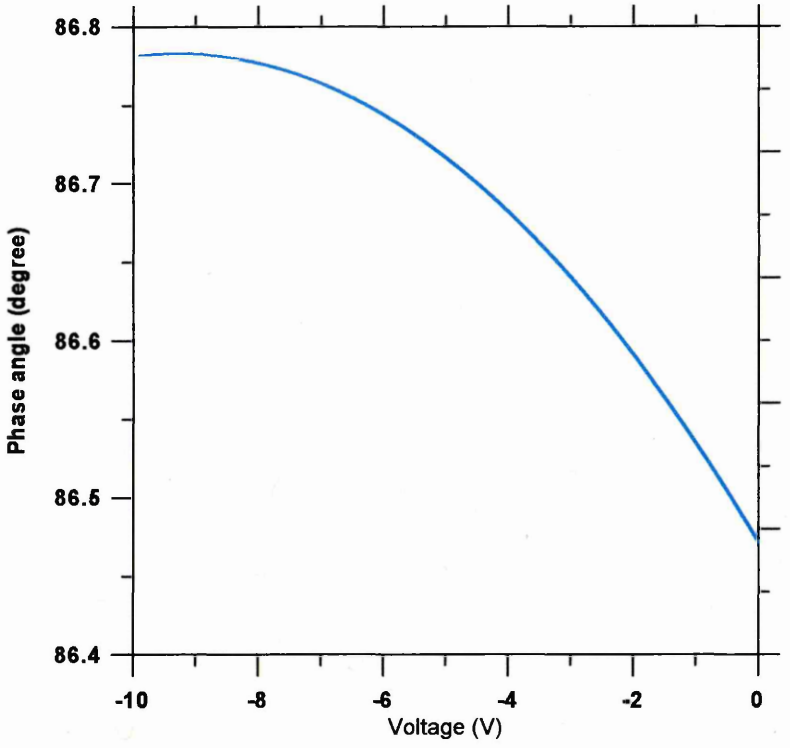

Figure 8-14 Change of phase angle of Schottky diode on diamond with reverse bias voltage

The measured C-V data can be manipulated to plot a graph of C^{-2} versus V_{app} using the following equation [Singh,1994];

$$C^{-2} = \left(\frac{2}{qN_A \varepsilon_o \varepsilon_r A^2} \right) \left(V_{bi} - V_{app} \right) \qquad 8.7$$

Equation 8.7 suggests that the intercept of the curve on the C^{-2} axis ($V_{app} = 0$) will yield the built-in potential, V_{bi}.

The doping concentration is obtained by plotting C^{-2} against the voltage V and taking the slope $d(C^{-2})/dV$; the depth (w) at which the concentration is evaluated is calculated using the following equation [Schroder 1998];

$$w = \left[\frac{2\varepsilon_r \varepsilon_o \left(V_{bi} - V_{app} \right)}{qN_A} \right]^{1/2} \qquad 8.8$$

where, ε_r is the relative dielectric constant, ε_o the free space permittivity, $\varepsilon_r \varepsilon_o = \varepsilon$ which is the total permittivity of diamond.

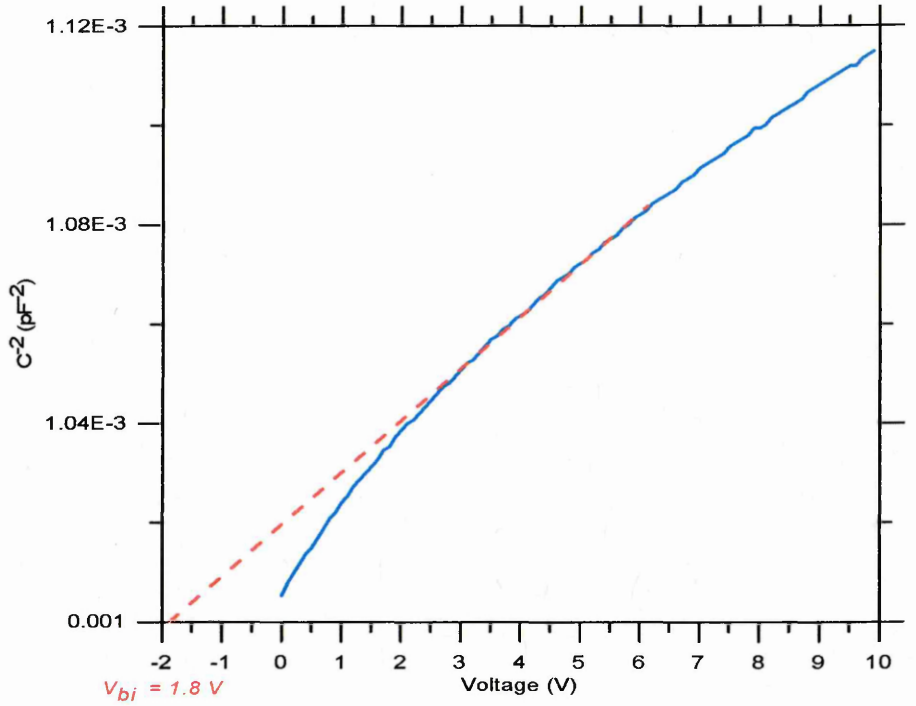

Figure 8-15 C^{-2} as a function of forward bias V_{app} on low boron sample

Using the data in figure 8-15, the BH of the Schottky diode can be calculated from equation 8.9

$$\varphi_B = V_{bi} + E_F + \frac{kT}{q} \qquad 8.9$$

where $$E_F = \frac{kT}{q} \ln \frac{N_A}{N_V} \qquad 8.10$$

From figure 8-15 V_{bi} = 1.8 V where V_{bi} is the built in potential, also the slope is proportional to N_A (=8×10^{15} cm^{-3}),

For p-type diamond, $N_V \approx 1\times10^{19}$ cm^{-3}, and kT/q = 0.026 J/C at room temperature. From equation 8.10

$$E_F = 0.026 \ln (8\times10^{15}/1\times10^{19}) = -120 \text{ meV}$$

Therefore the BH (φ_B) from this C-V measurement is:

1.8 + (-0.12) + 0.026 = 1.7 eV,

which shows a good diode with BH 1.725 eV.

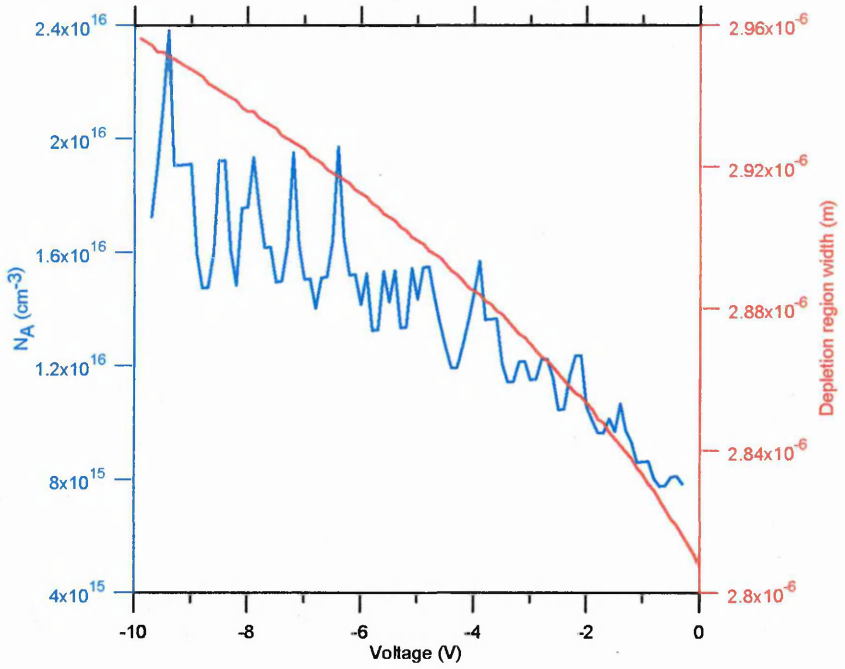

Figure 8-16 Change in carrier density and depletion region as a function of voltage width for the low boron doped sample.

Figure 8-16 illustrates the carrier concentration (N_A), and depletion region width (w) as a function of voltage. The figure shows that the depletion region width increases very slightly with increasing reverse bias, and the carrier concentration varies from 8×10^{15} cm^{-3} to $\approx 2\times10^{16}$ cm^{-3} as the voltage is varied from 0 to -10 volt. This is almost certainly due to hydrogen passivating the boron nearer the surface, because the carrier concentration decreases towards the surface.

The doping profile for the semiconductor wafer, i.e. a plot of the doping concentration versus the distance from the junction, can be derived using one of two possible sets of equations. Firstly, the depletion region width (corresponding to a measured capacitance value or applied bias) can be calculated from equation 6.1.

The use of equation 8.7, however, requires V_{bi} to be determined using the intercept of C^{-2} from equation 8.7, see figure 8-15. Secondly, the doping concentration, N_A, (corresponding to measured capacitance value) can be determined using the following equation:

$$N_A = \left[\frac{C^3}{\left(q\varepsilon_o\varepsilon_r A^2\right)}\right]\left(\frac{dC}{dV_{app}}\right)^{-1} \qquad 8.11$$

Equation 8.11 is derived by manipulating equation 8.7 and manipulating and differentiating equation 8.10.

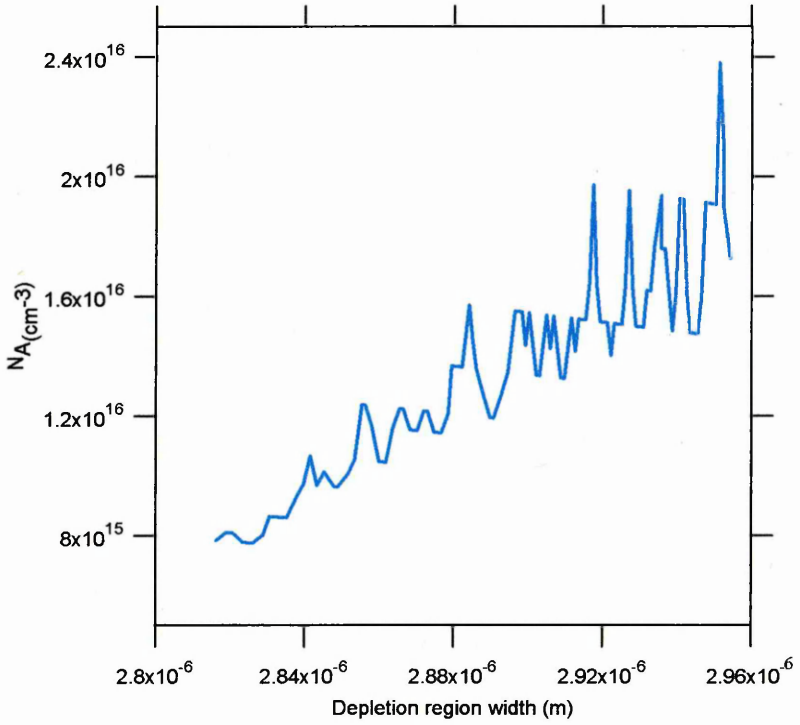

Figure 8-17 Carrier concentration of low boron diamond Schottky diode as a function of depletion region width (w).

Figure 8-17 shows that the concentration of carriers (p) increases with increasing depth (w). The carrier concentration calculated from the C-V curve is reduced near the surface, as is often observed in silicon where the dopant has been passivated by the unintentional introduction of hydrogen. In silicon the hydrogen-boron complex is very strongly bonded and is electrically inactive, and the same is true in diamond.

Figure 8-18 shows the capacitance as a function of temperature at a fixed (constant) voltage of -1V of the semiconducting diamond that has resistivity of 800 Ω-cm. The capacitance is not defined below about 180K, but increases rapidly above about 240K, which is coincident with the lower boron atoms beginning to ionise, hence the capacitance rises as temperature rises, and the depletion region becomes smaller. This clearly shows the effect of the hole freeze-out onto the acceptor boron atoms between

200K and 300K. Higher resistively diamond showed the same effect at the same temperature.

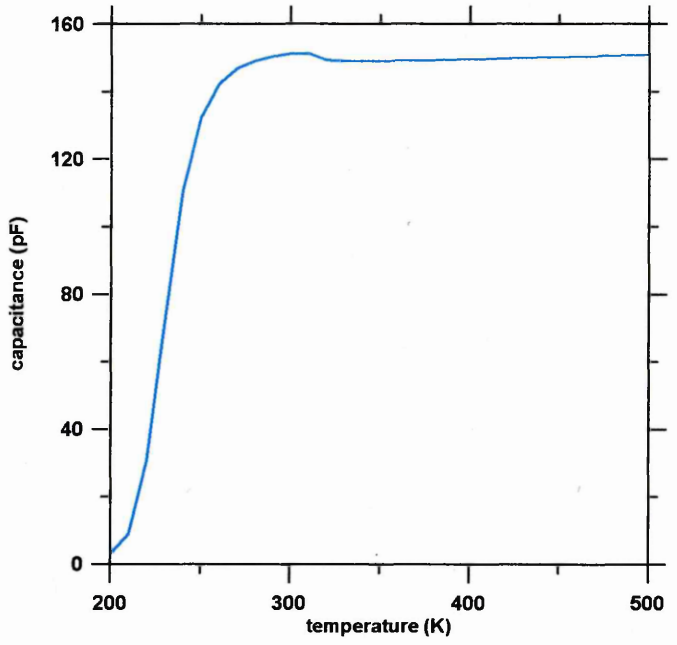

Figure 8-18 Capacitance as a function of temperature of semiconducting diamond with a resistivity of 800 Ω-cm. Carrier freeze-out onto the boron atoms occurs between 200 K and 300 K in diamond.

8.3.4 Phase angle versus temperature

C-V can measure the phase angle at a given frequency as a function of temperature, and the phase angle at a given temperature as a function of frequency. The measurements were made at different voltages (-2, -1, and 0 V) to confirm the results, but only the measurements taken at -1 V are shown in Figures 8-19 and 8-20. The temperature was varied between 200 and 500K and the frequency between 10 kHz and 10 MHz. The carriers were largely frozen out below 200K which is why this was chosen as the lower limit of the temperature range.

The phase angle generally increases with increasing temperature up to about 250K. At this temperature the phase angle reaches about 86° for all frequencies in the range 200 kHz to 4 MHz. That means a good diode is achieved above 240 K, for frequencies between 200 kHz and 4 MHz. Below 240 K the dopants are not ionised and there are hardly any free holes. Therefore below 240 K the diamond has a high series resistance and a poor phase angle is to be expected.

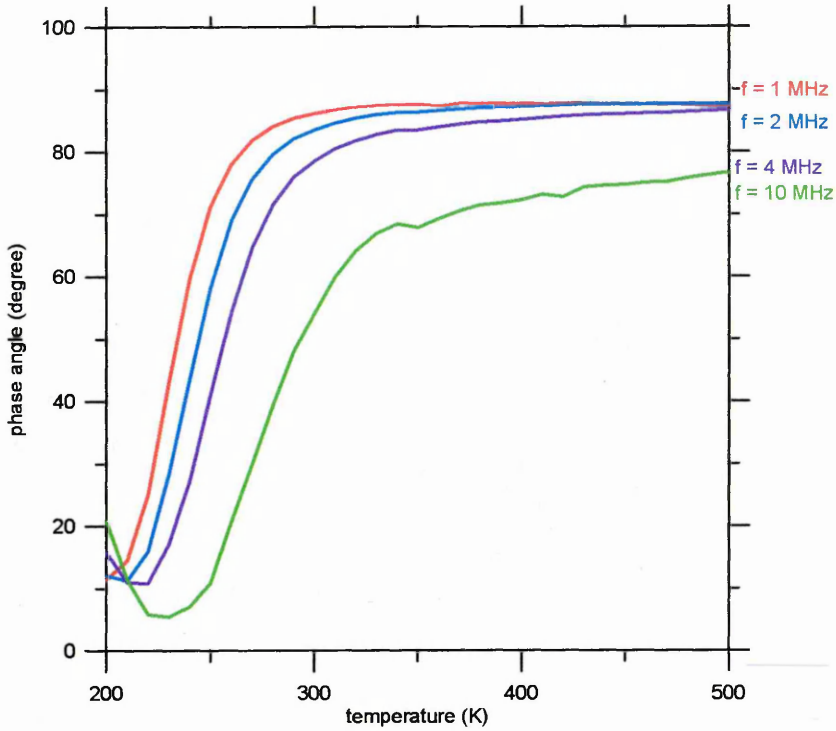

Figure 8-19 Phase angle versus temperature at various frequencies in high boron doped diamond measured at 1-10 MHz.

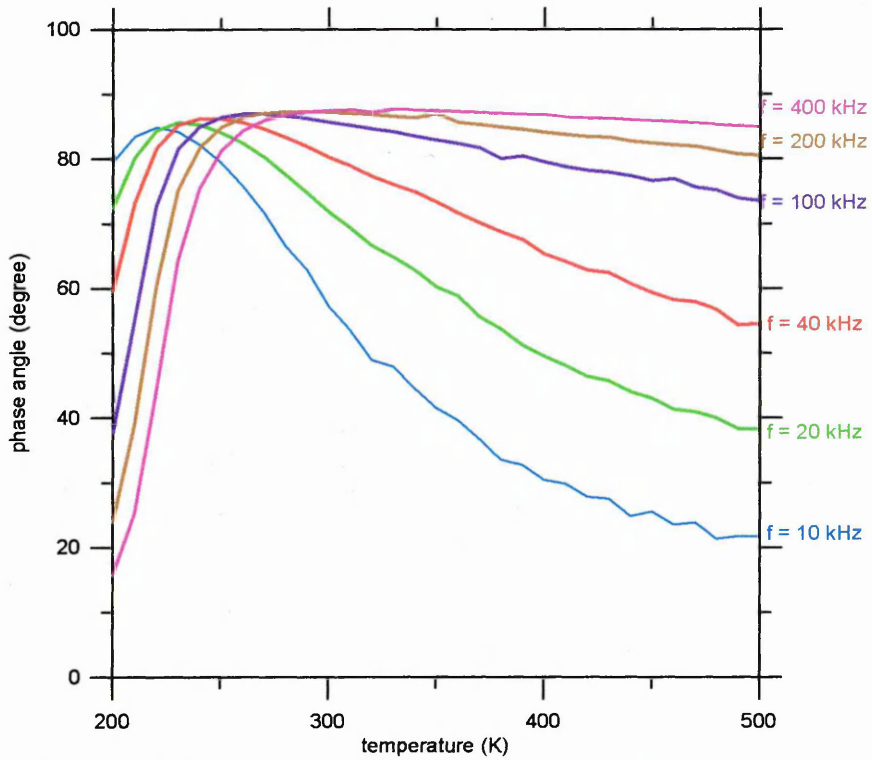

Figure 8-20 Phase angle versus temperature in high boron doped diamond measured at 10-400 kHz

As can be seen in figures 8-19 and 8-20, the diode shows the best behaviour in the range from about 400 kHz to about 4 MHz, and when the temperature is between about 300K and 500K. Outside these ranges the diode becomes either resistor-like or acts as an insulator. When the temperature is less than 220K, the phase angle is less than 80° for all frequencies, and when the temperature is more than 300K the phase angle is less than 80° for frequencies less than 400 kHz or greater than 4 MHz. To confirm these results figure 8-21 shows the phase angle versus frequency (between 0 and 1MHz) at different temperatures. This figure confirms the results obtained from figures 8-19 and 8-20.

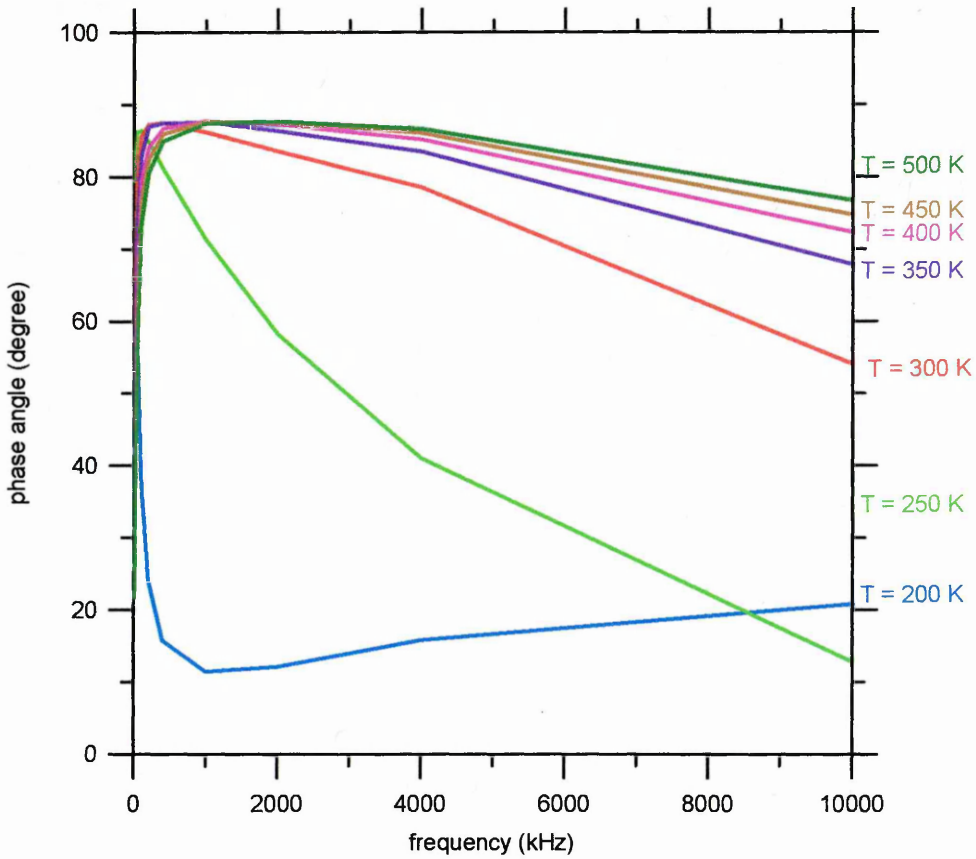

Figure 8-21 Phase angle versus frequency at different temperatures in high boron doped diamond

8.3.5 Capacitance versus temperature

The variation of capacitance with temperatures and reverse bias is shown in Figure 8-22. The temperature was changed from 200K to 500K at different reverse bias voltages between 0 and 4 volts.

The capacitance increases with temperature very rapidly until about 220 to 250K, after which, depending upon the bias, the capacitance levels off. This means that substantial ionisation of the boron is reached before about 280K. From the measurements of the phase angle as a function of temperature and capacitance it is possible to deduce that hole emission from boron acceptors should take place over the temperature range 220K to 300K.

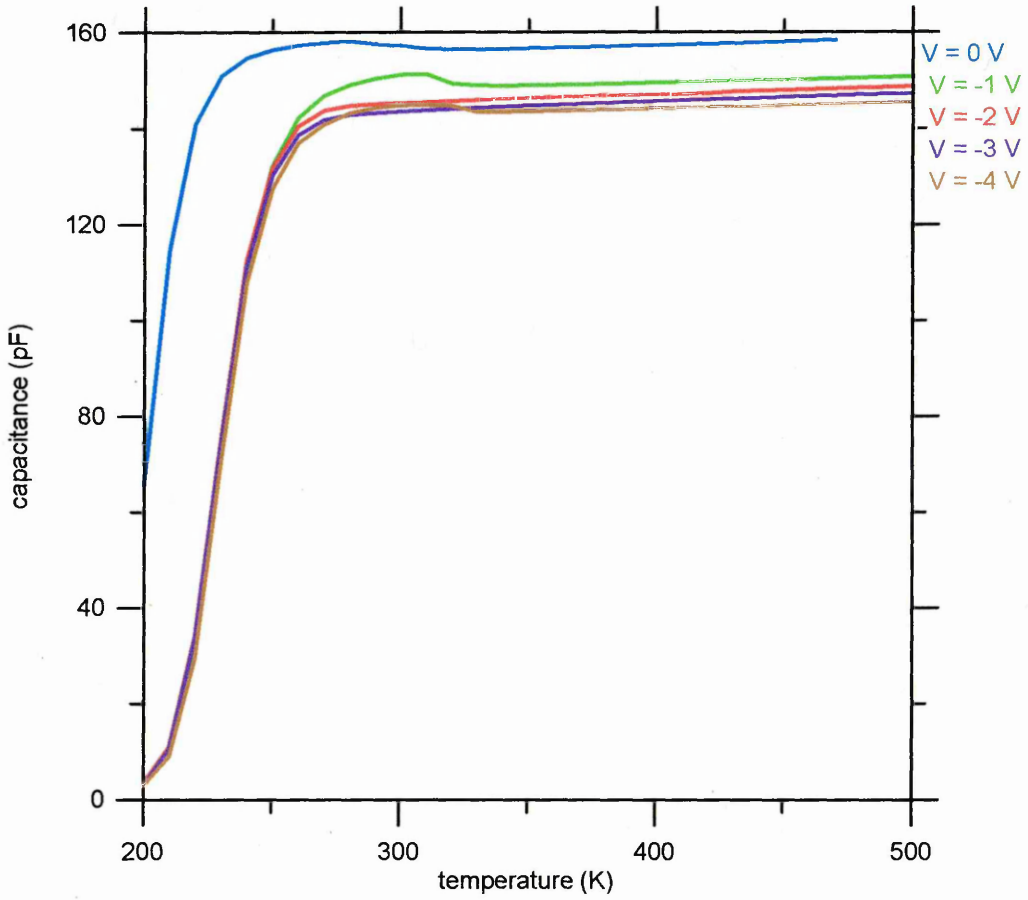

Figure 8-22 Capacitance versus temperature for high boron doping at different bias voltages, V= 0, -1, -2, -3 and -4V.

From figure 8-22 the voltage at which to measure DLTS and LDLTS was determined as between 0 and - 4V. The capacitance starts to level off at about 220 - 250 K for all the bias voltages applied implying that holes have started to be emitted to the valence band by 250 K. From I-V measurements and other considerations, we know that only 0.2 % ionisation occurs at 300K [Thonke, 2003]. The capacitance decreases as the reverse bias is increased, which means that the depletion region is increasing with applied voltage and the geometric capacitance has been reached.

There are other relevant parameters besides the phase angle, the capacitance, the carrier concentration and the depletion region width; these include the ideality factor, the series resistance and the BH of the diamond Schottky diode, as mentioned earlier.

8.4 Depletion region width (w)

To check whether the parameters extrapolated from experimental C-V data are valid, it is advisable to determine the depletion region by a second method. It is possible to calculate the depletion region theoretically. The depletion region width found using C-V data was 2.81×10^{-6} m at nearly zero bias, see figure 8-16. This result is compared with calculations based upon resistance measurements with a four point probe technique to measure the resistivity of the sample.

Conductivity, $\sigma = q(n\mu_n + p\mu_p)$ 8.12

For p-type semiconductor $\sigma = qp\mu_p$ 8.13

Conductivity, $\sigma = 1/\rho$ 8.14

where ρ is the resistivity of the diamond, p is the hole concentration and μ_p is the hole mobility.

the probe spacings were chosen so that equation 8.5 [Schroder199],

$$\rho = F\left(\frac{V}{I}\right) = 4.53\left(\frac{V}{I}\right) \quad 8.15$$

F is the correction factor $(\pi / ln2) = 4.53$ from Sze [1981], and is a constant for the material.

From the four point probe measurements at room temperature, the average voltage, measured from the diamond samples was 29.7×10^{-3} V, and the average current was 80×10^{-6} A.

Therefore, $\rho = 4.539(V/I) = 4.53(29.7\times 10^{-3} / 80\times10^{-6}) = 1682\ \Omega/\square$.

The carrier concentration is $p = 1/q\rho\mu_p = 8 \times 10^{14}$ cm^{-3}, from the C-V measurements. Therefore the mobility of holes (μ_P) is calculated to be = 46.5×10^{-2} cm^2/Vs at 300 K. The mobility figure is so low because the material is polycrystalline.

$$\text{The depletion region } w = \left[\frac{2\varepsilon V_{bi}}{qp}\right]^{1/2} \qquad 8.16$$

where V_{bi} is the built in voltage and given by $V_{bi} = \varphi_m - \varphi_s$, 8.17

φ_m is the work function of the aluminium = 4.1 eV,

φ_s is the work function of diamond semiconductor = 4.8 eV, and

$\varepsilon = \varepsilon_o \varepsilon_r$, ε_o is the permittivity of vacuum = 8.85×10^{-14} Fcm^{-1} and ε_r is the relative permittivity of diamond = 5.7.

Hence $V_{bi} = 4.1 - 4.8 = -0.7$ V, although this is a very simplistic approach and probably gives rise to an error in V_{bi}.

By substitution in equation 8.16

$$w = 2.37 \times 10^{-6} \text{ m}$$

From these calculations, the depletion region width is 2.37×10^{-6} m. The experimental results suggest the depletion region is 2.81×10^{-6} m in the low boron sample. The two results are in very good agreement, so the measurements of I-V, C-V may be taken as correct.

Figure 8-4 and 8-5 show that the current in forward bias starts increasing rapidly at about 1.8 volt, but in reverse bias the reverse current is only small, though increasing with increasing voltage until breakdown. Because the resistance of the diamond is very high, the forward current is quite small ($< 10^{-5}$A), but the reverse current is a non-negligible.

The phase angle approaches the ideal value (90°), and is between 86° to 89° for all the fabricated diamond Schottky diodes. Because of the resistance of the diamond, the depletion region (w) is very large, which makes the change of the capacitance over few

volts very small, as seen in figure 8-13. The implication of this is that a change of capacitance which is caused by trap filling and emptying, as in DLTS, might be too small to measure.

The sample works as a capacitor with resistors in series and parallel. Thus the current will lead the voltage by some phase angle as shown in figure 8-23. Ideally, if infinite resistance is present, and hence the current through the resistance is zero, the lead angle is 90°. But the actual value of 86° indicates that a real, non-zero parallel resistance (R_d) is present.

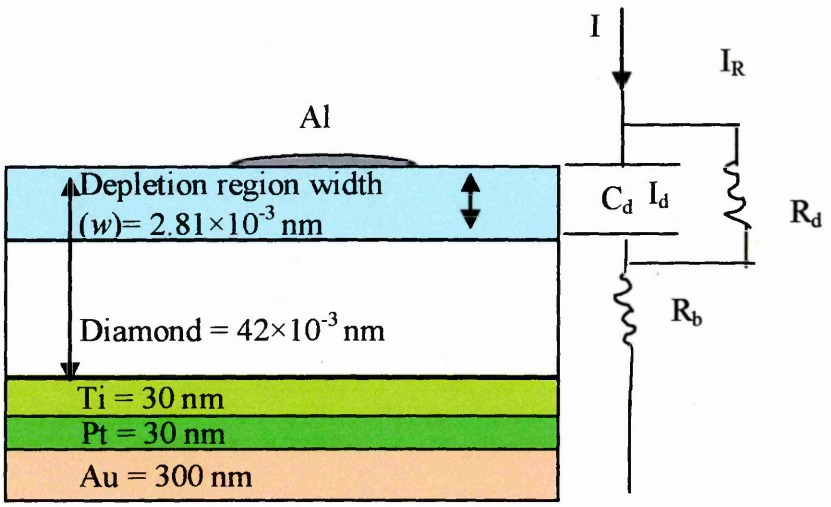

Figure 8-23 Structure of diode and equivalent circuit of the sample.

Figure 8-23 shows the structure of the bulk of the diode and the depletion region. On the right is shown the equivalent circuit relating to the device structure. Figure 8-23 also shows R_d and R_b, the resistances of the depletion region and the diamond bulk respectively. Figure 8-24 shows I_d and I_R, representing the current flow through capacitor and the resistor (diamond bulk) respectively, I is the total current through the diamond device.

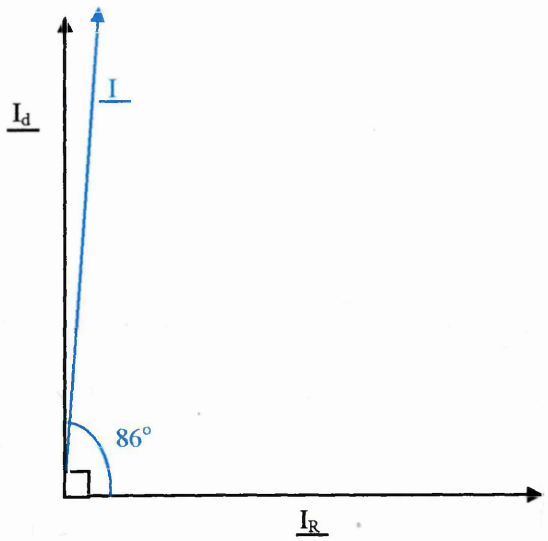

Figure 8-24 Vectorial representation of current flows in the capacitor and resistor in series connection.

It was noted that the value of this difference between I_R and I_d increased with increasing applied voltage where I_d, I_R and I are vectors. The thickness of the depletion region obtained the C-V measurements was determined at zero voltage as ~ 2.81×10^{-6} m. The thickness of the diamond sample measured using an optical microscope was 42 x 10^{-6} m.

However, these experiments show that it is possible to manipulate the edge of the depletion region of semiconducting diamond in these samples by changing the reverse bias applied to a Schottky diode, and extract the series resistance (and resistivity) from the phase diagram. It is assumed that the series resistance dominates, as the depletion region is found to be only 6 % of the layer thickness. The phase angle would be adequate for capacitance DLTS measurements but leakage currents are relatively high. We attribute this to leakage along grain boundaries in the samples.

8.5 DLTS characteristics

The particular DLTS measurement system used in this work was the Bio-Rad system DL 4600. This system was developed in the Solid State Electronics Group of the Department of Electrical Engineering and Electronics at UMIST (Manchester). Figure 8-25 shows a block diagram of the system, which consists of a DLTS controlled capacitance measurement, computerised temperature control, and variable temperature cryostat.

The DLTS system contains a biasing circuit for applying a reverse bias, a bias pulse generator, and a temperature controller. The pulse generator emits various excitation pulses for the different modes of operation. By adjusting the width of the fill pulses, rate windows from 0.8 per second to 5000 per second can be selected. Two simultaneous rate window settings (represented by the A and B outputs) are allowed by the triple pulse system. The temperature of the sample is controlled by the computer program or manually by a dial on the front panel of the controller. Both the heating element and the flow of liquid nitrogen (using a pump) are governed by the control unit. The temperature can be varied at a constant rate which is changeable from $0.1Ks^{-1}$ to $0.9Ks^{-1}$. The true values of sample capacitance are recorded during the measurements by adjusting the zero to compensate for the capacitance of the cryostat and leads. This also enables the observation of very small values of ΔC, by subtracting out all the background capacitance.

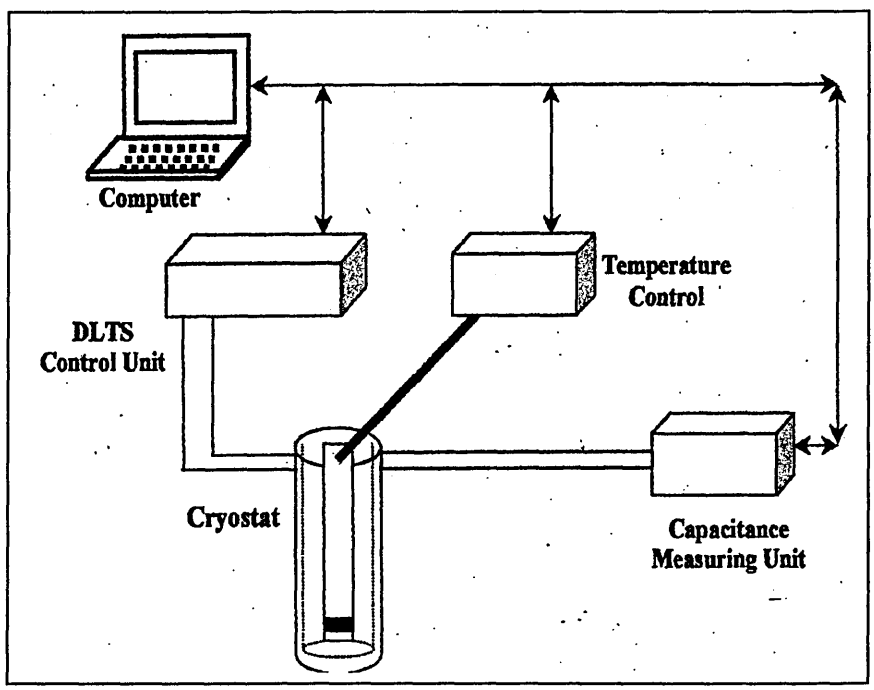

Figure 8-25 Diagram of conventional DLTS measurement system.

A cryostat forms the third part of the system, of the continuous liquid nitrogen flow type, and is used to vary the temperature of the sample. The sample is heated using an integral heater and its temperature is measured by a platinum resistance thermometer. The temperature range used was from 80 to 450 K. The PC is also used to store the measured data and determine the various parameters.

For LDLTS measurements, a chosen closed cycle cryostat system is used. The Trap-View computer program developed at UMIST was used to run the DLTS system for Si. The reverse bias was between -1 to -5 V, the fill pulse was typically 1 ms in length, and the capacitance range was from 3 to 30 pF depending on the sample, i.e., a sample with a high carrier concentration ($>10^{16}$ cm^{-3}) requires a high capacitance range; a sample with the low carrier concentration needs a small capacitance range. Since closed cycle refrigeration is employed, the temperature can go down to 80 K, and it was routinely scanned between 300-80 K. The temperature consistency was checked by reversing the temperature ramp to examine for any hysteresis.

Capture cross section measurements were carried out on the liquid nitrogen DLTS system, that is, a system with a box-car integrator for signal processing which was connected to an oscilloscope. The capacitance meter chosen was the Boonton 72 B, with a boxcar (as indicated above) and integrator for signal processing. Capture cross-sections were measured by keeping the reverse bias voltage fixed i.e., 1.5 V and fixed rate window i.e., 200/s respectively, while varying fill pulses from 10 ms to 10 ns. A specially designed fast interface was used to ensure that even the shortest pulses remained square.

For depth profiling, the bias voltage was changed and the DLTS signal values were recorded whilst other parameters were held constant: the temperature, the fill pulse (1 ms) and rate window (200/s). Forward bias injection was not attempted during these measurements. The temperature ramp was reversed so that the temperature consistency could be justified.

Concentration versus depth profiles were found by selecting one of eight rate windows and holding the temperature constant within ± 0.5 K at the maximum of the chosen DLTS peak. The steady-state reverse bias voltage was kept constant while the amplitude of the majority-carrier pulse was gradually increased. It was then possible to extract the depth profiles from the pulse-amplitude dependence of the DLTS signal, where the voltage-to depth calculations were carried out by the conventional square-root dependence for a Schottky barrier junction.

As mentioned, DLTS is a very sensitive technique for detecting deep levels in semiconductor materials and to study very high resistivity materials. The fourteen Schottky diodes on boron-doped diamond films were tested using DLTS in an attempt to characterise any electrically active defects. Charge flowing during the fill pulse will be stored in any available defects in the diamond structure. If the diamond was perfect (although minor imperfections will always exist in practice), and any devices fabricated on it were also perfect, the DLTS output would have no signal, and be a straight line with zero output.

The C-V measurements showed a very small change in the capacitance (from ≈ 29.6 pF to 31.6 pF, when the voltage was changed between 0V to 10V) as illustrated in figure 8-13. DLTS was carried out on all fourteen Schottky diodes, but plotted here is only the data for the diode with the lower level of boron doping. The rate windows from 4/s to 10,000/s were sampled, the applied voltage varied from -5 to 0 V, the pulse length from 10 ns to 20s, the fill pulse voltage between + 10 to -1 V, and the range of ΔC from 3 pF to 1000 pF. Figures 8-26, 8-27, 8-28 and 8-29 indicate that we could not detect any defects using DLTS. The same types of figures were found for all voltages, ΔC, pulses bias and rate windows. All the parameters were changed many times and the measurements carried out in more than 300 attempts to find any peaks, but the results were always the same. A noisy line was recorded with no perceived signal, this means no peaks for impurities or defects are apparent for the sample doped diamond. It was decided to use the LDLTS measurement system to see what would be found.

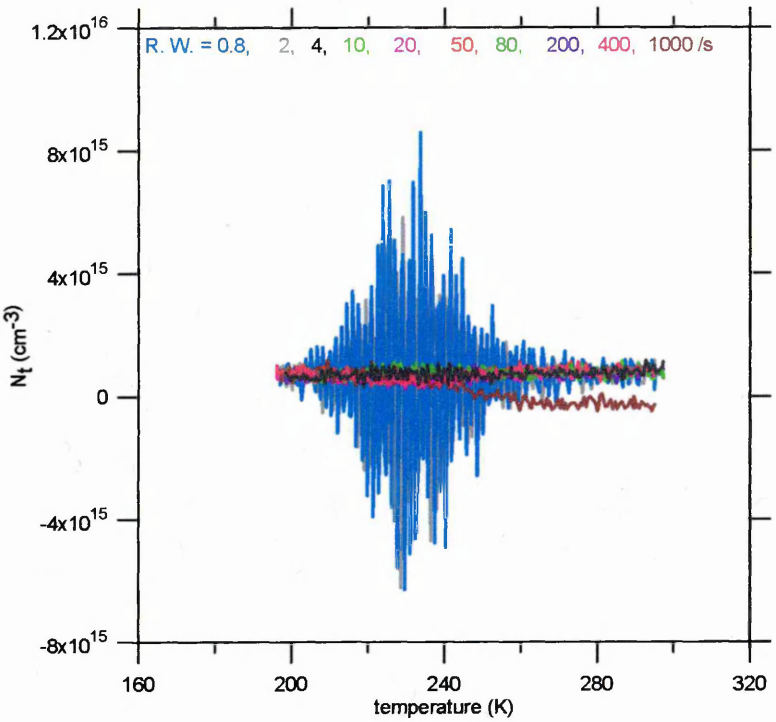

Figure 8-26 DLTS measurement when V = -1.5V, high boron doped diamond.

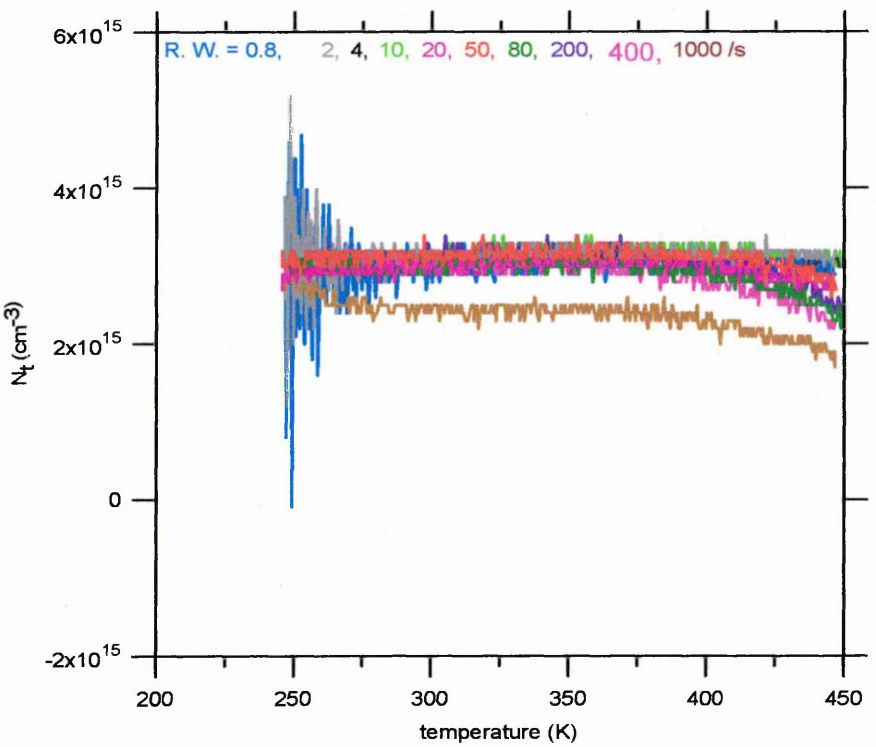

Figure 8-27 DLTS measurement of high boron doped diamond.

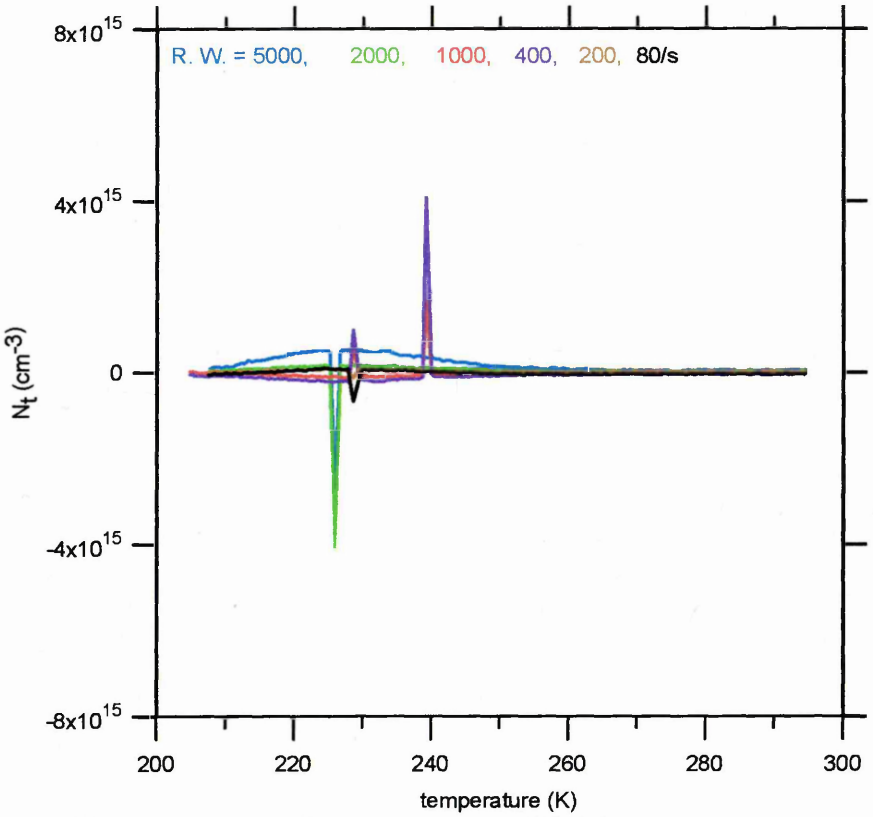

Figure 8-28 DLTS measurement of high boron doped diamond.

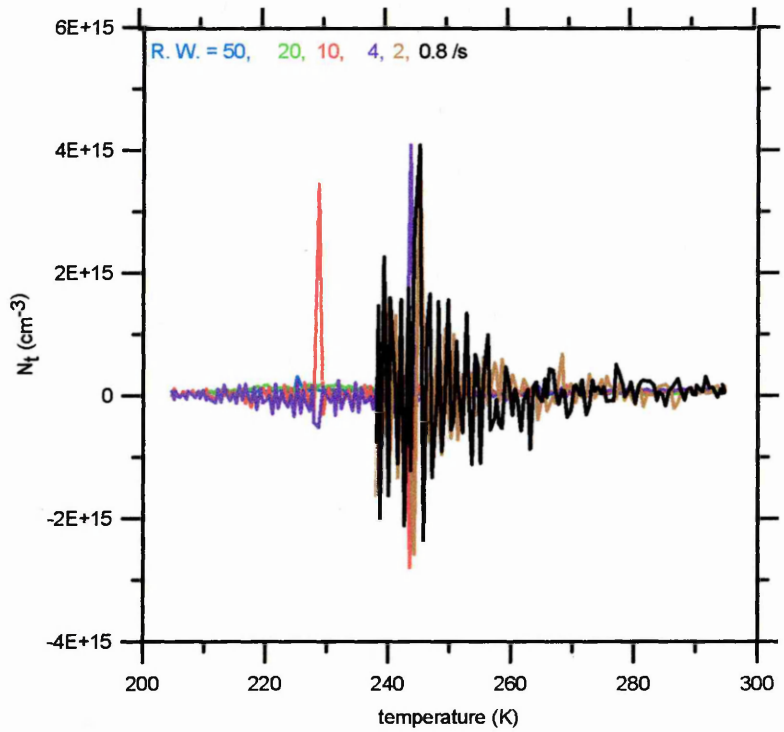

Figure 8-29 DLTS measurement of high boron doped diamond.

To make sure that the experimental arrangement is capable of detecting traps in a sample, DLTS was also carried out on p-type silicon Schottky diodes and p-type silicon-germanium Schottky diodes. The results gave good peaks depending on the

defects or impurities in the material. Those peaks were an indication that the equipment and its setup were capable of detecting peaks related to the presence of traps in the sample both in silicon, which is not shown here, and the silicon-germanium which will be shown later in Chapter 9.

8.6 Laplace DLTS characteristics

Despite the fact that the conventional DLTS technique has facilitated the development of major advances in the understanding of the electronic levels in semiconductors, the ability of this technique to resolve closely spaced energy levels is very poor. It produces a broad peak even for "perfect" defects which do not have complicating factors. Variation of the time constant in defect emission will lead to further broadening of the peak, so time constants must be well separated to reveal any fine structure of the defect. LDLTS [Dobaczewski *et al,* 1994] gives good resolution and can reveal the fine structure of defects. In LDLTS, computation based on a regularisation technique produces a plot of the spectral density as a function of emission rate rather than time filtered capacitance charge versus temperature.

LDLTS was used in this work as an alternative to DLTS as it is more sensitive. The sample is allowed to reach equilibrium at the chosen temperature and then the capacitance transient is sampled. The technique allows 1 - 30000 scans to be performed, each comprising 10 to 30000 samples taken at rates between 10 Hz and 100 kHz. Once the transient has been captured, preliminary analysis of the transient can be carried out using either a simple one-exponential fitting or a multi-exponential fitting using a statistical approach. These fits are regulated by the user's choice over the length of transient to be examined. More detailed analysis, used in the characterization of the material, involves calculating the inverse transform spectrum using one of a number of regularisation techniques. With this carefully designed system and transient averaging, it is possible to resolve the time constant for a transient with a signal to noise ratio of ~ 1000:1 [Evans-Freeman *et al*, 2000]. This implies that the concentration of defects must lie between 1 and 10 % of the shallow doping level for LDLTS to give sensible data.

A plot of peak intensity as a function of emission rate is produced. If the transient is truly exponential, only one peak is visible in the LDLTS spectrum. The area under each sharp peak is proportional to the trap concentration. There is no temperature

hysteresis as each data point is obtained at a fixed temperature in a high stability cryostat. Therefore data points as close as 1K apart can be obtained.

Diodes on diamond with three different boron concentrations have been used for LDLTS. LDLTS was carried out at temperatures from 100 K to 500 K and at 5K intervals. Intervals of 1 K were used if peaks were detected in a region (e. g 240-250 K in highly doped diamond).

The peaks in figure 8-30 (offset for the sake of clarity), of diamond with a high concentration of boron do not correspond to defects in the crystals because they did not move when the temperature changed. The emission rate should increase as the temperature increases. However, careful inspection showed the emission rate at a rate window of 1000/s did not change with temperature indicating that it is not due to a defect, but is caused by electronic noise; therefore this was neglected. This implies that the peaks were not introduced by defects in the diode, but the cause is not yet known. During LDLTS measurements, there is no saturation interval in the fill pulse-ΔC curve, not shown here, was observed. In order to deeply investigate that behaviour, the sampling rate was altered a number of times. Again the curve did not reached saturation. The transient never saturated even when the samples rate slow transient was not seen, as explained in Section 6.4. This means that an alternative approach should be used to determine the defects in boron doped diamond.

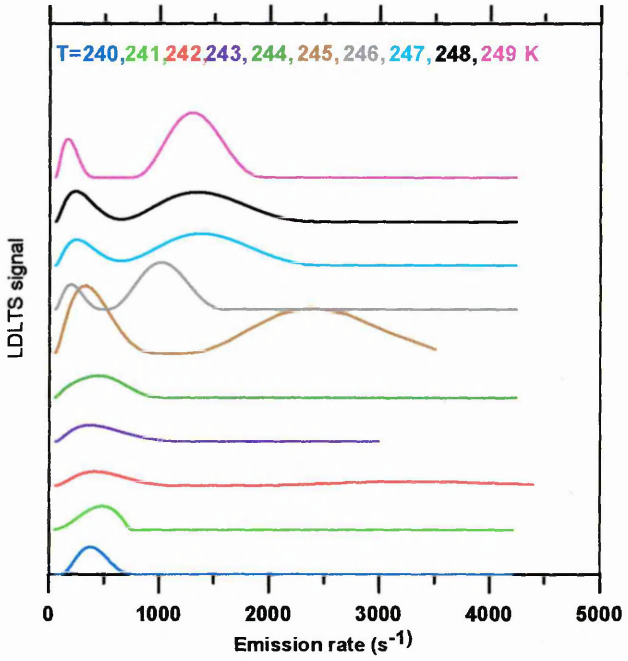

Figure 8-30 Peaks in LDLTS at different temperatures versus emission rate, of diamond with a high concentration of boron.

8.7 Scanning electron microscopy

As the DLTS and LDLTS failed to show any deep electronic states other than the boron in the diamond Schottky diodes, SEM was used to study the crystal structure of the diamond and also the interfaces between the deposited and evaporated metals and the diamond. In this section we are going to show and analyse the SEM images of the less heavily boron-doped sample. This is a polycrystalline diamond film grown by CVD technique on a non-lattice-matched substrate (almost certainly silicon), which was subsequently removed by the growers.

The composite secondary electron image (SEI) of the diamond film in cross-section is shown in figure 8-31 and was taken with an accelerating voltage of 8 kV. The original substrate-film interface is at the bottom of the figure, and the growth direction is vertically upwards. A few non-conducting dust particles were present on the surface of the specimen, as indicated. A large number of very small nuclei are seen at the original substrate-film interface (there was no attempt to achieve epitaxial growth of this sample), but within 7 ± 2 μm preferential growth of grains with a favourable orientation has caused the structure to evolve to contain fewer, larger columnar grains.

Figure 8-31 Secondary electron images of a cross-section of a polycrystalline diamond film, illustrating the columnar nature of the grains.

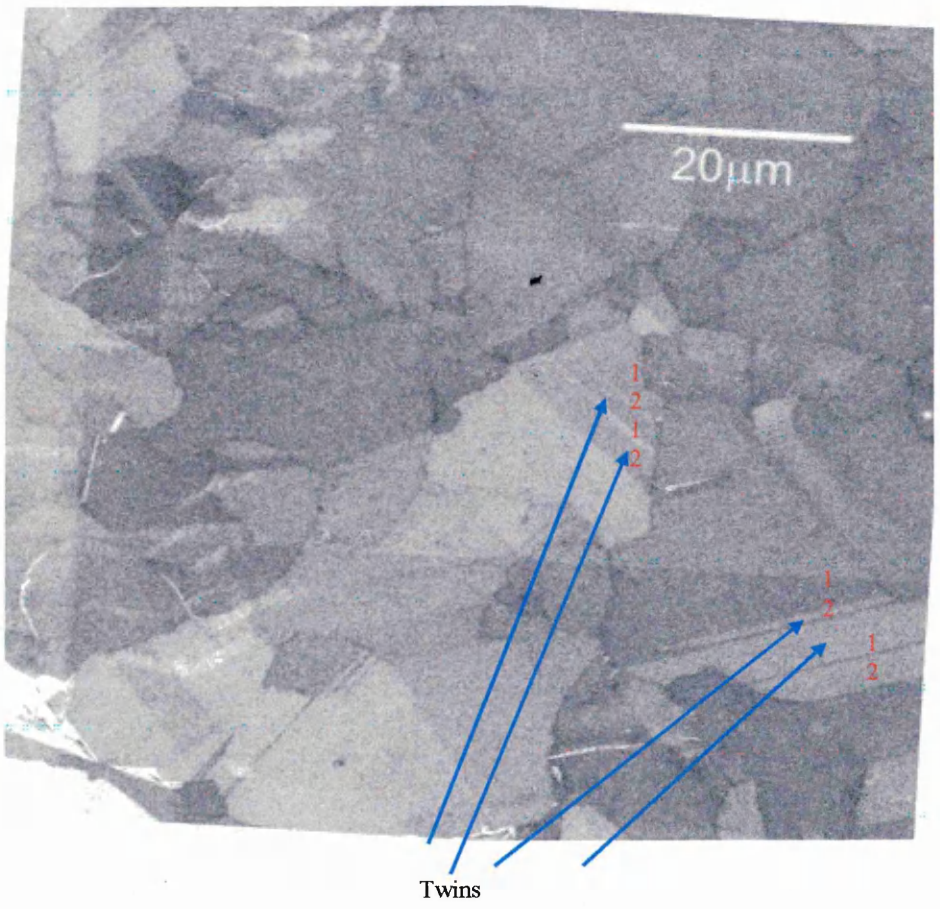

Figure 8-32 Secondary electron image of the top surface of the polycrystalline diamond film.

Figure 8-32 is a secondary electron image (SEI) of the top surface of the diamond film taken with an accelerating voltage of 8 kV. Twinning is apparent in many of the grains, which are relatively equiaxed in this plane. The grain size in the film at the surface is 11.2 ± 1.7 μm (with 95% confidence). The high degree of crystallinity in the film at this point in its growth is readily apparent from the detail visible in the micrograph of the as-received surface.

Figure 8-33 is a SEI of the specimen tilted to 45° to enable examination of both the original substrate-film interface and the edge of the film. The roughness of both the substrate-film interface and the edge of the film are exaggerated by the tilt.

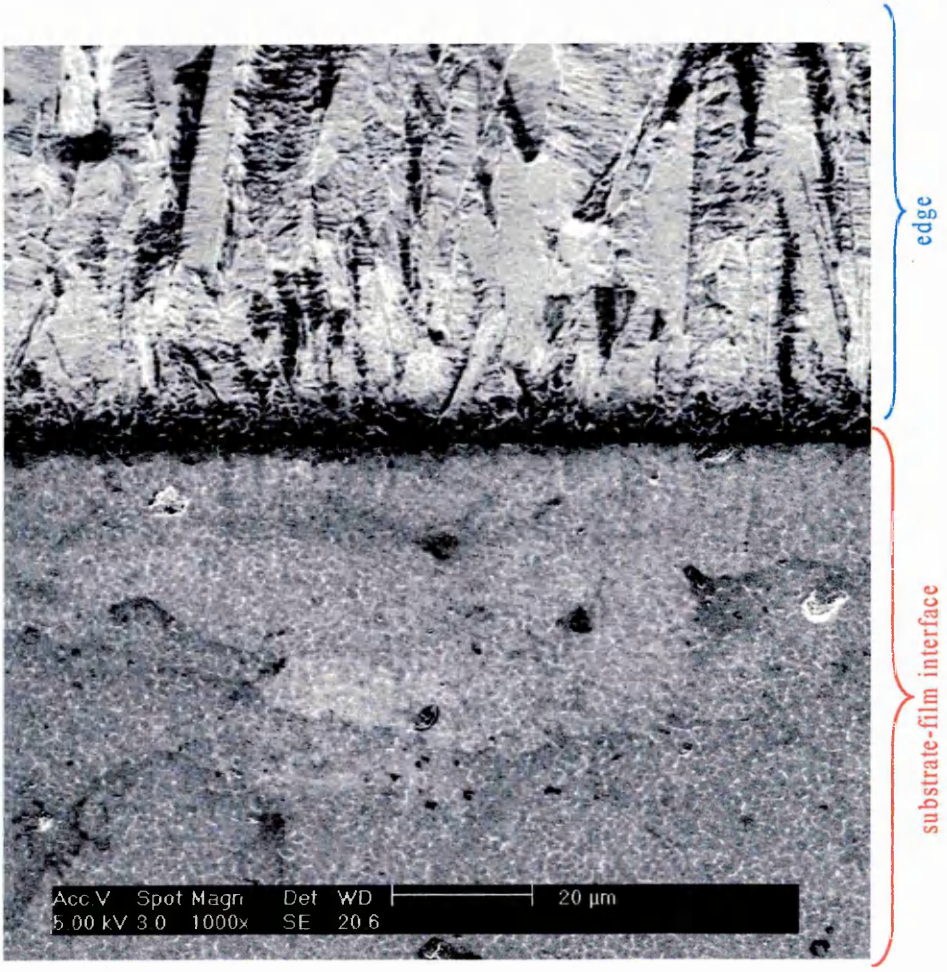

Figure 8-33 Secondary electron image of specimen tilted to show both original substrate-film interface and edge of film.

Figure 8-34 is a SEI of the original substrate-film interface without tilt. It is evident that the crystallinity of the initial monolayer of the diamond film is not well-developed.

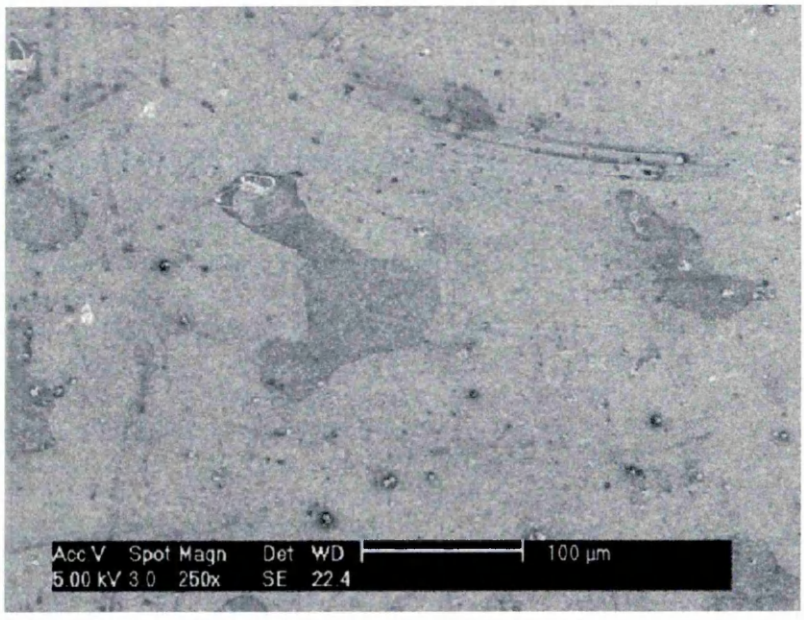

Figure 8-34 Secondary electron image of original substrate interface.

It is generally assumed that diamond nucleation is a result of the suppression of graphite nucleus formation and a simultaneous stabilization of the diamond surface and diamond nuclei by forming sp^3 carbon hydrogen surface bonds. For the usual low-pressure diamond synthesis, a preferential etching of sp^2 carbon by atomic hydrogen is also assumed [Pehrsson *et al*, 1993]. It is known that diamond nucleation is strongly influenced by the chemical nature of the substrate [Haubner, and Lux, 1994; Lux, and Haubner, 1991], due to chemical and physical interactions between the substrate material and reaction gases. Much effort is still being put into research for a better understanding and a better control of diamond nucleation [Demuynck *et al*, 1997; Maillard-Schalter *et al*, 1997; Thurer *et al*, 1996; Kalss *et al*, 1998].

The results of the SEM investigation of the microstructure of the less heavily boron-doped film agree well with the current understanding of the nucleation and growth of diamond by Liquid Phase Epitaxy (LPE). The substrate-film interface shows many small grains with relatively poor crystallinity. Preferential growth of those nuclei oriented with a fast growth directed perpendicular (or nearly perpendicular) to the surface rapidly reduces the number of grains in the film, with a concomitant increase in grain size and also crystallinity. Growth twins are well documented in diamond [Chepurov *et al*, 2000], and their existence in the microstructure is to be expected.

The film was also examined by SEM after the oxygen plasma treatment necessary to passivate surface states for satisfactory electrical contacts. It proved no longer possible to see any surface microstructure, and both upper and lower faces appeared identical in the secondary electron image.

8.8 Discussion

I-V results: some leakage current is observed but not from surface conduction, this was proved by fabricating fourteen diodes with three different levels of doping (four diodes for each of two levels of doping, and six for the third). Schottky diodes were made on both sides of the diamond layer, to test for surface leakage, but no current was detected in that case at all. It is deduced that the current observed from the Schottky-Ohmic combination is therefore due to that flowing through the semiconducting diamond probably down grain boundaries.

LDLTS results: early results suggest that there is a very slow component to the capacitance transient after the fill pulse. It is not uniform, and it would appear that there is a deep reservoir of charge emptying into the valence band very slowly. Postulating that this could be due to electrically active grain boundaries discharging. Further work investigating this phenomenon as a function of fill conditions is under way.

Capacitance measurements have been performed on the diode to establish their suitability for DLTS and LDLTS techniques. Preliminary measurements were carried out on the phase angle as a function of measurement frequency. The best results for the phase angle (the nearest experimental value to the ideal 90°, was 86°) for all diamond Schottky diodes were obtained for a measurement frequency of 1 MHz, and room temperature.

8.9 Summary

The results obtained in this work show that Ohmic contacts can be fabricated on semiconducting diamond by sputtering layers of titanium, platinum and gold. Schottky diodes can be made by evaporating aluminium through holes in a flat metal mask on to the surface.

I-V measurements confirm that the diode had acceptable current-voltage characteristics. C-V measurements show that the phase angle between capacitance and

voltage is acceptably close to 90^0 for temperatures greater than 300K and frequencies above 200 kHz.

Experimental measurements found the width of the depletion region to be 2.81×10^{-6} m. The calculations based on conductivity measurements gave a width of 2.73×10^{-6} m. It is considered that these two results are in acceptable agreement.

SEM confirmed the high density of grain boundaries and twins are located in diamond. Because there are no determinable electronic defect states in the diamond samples tested, future work will be with single crystal diamond doped with boron to avoid the effects of grain boundaries.

A preliminary study of the electrical quality of Schottky diodes on boron doped CVD diamond has been presented. It has been shown that the depletion region width can be varied using the applied voltage even in a thin sample. Moreover, it has been shown that the phase angle would be sufficient for capacitance DLTS to be carried out. The phase angle as a function of voltage is consistent with a slightly varying series resistance as the depletion region increases. This is analogous to similar tests carried out on silicon. This work paves the way for a high temperature study by DLTS of deep levels in the material.

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Chapter 9

Silicon germanium Schottky diode

9.1 Introduction

Silicon devices dominate the microelectronics industry. They account for more than 98% of sales in the global semiconductor market because of their low manufacturing cost. However, the driving force behind today's growth in high-speed optical networking and inexpensive lightweight personal communications devices is not silicon but silicon-germanium. This technology increases operating speed, reduces electronic noise, lowers power consumption, supports higher levels of integration, and thus enables the design of more functional components on a chip [Quellette, 2002].

If germanium is added to silicon, the larger germanium atoms interact with the smaller silicon atoms to form the compound SiGe. Inter-atomic tensions within the layer generally drastically increase charge carrier mobility and hence improve the conductivity of the SiGe compound. SiGe offers semiconductor technology a whole string of advantages: the germanium in the SiGe improves silicon conductivity and makes devices containing SiGe faster. Alternatively, the SiGe can be used to strain certain regions of Si (e.g. the channel in MOSFET) also leading to higher mobilities. The result is increased performance with lower power consumption. Because silicon and germanium are chemically similar, high performance silicon-germanium devices can be fabricated at fairly low cost making it an attractive semiconductor material. Thanks to these advantages and a relatively modest technology investment, SiGe has given rise to further generations of integrated circuits to keep pace with rising industry and consumer demands.

There are various physical reasons why SiGe devices cannot be fabricated directly onto a silicon wafer, such as lattice mismatch which may lead to a massive dislocation density, and poor crystal integrity. A typical solution is to somehow convert the silicon wafer to a SiGe wafer. The added SiGe top layer must not disturb the perfect monocrystalline structure of the silicon below, so there are various intervening SiGe buffer layers to ease the transition. The finished SiGe wafer with its silicon base, buffer layers and SiGe cap is known as a virtual substrate.

There is a 4.2 % difference in the lattice constants of silicon and germanium, and so if one is to be grown on the other the layer is strained and must be grown below the critical thickness, defined in Section 9.4. This strain may be used to vary the band gap energy, band discontinuities, effective masses, and a substantially higher mobility than unstrained silicon material is the result. Hence silicon-germanium devices can have substantially faster performance than conventional silicon transistors while being produced on lightly modified silicon production lines [Quellette, 2002].

The aim of this work was to fabricate SiGe Schottky diodes on virtual substrates provided by Atmel in Newcastle, and to study the defects in these diodes. A comparison was made of the phase angle, capacitance, and depletion region width as a function of applied voltage, between the diamond diodes in the previous chapters and the SiGe Schottky diode. The experimental results from seven samples with more than forty SiGe Schottky diodes will be presented.

The Schottky diode under investigation is a p-doped SiGe virtual substrate. Ti-Al was sputtered to create the Schottky barrier. On the rear, Al was evaporated to create the Ohmic contact. The epitaxial profile and layer composition were presented earlier in Section 6.7. First, a review of the properties of strained SiGe on Si is presented.

9.2 Structural properties of $Si_{1-x}Ge_x$/Si layers

Silicon and germanium have the same crystal structure as diamond, and show complete solid solubility in each other. The maximum lattice misfit of 4.2 % between silicon and germanium is due to the difference between the lattice parameters of silicon (5.431 Å) and germanium (5.658 Å). If the thickness of the SiGe alloy is kept below the critical thickness [Matthews, 1975], then the epitaxially grown SiGe on Si will be a strained epilayer. The strain produced causes an extra change in the band structure

which is useful for several device applications. This strain can be relaxed by the introduction of misfit dislocation if the heterostructure epilayers are annealed at high temperature, or if the thickness of $Si_{1-x}Ge_x$ layer exceeds this critical thickness.

9.3 Lattice misfit parameter

The lattice parameter of $Si_{1-x}Ge_x$ alloys in the compositional range ($0<x<1$) varies linearly with germanium content according to Vegard's law as

$$a_{alloy} = a_A + a_B \qquad 9.1$$

where alloy is a $Si_{(1-x)}Ge_{(x)}$, A is $Si_{(1-x)}$, B is $Ge_{(x)}$, a_{SiGe}, a_{Si}, and a_{Ge} are the lattice constants of $Si_{1-x}Ge_x$, Si, Ge respectively, where x is the mole fraction. It is obvious that the lattice parameter of the $Si_{1-x}Ge_x$ alloy is greater than the lattice parameter of silicon. Hence, growing a $Si_{1-x}Ge_x$ alloy on a silicon substrate will be associated with a lattice misfit. The value of the misfit parameter associated with a $Si_{1-x}Ge_x$ alloy layer and substrates is defined as [Jain and Hayas, 1991]

$$\xi(x) = (a_{SiGe} - a_{Si})/\, a_{Si} \approx (a_{Ge} - a_{Si})/\, a_{Si} \approx 0.042x$$

9.4 Critical layer thickness (h_c)

When $Si_{1-x}Ge_x$ alloys are grown on silicon substrates, the first atomic layers which are deposited will be strained by the formation of a coherent interface when the in-plane lattice constant of the film matches the silicon lattice parameter. When the thickness of the film exceeds a critical value, strain relaxation will occur by formation of misfit dislocations. So, the critical thickness h_c is the thickness below which a good quality layer or superlattice can be grown without the introduction of misfit dislocations. Van der Merwe [1972], first showed that defects could be avoided in growth of $Si_{0.7}$-$Ge_{0.3}$ films on silicon when the thickness was in the order of 10-100Å. In our sample the germanium was introduced gradually in order not to cause a sudden major strain in structure, the shape of the sample structure is shown in figure 6.5 Chapter 6. The structure is based on having a virtual substrate for growing a device on top of it as the composition varies from x = 0 to x = 30 % over a thickness of 3000 nm.

If a top layer of $Si_{0.7}$ $Ge_{0.3}$ is grown on a graded substrate of $Si_{1-x}Ge_x$ where the grading is x = 0 to x = 30%, there will not be any strain introduced in the top layer. If

one tried to grow $Si_{0.7}$ $Ge_{0.3}$ on top of pure silicon one would be limited by the critical thickness of 22 nm, shown in the following calculation [Theodorou *et al*, 1994, Wolfgang *et al*, 1998].

$$a_{alloy} = x\, a_A + (1-x)\, a_B \qquad 9.2$$

where $a_{(Si1-xGex)}$ is the misfit lattice constant, a_{Si} is, the Si lattice constant and a_{Ge} is the Ge lattice constant.

In order to find the critical thickness, we define the misfit ξ as

$$\xi = [a_{alloy} - a_A]/a_A \qquad 9.3$$

and the critical thickness h_c is defined as

$$h_c = a_A / 2\,\xi \qquad 9.4$$

performing this calculation for 30 % Ge leads to h_c = 22 nm.

The critical thicknesses necessary for different concentrations of germanium up to 30 % are shown in figure 9-1.

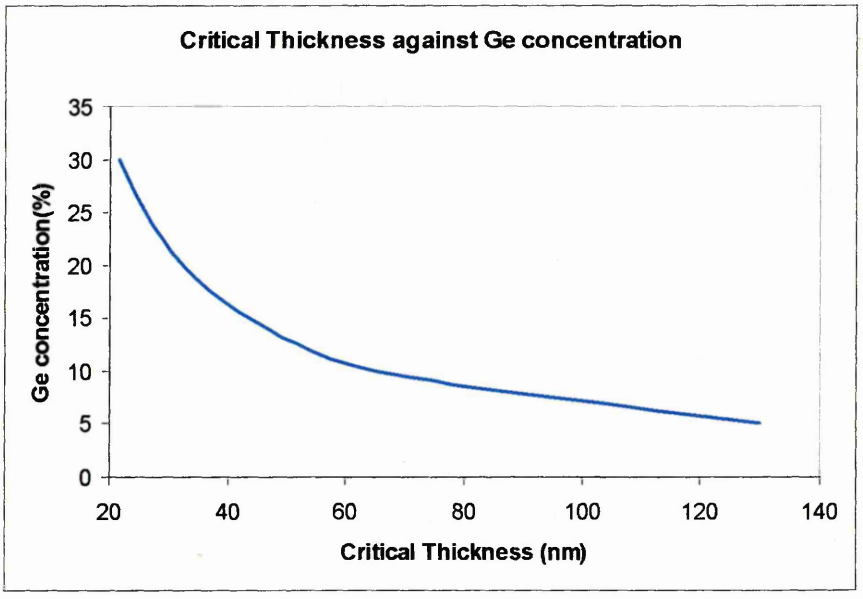

Figure 9-1 Critical thickness (h_c) as a function of germanium concentration in the $Si_{1-x}Ge_x$ layer.

9.5 Experimental results

Seven samples with a total number of forty SiGe Schottky diodes have been investigated. In order to characterise the fabricated Schottky diodes I-V and C-V measurements were carried out. As the presence of defects in a diode is an important measure of its ideality, DLTS and LDLTS measurements were carried out on all the diodes. It should be noted that all the samples were of the same structure, also the same procedures were used to fabricate Schottky diodes. We have chosen the best sample of those seven samples and all the characterisation experiments were carried out on that sample.

9.5.1 Current-voltage measurements

An I-V measurement is a powerful tool with which to electrically characterise a diode. The I-V measurement is needed to study the rectification of the diode under test and to make sure that the diode has the rectification necessary for the DLTS experiment. Additionally, the reverse leakage current can be investigated using the I-V currents. The I-V plots of the diodes were made using a Hewlett-Packard Programmable meter-voltage source (hp 4140B PA Meter/DC voltage source).

All the I-V measurements of the samples were acomplished at room temperature with voltage biased from -15 to 5 volts. The fabricated diodes were placed on the holder and were fixed by a sprung gold pin for good contact. In this system, the reverse bias connection was checked before the I-V measurements were made. Figure 9-2 shows the I-V curve for one of the fabricated SiGe Schottky diodes. The window in figure 9-2 shows the reverse bias region in more detail. It can be seen from the I-V curve that the built in voltage is nearly 0.3 V which indicates a small Schottky barrier height in the forward bias region. Also, a study of the higher resolution curve shows a reverse current of about 5.5×10^{-7} A at reverses bias voltage of more than -10 V and this value increases with increasing reverse voltage. It is clear that the diode presents only a small leakage current which is an indication of a good Schottky diode.

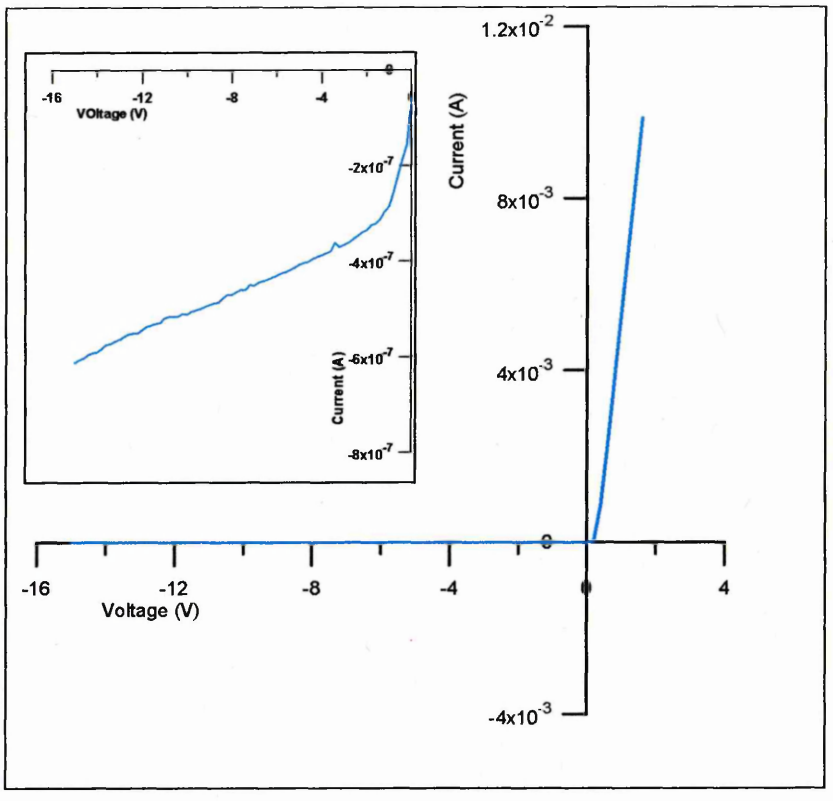

Figure 9-2 I-V curve at room temperature of a Schottky diode on Si_{1-x} Ge_x grown on a virtual substrate, inset shows the reverse bias region in more detail. The diode shown is the least leaky of all the tested samples.

9.5.2 Capacitance-voltage measurements

The C-V characteristic of a Schottky diode is also a key factor in its characterisation. C-V measurements are based on the depletion region properties. The capacitance profiling of a diode is very important in determining whether the DLTS experiment should be carried out or not. The C-V measurements on all samples were undertaken at room temperature with reverse bias voltage from -10 to zero volts using a programmable Hewlett-Packard LCR meter. A computer program was used to plot the C-V curve, for each diode under test. Information about the phase angle and its variation with the applied bias voltage can be also monitored during the capacitance profiling experiment.

Figure 9-3 illustrates the change of capacitance and phase angle with applied reverse bias. The latter determines whether the diode has a high resistance or not (90° phase angle indicates an ideal diode).

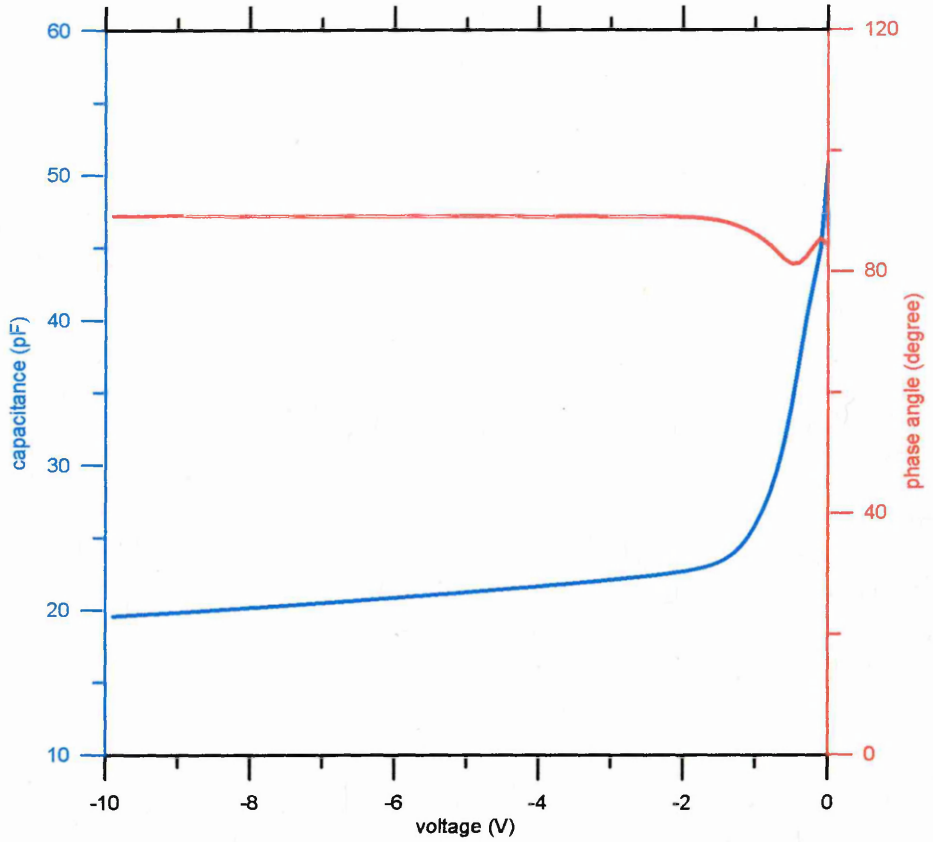

Figure 9-3 Variation of capacitance and phase angle with applied reverse bias of $Si_{0.7}$ $Ge_{0.3}$ grown on a virtual substrate.

It can be seen that according to the change in capacitance over the whole range of applied reverse bias the diode is suitable for the DLTS experiment. Due to its great importance the variation of phase angle with applied reverse bias can be seen in more detail in figure 9-4. The latter figure indicates that the phase angle increases with increase in reverse bias, which is indicative of an increase in diode resistance. The phase angle varied from 81.5° to 89.5° over a range of reverse bias from 0 to -10V. The fact that the phase angle is over 80° on the whole range of the applied voltage indicates a very good Schottky diode.

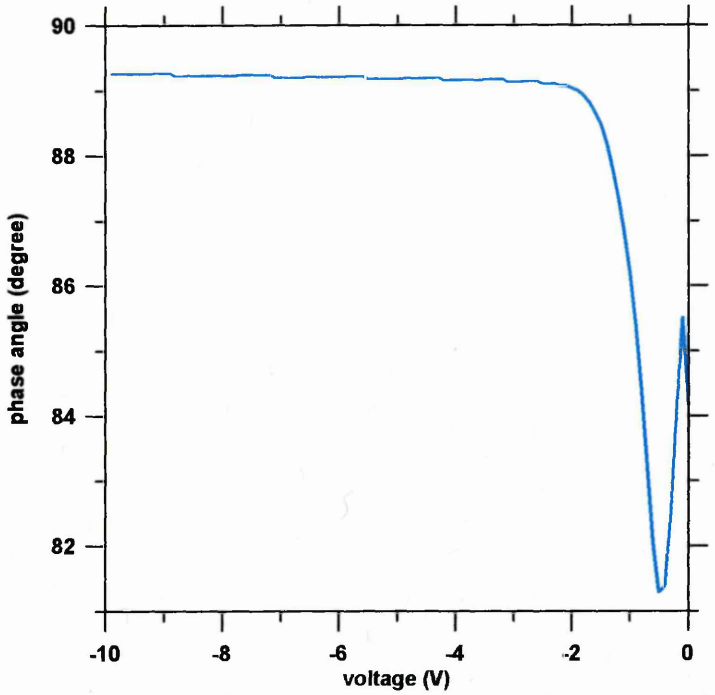

Figure 9-4 Variation of phase angle with reverse bias in more detail of the $Si_{0.7}Ge_{0.3}$ Schottky diode grown on a virtual substrate.

In figure 9-5 we can see that the change of capacitance due to change in reverse bias is very wide, between 18 pF and 50 pF, which indicates that the diode is working as a very good capacitor. The rapid change in the phase angle at low reverse bias will be discussed later on (Section 9.6.1)

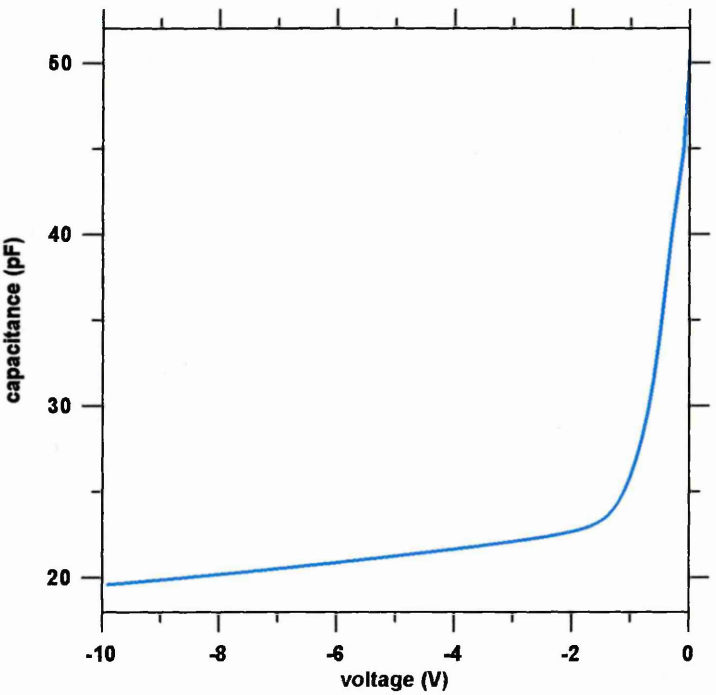

Figure 9-5 Change of the capacitance as function of reverse bias voltage of the $Si_{0.7}Ge_{0.3}$ Schottky diode grown on a virtual substrate.

One item of important information that can be extracted from the C-V measurement is the change of hole concentration with reverse bias. C-V depth profiling also monitors the change in depletion region width (w) with applied reverse bias. In figure 9-6 the variation of the depletion region width is quite clear and also indicates the diode is a very good capacitor in the reverse bias region.

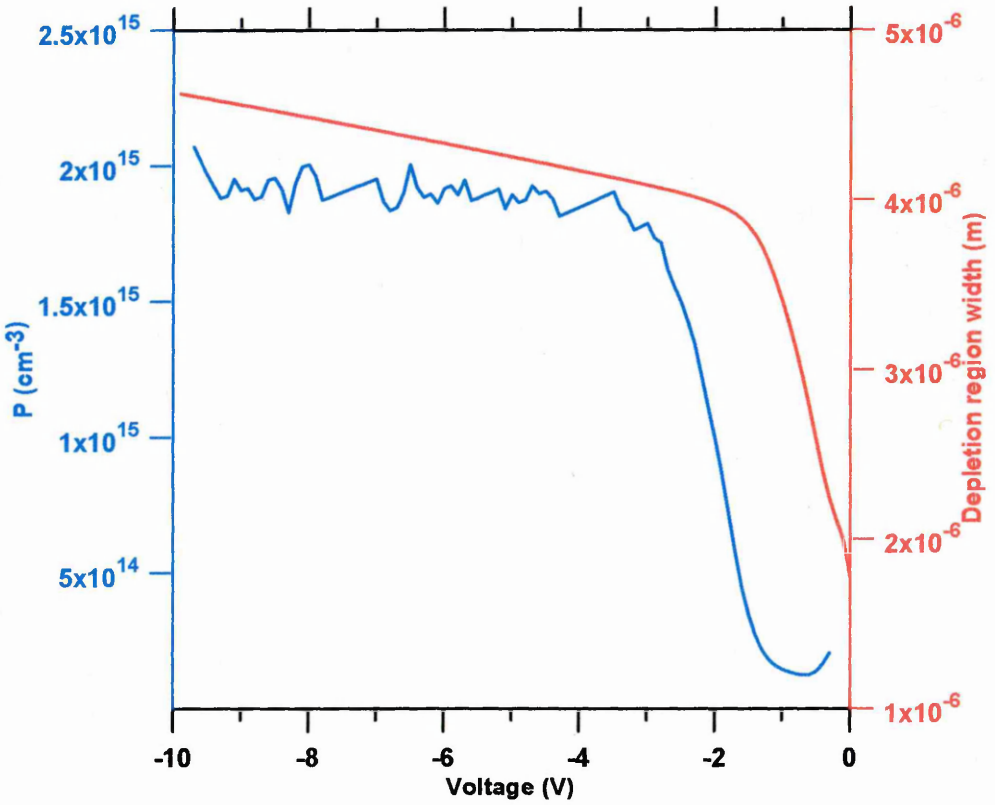

Figure 9-6 Variation of boron concentration and depletion region width with reverse bias voltage of the $Si_{0.7}$ $Ge_{0.3}$ Schottky diode grown on a virtual substrate.

Comparison between the thickness of the sample (5.515×10^{-6} m, see figure 7-5 Chapter 7) and the width of the depletion region (between 1.8×10^{-6} m, when the voltage is nearly zero in reverse bias and 4.6×10^{-6} m when the voltage is nearly -10V, see figure 9-6) means that we can measure the DLTS for the whole of the virtual substrate but we cannot easily profile through it.

The CVD growth technique introduced hydrogen, as it is in the carrier gas, and it has recently become clear that hydrogen plays a role in the formation of electrically active defects [Sque, 2004] also chemical processing introduces hydrogen in the sample. During the processing of the SiGe Schottky diode, hydrofloridic acide (HF) was used

for surface preparation. In figure 9-6 at low reverse voltages (<-3V), the presence of hydrogen by growth or processing causes a remarkable drop in carrier concentration, caused by the formation of B-H pairs, which compensates the boron atom.

9.5.3 DLTS measurements

The DLTS measurements were carried out using a 1 MHz capacitance bridge (fill pulse time 2 ms), pulse generator, and a liquid-nitrogen-cooled cryostat (80 - 350 K). The DLTS spectra were obtained at constant repetition frequency while changing the temperature. Measurement of the carrier concentration, the energy position, and the capture cross-section of the observed defects spectra have been explained earlier in (Chapters 5 and 6). The equipment and the measurement procedures were illustrated in Chapter 4, and a description of the experiment given in Chapter 8 for the Schottky diamond diodes.

As before, the Trap View computer software was used. Two rate windows were simultaneously obtained from one temperature scan, and a ratio of 5/2 was chosen for all measurements. The bias was usually -1.5, the fill pulse length was 2 ms, the temperature scanned between 80 to 350 K. the temperature consistency was checked by reversing the temperature ramp to examine for any hysteresis. During all the measurements, no forward bias injection was performed. Ten rate windows from 5000/s to 0.8/s were performed; only six rate windows are plotted in figure 9-7.

Measuring the DLTS characteristics of the SiGe diodes showed two peaks, indicating that there are defects in the samples. Various parameters shown in table 9.1 were altered until good clear peaks were found; one of these measurements is plotted here, as shown in figure 9-7.

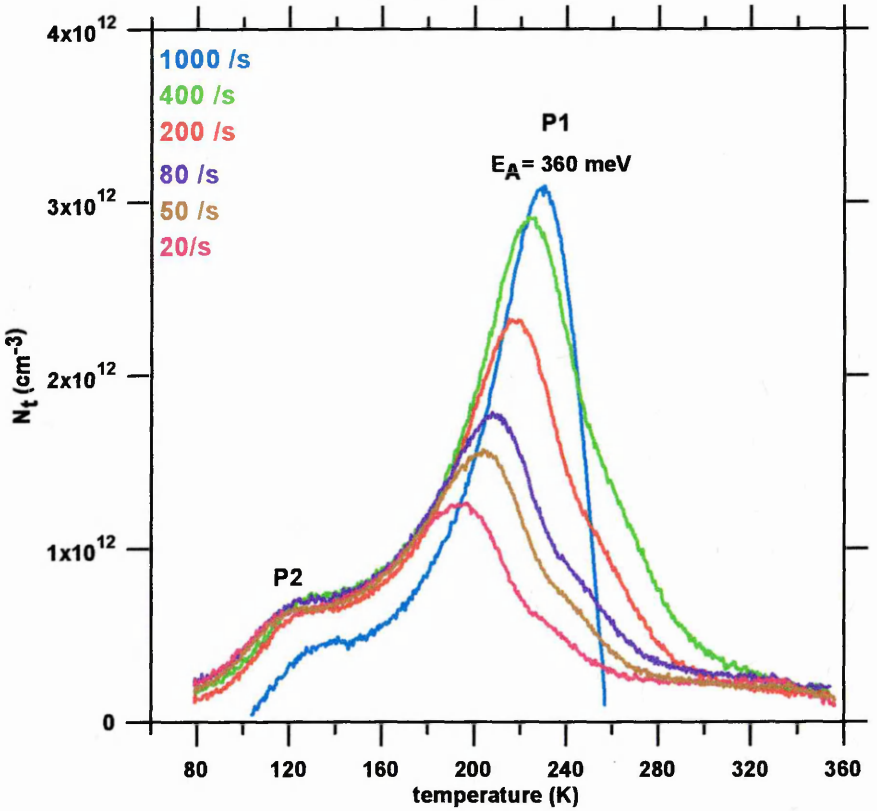

Figure 9-7 DLTS at different rate windows of $Si_{0.7}$ $Ge_{0.3}$ grown on a virtual substrate.

Voltage (V)	Fill pulse (V)	Capacitance (pF)	Phase angle (°)	Depletion region (m)	Fill pulse length (ms)
-1.5	0.1	23	87	3.67×10^{-6}	2

Table 9-1 Parameters for the DLTS measurements shown in figure 9-7

The measurements were carried out at variable temperatures from 80 to 400 K, and the rate windows used were 1000, 400, 200, 80, 50 to 20/s. Figure 9-7 shows the DLTS spectrum of SiGe diode, two peaks can be distinguished, one peak below 150 K (P2), which is small but fairly symmetrical and likely to be due to a low concentration of point defects, the second is a large peak occurring above 190 K (P1); the broadening in this peak would be caused by having different types of defects in the sample, this assumption will be discussed later on.

The DLTS peak height in figure 9-7 clearly decreases as the rate window decreases. This effect may be due to one or more reasons, including the temperature dependence of forward bias injection current which is an inherent property of non-

exponential capacitance transients and has been predicted for alloy-broadened or dislocation-related deep levels [Omling *et al*, 1983] or a possible slight temperature dependence of the capture cross section. A similar effect has been observed for majority-carrier hole trapping in $Si_{0.3}Ge_{0.7}/Si$ samples, where temperature dependent injection is not an issue [Grillot *et al*, 1995]. Hence, the observed DLTS spectrum exhibits non-ideal behaviour as compared to that of point defects. Since these lattice-mismatched SiGe/Si samples are known to have a high dislocation density, up to 10^9 cm^{-2} in the graded region [Watson *et al*, 1994], we investigated the capture kinetics of this hole trap, to determine if the observed hole trapping is dislocation related. DLTS shows that the saturation value of the signal is $\Delta C = 0.35$ pF at the rate window 1000/ s, and the diode capacitance is ~ 22 pF at a voltage of - 1.5 V; hence, the observed traps easily fall within the $\Delta C \setminus C << 1$ limit (1.6×10^{-2}).

9.5.4 Determination of trap parameters

a- Trap activation energy E_A

The DLTS peak can only be observed at temperatures where the trap emission rate is within an emission rate window. The emission rate (e) is given by

$$e = \frac{N_V \sigma_P V_{th}}{g} \exp\left(\frac{-E_A}{kT}\right) \qquad 9.5$$

Where N_V is the effective density of states, σ_P is the capture cross section of the deep level, V_{th} is the thermal velocity and g is the degeneracy of the level (g =2). If σ_P is independent of temperature, then the activation energy E_A represents the distance of the trap from the band edge. E_A can be obtained from the slope of the plot of ln (e/T^2) against 1/T or 1000/T (since $N_V V_{th}$ varies approximately as T^2).

The activation energy (E_A) of the first peak (P1) was obtained from a plot of ln (e_P/T^2) against 1/T, as shown in figure 9-8. The slope of the solid line gave an activation energy of 360 meV, although P2 was too noisy for meaningful calculation.

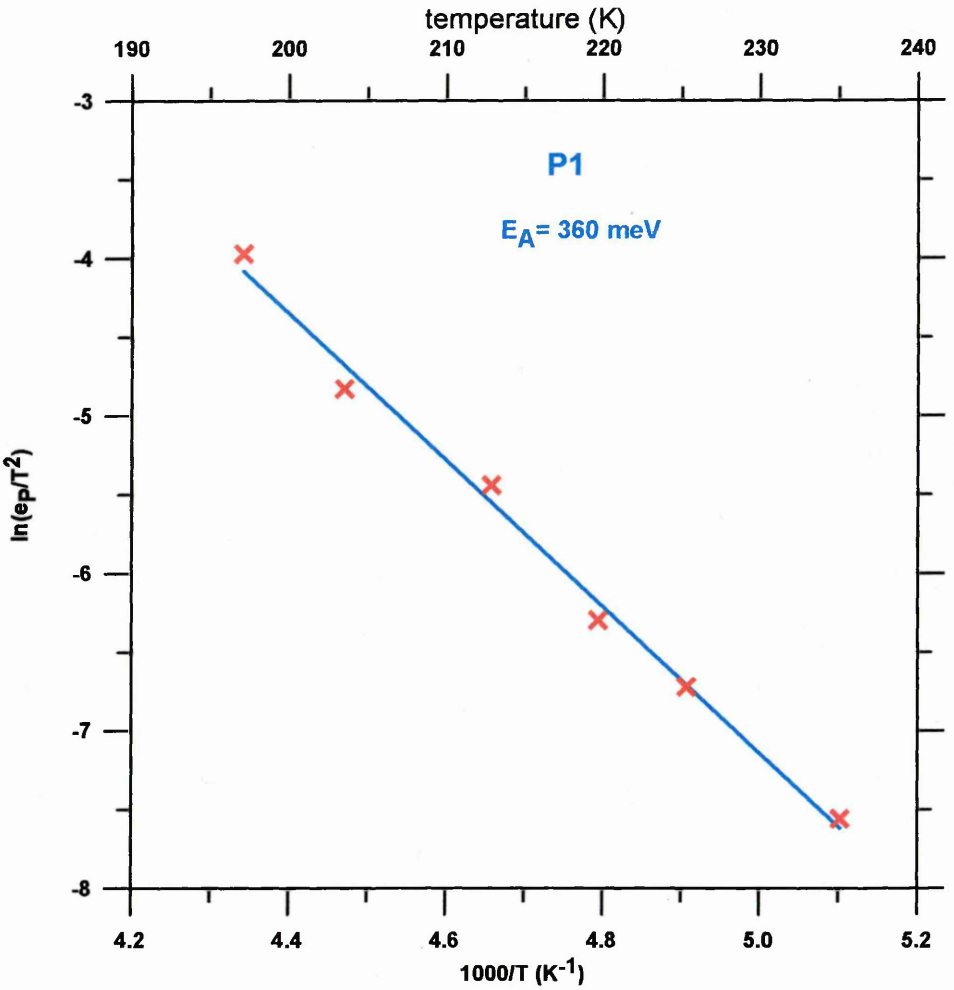

Figure 9-8 Arrhenius plots for activation energy for P1

b- Trap concentration N_T

The trap concentration N_T is given by

$$N_T = 2N_A\left(\frac{\Delta C}{C}\right) \qquad 9.6$$

where ΔC is the capacitance due to a saturating injection pulse (i.e., data from the DLTS measurements), C is the capacitance of the diode under quiescent reverse biased conditions, and N_A is the net acceptor concentration when the trap is observed. These relationships apply accurately only when (1) the trap and the doping density are uniformly distributed, with a field independent emission rate; (2) only a single emission process occurs at a deep level; and $N_T << N_A$.

The trap concentration was calculated for every temperature and is plotted in figure 9-7.

c- Capture cross section measurements

Capture cross section measurements were carried out on the older UMIST DLTS system, that is, a system with a box-car integrator for signal processing which was connected to an oscilloscope.

In order to determine the hole capture cross sections (σ_P) of the traps under consideration, DLTS measurements on the SiGe sample were made at different fill pulse lengths (0.4 to 12000 μs). With a reverse bias of – 1.5 V, a reduction in pulse lengths caused the DLTS peak height to be reduced. The capture cross section has been calculated for peak P1 using two different rate windows 200 /s and 80 /s, i.e. at two different temperatures. The capacitance varied with fill pulse length. Figures 9-9 and 9-10 show the variation of capacitance with the fill pulse length, at rate windows of 200 /s and 80 /s respectively. Both figures, show the transient area at higher resolution. From DLTS measurement in figure 9-7 and other measurements for different fill pulse length plotted in figure 9-9, 9-10 the capture cross section is calculated in figures 9-11, 9-12. The gradient of the curve is approximated by the slope of the straight line [the dots are experimental data, line is best fit exponentially].

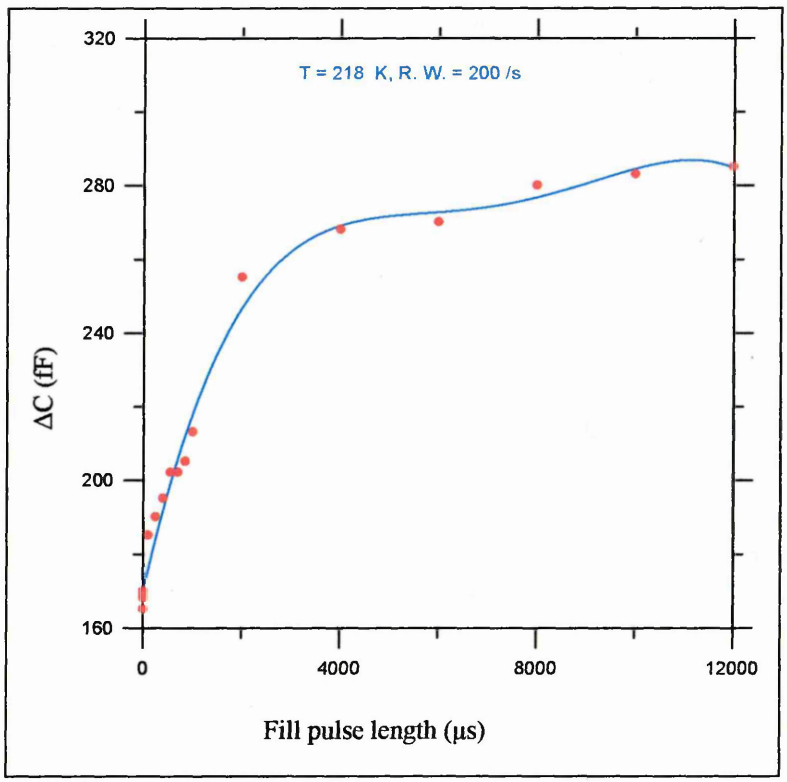

Figure 9-9 ΔC as a function of fill pulse length for the SiGe sample, T = 218 K rate window = 200 /s.

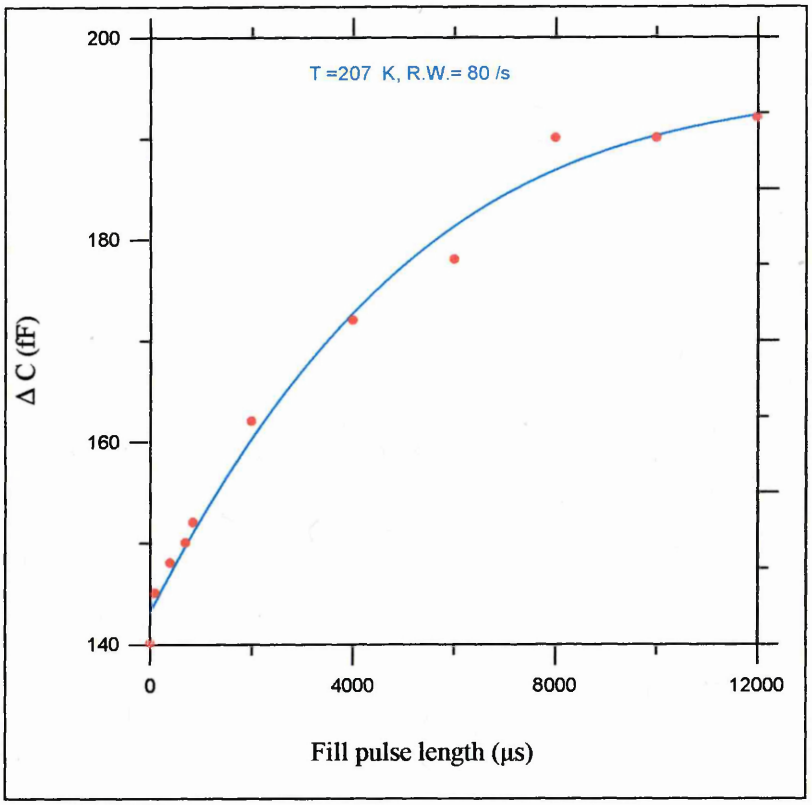

Figure 9-10 ΔC as a function of fill pulse length for the SiGe sample, T = 207 K, rate window = 80/s.

It is known that extended defects can exhibit electrical activity, and that if they do, their behaviour is significantly different from point defects with respect to free carrier trapping. As carrier capture proceeds the extended defects become gradually charged up. Capture cross sections of point defects are calculated according to the following equation:

$$ln\,[(\Delta C_\infty - \Delta C_t)/\Delta C_\infty] = \sigma_P V_{th} p_p t_p \qquad 9.7$$

where t_p is the pulse length, p_p is the majority carrier population, V_{th} is the thermal velocity, ΔC_∞ is the equilibrium capacitance value, and ΔC_t is the capacitance at time t. The majority capture cross section obeys a linear dependence on the logarithm of a combination of capacitance terms. Deviation from this relationship provides a sensitive test for the presence of extended defects that exhibits coloumbic repulsion because the repulsive force reduces subsequent carrier capture at the defect. The capture cross section therefore becomes dependent upon the amount of charge already captured at the defects, and in essence, becomes time dependent.

The capture cross section (σ_P) for the peak P1 was calculated from plotting ln [(ΔC_∞ - ΔC_t)/ ΔC_∞] vs pulse length, as shown in figures 9-11and 9-12. The y axis data points were calculated from figures 9-9 and 9-10, with the value of ΔC_∞ taken from the curve when it has levelled off. Unfortunately, for the range of fill pulse lengths available the curves did not level off but continued to increase and it was not possible to get a definite value for ΔC_∞. This adds to the suggestion that these peaks do not occur due to simple point defects in the sample.

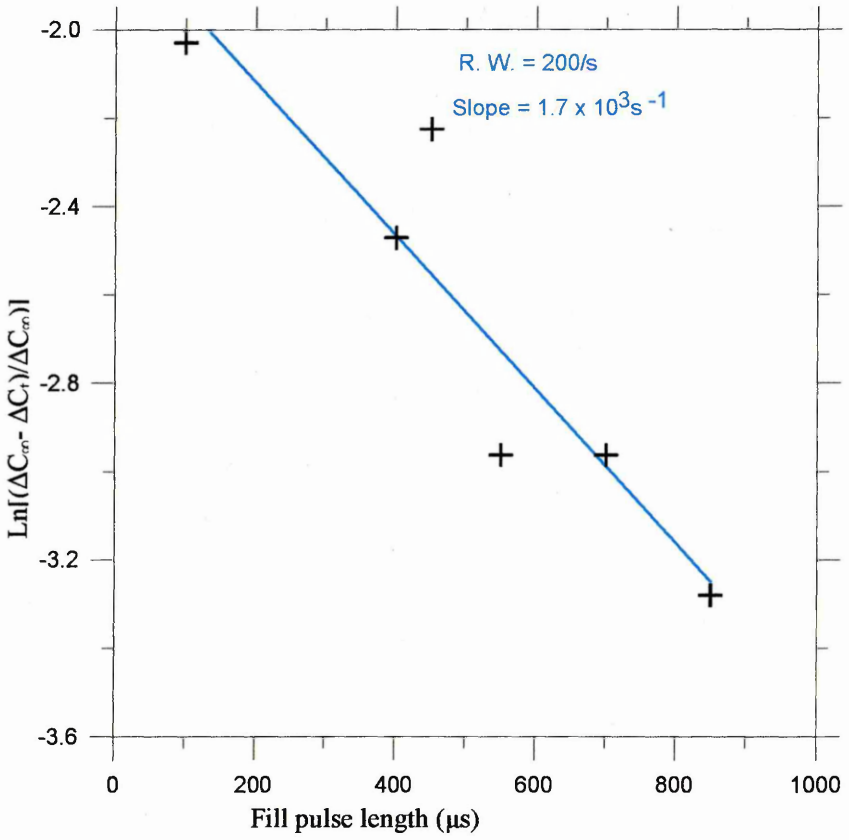

Figure 9-11 Change in capacitance as a function of fill pulse length, for a rate window of 200/s.

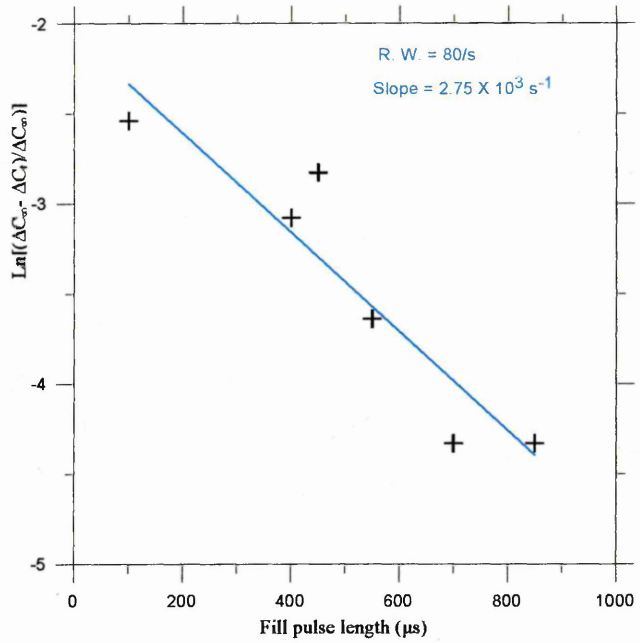

Figure 9-12 Change in capacitance as a function of fill pulse length, for a rate window of 80/s.

From figure 9-11 for peak (P1) at a rate window 200/s, the slope is -1.7×10^3 s^{-1}, and from figure 9-12 when the rate window is 80/s, the slope is -2.75×10^2 s^{-1}. The carrier concentration is 1.127×10^{14} cm^{-3} from the C-V measurement and the thermal velocity (V_{th}) is assumed constant at 8.5×10^6 cm s^{-1} at a temperature 218 K. The capture cross section was calculated to be $1.77 \times 10^{-18} cm^2$, at a rate window of 200/s, and 2.9×10^{-18} cm^2, at a rate window of 80 /s. Although these values are consistent with each other, clearly the line through the data is poor fit and this analysis has failed, as values of 10^{-18} cm^2 are not reasonable i.e. too small for the large DLTS peaks seen earlier.

Filling of extended-defects by carriers alters the local band structure around the defect. This has been established by electron beam induced current measurement [Wilshaw and Booker, 1985, Evans-Freeman *et al*, 2004] and DLTS measurements [Qian *et al*, 1993]. However, DLTS yields quite broad peaks from our samples, as seen in figure 9-7. So, further fill pulse length studies in DLTS are required to establish whether the trap is due to point or extended defect-related-states.

Exponentially decaying tails of free carriers extend from the neutral material (bulk) into the depletion region of p-n junctions or Schottky barriers. In non-

equilibrium, deep level impurities in the depletion region may readily capture free carriers from these tails. The strongly non-exponential time dependence of the capture has been calculated by Meijer *et al*, [1984] and compared with exponential data. This means that a non-exponential time dependence is particularly important in DLTS, and it also appears in many other junction measurements with deep levels. Since the free-carrier concentration decreases very rapidly, it is an other, but not always, a good approximation to consider them as abrupt junctions.

9.5.5 Laplace DLTS

LDLTS was carried out for the SiGe sample using many different temperatures. The spectra consists of many peaks, as shown in figure 9-13. The emission rate is expected to increase with temperature; however, this behaviour is not observed. The peaks appear, generally, to remain stationary as the temperature increases, though some slight shift in either direction can be observed. Because this sample was lightly doped, a varying germanium content was always present in the volume excited by DLTS because the depletion region encompassed the entire virtual substrate.

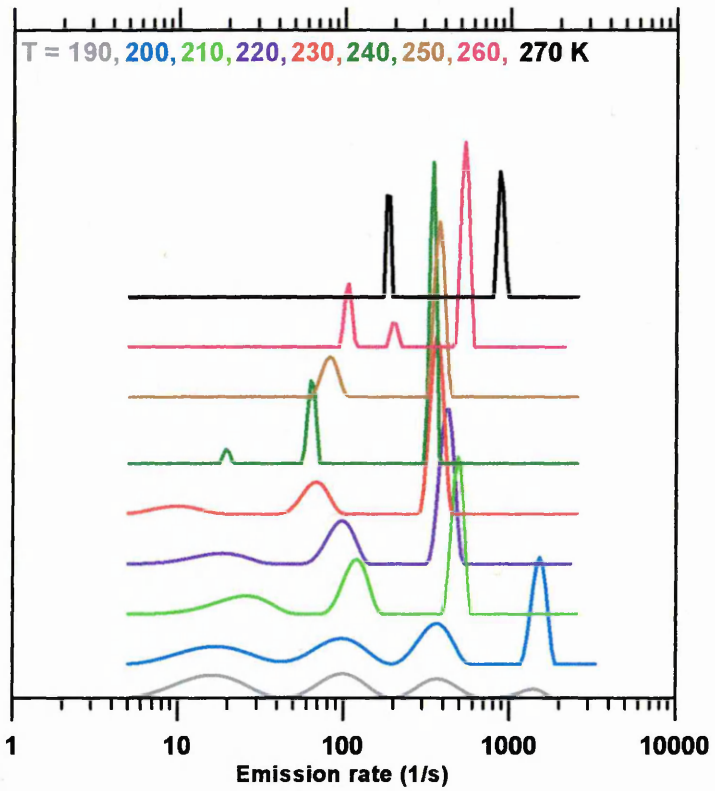

Figure 9-13 LDLTS of peak P1, for SiGe virtual substrate

According to LDLTS measurements, the peak's emission rate should increase as the temperature increases. It is assumed that the hole trap in this case is not tied to valence band and therefore an infinite range of E_A is present in the sampled volume. Hence it is suggested that LDLTS is not useful in this case.

9.6 Comparison between C-V measurements for diamond and SiGe Schottky diodes

9.6.1 Variation of phase angle with voltage

Figure 9-14 shows that the variation of phase angle with the applied reverse bias is very small (~ 0.3°) in the fabricated Schottky diamond diode, whereas in the case of the SiGe diode the variation is ~ 6°. This comparison indicates that the diamond Schottky diode more closely approximated an ideal diode from the phase angle point of view.

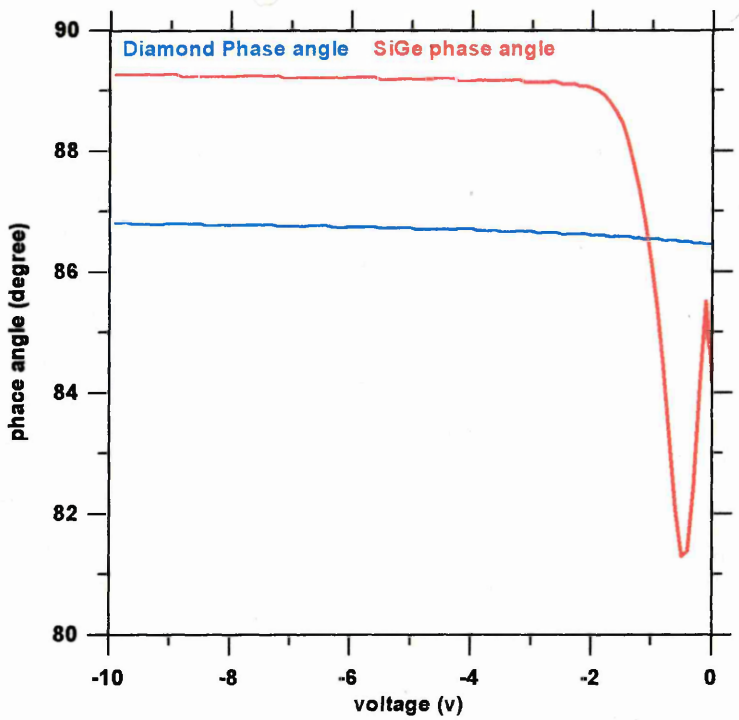

Figure 9-14 Phase angle as a function of applied reverse bias voltage for SiGe (red) and diamond (blue)

The diamond device is a simple interface between the diamond material and the Schottky metal (Al) hence the measurement refers to the bulk of the diamond. In the SiGe Schottky diode, the structure contains different materials Si, SiGe (30 %) and a

graded structure. This make the phase angle suffer a great change at low voltage where the interfaces will affect the change in the phase angle as shown in figure 9-14, and the resistance of the diode will change. This is best understood by examining figure 9-16.

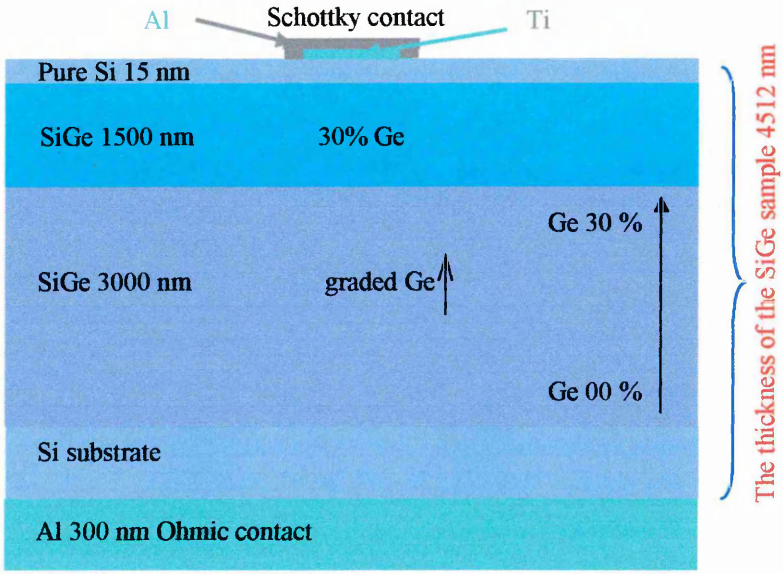

Figure 9-15 Schematic of the SiGe Schottky diode shown in figure 7-5.

9.6.2 Variation of capacitance with voltage

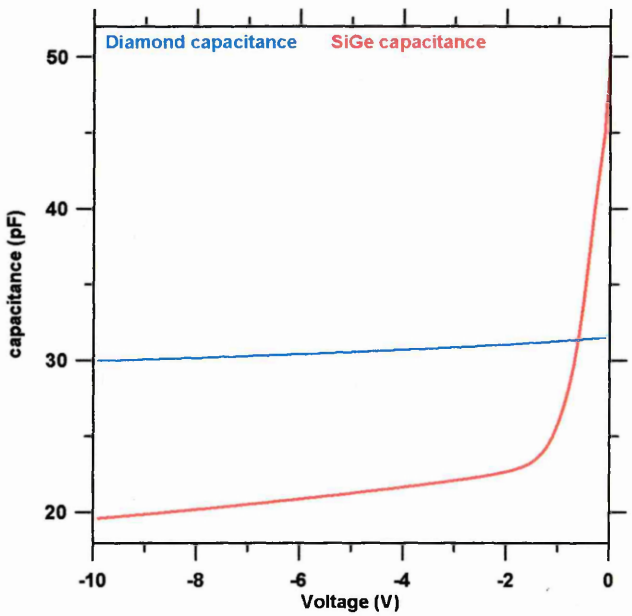

Figure 9-16 Capacitance as a function of reverse bias voltage for SiGe and diamond Schottky diodes

Figure 9-16 shows the capacitance variation (ΔC) for both diamond and SiGe Schottky diodes. This change was calculated to be 1.6 pF for diamond (see figure 8-16) and 40.2 pF for SiGe (see figure 9-5). Those results imply that in the case of Schottky diamond diodes it will be more difficult to detect any peaks using DLTS, making it less suitable for detecting defects. In the case of Schottky SiGe diodes, the situation is different as we can detect a large variation in capacitance and DLTS experiments were able to detect ΔC.

9.7 Summary

In this chapter a Schottky diode was fabricated on a SiGe virtual substrate. The structure of the sample and the growth process play an important role in how good a Schottky diode can be fabricated using that structure, as discussed in Section 9.2. Structural properties of $Si_{1-x}Ge_x/Si$ layers were illustrated. The lattice misfit parameter and critical thickness are two important factors that control the engineering of a desired structure; hence their definition and how to theoretically calculate them were introduced in Sections 9.3 and 9.4. I-V measurements, and C-V measurements and DLTS measurements were used to electrically characterise the fabricated SiGe Schottky diode.

Section 9.5.5 contains the determination of trap parameters and the electronic behaviour of the traps found in the sample. Trap activation energy, trap concentration and capture rate were discussed. It was shown that, for this particular sample, LDLTS could not be used because of the variation in the germanium content. Finally, in Section 9.6 we have illustrated a comparison between the behaviour of the diamond and SiGe Schottky diode from the C-V measurements point of view to offer an explanation as to why we would not detect a signal in the DLTS of the diamond, even though the SEM clearly showed the presence of extended defects.

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Chapter 10

Conclusions and future work

10.1 Conclusions

Properties and classification of diamond were illustrated, and different methods used for the production of synthetic diamond were discussed. After a brief review of defects that can be found in diamond we concluded that the presence of defects in a diamond sample would have a great effect on the electronic behaviour of a device fabricated from that sample. Some of these defects are structural defects such as twin defects, dislocation, etc, and external defects such as adding impurity to the semiconductor material intentionally or unintentionally, or deformation defects by irradiation or implantation.

One of the objectives of this research was to illustrate the different characterisation methods which were used to study fabricated diodes. I-V and C-V measurements provide the electrical characteristics of the diodes and were also used to study its behaviour. I-V measurements on the final fabricated Schottky diamond diode confirmed that it had acceptable current-voltage characteristics and I-V measurements at different temperature were carried out. Based on these measurements, the barrier height (φ_B) and ideality factor (n) for the diamond Schottky diode were calculated. We report a good ideality factor of 1.3 at a temperature of 400K. Also the barrier height was found to be in good agreement with the published data from other researchers. C-V measurements show that the phase angle between capacitance and voltage is acceptably close to 90^0 for temperatures greater than 300K and frequencies above 200 kHz.

Using information obtained from I-V and C-V measurements, DLTS and LDLTS measurements were carried out. DLTS measurement is a powerful tool used to study the electronic behaviour of the deep levels in conventional semiconductors and use of DLTS to study the electronic behaviour of the deep levels in diamond films was

discussed. Due to the limitations of DLTS, UMIST (Manchester) developed the high resolution Laplace DLTS technique. However, we failed to observe any peaks due to the resistive nature of the diamond and the low values of ΔC. We were able however to manipulate the depletion region edge with voltage, which paves the way for future DLTS work an higher doped samples.

In the last section of Chapter 8, we discussed Scanning Electron Microscopy. SEM was used to study the crystalline structure of the diamond samples to investigate the defects in those samples. Analysis of the SEM of the diamond samples showed that the diamond samples suffered from grain boundaries and twin defects.

It was demonstrated that using aluminium allows the production of a good Schottky barrier diode on diamond and we report the fabrication of a diamond Schottky diode featuring excellent electrical characteristics. The leakage current for the low boron doped sample was as small as 10^{-7}A, and was as low as 10^{-6}A for the highly boron doped samples, which is the smallest ever reported leakage current for this type of diamond Schottky diode. All the steps carried out to prepare the samples for Schottky diode fabrication are described.

The results obtained in this work show that properly prepared and carried out, Ohmic contacts can be attached to the faces of the sample. In this work we sputtered layers of titanium, platinum and gold on the rear of the sample, and evaporated aluminium through holes in a flat metal mask onto the front face of the sample. Experimental measurements found the width of the depletion region to be 2.89 μm. From this the mobility was calculated and found to be 46.5×10^{-2} cm^2/Vs.

After the study and fabrication of a diamond Schottky diode, we examined the possibility of fabricating a Schottky diode on a virtual substrate. Based on the electrical characterization of the fabricated SiGe Schottky diode, the leakage current was as low as 10^{-7} A (for doping concentration between 5×10^{14} to 2.5×10^{16} cm^{-3}). From the phase angle point of view, diamond Schottky diode showed a small variation in resistance due to the fact that there is only one semiconductor/metal interface between diamond and aluminium. In the case of SiGe Schottky diode, the structure contains different materials (Si, $Si_{0.7}Ge_{0.3}$) which will introduce a higher difference in resistance causing the phase angle suffer a great change at low voltage. From the capacitance profiling point of view,

diamond Schottky diode showed small capacitance variation compared to the capacitance variation of the SiGe Schottky diode.

Experiments showed two peaks in the temperature between 190-260K and 90-120K. LDLTS measurements were carried out to further investigate the results obtained from the DLTS measurements, and the variation in peak location and intensity indicated that the defects in the sample were not point defects. Capture cross-section measurements and calculations were carried out to study the electronic behaviour of the traps. The relation between the change in capacitance and fill pulse width indicated that the defect is an extended defect.

SEM confirmed the high density of grain boundaries and dislocations in the CVD diamond. Because there are no determinable defects in the diamond samples by DLTS, future work will be with single crystal diamond doped with boron to avoid the effects of grain boundaries. The SiGe DLTS results show that the virtual substrate was highly defective, which has serious consequences for device performance if included in new device designs.

10.2 Future work

One of the draw backs in the diamond samples was the lack of a good crystalline structure and poor acceptor ionisation, which made the defects investigation using DLTS and LDLTS impossible. The use of a single crystal CVD diamond samples would enable the study of different types of defects using conventional DLTS and LDLTS although the acceptor ionisation problem will remain with boron, as the activation energy is 370 meV.

In case of SiGe samples, the virtual substrate was undoped yielding a wider depletion region width. Doping the virtual substrate would decrease the depletion region width (w) which will enhance the electronic behaviour of the Schottky diode fabricated using that sample. However, industry is undecided about whether to adopt virtual substrates, because of their highly defective nature, and, at present (since year 2000) seems to be moving towards producing small, as-grown local strained SiGe regions. These provide compressively strained electrical studies may not now be as strong as it was when this study was commenced.