Engineering of Electroplated Materials for Multilayer Next Generation Graded Bandgap Solar Cells

Ayotunde Adigun OJO

A thesis submitted in partial fulfilment of the requirements of
Sheffield Hallam University for the degree of
Doctor of Philosophy

October 2017

Declaration

I hereby declare that the work described in this thesis is my work, done by me and has not been submitted for any other degree anywhere.

Ayotunde Adigun Ojo

Acknowledgement

The achievements made in this work would not have been possible without the grace and blessings of God who makes all things beautiful in His time. Tremendous appreciation goes to my Director of Studies (DOS) Prof. I.M. Dharmadasa for his professional mentorship. I do also recognise my second supervisor Prof. Wayne Cranton, Dr. A.K. Hassann and Dr. Paul Bingham for their contributions.

Sincere appreciation goes to all the members of the Solar Energy Research Group of Sheffield Hallam University; this includes Dr. O.K. Echendu, Dr. F. Fauzi, Dr. N.A. Abdul Manaf, Dr. H.I. Salim, Dr. O.I. Olusola, Dr. M.L. Madugu, Dr. Burak Kadem and Dr. Yaqub Rahaq for their useful advice, technical discussions, and constructive criticisms. Appreciation also goes to MERI member of staff including Gillian Hill, Gail Hallewell, Rachael Toogood, Corrie Houton, Gary Robinson, Deeba Zahoor, Stuart Creasy, Paul Allender, Bob Burton, and Dr. Tony for their administrative and technical support during my research program. I do also acknowledge the contributions of my friends within MERI most especially Olalekan Ojedokun, Abubakar Mohammed, Oluwaseun Oluwafemi and Alireza Dastan to mention but a few. I do recognize the VC, DVCs, Dean of Engineering, HOD Mechanical Engineering and other departmental and faculty colleagues in Ekiti State University (EKSU), Ado-Ekiti, Nigeria.

I am eternally grateful to my wife Moyosore Ayotunde-Ojo for standing by me through the thick and thin. Most especially for taking care of our children (Ayomide and Olamide Ayotunde-Ojo) in my absence. You are indeed a treasure of inestimable value. Appreciation also goes to my parents (Mr & Mrs A.K. Ojo) for their moral support and also to my in-laws (Mr & Mrs Ajiboye) for their encouragement. To my sweet sister Ajibola Elubeku, I say thank you for your continued support. To my late brother Adebayo Moyosore Ojo, it still feels like yesterday when you left to answer the call above. Thank you for the positive contributions you made in all our lives.

Appreciation also goes to my extended family including The Elubeku's, The Ogunjimi's, The Afolabi's, The Agbaje's, The Omope's, The Bamidele's and The Ogunleye's for their moral support. I do acknowledge the staff and management of Northfield Nursing Home, most especially Jenny P., Kelly C., Danielle H., Jenny C., Sue F., Valery T., Carley A., Maxine S., George M., Ula K., Rachael P., Alina P., Shirley, Ally W., Annette and Mark for all their support. Thanks and God bless you all.

Dedication

This research work is dedicated to God almighty for his salvation, love, grace, guidance and abundant blessings that always sees me through all things.

Ayotunde Adigun Ojo

List of Publications

Journal Publications

1. A.A. Ojo, I.M. Dharmadasa, Electrodeposition of fluorine-doped cadmium telluride for application in photovoltaic device fabrication, Mater. Res. Innov. 19 (2015) 470–476. doi:10.1080/14328917.2015.1109215.

2. A.A. Ojo, I.M. Dharmadasa, Investigation of electronic quality of electrodeposited cadmium sulphide layers from thiourea precursor for use in large area electronics, Mater. Chem. Phys. 180 (2016) 14–28. doi:10.1016/j.matchemphys.2016.05.006.

3. A.A. Ojo, I.M. Dharmadasa, 15.3% efficient graded bandgap solar cells fabricated using electroplated CdS and CdTe thin films, Sol. Energy. 136 (2016) 10–14. doi:10.1016/j.solener.2016.06.067.

4. I. Dharmadasa, A. Ojo, H. Salim, R. Dharmadasa, Next Generation Solar Cells Based on Graded Bandgap Device Structures Utilising Rod-Type Nano-Materials, Energies. 8 (2015) 5440–5458. doi:10.3390/en8065440.

5. H.I. Salim, O.I. Olusola, A.A. Ojo, K.A. Urasov, M.B. Dergacheva, I.M. Dharmadasa, Electrodeposition and characterisation of CdS thin films using thiourea precursor for application in solar cells, J. Mater. Sci. Mater. Electron. 27 (2016) 6786–6799. doi:10.1007/s10854-016-4629-8.

6. A.A. Ojo, H.I. Salim, O.I. Olusola, M.L. Madugu, I.M. Dharmadasa, Effect of thickness: a case study of electrodeposited CdS in CdS/CdTe based photovoltaic devices, J. Mater. Sci. Mater. Electron. 28 (2017) 3254–3263. doi:10.1007/s10854-016-5916-0.

7. O.I. Olusola, M.L. Madugu, A.A. Ojo, I.M. Dharmadasa, Investigating the effect of GaCl3 incorporation into the usual $CdCl_2$ treatment on CdTe-based solar cell device structures, Curr. Appl. Phys. 17 (2017) 279–289. doi:10.1016/j.cap.2016.11.027.

8. A.A. Ojo, I.M. Dharmadasa, Progress in development of graded bandgap thin film solar cells with electroplated materials, J. Mater. Sci. Mater. Electron. 28 (2017) 6359–6365. doi:10.1007/s10854-017-6366-z.

9. A.A. Ojo, I.M. Dharmadasa, The Effect of Fluorine Doping on the Characteristic Behaviour of CdTe, J. Electron. Mater. 45 (2016) 5728–5738. doi:10.1007/s11664-016-4786-9.

10. A.A. Ojo, I.M. Dharmadasa, Optimisation of pH of cadmium chloride post-growth-treatment in processing CdS/CdTe based thin film solar cells, J. Mater. Sci. Mater. Electron. 28 (2017) 7231–7242. doi:10.1007/s10854-017-6404-x.

11. A.A. Ojo, I.M. Dharmadasa, Effect of Gallium Doping on the Characteristic Properties of Polycrystalline Cadmium Telluride Thin Film, J. Electron. Mater. (2017). doi:10.1007/s11664-017-5519-4.

12. I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, O.I. Olusola, H.I. Salim, M.L. Madugu, A.A. Ojo, Improvement of composition of CdTe thin films during heat treatment in the presence of $CdCl_2$, J. Mater. Sci. Mater. Electron. 28 (2017) 2343–2352. doi:10.1007/s10854-016-5802-9.

13. A.A. Ojo, I.O. Olusola, I.M. Dharmadasa, Effect of the inclusion of gallium in normal cadmium chloride treatment on electrical properties of CdS/CdTe solar cell, Mater. Chem. Phys. 196 (2017) 229–236. doi:10.1016/j.matchemphys.2017.04.053.

14. A.A. Ojo, I.M. Dharmadasa, Analysis of electrodeposited CdTe thin films grown using cadmium chloride precursor for applications in solar cells, J. Mater. Sci. Mater. Electron. (2017). doi:10.1007/s10854-017-7264-0.

15. I.M. Dharmadasa, A.A. Ojo, Unravelling complex nature of CdS/CdTe based thin film solar cells, J. Mater. Sci. Mater. Electron. 28 (2017) 16598–16617. doi:10.1007/s10854-017-7615-x.

16. A.A. Ojo, I.M. Dharmadasa, Analysis of the electronic properties of all-electroplated ZnS, CdS and CdTe graded bandgap photovoltaic device configuration, Sol. Energy. 158 (2017) 721–727. doi:10.1016/j.solener.2017.10.042.

Conference Proceedings

17. A. A. Ojo and I. M. Dharmadasa, "Electrodeposition of Fluorine Doped Cadmium Telluride for Application in Photovoltaic Device Fabrication", Proceedings of the 11th Photovoltaic Science, Applications and Technology Conference C97, University of Leeds, Leeds, United Kingdom, (2015) 109-112.

18. I. M. Dharmadasa, A.A. Ojo, H.I. Salim and R. Dharmadasa, "Next Generation Solar Cells Based on Graded Bandgap Devices Utilizing Rod-Type Electroplated Nano-Materials", Proceedings of the 11th Photovoltaic Science,

Applications and Technology Conference C97, University of Leeds, Leeds, United Kingdom, (2015) 169.

19. I. M. Dharmadasa, A.A. Ojo, H.I. Salim and R. Dharmadasa, "Next Generation Solar Cells Based on Graded Bandgap Devices Utilizing Rod-Type Electroplated Nano-Materials", Proceedings of the UK Semiconductor 2015, Sheffield Hallam University, United Kingdom, (2015) pp 102.

20. A. A. Ojo and I. M. Dharmadasa, "Effect of Fluorine Doping on the Characteristic properties of CdTe", Proceedings of the UK Semiconductor 2015, Sheffield Hallam University, United Kingdom, (2015) pp 129.

21. H. I. Salim, A. Ojo and I.M. Dharmadasa, "Effect of $CdCl_2$ and $CdCl_2+CdF_2$ treatment on the structural, morphological and optical properties of electrodeposited CdTe thin films" Proceedings of the UK Semiconductor 2015, Sheffield Hallam University, United Kingdom, (2015) pp 133.

22. I. M. Dharmadasa, A.A. Ojo, H.I. Salim and R. Dharmadasa, "Next Generation Solar Cells Based on Graded Bandgap Devices Utilizing Rod-Type Electroplated Nano-Materials", Proceedings of the BIT's 2nd Annual World Congress of Smart Materials - Develop New Path of Smartness. Grand Copthorne Waterfront Hotel, Singapore, Malaysia, (2016) pp 065.

23. A. A. Ojo and I. M. Dharmadasa, "Effect of multilayer structure on the characteristic properties of CdS/CdTe solar cell", Proceedings of the UK Semiconductor 2016, Sheffield Hallam University, United Kingdom, (2016) pp 079.

24. A. A. Ojo and I. M. Dharmadasa, "All Electrodeposited Next Generation Solar Cell Based on Multi-Layer Device Configuration", Proceedings of the 12th Photovoltaic Science, Applications and Technology Conference C97, University of Liverpool, Liverpool, United Kingdom, (2016) pp 61.

25. A. A. Ojo and I. M. Dharmadasa, "18% Efficient next generation graded bandgap solar cells fabricated using low-cost electroplated rod-type nano-materials", Proceedings of the 6th Annual MERI Research Symposium, Sheffield Hallam University, Sheffield, United Kingdom, (2016) pp 18.

Manuscript under preparation

26. Effect of iodine doping on both the material and electronic properties of CdTe.
27. Effect of pH on $CdCl_2+Ga_2(SO_4)_3$ treatment on CdS/CdTe-based solar cell.

Abstract

The work presented in this thesis aims to reduce cost per capita and increase the conversion efficiency of CdS/CdTe-based solar cells using multilayer graded bandgap configurations. To effect economic viability, electroplating technique was utilised as the low-cost semiconductor deposition technique. CdS and CdTe are the primary materials grown and explored in this thesis. These layers were characterised for their structural, morphological, compositional, optical, and electrical properties using X-ray diffraction, Raman spectroscopy, scanning electron microscopy, energy-dispersive X-ray spectroscopy, UV-Vis spectroscopy, photoelectrochemical cell measurement, current-voltage and capacitance-voltage measurement techniques.

The precursor (thiourea) utilised in the deposition of CdS solves the problem of sulphur precipitation during electroplating. Very few publications with explicit exploration on this subject are available in the literature. Further to this, the nitrate and chloride based CdTe precursors explored is an alternative to the sulphate based norm as reported in the literature. The effect of extrinsic doping of CdTe incorporating F, Cl, I and Ga was also systematically explored to improve both the material and electronic properties of CdTe. Doping of CdTe during growth was studied by adding the above dopants to the electrolyte. The inclusion of F and Ga into the regular $CdCl_2$ post-growth treatment (PGT) and the effect of pH were also explored with improved results as compared to the regular $CdCl_2$-PGT. The inclusion of Ga into the regular $CdCl_2$ post-growth treatment (PGT) and the effect of pH were also explored with the improved result as compared to the regular $CdCl_2$ PGT. The solar cell device configurations explored include *n-n+*large Schottky barrier (SB), *n-p*, *n-n-n+*SB and *n-n-p* incorporating CdS/CdTe-base semiconductors.

Based on all experimental findings as explored within the limit of this thesis, the most promising of the configurations examined are the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au with thicknesses of glass/FTO/(120 nm) *n*-CdS/(1200 nm) *n*-CdTe/(30 nm) *p*-CdTe/(100 nm) Au. The highest conversion efficiencies observed for two separate batches were 15.3% and 18.4%. The devices with the 18.4% efficiency showed some instability and therefore require further investigation. The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au configuration with thicknesses of glass/FTO/50 nm *n*-ZnS/(65 nm) *n*-CdS/(1200 nm) *n*-CdTe/(100 nm) Au also show promising results with the highest efficiency achieved being 14.1% owing to bandgap grading strengths.

Table of Contents

Chapter 1 - Introduction

1.1 Global energy supply and consumption

Energy is an essential constituent of economic growth and development whose demand increases with a corresponding increase in population [1]. With global population increase from 1 billion in the 1600s to 7.5 billion at present (2017) and a projected increase to 9.7 billion by 2050 [2], concerns over exhaustion, energy resources supply difficulties and substantial environmental impacts (such as depletion of the ozone layer, global warming, climate change, amongst others) have been raised for conventional energy sources [3,4]. The 2017 edition of British Petroleum's annual outlook as depicted in Figure 1.1 shows that fossil fuel has dominated the world's energy resource consumed with a commanding ~85%, ~5% to nuclear power and less than 10% to renewable energy resources [5]. This trend cannot be sustained without any catastrophic effect [3,4] with increasing energy demand, Hence, the requirement for a commensurate carbon-neutral energy source with energy resource equal to or greater than the present day energy demand is imperative.
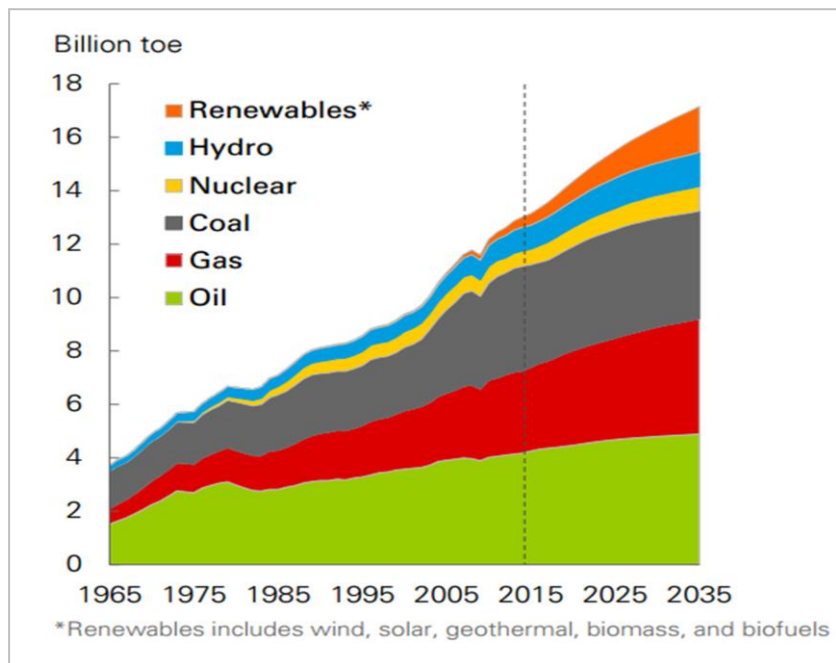
Figure 1.1: BP world energy consumption chart (2017). *(1 Btoe = 11.63 PWh)*

1.2 Energy sources

Depending on how long it takes for a primary energy source to be replenished, energy sources can be categorised as either non-renewable or renewable (or alternative) energy sources.

1.2.1 Non-renewable energy sources

Non-renewable energy sources are sources that are not replenishable within a human lifetime. Energy sources such as fossil fuels (crude oil, natural gas, coal and other petroleum products) and uranium (for nuclear energy) fall under non-renewable energy sources [6]. Fossil fuels are generated from combustible geological deposits of organic materials formed from decayed animals and plants buried in the earth's crust at high pressure and temperature over thousands and millions of years. The combustion of fossil fuel products or by-products releases a tremendous amount of greenhouse gases. Uranium ore which serves as fuel in nuclear plants due to its radioactive property is classified as non-renewable due to their rarity, as it is mined in limited locations around the globe.

1.2.2 Renewable energy sources

Renewable or alternative energy sources are sources that are replenishable within a human lifetime. Sunlight, wind, hydro, ocean tide, geothermal heat and biomass are primary energy sources which fall under this classification due to their infinite nature and reusability without exhaustion but continue their endless cycle. It is interesting to note that most of the renewable energy resources other than geothermal energy and tidal wave energy depend directly or indirectly on sunlight. With about 4.3×10^{20} J [7] and an estimated 1367 Wm^{-2} irradiance made available to the earth's surface through sunlight, solar energy emerges by far as the most abundant exploitable resource. Based on these facts, research and development have been deployed into the science and technology of achieving high solar energy conversion efficiency and reduction in the cost of production.

1.3 Solar energy

With a mass of about 2×10^{30} kg, a diameter of 1.39×10^{9} m, a surface temperature of about ~6000 K and a core temperature of about $\sim 1.5 \times 10^{7}$ K, the sun stands as the primary source of solar energy and the centre of the solar system [8]. The energy generated by the sun is achieved by the constant fusion of hydrogen to helium nuclei and the release of a significant amount of energy (in the form of electromagnetic radiation and heat) in a process known as the thermonuclear process. The radiation from the sun reaches the earth at ~480 s putting into consideration the speed of light $(2.99 \times 10^{8}$ $ms^{-1})$ and the mean distance between the earth and the sun $(1.496 \times 10^{8}$ km). The average amount of radiation measured at the sun's surface is about 5.691×10^{7} Wm^{-}

^{2}, while just ~1367 Wm^{-2} reaches the earth's atmosphere [9]. Out of this, 51% of the radiation reaches the earth surface with enough energy in one hour to cater for global energy utility in a year [7,10]. The remaining radiation is accounted for by the reflection of the incident radiation back into space and the absorption of the radiation by the atmosphere which is valued at about 30% and 19% respectively [11], as shown in Figure 1.2. The high attenuation of the solar radiation as it reaches the earth as compared to the radiation on the surface of the sun can be attributed to the effect of air mass (AM).
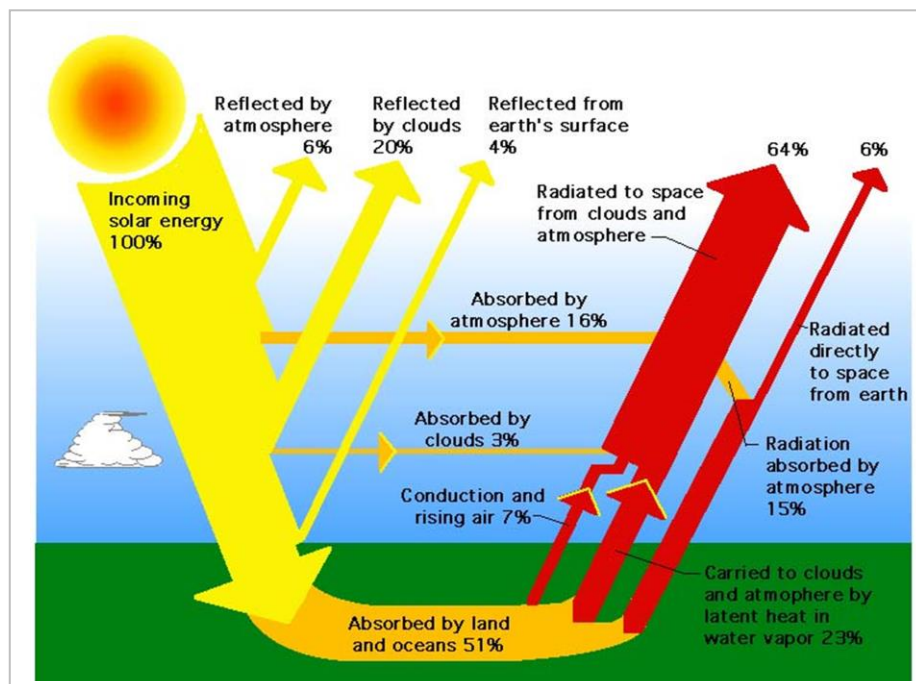
Figure 1.2: Global modification of incoming solar radiation by atmospheric and surface processes. (Adapted from Ref. [11])

1.4 Air mass coefficients

Air mass (AM) is a measure of how sunlight propagates through the Earth's atmosphere. It can also be defined as the shortest path through the atmosphere that sun rays pass through before reaching the surface of the earth. Air mass accounts for the attenuation of the radiation measured at the sun's surface compared to that measured at the earth's surface. The attenuation is due to absorption, reflection and scattering caused by the ozone layer (O_3), water molecules, carbon dioxide (CO_2), dust and clouds as sunlight pass through the atmosphere [9,12]. Furthermore, the density of the atmosphere and the path length of the sunlight impacts the attenuation of the radiation.

Air mass zero (AM0) refers to the standard spectrum outside the earth's atmosphere or the solar irradiance in space. The power density of AM0 is valued at 1367 Wm^{-2} [9].

This value is used for the characterization of solar cells used in outer space. AM1.0 is used for tropical regions on earth surface where the sun is directly above the earth's zenith point. The incident power per area is valued at 1040 Wm^{-2} [9]. AM1.5 valued at 1000 Wm^{-2} or 100 $mWcm^{-2}$ [9] defines the power density of the incident solar radiation reaching the earth's surface known as Insolation. This value is used by the PV industry as Standard Test Condition (STC) for terrestrial solar panels characterizations.

1.5   Energy distribution of the solar spectrum

As the solar radiation emanating from the surface of the sun reaches the atmosphere, its intensity and spectral configuration changes due to attenuation. The spectral configuration known as the solar spectrum reaching the earth surface spans across the wavelengths (λ) of three spectra regions namely: ultraviolet (UV), visible (Vis), and infrared (IR) as shown in Figure 1.3 [13]. The ultraviolet region is approximately 5% of the total irradiation with a wavelength <400 nm, the visible region lies within the wavelength range of (380 and 780) nm, and it is approximately 43% of the irradiance. While the infrared region has a wavelength >780 nm and it is about 52% of the irradiance distribution.
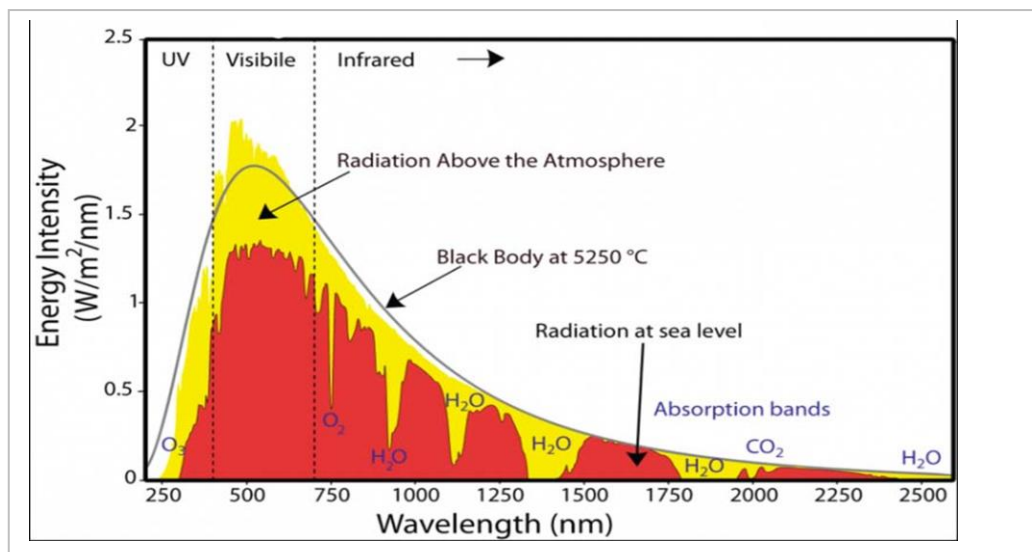
Figure 1.3: The solar spectrum showing the spectral irradiance as a function of photon wavelength at outer Earth's atmosphere (black body), at the top of the atmosphere (AM0) and at the sea level (AM1.5). (Adopted from Ref. [13])

Based on requirements, solar energy technology has grown to focus on different spectral regions. The solar thermal technology is inclined to harness energy from the infrared region in the form of heat while the solar photovoltaic (PV) and concentrated solar power (CSP) harnesses energy from both the visible and the ultraviolet spectral regions.

However, recent development in PV has shown the possibility of harnessing energy from the UV, Vis and IR regions [14,15]. In the research work presented in this thesis, emphasis will be laid on photovoltaic solar energy conversion technology using II-VI semiconductor materials.

1.6 Photovoltaic solar energy conversion

Photovoltaic (PV) energy conversion technology referred to the direct conversion of solar energy (electromagnetic radiation from the sun) into electricity. The technology entails the generation of electrical power by converting solar radiation into a flow of electrons in the form of direct current (DC). Photons from solar radiation excite the electrons in a photovoltaic device into a higher state of energy, allowing them to act as charge carriers. The technology requires the use of suitable semiconductor materials with photovoltaic property, the formation of a depletion region from which electron-hole (e-h) pairs are created - provided photons with energy level higher than the bandgap are introduced, efficient separation of charge carriers before recombination, and transportation of the charge carrier through an external circuit [16]. For an excellent PV conversion, it is imperative that all the stated requirements are met. Figure 1.4 shows the schematic representation of the PV effect using a simple *p-n* junction configuration.

The absorber material utilised in PV cells fabrication are categorised under first, second and third generation (next generation) solar cells. The first generation solar cells include monocrystalline silicon (mono-Si) and polycrystalline silicon (poly-Si) based solar cells [17]. The first generation solar cells are the most established of all the solar cell categories. They are known for high material usage (bulk materials) and high fabrication cost. The second generation solar cells incorporate thin film technology with reduced material usage, material/fabrication cost and they are scalable. Examples of the second generation solar cells include amorphous silicon (a-Si), cadmium telluride (CdTe) [18] and copper indium gallium diselenide (CIGS) [16,19]. The third generation solar cells are characterised by thinner films, low fabrication temperatures, and lower cost. They tend to overcome the Shockley–Queisser limit of power efficiency for single bandgap solar cells [20–24].
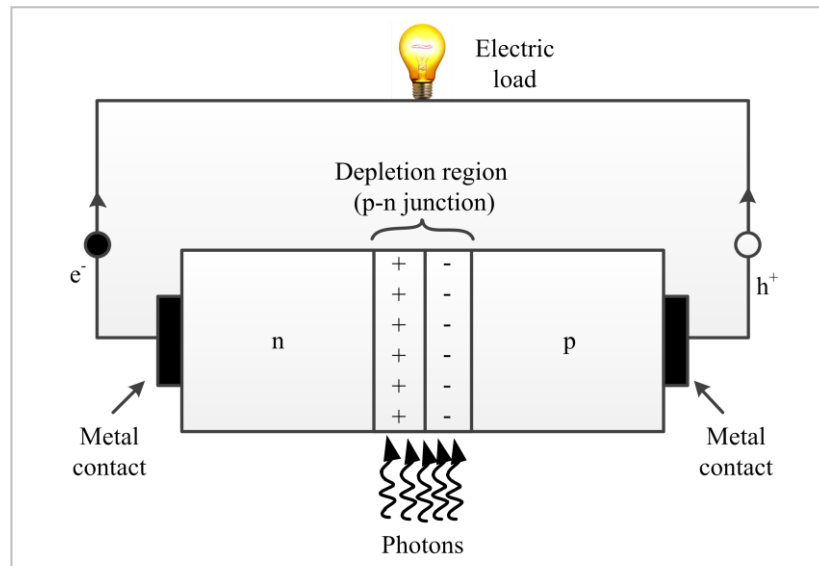
Figure 1.4: Schematic diagram of a simple p-n junction showing photon absorption, e-h creation, e-h separation and the effect e-h collection through the external circuit.

With such high economic potential from both the second and third generation solar cells, Si-based (first generation) cells still hold the highest PV efficiency for terrestrial solar modules [25] and the most significant market share due to its well-established technology.

1.6.1 Operating configuration of photovoltaic solar cells

According to the literature [26–28], the two primary configurations of a thin film solar cell are the substrate and superstrate device configurations. The classification depends on the sequence in which the layers are deposited (see Figure 1.5).
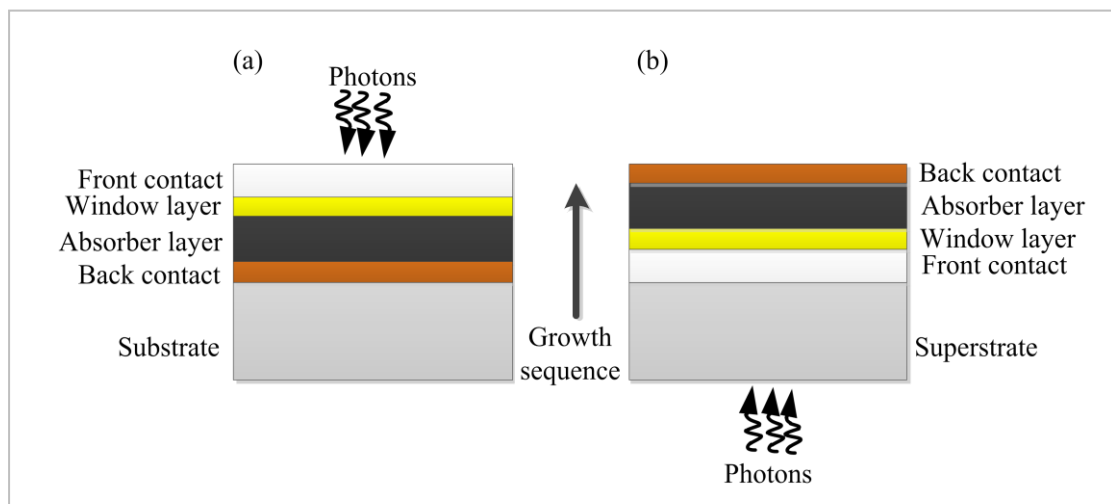
Figure 1.5: Schematic cross-section of substrate and superstrate configurations of thin film solar cells. Both configurations are capable of generating high photon to electron conversion efficiency [24,29–32]. A similar feature to both configurations is that photons enter the solar cell devices through the front contact and the window layer. But distinctively, in

the superstrate configuration photons pass through the glass before reaching the window layer/absorber layer junction. This is unlike the substrate configuration where photons are directly admitted to the window layer/absorber layer junction without any apparent or significant obstruction asides the shading of the cells by the front contacts. It is therefore crucial that the top transparent conducting oxide and glass utilised in the superstrate configuration must fulfill several stringent requirements, including low sheet resistance, temperature durability, excellent chemical stability, excellent adhesion and high optical transmission in the spectrum of interest.

The solar cell device fabrication work done during this program as reported in this thesis use the superstrate configuration. This is due to the following reasons:

i. The semiconductor deposition technique utilised: a conducting substrate such as fluorine doped tin oxide (FTO) is required as the electrode on which the semiconductor is deposited using the electroplating technique. (see Section 1.6).

ii. The metal back contact as required in substrate configuration has a high tendency of dissolving in the acidic aqueous electrolyte, thereby resulting in contamination/doping of the electrolyte and alteration of deposited material properties.

iii. The cadmium telluride (CdTe) absorber layers utilised in this work have been known to have higher pinhole density when grown directly on transparent conducting oxide (TCO) such as FTO as compared to CdTe grown on cadmium sulphide (CdS) with minimum pin-hole formation.

1.7 Photon energy

Solar radiation comprises of elementary particles known as photons. A photon can be described as a discrete bundle (or quantum) of electromagnetic (or light) energy. A photon is characterized either by its wavelength (λ) or by its equivalent energy (E). Photon energy (E) can be related to its frequency by the Equation 1.1 and Equation 1.2.

$$E = hf \qquad \qquad \text{Equation 1.1}$$

where E (J) is the photon energy, h is the Plank's constant given as 6.626×10^{-34} Js, f is the frequency measured in hertz (Hz), c is the speed of light given as 2.998×10^8 ms^{-1} and λ is the wavelength.

$$E = \frac{hc}{\lambda} \qquad \text{Equation 1.2}$$

The relationship expressed by Equation 1.2 shows that light having low energy photons (such as "red" light) has a long wavelength while light having high energy photons (such as "blue" light) have a short wavelength.

Evaluation of the numerator expression in Equation 1.2 gives, $hc = 1.99 \times 10^{-25}$ Jm. With the appropriate unit conversion, hc can also be written as:

$$hc = \left(1.99 \times 10^{-25}\, \text{Jm}\right) \times \left(\frac{1\,\text{eV}}{1.602 \times 10^{-19}\,\text{J}}\right) = 1.24 \times 10^{-6}\, \text{eVm}$$

Further, to convert the unit to nm (the units for λ):

$$\left(1.24 \times 10^{-6}\, \text{eVm}\right) \times \left(10^{9}\, \text{nm/m}\right) = 1240\, \text{eV nm}$$

Therefore, Equation 1.2 can be re-written as:

$$E = \frac{1240}{\lambda} (\text{eV}) \qquad \text{Equation 1.3}$$

1.8 Photovoltaic timeline and state of the art

The photovoltaic effect was first observed in 1839 by Alexandre-Edmond Becquerel on semiconductor materials. Other groups such as Daryl Chapin et al. from the Bell laboratories in 1954, Hoffman Electronics Corporation in 1960, etc. have all contributed to the development of PV solar technology. The increase in research and development in alternative energy generation technology was primarily due to the oil crisis in the 1970s. The importance of solar energy cannot be over emphasized, as its importance was been lauded in a scientific article as far back as 1911 with a catching caption, which reads, "*in the far distant future, natural fuels having been exhausted, "solar power" will remain as the only means of existence of the human race*" [33]. At present, the need for high-efficiency PV systems and reduction in the $/Watt cost is highly essential for the world's ever-growing population and demand for energy to achieve sustainability. Towards achieving this task, a few of the landmarks by researchers and industries within the PV community are being captured in Table 1.1.

Table 1.1: Timeline of photovoltaic solar energy technology [16].

Year	Events
1839	Discovery of PV by Edmund Becquerel when he was 19 years old.
1883	Charles Fritts developed the first solar cell using elemental selenium as the light absorbing material.
1916	Robert Millikan experimentally proved photoelectric effect.
1918	Jan Czochralski developed a method in which single crystal silicon can be grown.
1923	Albert Einstein won the Nobel Prize for explaining the photo-electric effect.
1954	4.5% efficient silicon solar cells were produced at Bell laboratory.
1959	Hoffman Electronics produced 10% efficient silicon cells and was launched with PV array of 9600 cells.
1960	Hoffman Electronics produced 14% efficient silicon solar cells.
1970s	The first oil crisis gave a kick-start to search for low cost alternative systems for terrestrial energy conversion, accelerating PV research activities.
1980s	Thin film CdTe and $CuInGaSe_2$ (CIGS) solar cells were introduced into the mainstream of PV research.
1990s	Dye Sensitised Solar Cell (DSSC) or "Grätzel Solar Cell" was introduced.
2000s	Organic solar cells were introduced to the PV field.
2013	First Solar produced 16.1 % efficiency for small area solar cell using Thin Film CdTe.
2014	First Solar produced 20.4 % efficiency for small area solar cell using Thin Film CdTe.
2015	First Solar produced 21.5 % efficiency for small area solar cell using Thin Film CdTe.
2016	First Solar produced 22.1 % efficiency for small area solar cell using Thin Film CdTe.

Other notable solar cell efficiencies documented in the literature include: Si (crystalline) at 25.7%, gallium indium phosphide (GaInP) at 21.4%, copper indium gallium di-selenide (CIGS) thin-film at 22.6%, copper zinc tin sulphide selenium (CZTSS) thin-film at 12.6%, copper zinc tin sulfide (CZTS) thin-film at 11.0%, perovskite thin-film at 22.1% and organic thin-film at 12.1% [34].

1.9   Research aims and objectives

The motivation for the work reported in this thesis is based on previously proposed and experimented model by Dharmadasa in 2002 [15,35], with a record conversion efficiency of 18% for the CdTe-based solar cell at the time. The main feature of the

work reported by Dharmadasa's group was the *n-n*-heterojunction +large Schottky barrier configuration. The present work aims to incorporate a similar architecture and improve the conversion efficiency using graded bandgap device structures and low-cost electroplated (ED) semiconductor materials from aqueous solutions. The semiconductor materials explored in this thesis include CdS and CdTe while the effect of in-situ doping of CdTe with Cl, F, I and Ga was also investigated and reported [36–41]. The exploration of the semiconductor material involves the optimisation of the material layers through the study of their structural, compositional, optical, morphological, and electrical properties using available facilities in the Material and Engineering Research Institute at Sheffield Hallam University (MERI-SHU). Other semiconductor materials such as ZnS and ZnTe were outsourced from other scholars within the research group. The effect of post-growth treatment (PGT) using $CdCl_2$, $CdCl_2+CdF_2$ and $CdCl_2+Ga_2(SO_4)_3$ treatment on the structural, optical, morphological properties of the electrodeposited layers and device performances of the fabricated solar cells were also explored and reported [42–44]. In this research program, both the investigated and the outsourced semiconductor layers were incorporated into different graded bandgap configurations and reported [22,24].

The distinct feature of this research work includes;

i. The use of thiourea ($SC(NH_2)_2$) as the sulphur (S) precursor for electrodeposited CdS to prevent sulphur precipitation in the electrolytic bath [36].

ii. The use of cadmium nitrate ($Cd(NO_3)_2$) as a precursor for CdTe due to the scarce literature in the electrodeposition PV field.

iii. Incorporating $GaCl_3$ into the well-established $CdCl_2$ post-growth treatment [42–44], in-situ doping of CdTe in an aqueous electrolytic bath [36–41].

iv. The exploration of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration [24].

Figure 1.6 shows the outline of the work reported in this thesis, but the research objectives are as follows:

i. Growth and optimisation of electrodeposited semiconductor materials (CdS and CdTe) from aqueous electrolytic baths using 2-electrode configuration.

ii. Obtaining suitable deposition voltage range for the semiconductor layer deposition from cyclic voltammetric data.

❖ Optimisation and study of layers are performed through the study of the structural, compositional, morphological, optical, and electrical properties of the ED-CdS, and ED-CdTe layers using X-ray diffraction (XRD), Raman spectroscopy, Scanning electron microscopy (SEM), UV-Vis spectroscopy, Photoelectrochemical (PEC) cell and Solar simulating system. All the itemised equipment are available in Material and Engineering Research Institute at Sheffield Hallam University (SHU).

iii. Doping and study of the effect of in-situ doping of CdTe with Cl, F, I and Ga.

iv. Study of the effect of post-growth treatment (PGT) using $CdCl_2$, $CdCl_2+CdF_2$ and $CdCl_2+Ga_2(SO_4)_3$ treatment on the structural, optical, morphological properties and device performance of the fabricated solar cells.

v. Fabrication of solar cell devices incorporating the basic glass/FTO/*n*-CdS/*n*-CdTe heterojunction +large Schottky barrier (SB) at *n*-CdTe/metal interface and other configurations including glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au, glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au, and glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/*p*-CdTe/Au were explored.

vi. Assessment of the efficiency of the fabricated thin film solar cells using current-voltage (I-V) measurement and developing these devices by optimisation of all processing steps to achieve highest possible efficiency. Device parameters were also assessed using capacitance-voltage (C-V) measurements.

1.10 Conclusions

This chapter presented in brief, the increasing demand for energy and the significance of renewable energy sources as well as the detrimental effect of conventional (non-renewable) energy sources. Amongst renewable energy sources, the enormity of solar energy, its origin and influence of air mass (AM) on the solar energy were discussed. The technology for harvesting solar energy with emphasis on photovoltaic solar cell and its timeline was also iterated. The last section of this chapter presents the aims and objectives of this research program.
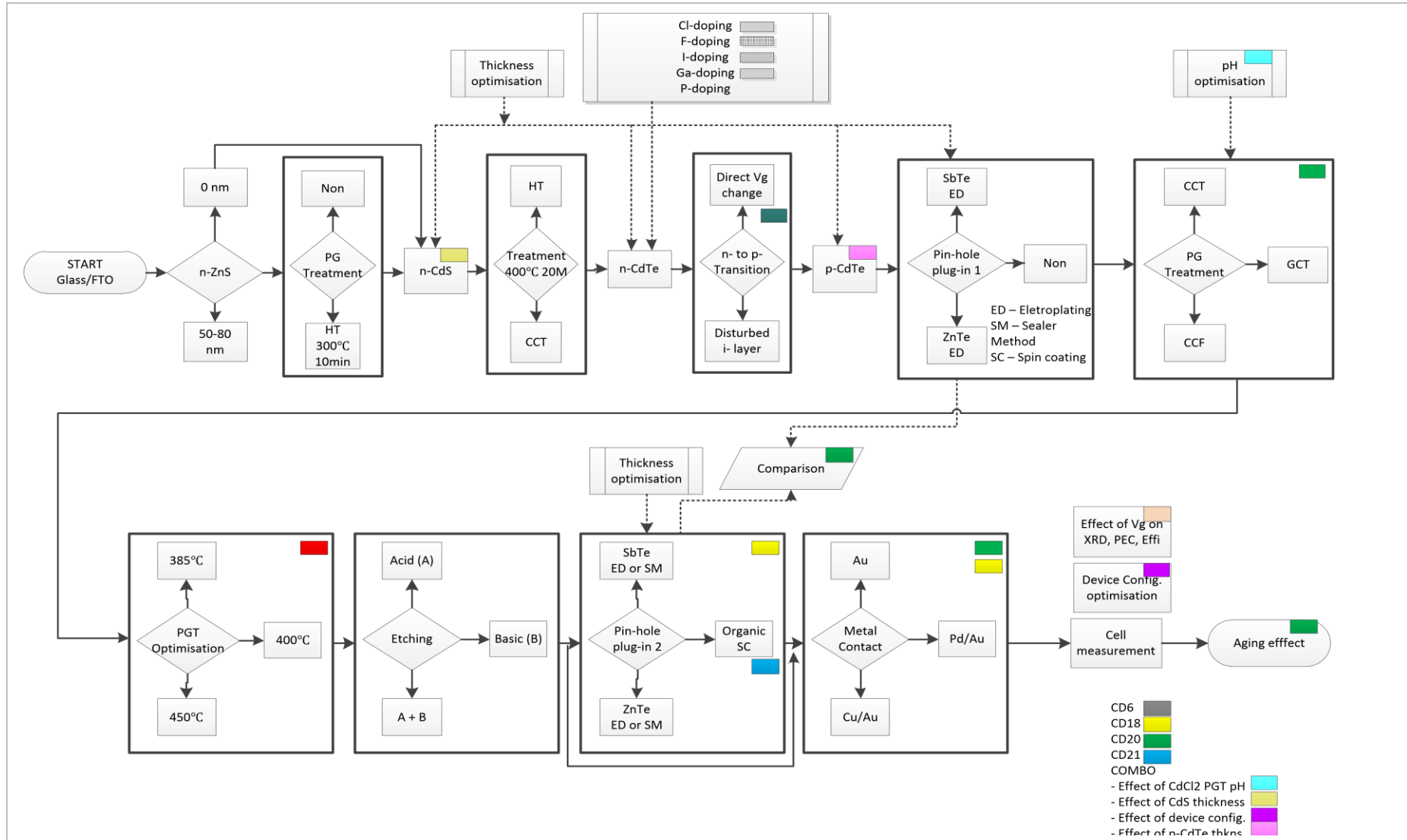
Figure 1.6: Outline of the work reported in this thesis.

Chapter 2 -   Photovoltaic solar cells – Materials, Concepts and Devices

2.1   Introduction

This chapter focuses on the review of the literature and the science background of solar energy materials and solar cells. The various classifications of solid state materials and the physics of junctions and interfaces in solar devices will be discussed. The main categories of solar cells will be presented in brief coupled with a general overview of next-generation solar cells.

2.2   Solid state materials

The prominent property peculiar to the classification of solid state materials is their bandgap (E_g) as determined by the interatomic interaction resulting into valence band (E_v) and conduction band (E_c) energy states as defined by the Band theory [45]. Unlike the Bohr's model of isolated atoms which exhibit discrete energy levels (or shells) and their electron configuration is determined by atomic number [46], the Band theory defines the interaction between multiple atoms in which the discrete energy shells broaden into energy bands. The outermost shells of the atoms (with their various subshells) which are more loosely bound to respective nuclei merge to form more available energy levels where the electrons can move about. Increase in the number of atoms leads to the formation of discrete energy bands with energy levels that can be occupied by electrons separated by gaps in which there can be no electrons. The ease at which electrons can move between bands under the influence of excitation energy is determined by the band gap between the bands.

Figure 2.1 (a), Figure 2.1 (b) and Figure 2.1 (c) shows the schematic band diagrams of a conductor, semiconductor, and an insulator respectively. The conduction band (*CB*) is the electron-empty energy band and E_c is the lowest level of *CB* while the valence band (*VB*) is the allowed energy band that is filled with electrons at 0 K [45,47] and the top of the *VB* is labelled E_v. For conductors (Figure 2.1 (a)) such as metals, the *CB* overlaps with the *VB* which is partially filled with electrons. Due to the overlap and the partially filled band with electrons, electrons move freely and require no external excitation to be promoted to the E_c [45]. Therefore the material possesses high conductivity attributable to the presence of conduction electrons contributing to current flow.

For both semiconductors and insulators, as respectively shown in Figure 2.1 (b) and Figure 2.1 (c), their conduction bands are empty of electrons, valence bands are filled with electrons and there exists a gap in between their E_v and E_c at 0 K [45,47]. Due to the small energy gap in between the E_c and E_v for semiconductors, an introduction of external excitation energy such as photons or thermal agitation at room temperature can promote electrons from the E_v to the E_c leaving behind some unoccupied states known as holes. But for insulators, the bandgaps are large, making it difficult for electrons to be promoted from the E_v to E_c. Therefore, their *VB* s are full of electrons and *CB* s are empty resulting in low electrical conductivity.
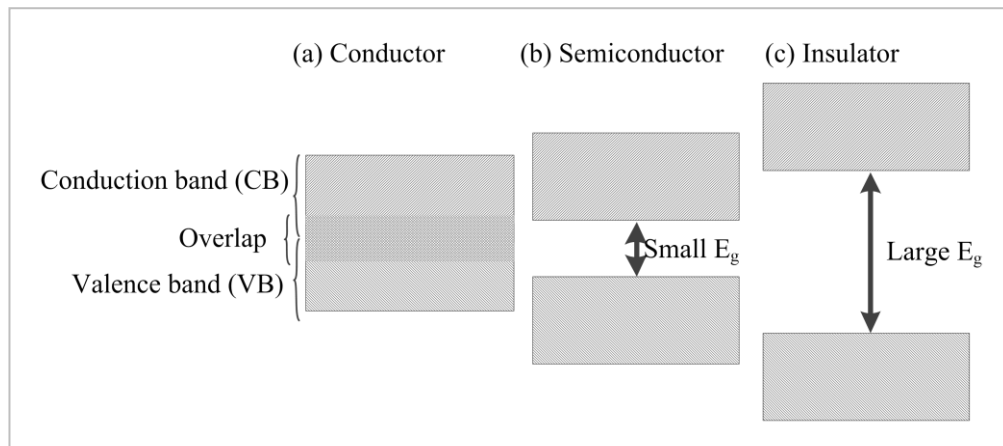
Figure 2.1: Energy band diagrams of (a) a conductor (b) a semiconductor and (c) an insulator.

Further to the classification of solid state material according to the energy bandgap (E_g), the electrical conductivity (σ) property can also be utilized [16,48] (see Table 2.1).

Table 2.1: Summary of main properties of different classes of solid state materials.

Parameter	Electrical conductors	Semiconductors	Electrical insulators
Electrical conductivity σ $(\Omega\ cm)^{-1} \equiv S$	~10^6 - 10^0	~10^0 - 10^{-8}	~10^{-8} - 10^{-20}
Bandgap E_g (eV)	≤ 0.3	~$0.3 - 4.0$	>4.0

2.2.1   Semiconductor materials and their classification

Semiconductor materials are usually solid-state chemical elements or compounds with properties lying in between that of a conductor and an insulator [47]. As shown in Table 2.1, they are often identified based on their electrical conductivity (σ) and bandgap (E_g)

within the range of ~(10^{-1} to 10^{-8}) (Ωcm)$^{-1}$ and ~(0.3 to 4.0) eV respectively [16]. Furthermore, semiconductor materials can also be classified based on their band alignment, elemental composition and dopant incorporation as respectively discussed in Sections 2.2.1.1 to 2.2.1.3.

2.2.1.1   Classification based on band symmetry

Classification of semiconductors can be based on the alignment of electron momentum (p) of the minimum energy difference between the bottom of the conduction band E_c and the top of the valence band E_v. Figure 2.2 (a) and Figure 2.2 (b) show the schematic diagrams of energy-momentum (E-k) plots for the direct and indirect bandgap semiconductor respectively.
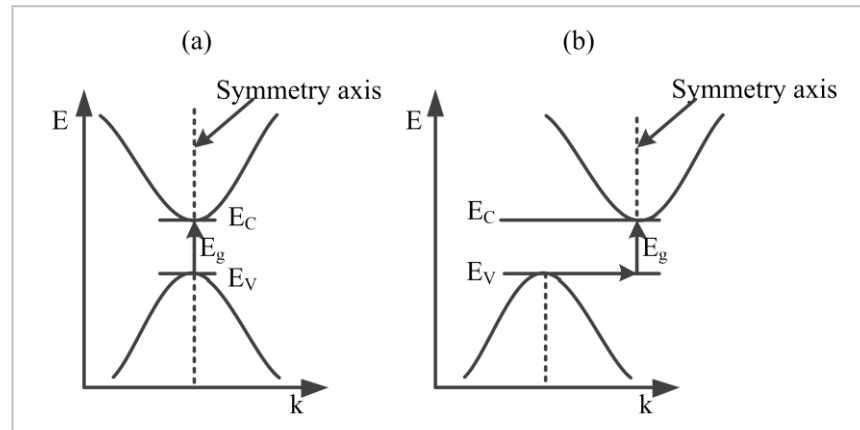
Figure 2.2: Schematic plot of E-k for (a) direct bandgap semiconductor and (b) indirect bandgap semiconductor.

Classically, the force on each charge carrier $F=m^*a$, (where m^* is the effective mass of electron or hole involved in the transition, a is the acceleration and v is the velocity). The momentum vector k of a charge carrier can be approximated from the kinetic energy E of the charge carrier as defined in Equation 2.1.

$$E = \frac{1}{2}m^*v^2 \qquad\qquad \text{Equation 2.1}$$

$$\text{where } p = m^*v \qquad\qquad \text{Equation 2.2}$$

Therefore, Equation 2.1 can be rewritten as Equation 2.3

$$E(k) = \frac{p^2}{2m^*} \qquad\qquad \text{Equation 2.3}$$

or Equation 2.4 [47,49] as redefined by de Broglie, where p equals $\hbar k$, $\hbar$ is the reduced Plank's constant defined as ($h/2\pi$) and k is the wave vector which equals ($2\pi/\lambda$).

$$E(k) = \frac{\hbar^2 k^2}{2m^*}$$ Equation 2.4

For direct bandgap semiconductors, both the conduction band minima and the valence band maxima occur at the same crystal momentum. This implies that an electron at the top of the valence band can move to the bottom of the conduction band if it possesses sufficient energy, without any change in its momentum vector [47,49]. Thus, an energized electron moves with a single effective mass (m^*) along the symmetry axis and thereby momentum is conserved. Semiconductors in this category include ZnS, CdS, CdTe, etc. Contrarily, the conduction band minima and the valence band maxima occur at different crystal momentums for indirect bandgap semiconductor materials. This is consequential to a change in the momentum of the energized electron moving from the top of the valence band to the bottom of the conduction band. Thus, the involved energized electron will have two effective masses m_l^* and m_t^* which will respectively be longitudinal and transverse with respect to the symmetry axis as shown in Figure 2.2 (b). Phonons (a quantum of lattice vibration) which fundamentally possess a significant amount of momentum and relatively low energy make up for the difference in momentum in indirect bandgap semiconductor [47,49]. This participation of phonons is necessitated for the conservation of both energy and momentum for a fundamental transition electron to be effected. Semiconductors in this category include Ge, Si, GaP, etc.

2.2.1.2   Classification based on elemental composition

As documented in the literature, semiconductor materials utilized in photovoltaic applications are mostly crystalline inorganic solids which lie between groups I and VI within the periodic table [16]. Based on elemental composition, semiconductor materials can be classified as elemental, binary, ternary or quaternary semiconductors (see Table 2.2).

Elemental semiconductors consist of a single element in group IV with typical examples including C, Si, and Ge. Other compound semiconductor materials such as the binary (III-V and II-VI), ternary and quaternary semiconductors are produced when two, three or four elements chemically react with one another respectively. In this research work,

all the semiconductor materials grown and explored belong to the binary (II-VI) semiconductor group.

Table 2.2: Summary of semiconductor elements and compounds available for use in photovoltaic applications.

Semiconductor family	Examples of Semiconductors
Elemental semiconductors	C, Si, Ge
III-V semiconductors	AlN, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb
II-VI semiconductors	ZnS, ZnSe, ZnTe, ZnO, CdS, CdSe, CdTe, CdO
Ternary compound semiconductors	$CuInSe_2$ (CIS), $Cd_xMn_{(1-x)}Te$ (CMT), $Cd_xHg_{(1-x)}Te$, $Al_xGa_{(1-x)}As$
Quaternary compound semiconductors	$CuInGaSe_2$ (CIGS), $AgInGaSSe_2$, $Cu_2ZnSnSSe_4$ (CZTS)

2.2.1.3   Classification based on dopants

Further to the classification of semiconductors based on band symmetry and elemental composition as discussed in Sections 2.2.1.1 to 2.2.1.2, semiconductors can also be classified based on incorporated impurities; intrinsic and extrinsic semiconductors. Pure or undoped semiconductor materials without any significant incorporation of external dopant species are referred to as intrinsic or i-type semiconductors [49]. For example, an elemental semiconductor material such as silicon (Si) has four valence electrons in its outermost shell which are utilised in the formation of covalent bonds with other Si atoms as shown in Figure 2.3 (a). Therefore, there are no free electrons in pure Si to partake in the flow of electric current. This results in reduced conductivity at absolute zero temperature. But with excitation energy equal or higher than the bandgap of the semiconductor, the only charge carriers are the electrons promoted to the E_c and the holes in the E_v that arise due to excitation of electrons to the E_c. Even in this state, the number of electrons in the E_c and the holes in the E_v are equal. For i-type semiconductor materials, the Fermi level is located in the middle of the bandgap as shown in Figure 2.3 (d). The Fermi level defines the highest energy state within the bandgap that has a 50% probability of being occupied by electrons in a semiconductor material at any given time at absolute zero temperature. It should be noted that the electrical conduction type of compound semiconductor materials as discussed in Section 2.2.1.2 can either be

dominated by intrinsic doping (based on the percentage composition of the elemental constituents [24]) or by intrinsic defect (resulting from Fermi level pinning [50]).
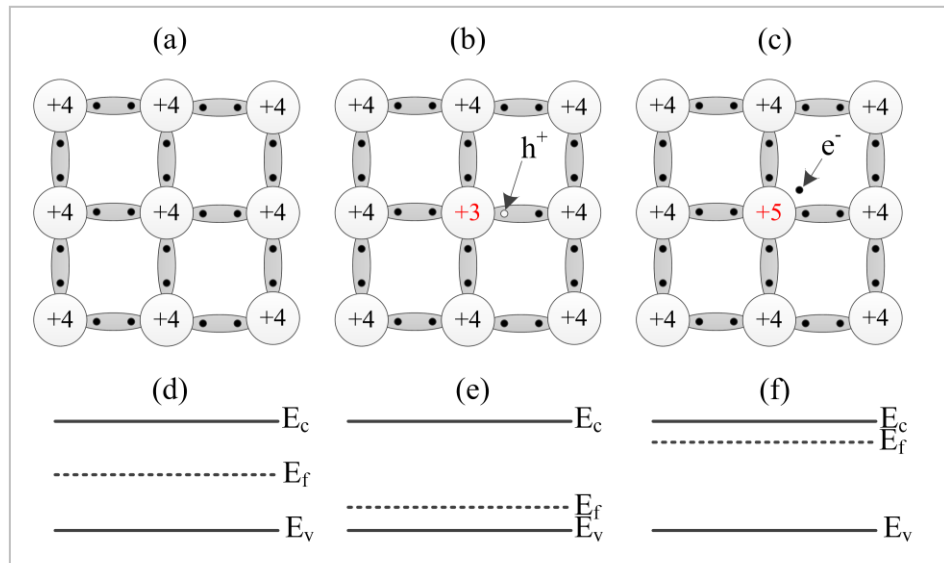
Figure 2.3: Schematic diagram of (a) intrinsic (b) p-doped and (c) n-doped semiconductor materials bonds. The band diagram of (d) intrinsic (e) p-doped and (f) n-doped semiconductor materials.

Extrinsic semiconductors are referred to as impure semiconductors due to the incorporation of external dopant element(s). The process or system of incorporating a suitable impurity into an intrinsic semiconductor in parts per million (ppm) level is referred to as doping. Depending on the included impurity, an extrinsic semiconductor can either be a *p*-type or an *n*-type semiconductor. It should be noted that the conductivity type of a semiconductor material is *p*-type provided holes are the majority carriers due to the inclusion of dopants from a group with lower valence electrons (acceptor impurity). And the conductivity type is *n*-type provided electrons are the majority carriers due to the inclusion of dopants from a group with higher valence electron (donor impurity). As shown in Figure 2.3 (b) and Figure 2.3 (c), doping Si which is a group IV element with a group III or group V element will result either in a *p*- or *n*- conductivity type due to the incorporation of excess holes or excess electrons respectively [49]. Therefore, the Fermi level for the *p*-type material is positioned close to E_v (see Figure 2.3 (d)) and that of the *n*-type materials is positioned towards E_c (see Figure 2.3 (e)). In addition to the effect of dopants on the conductivity type of a semiconductor, defects are also one of the principal factors which determine the Fermi level pinning position in the semiconductor material [51,52].

2.3   Junctions and interfaces in solar cell devices

Solar cell fabrication involves the formation of junctions between two or more semiconductors or between semiconductors and insulators or metals when brought in close contact with one another. As documented in the literature, the nature of the contact or junction formed is significant to the strength of the electric field, charge carrier creation and separation, pinning of the Fermi level and the formation of either an Ohmic or a rectifying (Schottky) contact. This section focuses on the types of the junction formed, their properties and their applicability in solar cells.

2.3.1   Homojunction and heterojunction

Junction formation in semiconductors can either be between layers of similar semiconductor materials known as homojunction or between dissimilar semiconductor materials known as a heterojunction. Simple device configurations of both homojunction and heterojunction may be in the form of p^+-p, n-p or n-n^+ as demonstrated in the literature for solar cell device applications [27,49,53–55]. Furthermore, depending on the doping concentration of the semiconductor layers in contact, a junction can be considered as one-sided.

2.3.2   *p-n* and *p-i-n* junction

The *p-n* junction is regarded as the primary building block of most semiconductor application devices [47,49]. Figure 2.4 shows the schematic illustration and energy band diagram of *p-* and *n-* type a semiconductor material prior and after *p-n* junction formation. As shown in Figure 2.4 (a) and Figure 2.4 (c), a *p-n* junction is formed between suitable *p*-type and *n*-type semiconductor materials.

Due to the excess of holes and electrons present in *p*-type and *n*-type semiconductor materials respectively, when the semiconductors are in intimate contact, holes from the *p*-type material diffuse into the *n*-type material leaving behind negatively charged acceptor atoms, while electrons from the *n*-type material diffuse into the *p*-type material leaving behind positively charged donor atoms [47] (see Figure 2.4 (b)). The diffusion leads to Fermi level equalisation and band bending as shown in Figure 2.4 (d). Owing to the presence of accumulated positive ion cores in the *n*-type material and negative ion cores in the *p*-type material, further diffusion of charge carriers is halted and an electric field *E* is induced around the junction (*E=-dV/dx where V is the voltage and x is the distance between plates*), which is depleted of mobile carriers. This region is referred to as the depletion region (*W*) or space charge region. *W* is the summation of the distances

by which the depletion region extends into *p*-type (X_p) and *n*-type (X_n) semiconductors respectively. The supporting equations for the parameters are later discussed in Section 3.5.2.
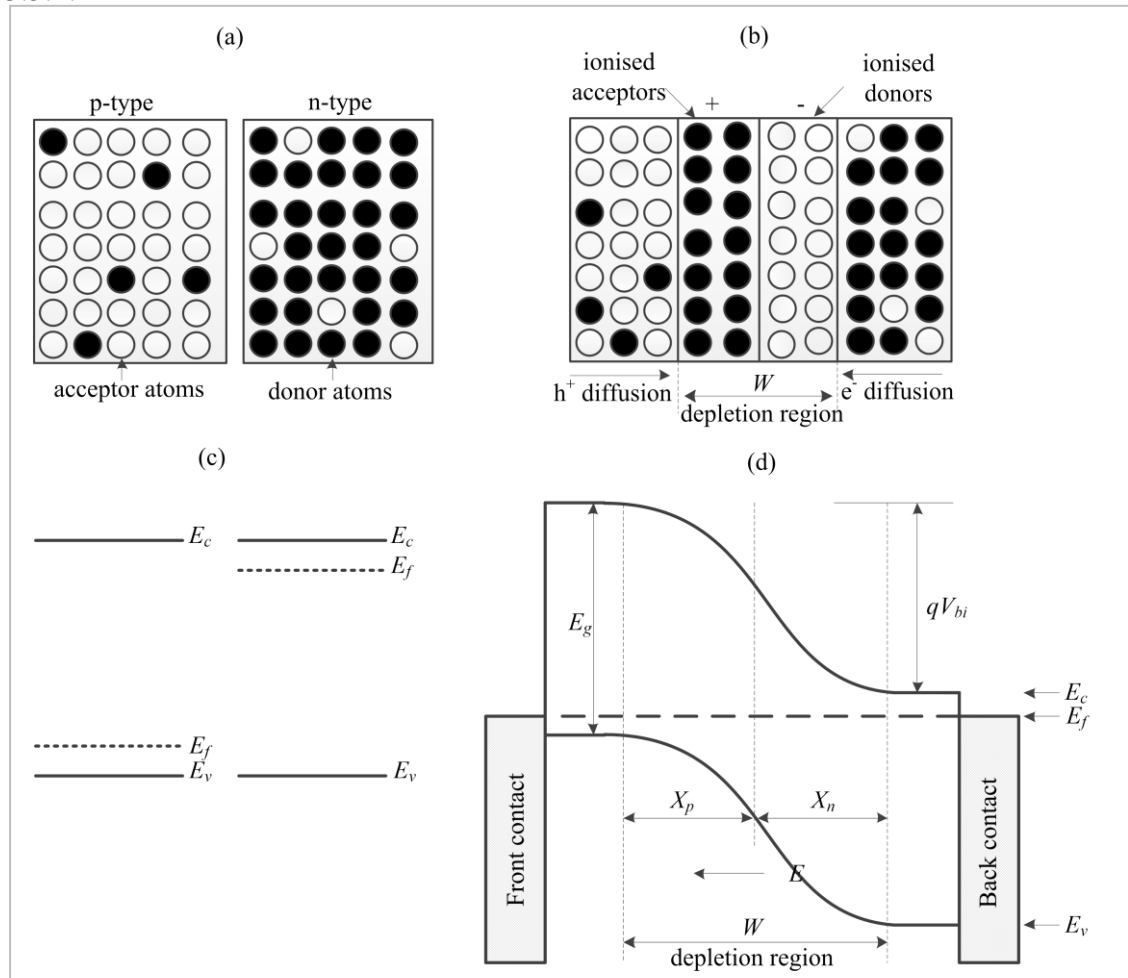
Figure 2.4: Schematic illustration of (a) *p*- and *n*- type material prior junction formation, (b) after *p-n* junction formation and energy band diagram of (c) *p*- and *n*-type semiconductor materials prior to the formation of *p-n* junction and (d) after close intimate contact formation.

The *p-i-n* junction configuration as shown in Figure 2.5 is a proceed of the *p-n* junction with a doping profile incorporating a sandwiched intrinsic (*i*-type) semiconductor layer in between *p*- and the *n*-type layers. The functionality of a *p-i-n* is similar to that of a *p-n* junction in which the Fermi levels of both the *p*- and the *n*-type semiconductors are aligned through the *i*-type material. Due to the complexity of fabricating intrinsic semiconductor materials [56], high resistive *p*- and *n*-type semiconductor materials with low doping concentration may be utilised since healthy depletion is dependent on the doping concentration of the semiconductor materials in contact. The incorporated *i*-type semiconductor controls the depletion width depending on its application [16,57]. For

applications such as photovoltaic devices, the incorporation of a wide *W* is essential for effective creation and separation of charge carriers, but an optimisation of *W* is vital due to a reduction in the electric field; *E=-dV/dx*.
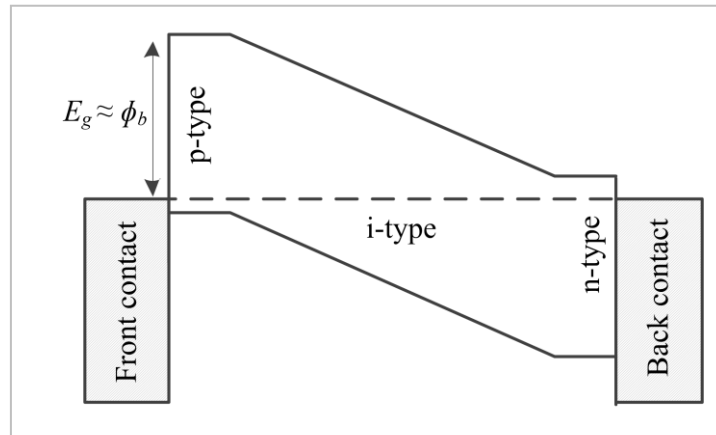
Figure 2.5: Energy band diagram of a *p-i-n* junction device.

Furthermore, the merit of this configuration includes the ability to achieve a high potential barrier ϕ_b close to the band gap of the semiconductor material [16] which is synonymous to achieving high open-circuit voltage (V_{oc}). The advantages of the *p-i-n* structure have been reported in the literature [16,57].

2.3.3   *p-p$^+$* and *n-n$^+$* junction

As discussed in Section 2.3.1, the formation of *p-p$^+$* or *n-n$^+$* junctions may either be homojunction or heterojunction configuration depending on the semiconductor materials in contact. Figure 2.6 shows the band diagram of *p-p$^+$* and *n-n$^+$* junctions.
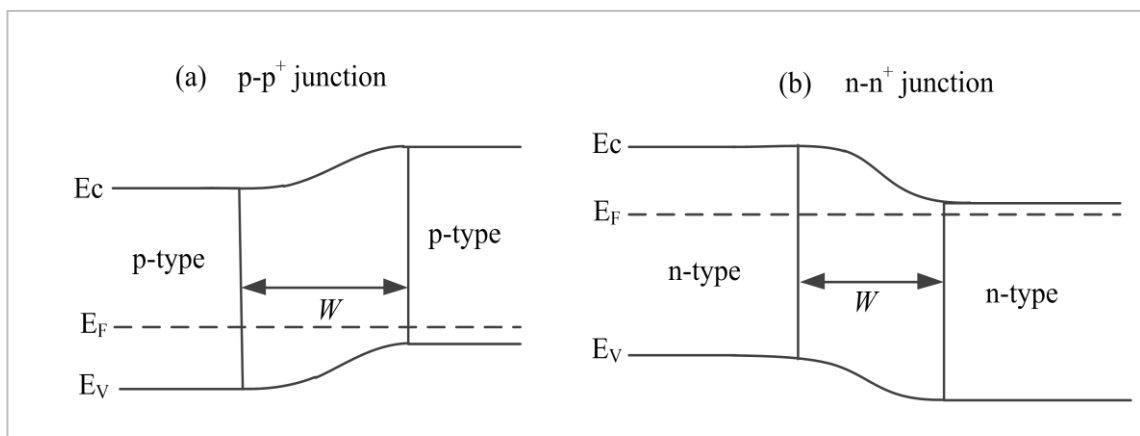
Figure 2.6: Band diagrams of *p-p$^+$* and *n-n$^+$* junctions.

The observable characteristic of such junctions is a small potential step (low barrier height). The incorporation of such configuration has been reported in the literature [27,58] to give comparatively high photon to electron conversion.

2.3.4   Metal-Semiconductor (M/S) interfaces

As previously discussed in Section 1.6, one of the prerequisites of effective photovoltaic energy conversion includes efficient transportation of the charge carrier through the external circuit [16]. For this to be achieved, at least two metal/semiconductor (M/S) contacts are required. Therefore selecting the appropriate metal contact with required M/S junction property is essential. Metal/Semiconductor junctions can either be a non-rectifying (Ohmic) or rectifying (Schottky) contact. Ohmic contact allows the flow of electric current in both directions across the M/S junction. The relationship between the current and voltage across the junction is linear (obeys Ohm's law). Conversely, Schottky contact does allow current flow only in one direction across the junction [59]. Notable parameters in the annotation of M/S contact includes the work function of the metal in contact (ϕ_m), the work function of the semiconductor (ϕ_s) and the electron affinity of the semiconductor (χ_s). The work function (ϕ) is defined as the minimum energy required to remove an electron to infinity from the surface of a given solid state material. On the other hand, the electron affinity (χ) is defined as the amount of energy released or spent when an electron is added to a neutral atom [49].

2.3.4.1   Ohmic contacts

Ohmic contacts are M/S contacts that possess negligible contact resistance relative to the bulk semiconductor resistance [49]. The formation of Ohmic contact is dependent on the relative energy difference (or barrier height ϕ_b) between the work function of the metal in contact (ϕ_m) and the electron affinity of the semiconductor (χ_s). With ϕ_b less than 0.4 eV [16], Ohmic contacts exhibit narrow depletion region and negligible/non-rectifying capabilities. Figure 2.7 (a) and Figure 2.7 (b) show the energy band diagrams of a metal and p-type semiconductor before and after intimate contact where $\phi_m > \phi_s$ and Figure 2.7 (c) and Figure 2.7 (d) show that of metal and n-type semiconductor where $\phi_m < \phi_s$.

For thermal equilibrium to be achieved between the p-type semiconductor and the metal as shown in Figure 2.7 (a) and Figure 2.7 (b), electrons flow from the p-type semiconductor into the metal whereby increasing the hole concentration of the p-type semiconductor material [47]. Under forward bias condition, holes produced in the p-

type semiconductor can easily tunnel through into the metal from the semiconductor due to non-existence or minimal effect of the depletion region formed at the M/S junction.
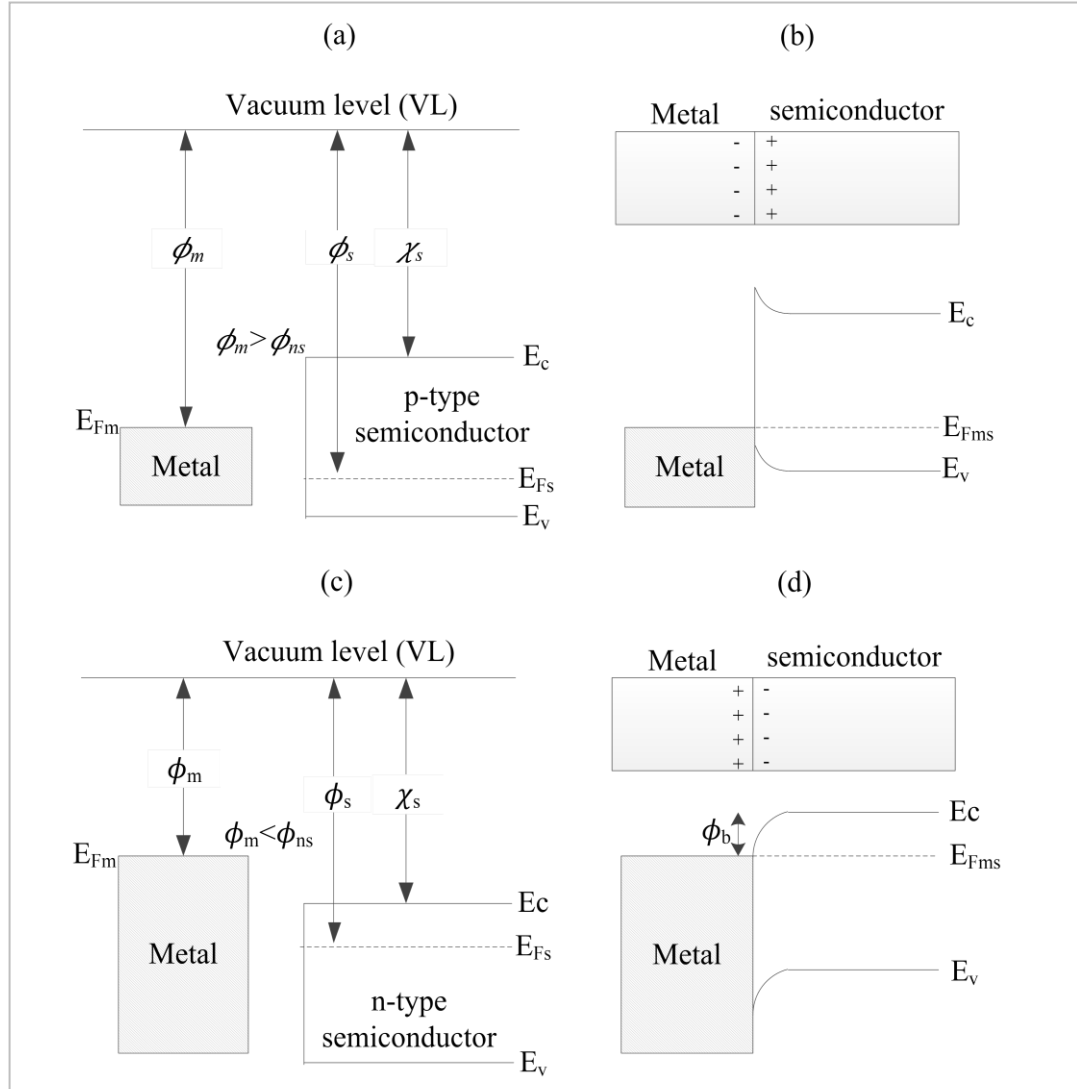
Figure 2.7: Energy band diagrams showing the formation of Ohmic contact between both *p*- and *n*-type with appropriate metal.

On the contrary, for thermal equilibrium to be achieved between the *n*-type semiconductor and metal as shown in Figure 2.7 (c) and Figure 2.7 (d), electron flow from the metal to the semiconductor and increases the electron concentration of the *n*-type semiconductor [47]. Under forward bias condition, electrons flow freely from the semiconductor to the metal due to the absence of any barrier. Under reverse bias condition, the electrons flow from the metal to the semiconductor encounter a barrier $\phi_b=(E_c-E_{Fms})$ as shown in Figure 2.7 (d). But due to the low barrier, electrons can still flow across. It should be noted that the analogy given above is under ideal conditions,

complexities due to surface states at the M/S junction or intrinsic defect [52,60,61] may cause the Fermi level to pin at an energy level whereby V_{bi} >0 V, independent of the metal work function ϕ_m.

Alternatively, Ohmic contact can be achieved by heavily doping the semiconductor material directly in contact with the metal [49]. The heavy doping of the semiconductor decreases the width of the depletion region, which increases the tunnelling probability of electrons through the barrier [49]. In other words, tunnelling becomes the dominant mechanism for current transport across the barrier and this allows the flow of electrical current in both directions with linearity between current and bias [45]. The current transport mechanism in M/S junctions will be further discussed in Section 2.3.4.3.

2.3.4.2 Rectifying (Schottky) contacts

Rectifying contact is achieved between a semiconductor and metal when the potential barrier height ($\phi_b=\phi_m-\chi_s$) is more than 0.40 eV [16]. Consequently, a depletion region extending reasonably into the semiconductor is formed provided there exist a substantial difference between the work function of both the semiconductor (ϕ_s) and the metal (ϕ_m) in contact. The formation of a Schottky barrier between a *p*- or an *n*- semiconductor with metal requires that $\phi_m<\phi_{sp}$ or $\phi_m>\phi_{sn}$ respectively which is unlike the Ohmic contact. Figure 2.8 shows the energy band diagrams for the formation of a Schottky barrier between a metal and either an *n*-type or a *p*-type semiconductor before and after metal/semiconductor contact. For this type of metal/*n*-type semiconductor contact, electrons continuously flow from the *n*-type semiconductor to the metal due to the comparatively higher Fermi level of the semiconductor ($\phi_m>\phi_{sn}$). This continuously lowers the *n*-type semiconductor Fermi level as a result of the reduction in electron concentration and bends the band until an alignment with the metal work function is reached, and thermal equilibrium is established (Figure 2.8 (b)). Consequently, negative charges build-up at the metal surface and likewise positive charges build-up at the semiconductor surface near the junction. This creates an internal electric field (*E*) and a depletion region of width (*W*) [47] around the M/S interface where band bending takes place. A similar phenomenon is experienced for Schottky M/S contact formed between a metal and a *p*-type semiconductor. In this case, electron flows from the metal to the semiconductor until thermal equilibrium is achieved as shown in Figure 2.8 (c) and Figure 2.8 (d).
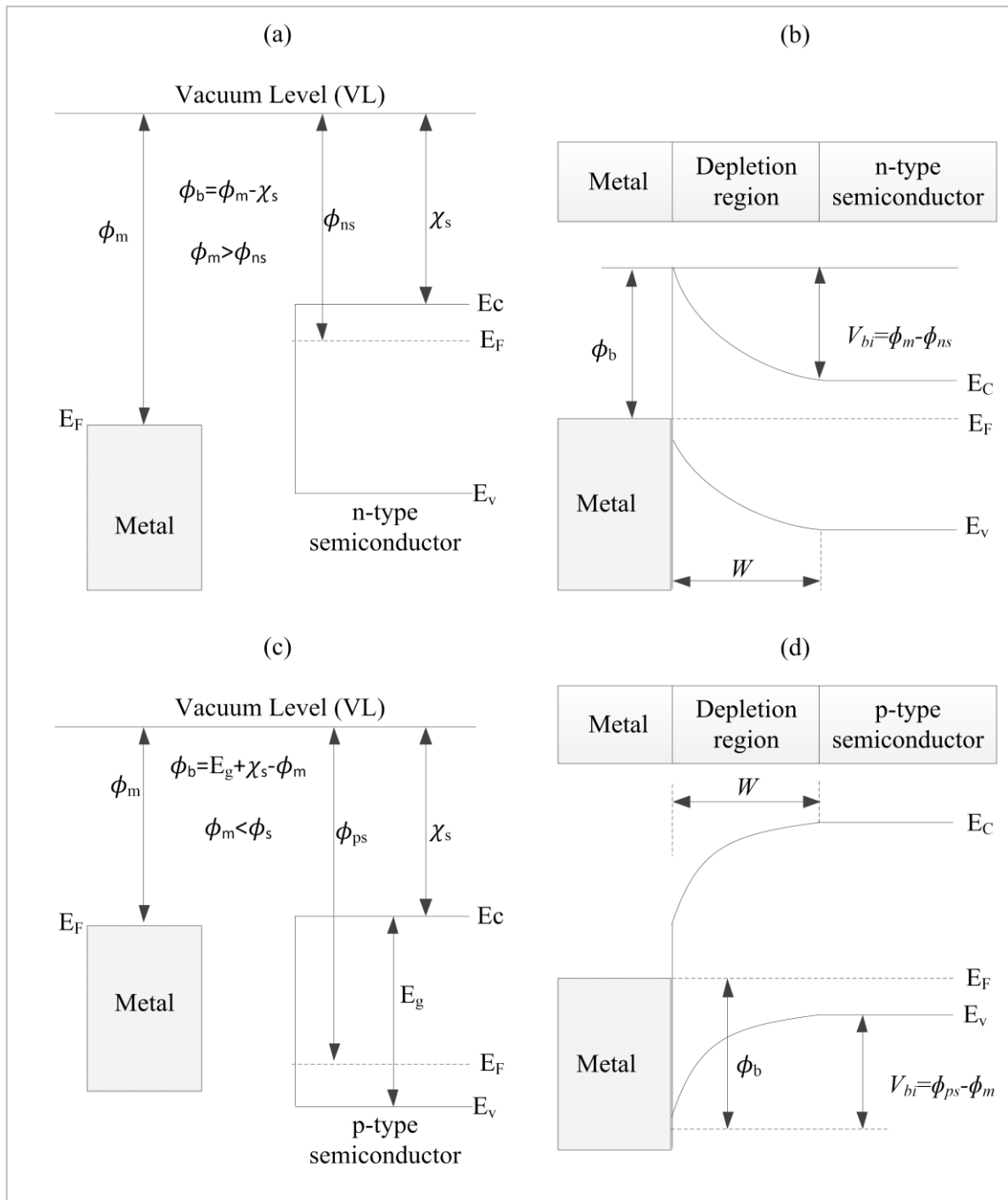
Figure 2.8: Energy band diagrams for the formation of Schottky barrier between a metal and a semiconductor. (a) Metal and *n*-type semiconductor before contact (b) after metal/semiconductor contact (c) metal and *p*-type semiconductor before contact and (d) after metal/semiconductor contact.

The built-in potential (V_{bi}) which prevents further diffusion of charge carriers across the depletion region and the barrier height (ϕ_b) of the metal/*n*-semiconductor Schottky contact can be mathematically defined as Equation 2.5 and Equation 2.6 respectively.

$$V_{bi} = (\phi_m - \phi_{ns})$$ Equation 2.5

$$\phi_b = (\phi_m - \chi_s)$$ Equation 2.6

While the V_{bi} and the ϕ_b of the metal/p-semiconductor Schottky contact can be mathematically defined as Equation 2.7 and Equation 2.8.

$$V_{bi} = (\phi_{ps} - \phi_m)$$ Equation 2.7

$$\phi_b = (E_g + \chi_s - \phi_m)$$ Equation 2.8

The ideal/theoretical narrative given above is quite different from practical applications due to complications associated with intrinsic defects, surface and interface states at the semiconductor/semiconductor (S/S) and M/S junctions [60,62,63]. Amongst such defects include interstitial and vacancy (dangling bond) [63] in the crystal lattice which are respectively due to transferred atom from the surface into the interstitial site and incomplete bonding, lattice mismatch between consecutively grown semiconductor materials, impurities, oxide film formation at the interface [64] amongst others. Hence the dominant mechanism determines the pinning position of the Fermi level which may be independent of the metal work function ϕ_m [59,62]. This observation has been documented in the literature for semiconductor materials such as CdTe, Cu(InGa)(SeS)$_2$ [52], GaAs, InP [65], Si [66] etc.

As documented in the literature, the defect region leads to the distribution of electronic levels within the forbidden bandgap at the interface as shown in Figure 2.9 (a). The surface state is characterised by a neutral state E_o [63]. The states above the E_o contain acceptor-like defects which are neutral when empty but obtains electrons to become negative. The donor-like defect states below E_o are neutral when full, release an electron and becomes positive [49,63,64]. It should be noted that all energy states below E_F are occupied by electrons. Therefore, for a bare semiconductor, electrons accepted by the acceptor-like defects are taken from the semiconductor - just below the surface. This result in a band bending until equilibrium is reached between the interface state charge Q_{it} and the depletion region charge Q_D even prior M/S contact [49]. Therefore Equation 2.6 can be rewritten as Equation 2.9 at high surface state density when E_F is pinned close to E_o.

$$\phi_b = E_g - \phi_o$$ Equation 2.9

Therefore, it is essential that defects are adequately controlled due to their contribution in Schottky barrier formation which could be beneficial as in the case of impurity PV effect [67] or detrimental because they constitute of trap centres for charge carriers [68].
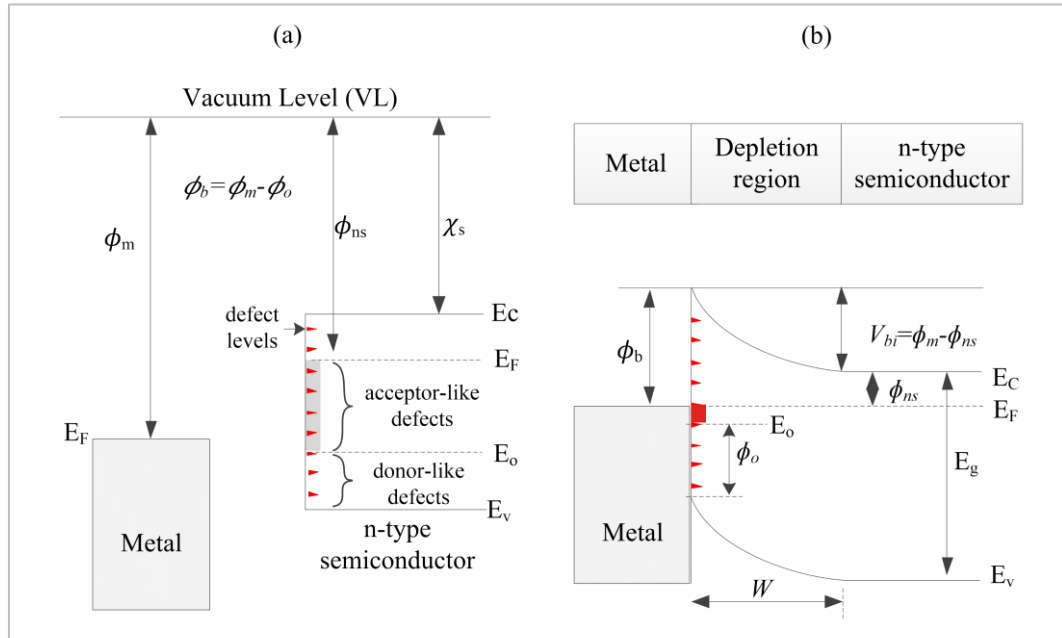
Figure 2.9: Energy band diagrams for the formation of Schottky barrier between a metal and a semiconductor. (a) Metal and *n*-type semiconductor before contact (b) after metal/semiconductor contact incorporating surface states.

2.3.4.3   Current transportation mechanism in rectifying contacts

As documented in the literature, the solar cells under illuminated condition are equivalent to forward bias condition [52,59]. Similarly for M/S junctions, the direction of electron flow under illuminated condition (reverse bias) and in dark conditions (forward bias) differs. Figure 2.10 (a) and Figure 2.10 (b) show the current transport mechanisms across Schottky junction under illuminated (or reverse biased) condition and under forward bias in dark conditions (or forward biased) respectively.

The current transport mechanisms across a forward biased Schottky barrier as shown in Figure 2.10 includes:

i.   Thermionic emission of electrons over the potential barrier of the semiconductor material into the metal. This is dominant for moderately doped semiconductor material with doping density $N \leq 10^{-15}$ cm^{-3}.

ii.   Quantum mechanical tunneling of electrons through the potential barrier. This is dominant for heavily doped semiconductor material which results in the thinning of the depletion region.

iii.   Recombination in the space-charge region.

iv.   Recombination in the neutral region due to hole injection from the metal into the semiconductor.
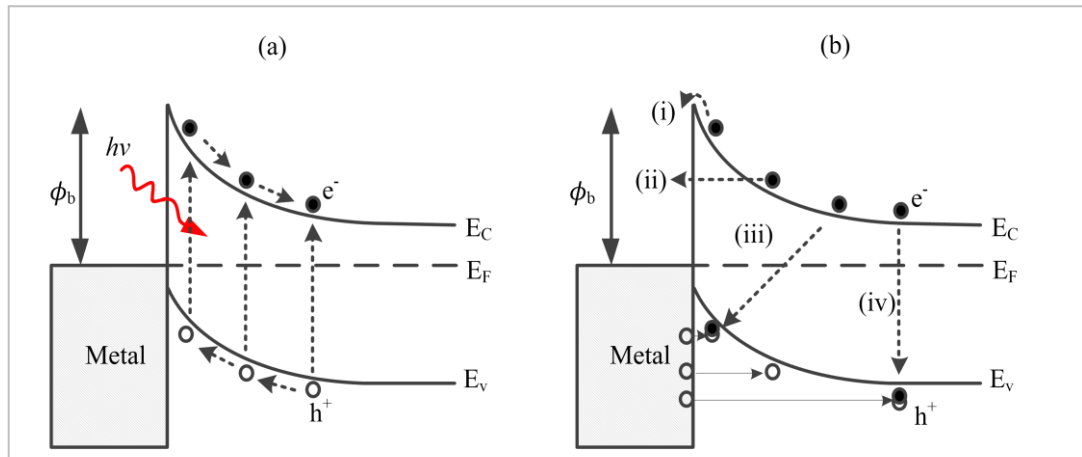
Figure 2.10: Current transport mechanisms across a Schottky junction under (a) illuminated condition (or reverse biased) and (b) dark condition (or forward biased).

For an ideal Schottky barrier diode, thermionic emission (the thermally induced flow of charge carriers over the potential barrier) is the preferred current transportation mechanism, while mechanisms (ii), (iii) and (iv) causes deviation from this ideal behavior [59,63]. The effect of this current transport mechanisms is further elaborated in Section 3.5.1.1.

2.3.5   Metal-Insulator-Semiconductor (MIS) interfaces

M/S Schottky devices are mainly characterised by comparatively lower barrier height (ϕ_b) and hence lower open circuit voltage (V_{oc}) as compared to *p-n* junctions [49,59]. The Schottky barrier represents approximately half of the *p-n* junction [16]. However, the barrier height of M/S junction can be increased close to the semiconductor bandgap by pinning the Fermi level close to the valence band and by the incorporation of an insulating layer in between the metal and the semiconductor interfaces as shown in Figure 2.11. The insulating layer with an optimum thickness δ ranging between (1 to 3) nm [49] decouples the metal from the semiconductor as shown in Figure 2.11. The incorporated i-layer eliminates the interface interaction between the metal and the

semiconductor, thereby improving the lifetime of the electronic devices by reducing the degradation of the electrical contact and increasing both the band bending and the potential barrier height. On the other hand, the incorporation of the i-layer may result in the reduction of device efficiency due to a decrease in short-circuit current density (J_{sc}) as a consequence of the increase in the series resistance (R_s). The increase in the *n*-value due to the insertion of the i-layer helps in increasing the V_{oc} of the device [49].
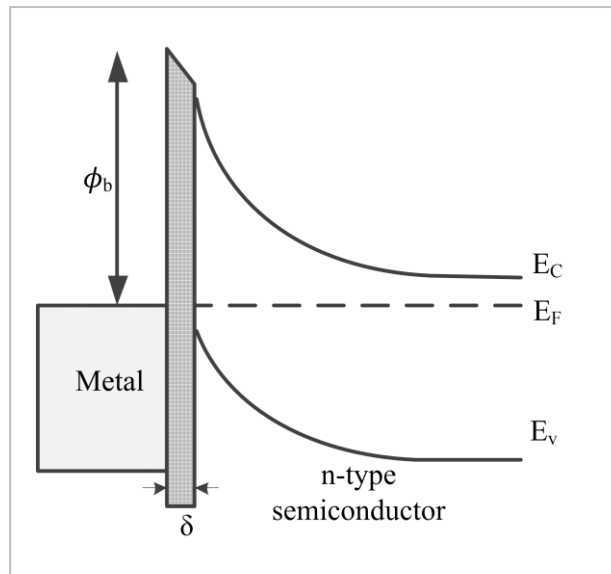
Figure 2.11: Energy band diagram of an MIS interface showing enhancement in potential barrier height due to incorporation of thin insulating layer of thickness, δ at the interface.

As reported in the literature, the i-layer may be an oxide layer [69,70] and might not be grown intentionally [64]. The fabricated solar cell devices as reported in this thesis are mainly based on the Schottky barrier structures with no intentional oxide layer formation.

2.4   Types of solar cells

Although, the basic functionality of a solar cell is photon to electron-hole (e-h) pair generation through photovoltaic effect, which is a physical and chemical phenomenon; the semiconductor material utilised (see Section 2.2.1) and the integrated technology is slightly different. This section discusses in brief, the underlining technology of different types of solar cells.

2.4.1   Inorganic solar cells

Inorganic materials such as silicon (Si) are by far the most researched, established and prevalent semiconductors in the photovoltaic market till date. So far, the highest efficiency solar cells have been fabricated using Si for terrestrial solar module [25]. Inorganic semiconductor materials used in photovoltaic includes mono and polycrystalline silicon, amorphous silicon, and other elemental, binary, ternary and quaternary compounds as discussed in Section 2.2.1.2 and shown in Table 2.2.

With crystalline silicon (c-Si) holding the dominant market share of photovoltaic cells, II-VI semiconductors such as cadmium telluride (CdTe) [71] is potentially one of the main rivals in cost/watt. The main setback of CdTe is the toxicity of cadmium (Cd) and a limited supply of tellurium (Te). But as argued in the literature, Cd which is a by-product of zinc, lead and copper is more stable and less soluble in CdTe compound form, impossible to release Cd during normal CdTe cells operation and unlikely to dissociate into its constituents during fires in residential roofs [71]. Therefore utilisation of Cd in CdTe compound form reduces its toxicity while generating renewable energy.

The basic functionality of inorganic materials is the absorption of photons which break bonds between atoms and create electron-hole pairs that are used for electricity generation.

2.4.2   Organic solar cells

Organic solar cells (OSC) are one of the developing technologies taking a niche at the dominance of Si-based solar cell due to properties such as reduction in the cost of production, the flexibility of solar module, reduced the thickness of PV material and can be fabricated using roll-to-roll production [72]. The main setback of OSC is that they are still mainly under investigation and lab-based devices due to their stability issues. The basic technology requires the incorporation of photoactive polymer in between metal contacts as shown in Figure 2.12.
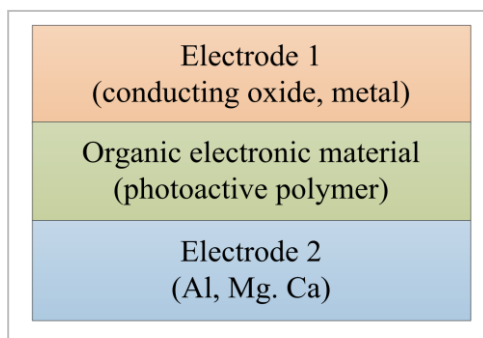
Figure 2.12: Schematic diagram of a single layer organic photovoltaic cell.

Unlike the inorganic solar cells in which the electric fields are generated at the rectifying junctions which separate the e-h pairs created by the absorption of photons with energy higher than the semiconductor bandgap, the electric field generated in the organic solar cell is due to the differences in the work function ϕ between the two electrodes. When the organic polymer layer absorbs photons, electrons will be excited to the lowest unoccupied molecular orbital (LUMO) or conduction band and leave holes in the highest occupied molecular orbital (HOMO) or valence band, thereby forming excitons [73]. The created potential due to the different work functions helps to split the exciton pairs, pulling electrons to the positive electrode and holes to the negative electrode.

2.4.3   Hybrid solar cells

Hybrid solar cells also known as organic-inorganic solar cells are another cheap alternative to the well-established inorganic solar cells such as Si-based solar cells. The hybrid solar cell is a combination of both organic and inorganic materials, and therefore it combines the unique properties of highly efficient inorganic semiconductors with the low-cost film forming properties of the conjugated polymers [74,75]. The main disadvantages of the hybrid solar cell include numerous surface defects, improper organic-inorganic phase segregation, comparatively low charge mobility due to the disordered orientation of organic semiconductor molecules, instability issues at high relative humidity, and lower efficiency as compared to established inorganic solar cells [76]. The basic materials utilised in the fabrication of hybrid solar cells include Si, cadmium compounds, metal oxide nanoparticles and low bandgap nanoparticles and carbon nanotubes (CNT) [77]. Examples of hybrid solar cells include dye-sensitised solar cell (DSSC) and perovskite solar cell which differs from each other due to the light absorber layer incorporated. Based on the new light absorber material in the solid

state sensitised solar cell (perovskite), the power conversion efficiency (PCE) has increased to 22.1% from 11.9% in DSSC [78]. Once the main issue of instability and lifetime of hybrid solar cells are rectified, they are believed to have a high commercial tendency to niche a substantial fraction of the photovoltaic market.

2.4.4   Graded bandgap solar cells

The basic concept behind graded bandgap (GBG) solar cell is the possibility of effective harnessing of photons across the ultraviolet (UV), visible (Vis) and infrared (IR) regions [14]. This concept has been validated in the literature across organic, inorganic [22,67] and hybrid [14,79] solar cell technology. Graded bandgap can be achieved by grading the absorber layer in such a way that the bandgap varies throughout the entire thickness [67]. GBG can also be produced by successively growing semiconductor materials on top of each other in which the layers are arranged such that the bandgap decreases gradually while the conductivity type gradually changes from one type to the other.

The earliest work that theoretically described the functionality of GBG configuration was reported by Tauc in 1957 [80]. His work elucidates the possibility of GBG solar cell configuration attaining higher conversion efficiency above the well-explored *p-n* junction cells stimulated interest in the photovoltaic research community. Taking into consideration the photogenerated current, it was theoretically proved that GBG solar cell configurations are capable of attaining a conversion efficiency of ~38% under AM1.5 [81,82] as compared to the 23% of single *p-n* junction solar cells. Based on this theoretical understanding, the first sets of graded bandgap cell were fabricated and reported in the 1970s [83,84] by gradual doping of *p*-type gallium arsenide (GaAs) with aluminium. The published works demonstrated a single-sided *p*-type grading of *p*-Ga$_{1-x}$Al$_x$As/*n*-GaAs solar cell. In 2002, the first model of full solar cell device bandgap grading was proposed and published by Dharmadasa et al. [15]. The graded bandgap (GBG) architectures as proposed by Dharmadasa et al. [14,35] can be facilitated by incorporating either an *n*-type or *p*-type wide bandgap front-layer with a gradual reduction in bandgap towards *p*-type or *n*-type back layer respectively as shown in Figure 2.13. The devices fabricated using the latter is more advantageous due to higher potential barrier height achievable [22]. The advantages of graded bandgap solar cells include;

i.   The possibility of harnessing photons across the solar spectrum (in the UV, Vis and IR region).

ii.   The reduction/elimination of thermalisation of "hot carriers" due to shared photon absorption at different regions of the solar cell.

iii.   The improvement of e-h pair collection due to the presence of electric field (or depletion width) spanning approximately throughout the entire thickness of the solar cell to reduce recombination and generation (R&G).

iv.   Incorporation of impurity PV effect and impact ionisation in GBG solar cell configuration to reduce R&G and further increase photo-generated current density [22,67].
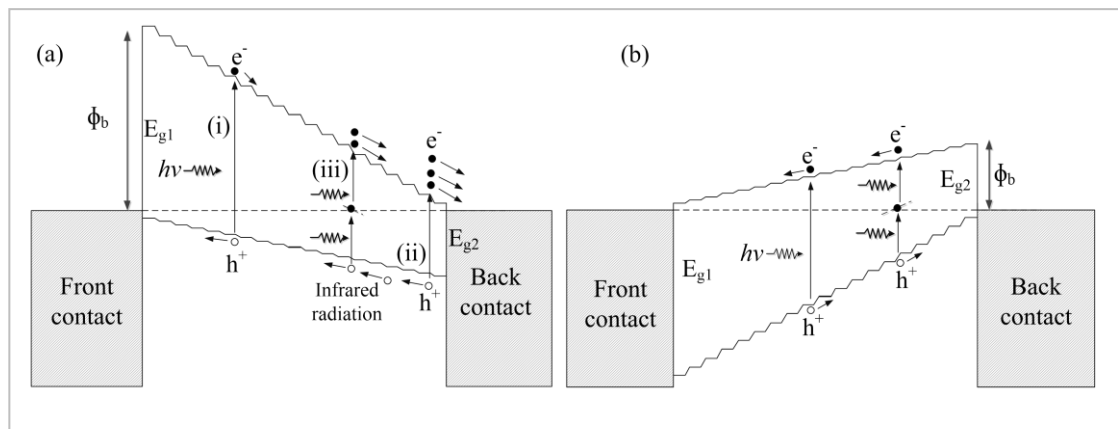
Figure 2.13: Schematic representation of graded bandgap solar cells based on (a) *p*-type window layer and (b) *n*-type window layer [14,79].

Further to the underlying operating principles of photovoltaic solar cells as discussed in Section 1.6, the e-h pair generated due to the absorption of high energy photons as shown in Figure 2.13 (a)-(i) is effectively separated by the strong built-in electric field spanning approximately the width of the device. The strong built-in electric field owing to the steep gradient produced as a result of the device architecture forces the electron to accelerate towards the back contact. Such electron moving at high kinetic energy (KE) may transfer its momentum to atoms located towards the rear end of the GBG device structure and break interatomic bonds, thereby creating additional e-h pairs as shown in Figure 2.13 (a)-(i). This mechanism is referred to as band-to-band impact ionisation. On the other hand, the low energy photon near and within the IR region propagate towards the rear end of the GBG device structure. The IR can also be involved in the creation of e-h pairs either directly by exciting the electron from the valence band (E_v) to the conduction band (E_c) or predominantly by promoting the electrons to the defect levels within the forbidden gap. The presence of defects at M/S junction as previously

discussed in Section 2.3.4 can be positively utilised if adequately controlled [67]. The present defect may have been the naturally existing defects within the material. The recombination of the e-h pair by IR photons are avoided due to the immediate transfer of its paired hole as a result of the strong electric field in the GBG. Therefore, the electron becomes trapped in the defect level until further absorption of IR photon to promote the electron to the conduction band. The newly excited electron can push the initially excited electrons at one of the defect levels to a higher defect level or to the E_c. This mechanism is known as impurity PV effect [67,85] (see Figure 2.13 (a)-(iii). Further to this, there is a possibility of having both impact ionisation and impurity PV effect mechanisms function in unison. This is achieved by the transfer of momentum from high KE electron accelerating to the GBG device rear end to promote the trapped electron in the defect level during impurity PV effect. The combination of both impact ionisation and impurity PV effect results in an avalanche effect during this process.

The downside to bandgap grading in GBG solar cells includes high technicality required in growth, the unpredictability of layer characteristic after post-growth treatment amongst others.

2.5   Next generation solar cell overview

The competitiveness of solar cells lies within its conversion efficiency while its economic viability is determined by its production cost. Semiconductor deposition techniques such as electrodeposition matches the economic requirements provided efficient solar cells can be fabricated using the technique. Improvements of CdS/CdTe solar cells after about two decades of stagnation has been achieved through better understanding of materials and device issues. In a view of increasing efficiency and/or economic viability, several concepts and innovative technologies proposed include intermediate band solar cell [81], quantum dots and quantum wells solar cell [86], down and upconversion solar cell [87], plasmonic solar cell [88], hot-carrier solar cell [89], tandem solar cell with tunnel junctions [90], dye-sensitised and Perovskite solar cells [91] and graded bandgap solar cell [35,92]. Amongst the proposed concepts only tandem solar cells and graded bandgap solar cells have experimentally shown reasonable efficiency with required stability and the potential for increasing performance. The main difference between these two approaches is that the tandem solar cells efficiency increase is mostly due to increase in open-circuit voltage, V_{oc} while in the graded bandgap (GBG) solar cells the efficiency is mainly increased due to

increase in the short-circuit current density, J_{sc}. The high J_{sc} in GBG is as a result of E_c to E_c and E_v to E_v (parallel connection) along the GBG interfaces [35]. The main drawback of tandem solar cells is the series connection of cells resulting into the reduction in charge carrier mobility and increase in the recombination of e-h pairs generated within the cell while the graded bandgap solar cell's disadvantage is the technicality of growth required.

2.6   CdS/CdTe based solar cells

Based on electronic and optoelectronic properties such as a near-ideal direct bandgap of 1.45 eV, high absorption coefficient $>10^4$ cm^{-1} at 300 K and the ability to absorb all usable energy from the solar spectrum within a thickness <2 μm [93], CdTe has proved to be an excellent II-VI semiconductor material. CdTe-based solar cells have been well explored to develop low-cost and high-efficiency solar cells as an alternative to the present-day fossil fuel dependent energy sources which are harmful to our ecosystem sustainability.

Table 2.3: Summary of CdS/CdTe solar cell efficiency landmarks.

Year	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	Team
1977	8.5	-	-	-	Matsushita
1981	8.9	710	16.5	0.58	Kodak
1983	10.3	725	21.2	0.67	Monosolar
1988	11.0	763	20.1	0.72	AMETEK
1990	12.3	783	25.0	0.63	Photon energy
1991	13.4	840	21.9	0.73	UoSF
1992	14.6	850	24.4	0.71	UoSF
1993	15.8	843	25.1	0.75	UoSF
1997	16.0	840	26.1	0.73	Matsushita
2001	16.4	848	25.9	0.75	NREL
2001	16.5	845	25.9	0.76	NREL
2011	17.3	842	29.0	0.76	First Solar
2012	18.3	857	27.0	0.77	GE
2013	18.7	852	28.6	0.77	First Solar
2013	19.6	857	28.6	0.80	GE
2014	21.4	876	30.3	0.79	First Solar
2016	22.1	887	31.7	0.79	First Solar

The exploration of CdTe-based solar cells is dated as far back as 1947 with the measurement of photoconductivity of incomplete phosphors of CdTe [94]. The photovoltaic potential of the CdTe-based solar cell was first theoretically demonstrated by Loferski in 1956 [95]. His work iterated that semiconductor materials with bandgaps close to 1.5 eV would possess the highest possible conversion efficiencies. Adirovich et al. published the first work on CdS/CdTe polycrystalline solar cell with superstrate configuration. in 1970 [93,96] with PV conversion efficiency >2%. Based on the extensiveness of the research work undergone within the CdTe-based PV field afterward, the listing as shown in Table 2.3 can only be viewed as a selection of the landmarks in CdTe-based solar cells till date.

2.7   Conclusions

This Chapter discussed in brief, the properties of solid-state materials with main emphasis on semiconductors and their classifications. The properties of semiconductor which makes them suitable for photovoltaic applications and properties of the junctions formed between S/S and M/S were also discussed. Further to this, the basic operations, advantages and disadvantages of different solar cell types were also presented in addition to the brief overview of next-generation solar cells.

Chapter 3 -   Techniques utilised in materials growth, materials, and device characterisation.

3.1   Introduction

Most semiconductor deposition techniques are capable of producing high-quality thin films using complex systems at a very high manufacturing cost. However, new researches are aimed towards reducing material usage, cost of production and improving the fabricated device performances. Consequently, the cost of many devices including solar cells has been reduced by using thin films [97,98]. The deposition of thin film semiconductor materials with thicknesses ranging between few nanometers (nm) to micrometers (μm) is achievable using several techniques as documented in the literature. The main deposition technique being focused on in this program is electrodeposition due to its significance in the research work as reported in this thesis. Further to this, the analytical methods utilised in characterising and optimising the deposited semiconductor materials and devices will also be discussed.

3.2   Overview of thin film semiconductor deposition techniques

Thin film semiconductor deposition techniques can be broadly aligned under physical or chemical deposition categories. The physical deposition refers to the technologies in which material is released from a source and deposited on a substrate using thermodynamic, electromechanical or mechanical processes [99]. This technique includes closed space sublimation (CSS), molecular beam epitaxy (MBE), radio frequency (RF) sputtering, and magnetron sputtering amongst others. On the other hand, the chemical deposition techniques are accomplished by the utilisation of precursors either in their liquid or gaseous state to produce a chemical reaction on the surface of a substrate, leaving behind chemically deposited thin film coatings on the substrate. Such technique includes electrodeposition (ED), chemical bath deposition (CBD), chemical reduction plating, spin coating and chemical vapour deposition (CVD) processes. Other subdivisions of chemical vapour deposition (CVD) include metalorganic CVD (MOCVD), atmospheric pressure CVD (APCVD), etc [99].

However, based on simplicity of technique, columnar growth, self-purification, ease of extrinsic doping [39], ease of depositing *n*-type, *i*-type and *p*-type semiconductors (for semiconductor materials whose conductivity type depends on stoichiometry) by varying the deposition potential, scalability, manufacturability [100–102], and economic

viability [103] amongst other advantages, electrodeposition is considered as one of the edging thin film deposition techniques [16]. Electrodeposition is not without its challenges; this includes requirements for a conducting substrate, pinhole (due to its nucleation mechanism [38]), low process temperature (as improved crystallinity is achievable at higher deposition temperature [104]) and comparatively longer deposition time, etc.

3.3   Electrodeposition growth technique

Electrodeposition is the process of depositing metals or compound semiconductors on a conducting substrate by passing an electric current through an ionic electrolyte in which metal or semiconductor ions are inherent [105]. The passage of current is required due to the inability of the chemical reaction resulting in the deposition of the solid material on the conducting substrate to proceed on its own as a result of positive free energy change ΔG of the reaction.

Although electrodeposition can be categorised based on power supply source, working electrode and electrode configuration (as shown in Figure 3.1), the basic deposition mechanism and setup remains similar. The basic deposition mechanism entails the flow of electrons from the power supply to the cathode. The positively charged cations are attracted towards the cathode and negatively charged anions to the anode. The cation or anions are neutralised electrically by gaining electrons (through reduction process) or losing an electron (through oxidation process) and being deposited on the working electrode (WE) respectively [105]. The typical ED setup of two-electrode (2E) configuration as shown in Figure 3.2 consist of deposition container (beakers), deposition electrolyte, magnetic stirrer, hotplate, power supply, a working electrode, a counter electrode and an optional reference electrode (RE) in the case of 3-electrode (3E) configuration.

In this research work, potentiostatic power source, cathodic deposition in which semiconductors are deposited on the cathode and two-electrode (2E) configuration were utilized in the deposition of all the semiconductor layers. The use of potentiostatic power source was due to the effect of deposition voltage on the atomic percentage composition of elements in the electrodeposited layer, which is one of the factors determining the conductivity type [24,106]. The cathodic deposition was utilized due to its ability to produce stoichiometric thin films with good adherence to the substrate as

compared to anodic deposition [107]. In conjunction, most of the metal ions deposited as reported in this thesis are cations.
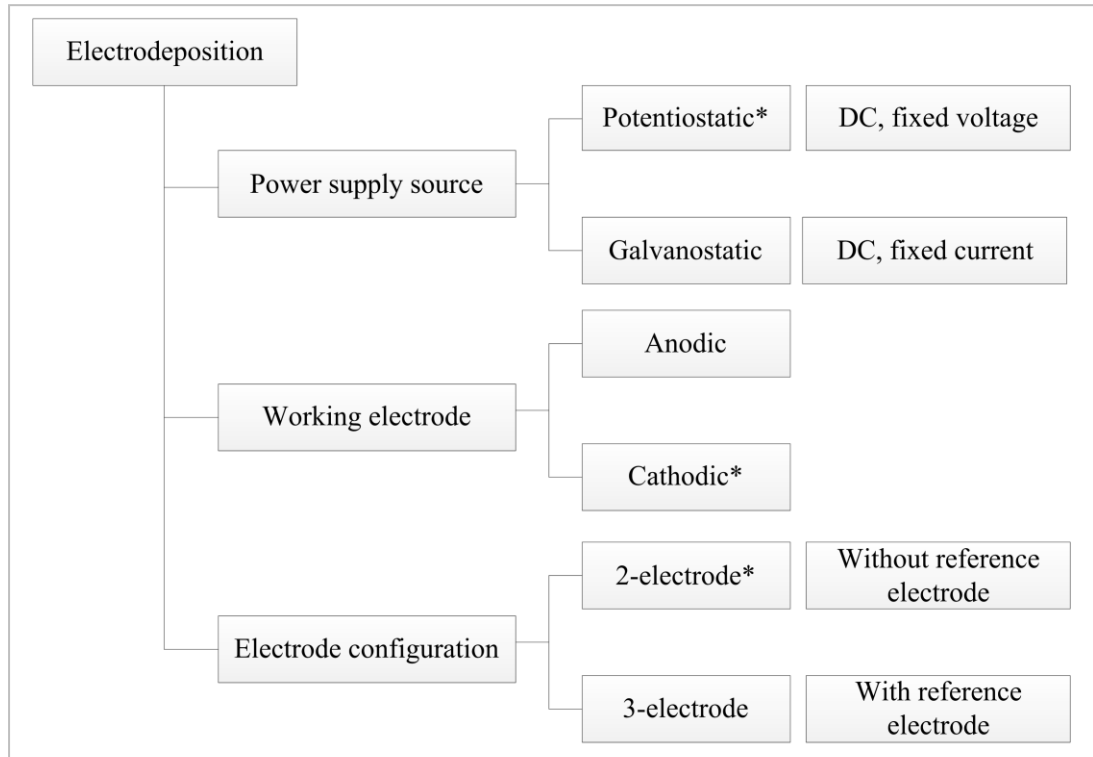
Figure 3.1: The main categories of electrodeposition technique. * signifies the utilised options in this research work.

The two-electrode configuration as shown in Figure 3.2 was utilised due to its industrial applicability, process simplification and also to eliminate possible K^+ and Ag^+ ions doping [108,109] which may emerge from the Ag/AgCl or saturated calomel electrode (SCE) reference electrodes. Taking the electrodeposition of n-CdS and n-CdTe layers which are respectively utilised as the main window and absorber layers in this thesis into perspective, both K^+ and Ag^+ from group I of the periodic table are considered as p-type dopants. Therefore, any leakage of K^+ and Ag^+ into the electrolytic bath may result in compensation leading to the growth of highly resistive material which has a detrimental effect on the efficiency of fabricated solar cells. This has been experimentally shown and reported in the literature [108].

The two-electrode electrodeposition configurations are not without challenges, with the main challenge being the fluctuation or drop in the potential measured across the cathode and the anode during deposition. This is due to the alteration in resistivity of the substrate with increasing semiconductor layer thickness and the change in the ionic concentration of the electrolyte. Unlike the 3-electrode configuration, the potential

difference is measured across the working and the reference electrodes while the measured current is between the working and the counter electrodes. In general, other factors such as the pH of the electrolyte [110], applied deposition potential [24,106], deposition temperature [111], stirring rate [112] and concentration of ions in the deposition electrolyte [110] affects the electrodeposition process and the properties of the deposited layers.
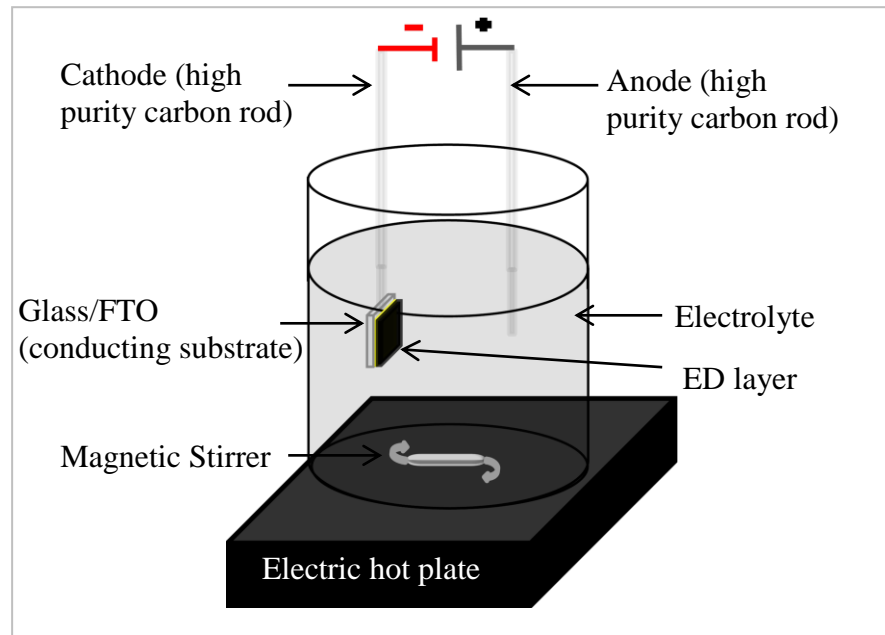
Figure 3.2: Typical two-electrode electrodeposition set up.

The electrodeposition of both metals and semiconductors is governed by Faraday's laws of electrodeposition. The first law states that "The amount of substance liberated or deposited at an electrode is directly proportional to the quantity of electricity passed through the electrolyte." This principle can be mathematically represented by Equation 3.1, where m is the mass of a substance liberated or deposited on an electrode, Q is the total electric charge and Z is a constant known as equivalent chemical weight.

$$m = ZQ$$ Equation 3.1

Faraday's second law of electrolysis states that, when the same quantity of electricity is passed through several electrolytes, the mass of the substances deposited or liberated are proportional to their respective chemical equivalent or equivalent weight. The chemical equivalent weight can be defined as the ratio of molecular weight to the valence number of ions (electrons transferred per ion) as shown in Equation 3.2, where M is the

molecular mass (gmol^{-1}), z is the valence number, n is the number of electrons transferred in the chemical reaction for the formation of 1 mole of substance in gcm^{-3} and F is the Faraday's constant (96485 Cmol^{-1}).

$$Z = \left(\frac{M}{z}\right) = \left(\frac{M}{nF}\right)$$

Equation 3.2

Therefore, Equation 3.1 can be rewritten as Equation 3.3

$$m = \left(\frac{Q}{F}\right)\left(\frac{M}{n}\right)$$

Equation 3.3

knowing that

$$Q = it$$

Equation 3.4

$$\rho = \frac{m}{TA}$$

Equation 3.5

Where i is the average deposition current (A), t is the deposition time (s), J is current density (Acm^{-2}), ρ is the density (gcm^{-3}), T is the thickness (cm), and A is the surface area of the substrate in contact with the electrolyte (cm^2). Therefore, Equation 3.3 can be further modified as Equation 3.6,

$$T = \left(\frac{1}{nF}\right)\left(\frac{itM}{\rho A}\right) = \left(\frac{JtM}{nF\rho}\right)$$

Equation 3.6

The relationship can be used to estimate the thickness of electrodeposited layers.

3.4   Material characterization techniques

3.4.1   Cyclic voltammetry

Cyclic voltammetry is a technique utilized in the study of the electrochemical reaction of the electrodeposition process by measuring the electric current through the electrolyte as a function of potential sweep across the electrodes [113]. In other words, it can be defined as the current-voltage characteristics of the electrolyte that describes the conduction of electrical current through the electrolyte (resulting in the oxidation or reduction of ions) as a result of the potential applied. Therefore it is necessary to perform a voltammetric study on electrolytic baths from which semiconductor layers are to be deposited to identify the cathodic voltage range suitable for their deposition.

Cyclic voltammetry is performed by scanning the potential across both the working and counter electrodes in the forward and reverse direction to qualitatively identify both the deposition and dissolution sequence of elements of the semiconductor. With this qualitative information, the suitable region from which the deposition of near-stoichiometric semiconductor layers can be determined for further characterization using techniques which will be discussed in the following sections.

For the cyclic voltammetric study in this work, the power source utilized is GillAC computerised potentiostat (ACM instrument) while the voltage range scanned and scan rate were (0 to 2000) mV and 3 mVs^{-1} respectively.

To further pinpoint the deposition potential (V_i) in which stoichiometric semiconductor material can be deposited based on material properties, characterisation of the deposited layers within the observed deposition range from the voltammetric study needs to be explored. The structural features of the deposited layers were obtained using the X-ray diffraction (XRD) and Raman spectroscopy. The morphological features were obtained using scanning electron microscopy (SEM). The compositional analyses were performed using energy-dispersive X-ray spectroscopy (EDX). The optical features were determined using ultraviolet-visible (UV-Vis) spectroscopy. The electronic property such as conductivity type was determined using photoelectrochemical (PEC) cell measurement, while the resistivity was determined using the direct current (DC) conductivity measurement technique.

3.4.2 X-ray diffraction (XRD) technique

X-ray diffraction (XRD) technique is a non-contact and non-destructive technique utilised in the determination of the structural properties of materials. Information on lattice parameters and sample texture such as atomic planes, phase identification, lattice spacing, the intensity of individual diffractions, preferred orientation and crystallite size can be obtained.

Figure 3.3 shows the main components of XRD equipment which comprises of the sample holder, X-ray tube, and X-ray detector. The sample to be investigated is placed in the sample holder. X-rays generated in the X-ray tube is channeled through a monochromator (to select radiation of a single wavelength or energy) to be filtered and then assembled using a collimator (to produce a parallel beam of rays or radiation). The X-rays are further channeled through both the divergent and anti-scatter slits to limit the divergence of the incident X-ray beam and output noise (due to amorphous or air

scattering) respectively. The interaction between the X-rays after being channeled through the monochromator and the slits onto the sample under investigation is referred to as interference. During XRD operation, the incident angle of the X-rays on the sample under investigation changes due to the movement of the X-ray tube along the diffractometer circle to focus the rays onto the sample under investigation.
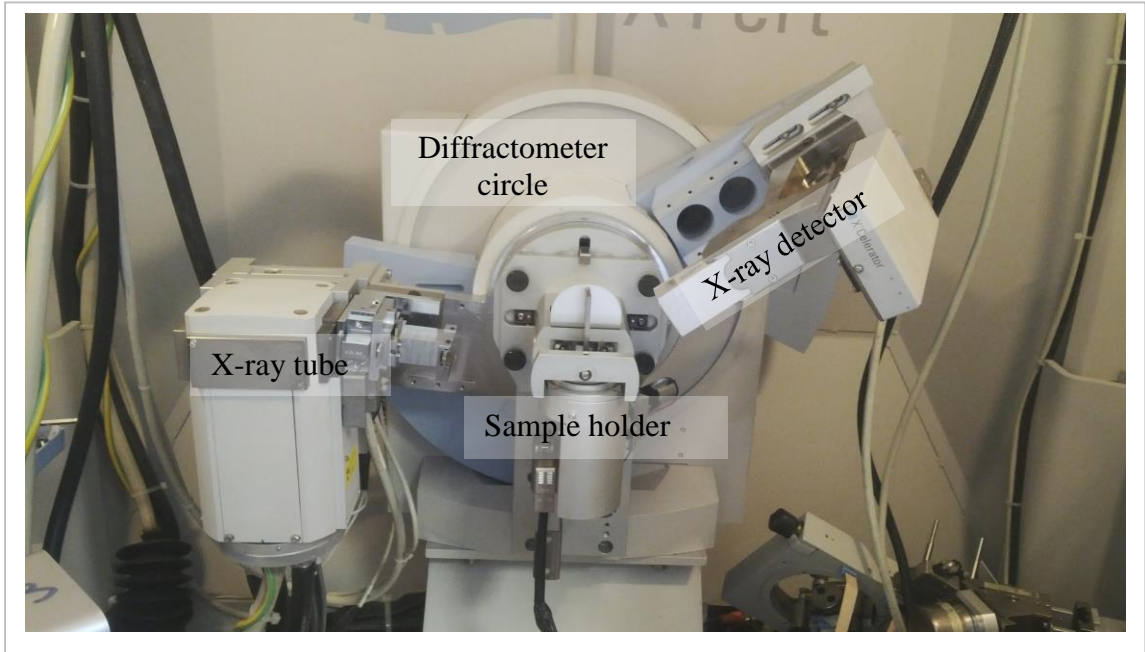
Figure 3.3: XRD equipment setup showing its main components.

The interaction between X-rays and atoms of a crystal results in the elastic scattering of the rays by the electrons of the atom. The reflection of incoming rays by electron in the atom gives rise to diffracted rays. It should be noted that X-ray is an electromagnetic radiation within the wavelength range of (1 to 100) Å. The X-ray wavelength range falls within the same order of magnitude as the typical interatomic distance in a crystal. For this reason, it is why it is easy for X-rays to be diffracted by the crystal structures [114]. Scattered rays may either support one another (constructive interference) or interfere and eliminate one another (destructive interference). It should be noted that the principle of XRD is based on the constructive interference which is governed by Bragg's law. Therefore, the conditions of interaction as stated by Bragg's law shown in Equation 3.7 is fulfilled when the interaction between the sample being investigated and the incident X-rays having wavelength λ (Å) produces constructive interference and diffracted rays.

$$n\lambda = 2d\sin\theta$$ Equation 3.7

Where n is the whole number, λ is the wavelength, d is the lattice spacing (interatomic distance), and θ is the angle between the incident beam and atomic plane. The Bragg's law is derived from Figure 3.4, where the path difference between the two adjacent X-rays ABC and EFG is PF+FQ which is equal to $2d \sin\theta$.
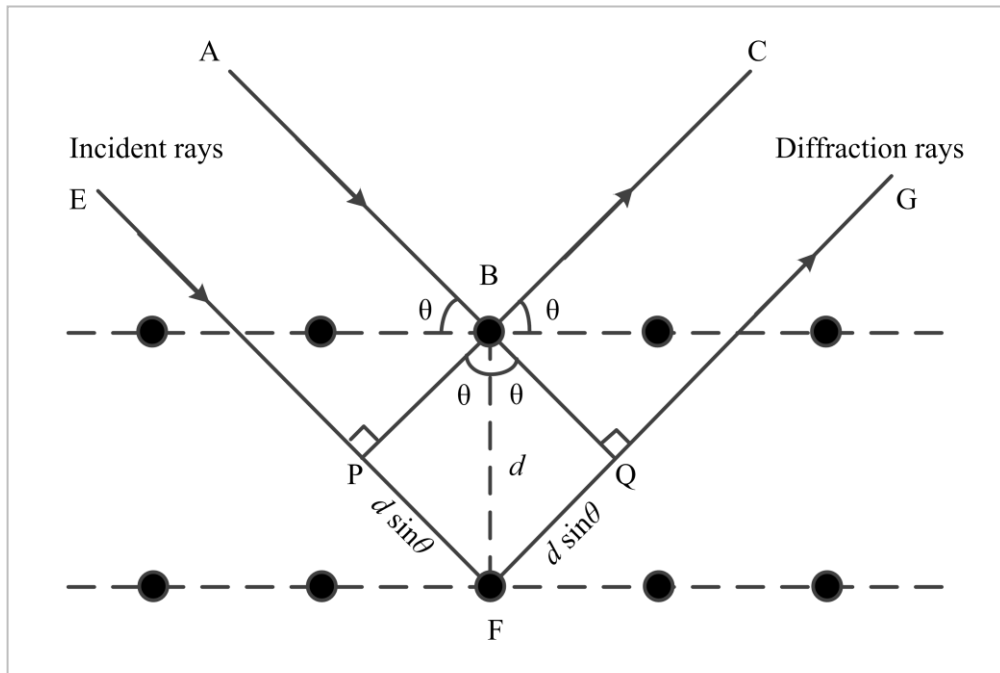
Figure 3.4: The basic principle of X-ray diffraction showing constructive interference when Bragg's law is satisfied.

Therefore, if $2d \sin\theta$ is equal to the integral multiple of the X-ray wavelength ($n\lambda$) resulting in a constructive interference which produces a peak in intensity. Then the X-ray detector detects, processes and converts the diffracted X-rays signal to a count rate which is being sent to a computerised device as a function of the diffraction angle 2θ. The data obtained using XRD includes d-spacing for diffraction which can be compared with the Joint Committee on Powder Diffraction Standards (JCPDS) for easy identification of crystalline elements and compounds.

Based on the XRD peaks obtained, crystallite size can be evaluated using Debye-Scherrer's equation as shown in Equation 3.8. Where D is the crystallite size (nm), λ is the X-ray wavelength (Å), β is the full width at half maximum (rad) of the investigated peak, θ is the Bragg's angle (°), and the constant $K=0.94$ is the geometry of spherical crystal. However, it should be noted that there is a limitation of the use of Scherrer's

equation in determining the crystallite size. This equation is formulated to calculate grains sizes within few tens of nanometers [115].

$$D = \frac{0.94\lambda}{\beta \cos\theta}$$ Equation 3.8

In this thesis, the X-ray diffraction (XRD) scans were carried out within the range of $2\theta=(20$ to $70)°$ using Philips PW X'pert diffractometer with Cu-K$_\alpha$ monochromator having a wavelength of 1.54 Å. The source tension and current were set to 40 kV and 40 mA respectively. Between $2\theta=(20$ to $70)°$, a step count of ~2000 was utilised amounting to a possible uncertainty range of ±0.02°. The obtained diffraction peaks were fitted and analysed using PANalytical X'Pert HighScore Plus.

3.4.3   Raman spectroscopy technique

Raman spectroscopy is a very efficient and non-destructive characterisation technique which can be utilised for the identification and investigation of molecular fingerprint, crystallinity, strain, and stress of the solid-state materials [116]. The technique relies on the inelastic scattering of monochromatic light, which is mainly laser source ranging from ultra-violet (244 to 400) nm through visible (400 to 780) nm to near infrared (785 to 900) nm.
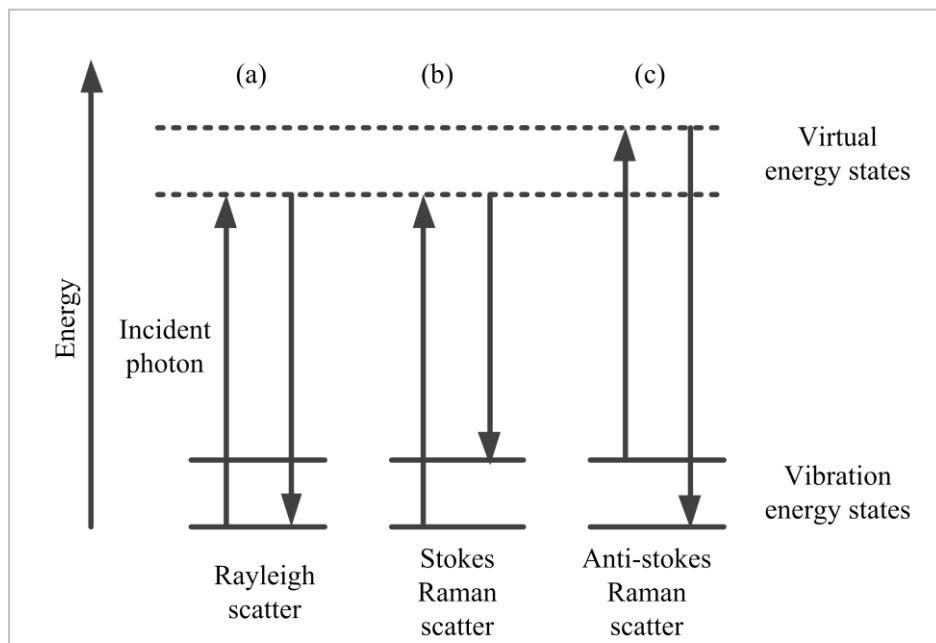
Figure 3.5: Schematic representation of the Raman transitional schemes (a) Rayleigh scattering (b) Stokes Raman scattering and (c) Anti-Stokes Raman scattering.

As shown in Figure 3.5, the interaction between the laser light and the molecules of the material under investigation results in the vibration of the molecules which eventually leads to the emission of scattered light when returned to its vibration energy states after excitation. The change in vibration energy state between the original state and the new state gives the shift in the energy of the emitted photon [117]. The excited molecule may return to its original vibration energy state and emit scattered radiation with frequency (v_f) equal to the frequency of the incident laser light in the case of Rayleigh scattering. Molecules may return to a higher or lower vibration energy state than the original state, and this phenomenon is respectively known as Stokes-Raman scattering, or anti Stokes-Raman scattering respectively. The emitted scattered light is detected by a photon detector, analysed in computerised Raman equipment and displayed as Raman spectrum on the computer visual display unit. The Raman spectra reported in this thesis were obtained using Renishaw's Raman spectrometer with an argon laser and an excitation wavelength of 514 nm.

3.4.4   Scanning electron microscopy (SEM) technique

Scanning Electron microscopy (SEM) is a technique utilised for morphological analysis of material surfaces. Figure 3.6 shows the schematic diagram of SEM equipment with the inclusion of its major components. Scanning Electron microscopy is performed in a high vacuum chamber (of about 10^{-4} Nm^{-2}) in which the surface of the material under investigation is scanned with a focused beam of high-energy electrons generated at high voltage in the electron gun. The electron gun situated at the upper part of the microscope column may contain either Tungsten filament, Lanthanum hexaboride (LaB_6) or Cerium hexaboride (CeB_6) solid-state crystal or field emission gun (FEG) which are the main sources of electrons in an SEM equipment [118].

Electrons are produced at the electron source at a high voltage ranging between 5 kV and 30 kV depending on the equipment specifications. The generated beam of high-energy electrons is channeled down the microscope column towards the sample being investigated through series of condenser lenses and apertures. The condenser lenses focus the incident electron beam on to the sample under investigation, while the aperture is the opening through which the electron beam is channeled. The positioning of the electron beam on the sample under investigation is controlled by scan coils placed above the objective lens as shown in Figure 3.6. The scan coil also allows the electron beam to scan the sample surface area in a raster scan pattern [119]. The

interaction between the primary electron beam and the atoms in the sample under investigation produces several signals based on both inelastic and elastic interactions [119]. Resulting signals include secondary electrons, backscattered electrons, Auger electrons and characteristic X-rays [119] which contains information about the surface topography and composition sample under investigation. The resulting signals are sensed and collected by the detectors and processed to produce images visible on the visual display unit. As shown in Figure 3.7, the probing depth of the signals resulting from these interactions are different within the sample from which they can escape due to their unique physical properties and energies [119].
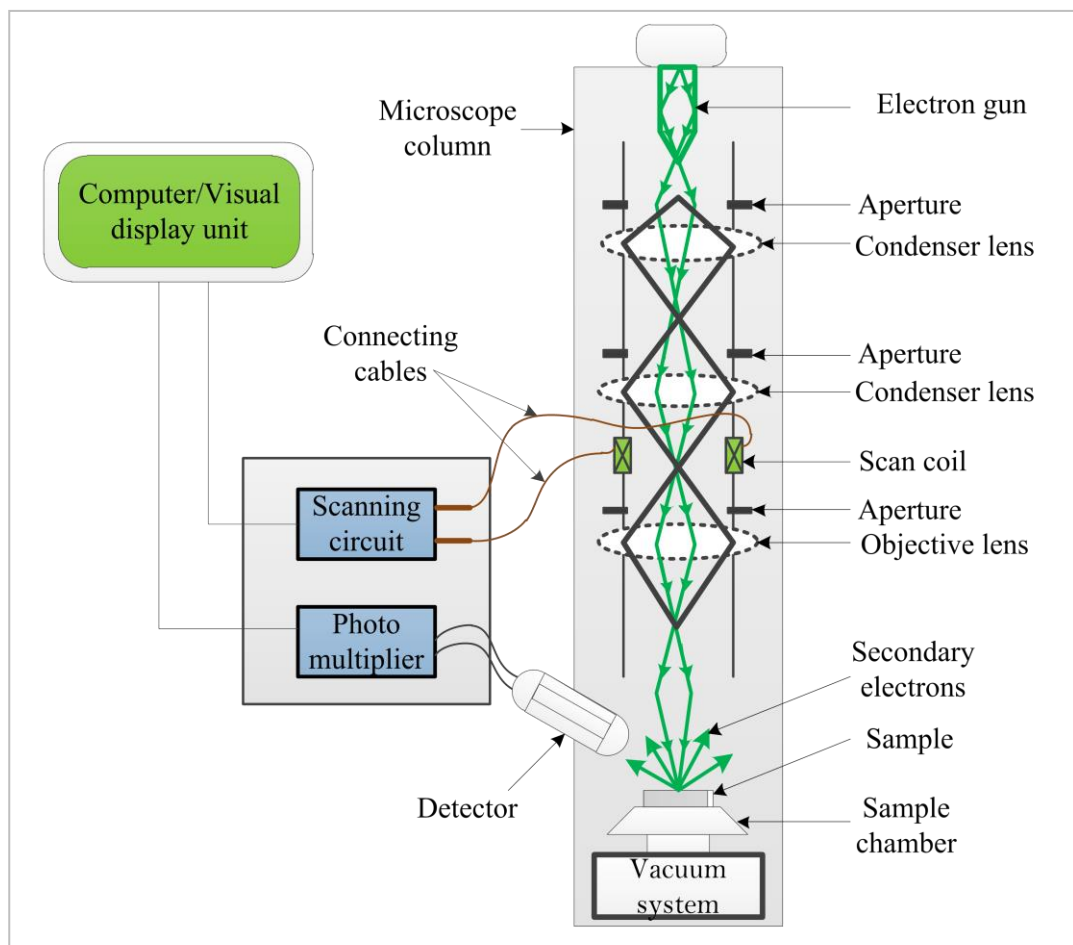
Figure 3.6: Schematic diagram of a scanning electron microscope.

Image formation in SEM is accomplished by mapping either the intensity of secondary electron (SE) or the backscattered electron (BSE) signals from the specimen [119]. The secondary electrons (SE) are low-energy electron ejected from the outer shell of an atom in the sample under investigation after the inelastic interaction between the primary electron beam and the sample. Secondary electrons are created close to the

surface of the sample within a depth of (5 to 50) nm [119] and therefore produces information on the morphology of the sample under investigation. SE are more influenced by surface properties (such as sample work function and local surface curvature) rather than by the atomic number. It should be noted that an increase in atomic number increases the SE signal produced [120]. The SE signals are detected by secondary electron detector (SED).

Backscattered electrons (BSE) are higher energy electrons which originate from the elastic interaction between the primary electron source and the nucleus of an atom within the sample. The interaction results in minimal energy loss and scattering of the electrons in a different direction. The electrons scattered towards the surface of the sample is being detected by the backscattered electron detector (BSED). BSE gives compositional information on samples. The intensity of BSE signal is affected by the atomic number of the specimen, with higher atomic numbered element showing higher intensities; this is because atoms having higher atomic numbers easily backscatter [119,120]. BSE occur at a notable depth within the sample depending on the beam energy and the sample composition [119].
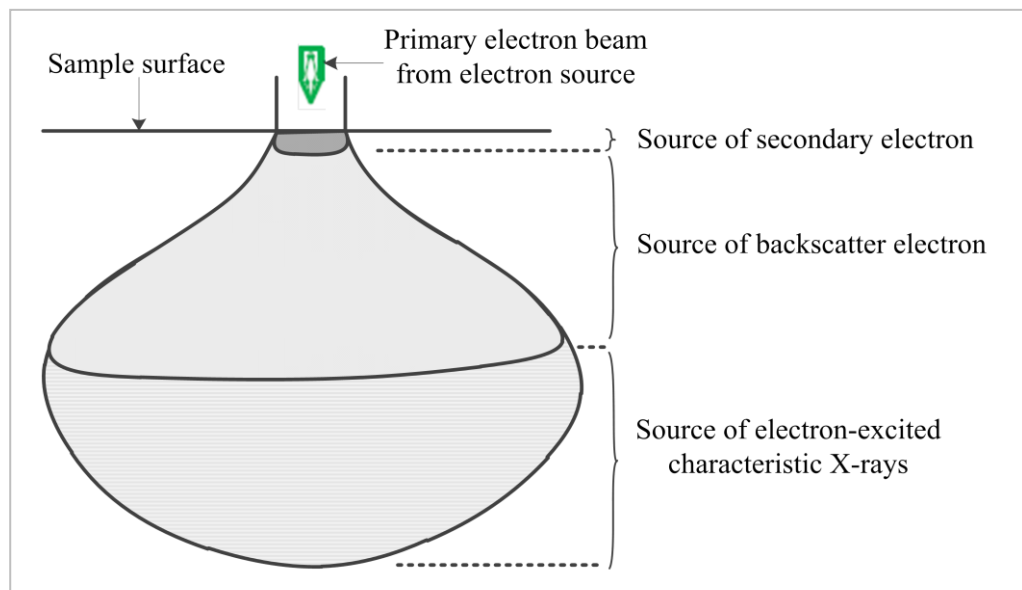
Figure 3.7: Typical diagram illustrating the production of three different signals within the specimen volume as a result of sample-electron interaction.

The SEM images reported in this thesis were carried out using FEI Nova 200 NanoSEM at a magnification of ×60000 and an accelerating voltage of 10 kV. For comparability, the accelerating voltage for all the layers explored was kept constant due to the relationship as shown in Equation 3.9 [121], where *A* is the atomic weight, *H* is the

penetration depth, V is the acceleration voltage, z is the atomic number and ρ is the density. Based on Equation 3.9, the probing depth for CdS and CdTe are ~955 nm and ~879 nm respectively.

$$H = \frac{0.0276 A V^{1.67}}{z^{0.89} \rho}$$

Equation 3.9

The investigated samples (glass/FTO/deposited layer) were thoroughly cleaned using methanol, rinsed in deionised water and dried in a stream of nitrogen gas. The sample was attached to the conductive SEM stub using conductive carbon adhesive discs. Silver paint was also utilised to electrically connect the stub and glass/FTO on which the thin film was deposited. The electrical connectivity was required to avoid noise in SEM image due to charging effects which occur on non-conductive material as it is in this case, the glass/FTO substrate.

3.4.5   Energy dispersive X-ray (EDX) technique

Energy dispersive X-ray spectroscopy (EDX) is an analytical technique utilised for the compositional analysis of elements contained in a material. It is a technique used in conjunction with SEM as discussed in Section 3.4.4. The resulting signals due to the interaction between the primary electron beam and sample under investigation include secondary electrons, backscattered electrons, Auger electrons and characteristic X-rays [119]. The SEM image utilises secondary electrons and backscattered electrons for image formation, while the EDX uses the characteristic X-rays for elemental composition analysis.

Characteristic X-rays are generated by inelastic interactions between the primary electron beam and the inner shell electron of the atom of the sample under investigation. The inner shell electron is emitted from the sample's atom (ionization) [119] as shown in Figure 3.8. The hole created in the inner shell is being filled by the electrons from the outer shell in a process known as relaxation of an atom into its neutral state.

The transition of an electron from the outer shell to the inner shell during relaxation releases unique amount of energy from the atom in the form of X-ray photon which is equivalent to the energy difference between the two shells. The characteristic X-ray is a fingerprint of the element from which it is emitted. The emitted X-ray is sensed and collected by the EDX detector. The EDX detector also separates the characteristic X-rays of the different elements into different energy spectra. As shown in Figure 3.8, the nomenclature of the emitted X-rays is dependent on the inner shell on which the hole is

situated and the outer shell from which the electron transit to fill the hole. The EDX measurements reported in this thesis were carried out using EDX detector attached to FEI Nova 200 NanoSEM.
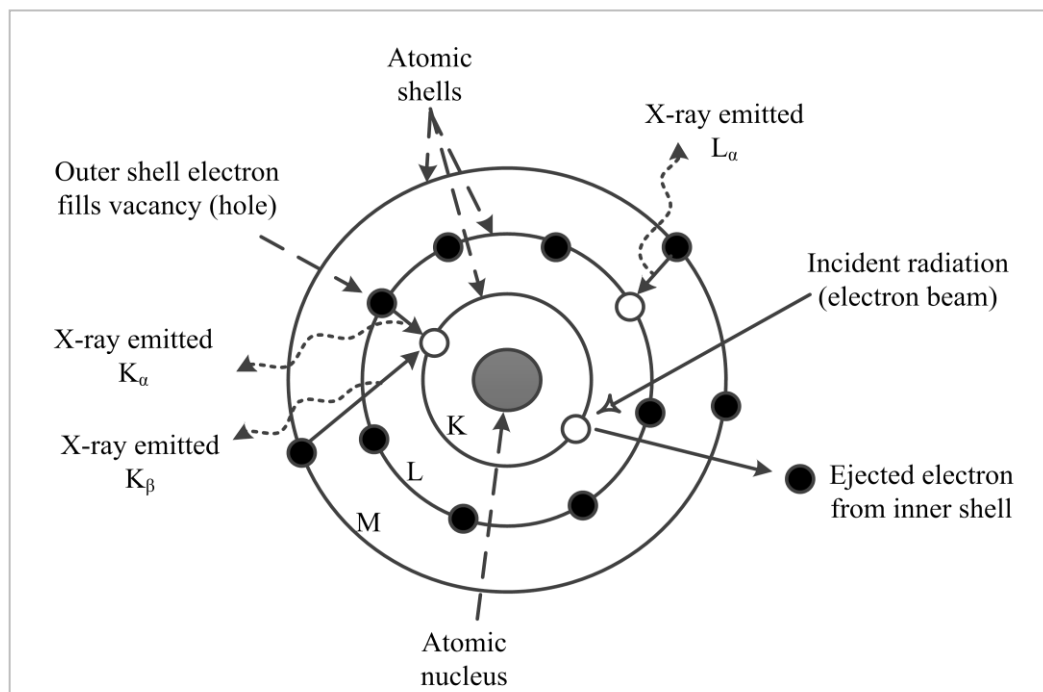
Figure 3.8: Schematic diagram of Energy Dispersion X-ray Spectroscopy (EDX).

It should be noted that the downside to the use of EDX includes:

i.   Limitation of EDX sensitivity of element(s) to ~1000 ppm by weight unless counting time is increased.

ii.   Analytical accuracy of ~2% due to uncertainties due to the composition of the standard utilised, overlapping elemental peaks and background corrections [122].

Due to this possible error range of ±2%, the elemental concentration data obtained were processed as a ratio one element to the other to nullify the error.

3.4.6   Ultraviolet-Visible (UV-Vis) Spectrophotometry technique

The UV-Vis spectroscopy is a technique used for the analysis of the optical properties of an optical material. Such optical properties include the absorbance, transmittance, and reflectance of light incident on an optical material. The technique is performed using a UV-Vis spectrophotometer which is capable of scanning wavelength range between the near ultraviolet (UV)~(200 to 400) nm and visible (Vis) regions ~(400 to700) nm.

As shown in Figure 3.9, the basic components of a UV-Vis spectrophotometer comprise of a light source, monochromator, photodetector, signal processor and visual/computer display unit. The light produced by the light source is usually a combination of halogen lamps with a wavelength ranging between ~(320 to 1100) nm for the visible and near-infrared regions and the deuterium lamps with a wavelength ranging between (190 to 370) nm used for the ultraviolet region.

The monochromator functions as an optical device that selectively transmits narrow wavelength of light from a broader range of wavelength available at the input. The monochromator contains other components such as the entrance and exit slits, collimator and focusing lenses and diffraction grating. The entrance slit narrows the white light from the light source incident on the collimator lens, while the collimator lens functions as a device that makes parallel the incident light on the diffraction grating. The diffraction grating separates the polychromatic incident light into its component wavelengths (monochromatic light). The monochromatic light is focussed on the sample under investigation through the exit slit which debars the propagation of any stray light on to the sample. Depending on the optical properties of the sample, a fraction of the monochromatic beam intensity is absorbed while the rest is either transmitted or reflected.
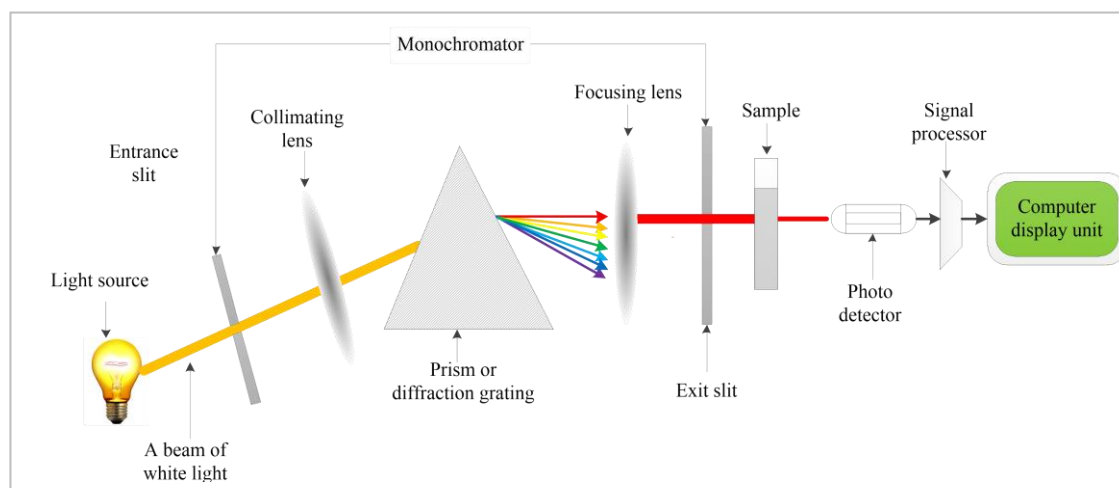
Figure 3.9: Schematic diagram showing main components of UV-Vis spectrometre.

The relationship between the incident beam intensity (I_o) on the sample under investigation and the transmitted beam intensity (I) can be represented using Equation 3.10.

$$I(x) = I_o \exp(-\alpha x)$$ Equation 3.10

Where x is the thickness of the sample (which is mainly a semiconductor material in this thesis), and α is a material constant known as the absorption coefficient which determines the rate of absorption of light by a material as it propagates through it. The transmittance (T) of the sample under investigation can be defined as the ratio of the incident beam intensity (I_o) to the intensity of the transmitted beam (I) (see Equation 3.11).

$$T = \frac{I}{I_o}$$ Equation 3.11

The relationship between the transmittance (T) and absorbance (A) of the sample under investigation as defined in the literature can be represented by Equation 3.12 [123].

$$A = \log_{10}\left(\frac{I_o}{I}\right) = \log_{10}\left(\frac{1}{T}\right)$$ Equation 3.12

The reflectance R can be obtained using Equation 3.13, where n is the real part of the complex refractive index (N) of semiconductor material.

$$R = \frac{(n-1)^2}{(n+1)^2}$$ Equation 3.13

The complex refractive index N can be obtained using Equation 3.14, where K is the extinction coefficient (the imaginary part of the refractive index).

$$N = n + iK$$ Equation 3.14

As shown in Figure 3.9, the fraction of the incident monochromatic light transmitted through the sample is detected by the photodetector. The photodetector converts the photons incident on it into current by the generation of electron-hole (e-h) pairs from its *p-n* junction configuration. Concerning the monochromatic light wavelength, the signal is processed and amplified by the signal processor and displayed on the computer display unit. From the optical property data accumulated using the spectrometer for a specified wavelength range, the bandgap of the semiconductor material can be estimated by plotting a graph of absorbance square (A^2) against photon energy (hv) and extrapolating the straight line portion of the absorption curve to the photon energy axis. Alternatively, Tauc's plot of $(\alpha hv)^2$ against (hv) can also be utilised [124]. The Tauc's formula as shown in Equation 3.15 depicts the relationship between absorption

coefficient (α), bandgap energy (E_g), Planck's constant (h) and the incident photon frequency (v) for a direct bandgap material. Where k is the proportionality constant which depends on the refractive index of the sample under investigation and n is the power factor of the transmission mode. The value m equals 0.5 for direct bandgap and 2.0 for indirect bandgap materials. Based on the literature, sharp absorption edge signifies lesser impurity energy levels and defects in the thin film [30,125,126].

$$\alpha = \frac{k\left(hv - E_g\right)^m}{hv}$$

Equation 3.15

With CdS/CdTe-based solar cells being within the confines of this thesis, it should be noted that optical losses such as reflection and parasitic absorption have been associated with lowering the conversion efficiency of cadmium sulphide/cadmium telluride (CdS/CdTe) -based solar cells. The predominant loss of ~15% of the attainable short-circuit current density J_{sc} of the fabricated cells is associated with the parasitic absorption of the buffer and/or the window layer [127–129]. Based on literature and other experimental work later discussed in Chapter 6, parasitic absorption can be reduced through buffer and/or window layer thickness optimisation [38,130,131]. While reflection losses at the air-glass, glass-transparent-conducting-oxide (TCO), TCO-CdS, and CdS-CdTe accounts for ~8% loss of the attainable J_{sc} of the fabricated solar cells [127–129]. Reflection losses are reducible to <2% using antireflection coatings [132].

3.4.7   Photoelectrochemical (PEC) cell characterisation technique

Photoelectrochemical (PEC) cell measurement is a simple technique utilised for the determination of the conductivity type of a semiconductor material [16]. The preference of PEC cell measurement to the more robust Hall Effect measurement is due to the inclusion of underlying transparent conducting oxide (TCO) substrate on which the semiconductor material is deposited. Due to the high conductivity of the TCO, as compared to the semiconductor layer deposited on it, the TCO serves as a current alternative route under Hall Effect technique. Therefore the electrical parameters obtained are deemed unreliable due to the influence of the TCO.

Figure 3.10 shows the basic setup of PEC cell measurement which includes DC source, light source, digital voltmeter, semiconductor (sample under investigation), a counter electrode, inner beaker, outer case, and electrolyte. The electrolyte utilised for all the PEC measurement presented in this work is 0.10 M $Na_2S_2O_3$ in 20 ml of deionised water. The measurements were taken at ~25°C.
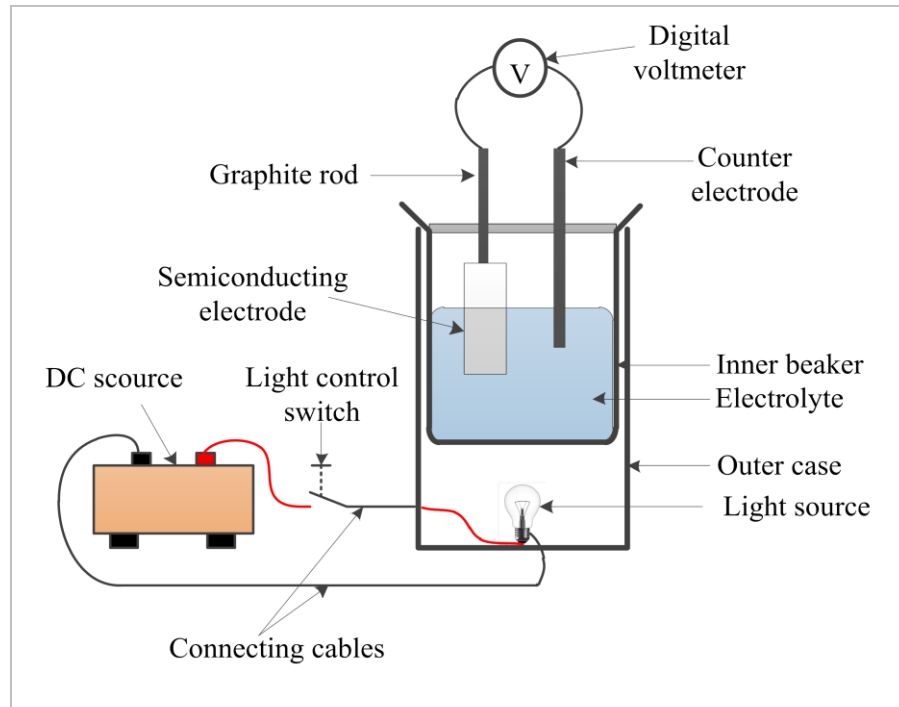
Figure 3.10: Typical schematic diagram of the experimental setup for PEC cell measurements.

PEC cell measurement is based on the formation of a semiconductor/electrolyte (S/E) junction similar to an M/S junction when a semiconductor and suitable electrolyte are brought in contact. Due to the difference between the Fermi level E_F of the semiconductor and the energy level of the electrolyte E_{oREDOX}, transfer of electron occurs between the two equilibria positions until a new equilibrium is achieved in which the Fermi level of the semiconductor aligns with the energy level of the electrolyte ($E_{oREDOX} = E_F$). This results in the formation of a Schottky barrier in which the band bending direction and the flow of electron is determined by the conductivity type of the semiconductor as shown in Figure 3.11. Under the illuminated condition, photons with energy higher than the semiconductor bandgap are absorbed into the depletion region at the S/E junction creating electron-hole (e-h) pairs. The creation of the e-h pairs disrupts the equilibrium position attained ($E_{oREDOX} = E_F$) under dark condition and shifts in the E_F value to a new energy level (E_{Fn} or E_{Fp}) closer to the initial semiconductor Fermi level before contact with the electrolyte [133] as shown in Figure 3.11 (c). This results in the reductions in band bending and potential change due to Fermi level position alteration (ΔE) which corresponds to Equation 3.16 [133] for measurements taken under illuminated and dark conditions.

$$\Delta E = \left(\frac{1}{e}\right)\left|{}^*E_F - E_F\right| = E_{light} - E_{dark} \qquad \text{Equation 3.16}$$

Based on this understanding, the voltage across the semiconductor and the counter electrode are recorded under both dark and illuminated conditions. The difference between the voltages measured under illuminated (V_L) and dark (V_D) conditions represent the PEC signal or open circuit voltage of the semiconductor/electrolyte junction. It should be noted that PEC signal may give a zero value due to wide bandgap range in insulators, overlapping bandgap in conductors (metal) or the mid-gap positioning of the Fermi level in an intrinsic semiconductor.
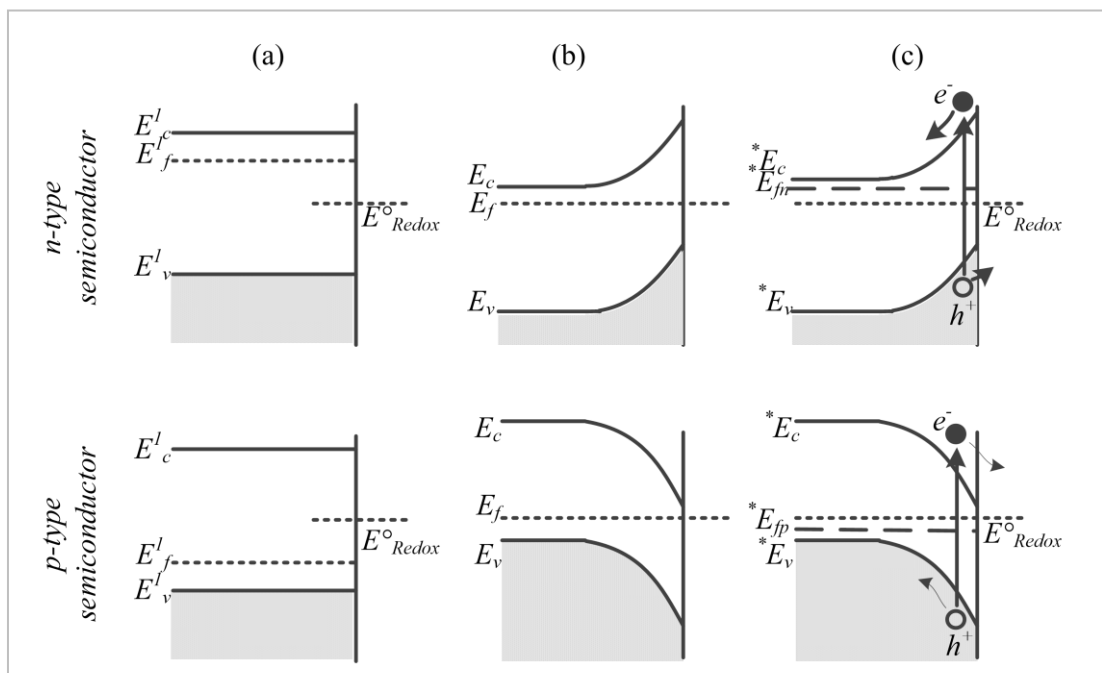
Figure 3.11: Band diagram formation between semiconductor and electrolyte (a) before the semiconductor makes contact with the electrolyte, (b) after the semiconductor makes contact with the electrolyte under dark condition and (c) after the semiconductor makes contact with the electrolyte under illumination condition.

3.4.8   Direct Current conductivity measurement technique

The DC conductivity measurement utilises Ohmic law concept in determining the electrical resistivity (ρ) and conductivity (σ) of semiconductor materials. This is achieved by forming two Ohmic contacts with the semiconductor material through careful metal contact selection. For Ohmic contacts to be formed, the difference between metal work function ϕ_m and semiconductor electron affinity χ_s should not

exceed ~0.40 eV [16]. In this technique, varying DC voltages between -1.00 V and 1.00 V are applied at constant steps across the two semiconductor terminals. The corresponding DC current that flows through the semiconductor material is measured using an ammeter. In this research work, the DC conductivity measurements were carried out using Keithley 2401 sourcemeter.
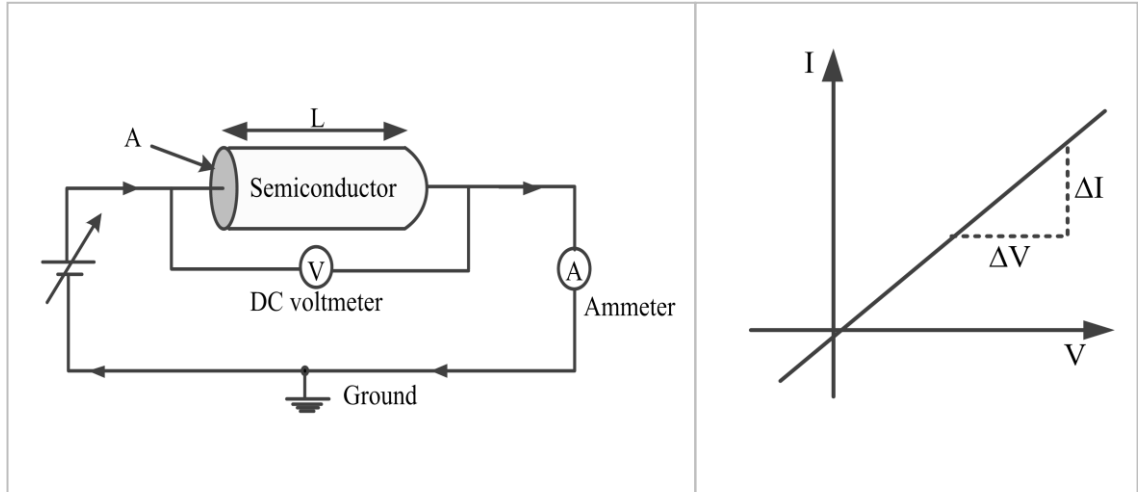
Figure 3.12: Typical schematic of circuit diagram used to measure DC conductivity of semiconductor thin films, (b) Typical I-V characteristics used to measure the resistance of a semiconductor.

The obtained (I-V) data give a straight line graph passing through the origin (0, 0) as shown in Figure 3.12. The slope inverse of the straight line graph gives the resistance R as shown in Equation 3.17.

$$R = \frac{\Delta V}{\Delta I}$$
Equation 3.17

It is well known that Resistance R and Resistivity ρ can be related according to Equation 3.18 [49]

$$R = \frac{\rho L}{A}$$
Equation 3.18

which can be rearranged as Equation 3.19

$$\rho = \frac{RA}{L}$$
Equation 3.19

Where ρ (Ω.cm) is the electrical resistivity, A (cm^2) is the cross-sectional area, and L (cm) is the thickness. Furthermore, resistivity ρ (Ω.cm) and conductivity σ (Ω.cm)$^{-1}$ are related according to Equation 3.20.

$$\sigma = \frac{1}{\rho}$$

Equation 3.20

3.5   Device characterisation techniques

After the optimisation of the semiconductor layers based on their material properties, electronic devices such as solar cells were fabricated. The electronic properties of the fabricated solar cell devices were explored using both the current-voltage (I-V) and capacitance-voltage (C-V) techniques. For both techniques, the bias range is set between -1.0 V to +1.0 V and the resulting current and capacitance are measured respectively. Both the I-V and C-V tests are non-destructive tests. The I-V characteristics were explored under both dark and illuminated (AM1.5) conditions, while the C-V characteristics were explored under dark condition. It should be noted that due to the underlying transparent conducting oxide (TCO) which is a prerequisite for electrodeposition technique, robust electronic characterisation technique such as Hall Effect measurement is unsuitable for the acquisition of electrical parameters required. Hence, the I-V and C-V characterisation techniques were explored as an alternative method to extract material properties such as doping concentration and charge carrier mobility.

3.5.1   Current-Voltage (I-V) characterisation

The use of current-voltage (I-V) technique for Schottky diode characterisation has been well explored in the determination of semiconductor electronic properties under both dark and AM1.5 illuminated conditions. Under dark condition, the obtained I-V data can be plotted as log-linear or linear-linear graphs. From the log-linear graphs, device parameters such as rectification factor (RF), ideality factor (n), saturation current (I_o) and potential barrier height (ϕ_b), can be determined while shunt (R_{sh}) and series (R_s) resistances can be determined from linear-linear I-V graphs. Other solar cell parameters such as open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF) and conversion efficiency (η) can be determined from the linear-linear I-V curve measured under AM1.5 illuminated condition. It should be noted that R_{sh} and R_s can be evaluated

under both dark and AM1.5 conditions, but due to the possible fluctuations of irradiation intensity under illuminated condition and its effect on other diode parameters [134], the R_{sh} and R_s obtained under dark condition is considered to be more viable.

A typical linear-linear I-V curve under illuminated condition iterating the effect of R_{sh} and R_s on the I-V curve and their equivalent circuits are shown in Figure 3.13. For an ideal diode, as shown in Figure 3.13 scenario (a), the R_{sh} and R_s equal infinity and zero respectively [49].
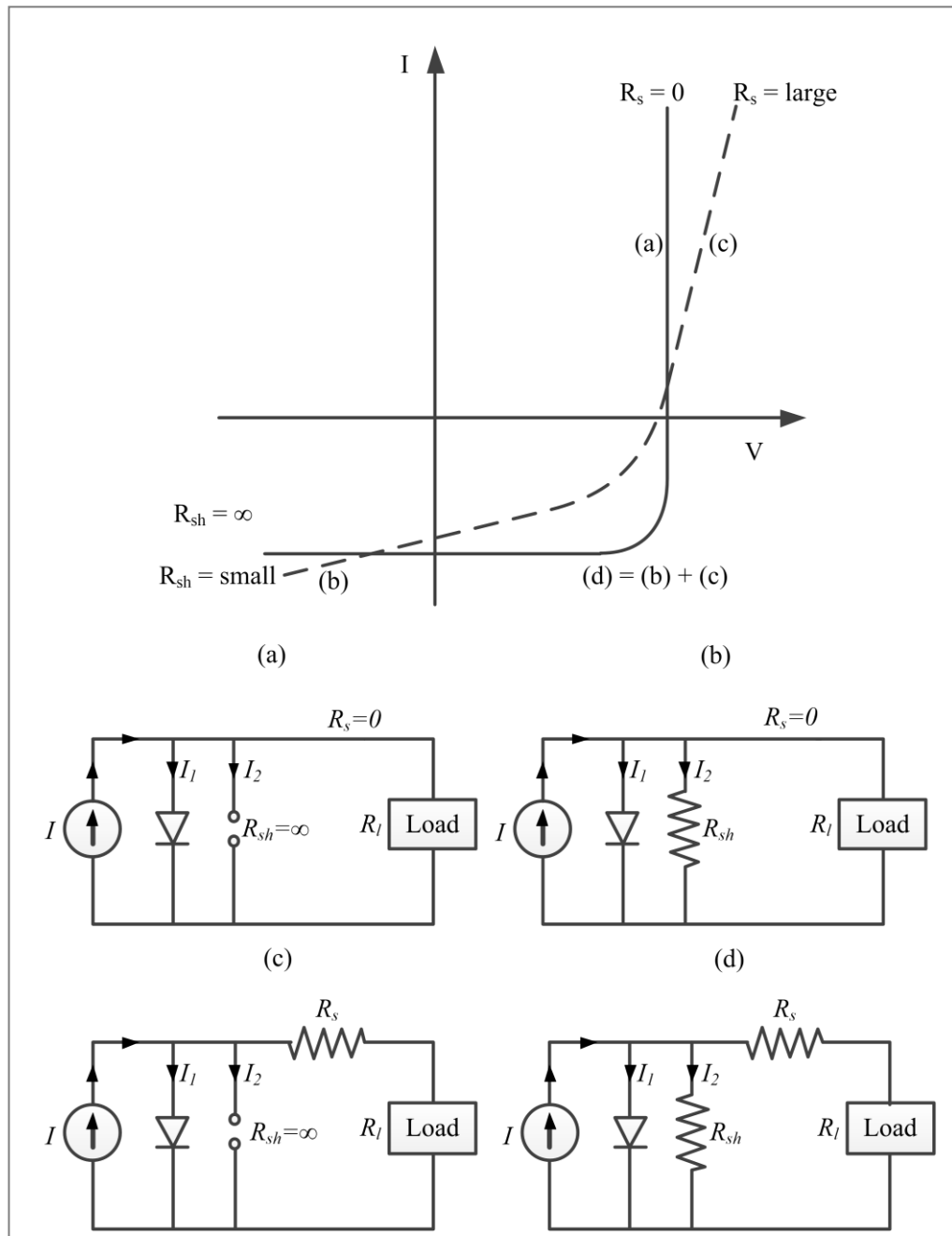
Figure 3.13: The effect of R_s and R_{sh} on I-V curves of PV solar cells and their single diode equivalent circuits.

In this case, the R_{sh} behave like an open circuit voltage and all the photo-generated current I flow only through the solar cell (represented by diode D) and resulting in the maximum possible current output. It should be noted that reductions in the R_{sh} as shown in Figure 3.13 scenario (b) will lead to the creation of an alternative flow path for current through which a fraction of the photo-generated current is lost through shunt. By Kirchhoff's law, the total photo-generated current I divide into I_1 and I_2. I_1 goes through the solar cell represented by a diode, D, while I_2 goes through the shunt path. Reductions in R_{sh} which is often related to the semiconductor material quality may also result in the reduction of other solar cell parameters such as FF and V_{oc} [135].

As shown in Figure 3.13 scenario (c), an increase in R_s results in voltage drop before the load. R_s is associated with M/S contact resistance, usage of highly resistive semiconductor material and the presence of excess oxide layer in between the M/S interface [136]. The main impact of R_s is the reduction of photon to electron conversion efficiency via J_{sc} and FF reduction [136]. The combination of scenarios (b) and (c) as shown in Figure 3.13 scenario (d) with low R_{sh} and high R_s results into a gradual reduction in V_{oc}, $J_{sc,}$ and FF which ultimately affects the efficiency of the solar cell.

3.5.1.1   I-V characterisation under dark condition

Under dark condition, solar cell devices behave like a diode due to the formation of semiconductor p-n junction or M/S Schottky contact. Typical linear-linear and log-linear I-V characteristic curves are shown in Figure 3.14. The I-V characteristics of Schottky type diode under dark condition can be expressed by Equation 3.21 [59].

$$I_D = SA^*T^2.\exp\left(\frac{-e\phi_b}{kT}\right)\left[\exp\left(\frac{eV}{nkT}\right)-1\right]$$ Equation 3.21

Where I_D is the electric current in dark condition (A), I_0 is the reverse saturation current (A), S is the area of the contact (m^2), A^* is the effective Richardson constant for thermionic emission ($Acm^{-2}K^{-2}$), T is the temperature (K), e is the electronic charge (1.60×10^{-19} C), ϕ_b is the potential barrier height (eV), k is the Boltzmann constant (1.38×10^{-23} JK^{-1}) and n is the ideality factor of the diode.

since $$I_0 = SA^*T^2.\exp\left(\frac{-e\phi_b}{kT}\right)$$ Equation 3.22
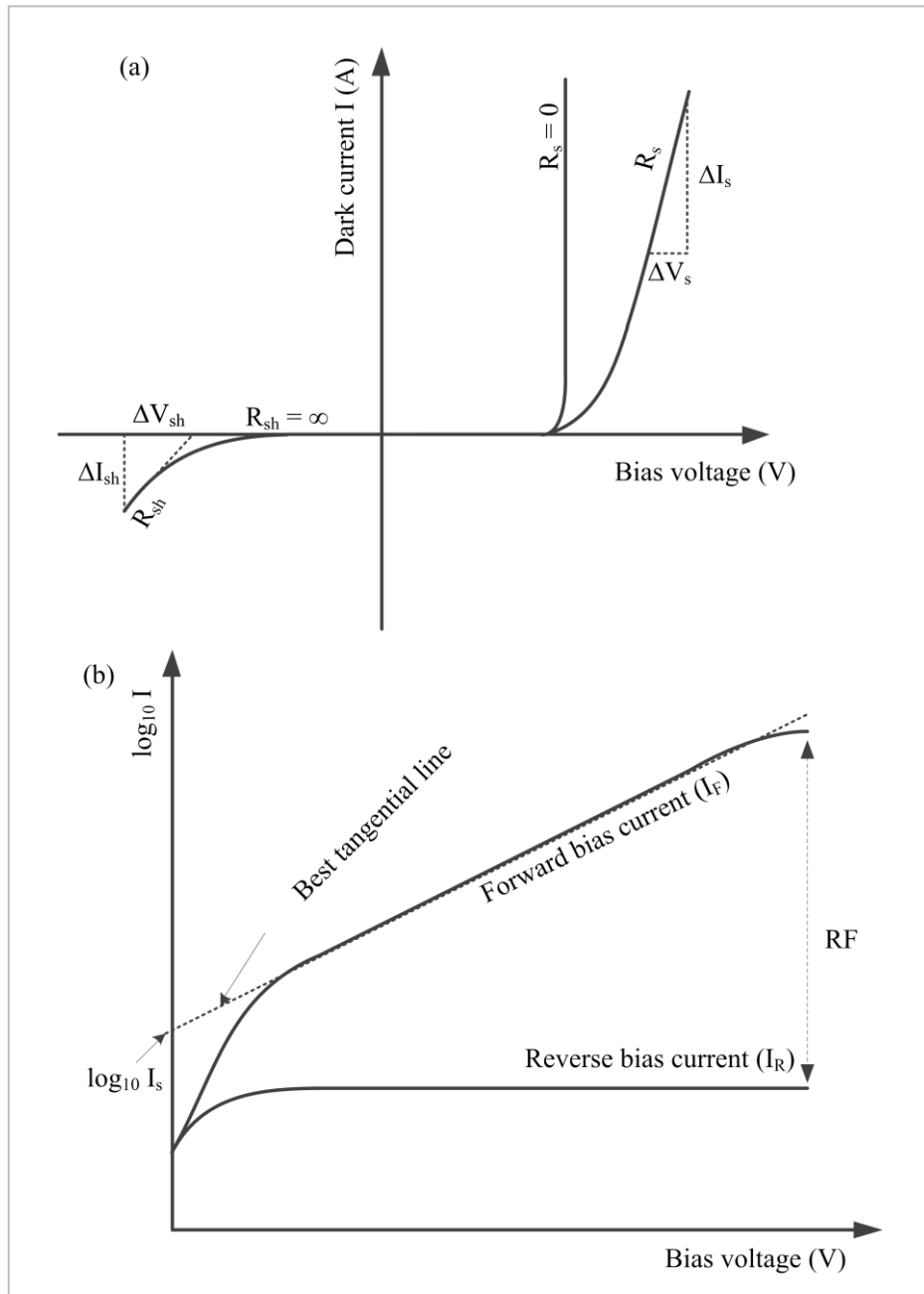
Figure 3.14: The plot of (a) linear-linear and (b) log-linear graphs of diodes measured dark condition.

$$\phi_b = \frac{kT}{e} \ln\left(\frac{SA^*T^2}{I_0} \right)$$ or   Equation 3.23

Equation 3.21 can be rewritten as

$$I_D = I_0 \left[\exp\left(\frac{eV}{nkT} \right) - 1 \right]$$ Equation 3.24

As reported by Rhoderick and Williams 1982 [59], if the applied voltage across the diode exceeds 75 mV, then

$$\exp\left(\frac{eV}{nkT}\right) \rangle\rangle \, 1$$

<div align="right">Equation 3.25</div>

Equation 3.24 can be rewritten as

$$I_D = I_0 . \exp\left(\frac{eV}{nkT}\right)$$

<div align="right">Equation 3.26</div>

or

$$\log_{10}(I_D) = \left(\frac{e}{2.303nkT}\right).V + \log_{10}(I_0)$$

<div align="right">Equation 3.27</div>

or

$$\ln I_D = \left(\frac{e}{nkT}\right)V + \ln I_0$$

<div align="right">Equation 3.28</div>

Therefore, from the plot of $\log_{10}(I_D)$ versus voltage applied (V) as shown in Figure 3.14 (b), parameters such as I_0, rectification factor (RF), ϕ_b and n can be obtained. The intercept of the best forward bias tangential line on the current axis gives the saturation current I_o, while the slope in the forward bias gives the value through which the ideality factor n was calculated using Equation 3.30 with the consideration that the largest gradient of the curve gives the lowest value of n [59]. The n value provides information on the current transportation mechanism such that for an ideal diode, where the current transport mechanism is through thermionic emission (n = 1.00). When n value is 2.00, then the current transport mechanism is entirely through recombination and generation (R&G), but if n value is between 1.00 and 2.00, then the current transport mechanism consists of both thermionic emission and R&G [59]. For n values above 2.00, the current transportation mechanism is not limited to thermionic emission and R&G but also due to the tunneling of high energy electron through the barrier height [137]. Large R_s value of the diode also contributes to the increase in n values.

$$slope = \frac{\Delta \log_{10} I}{\Delta V} = \frac{e}{2.303nKT}$$

<div align="right">Equation 3.29</div>

$$n = \frac{e}{KT}\left(\frac{1}{2.303 \times slope}\right) \cong \frac{16.78}{slope}$$

<div align="right">Equation 3.30</div>

The rectification factor *RF* which helps in determining the quality of a rectifying diode can be calculated as the ratio of forward current to reverse current at a constant voltage as estimated from the $\log_{10}(I_D)$ versus voltage (*V*) plot. As documented in the literature, *RF* values at an excess of 10^3 are sufficient for a high-performance solar cell [16]. The barrier height ϕ_b was calculated using Equation 3.23 and the effective Richardson constant A^* was calculated using Equation 3.31:

$$A^* = \frac{4\pi m^* k^2 q}{h^3}$$

Equation 3.31

Where m^* is the effective electron mass, and *h* is the Planck's constant (6.626×10^{-30} $cm^2 kgs^{-1}$). Depending on the conductivity type of the semiconductor, the effective electron mass can be denoted as m_e^* or m_p^* for *n*-type and *p*-type semiconductor material respectively. The effective electron masses of *n*-CdS, *n*-CdTe and *p*-CdTe are given by $0.21m_o$, $0.1m_o$ and $0.63m_o$ [138,139] respectively. The free electron mass $m_o = 9.1 \times 10^{-31}$ kg.

3.5.1.2   I-V characterisation under illumination

Under illuminated condition, the direction of flow of photo-generated current I_L is opposite to that of the forward current under dark condition I_D as shown in Figure 3.15. The total current of the ideal solar cell is illustrated in Equation 3.32.
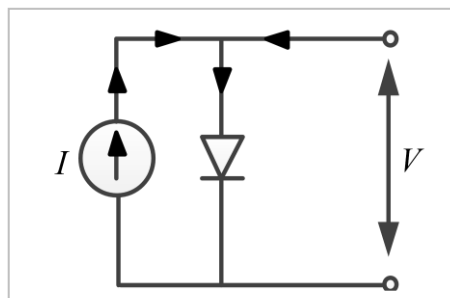
Figure 3.15: The equivalent circuit of an ideal solar cell.

$$I_L = I_D - I_{SC}$$

Equation 3.32

Where I_L is the load current, I_D is electric current in dark condition or the diode current, and I_{sc} is the photo-generated current. With the incorporation of I_D from Equation 3.24, Equation 3.32 can be rewritten as:

$$I_L = I_0 \left[\exp\left(\frac{eV}{nkT}\right) - 1 \right] - I_{sc} \qquad \text{Equation 3.33}$$

Under open circuit condition when I_L=0 and V=V_{oc} as shown in Figure 3.16, Equation 3.33 can be rewritten as:

$$0 = I_0 \left[\exp\left(\frac{eV_{oc}}{nkT}\right) - 1 \right] - I_{sc} \qquad \text{Equation 3.34}$$

or $\qquad I_{sc} = SA^*T^2 \left[\exp\left(\frac{-e\phi_b}{kT}\right) \right]\left[\exp\left(\frac{eV_{oc}}{nkT}\right) - 1 \right] \qquad$ Equation 3.35

By taking the natural logarithm of Equation 3.35 and noting that:

$$J_{sc} = \frac{I_{sc}}{S} \qquad \text{Equation 3.36}$$

Equation 3.35 can be rewritten as:

$$V_{oc} = n \left[\phi_b + \frac{kT}{e} \ln\left(\frac{J_{sc}}{A^*T^2}\right) \right] \qquad \text{Equation 3.37}$$

Equation 3.37 shows the dependence of increasing V_{oc} value on the increase of n and ϕ_b, values. However, due to the significance of n value on current transportation mechanism and its effect on J_{sc}, a limiting value of $n \leq 2.00$ is desirable for high-efficiency solar cell devices. It should be noted that in Schottky diodes, the V_{oc} of a solar cell device can also be improved by incorporating thin insulating layer between metal-semiconductor (M/S) contact to give an MIS structure [140,141] as discussed in Section 2.3.5, in which both the V_{oc} and the ϕ_b show considerable improvements. Furthermore, reduction in the temperature of solar cells can also improve V_{oc} value as a reduction in temperature minimises thermal agitation of the charge carriers [16,142].
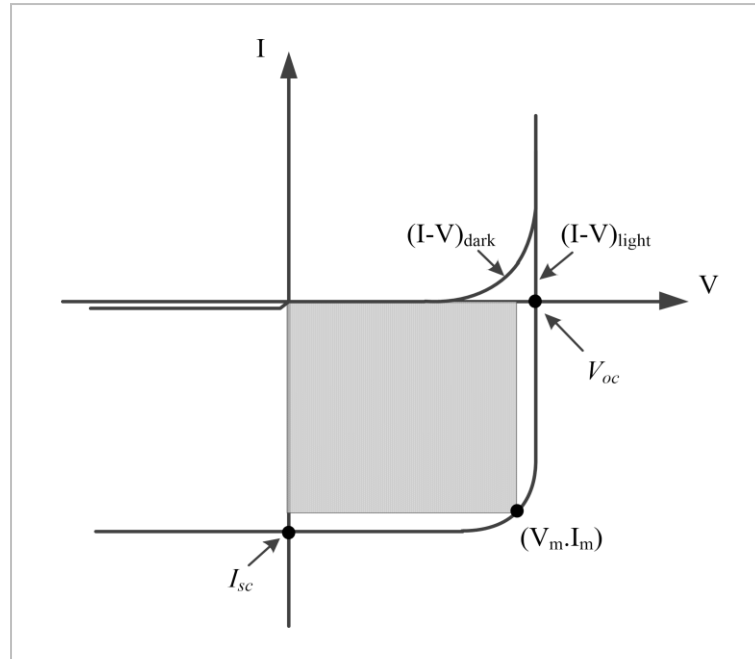
Figure 3.16: Typical I-V curve of solar cells measured under dark and illuminated conditions.

Another parameter which can be determined from the I-V curve under AM1.5 condition as shown in Figure 3.16 is the fill factor *FF*. The *FF* can be defined as the ratio of the maximum power P_{max} of the solar cell to the product of I_{sc} and V_{oc} as shown in Equation 3.38. Improvements in *FF* can be achieved with an increase in R_{sh} and reduction in R_s values. Maximum FF value can be attained under ideal diode condition where R_{sh} is ∞ and R_s=0 Ω.

$$FF = \frac{P_{\max}}{I_{sc}V_{oc}} = \frac{I_m V_m}{I_{sc}V_{oc}}$$
Equation 3.38

The efficiency of the solar cell (η) which can be defined as the ratio of power output P_{output} to power input P_{input} can be illustrated as shown in Equation 3.39.

$$\eta = \frac{Power\ output}{Power\ input} = \frac{V_m I_m}{P_{in}} = \frac{V_{oc} \cdot I_{sc} \cdot FF}{P_{in}}$$
Equation 3.39

Under standard AM1.5 illuminated condition, P_{input} is 1000 Wm^{-2} (100 mWcm^{-2}), therefore, Equation 3.39 can be rewritten as:

$$\eta = \frac{V_{oc} \cdot J_{sc} \cdot FF}{P_{in}}$$
Equation 3.40

All the I-V measurements for both AM1.5 illuminated (1000 Wm^{-2}) and dark conditions as reported in this thesis were performed using Rera Solution I–V measurement system in the ambient environment. The Rera Solution I–V measurement system is constituted of Keithley 2401 SourceMeter, LOT Quantum Design GmbH arc light source and a computer laptop running Rera Tracer IV software. The I-V system was precalibrated using RR267MON standard silicon solar cell.

3.5.2   Capacitance-Voltage (C-V) characterisation

Capacitance-Voltage (C-V) technique has been well explored in the literature and utilised for the determination of diode electronic properties, in which parameters such as capacitance at zero bias (C_o) can be directly determined from the C-V curve while other parameters such as Fermi level (E_F) position with respect to both the conduction (E_C) and valence bands (E_V), built-in potential (V_{bi}), doping concentration of donors (N_D) or acceptors (N_A), barrier height Φ_b, charge carrier mobility ($\mu_\perp$) and the depletion width at zero bias (W) [49] can be determined using Mott-Schottky plots. The Mott-Schottky plot is a graph of C^{-2} against V. For this report, the C-V technique was performed at 1 MHz due to the reduction in defect interference at high frequency [143], under dark condition due to noise caused by the high capture and emission of electrons at R&G centers [144] at room temperature.

Under reverse bias condition, *p-n* or Schottky junctions are identical to parallel plate capacitors. In which, the junction contains immobile electron-hole pairs within the depletion region and semiconductor material or metal (in the case of Schottky junction) serves as the electrode or conducting plates of the capacitor due to their reduced resistance as compared to the high resistance at the depletion region. The charged layer generated at the junction due to potential barrier formation is known as the junction capacitance. The junction capacitance, C of the depletion region is given by Equation 3.41.

$$C = \frac{\varepsilon_s A}{W} = \frac{\varepsilon_o \varepsilon_r A}{W} \qquad \text{Equation 3.41}$$

Where $\varepsilon_s = \varepsilon_o \varepsilon_r$ is the permittivity of semiconductor (Fcm^{-1}), ε_o is the permittivity of free space (8.85×10^{-14} Fcm^{-1}), ε_r is the relative permittivity (or the dielectric constant) of the semiconductor material (ε_r is 8.9 for ZnS, 8.9 for CdS and 11.0 for CdTe [145]), *A* is the

cell contact area, W is the width of depletion region (cm). The capacitance can also be expressed per unit area (C_A). Therefore Equation 3.41 can be rewritten as Equation 3.42.

$$C_A = \frac{C}{A} = \frac{\varepsilon_s}{W} = \frac{\varepsilon_o \varepsilon_r}{W}$$

Equation 3.42

The built-in potential can be estimated using Equation 3.43 and graphically shown in Figure 3.18 [47].

$$V_{bi} = \frac{kT}{e} \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

Equation 3.43

And the depletion width W is given by:

$$W = \sqrt{\frac{2\varepsilon_s}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) V_{bi}}$$

Equation 3.44

Where N_A is the acceptor concentration, N_D is the donor concentration, and n_i is the intrinsic concentration. The intrinsic concentration n_i defines the steady state situation of an intrinsic semiconductor under thermal agitation and constant electron excitation from E_v to E_c, in which the number of electrons in the conduction band equals the number of holes in the valence band.

For one-sided abrupt junction where the p-type semiconductor material is highly doped ($N_A \gg N_D$), the depletion region extends more into the n-type semiconductor material. Conversely, if the n-type semiconductor material is highly doped ($N_D \gg N_A$), the depletion region extends more into the p-type semiconductor material. Therefore, Equation 3.44 can be rewritten as Equation 3.45, where $N=N_D$ for $N_A \gg N_D$ and $N=N_A$ for $N_D \gg N_A$.

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{eN}}$$

Equation 3.45

It should be noted that Equation 3.44 and Equation 3.45 holds when there is no externally applied voltage (V) across the junction. In the presence of an externally applied voltage across the junction, the total voltage across the junction is (V_{bi}-V), where, V is positive for forward bias and negative for reverse bias [49]. Therefore, the

depletion width (*W*) under externally applied voltage for the one-sided abrupt junction is given by Equation 3.46.

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V)}{eN}}$$

Equation 3.46

Consequently, Equation 3.41 can be rewritten as Equation 3.47

$$C = \frac{\varepsilon_s A}{\sqrt{\dfrac{2\varepsilon_s(V_{bi} - V)}{eN}}} = A\sqrt{\frac{e\varepsilon_s N}{2(V_{bi} - V)}}$$

Equation 3.47

With respect to the depletion capacitance per unit area as shown in Equation 3.42, Equation 3.47 can be redefined as Equation 3.48.

$$C_A = \frac{C}{A} = \sqrt{\frac{e\varepsilon_s N}{2(V_{bi} - V)}}$$

Equation 3.48

Figure 3.17 shows the typical graph of capacitance per unit area (*C_A*) against bias voltage (*V*) from which the *C_o* capacitance per unit area at zero bias can be determined. It should be noted that the obtained *C_o* value from this graph is utilised in the calculation of the depletion width at zero bias using Equation 3.41.
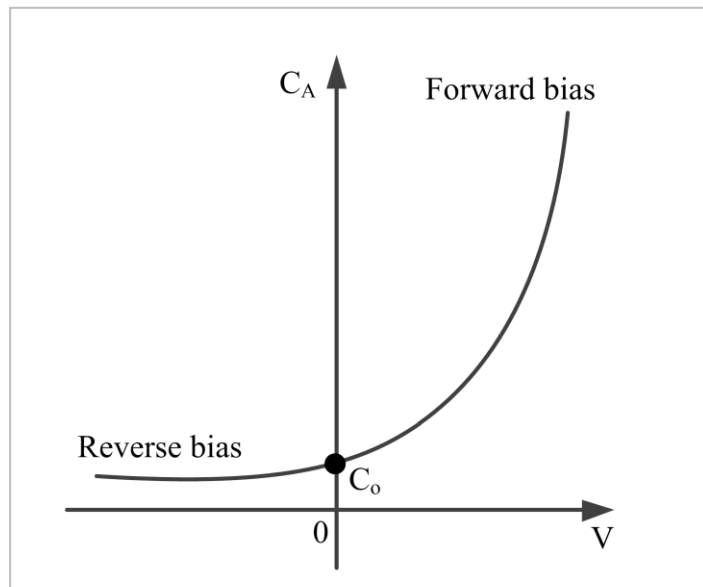
Figure 3.17: Schematic of typical plot of C_A against V under both forward and reverse bias conditions.

The equation defining the Mott-Schottky plot from which other parameters are determined can be achieved by squaring both sides of Equation 3.48 and rearranging it to give Equation 3.49, where V is either positive or negative for forward or reverse bias respectively.

$$C_A^2 = \frac{e\varepsilon_s N}{2(V_{bi} - V)} \text{ or } C^2 = \frac{e\varepsilon_s NA^2}{2(V_{bi} - V)}$$ Equation 3.49

Equation 3.49 can also be expressed as Equation 3.50

$$\frac{1}{C^2} = C^{-2} = \frac{2}{e\varepsilon_s NA^2}(V_{bi} - V)$$ Equation 3.50

As observed in Equation 3.50, a plot of C^{-2} against V for one-sided abrupt junction should produce a straight line [49] as shown in Figure 3.18 (a) due to its equivalence to straight line equation ($y = mx+c$) where m is the slope. But as a result of the effects of defects, traps, surface states, interfacial resistive layers (attributable to oxidation) producing excess capacitance and inhomogeneity of the semiconductor layer in the diode, deviation from linearity are usually observed [146] as shown in Figure 3.18 (b). The slope of the C^{-2} against V plot can be defined as shown in Equation 3.51, and the extrapolation to $C^{-2} = 0$ gives the built-in potential (V_{bi}).
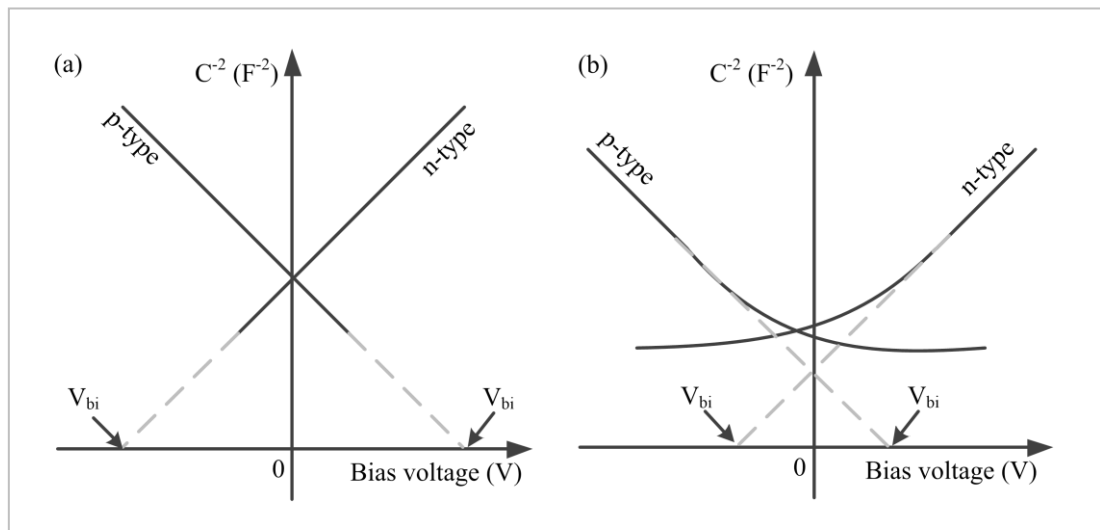
Figure 3.18: Typical Mott-Schottky plots of *p*- and *n*-type semiconductors (a) for an ideal diode and (b) non-ideal diode.

$$slope = \frac{2}{e\varepsilon_s NA^2}$$

Equation 3.51

Therefore, with the known value *m* (slope) and the V_{bi} from Mott-Schottky plot, the doping density (*N*) can be calculated by rearranging Equation 3.51 as Equation 3.52.

$$N = \frac{2}{\varepsilon_s eA^2 \cdot slope}$$

Equation 3.52

The effective density of states both in the conduction (N_c) and valence (N_v) bands are respectively shown in Equation 3.53 and Equation 3.54. The equations show the dependence of the effective density of states on temperature and the nature of semiconductor material. Therefore, the N_c and N_v values differ for different semiconductor materials and conductivity types.

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2}$$

Equation 3.53

$$N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2}$$

Equation 3.54

Where m_e^* and m_p^* are the electron and hole effective masses for *n*-type and *p*-type semiconductor materials respectively (with all parameters predefined in Section 3.5.1.1).

With the doping density N_A or N_D (Equation 3.52) and the effective density of states N_c and N_v as calculated from Equation 3.53 or Equation 3.54 derived from Mott-Schottky plot, the Fermi level E_F, charge carrier mobility $\mu_\perp$ and the barrier height ϕ_b can be calculated with the assumption that all excess donor (N_D) or acceptor (N_A) atoms are wholly ionised at room temperature as shown in Equation 3.55, Equation 3.56, Equation 3.57, and Equation 3.58. Therefore, the Fermi Dirac probability function of electrons occupying the donor state is $n \approx (N_D - N_A)$.

$$\Delta E = E_C - E_F = \frac{kT}{e}\ln\left(\frac{N_C}{N_D - N_A}\right)$$

Equation 3.55

or
$$\Delta E = E_F - E_V = \frac{kT}{e} \ln\left(\frac{N_V}{N_A - N_D}\right)$$
Equation 3.56

$$\mu_\perp = \frac{\sigma}{ne} = \frac{\sigma}{(N_D - N_A)e}$$
Equation 3.57

$$\Phi_b = V_{bi} + E_F + \frac{kT}{e}$$
Equation 3.58

The C-V measurements as reported in this thesis were performed using Hewlett Packard 4284A 20 Hz – 1 MHz Precision LCR Meter (Yokogawa Hewlett Packard, Japan) with a Keithley 6517A Electrometer/High Resistance Meter.

3.6   Conclusion

This chapter discussed the main semiconductor deposition technique utilised in this report. It further expatiates on the techniques employed in the analysis and investigation of the deposition voltage, elemental deposition sequence, structural, morphological, compositional, optical and the electrical properties of the semiconductors. The analysis and investigation are aimed at optimising both growth and treatment conditions for device purposes. Further to material properties, both I-V and C-V techniques were also utilised for the charcaterisation of the fabricated devices. The results presented in this thesis using the techniques mentioned above were repeatedly performed to ascertain the reproducibility of similar trends. Errors bars were also utilised in the displayed results where appropriate.

Chapter 4 -   CdS deposition and characterisation

4.1   Introduction

The study of the structural, optical, morphological and physical properties of binary compound semiconductors such as cadmium sulphide (CdS) thin films is a subject of current interest due to its applications in optoelectronic and large area electronic devices. In photovoltaics, polycrystalline CdS thin films are often used as a window layer in the CdS/CdTe solar cells configuration to achieve high conversion efficiency. CdS thin films have been grown using over ten different techniques [147] as reported in the literature with electrodeposition edging other deposition based on its simplicity, low cost, scalability amongst other attributes [16]. The electrodeposition of CdS as reported in the literature is done mainly by using Sodium thiosulfate ($Na_2S_2O_3$) as the sulphur precursor. This precursor is associated with the formation of sulphur precipitates during growth and the accumulation of sodium, Na, in the electrolytic bath [148]. The incorporation of p-type dopants such as Na into CdS layers through absorption or chemical reaction will reduce the electrical conductivity of the grown layer and thus constitute a drawback in the electrical property of the CdS layer [148]. Therefore, in view of depositing CdS from other sulphur precursors without the aforementioned drawbacks, other sulphur sources need to be explored. Sulphur source such as thiourea (NH_2CSNH_2) have been well established in the growth of CdS using chemical bath deposition (CBD) technique, but the literature on the use of the electrochemical technique for this precursor is scarce. The electrodeposition (ED) technique is comparatively advantageous with respect to deposition process continuity and Cd-containing waste reduction. Although, preliminary investigation of the electrodeposition of CdS from thiourea was explored in 2001 by Yamaguchi et al. [149], this chapter presents in full the comprehensive details of the growth and characterization of CdS from NH_2CSNH_2 precursor and further investigates the effect of $CdCl_2$ treatment, film thickness and heat treatment duration on the electronic quality of electrodeposited CdS layers.

This chapter goes beyond the growth and characterisation norm into the comparative analysis of the electronic properties of electrodeposited CdS using thiourea precursor to CBD-CdS and single crystal CdS previously reported in the literature.

4.2   Electrolytic bath and substrate preparation for CdS

4.2.1   Electrolytic bath preparation

CdS thin films were cathodically electrodeposited on glass/FTO substrates by the potentiostatic technique in which the counter electrode was a high purity graphite rod. Cadmium chloride hydrate ($CdCl_2 \cdot xH_2O$) of 98% purity and thiourea (NH_2CSNH_2) of 99% purity were used as cadmium and sulphur sources respectively. The electrolyte was prepared by dissolving 0.12 M $CdCl_2$ xH_2O and 0.18 M NH_2CSNH_2 in 800 ml deionised (DI) water contained in a 1000 ml polypropylene beaker. The polypropylene beaker was placed in an 1800 ml glass beaker containing DI water. The glass beaker serves as the outer bath and helps to maintain uniform heating of the electrolyte. The ED bath described is a mimic of the setup as discussed in Section 3.3. The solution was stirred and electro-purified for ~50 hours to reduce the impurity level and to achieve homogeneity of the solution. The electrolytic bath containing 0.12 M $CdCl_2$ xH_2O and 0.18 M NH_2CSNH_2 in 800 ml DI water will be referred to as CdS bath henceforth.

Afterwards, a complete characterisation of the CdS grown at different voltages was undertaken to determine the optimum growth voltage (V_g). For these experiments, the bath temperature was maintained at 85°C during the CdS growth to achieve higher crystallinity due to high deposition temperature [104]. However, the temperature increase is limited due to the use of aqueous solution. The pH value was adjusted to 2.50±0.02 at the start of deposition using diluted solutions of HCl and NH_4OH for all the samples. It is essential to maintain the pH of the electrolytic bath between 2.00 and 3.00 as an increase or decrease in pH outside this range results into the formation of white precipitates of cadmium hydroxide and rapid precipitation of CdS respectively [150]. The two-electrode configuration was used in this study with glass/FTO as the working electrode. The working electrodes of sheet resistance ~7 $\Omega/\square$ were cut into 2×4 cm^2 pieces, and a high purity carbon rod was used as the anode. A computerized Gill AC potentiostat was utilised as the power supply source. The cyclic voltammograms of the resulting electrolyte(s) were recorded before the deposition of CdS layer to determine the possible deposition voltage range of CdS.

4.2.2   Substrate preparation

Substrates were ultrasonically cleaned at the initial stage in soap solution for 20 minutes and rinsed in deionised (DI) water. The substrates were then cleaned thoroughly with methanol and acetone to remove any grease and rinsed in DI water. Finally, the FTO is

submerged in a clean beaker of DI water and transferred directly into the electroplating bath. Prior to characterisation, electrodeposited CdS layers were rinsed, dried and divided into two halves. Half were left as-deposited, and the other half were $CdCl_2$ treated at 400˚C in the air to enhance both their material and electronic properties. The $CdCl_2$ treatment was performed by adding few drops of aqueous solution containing 0.1 M $CdCl_2$ in 20 ml of DI water to the surface of the semiconductor layer. The full coverage of the layers with the treatment solutions was achieved by spreading the solution using solution-damped cotton bud. The semiconductor layer was allowed to air-dry and heat treated at 400°C for 20 minutes. Both the as-deposited and $CdCl_2$ treated CdS layers were characterised afterward for both their material and electronic properties.

4.3   Growth and voltage optimization of CdS

Asides the glass/FTO substrate utilised for cyclic voltammetry, the CdS layers were electrodeposited between the deposition voltages 789 mV and 793 mV for 2 hours per sample. The deposition range was determined based on information obtained via cyclic voltammetry (see Section 4.3.1).

4.3.1   Cyclic voltammetric study

The cyclic voltammogram is a plot of current density as a function of the applied voltage across an electrolytic bath. Figure 4.1 shows the cyclic voltammogram of an aqueous solution of a mixture of 0.12M $CdCl_2 \cdot xH_2O$ and 0.18 M NH_2CSNH_2 in 800 ml of DI water during the forward and reverse cycles between 100 and -2000 mV cathodic voltage at pH 2.50 ± 0.02 and a fixed scan rate of 3 mVs^{-1}. The stirring rate and temperature of the bath were kept constant at 300 rpm and 85˚C respectively.

According to the redox potential value of cadmium and sulphur ions, sulphur deposits first (with an E˚ value of -0.43 V w.r.t. standard H_2 electrode), followed by cadmium (with an E˚ value of -0.40 V w.r.t. standard H_2 electrode). The complete electro-chemical equation for the formation of CdS at the cathode can be written as Equation 4.1.
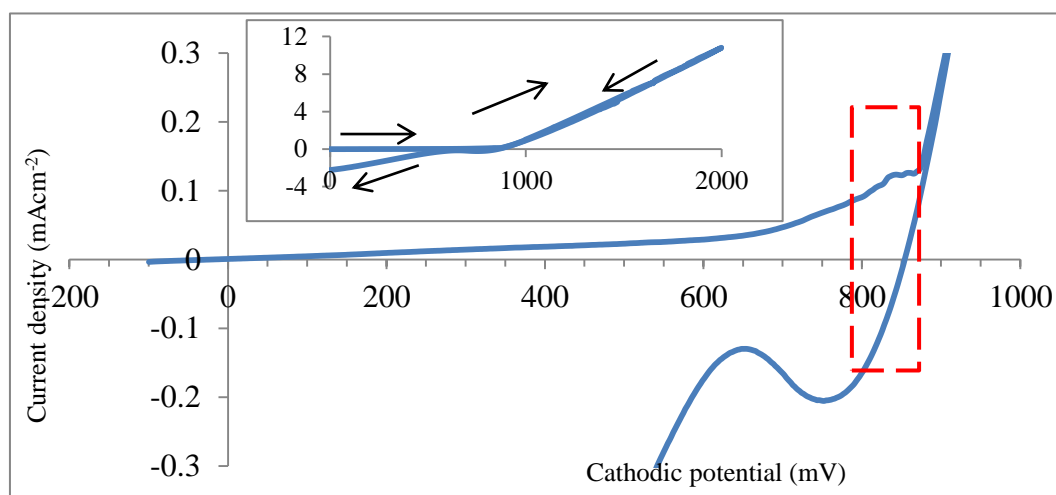
Figure 4.1: A typical cyclic voltammogram for deposition electrolyte containing the mixture of 0.12 M $CdCl_2 \cdot xH_2O$ and 0.18 M NH_2CSNH_2 at ~85˚C and pH=2.50±0.02. The inset shows the full cyclic voltammogram measured between (0 to 2000) mV.

$$Cd^{2+} + S_2O_3^{2-} + 2e^- \rightarrow CdS + SO_3^{2-}$$ Equation 4.1
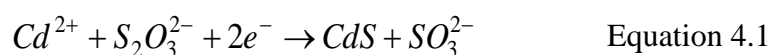
It was observed in the forward cycle that between the cathodic voltage range 785 mV and 880 mV, the deposition current density appears to be fairly stable within the range of ~130 μAcm^{-2}. The growth voltage range (i.e., 785 mV to 880 mV) had been pre-characterized at cathodic voltage steps of 10 mV using XRD analysis (the result is not presented in this thesis). The highest XRD peak intensity was observed at 790 mV. Therefore, the surrounding cathodic voltage was scanned at steps of 1 mV to investigate surrounding growth voltage values further. The result of the characterised CdS layers grown between the cathodic voltages of (788–793) mV using PEC cell measurement, optical absorbance, and transmittance measurement, XRD and SEM were used to determine the optimum growth conditions.
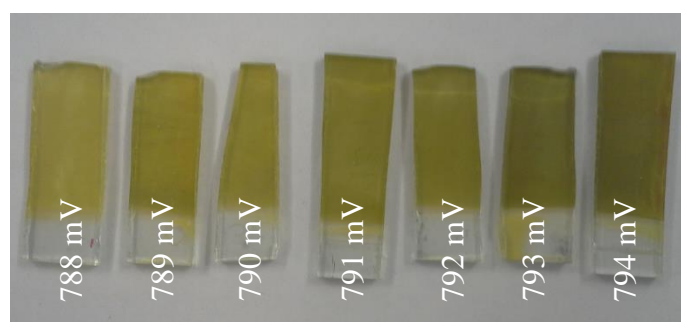
Figure 4.2: The physical appearances of as-deposited CdS grown at V_g from 788 mV to 794 mV grown for 20 minutes each.

It was also observed during the voltammetric cycle that the deposited film colour changes to transparent yellow at growth voltages (V_g) ≤780 mV which suggests a region of sulphur richness. The deposited film colour turns to greenish-yellow at growth voltage above 780 mV which indicate the presence of stoichiometric or near stoichiometric CdS thin films. As the growth voltage increases above 793 mV, the film colour changes to dark green as shown in Figure 4.2. This can be attributed to Cd richness in CdS. Above 880 mV cathodic voltage, high current density is observed with a detrimental effect on the ED-CdS layer quality. The sharp increase in current density might be due to the electrolysis of water and the deposition of Cd dendrites.

Based on observation, the stoichiometric CdS thin film range can be qualitatively predicted by appearance during the voltammetric cycle. But, exploring other material characterisation techniques are still required for quantitative assessment of the deposited CdS layers at different cathodic voltages. It was interesting to observe no sulphur precipitation throughout these sets of experiments which is one of the problems associated with other sulphur precursors in the electrodeposition of CdS [151,152].

4.3.2   X-ray diffraction study

After preliminary growth and characterization, CdS layers were grown between (788–793) mV cathodic voltages at 1 mV step change so as to comb the cathodic voltages surrounding the predetermined 790 mV to identify the stoichiometric or near stoichiometrically grown CdS layer. For this work, each CdS samples were grown for the same time duration and $CdCl_2$ treated under the same condition. The observed XRD peaks/crystallinity for both the as-deposited and $CdCl_2$ treated CdS layers within the cathodic voltage range of (788–793) mV were compared as shown in Figure 4.3 (a), Figure 4.3 (b), Figure 4.4 and Figure 4.5.

As observed in Figure 4.3, all the as-deposited CdS layers were polycrystalline with a preferred peak orientation along the CdS (002)H plane which coincides with the FTO peak at angle 2θ=26.68˚. The as-deposited CdS layers were polycrystalline with peak orientations corresponding to CdS (100)H at 2θ=24.90˚, CdS (002)H at 2θ=26.68˚, CdS (101)H at 2θ=28.86˚, CdS (220)C at 2θ=46.98˚, CdS (103)H at 48.01˚, Cd (101)H at 2θ=38.89˚ and S (319)O at 2θ=42.63˚ present. This indicates the inclusion of elemental Cd and S, together with cubic CdS phase within the main phase of hexagonal CdS. The preferred peak orientation along the CdS (002)H plane coincides with FTO peak at 2θ=26.68˚. Due to the effect of the FTO peak on the CdS (002)H peak intensity, CdS

(101)H at $2\theta=28.86°$ with the second predominant peak intensity was utilised as the preferred peak for analysis of the CdS layers. After $CdCl_2$ treatment, peaks identified as Cd (101)H at $2\theta=38.89°$, S (319)O at $2\theta=42.63°$ and CdS (220)C at $2\theta=46.98°$ completely disappears as observed in Figure 4.3 (b) and Figure 4.5. This can be attributed to the diffusion and evaporation of excess sulphur, the formation of CdS from the reaction between elemental Cd and S to form hexagonal-CdS and the instability of cubic phase CdS after heat treatment [153,154]. A substantial increase in XRD peak intensity of CdS in hexagonal phases was also observed after $CdCl_2$ treatment except for CdS (103)H as shown in Figure 4.5.

It is well documented in the literature that CdS can grow in two different crystalline structures, namely the hexagonal (wurtzite structure) and the cubic (zinc blend structure) with the hexagonal being the more metastable phase [153,154]. Hence, the hexagonal CdS phases were retained after $CdCl_2$ treatment at 400°C for 20 minutes. The initial presence of CdS in both hexagonal and cubic phases in the as-deposited layers may be attributed to vigorous stirring during growth at low temperature as argued by Kaur et al. [8]. All the hexagonal phases of CdS in the as-deposited layer showed a substantial increase in intensity after $CdCl_2$ treatment except for CdS (103)H as shown in Figure 4.5. These alterations in the XRD peak intensity might be due to the reorientation of the crystal lattice during heat treatment in the presence of $CdCl_2$ [9].

A plot of preferred orientation (CdS(101)H) peak intensity against cathodic voltage for both as-deposited and $CdCl_2$ treated samples, as depicted in Figure 4.4, shows that the highest peak intensity was attained at 791 mV under the conditions used in this work. This observation signifies the possibility of growing stoichiometric or near-stoichiometric CdS at 791 mV away from the S-rich CdS obtained at V_g lower than 791 mV or Cd-rich CdS obtained at V_g higher than 791 mV as explained in Section 4.3.1. The extracted XRD data from these CdS material work matches the JCPDS reference file No. 01-080-0006 and 00-001-0647 for both the hexagonal and cubic phases respectively. The crystallite size, D was calculated using the Scherrer's formula as shown in Equation 3.8. The summary of the XRD data and obtained structural parameters of the CdS (101)H preferred diffraction orientation for layers grown between 780 mV and 800 mV is shown in Table 4.1, while Table 4.2 summarises all the XRD diffractions observed for CdS thin film layer grown at V_g=791 mV.
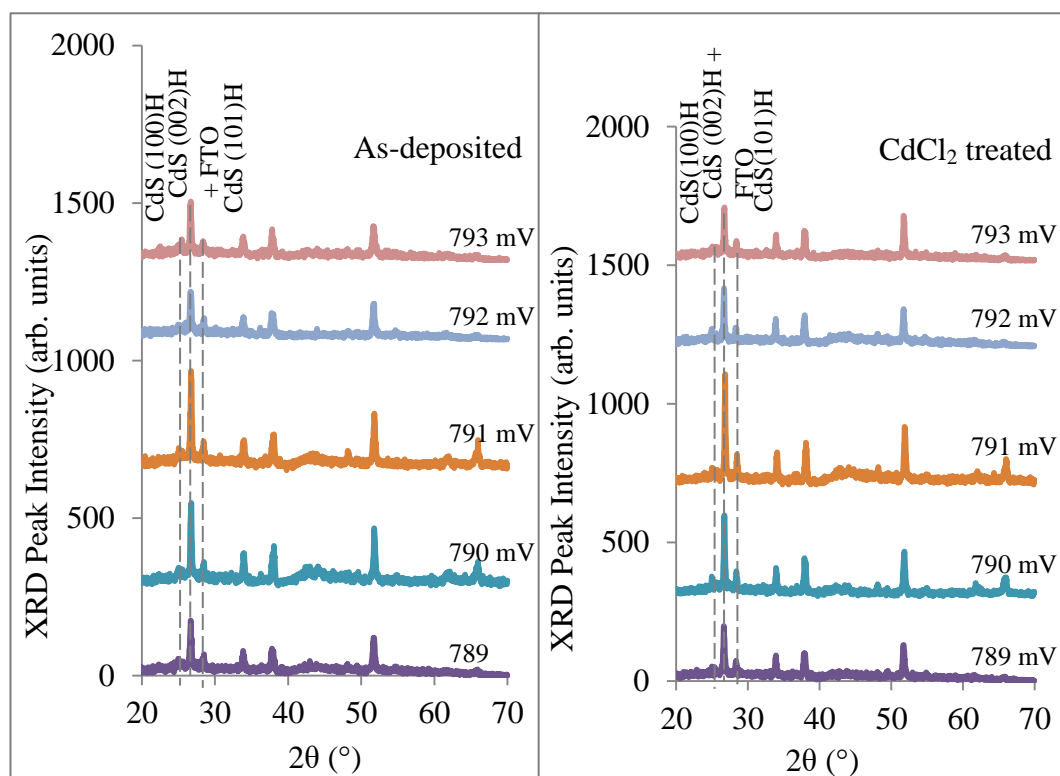
Figure 4.3: Typical XRD patterns of CdS layers grown between 789 mV and 793 mV deposition potential for (a) As-deposited CdS layers (b) CdCl$_2$ treated CdS layers at 400˚C for 20 minutes.
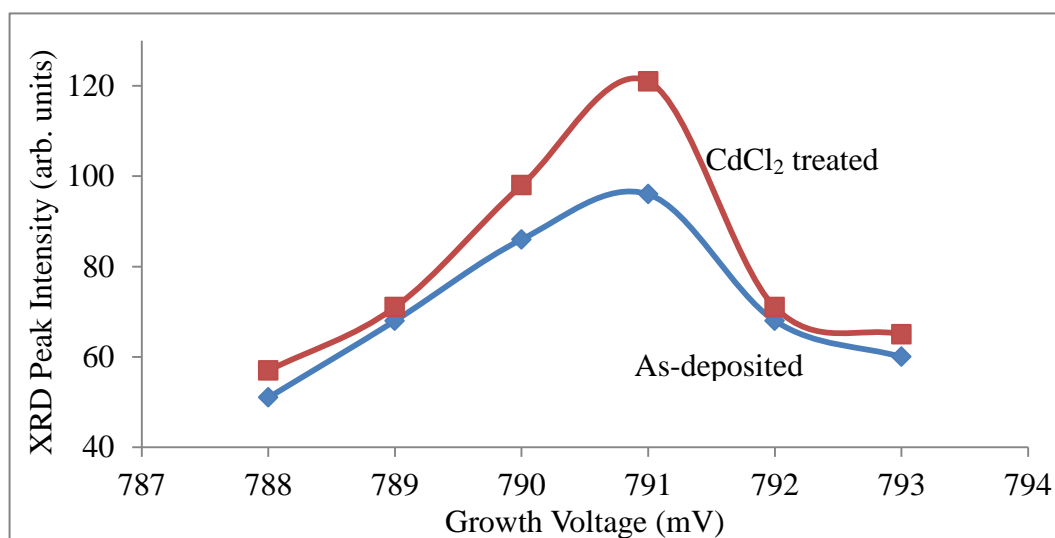
Figure 4.4: Comparative analysis of CdS (101)H peak for as-deposited and CdCl$_2$ treated layer grown at different growth voltages between 788 and 793 mV.
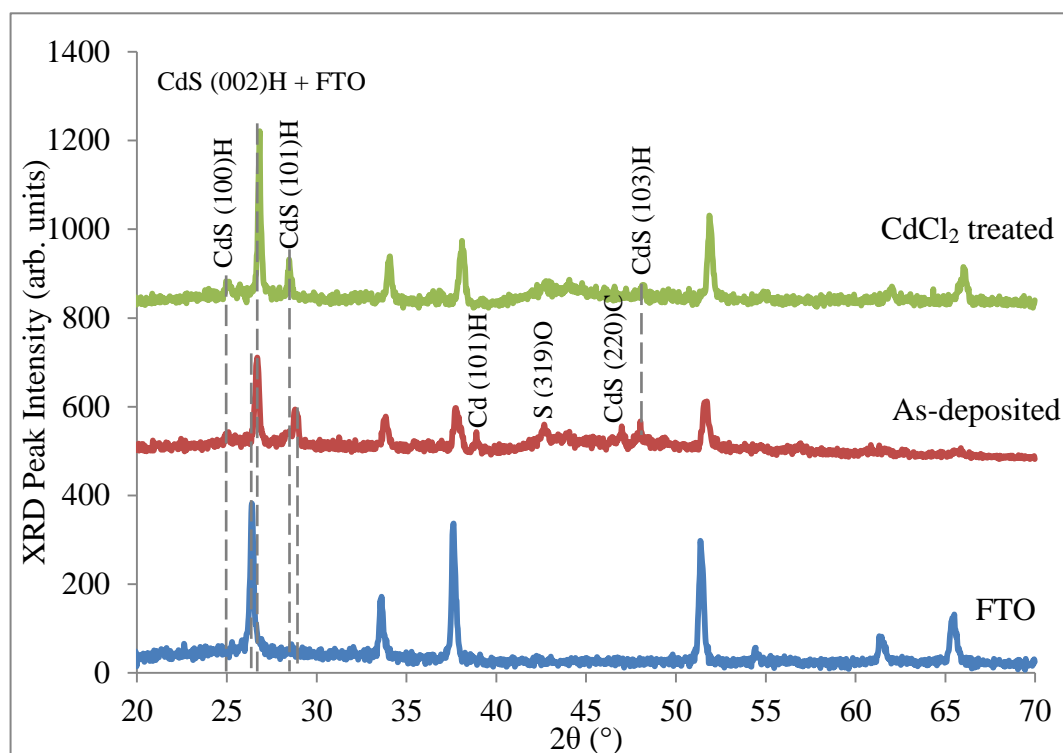
Figure 4.5: Comparative analysis of XRD peaks from as-deposited and CdCl$_2$ treated CdS layers grown at 791 mV.

Table 4.1: The XRD analysis of CdS layers grown between cathodic potential of 780 mV and 800 mV for the as-deposited and the CdCl$_2$ treated layers at 400˚C for 20 minutes in air.

Growth voltage (mV)	2θ (°)	Lattice Spacing (Å)	FWHM (°)	Crystallite Size D (nm)	Plane of Orientation (hkl)	Assignments
As-deposited						
780	28.4	3.14	0.389	21.9	(101)	Hexagonal
789	28.47	3.13	0.259	32.9		
790	28.43	3.13	0.259	32.9		
791	28.83	3.09	0.194	44.0		
792	28.39	3.14	0.259	32.9		
793	28.44	3.14	0.259	32.9		
800	28.36	3.14	0.389	21.9		
CdCl$_2$ treated						
780	28.41	3.13	0.389	21.9	(101)	Hexagonal
789	28.34	3.14	0.194	43.9		
790	28.34	3.14	0.194	43.9		
791	28.45	3.13	0.129	65.9		
792	28.42	3.14	0.195	43.9		
793	28.31	3.15	0.195	43.9		
800	28.38	3.14	0.195	43.9		

Table 4.2: The XRD analysis of CdS layers grown at cathodic potential of 791 mV for the as-deposited and the $CdCl_2$, heat-treated layers at 400˚C for 20 minutes in air.

Sample	2θ (°)	Lattice Spacing (Å)	FWHM (°)	Crystallite Size D (nm)	Plane of Orientation (hkl)	Assignments
As-Deposited						
	24.90	-	-	-	(100)	Hex CdS
	26.69	3.34	0.227	37.5	(002)	Hex CdS/FTO
	28.83	3.09	0.195	44.0	(101)	Hex CdS
	38.92	2.31	0.195	45.2	(101)	Hex Cd
	42.64	2.12	0.390	22.9	(319)	Orth S
	47.00	1.93	0.260	34.8	(220)	Cubic CdS
	48.02	1.89	0.195	46.7	(103)	Hex CdS
$CdCl_2$ treated						
	25.07	3.55	0.260	32.7	(100)	Hex CdS
	26.80	3.32	0.130	65.7	(002)	Hex CdS/FTO
	28.45	3.13	0.130	65.9	(101)	Hex CdS
	48.17	1.88	0.162	56.0	(103)	Hex CdS

For the CdS layers grown between 780 nm and 800 nm as shown in Table 4.1, calculated crystallite sizes ranging between (21.9–44.0) nm for the as-deposited and (21.9 – 65.9) nm for the $CdCl_2$ treated CdS layers were observed. Apart from the CdS layer grown at 780 mV, an increase in the crystallite sizes of all the CdS layers was observed after $CdCl_2$ treatment. This observation might be due to the coalescence of crystallites and recrystallisation, reduction in strain/stress resulting in an overall improvement in the structural properties of CdS layers after $CdCl_2$ treatment. Under the as-deposited and $CdCl_2$ conditions, the highest crystallite sizes were observed at 791 mV.

4.3.3   Raman study

Figure 4.6 shows typical Raman spectra of ~500 nm thick layers of both as-deposited and the $CdCl_2$ treated samples of CdS. In this spectra, strong scattering due to the longitudinal optical (LO) vibration mode was observed for both the as-deposited and $CdCl_2$ treated layers. For the as-deposited CdS layer, the dominating 1LO peak was

observed at ~303 cm^{-1} while a broad 2LO peak was observed at ~604 cm^{-1}. The 1LO and 2LO peaks for the CdCl$_2$ treated samples were observed at ~300 cm^{-1} and 602 cm^{-1} respectively. The slight red shift observed in the 1LO and 2LO peak positions after heat treatment at 400°C for 20 minutes in the presence of CdCl$_2$ in the air is logged in Table 4.3. This shift in Raman peaks can be attributed to internal dislocation and extrinsic defect in CdS layer as a result of tensile or compressive stresses [153]. Tensile and compressive stresses affect the Raman spectrum by a red shift and a blue shift [155]. Furthermore, the obtained FWHM from the Raman spectra shows a reduction in its value after CdCl$_2$ treatment which is an indication of an improvement in the crystallinity and increased the grain size of the treated layer. This analytical trend is consistent with that observed from the XRD analysis.
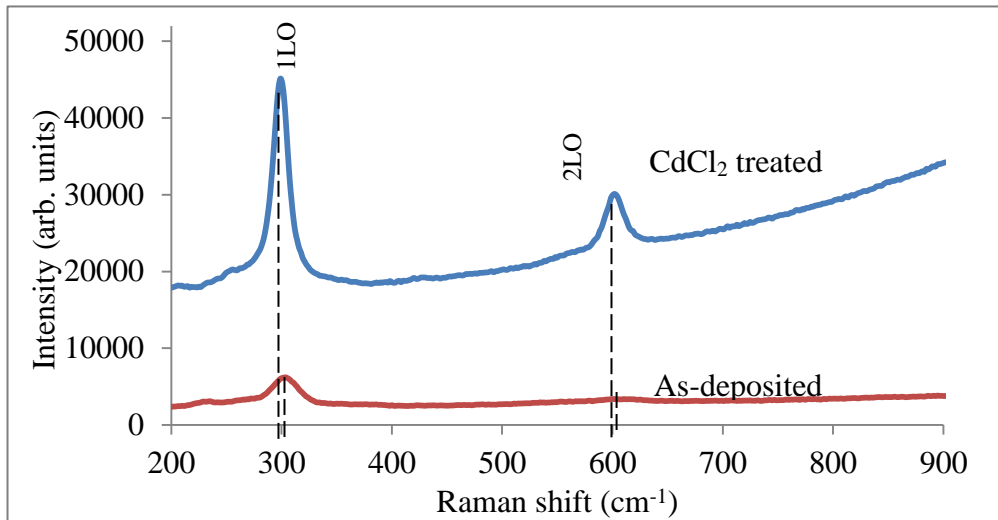
Figure 4.6: Raman spectra of as-deposited and CdCl$_2$ treated CdS thin films grown at 791 mV.

Table 4.3: Raman Analysis of As-deposited and CdCl$_2$ Treated CdS layers.

	As-deposited CdS		CdCl$_2$ Treated CdS	
	1LO	2LO	1LO	2LO
Raman peak position (cm^{-1})	303	604	299	601
Intensity (arb. unit)	3645.7	390.6	26017.0	7504.7
FWHM	28.73	51.44	16.28	20.71

4.3.4   Thickness measurements

The thickness measurement of layers grown between (787 to 793) mV was carried out both theoretically and experimentally. The theoretical measurement was estimated using Faraday's law of electrolysis as discussed in Section 3.3 and shown in Equation 3.6. The number of electrons transferred n for the deposition of 1 molecule of CdS is 2 (that is, $n=2$ for CdS). The experimental thickness measurement was carried out using UBM Microfocus optical depth profilometer (UBM, Messtechnik GmbH, Ettlingen, Germany). It was observed in Figure 4.7 (a) that the value of the measured thickness was lower than the calculated thickness using Faraday's law of electrolysis. This can be attributed to the assumptions made in Faraday's law of electrolysis that all the electronic charges contribute to the deposition of CdS. This assumption is without any consideration of the electronic charge contribution from the decomposition of water into its constituent ions at voltages above 1230 mV [156].
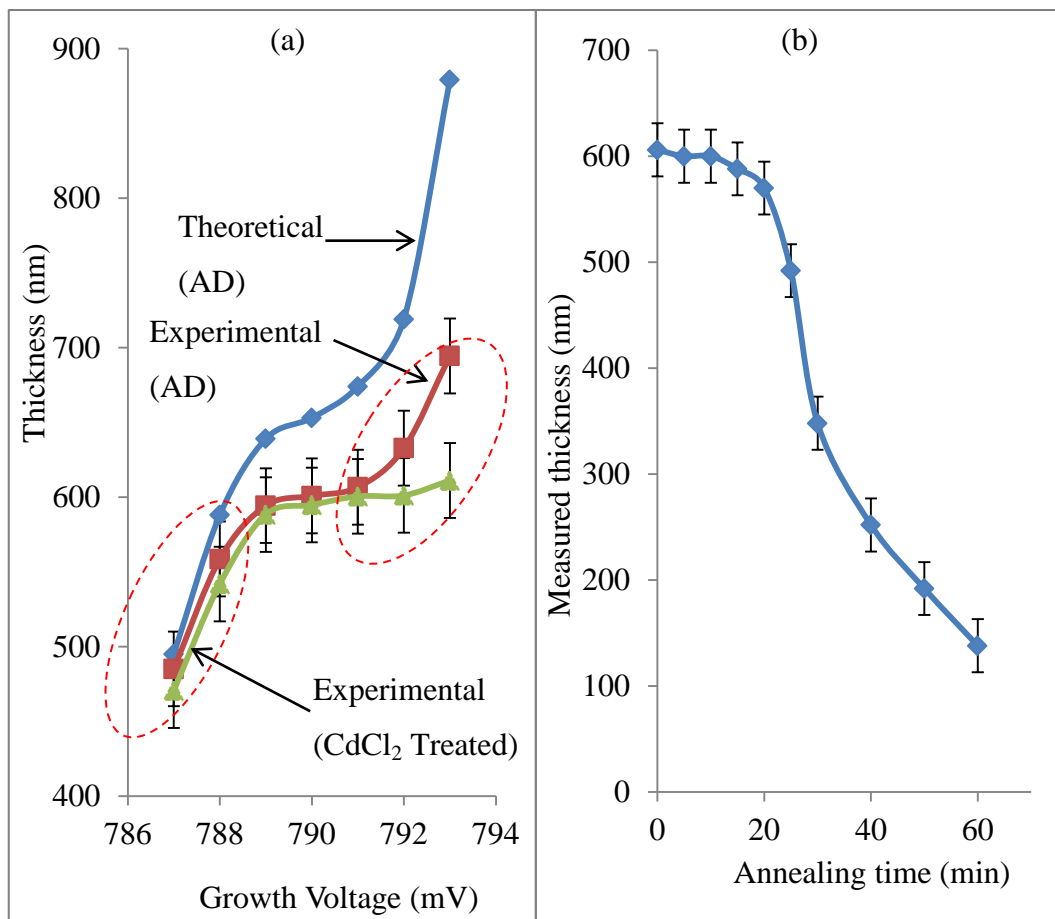
Figure 4.7: (a) Graph of CdS layer thickness (theoretical and experimental) against growth voltages for both as-deposited and CdCl$_2$ treated CdS layers and (b) graph of measured CdS layer thickness against different annealing duration in air at 400˚C in the presence of CdCl$_2$.

It was also observed that the growth current density increases with an increase in growth voltage and therefore results in increased film thickness and also changes were observed in the coloration of the deposited film. It is worth noting that for these experiments, all the CdS layers were grown for the same time duration and heat treated under the same condition. As shown in Figure 4.7 (a), after heat treatment at 400˚C for 20 minutes in the presence of $CdCl_2$, the thickness of the samples grown at 787 and 788 mV show a slight reduction in thickness which might be a result of the loss of sulphur from the S-rich CdS layers. The thickness of the samples grown between (789 and 792) mV remained virtually unchanged which might be attributed to stoichiometric or near-stoichiometric nature of the grown layer within this range. The layers grown above 791 mV shows a sharp reduction in thickness as a result of the sublimation of cadmium from the Cd-rich CdS layer. This observation indicates that stoichiometric CdS can withstand the heat treatment, but either S-rich CdS or Cd-rich CdS layer easily breakdown and sublime under the same conditions.

Further experimentations were performed to determine the effect of heat treatment duration in the presence $CdCl_2$ as shown in Figure 4.7 (b). A reduction in thickness due to sublimation of CdS layer was observed after 20 minutes and a sharp reduction after 25 minutes heat treatment duration. Based on this result, heat treatment of CdS in the presence of $CdCl_2$ above 20 minutes results in layer deterioration and sublimation of the CdS layer and might result into pin-hole formation.

4.3.5 Optical property analyses

The optical absorbance measurements were carried out on samples grown between (787 and 793) mV for both the as-deposited and the $CdCl_2$ treated samples. This characterisation was performed to determine the energy bandgap of each CdS layer and its conformity with the energy bandgap of the bulk CdS. The spectra of optical absorbance for the CdS thin films grown at different voltages for as-deposited and $CdCl_2$ treated samples are shown in Figure 4.8 (a) and Figure 4.8 (b). The square of absorbance (A^2) was plotted against the photon energy (hv) and the extrapolated straight-line section of the graph to the photon energy axis at A^2=0 gives an estimate of the bandgap energy. As observed, the as-deposited CdS layers grown within the explored growth voltage range show bandgaps ranging between 2.41±0.03 eV as shown in Figure 4.8 (a) and Table 4.4. The $CdCl_2$ treated samples grown within the same growth voltage range show a bandgap range between 2.41±0.01 eV. This slight

reduction in the bandgap range after CdCl$_2$ treatment might be attributed to pin-hole removal, re-crystallization of the lattice structure and improvement in material composition. Notably, the growth voltages surrounding 791 mV shows the comparatively sharp difference in the bandgap. This might be due to the insulative property of sulphur due to its richness as observed at low V_g and the metallic behaviour of cadmium due to its richness at high V_g. It was interesting to see that the layer grown at 791 mV shows 2.42 eV bandgap which is comparable with the standard bandgap for bulk CdS.
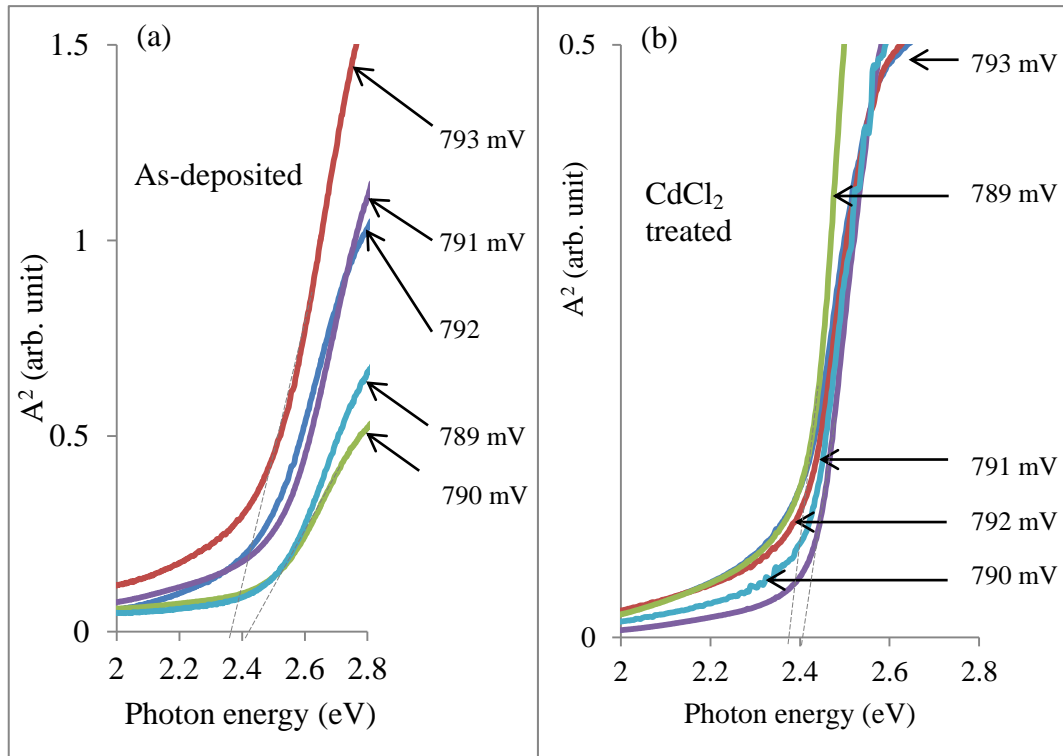
Figure 4.8: Optical absorption spectra for electrodeposited CdS thin-films between voltage range 789 to 793 mV for (a) as-deposited, and (b) CdCl$_2$ treated CdS at 400˚C for 20 minutes in air.

Table 4.4: The optical bandgap and transmittance of CdS layers grown at cathodic potentials between 789 mV and 793 mV for the as-deposited and the CdCl$_2$ treated layers at 400˚C for 20 minutes in air.

Growth voltage (mV)	789	790	791	792	793
Band gap for as-deposited CdS (eV)	2.45	2.44	2.42	2.42	2.39
Band gap CdCl$_2$ treated CdS (eV)	2.41	2.41	2.42	2.41	2.40
Transmittance for AD-CdS (%)	58	57	47	47	43
Transmittance for CdCl$_2$ treated CdS (%)	79	76	76	63	61

Also in Table 4.4, it was observed that the growth voltages outside the predetermined/explored range show bandgap values which were not close to the bulk-CdS value of 2.42 eV. This might be attributed to the richness of sulphur or cadmium in the grown CdS layers. Figure 4.9 shows the transmittance of the explored growth voltage range after heat treatment at 400°C for 20 minutes in the presence of CdCl$_2$. It is worth mentioning that all the samples show transmittance above 60% for wavelength larger than 512 nm.
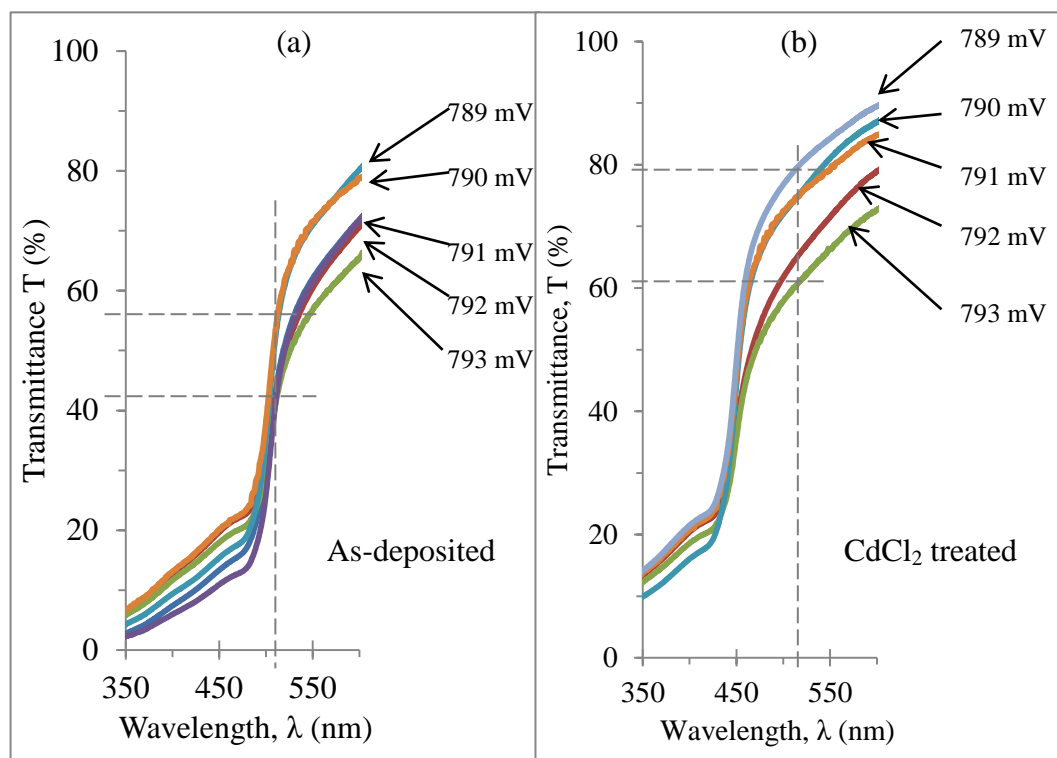
Figure 4.9: Optical transmittance spectra for electrodeposited CdS thin-films between voltage range 789 to 793 mV for (a) as-deposited, and (b) CdCl$_2$ treated at 400°C for 20 minutes in air.

4.3.6   Morphological studies

Figure 4.10 (a), Figure 4.10 (b) and Figure 4.10 (c) show the as-deposited (AD) SEM images of CdS layers grown between 789 mV and 793 mV, while Figure 4.10 (d), Figure 4.10 (e) and Figure 4.10 (f) show micrographs of the CdCl$_2$ treated CdS grown between 789 mV and 793 mV. All the layers were electrodeposited for 2 hours on glass/FTO substrates. From observation, all the as-deposited and CdCl$_2$ treated CdS layers explored show full coverage of the underlying glass/FTO substrate. For the as-deposited layers, slightly higher grain sizes were observed when grown at 791 mV within the range of (180 to 225) nm as compared to layers grown at 798 mV and 793

mV within the range of (130 to 200) nm. This observation which shows a hint of higher crystallinity at 791 mV, might be due to the improvement in the Cd/S stoichiometry toward 1/1 ratio. After CdCl$_2$ treatment, grain growth was observed for all the CdS layers explored. This observation is often associated with improvement in elemental composition, crystallinity, defect passivation, sublimation of excess elemental concentration, [30,157] amongst others.
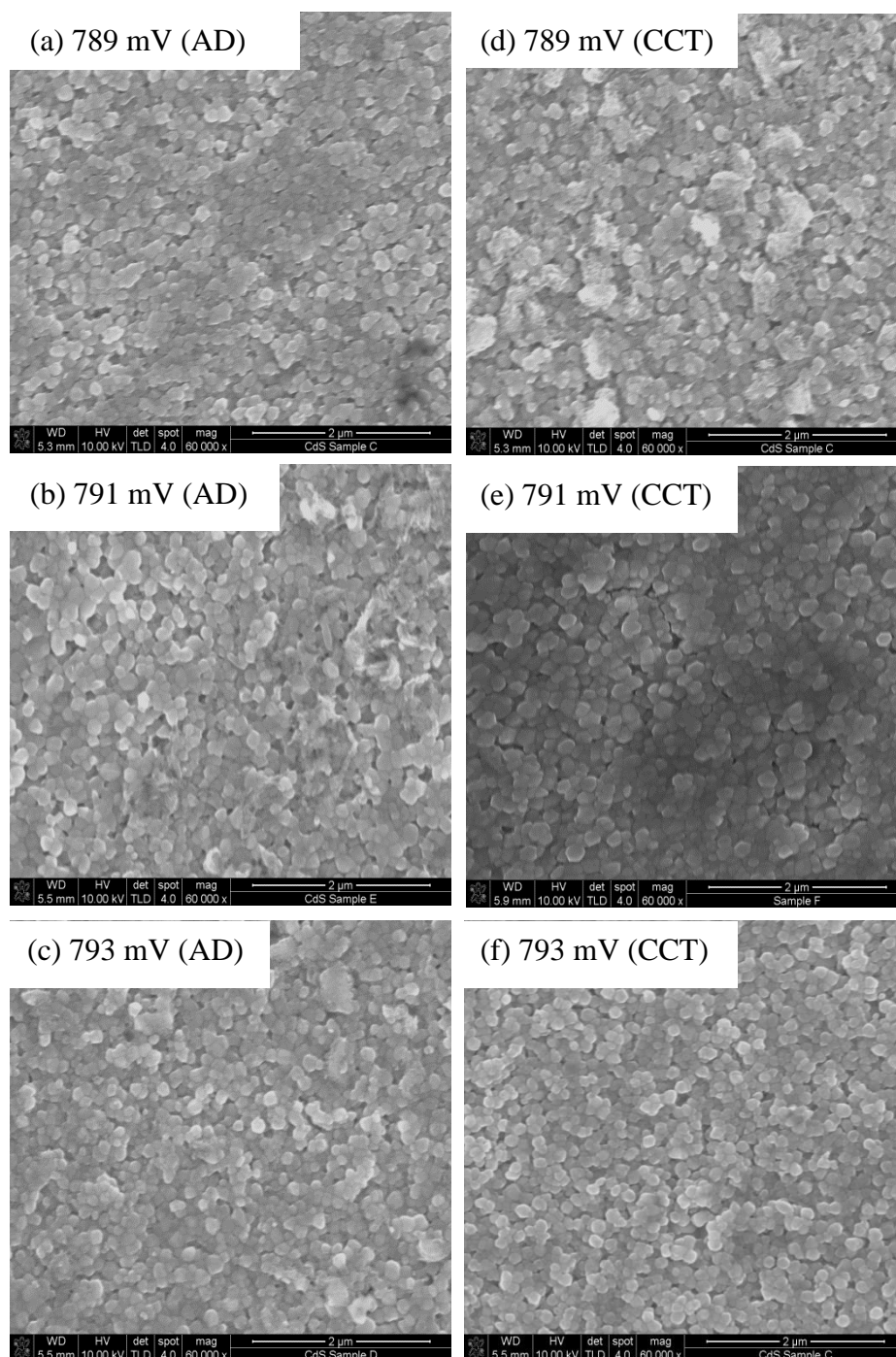
Figure 4.10: SEM micrographs of as-deposited (AD) and CdCl$_2$ treated (CCT) CdS layers grown at different voltages in the vicinity of 791 mV.

For the CdS layer grown at 789 mV, the underlying glass/FTO substrates were observed which might be due to the sublimation of excess elemental sulphur. Such gaps/pinholes may serve as shunt paths and reduction in device performance.

4.3.7   Compositional analysis

EDX measurements were performed to determine the atomic composition of Cd and S for both the as-deposited and $CdCl_2$ treated CdS films. Seven samples were grown at different cathodic voltages within the range of 788 to 794 mV at 1 mV step and used for the analysis. Figure 4.11 summarises the atomic ratio of Cd to S in CdS layers grown at different growth potentials as observed in EDX. The presence of other elements such as Sn and Cl were also noted. This is due to the underlying glass/FTO layer and the presence of chlorine in the CdS deposition bath and the $CdCl_2$ treatment as described in Section 4.2.1.
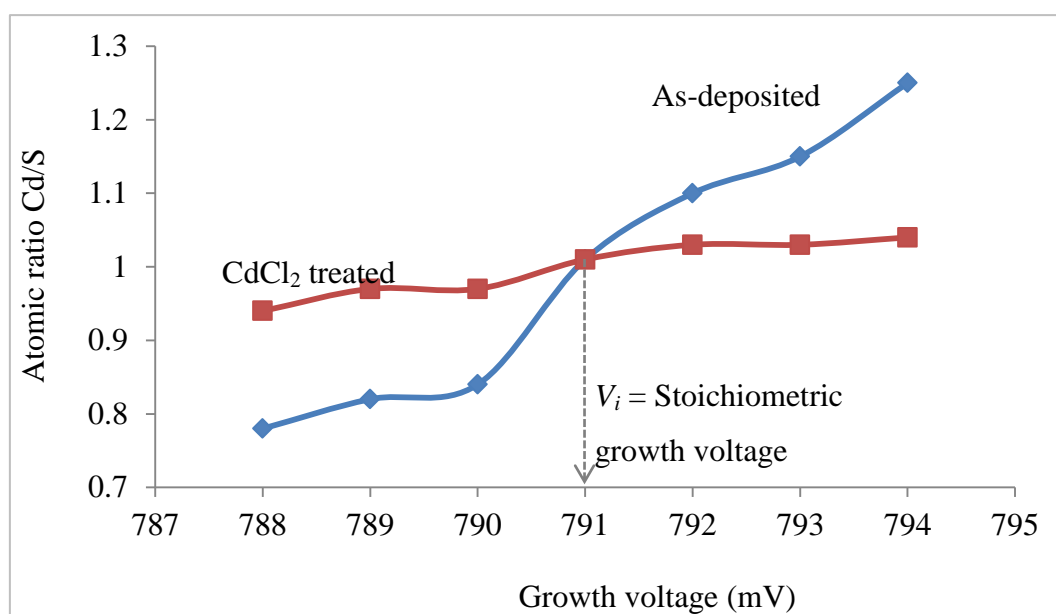
Figure 4.11: Graphical representation of percentage compositions ratio of Cd to S atoms in as-deposited and $CdCl_2$ treated CdS thin films at different deposition cathodic voltages.

As illustrated in Figure 4.11, S-rich CdS layers were observed when grown at voltages below 791 mV (V_i) with atomic ratios of Cd/S less than 1.0. This obtained data confirms the S-richness of CdS. A gradual increase in Cd content incorporated into CdS layer was observed with increasing growth voltage. Stoichiometric CdS was observed at 791 mV for both the as-deposited and the $CdCl_2$ treated layers with the Cd/S atomic ratio

equal to 1.01. It was interesting to observe that after $CdCl_2$ treatment, both the S-rich and the Cd-rich CdS tends toward stoichiometry. This observation further shows that $CdCl_2$ treatment improves CdS layer properties by reaction between unreacted Cd and S, and the sublimation of excess element from the layer. The result obtained in this section is in agreement with the visual, structural and optical observations earlier discussed in Sections 4.3.1, 4.3.2 and 4.3.5.

4.3.8   Photoelectrochemical (PEC) cell measurement

Figure 4.12 shows the PEC cell measurements of CdS layers grown between the cathodic voltages of (787 and 793) mV under both as-deposited and $CdCl_2$ conditions. As observed in Figure 4.12, both the as-deposited and the $CdCl_2$ treated layers were all *n*-type in electrical conduction. The *n*-type conductivity nature of CdS layers has been reported in the literature as an intrinsic donor defects in CdS layers [50,158]. This is due to the presence of Cd interstitials and S vacancies in the crystal lattice of the deposited CdS layers.
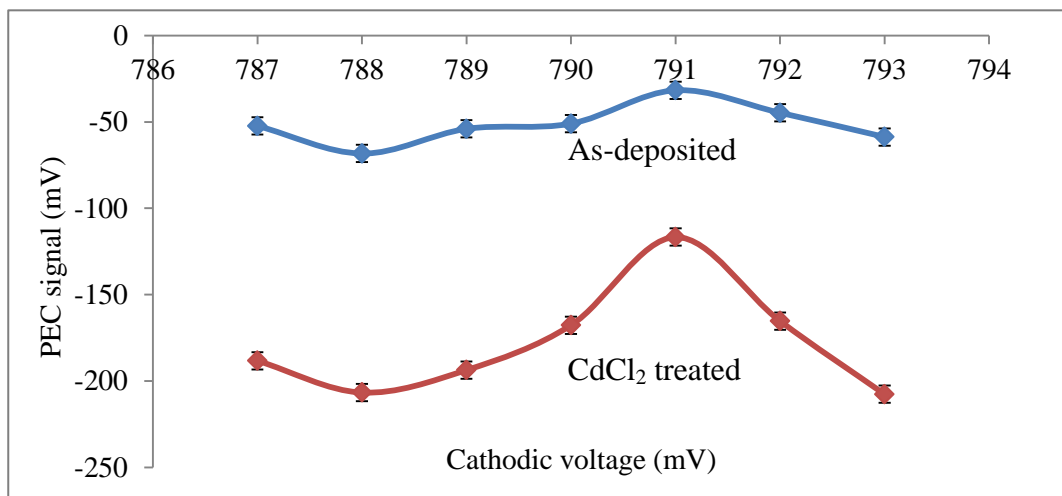
Figure 4.12: PEC signals for layers grown at different cathodic voltages, showing *n*-type electrical conductivity type for all samples investigated within explored conditions.

The magnitudes of the PEC signals in the $CdCl_2$ treated layers were higher than in the as-deposited layers. This might be as a result of the improvement of the depletion layer at the CdS/electrolyte junction due to the enhancement of the electronic quality of the CdS layer.

4.4   Effect of CdS thickness

For this experiment, only the CdCl$_2$ treated CdS layer will be discussed due to the triviality of the as-deposited layers. CdS layers grown at 791 mV cathodic voltage with thicknesses ranging from 50 nm to 200 nm on glass/FTO substrate were explored. The layers were CdCl$_2$ treated for 20 minutes at 400°C. The characteristic observations are discussed herein.

4.4.1   X-ray diffraction study based on CdS thickness

Figure 4.13 (a) shows the XRD micrograph of glass/FTO/CdS with variation in the CdS thickness between 50 nm and 200 nm, while Figure 4.13 (b) shows the both the H(101) CdS peak intensity and calculated crystallite size as a function of CdS layer thickness.
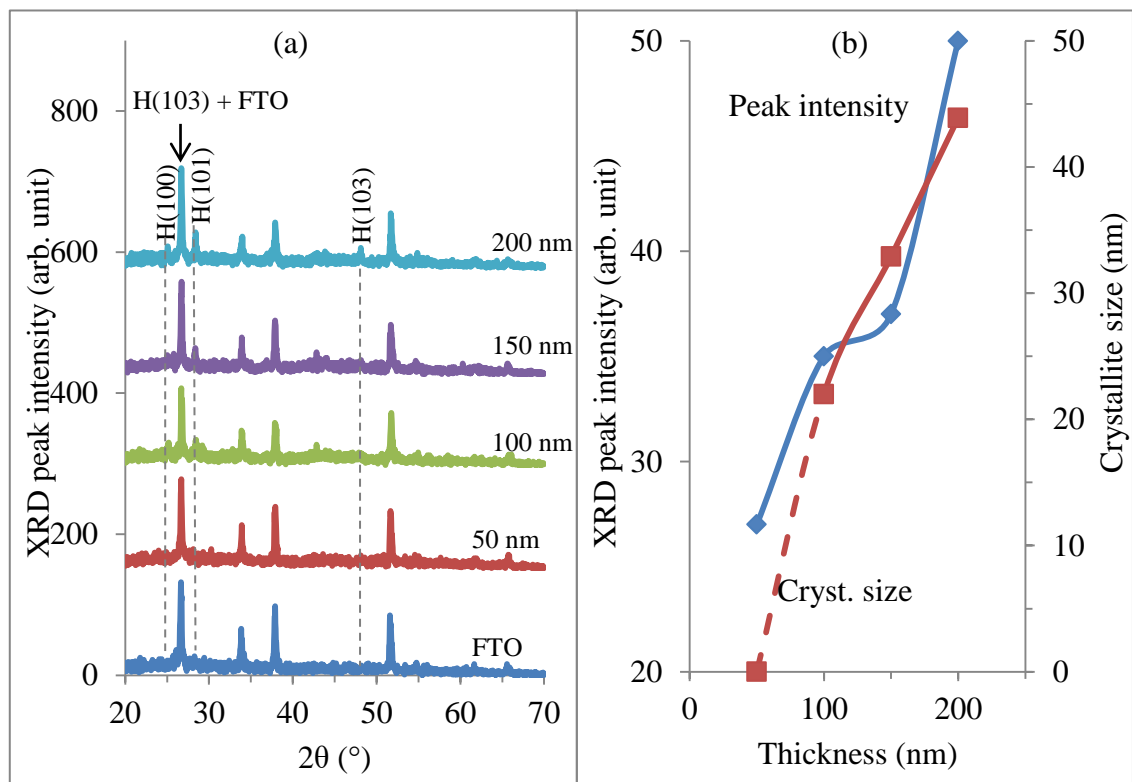
Figure 4.13: (a) Typical XRD patterns of different CdS layers with increasing thickness after CdCl$_2$ treatment and (b) Analysis based on H(101) CdS peak intensity and crystallite size as a function of CdS layer thickness.

It should be taken into account that the XRD fingerprints as shown in Figure 4.13 (a) were stacked together for better peak comparison. From observation, all the layers are polycrystalline in nature with peaks associated with hexagonal (100), (002), (101) and

(103) being observed at 2θ=24.9°, 26.7°, 28.4° and 48.0° respectively, due to the metastable nature of hexagonal CdS [153] after CdCl$_2$ treated [36].

From observation of the 50 nm thick CdS layer, it is clear that the peaks associated with H(101) are still at the emerging stage with no visible presence of peak associated with H(100) and H(103). With the increase in CdS thickness to 100 nm and above, peaks attributed to H(100) and H(103) planes were observed along with the H(101). An increase in reflection intensity with increasing thickness was noticeable. Based on this observation, it can be said that the increase in the reflection intensity is directly associated with increasing thickness of the CdS layer [36,159].

As shown in Figure 4.13 (b), the crystallite size was calculated using Scherrer's equation as shown in Equation 3.8. From observation, the H(101) preferred orientation reflection of the 50 nm thick CdS layer was indistinguishable by the Philips PW 3710 X'pert diffractometer for analysis due to its thinness or weak crystallinity. It should be noted that the electrodeposition of CdS commences with the deposition of sulphur before the deposition of cadmium is triggered [148]. Therefore, a sulphur rich CdS and weak CdS can be experienced at the initiation stages of nucleation of CdS. Furthermore, an increase in crystallite size was observed to be associated with the increasing the CdS layer thickness. A similar observation has also been documented in the literature by other independent researchers [36,159].

4.4.2 Optical properties based on CdS thickness

Figure 4.14 shows the graph of percentage transmittance versus wavelength for CdCl$_2$ treated glass/FTO/CdS layer. It was observed that the bandgap lies within 2.44±0.02 eV with the highest bandgap observed at 50 nm. This observation might be due to either the early nucleation stage in which the underlying glass/FTO substrate is not fully covered due to the mechanism of deposition in electroplating as discussed in Section 4.4.1 and the comparatively low crystallite size and crystallinity [160] as shown in Figure 4.13 (b) for the 50 nm thick CdS layer. Consequently, an increase in the steepness of the absorption edge and a shift of the absorption edge towards shorter wavelength were observed with increase in CdS thickness. This observation is well documented in the literature [159,161] with researchers such as Bosio, 2006 [30] and Han, 2011 [125] suggesting superior semiconductor material quality with steeper absorption edge due to lesser impurity energy levels and defects in the thin film.
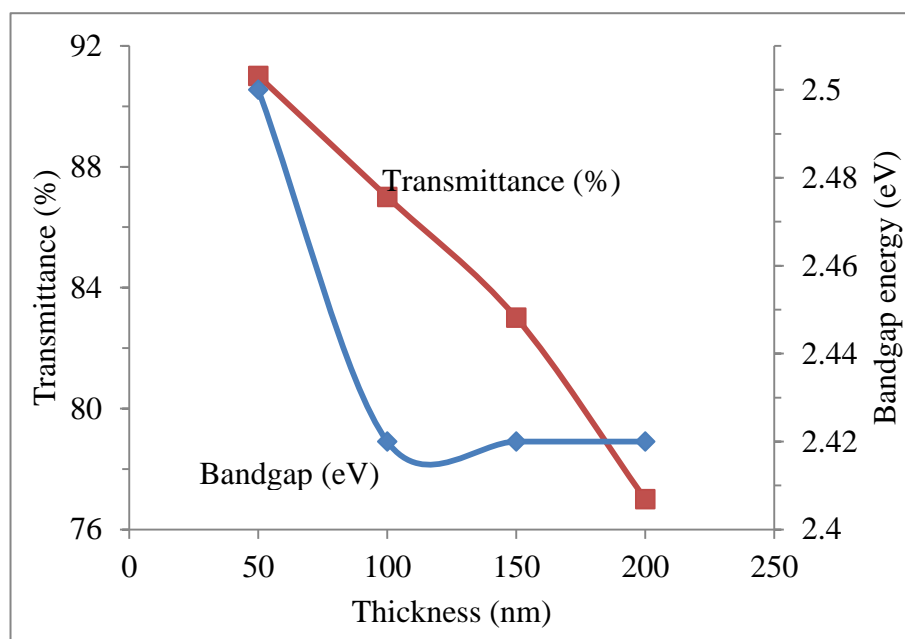
Figure 4.14: The effect of CdS film thickness on optical bandgap and transmittance spectra for CdCl$_2$ treated CdS thin-films at 400˚C for 20 minutes in air.

The reduction in bandgap observed with increase in thickness to 100 nm might be due to the full coverage of the underlying substrate. Consequently, reduction in transmittance from ~90% to ~75% was observed with increasing thickness from 50 nm to 200 nm as shown in Figure 4.14. It is important to note that thinner CdS layers give higher transmittance, hence higher photocurrent can be generated. On the other hand, thinner CdS layers have high tendency to suffer from discontinuities and defects such as pinholes [36,162] due to the nucleation mechanism of the deposition technique. Therefore it is pertinent that the optical property of the semiconductor layer and its thickness must be considered to achieve optimum photocurrent.

4.4.3   SEM studies based on CdS thickness

The SEM micrographs of 50, 100, 150 and 200 nm thicknesses of CdCl$_2$ treated CdS layers grown on glass/FTO are shown in Figure 4.15 (a-d) respectively. Although the as-deposited glass/FTO/CdS layers are not presented in this work due to its triviality, grain growth and the coalescence of grains is observed after CdCl$_2$ treatment. As observed in Figure 4.15 (a), full coverage of the underlying glass/FTO substrate has not been attained with the glass/FTO grains still visible beneath the CdS layer due to significant gaps between grains. This observation might be as a result of the early stage of nucleation of CdS to the underlying conducting substrate and also the columnar growth mechanism in electroplated semiconductors. With an increase in thickness to

100 nm and above as shown in Figure 4.15 (b-d), grains tend to be more closely packed with full coverage of the glass/FTO underlying substrate. It should be noted that the fabrication of a solar cell using the 50 nm pinhole infected CdS layer will lower the performance of the solar cell due to low open-circuit voltage, fill factor and short-circuit current density as a result of shunting.
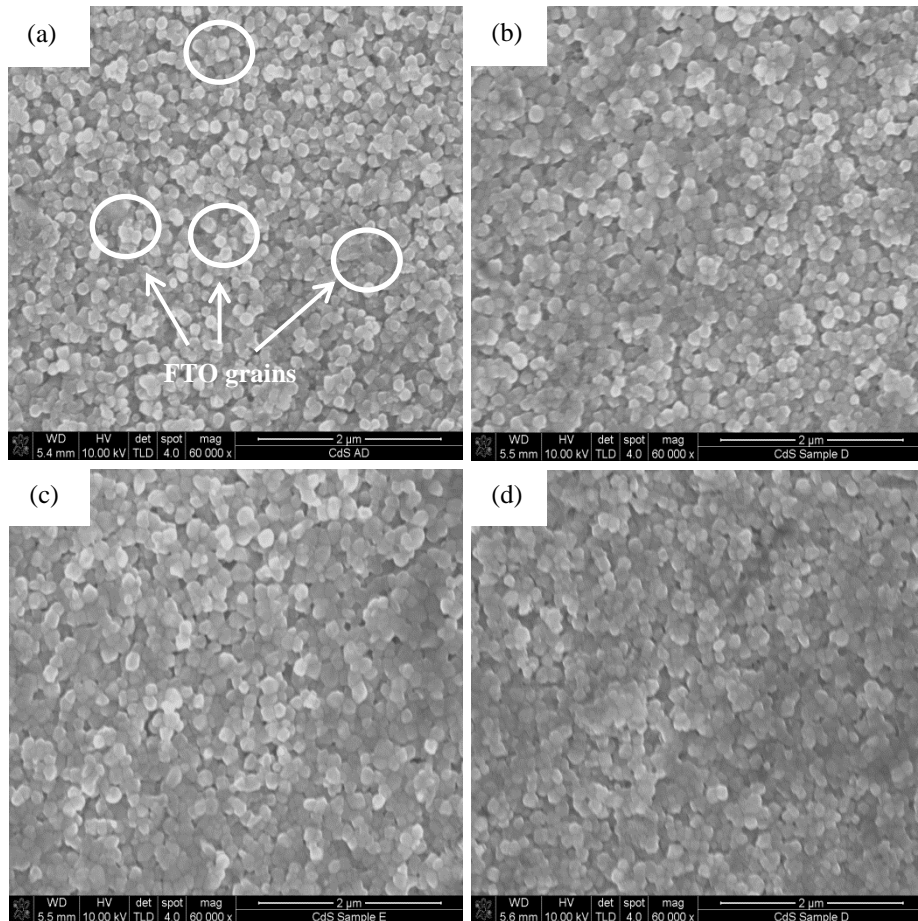
Figure 4.15: SEM micrograph images for as-deposited CdS with thicknesses of (a) 75 nm (b) 100 nm (c) 200 nm (d) 400 nm respectively.

4.5   Effect of CdS heat treatment temperature

For this set of experiments, ~500 nm thick CdS was electrodeposited at 791 mV on glass/FTO with a dimension $(4{\times}6)$ cm^2. After growth, the layer was cut into six pieces of $(4{\times}1)$ cm^2. One of the CdS layers was left as-deposited, while the others were CdCl$_2$ treated at different temperatures ranging from (380 to 450)°C for 20 minutes. The observed characteristic properties are discussed herein.

4.5.1 X-ray diffraction studies based on heat treatment temperature

Figure 4.16 (a) shows the XRD diffractions of CdS layers $CdCl_2$ treated at different heat treatment temperature but at constant time duration, while Figure 4.16 (b) shows the XRD results analysis based on both the H(101) and H(100) CdS diffraction peaks.
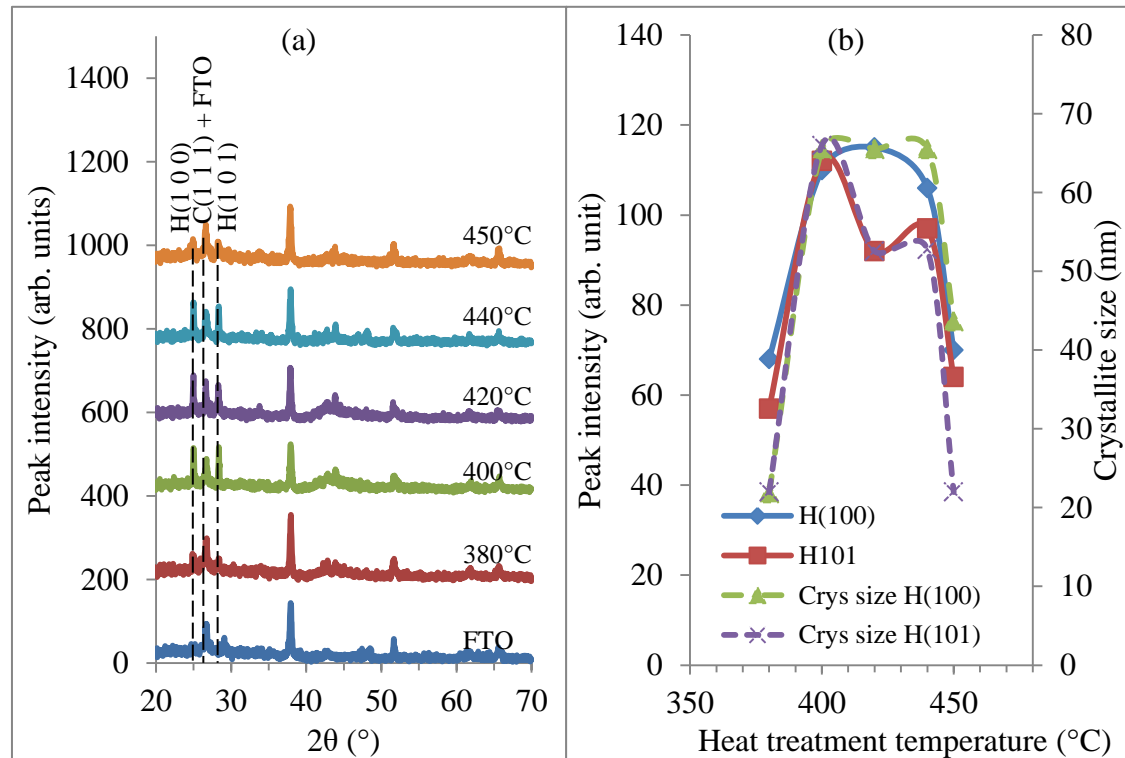
Figure 4.16: (a) Typical XRD patterns of CdS layers $CdCl_2$ treated for the same time duration at different heat treatment temperatures and (b) Analysis based on H(100) and H(101) CdS peaks as a function of CdS thickness.

As observed in Figure 4.16 (a), the preferred orientation for the $CdCl_2$ treated CdS layer between (380 and 400)°C for 20 minutes is H(101). But between (420 and 440)°C treatment temperature, recrystallisation, and competition of H(101) and H(100) phases were observed. Such observation has been documented in the literature on the effect of post-growth treatment temperature on recrystallisation of CdTe materials by Dharmadasa, 2014 [106].

Furthermore, no noticeable reduction in peak intensity was observed after 500°C treatment temperature, but reduction in crystallite sizes from ~(65 to 52) nm ensued. These observations attest to improvement in crystallinity after $CdCl_2$ treatment as documented in the literature with the optimal treatment temperature at 400°C due to reduced phase competition and observation of the highest crystallite size of ~65 nm calculated using both the H(101) and H(100) parameters as shown in Figure 4.16 (b).

Although other parameters need to be optimised, the effect of heat treatment temperature cannot be overlooked.

4.5.2   Optical properties based on heat treatment temperature

Figure 4.17 shows the effect of $CdCl_2$ treatment temperature on both optical absorption and transmittance of CdS layers. It is obvious from observation that an improvement in the bandgap is observed at (400 to 420)°C as compared to the layers treated below 380°C and above 420°C. The slightly high bandgap observed after 380°C $CdCl_2$ treatment of the CdS layers might be due to the incorporation of excess/unreacted elemental Cd and S resulting into comparatively low crystallinity as also observed in Figure 4.16. While the increase in the bandgap of CdS, $CdCl_2$ treated above 420°C might be due to the formation of large pinholes as shown in Figure 4.18 which allows the passage of photons at the explored wavelength and resulting into the high surge in transmittance as shown in Figure 4.17. At temperatures beyond 420°C, CdS layer thickness reduces due to sublimation of material and therefore both the measured transmittance and bandgap increases.
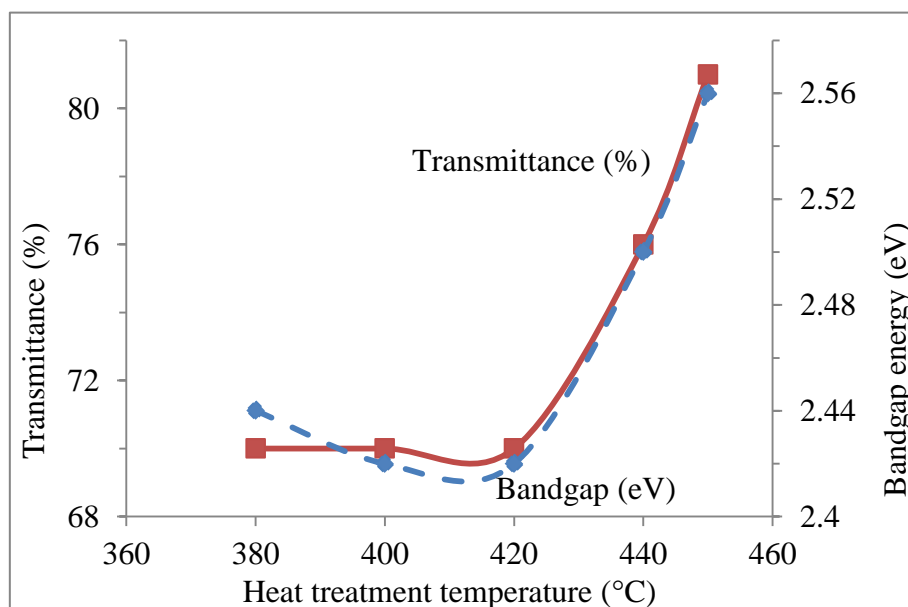
Figure 4.17: The effect of $CdCl_2$ treatment temperature on optical bandgap and transmittance of $CdCl_2$ treated CdS thin-films for a constant duration of 20 minutes in air.

4.5.3   SEM studies based on heat treatment temperature

Figure 4.18 shows the SEM micrographs of as-deposited and $CdCl_2$ treated CdS layers heat treated for 20 minutes in air at different temperatures. At constant $CdCl_2$ heat treatment duration for different temperatures, grain growth through the coalescence of

smaller grains was observed, with higher $CdCl_2$ treatment temperature correlating with an increase in grain size.
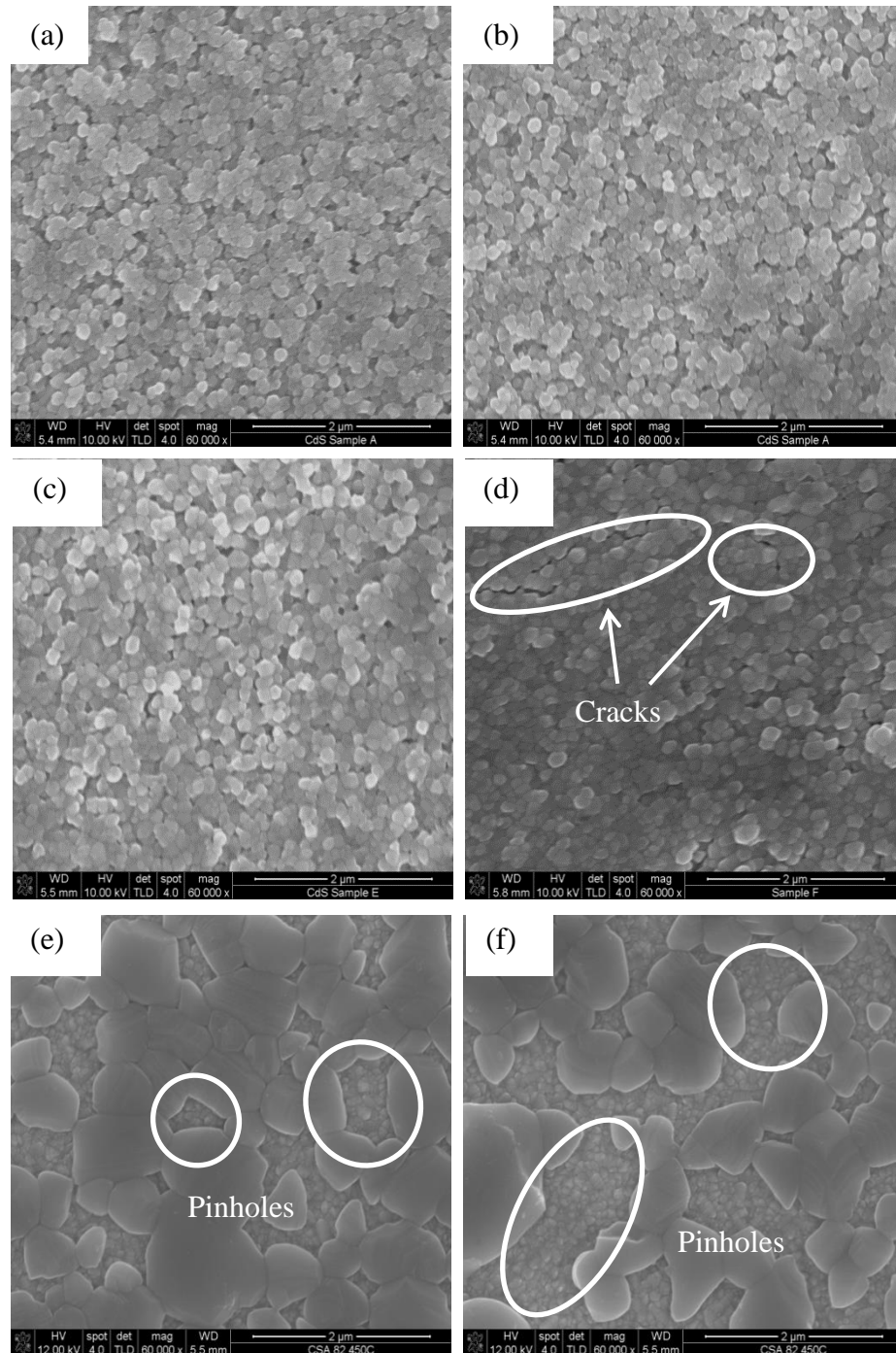
Figure 4.18: SEM micrograph images of (a) as-deposited and $CdCl_2$ treated CdS layers for 20 minutes in air at (b) 380°C (c) 400°C (d) 420°C (e) 440°C and (f) 450°C respectively.

The grain size for the as-deposited CdS was estimated to be between (120 and 200) nm. The $CdCl_2$ treated CdS at 380°C, 400°C, 420°C, 440°C and 450°C for 20 minutes were estimated to be within the ranges of (120 to 225) nm, (180 to 225) nm, (180 to 300) nm,

(300 to 2000) nm and (300 to 2000) nm respectively. At 420°C (see Figure 4.18 (d)) cracks were observed, while at 440°C and above, large pinholes were observed due to intensive coalescence of grains at such high temperatures. Furthermore, this observation might also be due to the mechanism of growth in electrodeposited semiconductor layers. It should be noted that nucleation of electrodeposited semiconductor material on glass/FTO underlying layer commences at the apex of the rough surface of the substrate due to the high electric field experienced at these tips. This mechanism of growth results in the column-like growth leaving pinholes within and around columns, they are gradually filled-up with an increase in layer thickness. Based on observation, layers heat-treated at 400°C seems better due to higher grain size as compared to the as-deposited CdS layers and $CdCl_2$ treated at 380°C without cracks and pinholes as observed at 420°C and above

4.6   Effect of heat treatment duration

These sets of experiments were performed on ~500 nm thick CdS layers which were $CdCl_2$ treated at 400˚C in the air for different time durations.

4.6.1   X-ray diffraction study based on heat treatment duration

Figure 4.19 (a) shows the XRD diffraction patterns of CdS $CdCl_2$ treated at 400°C for varied heat treatment durations ranging between (10 to 50) minutes, while Figure 4.19 (b) shows the graph of the preferred orientation CdS (H(101)) intensity and the calculated crystallite sizes against $CdCl_2$ heat treatment durations. As shown in Figure 4.19 (a), the preferred orientation of all the CdS layer explored were H(101). Based on observation, improvement in the H(101) CdS peak intensity was observed after $CdCl_2$ treatment at 400°C between (10 to 50) minutes due to the improvement in both electronic and material properties of the CdS layers as discussed earlier in Section 4.3.2 and also recorded in the literature [30,157].

As shown in Figure 4.19 (b), a gradual increase in the H(101) diffraction intensity was observed from the as-deposited layer and peaking at 20 minutes $CdCl_2$ treatment duration. Above this duration, a gradual reduction in the diffraction intensities was observed, which might be due to CdS layer deterioration through sublimation and increased pinhole density as observed morphologically (see Section 4.6.3). For the CdS layers $CdCl_2$ treated for 50 minutes, a complete collapse of both the H(101) and H(100) diffraction associated with CdS was observed which might be due to high material loss

due to sublimation as a result of prolonged heat treatment duration. Furthermore, no improvement in crystallite sizes was observed between the as-deposited CdS layer and the CdCl$_2$ treated layers for the duration of (10 – 30) minutes as depicted in Figure 4.19 (b). This observation might either be due to the limitation of Scherrer's equation for measuring large crystallites [115] or due to the sensitivity of the XRD equipment utilised in this work. These observations reiterate the importance of CdCl$_2$ treatment duration on crystallinity and crystallite size.
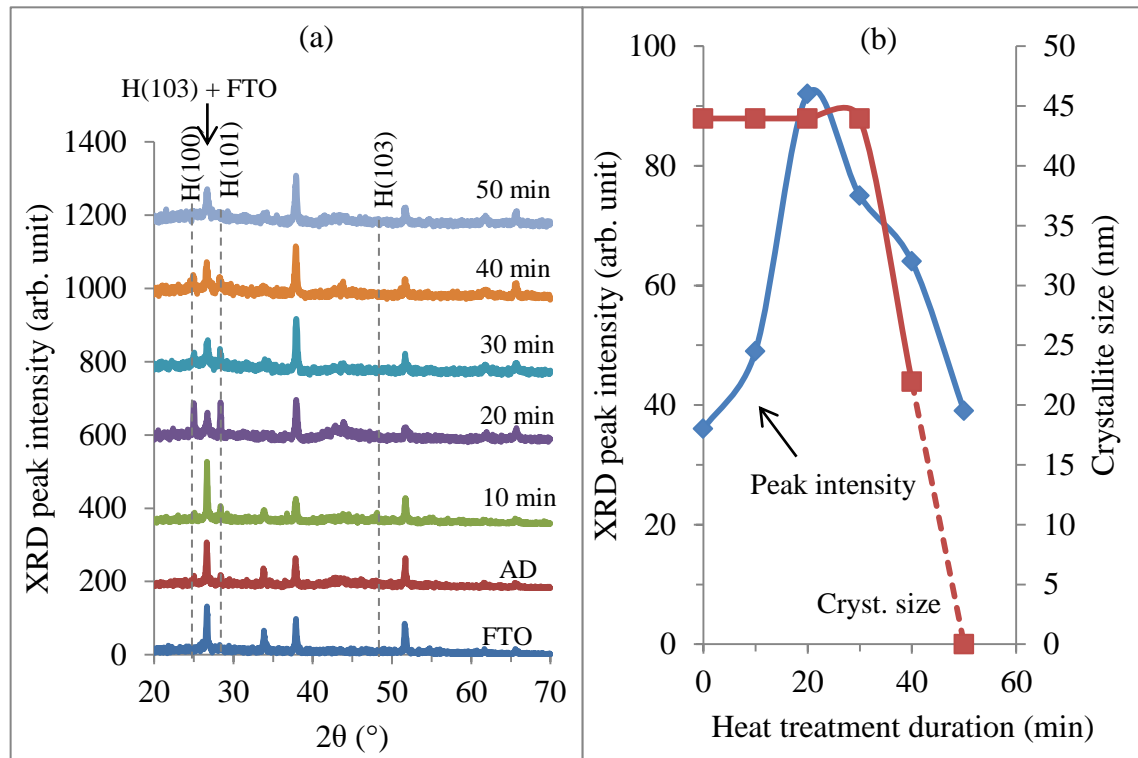
Figure 4.19: (a) Typical XRD patterns of CdS layers CdCl$_2$ treated at 400°C for different time durations and (b) Graph of the preferred orientation of CdS (H(101)) intensity and the calculated crystallite sizes against CdCl$_2$ heat treatment duration.

4.6.2   Optical properties based on heat treatment duration

Figure 4.20 shows the effect of heat treatment duration on both the bandgap and transmittance of CdS thin film CdCl$_2$ treated at 400°C in air. As shown in Figure 4.20, a gradual increase in transmittance was observed with increasing CdCl$_2$ treatment duration. It should be noted that the change in transmittance between 15 minutes and 25 minutes treatment duration is comparatively minimal with a transmittance difference of ~65%±2% as compared to others. Correspondingly, a similar trend was observed with bandgap energy of the CdS layers as shown in Figure 4.20. The initial increase in both transmittance and bandgap energy between (0 and 10) minutes can be attributed to the

improvement in CdS properties either by sublimation of excess elements (Cd and S), increase in CdS crystallinity and grain growth. While the CdS layers $CdCl_2$ treated between (15 and 25) minutes can be said to be highly crystalline CdS layer with full coverage of underlying FTO substrate. Evidence of these can be seen in the bandgap which equals the bulk CdS bandgap of 2.42 eV. These properties are required to produce high-efficiency solar cell devices. The increase in both the transmittance and bandgap energy observed for CdS layers $CdCl_2$ treated for durations above 25 minutes can be attributed to the severe loss of CdS layers and the formation of pin-holes. This observation is in accord with the thickness measurement discussed in Section 4.3.4.
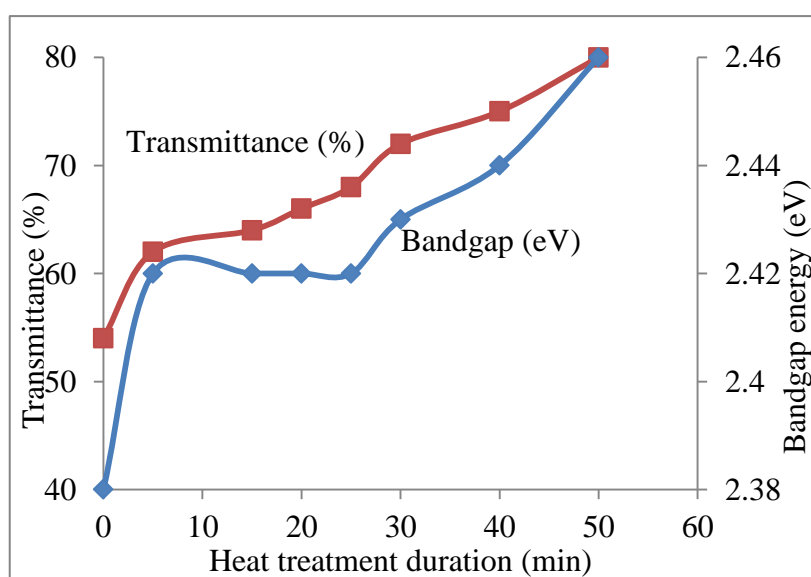
Figure 4.20: The effect of heat treatment duration on CdS thin-film grown at 791 mV and heat treated at different durations at 400˚C in the presence of $CdCl_2$.

4.6.3   SEM studies based on heat treatment duration

Figure 4.21 shows the SEM micrograph images of (a) as-deposited and $CdCl_2$ treated CdS at 400˚C for the durations of (b) 10, (c) 20, (d) 30, (g) 40 and (h) 50 minutes respectively. Topologically, the surface of the FTO/CdS substrate shows full coverage with CdS nanoparticles for the as-deposited and heated samples for 10, 20 and 30-minute duration. It was notable that the coalescence of grains and increase in grain sizes was slightly observable after 10 minutes heat treatment duration, with grain sizes within the range of (150 to 200) nm. A further increase in grain size to~ (300 to 550) nm was observed with an increase in the heat treatment duration. This microstructural change of the surface morphology as a result of heat treatment can be attributed to re-

crystallisation and the partial transformation of the mixed cubic/hexagonal phases into single hexagonal phase after heat treatment [163] as observed from XRD.
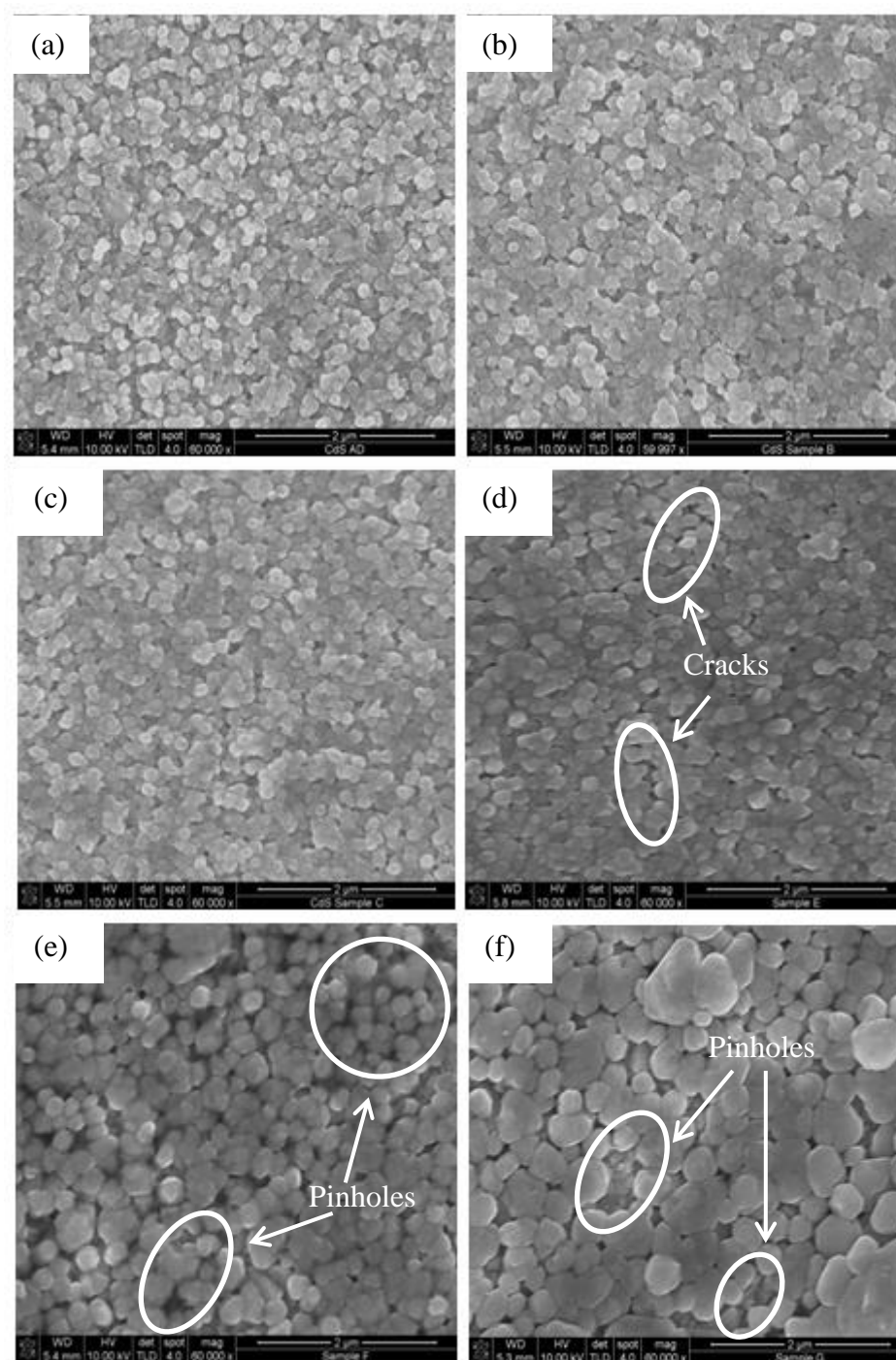
Figure 4.21: SEM micrograph images of (a) as-deposited and CdCl$_2$ treated CdS at 400˚C for the duration of (b) 10 (c) 20 (d) 30 (e) 40 and (f) 50 minutes respectively.

Gaps along the grain boundaries were observed for samples heat treated for 30 minutes and above. This can be attributed to the sublimation of the CdS layer and due to a build-up of larger CdS nanoparticles from the coalescence/growth of CdS crystallites [164] in

the vertical direction. These observations are in accord with the thickness measurement in Figure 4.7 (b).

4.7   Testing the electronic quality of CdS

4.7.1   Current-voltage characteristics with Ohmic contacts (DC conductivity)

The DC conductivity measurements were carried out on the electrodeposited CdS layers to determine the electrical conductivity (σ) and resistivity (ρ) of the layers. This experiment was performed to determine both the effect of film thickness and the heat treatment duration on the electrical properties of CdS layers. 2 mm diameter and 60 nm thick indium (In) contacts were evaporated onto CdS layers to give Ohmic behaviour. The electrical resistance (R) of the glass/FTO/CdS/In structure was calculated from the Ohmic I-V data under dark condition using Rera Solution PV simulation system. Using Equation 3.18, which incorporates resistance R, contact area A and film thickness L, the resistivity (ρ) was calculated.

The summary of the electrical resistivity and conductivity as a function of CdS layer thickness is tabulated in Table 4.5. To determine the effect of heat treatment duration on the electrical properties, 310 nm thick CdS was deposited on a (3×8) cm^2 FTO substrate and treated with CdCl$_2$ after growth. The substrate was cut into (3×1) cm^2 pieces before heat treating each substrate at 400°C for different time durations. As observed in Figure 4.22 (a), an initial stagnation of the resistivity of the CdS layer was observed for 5 and 10 minutes heat treatment duration which suggests that the latent heat required in melting grain boundaries, activate grain growth and forming crystalline mono-phased CdS have not been surpassed due to the gradual temperature increase of the substrate during their treatment time durations. The increase in the conductivity of CdS for samples heat treated for 20 minutes can be attributed to growth in grain size, reduction of grain boundaries and increased crystallinity of the CdS layer. While the samples heat treated above, 20 minutes duration shows a gradual decrease in conductivity which might be due to the deterioration of the CdS layer caused by sublimation of elements [148]. This reduction of electrical conductivity could also be due to compensation taking place by diffusion of *p*-dopant such as Na from glass substrate during prolonged heat treatment. This observation is in accordance with the structural, morphological, and optical properties discussed above. This shows that the optimum heat treatment at 400˚C is for ~20 minutes to achieve the highest electrical conductivity.

Table 4.5: Summary of electrical properties of CdS layers after heat treatment durations at 400˚C in the presence of $CdCl_2$ in air.

Heat treatment duration at 400°C (min)	Measured Thickness (nm)	Avg. Resistance (Ω)	Avg. Resistivity $\times 10^4$ (Ω.cm)	Avg. Conductivity $\times 10^{-5}$ (Ω.cm)$^{-1}$
5	302	28.4	2.97	3.39
10	300	28.3	2.97	3.39
20	285	20.2	2.23	4.51
25	246	22.8	2.91	3.48
30	174	24.8	4.47	2.32
40	126	20.6	5.13	2.09
50	96	20.4	6.67	1.57
60	69	20.8	9.46	1.09
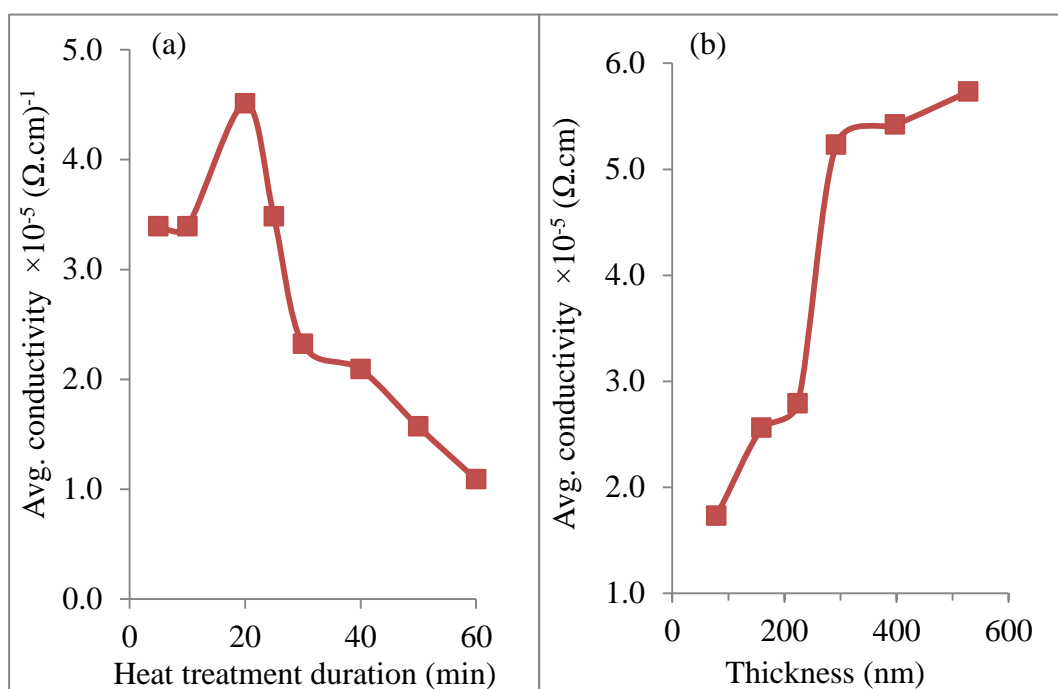
Figure 4.22: (a) The effect of heat treatment duration on the electrical conductivity of CdS thin films grown at 791 mV and heat treated at different durations at 400˚C in the presence of $CdCl_2$. (b) The effect of CdS film thickness on electrical conductivity for $CdCl_2$ treated CdS thin-films at 400˚C for 20 minutes in air.

Table 4.6: The effect of layer thickness on the electrical conductivity of CdCl$_2$ treated CdS layers.

Thickness (nm)	Resistance (Ω)	Avg. Resistivity $\times 10^4$ (Ω.cm)	Avg. Conductivity x 10^{-5} $(\Omega$.cm$)^{-1}$
79	15.4	6.11	1.73
159	15.4	3.94	2.56
223	25.5	3.58	2.79
292	18.7	2.01	5.23
397	23.5	1.86	5.42
528	30.0	1.79	5.73

Further experimentation on the effect of thickness on the electrical conductivity of CdS layers which had been post-growth treated with CdCl$_2$ at 400°C for 20 minutes shows that an increase in film thickness results into an increase in the conductivity as shown in Table 4.6 and Figure 4.22 (b). This can be attributed to the formation of large grains, reduction of voids/pin-holes, increase in S vacancy and Cd interstitials which serves as an *n*-type intrinsic dopant of CdS [158].

4.7.2   Current-voltage characteristics with rectifying contacts

The current-voltage (I–V) characteristics for rectifying contacts have been broadly used to study Schottky diodes and to determine some important device and material parameters. For these experiments, the thicknesses of CdS films were varied to determine the effect of thickness on the characteristic behaviour of glass/FTO/CdS/Au Schottky diodes. The I-V characteristics were measured in dark condition at a bias voltage range of (-1.00 to 1.00) V. The I-V characteristics of a Schottky diode under dark condition has been previously expressed in Section 3.5.1.1.

Figure 4.23 (a) shows a typical semi-logarithmic current vs. voltage curve measured under dark condition for Au Schottky contacts made on heat treated CdS, Figure 4.23 (b) linear-linear I-V curve of Au Schottky contacts made on heat treated CdS layers and Figure 4.23 (c) The effect of heat treatment duration at 400°C on ideality factor and potential barrier height for Au Schottky contacts under dark condition. The series resistance R_s and shunt resistance R_{sh} were calculated from the slopes of the linear-linear I-V curve in the forward and reverse bias respectively as shown in Table 4.7. It was observed that across all thicknesses in this experiment, the cells show infinite (∞) R_{sh} and $R_s \leq 0.1$ Ω which is close to that of an ideal diode with R_{sh} and R_s equal infinity (∞) and zero (0) respectively. The observed ideality factor was in the range of (1.63 to 1.83)

with a gradual increase in value with an increase in thickness as shown in Table 4.7. This shows that the current transport mechanisms in the depletion region of the M/S structure consist of both thermionic emission and recombination and generation (R&G) processes. Other factors such as the increase in R_s and tunneling through the diode could have increased the ideality factor n [16], but in this experiment, the R_s was 0.1 Ω. Further observations on the effect of thickness on CdS layer shows that thickness has no significant influence on the barrier height ϕ_b. The fabricated CdS diodes show an RF value of ~10^4 across all thicknesses. This indicates that the CdS layers are suitable for application in electronic devices.
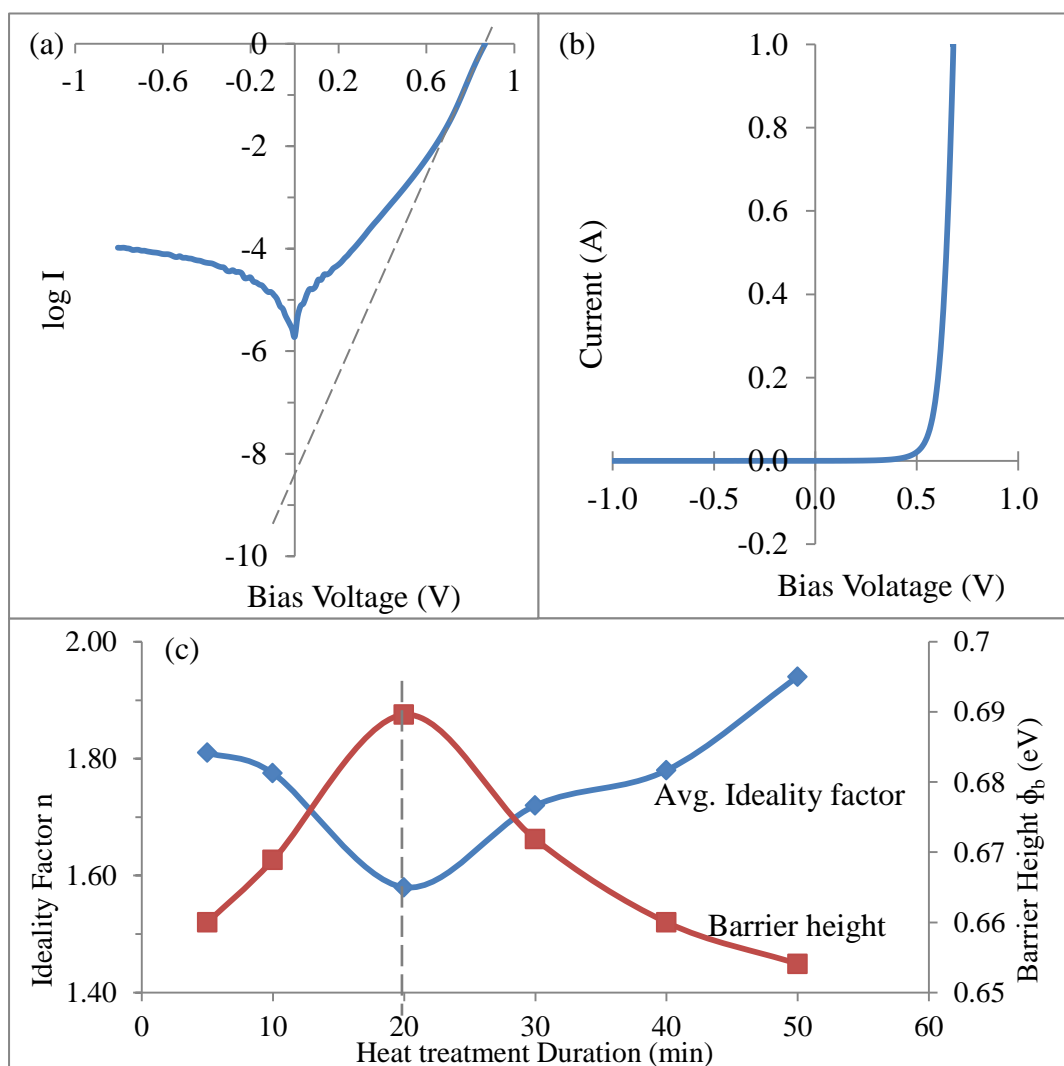
Figure 4.23: (a) A typical semi-logarithmic current vs. voltage curve measured under dark condition for Au Schottky contacts made on heat treated CdS (b) linear-linear I-V curve of Au Schottky contacts made on heat treated CdS layers and (c) The effect of heat treatment duration at 400˚C on ideality factor and potential barrier height for Au Schottky contacts on CdS under dark condition.

Table 4.7: The summary of observed parameters obtained from current-voltage (I-V) characteristics for CdS/Au Schottky diodes at different thicknesses.

Thickness (nm)	R_s (Ω)	R_{sh} (MΩ)	log RF	$I_o \times 10^{-7}$ (A)	n	Φ_b (eV)
79.0	0.089	0.96	4.2	3.46	1.68 -1.72	> 0.67
159.6	0.075	1.10	4.2	3.04	1.70 - 1.72	> 0.67
223.7	0.075	1.13	4.1	4.02	1.70 - 1.75	> 0.67
292.4	0.075	1.18	4.0	4.66	1.72 - 1.78	> 0.66
397.5	0.084	1.25	4.2	4.71	1.76 - 1.82	> 0.66
528.0	0.094	1.27	4.1	5.17	1.80 - 1.83	> 0.66

Additional experimentations on the effect of heat treatment duration on CdS layers as depicted in Figure 4.23 (c) shows an optimal value for both ϕ_b and n at 20 minutes heat treatment duration. This observation can be attributed to better material quality, high crystallinity, and minimisation of defect distribution. Material deterioration was observed at higher heat treatment duration as the n value tends towards 2.00, which show the presence of higher R&G centers.

4.7.3 Capacitance-voltage characteristics of rectifying contacts

The capacitance-voltage (C-V) technique was performed to determine important device and material characteristics such as position of Fermi level (E_F), built-in potential (V_{bi}), doping concentration of the material (N_D-N_A), barrier height Φ_b, charge carrier mobility $(\mu_\perp)$ and depletion layer width at zero bias of glass/FTO/CdS/Au Schottky diodes fabricated on varied CdS layer thickness. The justification for the use of combined I-V and C-V measurements for the estimation of the material's electronic parameters instead of Hall Effect measurement have been discussed in Section 3.5.

All the samples used in this experiment were CdCl$_2$ treated at 400°C for 20 minutes. The C-V measurements were performed in dark condition at a bias voltage range of (-1.00 to 1.00) V with 1 MHz AC signal at 300 K. The built-in potential (V_{bi}) and donor concentration (N_D-N_A) in this configuration can be determined using the Mott-Schottky plot as shown in Figure 4.24 using Equation 3.50 and Equation 3.52.
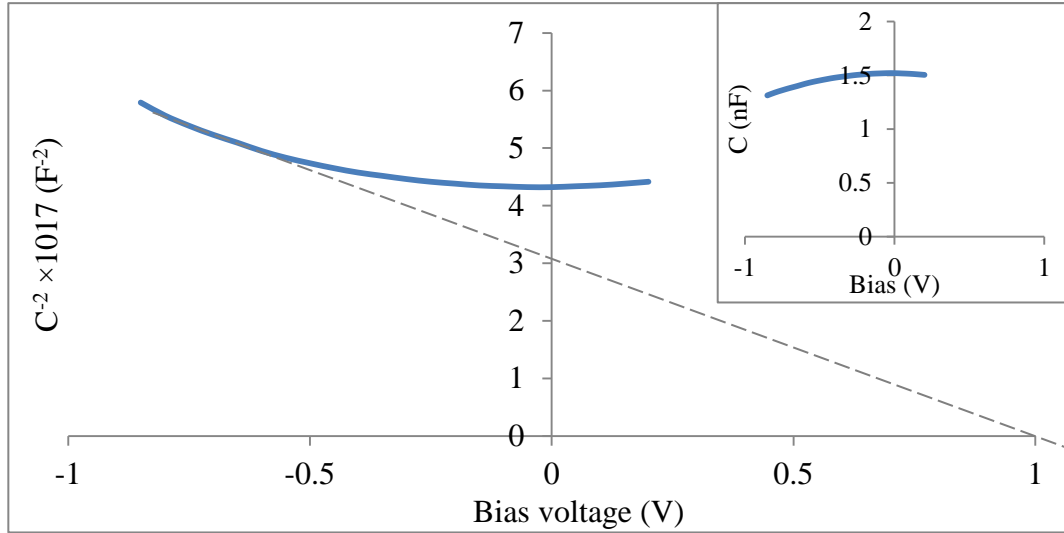
Figure 4.24: A typical Mott-Schottky plot for Schottky contacts made on electroplated CdS layers. Inset shows the variation of capacitance as a function of DC bias voltage.

For the experiments discussed in this thesis, It has been assumed that all excess donor atoms (N_D) are ionised at room temperature, therefore $n \approx (N_D - N_A)$ as shown in Equation 3.57. The $\mu_\perp$ is the mobility of electrons in the direction perpendicular to FTO surface. It should be noted that $\mu_\perp$ is different from the reported mobility values measured by conventional Hall Effect method. These values are $\mu_{//}$, and it represents the mobility of electrons moving parallel to the FTO layer. Due to the presence of grain boundaries, $\mu_{//}$ will be much smaller than $\mu_\perp$ for nano-crystalline CdS layers.

Further to this, cognisance should be taken of the calculated Φ_b values using C–V measurements (see Equation 3.58) as it is affected by the effects of defects and interfacial resistive layers producing excess capacitance and inhomogeneity of the semiconductor layer in the diode [146]. The calculated Φ_b was mainly to show the trend in this work. As observed from Table 4.8 and Figure 4.25 (a), the increase in average conductivity with respect to the increasing thickness of CdS layer can be attributed to the resultant effects on n and $\mu_\perp$ for electrons. The gradual increase in n values indicates that R&G centers increase with increase in thickness.

Table 4.8: The summary of observed parameters obtained from Mott-Schottky plots for CdS/Au Schottky diodes at different thicknesses.

Thickness (nm)	Range of Ideality factor n	$\sigma \times 10^{-5}$ $(\Omega cm)^{-1}$	Avg. $(N_D\text{-}N_A)$ $\times 10^{17} (cm^{-3})$	$(E_C\text{-}E_F)$ (eV)	Φ_b (eV)	$\mu_\perp \times 10^{-4}$ $(cm^2 V^{-1} s^{-1})$
79.0	1.68 -1.72	1.73	9.03	0.11	> 0.84	1.19
159.6	1.70 - 1.72	2.56	8.13	0.12	> 0.86	1.96
223.7	1.70 - 1.75	2.79	7.22	0.14	> 0.89	2.41
292.4	1.72 - 1.78	5.23	4.92	0.15	> 0.89	6.63
397.5	1.76 - 1.82	5.42	1.30	0.17	> 0.91	26.00
528.0	1.80 - 1.83	5.73	1.22	0.19	> 0.92	29.26

The mobility of charge carriers (free electrons) depends on scattering due to lattice vibration, ionised and neutral impurities, native defects and grain boundaries. Table 4.8 summarises the variation of parameters such as n, σ, $N_D\text{-}N_A$ and $\mu_\perp$ for CdS layers with increasing thickness. The diode behaviour observed in Figure 4.24 is typical for moderately doped semiconductors with the doping range of $(10^{15} – 10^{17})$ cm^{-3} [146]. Although, there are possibilities of obtaining varying doping concentrations under different growth conditions [146], in the case of this experimental work all growth parameters were kept constant.
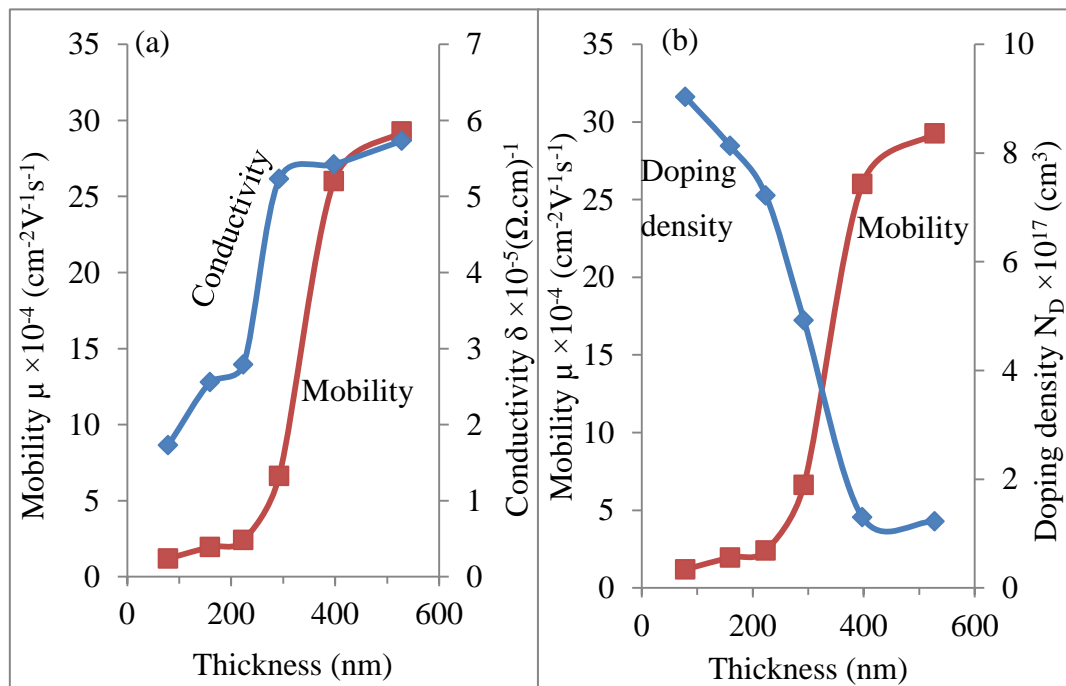
Figure 4.25: Graph of mobility and conductivity as a function of CdS layer thickness, (b) graph of mobility and doping density as a function of CdS layer thickness.

Additional experimentation was performed to determine the effect of heat treatment duration on 205 nm thick as-deposited CdS layer. The layers were subjected to post-deposition heat treatment at 400˚C at different heat treatment durations, after which glass/FTO/CdS/Au rectifying contacts were fabricated. As shown in Table 4.9 and Figure 4.26, low carrier mobility was observed for samples heat treated for a duration less than 10 minutes. This can be attributed to low CdS crystallinity and resulting high density of grain boundaries and defects as described in Section 4.7.2. The mobility reduction for heat treatment duration above 20 minutes can also be attributed to material deterioration and increase in defects. The heat treatment at 400˚C for 20 minutes in the air appears to be the optimum condition for post-deposition treatment. Under these conditions, doping concentration of $\sim 9.0 \times 10^{17}$ cm^{-3}, lowest n $\sim$1.65, the highest barrier height of 1.01 eV and the highest mobility $\mu_\perp$ $\sim$20.7 cm^{-2}V^{-1}s^{-1} were achieved for these devices on CdS films.

Table 4.9: The summary of observed parameters obtained from Mott-Schottky plots for CdS/Au Schottky diodes heat treated at 400˚C for different time duration.

HT duration (min)	$\sigma \times 10^{-5}$ (Ω.cm)$^{-1}$	n	$(N_D\text{-}N_A)$ $\times 10^{18}$ (cm^{-3})	E_F (eV)	Φ_b (eV)	$\mu \times 10^{-5}$ (cm^{2}V^{-1}s^{-1})
5	2.28	1.80 -1.82	5.53	0.15	> 0.88	2.57
10	2.24	1.76 - 1.79	1.71	0.18	> 0.91	8.18
20	2.99	*1.62 – 1.67*	*0.90*	0.20	> 1.01	20.70
30	2.11	1.70 – 1.75	5.53	0.15	> 0.88	2.38
40	1.79	1.75 – 1.81	9.03	0.14	> 0.82	1.24
50	1.31	1.90 – 1.97	16.25	0.12	> 0.75	0.50

To achieve better quality CdS layers required for highly efficient PV solar cell development, the doping density $(N_D\text{-}N_A)$, electrical conductivity (σ) and charge carrier mobility ($\mu_\perp$) should be optimised with significant consideration of layer thickness, heat treatment temperature, and duration. Other factors to consider such as the reduction of defects due to inherent impurities and production of larger grains to reduce native defects and scattering will further improve the properties of the layers. The observation of minimum ideality factor (n) at 20 minutes heat treatment duration shows the presence of minimum R&G centers under the treatment conditions.
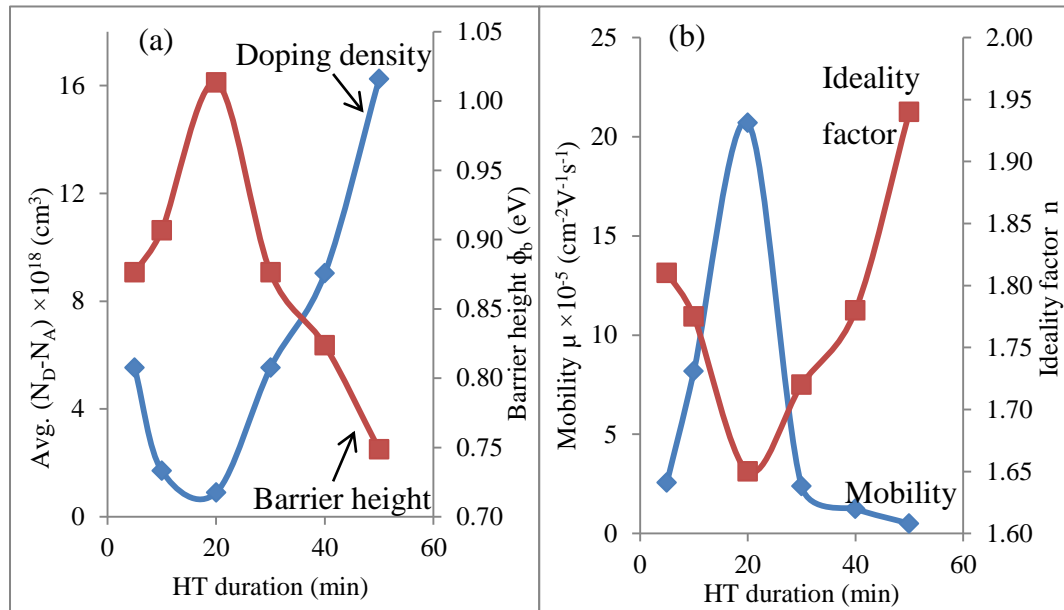
Figure 4.26: (a) Graphs of barrier height and doping density as a function of heat treatment duration and (b) graphs of mobility and ideality factor as a function of heat treatment duration.

Comparison of results on electrodeposited ED-CdS layers presented in this work with previously reported Schottky barrier work on thin films of CdS grown by chemical bath deposition (CBD) and bulk CdS crystals grown by melt-grown techniques show excellent prospects for development of ED-CdS layers. Table 4.10 summarises the main parameters available for comparison. Schottky barriers formed on all the layers exhibit similar parameters for RF and potential barrier height. Low n values for diodes made on bulk crystal show the presence of less R&G centers as expected. However, the diode properties observed for poly-crystalline CdS show that the layers have good electronic quality for fabricating excellent PV devices. Although the ideality factor n of both ED-CdS and CBD-CdS indicates that the charge carrier transportation mechanism is governed by both thermionic and R&G, it was interesting to observe that comparatively high rectification factor and low series resistance in the ED-CdS layer. The lower barrier height in electrodeposited CdS might be due to Fermi level pinning at the defect states or due to the presence of impurities.

Table 4.10: The summary of electrical property comparison between ED-CdS, CBD-CdS and bulk CdS crystal.

CdS material used	ρ (Ωcm)	RF	n	ϕ_b (eV)	R_s (Ω)	R_{sh} (Ω)	N_D-N_A (cm^{-3})	μ($cm^2V^{-1}s^{-1}$)
ED-CdS	2.2×10^4	10^4	1.65	1.01	0.1	10^6	10^{17}	2.1×10^{-4}
CBD-CdS [146]	10^5	$10^{3.3}$	1.50	1.02	20	-	10^{17}	10^{-3}
Bulk- CdS [272,273]	10^2	10^4	(1.08-1.30)	1.04(SXPS) 0.8 (I-V)	-	-	10^{16}	-

4.8   Conclusions

The work presented in this chapter demonstrates the electrodeposition of CdS using 2-electrode configuration from an electrolytic aqueous bath containing cadmium chloride hydrate ($CdCl_2 \cdot xH_2O$) and thiourea (NH_2CSNH_2) as cadmium and sulphur precursors respectively. Based on the material characterisation techniques explored, 791 mV was identified as the best cathodic potential in which stoichiometric ED-CdS is achieved. XRD results show that both cubic and hexagonal CdS were present in the as-deposited CdS layer, while, only the hexagonal CdS was retained after heat treatment at 400˚C for 20 minutes in the air in the presence of $CdCl_2$ with a preferred orientation along the (002) plane. Both the XRD and SEM results in this work indicate grain growth after $CdCl_2$ treatment and the formation of large clusters of CdS consisting of small crystallites size ranging from ~(23–47) nm as-deposited and ~(33–66) nm after $CdCl_2$ treatment and a cluster size ranging from 300 nm to 1µm. The optical absorption results showed a bandgap range of (2.40–2.42) eV after $CdCl_2$ treatment.

The effects of heat treatment temperature and heat treatment duration were also explored using thickness measurement, SEM, optical absorbance, and transmittance. Further analysis of the electronic properties of ED-CdS using both I-V and C-V measurements were also explored. Excellent rectifying diodes with rectification factor exceeding ~10^4 were formed with FTO/CdS/Au structures. The observed ideality factor ranges between 1.50–2.00 and a barrier height above 1.01 V were achieved. The C-V and Mott-Schottky plot of the effect of CdS layer thickness shows an increasing

conductivity and hence mobility with an increase in layer thickness. An inverse relationship between doping density and mobility was also observed. Comparisons of Schottky device parameters show that ED-CdS layers have good electronic quality when compared to CBD-CdS layers and bulk CdS crystal. The lowest ideality factor was observed after heat treatment at 400°C for 20 minutes which indicates the lowest R&G centers under the condition.

Chapter 5 -   CdTe deposition and characterisation

5.1   Introduction

Semiconductor materials from the II-VI group have been highly recognized for their importance in providing a range of materials with high optoelectronic conversion efficiency and also because they possess direct energy band gaps covering the significant portion of the solar spectrum. Cadmium telluride (CdTe) which belongs to the II-VI family is assumed to be one of the most prominent of the group, and its properties have been extensively investigated [104,165]. CdTe has found a wide range of applications as infrared windows, X- and ɣ-ray detectors and most especially PV solar cells due to its high absorption coefficient of about 10^4 cm^{-1} at 300 K in the visible and near IR region of the solar spectrum. As documented in the literature, CdTe with a near ideal direct band gap of 1.45 eV [95] possesses the ability to absorb 99% of incident photons with energy higher than the CdTe bandgap at 2 μm thickness [97,166]. The search for cheaper technologies for mass production and high optoelectronic conversion efficiency of photovoltaic solar cells has prompted the use of different thin film growth techniques in the deposition of CdTe. With over fourteen various growth techniques reported in the literature [165], low-cost, simplicity, scalability and manufacturability have been some of the attributes of the electrodeposition technique over others [16]. The literature reveals that $CdSO_4$ has been the main precursor in the electrodeposition of CdTe [167], but other precursors such as $Cd(NO_3)_2$ [168–170], $CdCl_2$ [152,171] amongst others are yet to be fully explored. Therefore, this report presents the comprehensive details of the growth and characterization of CdTe deposited using 2-electrode electroplating technique from an aqueous solution containing cadmium nitrate.

Furthermore, the effect of extrinsic doping and doping concentration of CdTe with halides (F, Cl and I) from group VII and Ga from group III of the periodic table were explored due to their unique properties and their suitability for use in electronic devices.

5.2   Electrolytic bath and substrate preparation for CdTe

5.2.1   Electrolytic bath preparation

CdTe thin films were cathodically electrodeposited on glass/FTO substrates by the potentiostatic technique. Cadmium nitrate tetrahydrate $Cd(NO_3)_2 \cdot 4H_2O$ of 99.997% purity, was used as the cadmium precursor while tellurium oxide (TeO_2) of 5N

(99.999%) purity was used as the tellurium source. The aqueous electrolyte was prepared with 1.5 M $Cd(NO_3)_2 \cdot 4H_2O$ in 800 ml deionised (DI) water contained in a 1000 ml polypropylene beaker. The polypropylene beaker was placed in an 1800 ml glass beaker containing DI water. The glass beaker serves as the outer bath and helps to maintain uniform heating of the electrolyte. The $Cd(NO_3)_2 \cdot 4H_2O$ solution was electro-purified for ~50 hours to reduce the impurity level. Afterwards, 0.0002 M of TeO_2 was added and stirred for 5 hours to achieve homogeneity of the mixed solution prior to electroplating.

It is worth mentioning that, due to the solubility issues of TeO_2 in aqueous solutions (but it is partially soluble in some acidic medium [172]), 0.03 M of TeO_2 solution was prepared by dissolving it in 30 ml of concentrated nitric acid (HNO_3), and stirred for about 1 hour. Afterwards, the acidic TeO_2 solution was diluted with 400 ml of DI water in a plastic conical flask. An initial 5 ml of the TeO_2 solution was added to the electro-purified aqueous $Cd(NO_3)_2 \cdot 4H_2O$ electrolyte to give a total concentration of 0.0002 M TeO_2. The electrolytic bath containing 1.5 M $Cd(NO_3)_2 \cdot 4H_2O$ plus 0.0002 M TeO_2 in 800 ml of DI water will be referred to as CdTe bath henceforth. Before electrodeposition, the CdTe bath temperature, pH, and stirring rate were maintained at ~85˚C, 2.00±0.02 and ~300 rpm respectively. The pH was adjusted using diluted solutions of HNO_3 and NH_4OH. The CdTe bath setup mimics the 2E configuration as described in Section 3.3. The working electrode (or cathode) utilised is glass/FTO with a sheet resistance of 7 $\Omega/\square$. Prior to the deposition of the CdTe layer, the cyclic voltammogram of the resulting CdTe bath was recorded to determine the possible deposition potential range of CdTe.

5.2.2 Substrate preparation

Substrates were ultrasonically cleaned at the initial stage in soap solution for 20 minutes and rinsed in deionised (DI) water. The substrates were then cleaned thoroughly with methanol and acetone to remove any grease and rinsed in DI water. Finally, the FTO was submerged in a clean beaker of DI water and transferred directly into the electroplating bath. Before characterisation, electrodeposited CdTe layers were rinsed, dried and divided into two halves. One half was left as-deposited, and the other half was cut into several samples and heat treated in the presence of $CdCl_2$ at 400˚C in the air for different time durations to enhance its properties. The $CdCl_2$ treatment was performed by adding few drops of aqueous solution containing 0.1 M $CdCl_2$ in 20 ml of DI water

to the surface of the semiconductor layer. The full coverage of the layers with the treatment solutions was achieved by spreading the solution using solution-damped cotton bud. The semiconductor layer was allowed to air-dry and heat treated at 400°C for 20 minutes.

5.3   Growth and voltage optimisation of CdTe

Asides the glass/FTO substrate utilised for cyclic voltammetry, the CdTe layers were electrodeposited between the deposition voltages of 1355 mV and 1385 mV for 3 hours. The glass/FTO/CdTe layers were cut into two. Half was left as-deposited while the other half was $CdCl_2$ treated as discussed in Section 5.2.2. Both the as-deposited and $CdCl_2$ treated CdTe layers were characterised afterward for both their material and electronic properties.

5.3.1   Cyclic voltammetric study

Figure 5.1 shows the cyclic voltammogram of an aqueous solution of a mixture of 1.5 M $Cd(NO_3)_2.4H_2O$, and 0.0002 M TeO_2 solution in 800 ml of DI water during the forward and reverse cycles between -100 and ~1500 mV cathodic voltage. The scanning rate was fixed at 3 mVs^{-1} and the pH was adjusted to 2.00±0.02. The bath temperature and the stirring speed were kept constant at ~85°C and 300 rpm respectively. In the electrodeposition of CdTe, tellurium deposits first, followed by cadmium due to its more positive standard reduction potential (E_o) value of +593 mV as compared to the -403 mV for tellurium [173] with respect to standard H_2 electrode. Ascribable to the high difference between the E_o potential of $HTeO_2^+$ and Cd^{2+}, the concentration of Cd^{2+} is kept much higher than $HTeO_2^+$ in the electrolytic bath [174,175]. It is observed from Figure 5.1 that Te starts to deposit in the forward cycle at a cathodic potential of ~130 mV (see in Figure 5.1) under the experimental conditions used according to the electrochemical reaction as shown in Equation 5.1.

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \qquad \text{Equation 5.1}$$
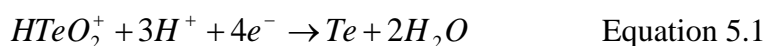
As the cathodic potential increases, more Te is deposited, and Cd starts to deposit at ~800 mV. The hump observed at ~800 mV (see inset in Figure 5.1) depicts the deposition of Cd on the cathode and the co-deposition of CdTe. The rate of deposition of Cd increases with an increase in the cathodic potential. Thus, the electrochemical

reaction of Cd deposition and the co-deposition of CdTe are shown in Equation 5.2 and Equation 5.3 respectively.

$$Cd^{2+} + 2e^{-} \rightarrow Cd$$ Equation 5.2
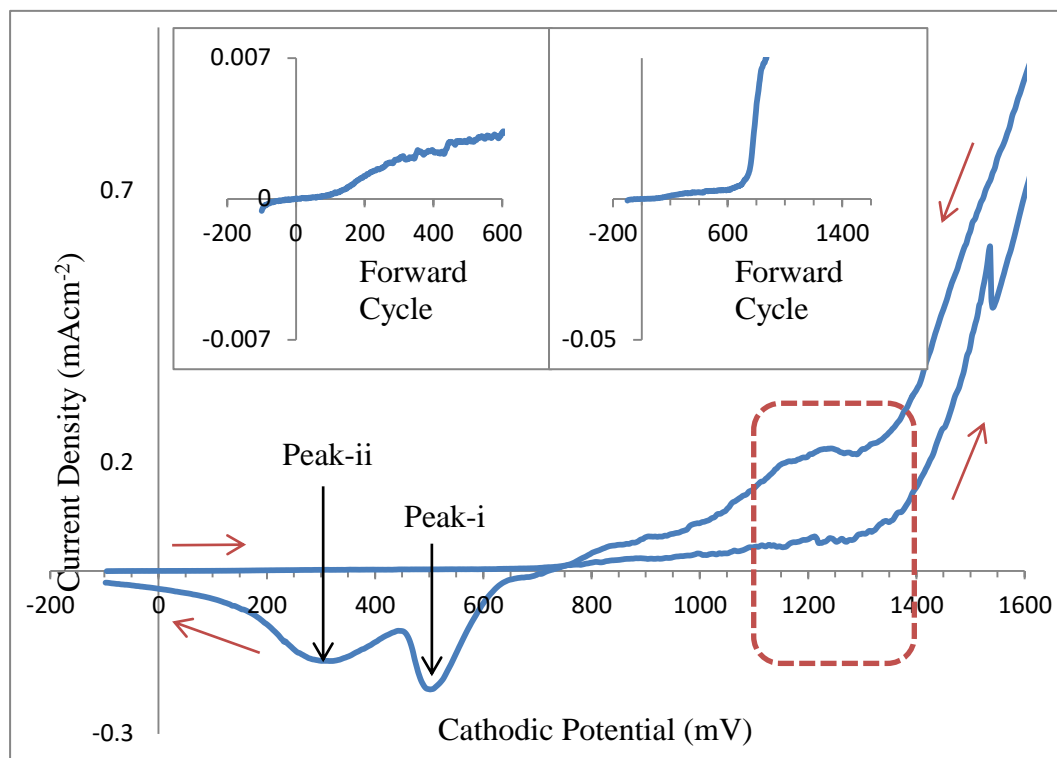
Figure 5.1: A typical cyclic voltammogram for deposition electrolyte containing the mixture of 1.5 M $Cd(NO_3)_2 \cdot 4H_2O$ and 0.0002 M TeO_2 solutions at ~85˚C and pH= 2.00±0.02. The inset is the expanded forward cycle. The insets are the expanded sections of the forward cycle for both Te and Cd deposition initiation.

In the forward cycle, it was observed that between the cathodic potential range of (1100 and 1420) mV, the deposition current density appears to be stable within the range of 150 μAcm^{-2} and 180 μAcm^{-2}. This range (i.e., 1220 mV to 1400 mV) had been pre-characterized at cathodic potential steps of 50 mV using XRD analysis (results are not presented in this report). The highest XRD peak intensity was observed at 1370 mV. Therefore, the surrounding cathodic potential was scanned at steps of 5 mV to identify the best growth potential.

$$HTeO_2^{+} + Cd^{2+} + 3H^{+} + 6e^{-} \rightarrow CdTe + 2H_2O$$ Equation 5.3
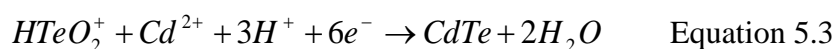
In the reverse cycle, peak-i at ~500 mV represents the dissolution of elemental Cd and Cd from CdTe, while broad peak-ii represents the dissolution of Te at ~309 mV. It is

highly imperative that the electrodeposition of CdTe should be done close to the stoichiometric point. Therefore, the cathodic voltage between (1355 and 1385) mV was characterized to determine the optimal growth voltage (V_g) for their material and electronic properties.

5.3.2 X-ray diffraction study

Figure 5.2 (a) and Figure 5.2 (b) shows the X-ray diffraction patterns for CdTe layers grown between 1355 mV and 1385 mV for both as-deposited and $CdCl_2$ treated layers respectively. Under all the growth voltages and treatment explored, X-ray diffractions associated with Cd_xTeO_y, the underlying FTO and predominant (111) cubic CdTe were observed at $2\theta = \sim21.64$, $23.90°$ and $37.62°$ respectively.
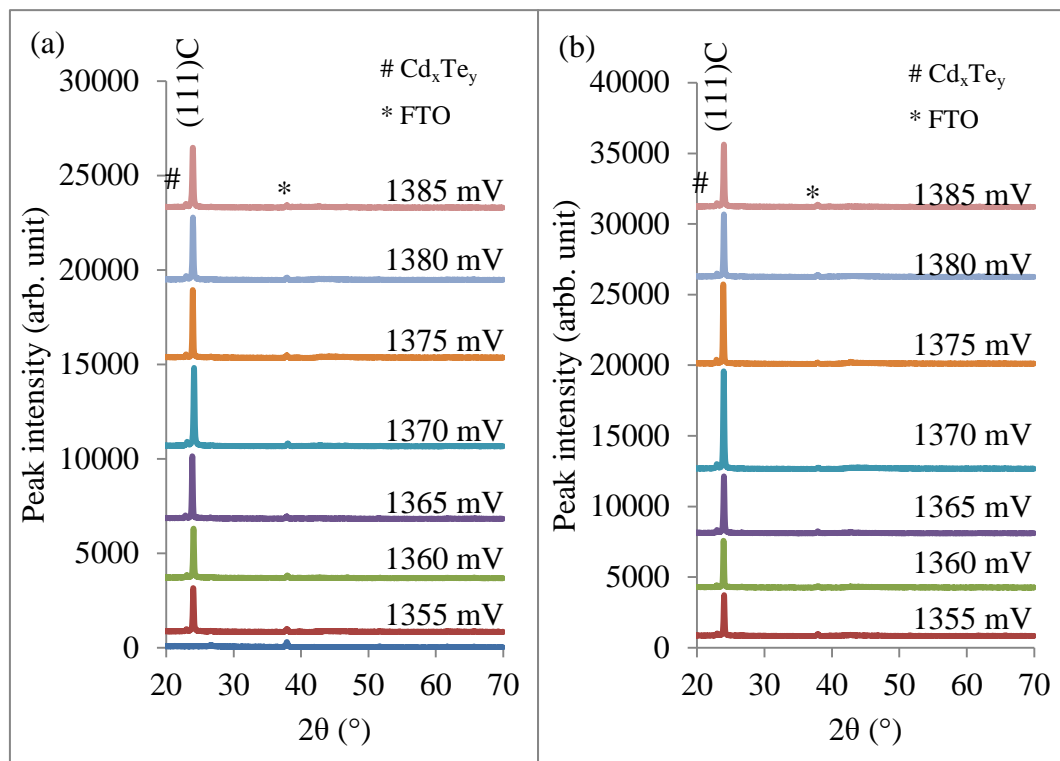
Figure 5.2: Typical XRD patterns of CdTe layers grown between (1355–1385) mV deposition potentials for (a) As-deposited CdTe layers and (b) $CdCl_2$ treated CdTe layers at 400˚C for 20 minutes.

The incorporated Cd_xTeO_y diffraction might be due to the oxidation of the CdTe top layer, while the FTO might either be due to the thickness of the deposited CdTe layers and the presence of pinholes due to columnar growth mechanism of CdTe layer [170,176]. It should be noted that the diffractions associated with elemental Te or Cd

were not observable due to CdTe growth voltage range within the vicinity of the stoichiometric CdTe.

For both the as-deposited and $CdCl_2$ treated CdTe layers as shown in Figure 5.2 and Figure 5.3, an increase in the diffraction intensity of the (111) cubic CdTe were observed between 1355 mV and 1370 mV, while the reduction in the intensity was observed at growth voltages above 1370 mV. This observation signifies that the highest crystallinity and stoichiometric CdTe was attained at 1370 mV, while CdTe layers grown at lower or higher growth voltage suffer from the richness of either Te or Cd respectively. Furthermore, improvement in the diffraction intensity was observable after $CdCl_2$ treatment of all the CdTe layers grown at different voltages as shown in Figure 5.3. This observation which is well documented in the literature can be attributed to grain growth and re-crystallisation of the crystal structure.
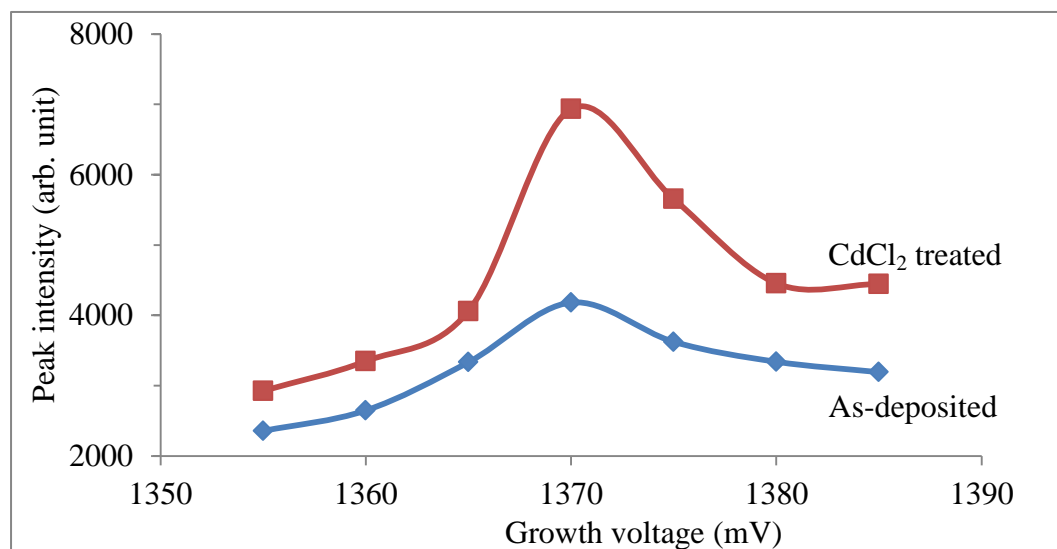
Figure 5.3: Comparative analysis of CdTe (111)C peak for as-deposited and $CdCl_2$ treated CdTe layers grown at different growth voltages between 1355 and 1385 mV.

The analysis of the (111) cubic CdTe diffraction for both the as-deposited and $CdCl_2$ treated CdTe layers grown between 1355 mV, and 1385 mV is shown in Table 5.1. From observation, the highest crystallite size of ~65.3 nm was observed between 1370 mV and 1375 mV for as-deposited CdTe layers and between 1365 mV and 1375 mV for $CdCl_2$ treated CdTe layers. Outside these ranges, lower crystallite sizes were observed, due to the richness of elemental Te or Cd in the CdTe. The extracted XRD data from these CdTe report matches the Joint Committee on Powder Diffraction Standards

(JCPDS) reference file No. 01-775-2086. The crystallite size, D was calculated using the Scherrer's formula (see Equation 3.8):

Table 5.1 The XRD analysis of as-deposited and the $CdCl_2$ treated CdTe layers grown between the growth voltage of 1355 mV and 1385 mV.

As-deposited

Growth voltage (mV)	2θ (°)	Lattice Spacing (Å)	FWHM (°)	Crystallite Size D (nm)	Assignments
1355	24.01	3.70	0.195	43.5	(111) cubic
1360	24.04	3.70	0.195	43.5	
1365	23.87	3.71	0.162	52.2	
1370	24.12	3.71	0.130	65.3	
1375	23.97	3.71	0.130	65.3	
1380	23.96	3.71	0.162	52.2	
1385	23.94	3.71	0.162	52.2	

$CdCl_2$ treated

Growth voltage (mV)	2θ (°)	Lattice Spacing (Å)	FWHM (°)	Crystallite Size D (nm)	Assignments
1355	24.01	3.70	0.162	52.2	(111) cubic
1360	23.95	3.71	0.162	52.2	
1365	23.99	3.71	0.130	65.3	
1370	24.12	3.71	0.130	65.3	
1375	23.97	3.71	0.130	65.3	
1380	23.98	3.71	0.162	52.2	
1385	23.98	3.71	0.162	52.2	

5.3.3   Raman study

Raman spectroscopy studies were performed on samples to determine the phonon modes, identify the phases and to determine the crystallinity of both the as-deposited and the $CdCl_2$ treated samples. The excitation source used was a 514 nm argon ion laser. Figure 5.4 shows typical Raman spectra for both as-deposited and the $CdCl_2$ treated CdTe layers grown at 1370 mV. The Raman peak at 165 cm^{-1} corresponds to the longitudinal optical (LO) phonon mode of CdTe, while the peak at 140 cm^{-1} corresponds to the E1 mode of hexagonal Te [177] and fundamental transverse optical (1TO) phonon mode of CdTe. After $CdCl_2$ treatment, the peak intensity observed at 140 cm^{-1} was reduced and the intensity of the CdTe observed at 165 cm^{-1} was increased due to the formation of CdTe from excess Te and Cd from $CdCl_2$ treatment. Frausto-Reyes, 2006 [178] described the increase in the Raman peak intensity as an increase in surface roughness which might be due to grain growth during $CdCl_2$ treatment, it should be

noted that due to the combination of both E(Te) and TO(CdTe) at 140 cm^{-1}, the change in intensity cannot be taken as a guide to observe any stoichiometric changes in the layers [44]. Furthermore, the slight Raman shift observed at 164 cm^{-1} can also be attributed to increase in crystallinity [179] after CdCl$_2$ treatment.
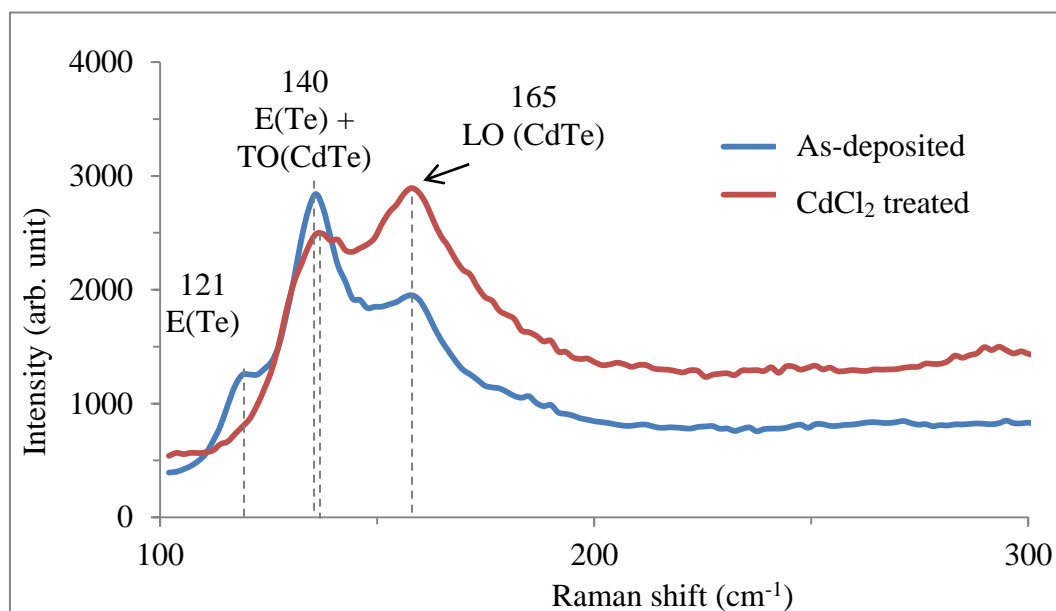
Figure 5.4: Raman spectra of as-deposited and CdCl$_2$ treated CdTe thin films grown at 1370 mV.

While Te diffraction(s) might not be clearly observed in the XRD peak patterns as discussed in Section 5.3.2 due to possible overlapping with FTO peak, a reduction in the E(Te) at 121 cm^{-1} was observable after CdCl$_2$ treatment (see Figure 5.4). This observation confirms improved crystallinity and stoichiometry after CdCl$_2$ treatment. It should be noted that the presence of Te might be due to the precipitation of Te in CdTe which is peculiar to CdTe grown under any technique [44,180,181]. This observation corroborates the summations made on the improvement of crystallinity after CdCl$_2$ treatment in Section 5.3.2 [44].

5.3.4   Thickness measurements

Both theoretically and experimentally, the thickness of electrodeposited CdTe layers were calculated and measured respectively, the results are shown in Figure 5.5. The theoretical thickness measurement using Faraday's law of electrolysis serves as the upper limit of thickness due to the assumption that all the electronic charges contribute to the deposition of CdTe without any consideration of the involvement of electronic

charges in the electrolysis of water at a voltage above 1230 mV [156]. The mathematical representation of the Faraday's law of electrolysis is shown in Equation 3.6, with predefined parameters. The number of electrons transferred (n) in the deposition of 1 molecule of CdTe is 6 ($n = 6$ for CdTe).
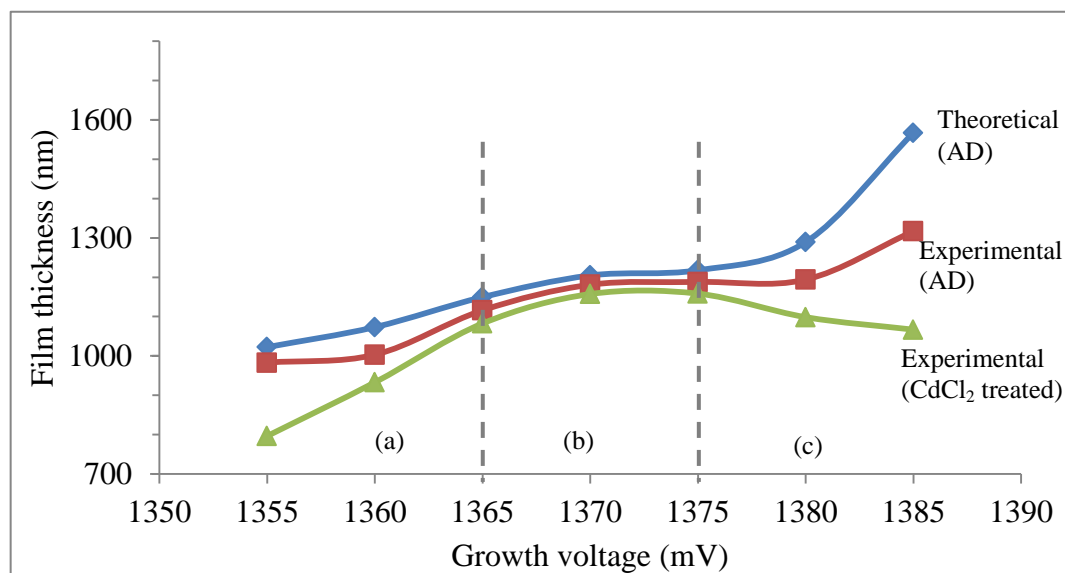
Figure 5.5: Graph of thickness against growth voltage for layers grown between 1355 and 1385 for the duration of 3 hours.

From the summations made from the cyclic voltammetric study in Section 5.3.1, it was observed that an increase in deposition voltage results into increase in the deposition current density. The increase in deposition current density can be related to the electrodeposited semiconductor layer thickness (Equation 3.6). Based on this relationship, increase in the thickness of the deposited CdTe layers grown at a different cathodic voltage for the same time duration as shown in Figure 5.5 can be explained. With the primary emphasis on the experimentally measured thicknesses, it was observed that after CdCl$_2$ treatment, a slight reduction of thicknesses in the CdTe layers measured between 1355 mV to 1360 mV and 1380 and 1385 were observed, while a considerable retention of thicknesses was observed for CdTe layers grown between 1365 mV and 1375 mV. These observations might be due to the sublimation of excess elements in the CdTe layers grown outside the growth voltage range in which possible stoichiometric or near stoichiometric CdTe can be deposited. It should be noted that the melting point of stoichiometric CdTe is ~1092°C, but the incorporation of excess elements (Cd, Te, O, and Cl) serves as impurities which affect the material and

electronic properties of the deposited CdTe layers such as the melting temperature. This observation, although not conclusive iterates the range in which stoichiometric or near stoichiometric CdTe can be grown.

5.3.5   Optical property analyses

The optical properties of the CdTe thin films were studied at room temperature using Carry 50 Scan UV-Vis spectrophotometer in the wavelength range of (200 to 1000) nm at room temperature. The measurements were carried out to study the optical absorbance characteristics of CdTe layers grown between the ranges of 1355 mV to 1385 mV under both as-deposited and $CdCl_2$ treatments. It should be noted that only the optical absorbance curves of cathodic voltages between 1360 mV and 1380 mV are shown in Figure 5.6 (a) and Figure 5.6 (b) for better visibility. The value of the obtained band gaps of the CdTe layers is shown in Table 5.2.
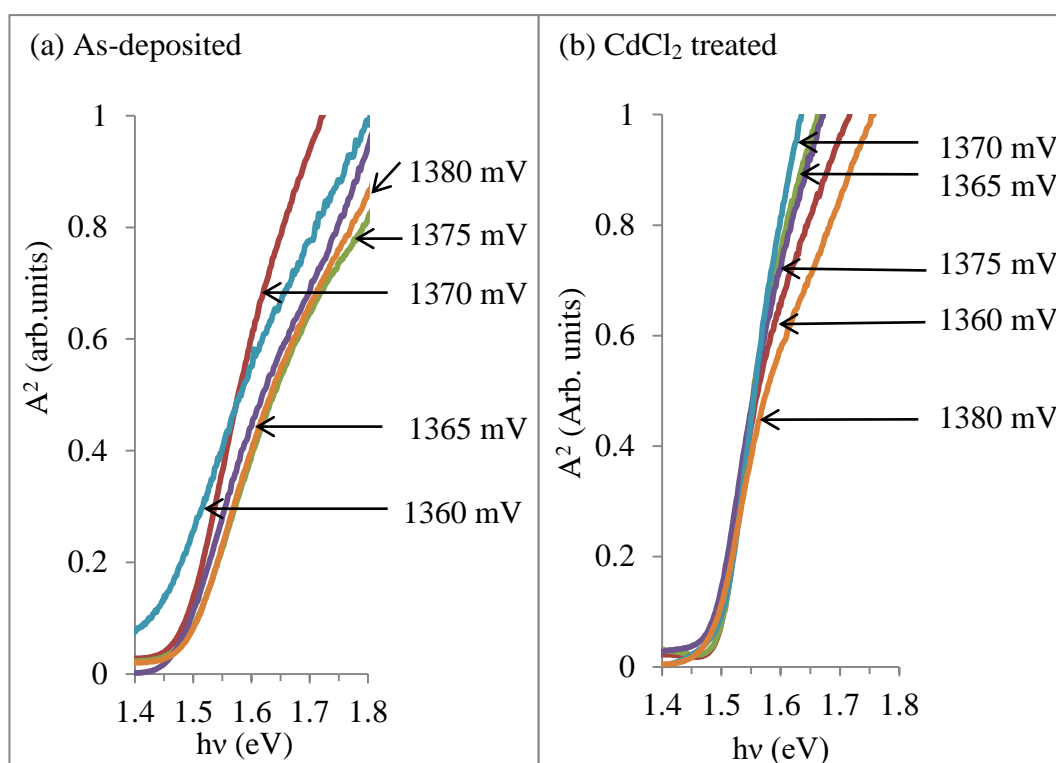
Figure 5.6: Optical absorption spectra for (a) as-deposited, and (b) $CdCl_2$ treated CdTe thin-films grown between 1360 mV to 1380 mV.

For the as-deposited CdTe layers as shown in Figure 5.6 (a) and Table 5.2, the range of the band gap observed spans between 1.42 eV for the lowest growth voltage explored (1355 mV) and 1.50 eV for the highest growth voltage explored (1385 mV). The

observation of low bandgap (1.42 eV) might be due to the incorporation of excess Te with a bandgap of 0.34 eV [182]. A narrower band gap range between 1.48 eV and 1.50 eV was observed for the explored CdTe layers after $CdCl_2$ treatment. This can be attributed to the improvement in the CdTe layers' optical property through the coalescence of smaller grains and grain growth [30,157], the formation of CdTe from unreacted elements [44], reduction in Te precipitation [44,180,183,184], and change in atomic composition [146] amongst other reasons. Further observations based on Figure 5.6 (a) and Figure 5.6 (b) show that the highest gradient of the optical absorption edge occurs at 1370 mV, which indicates the superiority of material quality due to lesser impurity energy levels and defects in the thin film [28,30].

Table 5.2: The optical bandgaps of both as-deposited and $CdCl_2$ treated CdTe layers grown between 1355 mV and 1385 mV.

Growth voltage (mV)	As-deposited (eV)	$CdCl_2$ treated (eV)
1355	1.42	1.49
1360	1.43	1.49
1365	1.48	1.49
1370	1.48	1.48
1375	1.48	1.48
1380	1.48	1.48
1385	1.50	1.50

5.3.6   Morphological studies

Figure 5.7 (a), Figure 5.7 (b) and Figure 5.7 (c) show the SEM images of as-grown CdTe layers grown at 1355 mV, 1370 mV and 1385 mV respectively, while Figure 5.7 (d), Figure 5.7 (e) and Figure 5.7 (f) are the SEM images after $CdCl_2$ treatment respectively. As shown in Figure 5.7, all the CdTe layers explored under both as-deposited and $CdCl_2$ treated conditions show full coverage of the underlying substrate. For the as-deposited CdTe layers, the presence of small grains, their agglomeration into curly floral-like grains and high grain boundary density were observed. The cluster sizes vary between ~50 nm and ~200 nm for CdTe layers grown at 1355 mV, ~200 nm and ~400 nm for CdTe layers grown at 1370 mV and ~50 nm and ~400 nm for CdTe layers grown at 1385 mV. It can be seen that the intrinsic doping of CdTe with either excess Te or Cd do affect the morphological property of the as-deposited CdTe layers. It should be noted that the incorporation of such high grain boundary density in CdTe

layer in the photovoltaic application will promote scattering of charge carriers at the grain boundaries [28,185] and reduction in charge carrier mobility [186].

After $CdCl_2$ treatment (Figure 5.7 (d), Figure 5.7 (e) and Figure 5.7 (f)), grain growth, reduction in grain boundary density and full coverage of underlying substrate were observed. Varying grain sizes between ~50 nm and ~500 nm were observed for CdTe layers grown at 1355mV, ~200 nm and ~2000 nm for CdTe layers grown at 1370 mV and ~200 nm and ~1500 nm for CdTe layers grown at 1385 mV.
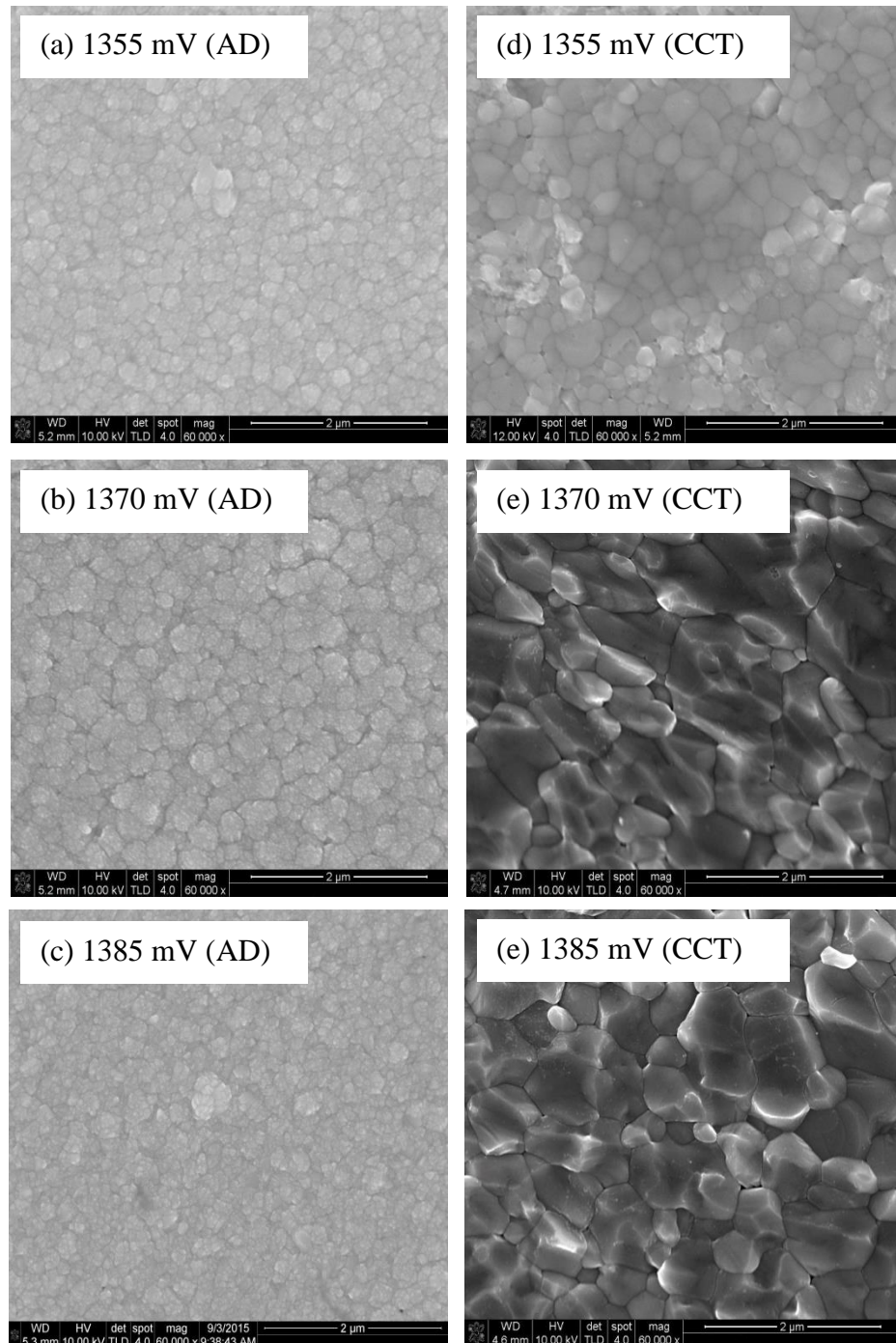
Figure 5.7: SEM micrograph of as-deposited (AD) and $CdCl_2$ treated (CCT) CdTe layers grown between 1355 mV and 1385 mV.

As documented in the literature, the incorporation of $CdCl_2$ during CdTe heat treatment facilitates grain growth, and recrystallization of the CdTe layer [30,157] coupled with the passivation of grain boundaries, improvement of the Cd/Te atomic stoichiometry and reduction of Te precipitates in CdTe [44]. Furthermore, the $CdCl_2$ treatment of CdTe in an oxygen-containing atmosphere is required to passivate the grain boundaries further and increase carrier concentration [187]. In accordance with the literature, increase in grain sizes was observable at all the explored V_g, with the largest grain size observed from CdTe grown at 1370 mV. This observation further depicts superiority of CdTe layers grown at 1370 mV morphologically.

5.3.7   Compositional analysis

For better visibility and comparability, Figure 5.8 shows the graph of the atomic ratio of Cd/Te for all CdTe layers grown between 1355 mV and 1385 mV under both as-deposited and $CdCl_2$ condition. Figure 5.9 (a), Figure 5.9 (b) and Figure 5.9 (c) show the EDX spectra of the as-deposited CdTe layers grown at 1355 mV, 1370 mV and 1385 mV respectively, while Figure 5.9 (d), Figure 5.9 (e) and Figure 5.9 (f) are the respective EDX spectra after $CdCl_2$ treatment. The unidentified EDX peaks in Figure 5.9 at (3.5 and 4.5) keV are for Cd and Te respectively [188]. As shown in Figure 5.8, CdTe layers grown at voltages lower and higher than 1370 mV shows richness in Te and Cd respectively under both as-deposited and $CdCl_2$ conditions.
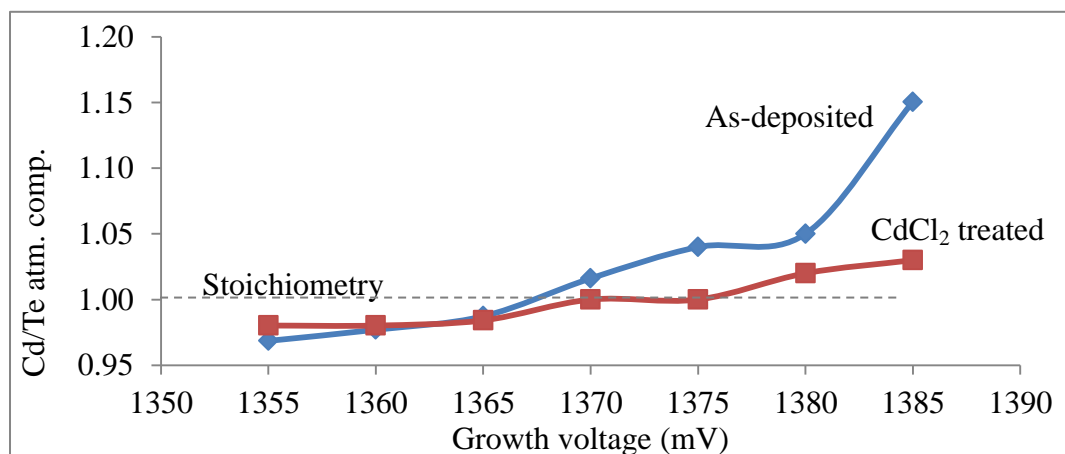
Figure 5.8: Graphical representation of percentage compositions ratio of Cd/Te for both as-deposited and $CdCl_2$ treated CdTe layers grown between 1355 mV and 1385 mV.

Stoichiometric CdTe layers under both as-deposited and $CdCl_2$ treated conditions were observed at ~1370 mV with the Cd/Te atomic ratio equal to 1.01.
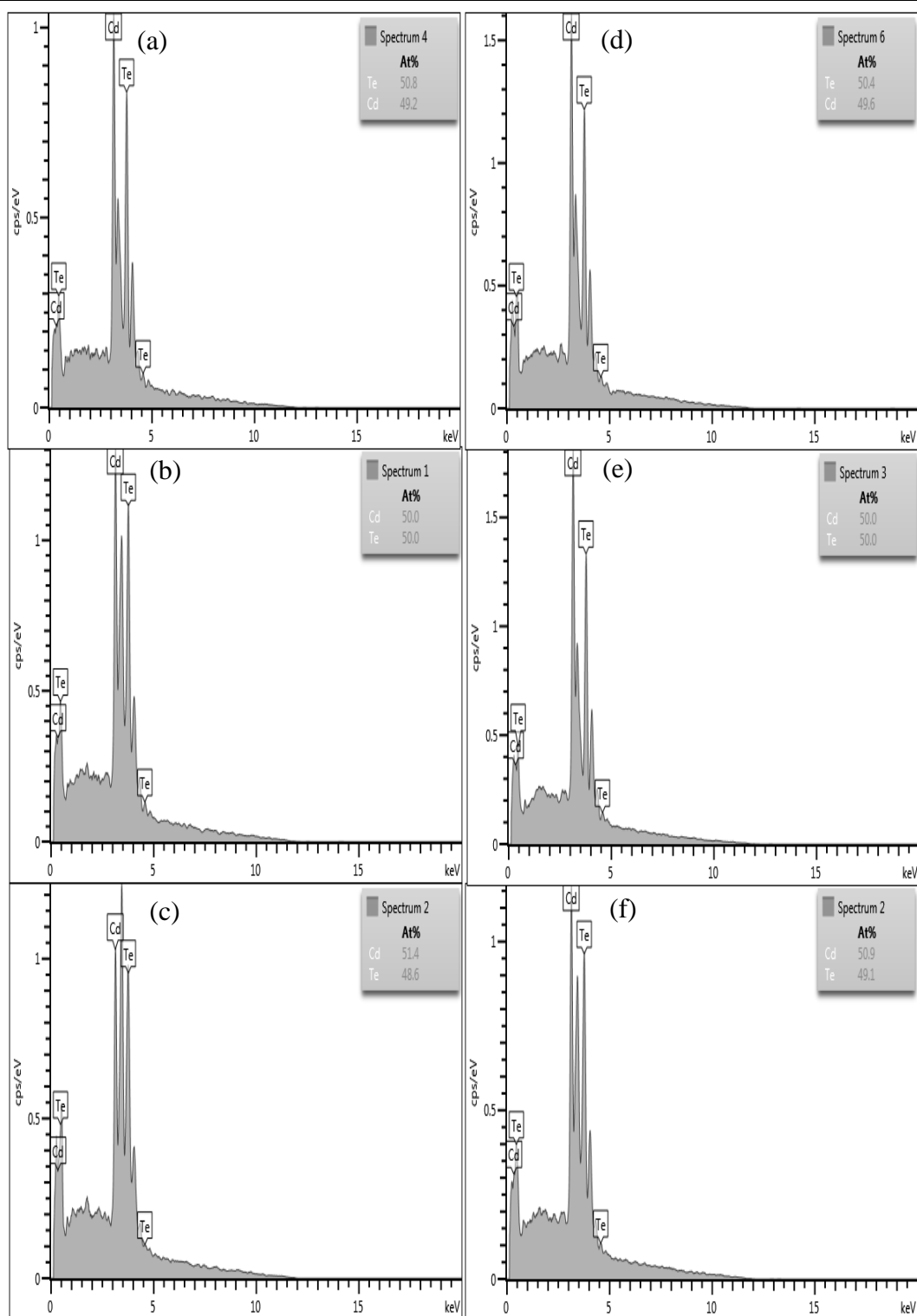
Figure 5.9: EDX spectra of the (a) Te-rich CdTe, (b) Stoichiometric CdTe and (c) Cd-rich CdTe. EDX spectra of CdCl$_2$ treated (d) Te-rich CdTe, (e) Stoichiometric CdTe and (f) Cd-rich CdTe. (All as-deposited CdTe layers were grown on the glass/FTO substrates for 2 hours duration.)

After CdCl$_2$ treatment of the CdTe layers, shifts towards stoichiometry of the Cd/Te atomic composition were observed for all the as-deposited CdTe layers. This

observation might be due to the dissolution of Te precipitates [44], sublimation of elemental Cd and Te from the CdTe layer and the reaction between unreacted Te with Cd from $CdCl_2$ [157]. This observation is in accord with the summations made in other sections.

5.3.8   Photoelectrochemical (PEC) cell measurement

The graphs of PEC measurements of the CdTe thin films grown between 1355 mV and 1385 mV under both as-deposited and $CdCl_2$ treated conditions against growth voltage is shown in Figure 5.10. The electrical conductivity type of the CdTe layer is determined by the polarity of the measured voltage difference as described in Section 3.4.7. As shown in Figure 5.10, electrodeposited CdTe layers can be deposited as either an *n-*, *i-* or *p*-type conductivity without extrinsic doping of CdTe layers [102]. From observation, the as-deposited CdTe layers deposited below 1370 mV were *p*-type, while the layers deposited at 1370 mV and above were *n*-type in electrical conduction. A transition growth voltage (V_i) from *p*-type to *n*-type CdTe was observed in-between 1365 mV and 1370 mV. After $CdCl_2$ treatment, a shift in the atomic composition ratio towards stoichiometry was observed. This might be due to the reaction between unreacted Te with Cd from $CdCl_2$ and the sublimation of excess elemental Cd and Te from the layer. The V_i depicts the growth voltage in which the atomic ratio of Cd to Te is at 1:1.
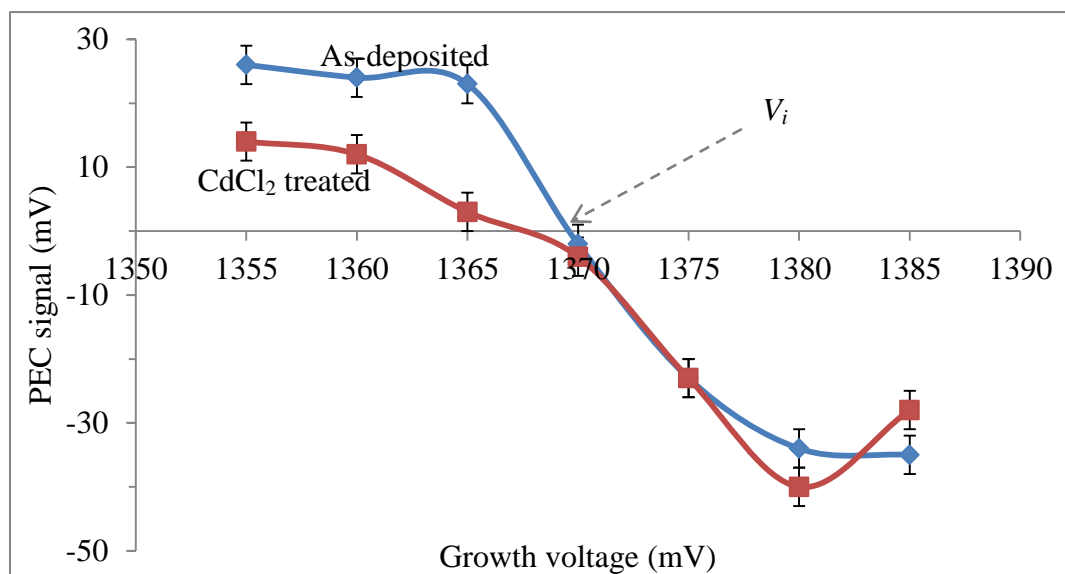
Figure 5.10: PEC signals for CdTe layers grown at different cathodic potentials, showing a transition from *p*- to *n*- type electrical conduction type at ~1370 mV.

Figure 5.11 shows the comparison between the compositional analysis as discussed in Section 5.3.7, structural analysis as discussed in Section 5.3.2 and the PEC cell measurement for the as-deposited CdTe layers grown between 1355 mV and 1385 mV.
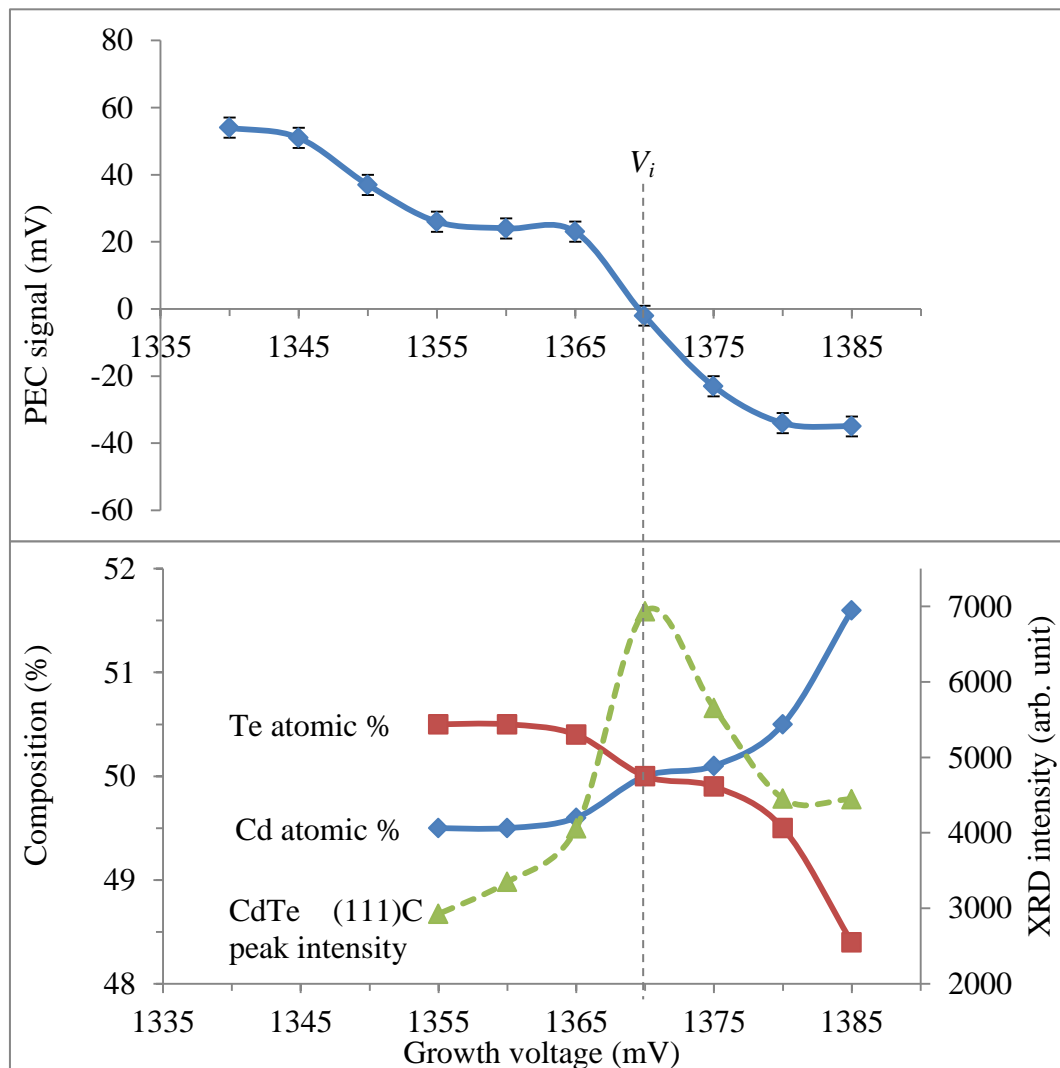
Figure 5.11: (a) PEC signals and (b) (111) XRD peak intensity for cubic CdTe and atomic composition of CdTe layers grown at different cathodic potentials between 1340 mV and 1385 mV, from electrolyte containing $Cd(NO_3)_2$ and TeO_2 solution. The p- to n-transition and the highest crystallinity of CdTe occur at the growth voltage of V_i when the composition changes from Te-rich to Cd-rich. (Adapted from Ref [24])

It can be deduced from Figure 5.11 that the conductivity type of the as-deposited CdTe layers electroplated under the conditions of this work is intrinsically affected by the elemental composition of Cd and Te. Te-richness gives p-CdTe and Cd-richness resulting in n-CdTe. The highest crystallinity of CdTe can be achieved at V_i (~1368 mV). After $CdCl_2$ treatment, although a shift towards the opposing conduction types was observed for both the p- and the n-type CdTe layers, their conductivity types were

retained. The observed shift towards stoichiometry can be attributed to the sublimation of excess element, the formation of CdTe via a chemical reaction between Cd from $CdCl_2$ and excess Te. Asides from the above mentioned, it should be noted that conductivity type change after $CdCl_2$ treatment may also be due to the heat treatment temperature, duration of treatment, initial atomic composition of Cd and Te, the concentration of $CdCl_2$ utilised in treatment, defect structure present in the starting material, and the material's initial conductivity type as documented in the literature [152,157,170,180].

5.4   Effect of CdTe thickness

For this set of experiments, $CdCl_2$ treated CdTe layers of thicknesses ranging between ~600 nm, and ~1800 nm were utilized. The CdTe layers were grown at a pre-optimised growth voltage of 1370 mV as discussed in Section 5.3. It should be noted that the effects of thicknesses of the as-deposited CdTe layers were not explored due to its triviality.

5.4.1   X-ray diffraction study based on CdTe thickness

Figure 5.12 (a) shows the XRD patterns of CdTe layers with different thicknesses, while Figure 5.12 (b) shows the graph of the (111)C CdTe peak intensity and crystallite size as a function of CdTe layer thicknesses.
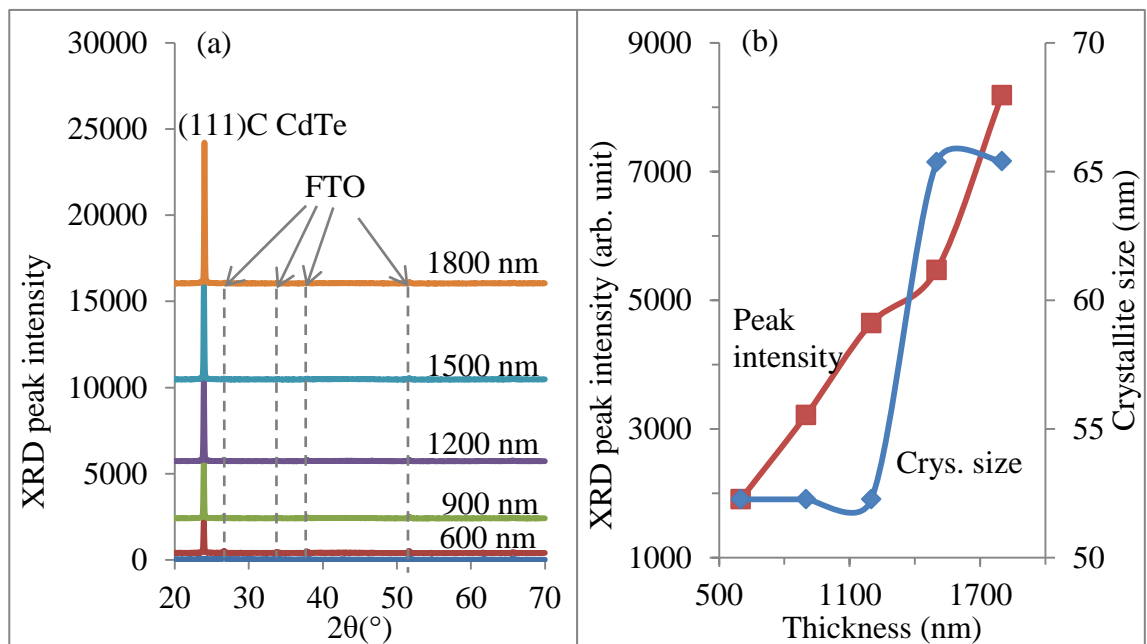
Figure 5.12: (a) Typical XRD patterns of different CdTe layer thicknesses after $CdCl_2$ treatment and (b) Analysis based on C(111) CdTe peak intensity and crystallite size as a function of CdTe thickness.

For all the explored CdTe thicknesses, the preferred orientation of (111) cubic CdTe were retained. Furthermore, a direct relationship between CdTe layer thickness and (111)C CdTe diffraction intensity was also observable as shown in Figure 5.12 (b), with the increase in CdTe layer thickness resulting into increase in (111)C CdTe intensity. With an emphasis on the crystallite size/CdTe thickness relationship as shown in Figure 5.12 (b), an increase in the crystallite size as calculated using Scherrer's equation was observed. As explained in the literature, the increase of the crystallite size (due to a decrease in FWHM) with an increase in CdTe layer thickness reflects the decrease in the concentration of lattice imperfections due to the decrease in the internal micro-strain within the films and an increase in the crystallite size [189].

5.5   Testing the electronic quality of CdTe

5.5.1   Current-Voltage Characteristics with Ohmic contacts (DC conductivity)

For this study, CdCl$_2$ treated CdTe layers deposited at different growth voltage between 1355 mV, and 1385 mV were utilised. The thicknesses of the CdTe layers utilised were maintained at ~1000 nm. Ohmic contacts were formed with the CdTe layers depending on the conductivity type. 100 nm thick gold (Au) contacts were evaporated on p-CdTe layers to give glass/FTO/p-CdTe/Au configuration, while 100 nm thick indium (In) contacts were evaporated on the n-CdTe to give glass/FTO/n-CdTe/In configuration. The metallisation processes were performed at 10^{-5} Nm^{-2}.

Table 5.3: Table of Resistance, resistivity and conductivity as a function of growth voltage.

Growth voltage (mV)	Resistance R (Ω)	Resistivity ρ $\times 10^3$ (Ω.cm)	Conductivity σ $\times 10^{-4}$ (Ω.cm)$^{-1}$
1355	34.84	7.10	1.41
1360	22.44	7.05	1.42
1365	22.65	7.12	1.41
1370	28.08	8.82	1.13
1375	16.37	5.14	1.94
1380	11.16	3.51	2.85
1385	5.28	1.66	6.03

Table 5.3 shows the resistance R, resistivity ρ and conductivity σ as a function of CdTe layer growth voltage. The resistances R were derived from the I-V curve generated under the condition as described in Section 3.4.8 and using associated Equation 3.19 and Equation 3.20. As shown in Table 5.3, a gradual increase in the conductivity with

increase in the cathodic voltage was observed which might be due to the incorporation of Cd. It should be noted that the spike in the resistance for the CdTe layer grown at 1370 mV might be due to the possible 1/1 atomic composition of Cd/Te in CdTe.

5.6 Doping of CdTe

Based on electronic and optoelectronic properties, CdTe has proved to be an excellent II-VI semiconductor material with a near-ideal direct bandgap of 1.45 eV [95] at ambient temperature for a single *p-n* junction. CdTe has attracted increasing interest due to its application in nuclear radiation detectors [190] and also in photovoltaic (PV) application. With photovoltaics (PV) being within the confines of this thesis, CdTe-based solar cells have been well explored with its main deficiency being the formation of tellurium precipitates distributed randomly over the whole volume of the CdTe layer during growth [109,181,191]. The formation of Te precipitates within the CdTe layer creates uncertainty in the post-growth and post-growth treatment stoichiometry control. Post-growth treatment in the presence of Cd [192] and halogens such as Cl, F and I [193–196] has been documented in the literature to reduce the Te precipitation [44]. Fernandez, 2003 [181] has also demonstrated the possibility of eliminating Te precipitation from the bulk of CdTe layer using gallium melt treatment, although, high Te precipitation density was observable on the opposite side of the surface not in contact with the Ga melt treatment. This observation was described as the capability of Ga to dissolve the Te precipitates in CdTe [181,192].

Although it has been argued that the complete elimination of Te precipitate in CdTe through growth modification or post-growth treatment conditions is impossible [181], this work focuses on the possibility of eliminating Te precipitates by the inclusion of different dopants such as Cl, F, I and Ga (in different CdTe baths) at different concentrations during the electrodeposition of CdTe. Furthermore, this section also evaluates the effect of these dopants on the electronic properties of CdTe to facilitate the device construction and thus promote their practical applications.

5.6.1 Effect of F-doping on the material properties of CdTe

CdTe has been extensively explored and tailored towards photovoltaic applications, especially the CdS/CdTe thin film configuration which has achieved efficiency up to 21.5% in 2015 [18,197]. The efficiency of the fabricated cells depends on all the layers and the corresponding interface states with special emphasis on the post-growth treatment with halogens such as chlorine and fluorine. $CdCl_2$ post-growth treatment has

been reported in the literature as an essential and sensitive step due to the enhancement in the photoelectrical, structural and morphological properties of CdTe layers which are crucial to achieving high-efficiency solar cell [30,157,180]. With an emphasis on fluorine, Rios-Flores [198] and Echendu et al. [199] amongst other authors have also reported further enhancement in CdTe properties with the inclusion of fluorine during CdTe growth and $CdCl_2$ post-growth treatment respectively. The incorporation of fluorine is deemed to increase the conductivity of the CdTe layer due to the excess electrons supplied by fluorine. The literature on the optimal concentration of fluorine in CdTe has not been well established in electrodeposited CdTe. Therefore, this work focuses on the optimisation of extrinsic fluorine doping concentration in CdTe thin films electrodeposition bath to achieve better material and device properties.

5.6.1.1 Growth of F-doped CdTe layers

Further to the CdTe bath preparation as described in Section 5.2.1, cadmium fluoride (CdF_2) of analytical reagent grade of 5N (99.999%) with a varied concentration between 0 and 50 ppm was incorporated into different electrolytic baths with the same measured precursors. The electrolyte was prepared by dissolving 1M $Cd(NO_3)_2 \cdot 4H_2O$ in 300 ml of deionized water contained in a 500 ml plastic beaker. Other bath conditions are a replica of the CdTe bath described in Section 5.2.1. All the CdTe:F layers deposited from all the F-doped CdTe baths were deposited at the pre-optimised cathodic voltage of 1370 mV based on the optical, structural, morphological and compositional analysis (see Section 5.2.1). A constant thickness of ~1100 nm was maintained for all the CdTe:F layers.

5.6.1.2 Material properties of CdTe:F
Structural Analysis

The structural properties of the undoped and fluorine doped CdTe layers are as presented in Figure 5.13. The CdTe layers deposited are polycrystalline with the significant presence of FTO reflections marked (*), Cd_xTeO_y reflection was observed at $2\theta=23.01°$ and prominent (111) cubic CdTe at $2\theta=23.90°$, while no reflection is associated with fluorine or fluorine compounds due to its presence in low concentration [40]. An increase in the intensity of the preferred CdTe (111)C phase was observed for the as-deposited and $CdCl_2$ treated CdTe layers with increasing F-doping concentration as shown in Figure 5.13. The XRD intensity reflection appears to have saturated at ~20 ppm for both as-deposited, and $CdCl_2$ treated layers with a steady reduction in intensity

above 20 ppm doping (see Figure 5.14). This observation suggests that the solubility limit of fluorine in the CdTe lattice at ~20 ppm, although further experimentation is still required. Increasing the F-doping concentration above this point results in a reduction in CdTe (111)C reflection intensity, incomplete crystallisation, and low adhesion to the underlying FTO substrate [200,201] as shown in Figure 5.14. This observation can be explained by the initial replacement of tellurium ions with fluorine ions in the CdTe lattice up to 20 ppm which aids the crystallisation of CdTe as shown in Figure 5.13. However, a further increase in F-doping concentration may readily be incorporated within the crystal lattice but not occupying the proper lattice position whereby increasing disorderliness results within the crystal structure [202,203]. Further to this, there is a possible formation of highly acidic hydrofluoric (HF) acid which may contribute to continuous etching of the glass/FTO and CdTe:F surfaces [166] and attacking Cd to give Te-rich CdTe layer [61].
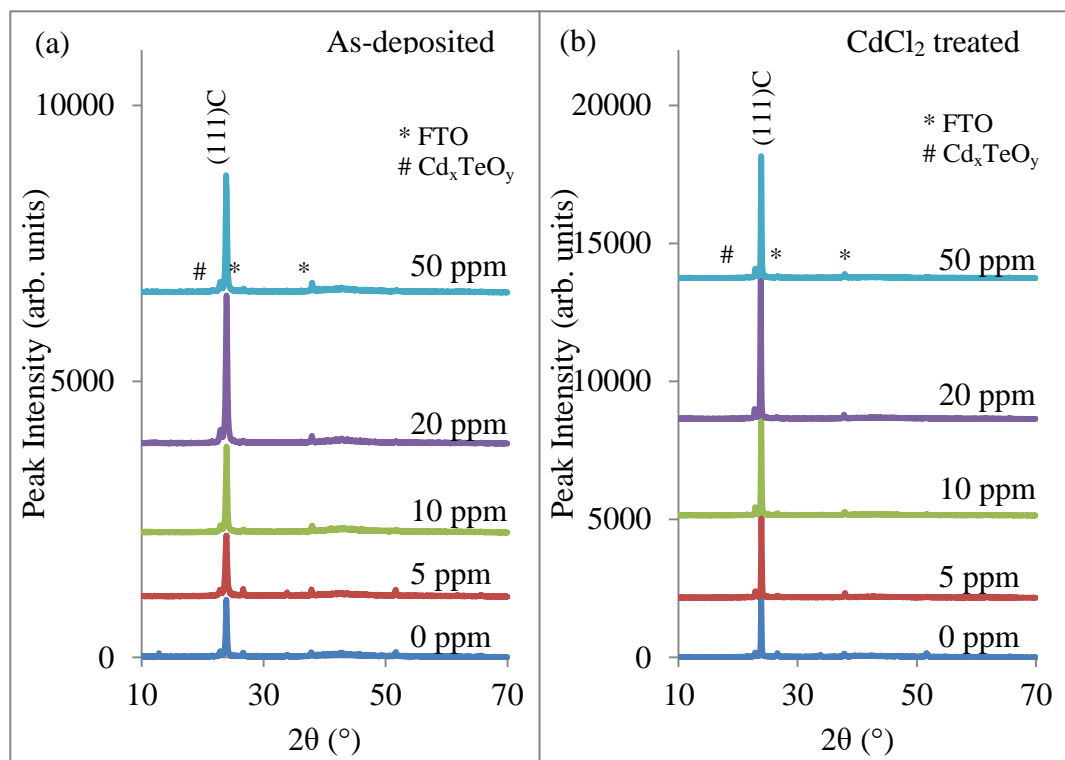
Figure 5.13: Typical XRD patterns of CdTe at different fluorine doping concentrations for (a) As-deposited CdTe layers and (b) CdCl$_2$ treated CdTe layers at 400°C for 20 min in air.

The XRD reflection intensity of layers improved after CdCl$_2$ post-growth treatment at 400°C for 20 min in the air as shown in Figure 5.13 (b) and Figure 5.14. This might be attributed to grain growth and re-crystallisation of the crystal structure. The highest

intensity was observed at 20 ppm fluorine concentration. For clarity, the observed CdTe (111)C reflection intensity was plotted against the concentration of F-doping in CdTe bath as shown in Figure 5.14. The initial reductions in full width at half maximum (FWHM) and resulting increase in crystallite size was observed with increasing F-doping concentration to 20 ppm in the as-deposited CdTe layers as shown in Table 5.4, while a further increase in F-doping concentration resulted in a reduction in the crystallite size. This observation can be attributed to the replacement of Te atoms from Group VI (atomic radius of 1.4 Å) with F atoms having a comparatively low atomic radius of ~0.5 Å from Group VII. This might lead to the contraction of the CdTe lattice, hence, a reduction in crystallite size [204,205] with increasing F atom concentration as observed in the as-deposited CdTe layer grown above 20 ppm concentration as shown in Table 5.4. The calculated crystallite size, D, for all the $CdCl_2$ treated CdTe layers using Scherrer's equation were all ~ 52.4 nm. The observation of the same value (~52.4 nm) for all F-doping concentration indicates the limitation of the use of Scherrer's equation for materials with larger grains [115].

The extracted XRD data from this CdTe work matches the Joint Committee on Powder Diffraction Standards (JCPDS) reference file number 01-075-2086-cubic.
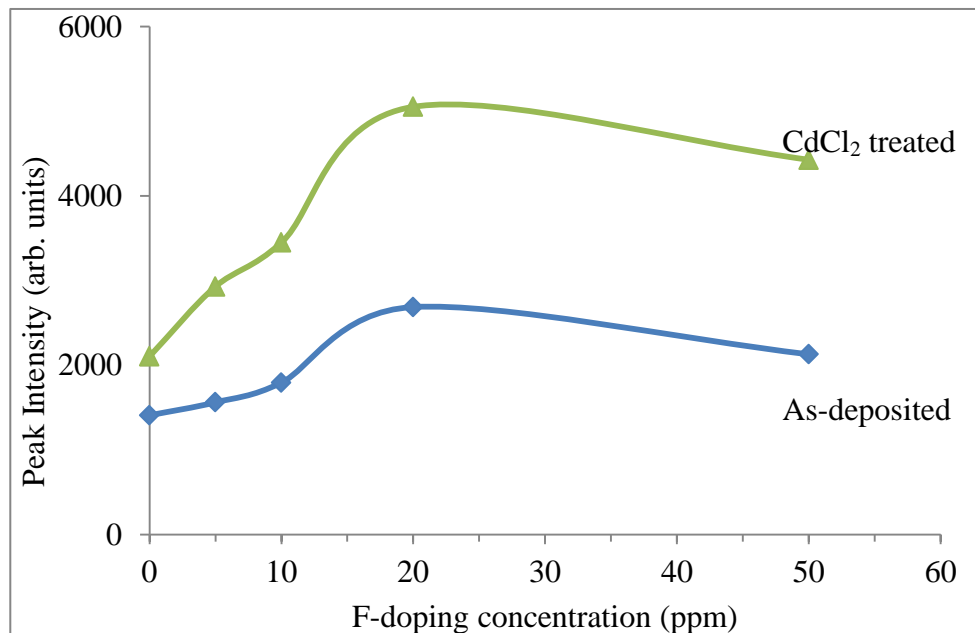
Figure 5.14: Comparative analysis of CdTe (111)C reflection intensity for as-deposited and $CdCl_2$ treated layers grown at different fluorine doping concentrations.

Table 5.4: The XRD analysis of CdTe layers grown at different fluorine concentrations.

F concentration (ppm)	2θ (°)	Lattice spacing (Å)	FWHM (°)	Crystallite size D (nm)	Plane of orientation (h k l)	Assignments
As-Deposited						
0	23.90	3.72	0.260	32.6	(111)	Cubic
5	23.91	3.72	0.259	32.8	(111)	Cubic
10	23.88	3.73	0.227	37.4	(111)	Cubic
20	23.90	3.72	0.227	37.4	(111)	Cubic
50	23.91	3.72	0.292	29.1	(111)	Cubic
CdCl$_2$ treated						
0	23.90	3.72	0.162	52.4	(111)	Cubic
5	23.93	3.72	0.162	52.4	(111)	Cubic
10	23.90	3.89	0.162	52.4	(111)	Cubic
20	23.90	3.74	0.162	52.4	(111)	Cubic
50	23.89	3.72	0.162	52.4	(111)	Cubic

Analysis of optical absorption

The optical bandgap of the as-deposited and CdCl$_2$ treated CdTe layers was analysed by plotting the A^2 against photon energy (hv) as shown in Figure 5.15 Noticeably in Figure 5.15 (a), stronger absorption edges were observed with increasing F-doping concentration in the as-deposited CdTe layers with no observable influence on the bandgap energy. The observed bandgap energy for the test samples falls within the range of 1.47 eV to 1.50 eV. A dissimilar trend was observed after CdCl$_2$ treatment of the CdTe layers as shown in Figure 5.15 (b). For CdTe doped with (0 to 20) ppm fluorine, a rise in the absorption edge, coupled with a reduction in the bandgap energy was observed. These observations can be attributed to improvement in material properties such as grain size, crystallinity amongst others. An increase in the doping above 20 ppm resulted in a reduction in the gradient of the optical absorption edge and also an increase in the optical bandgap [30,206]. This might be due to material quality deterioration such as sublimation of CdTe layer. It could be deduced from the optical parameters that fluorine doping concentration of ~20 ppm gives the best optical property with 1.46 eV bandgap. This observation is in accord with the structural and morphological observations.
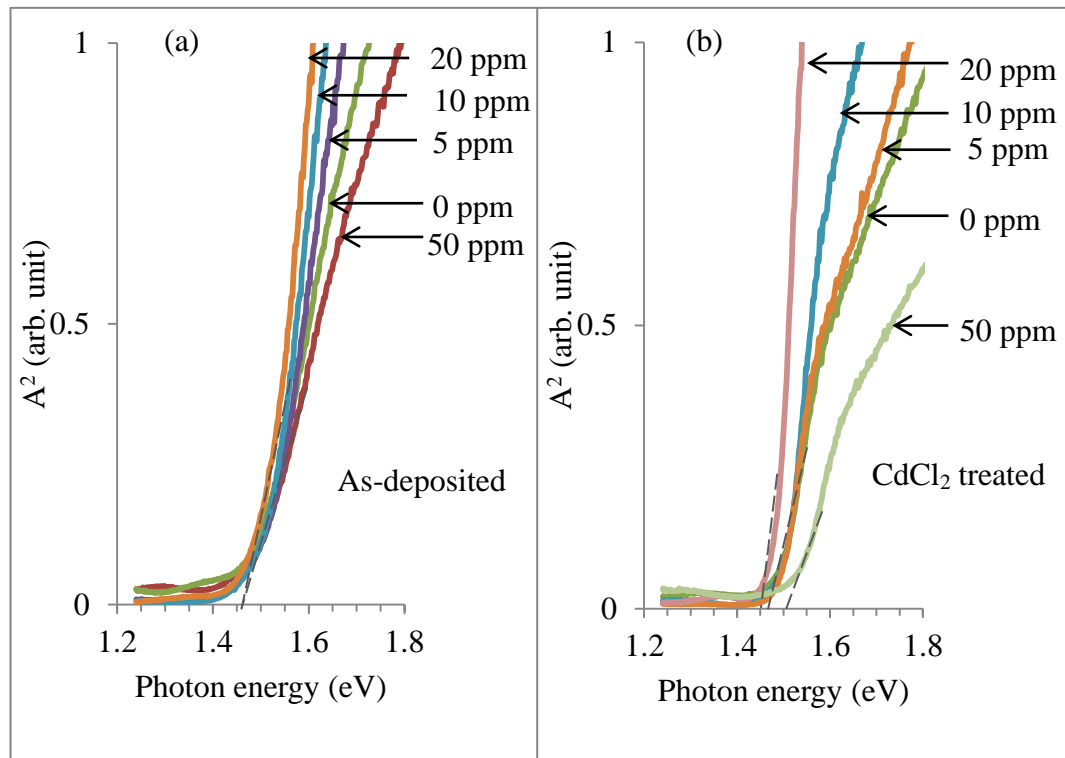
Figure 5.15: Optical absorption edge of CdTe with different doping concentrations of fluorine for (a) as-deposited, and (b) CdCl$_2$ treated (at 400˚C for 20 min in air) layers.

Morphological Analysis

Figure 5.16 (a), Figure 5.16 (b) and Figure 5.16 (c) represents the as-deposited CdTe layers containing 0, 20 and 50 ppm F-doping concentration respectively, while Figure 5.16 (d), Figure 5.16 (e) and Figure 5.16 (f) are the resulting micrographs after CdCl$_2$ treatment respectively. The as-deposited layers show full coverage of the underlying FTO substrate with a noticeable reduction in grain size and indistinct crystal boundary at 50 ppm F-doping concentration. The morphology reveals that the formation of grain boundaries has been suppressed due to the presence of superfluous fluorine at high concentration. The CdCl$_2$ treated layers show grain growth of ~(1, 1.9 and 1.4) μm for (0, 20 and 50) ppm F-doping concentration respectively. It could be said that the addition of fluorine to ~20 ppm is advantageous to grain growth while the inclusion of fluorine to 50 ppm is detrimental as observed in Figure 5.16 (f). Although large grains were observed, the formation of pin-holes and loss of CdTe layer will be detrimental to device parameters due to shunting.
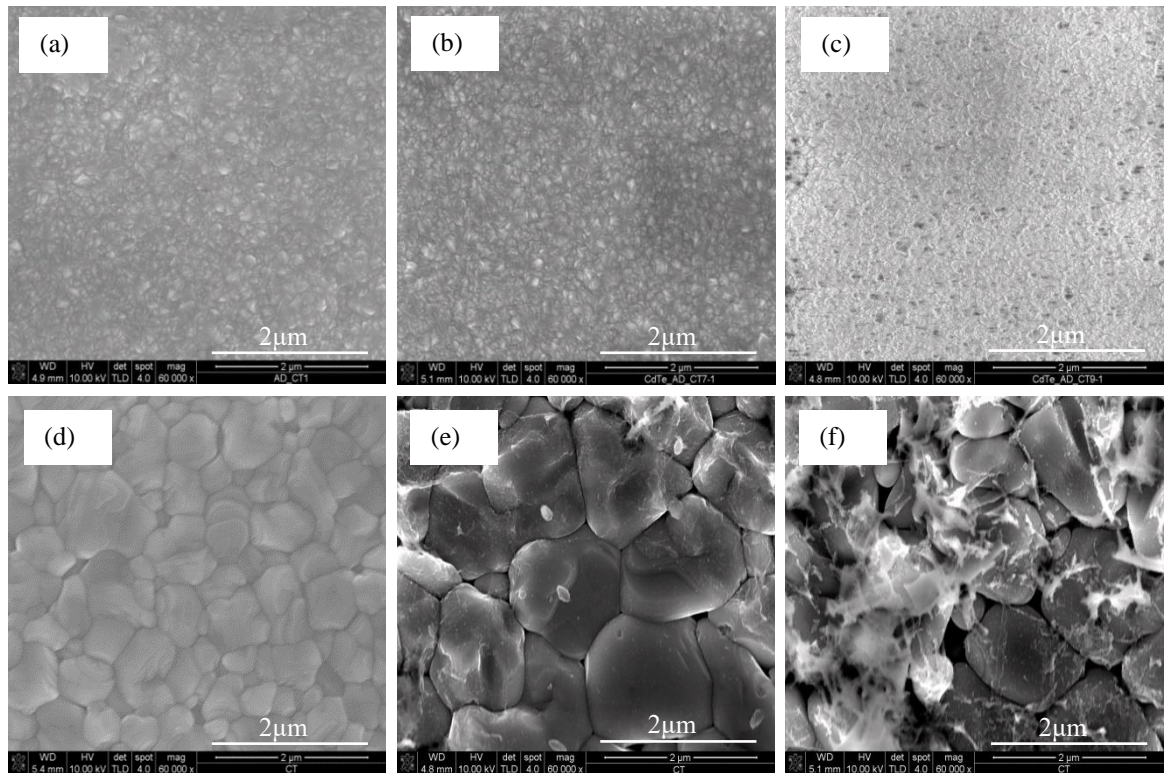
Figure 5.16: SEM micrographs for CdTe layers grown with F-doping concentration of (a) 0, (b) 20 and (c) 50 ppm and after CdCl$_2$ treatment of CdTe with F-doping of (d) 0, (e) 20 and (f) 50 ppm.

Compositional Analysis

The presence of base elements (Cd and Te) was observed at all doping concentrations of fluorine, and their percentage concentration for the as-deposited CdTe thin films is presented in Table 5.5. It was observed that the atomic composition of Cd was greater than Te in all the explored fluorine doping concentration range with an increase in the Cd/Te atomic composition ratio as shown in Table 5.5. This observation may not be due to the continuous replacement of Te ions with F ions at ppm level in the crystal lattice. It is important to note that due to the presence of nominal fluorine in ppm level in the electrolytic bath, the atomic concentration of fluorine in CdTe thin films at different concentration cannot be determined. However, the presence F in the electrolyte seems to act as a catalyst to produce Cd-rich layers. As argued by Dharmadasa et al., the defect levels in Cd-rich material is lower than those in Te-rich material [207]. Therefore, the CdTe layers doped with F should produce solar cell devices with enhanced parameters. In addition to the presence of Cd and Te atoms, the EDX results may show the presence of Sn, Si, F and O which is due to the underlying glass/FTO substrate and the oxidation

of CdTe film surface. The observation made from the compositional analysis gives a clue why the conductivity type is always *n*-type.

Table 5.5: Summary of the compositional analysis of as-deposited CdTe layers at different F doping concentration in CdTe bath.

F-doping concentration (ppm)	Atomic composition (%)		Cd/Te ratio
	Cd	Te	
0	51.70	48.30	1.07
5	51.80	48.20	1.07
10	52.20	47.80	1.09
20	53.50	46.50	1.15
30	53.40	44.60	1.19
50	55.30	44.70	1.25

Photoelectrochemical (PEC) Cell Study

Figure 5.17 shows a typical photoelectrochemical cell measurement of CdTe doped with a different concentration of fluorine. It was observed that both the as-deposited and $CdCl_2$ treated CdTe layers were all *n*-type in electrical conduction. This might be due to the presence of fluorine, an *n*-type dopant in the electrolytic bath. It has been well documented in the literature that the inclusion of halogens in CdTe serves as electron donor impurities by replacing Te atoms in the CdTe lattice with halogen atoms with higher valence electrons. This introduces additional free electrons and therefore makes the CdTe *n*-type. It should be noted that *n*-, *i*- and *p*- CdTe layers can be grown from the 0 ppm F-doping (i.e., undoped) CdTe bath through growth voltage alteration [170].

As shown in Section 5.6.1.2 (see compositional analysis), the presence of F in the bath replaces and reduces the excess deposition of Te. The Cd-richness makes the material more *n*-type in electrical conduction. The increase in observed PEC signal with increasing F-doping concentration might be due to increasing free electrons from the F-doping and increased Cd-richness.

As observed in Figure 5.17, the PEC signals for all $CdCl_2$ treated CdTe layers in this work tend to reduce. This difference can be attributed to the improvement in the material's electronic properties by the sublimation of excess element during the annealing process or the formation of CdTe through a chemical reaction between

precipitated Te in the layer and excess Cd from $CdCl_2$. Furthermore, the observed changes can also be attributed to the doping effect of fluorine.
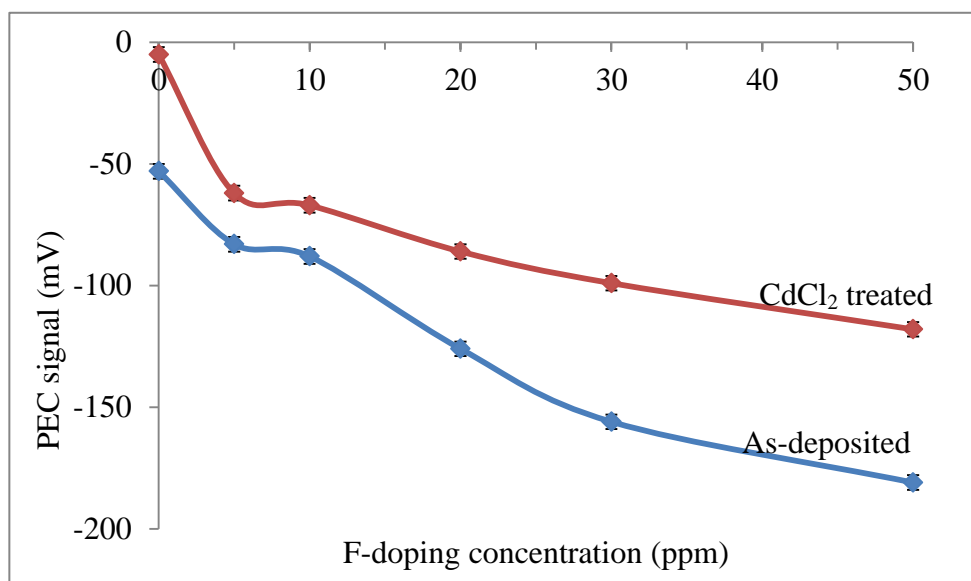
Figure 5.17: Photoelectrochemical cell measurement for both as deposited and $CdCl_2$ treated fluorine doped CdTe thin films.

DC conductivity study

The DC conductivity measurement was carried out on glass/FTO/*n*-CdTe/Al structure with different F-doping concentrations. The CdTe layers utilized in this experiment were ~1.1 µm thick, and $CdCl_2$ treated at 400˚C for 20 min in air. The evaporated Al on the CdTe was to make an Ohmic contact, while the I-V measurements were taken in dark conditions. By measuring several Ohmic contacts, the average resistance of the glass/FTO/*n*-CdTe/Al structures were determined. The electrical resistivity and conductivity were calculated with a known contact area and film thickness.

A typical DC conductivity against F-doping concentration in the CdTe bath is plotted in Figure 5.18. It was observed that the introduction of fluorine increases the electrical conductivity of the layers which saturates at ~20 ppm fluorine concentration. The saturation of DC conductivity further suggests the solubility limit of fluorine in CdTe lattice [202] as discussed in Section 5.6.1.2 (see structural and morphological analyses). Therefore, an increase in F-doping above 20 ppm results into superfluous addition under this experimental condition. As explained in Section 5.6.1, the inclusion of fluorine into the crystal lattice introduces free electrons which result in increased conductivity. The

enrichment of Cd also contributes to the electrical conductivity and the resultant effect is measured using this method.

Table 5.6: Electrical resistivity and conductivity as a function of fluorine doping concentration in the electrolytic bath.

F-doping concentration (ppm)	Resistance (Ω)	Resistivity $\times 10^3$ ($\Omega.cm$)	Conductivity $\times 10^{-4}$ ($\Omega.cm)^{-1}$
0	18.75	9.72	1.03
5	17.15	8.97	1.12
10	15.29	5.91	1.73
20	10.52	5.51	2.03
50	8.60	4.60	2.23
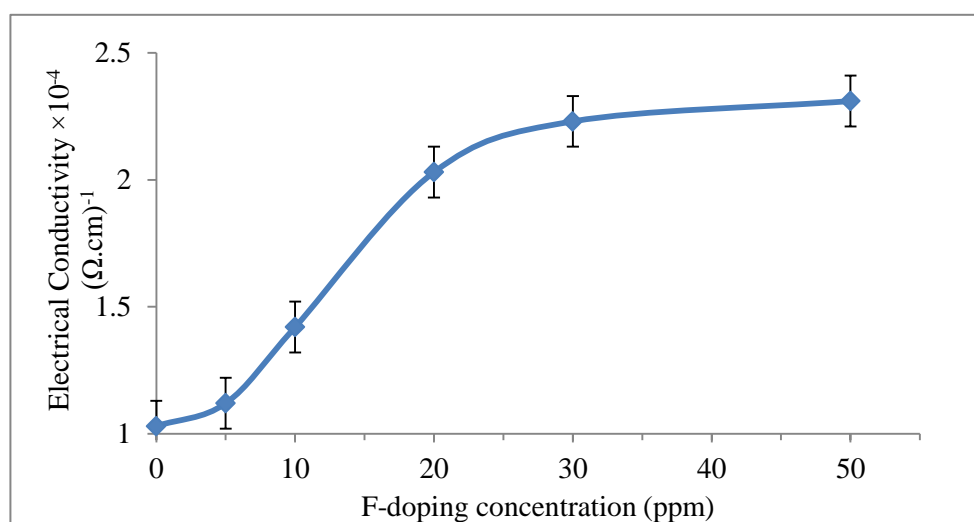
Figure 5.18: Graph of electrical conductivity against F-doping concentration in CdTe bath.

Summations

In this work, we have explored the effect of fluorine doping in a CdTe electrolytic bath on the CdTe layer as it affects it's structural, optical, morphological and compositional properties. An optimal F-doping concentration of 20 ppm in the electrolytic bath was observed under all material characterisations explored in this work due to the solubility limit achieved at 20 ppm F-doping and deterioration in material property afterward.

5.6.2   Effect of Cl-doping on the material properties of CdTe

Based on the initial observation of the improvement in CdTe material property with increasing concentration of chlorine doping in the CdTe bath, CdTe was grown from an electrolytic bath with the chlorine-based precursor. Therefore, the effect of growth voltage on the characteristic properties of the CdTe:Cl layers will be explored.

5.6.2.1   Growth of Cl-doped CdTe layers

CdTe:Cl thin films were electrodeposited cathodically on glass/FTO substrates by a potentiostatic technique in which the anode was a high purity graphite rod (see Section 3.3). The main difference to the CdTe bath as described in Section 5.3 is the utilisation of 1.5 M cadmium chloride hydrate $CdCl_2 \cdot xH_2O$ of 99.995% purity as cadmium precursor, while the setup and substrate preparation remained identical.

5.6.2.2   Material properties of CdTe:Cl

Cyclic Voltammetric Study

Figure 5.19 shows the cyclic voltammogram of an aqueous solution containing a mixture of 1.5 M $CdCl_2 \cdot xH_2O$ and a low level of pre-prepared TeO_2 solution in 400 ml of DI water during the forward and reverse cycle between 100 mV and -2000 mV cathodic voltage. The electrolytic bath pH was adjusted to 2.00±0.02 using dilute solutions of HCl and NH_4OH. The stirring rate and bath temperature were maintained at 300 rpm and ~85˚C respectively. Tellurium deposits first in the electrodeposition process due to its standard reduction potential value of +593 mV with respect to the standard H_2 electrode which is more positive than that of cadmium with standard reduction potential value of -403 mV.

It was observed from Figure 5.19 that the deposition of Te starts in the forward cycle at the cathodic potential of ~400 mV under the experimental conditions used (inset in Figure 5.19) according to the electrochemical reaction similar to Equation 5.1.

With an increase in cathodic potential, more Te is deposited. The deposition of Cd and formation of CdTe starts around ~1000 mV cathodic potential as depicted by the first hump shown in Figure 5.19. Tellurium-rich CdTe is expected at the initial stage of deposition of cadmium, afterward, with an increase in deposition potential and there exists a narrow cathodic potential window in which stoichiometric CdTe compound can be deposited. Further increase in the cathodic potential above this point increases the cadmium richness of electrodeposited CdTe. The electrochemical equation for Cd

deposition and the complete CdTe formation are similar to Equation 5.2 and Equation 5.3 respectively.
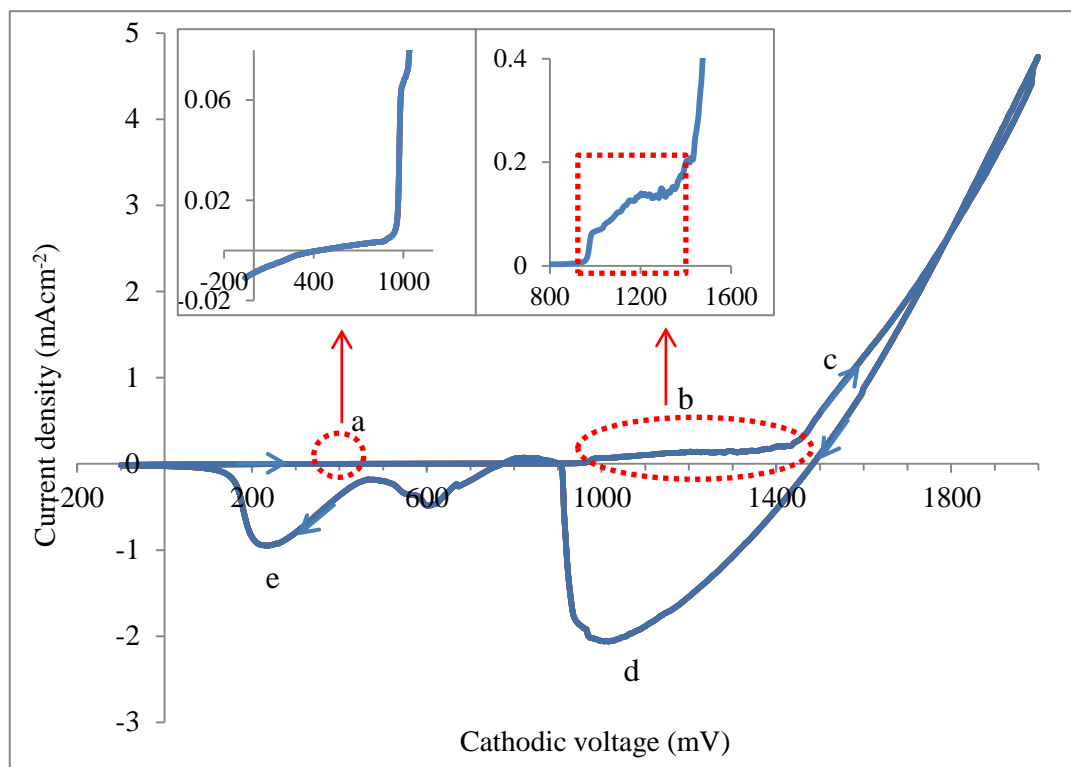
Figure 5.19: A typical cyclic voltammogram for deposition electrolyte containing the mixture of 1.5 M $CdCl_2 \cdot xH_2O$ and 0.0002 M TeO_2 solution at ~85°C and pH=2.00±0.02. The scan rate was set to 3 mVs^{-1}. The insets are the expanded sections of the forward cycle for both Te and Cd deposition initiation.

It should be noted that the steep increase in current density (marked c) at a cathodic voltage above ~1400 mV is due to either the formation of Cd dendrites on the working electrode or the electrolysis of water at any deposition potential above ~1230 mV [172]. Both scenarios have been reported to have a detrimental effect on the quality of the deposited CdTe layer [106]. However, the release of most active hydrogen atoms on the material surface also introduces an advantage of hydrogen-passivation during growth although the formation of hydrogen bubbles could be a disadvantage due to a possible cause of material layer peeling. Therefore, selecting the growth voltage has a crucial effect on the growth of a suitable CdTe layer. In the reverse cycle, the dissolution of elemental Cd and Cd from CdTe occurs in the voltage range of ~1500 mV and ~1000 mV, while the dissolution of Te from the glass/FTO substrate occurs below 750 mV as shown in Figure 5.19. Therefore, based on the information obtained from the voltammetric study, a cathodic potential range between 1000 mV and 1400 mV was

pre-characterised using XRD for as-deposited CdTe layers grown at a step size of 50 mV (results not presented in this thesis). The highest peak intensity signaling highest crystallinity was observed at 1350 mV, therefore, surrounding cathodic potentials were scanned at 10 mV intervals and characterised to identify the best cathodic potential in which stoichiometric and near-stoichiometric CdTe can be achieved.

X-ray Diffraction Study

This study aims to identify the cathodic potential in which stoichiometric or near-stoichiometric CdTe can be grown. This was done by observing the level of crystallinity through XRD peak intensity. Figure 5.20 (a) and Figure 5.20 (b) shows typical X-ray diffraction intensity plotted against 2θ angle for layers grown between 1330 mV and 1400 mV for both as-deposited and $CdCl_2$ treated CdTe layers. For both the as-deposited and $CdCl_2$ treated CdTe layers, only cubic CdTe phases were observed. CdTe (111)C peak corresponding to $2\theta=\sim23.8°$ is the dominant XRD peak and the preferred orientation of the electrodeposited CdTe at all growth voltages and conditions. Peaks attributed to CdTe, (220)C and (311)C corresponding to $2\theta=\sim38.6°$ and $2\theta=\sim45.8°$ were also observed asides the FTO peaks observed at $2\theta=20.6°$, $33.8°$, $37.9°$, $51.6°$, $60.7°$ and $65.6°$.
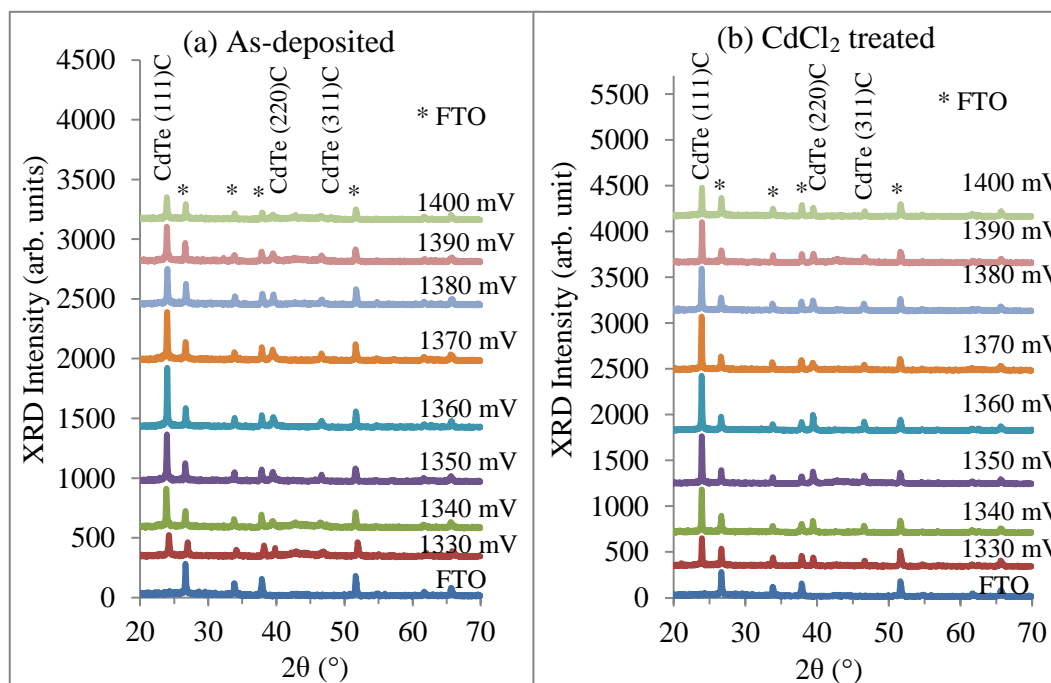
Figure 5.20: Typical XRD patterns of CdTe layers grown between 1330-1400 mV deposition potential for (a) As-deposited CdTe layers and (b) $CdCl_2$ treated CdTe layers at 400°C for 20 minutes in air.

For better comparison, XRD patterns were shifted up in the graph as shown in Figure 5.20 (a) and Figure 5.20 (b). As observed in both Figure 5.20 (a) and Figure 5.20 (b), the highest XRD peak intensity of the CdTe (111)C for both as-deposited and $CdCl_2$ treated CdTe layers were observed at 1360 mV. This suggests that highly crystalline CdTe corresponding to stoichiometric CdTe can be electrodeposited at 1360 mV cathodic voltage.

Figure 5.21 (a) shows the comparison of CdTe (111)C peak intensity as a function of the cathodic potential at which the layers were grown while Figure 5.21 (b) shows the graph of crystallite size against cathodic voltage.
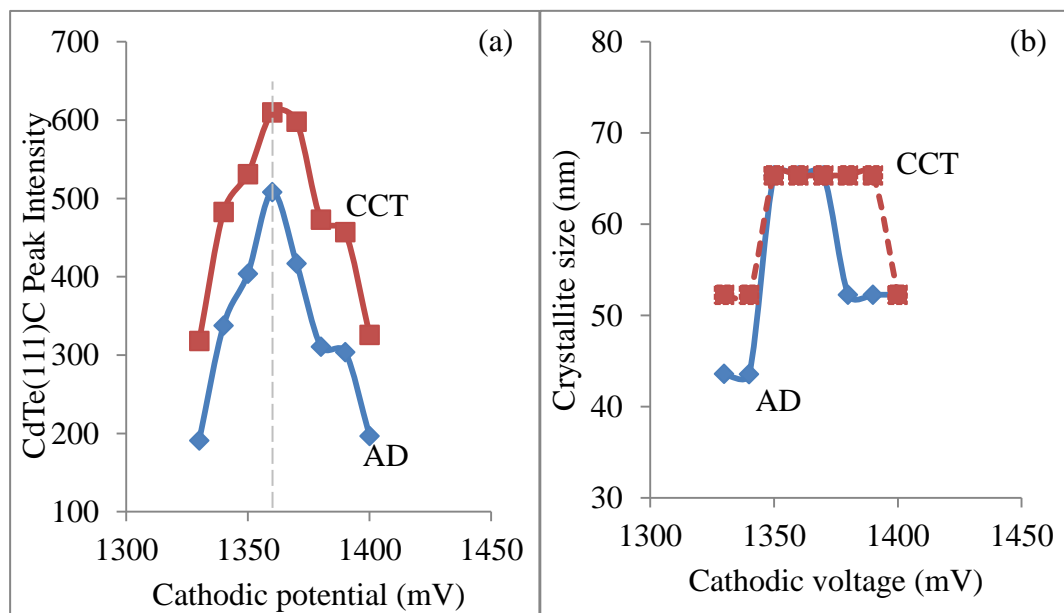
Figure 5.21: (a) Typical plots of CdTe (111) cubic peak intensity against cathodic voltage. (b) A typical plot of the crystallite sizes against cathodic voltage for the as-deposited and $CdCl_2$ treated CdTe layers grown between 1330 and 1400 mV.

It is clear from Figure 5.21 (a) that the treatment of the CdTe layer with $CdCl_2$ improved the level of crystallinity of the CdTe layers grown at all the explored cathodic voltages. This improvement can be attributed to grain growth and recrystallisation. Furthermore, this improvement could also arise from the formation of CdTe from unreacted excess Te presented in the layer reacting with Cd from $CdCl_2$ treatment. Full details of this recent understanding are reported by Dharmadasa et al., 2016 [44]. When the growth potential deviates from V_i, the crystallinity suffers due to the presence of two phases; CdTe and Te at lower cathodic potential and CdTe and Cd at high cathodic voltage.

Table 5.7: The summary of XRD analysis for CdTe layers grown for 2 hours at cathodic potentials between 1330 mV and 1400 mV for the as-deposited and the $CdCl_2$, treated layers at 400˚C for 20 minutes in air.

Cathodic voltage (mV)	2θ (°)	Lattice spacing (Å)	FWHM (°)	Crystallite size D (nm)
As-deposited				
1330	24.23	3.67	0.195	43.6
1340	23.85	3.73	0.195	43.6
1350	23.94	3.71	0.130	65.3
1360	24.02	3.70	0.130	65.4
1370	23.97	3.71	0.130	65.4
1380	23.99	3.71	0.162	52.3
1390	23.93	3.72	0.162	52.3
1400	23.95	3.71	0.162	52.3
$CdCl_2$ treated				
1330	23.95	3.71	0.162	52.3
1340	23.92	3.72	0.162	52.3
1350	23.94	3.71	0.130	65.3
1360	23.95	3.71	0.130	65.3
1370	23.91	3.72	0.130	65.3
1380	23.91	3.72	0.130	65.3
1390	23.97	3.71	0.130	65.3
1400	23.92	3.72	0.162	52.3

The extracted XRD data from these CdTe work matches the JCPDS reference file No. 01-775-2086. The crystallite size, D, was calculated using the Scherrer's formula (see Equation 3.8). The summary of XRD data and obtained structural parameters of CdTe thin films grown at cathodic voltages between 1330 mV and 1400 mV using cubic (111) peak are tabulated in Table 5.7.

As observed in Table 5.7 and Figure 5.21 (b), for the as-deposited CdTe layers, low crystallite size was observed at cathodic voltages of ±20 mV away from 1360 mV due to either Cd- or Te-richness of CdTe grown at these cathodic voltages. After $CdCl_2$ treatment, improvement in crystallite size was observed for all layers. This observation

is in accordance with the effect of $CdCl_2$ treatment on CdTe as reported in the literature [30,157]. However, it should be noted that there is a limitation of the use of Scherrer's equation in determining the crystallite size. This equation is formalised to calculate smaller grains [115] of polycrystalline materials and may not be suitable for the highly crystalline material. Therefore, as shown in Table 5.7 and Figure 5.21 (b), the crystallite size saturates at ~65 nm. This must be due to the limitation of Scherrer's equation and the XRD measurement system.

Thickness measurements

Figure 5.22 shows the graph of electrodeposited CdTe layer thickness estimated using both experimental and theoretical methods against cathodic voltage for CdTe layers grown for 120 minutes duration. The thickness of the layers grown between 1330 mV and 1400 mV was calculated theoretically using Faraday's law of electrolysis as shown in Equation 3.6.
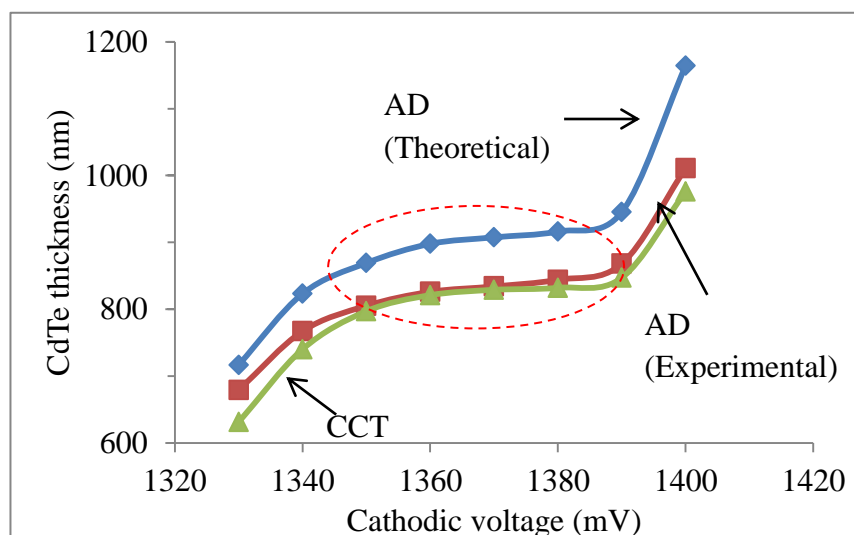
Figure 5.22: Graph of CdTe layer thickness (theoretical and experimental) against cathodic voltages for both as-deposited and $CdCl_2$ treated CdTe layers.

As observed in Figure 5.22, the value of the calculated thickness using Faraday's law of electrolysis was higher than the measured thickness. It should be noted that Faraday's law of electrolysis assumes that all the electronic charges flowing through the electrolyte contribute to the deposition of the CdTe layers without considering the electronic charges involved in the decomposition of water into its constituent ions. It was further observed that an increase in the cathodic voltage results in an increase in current density and hence affects deposited CdTe layer thickness. After $CdCl_2$

treatment, a slight reduction in thickness was observed. This might be due to the sublimation of CdTe or excess elemental Cd or Te. This also can be due to the formation of a denser layer after $CdCl_2$ treatment, between 1350 mV and 1390 mV cathodic voltages, a slightly uniform cathodic voltage which is an indication of the formation of CdTe layer with close deposition current density.

Optical Absorption Study

Using the data acquired through Carry 50 Scan UV-Vis spectrophotometer, the square of the absorbance (A^2) was plotted against the photon energy (*hv*) as shown in Figure 5.23 (a) and Figure 5.23 (b) for as-deposited and $CdCl_2$ treated CdTe layers grown at different growth voltages respectively. The straight line segments were extrapolated from the straight line to $A^2 = 0$ to estimate the energy bandgaps of the CdTe layers tabulated in Table 5.8 for comparison.
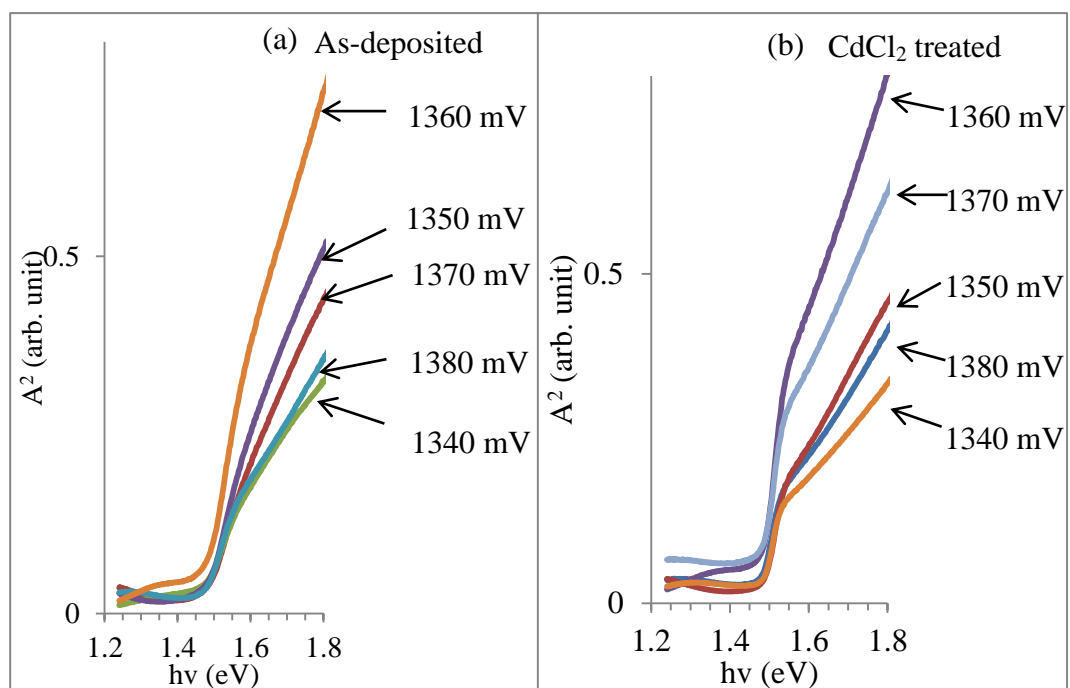
Figure 5.23: Optical absorption spectra for electrodeposited CdTe thin-films grown between cathodic voltage range between 1330 and 1400 mV; (a) for as-deposited, and (b) for $CdCl_2$ treated CdTe at 400˚C for 20 minutes in air.

As observed in Table 5.8, the bandgap of both the as-deposited and the $CdCl_2$ treated CdTe layers within the explored cathodic voltage range falls within 1.45±0.01 eV which is comparable with the bandgap of bulk CdTe [28]. As shown in Figure 5.24, the growth of CdTe at 1360 mV shows the sharpest absorption edge which signifies superior CdTe

layer [28,30] due to lesser impurity energy levels and defects in the thin film, while the growth of CdTe layer away from 1360 mV shows a reduction in the slope of the optical absorption edge in both the as-deposited and $CdCl_2$ treated CdTe layers due to Cd- or Te- richness in CdTe. It should be noted that $CdCl_2$ treatment utilised in this work increases the sharpness of the absorption edge across all growth voltages explored. This further attests to the improvement in the optical absorption of CdTe layer after $CdCl_2$ treatment as recorded in the literature.

Table 5.8: The optical bandgap and slope of absorption edge of CdTe layers grown at cathodic voltages between 1330 mV and 1400 mV for the as-deposited and the $CdCl_2$ treated layers at 400˚C for 20 minutes in air.

Cathodic voltage (mV)	Bandgap (eV)		Slope of absorption edge (eV^{-1})	
	As-deposited	$CdCl_2$ treated	As-deposited	$CdCl_2$ treated
1340	1.46	1.46	1.61	3.13
1350	1.46	1.46	2.13	3.13
1360	1.45	1.45	3.03	5.55
1370	1.45	1.45	1.75	4.35
1380	1.46	1.46	1.75	2.94
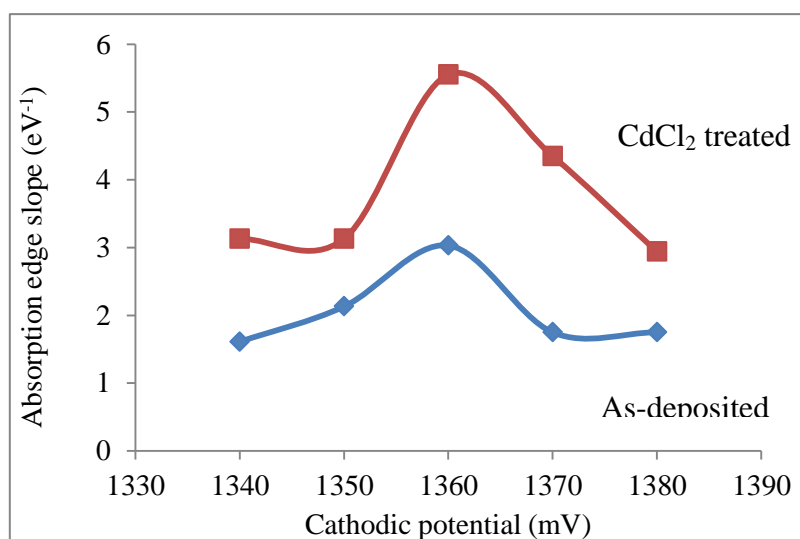
Figure 5.24: Graph of absorption edge slope against cathodic potential for as-deposited and $CdCl_2$ treated CdTe thin films.

Morphological and Compositional Analysis

For both the morphological and compositional experiments, CdTe layers were grown at cathodic voltages between 1330 mV and 1400 mV on glass/FTO for 120 minutes. Each glass/FTO/CdTe layer was divided into two halves; one half was left as-deposited while the other was $CdCl_2$ treated. Figure 5.25 shows the SEM images of as-deposited and $CdCl_2$ treated CdTe grown at 1330 mV, 1360 mV, and 1400 mV.
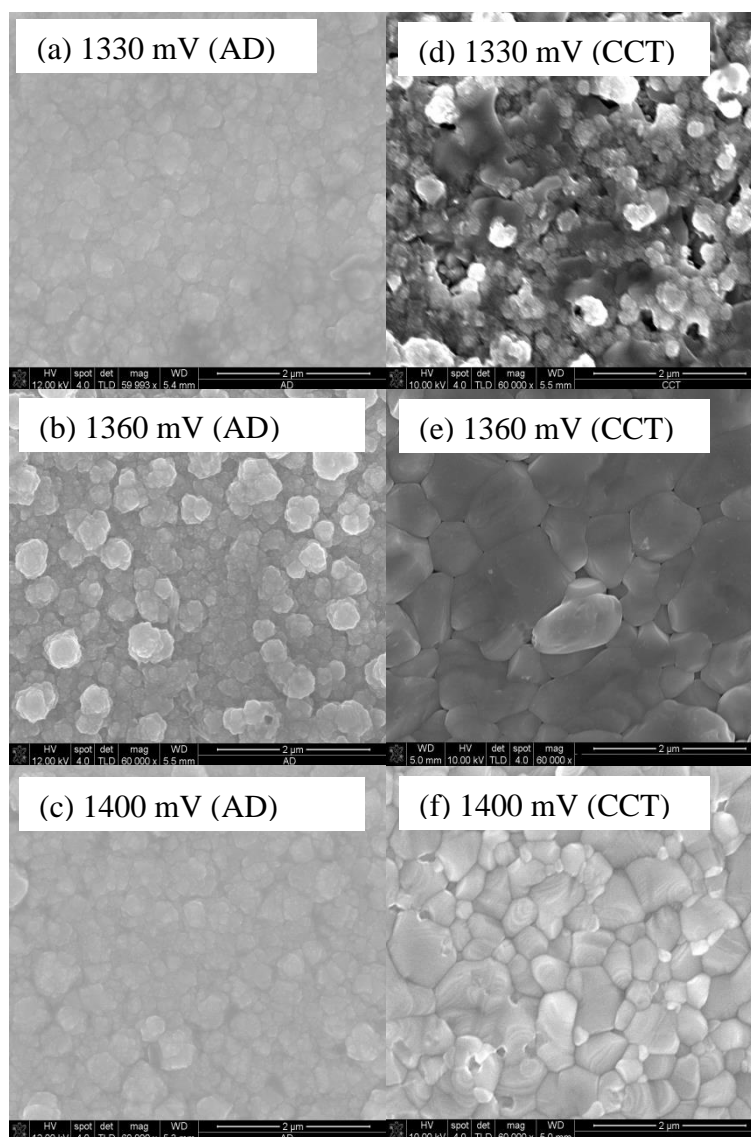
Figure 5.25: SEM micrographs for CdTe layers grown at 1330 mV, 1360 mV and 1400 mV (a-c) for as-deposited and (d-f) for $CdCl_2$ treated layers at 400°C for 20 minutes in air.

From topological observation, all the as-deposited CdTe layers show full coverage of the glass/FTO layer. The as-deposited CdTe layers show clear agglomeration of small crystallites forming into cauliflower-like clusters. After $CdCl_2$ treatment, larger crystals were formed through recrystallization, coalescence of grains [106]. The presence of

gaps was observable after CdCl$_2$ treatment in all the layers. For CdCl$_2$ treated CdTe layer grown at 1330 mV as shown in Figure 5.25 (d), high density of pinholes was observed. This might be due to the Te-richness, as a result of the deviation from stoichiometric value and properties as explained by Dharmadasa et al. [106]. The Cd-rich CdTe layer grown at 1400 mV shows less detrimental effect asides few pinholes along the grain boundaries. The major problem with the presence of pin-hole in between grain boundary is shunting due to contact between the back metal contact and the underlying substrate in solar cell structures. In comparison, larger grains are observed after CdCl$_2$ treatment for the layer grown at 1360 mV. The layers grown at 1400 mV shows better coverage of the underlying substrate, although the observed grains were smaller as compared to the layers grown at 1360 mV.

It should be noted that based on new material and device understanding in CdS/CdTe-based solar cells, the richness of Cd in CdTe layer has been demonstrated as more advantageous in high-efficiency device fabrication [208–211] as compared to Te-rich CdTe absorber layer.

Figure 5.26 shows the compositional analysis of as-deposited and CdCl$_2$ treated CdTe layers using EDX. As observed in Figure 5.26, both the as-deposited and CdCl$_2$ treated CdTe layers display Te-richness at a cathodic voltage lower than 1360 mV while CdTe layers grown at 1360 and above are rich in Cd.
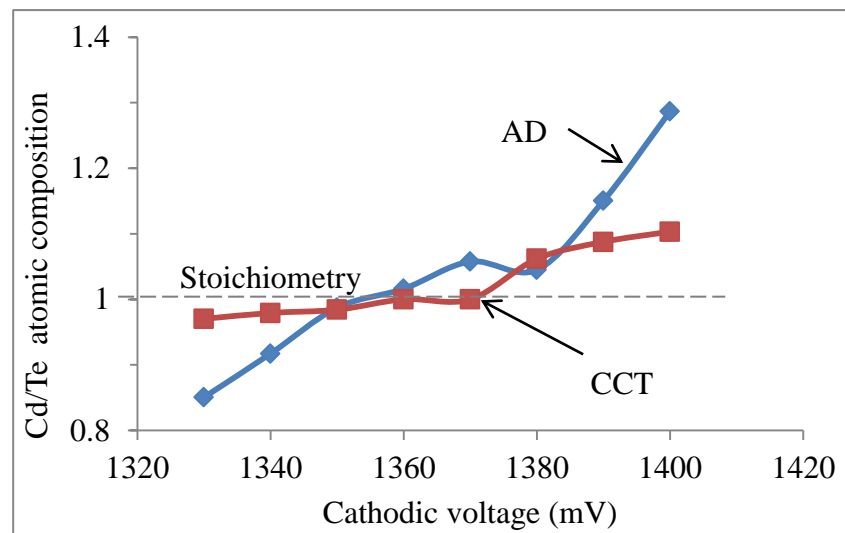
Figure 5.26: Graphical representation of Cd/Te atomic composition in as-deposited and CdCl$_2$ treated CdTe thin films at different deposition cathodic voltages.

Stoichiometric CdTe was observed at ~1360 mV for both the as-deposited and the CdCl$_2$ treated layers with the Cd/Te atomic ratio equal to 1.01. After CdCl$_2$ treatment, a shift in the atomic composition ratio towards stoichiometry was observed. This might be due to the reaction between unreacted Te with Cd from CdCl$_2$ and the sublimation of excess elemental Cd and Te from the layer. This result is in accord with the observations in Section 3.2.6.

Photoelectrochemical (PEC) Cell Study

Figure 5.27 shows the PEC cell measurement results for CdTe layers grown at cathodic voltages between 1330 mV and 1480 mV in both the as-deposited and CdCl$_2$ treated CdTe samples. Prior to the commencement of this experiment, the PEC cell was calibrated using a known *n*-type CdS layer. For the as-deposited CdTe layers shown in Figure 5.27, cathodic voltages lower than 1360 mV shows *p*-type electrical conductivity, while layers grown at 1360 mV cathodic voltage and above were *n*-type in electrical conduction. This is due to the Te-richness in the CdTe layers at lower growth voltages and Cd-richness in CdTe grown at higher cathodic voltages. This observation can be related to the redox potential of both Cd and Te, and also on the cyclic voltammetric study as explained in Section 3.1. It can be deduced that stoichiometric or near-stoichiometric CdTe can be achieved at the cathodic voltage between *n*- and *p*-CdTe layer where the atomic ratio of Cd to Te is at 50:50. This observation is in line with the high crystallinity level observed at 1360 mV in Section 3.2.1. The presence of only one phase (CdTe) at this voltage increases the crystallinity of the layer.

After CdCl$_2$ treatment, a shift in the PEC signal towards the *p*-type region was observed across the cathodic range explored. It should be noted that conductivity type change after CdCl$_2$ treatment could depend on factors such as; the heat treatment temperature, duration of treatment, initial atomic composition of Cd and Te, the concentration of CdCl$_2$ utilised in treatment, defect structure present in the starting material, and the material's initial conductivity type as documented in the literature [152,157,170,180]. It was interesting to see that CdTe layers grown at 1450 mV and above still retain their initial *n*-type conductivity after CdCl$_2$ treatment.
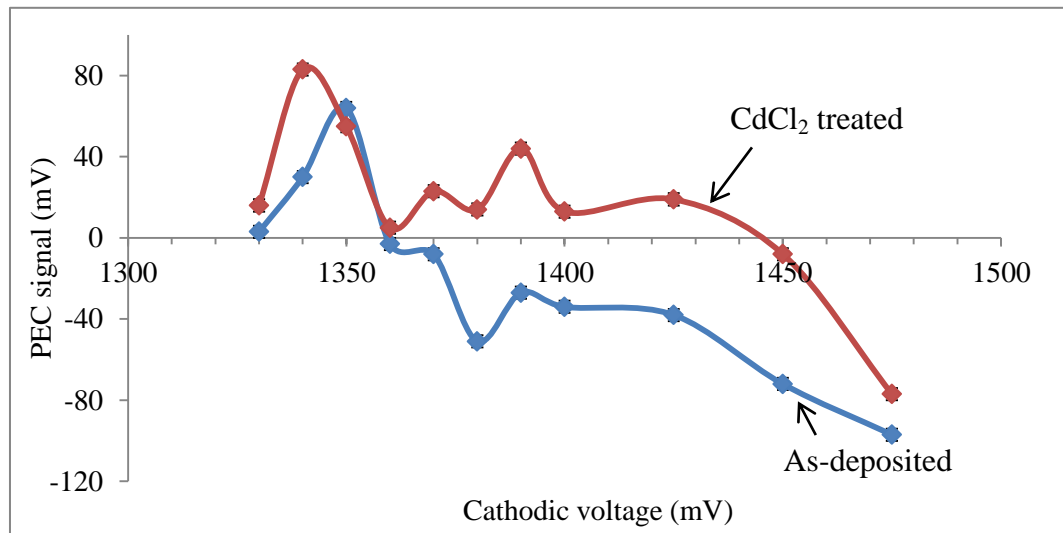
Figure 5.27: PEC signals for layers grown at different cathodic voltages between 1330 mV and 1480 mV for both as-deposited and CdCl$_2$ treated CdTe layers.

This observation is crucial to moving towards an understanding of CdCl$_2$ treatment. It is clear that composition change is one of the factors determining the electrical conductivity of CdTe layers. Te-richness produces p-CdTe while Cd-richness produces n-CdTe. The addition of Cl into CdTe is a complex issue. Substitution of Cl into Te sites makes the material n-type by acting like a shallow donor [109]. However, there is experimental evidence for the formation of a defect level at 1.39 eV below the conduction band during CdCl$_2$ treatment [183]. This shows that during the CdCl$_2$ treatment, acceptor-like defects are also formed closer to the top of the valence band, and this leads to the formation of p-type doping of CdTe. One explanation could be that Cl forms a complex with a currently unknown native defect. Therefore, Cl seems to act as an amphoteric dopant in CdTe.

In addition to the above doping effect, self-compensation can take place during heat treatment in the presence of CdCl$_2$ due to the existence of numerous native defects in the material. Therefore, the final electrical conductivity depends on the most dominant process taking place during this treatment.

The experimental evidence in Figure 5.27 shows the real situation; (i) in as-deposited layers Te-richness produces p-CdTe, and Cd-richness produces n-CdTe (ii) CdCl$_2$ treatment tends to change the material from n-properties towards p-properties. In other words, the Fermi level (FL) moves from the upper half towards the lower half of the bandgap. The tendency of the FL crossing the mid-point depends on the initial nature of the material layer. If the Cd-richness is dominant in the layers, the FL remains in the

upper half of the bandgap keeping the material *n*-type in electrical conductivity. In this discussion, effects of external impurities have been neglected. If an external impurity with dominant doping is introduced in the CdTe layer, the above analogy can be changed.

DC Resistivity

The DC resistivity experiment was performed on CdTe layers grown between the cathodic voltage of 1330 mV and 1400 mV. The CdTe layers were grown for 120 minutes each. 2 mm diameter of 100 nm thick gold contacts were evaporated at a low pressure of 10^{-5} Nm^{-2} on the *p*-type CdTe layer for both the as-deposited and $CdCl_2$ treated CdTe layers (glass/FTO/*p*-CdTe/Au), while 100 nm thick indium contacts were evaporated at a low pressure of 10^{-5} Nm^{-2} on the *n*-CdTe layers for both the as-deposited and $CdCl_2$ treated CdTe layers (glass/FTO/*n*-CdTe/In) to achieve Ohmic contacts for the metal/semiconductor interfaces [212,213].
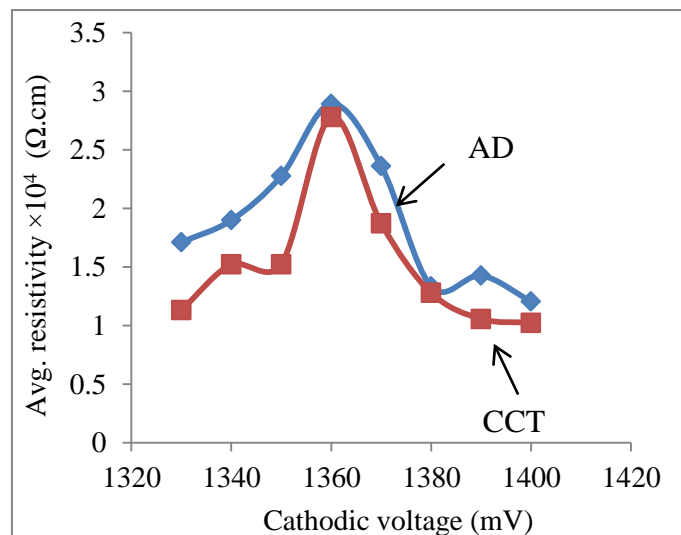
Figure 5.28: Typical graphs of electrical resistivity against cathodic voltage for CdTe layer grown within the cathodic voltages between 1330 mV and 1400 mV in both as-deposited and $CdCl_2$ treated conditions.

The electrical resistivity (ρ) of the layers was calculated using Equation 3.19, where *R* is the electrical resistance, *A* is the contact area, and *L* is the film thickness. The average electrical resistance (R) was calculated using the I-V data extracted under dark condition using the Rera Solution PV simulation system.

Figure 5.28 shows the plot of electrical resistivity (ρ) against the cathodic voltage in which the CdTe layers were grown. From observation in Figure 5.28, the resistivity of

CdTe layers reduces after CdCl$_2$ treatment which might be due to defect and grain boundary passivation, reduction of grain boundaries due to grain growth during CdCl$_2$ treatment, increase in CdTe crystallinity amongst other advantages of CdCl$_2$ treatment as documented in the literature [30,157].

Both the as-deposited and CdCl$_2$ treated CdTe layers grown at ~1360 mV cathodic voltage exhibit the high resistivity value. This is expected since the CdTe is stoichiometric and intrinsic in electrical conduction. The material grown at 1360 mV should, therefore, have the highest resistivity. However, cathodic voltages closer to the intrinsic voltage (V_i) would be favourable for the fabrication of devices due to high crystallinity, better optical and morphological properties achieved in stoichiometric or near-stoichiometric CdTe layers. It should be noted that based on the understanding as published by Dharmadasa et al (2002) [15,208,214] and new results as published by independent researchers such as Reese et al (2015) [210] and Burst et al (2016) [209], fabricating devices with slightly Cd-rich CdTe is favourable due to increased carrier lifetime and defect reduction amongst other advantages.

Summations

In this work, CdTe layers were successfully electrodeposited using a two-electrode configuration from an acidic and aqueous solution containing cadmium chloride hydrate CdCl$_2$·xH$_2$O and tellurium oxide TeO$_2$ as Cd and Te precursors respectively. XRD analysis shows cubic (111) CdTe diffraction as the preferred orientation of all the CdTe explored in this work, while, the highest diffraction intensity was observed at 1360 mV under both as-deposited and CdCl$_2$ treated conditions. After CdCl$_2$ treatment, an improvement in the absorption edge slope was observed with the highest slope signifying highest CdTe quality [30,215]. This was observed at 1360 mV. Morphologically, better glass/FTO substrate coverage was observed for Cd-rich CdTe layer grown at 1400 mV while Te-rich layer grown at 1330 mV show high pinhole density. The best underlying substrate coverage, grain growth, and size were observed at 1360 mV. PEC measurements show the ability to electroplate both *n*-, i- and *p*-type CdTe layers using precursors explored in this work.

5.6.3   Effect of I-doping on the material properties of CdTe

The motivation for the exploration of I-doping of CdTe is based on the new model as put forward by Dharmadasa and co-workers in 2002 [15,52]. This understanding associated Te richness in CdTe with defect levels close to the conduction band, while

Cd richness in CdTe is associated with defect levels close to the valence band from which higher barrier height can be achieved. Although Cd-rich CdTe can be achieved intrinsically, this work focuses on the optimisation of extrinsic iodine doping of CdTe since it is the best atomic replacement for Te atoms with minimal deformation to the CdTe lattice.

5.6.3.1   Growth of I-doped CdTe layers

CdTe:I thin films were electrodeposited cathodically on glass/FTO substrates by a potentiostatic technique in which the anode was a high purity graphite rod (see Section 3.3). The main difference to the CdTe bath as described in Section 5.3 is the incorporation of the varied concentration of cadmium iodide (CdI_2) between 0 ppm to 200 ppm with a purity of 99.995% to different CdTe baths containing same measured salts of Cd and Te precursors. The setup and substrate preparation remains identical to the CdTe bath as described in Section 5.3. All the CdTe:I layers explored were grown at 1370 mV based on prior analysis as demonstrated in Section 5.3.

5.6.3.2   Material properties of CdTe:I

Structural analysis

Figure 5.29 (a), Figure 5.29 (b), and Figure 5.29(c) shows the X-ray diffraction (XRD) spectra of CdTe:I layer under the AD, CCT and $CdCl_2+Ga_2(SO_4)_3$ treatment (GCT) conditions grown from electrolytic baths containing different I-concentration respectively. Figure (d) shows the CdTe (111) peak intensity at different post-growth treatment against I-doping concentration in the CdTe electrolytic bath. The GCT was performed by adding few drops of aqueous solution containing 0.1 M $CdCl_2$ and 0.05 M of $Ga_2(SO_4)_3$ in 20 ml of DI water to the surface of the semiconductor layer. The full coverage of the layers with the treatment solutions was achieved by spreading the solution using solution-damped cotton bud. The semiconductor layer was allowed to air-dry and heat treated at 400°C for 20 minutes.

From observation, diffraction peaks associated with CdTe (111), (220) and (311) all in the cubic phase were observed asides from the diffractions associated with the glass/FTO underlying substrates. It should be noted that the extracted XRD data from this CdTe:I work matches the Joint Committee on Powder Diffraction Standards (JCPDS) reference file number 01-075- 2086 on cubic CdTe layers. From the observations in Figure 5.29 (a), Figure 5.29 (b) and Figure 5.29 (c), no diffraction

associated with elemental Iodine or Iodine related compounds were observed in all of the explored XRD layers, which might be due to the low concentrations investigated and the sensitivity of the XRD technique utilised in this work.
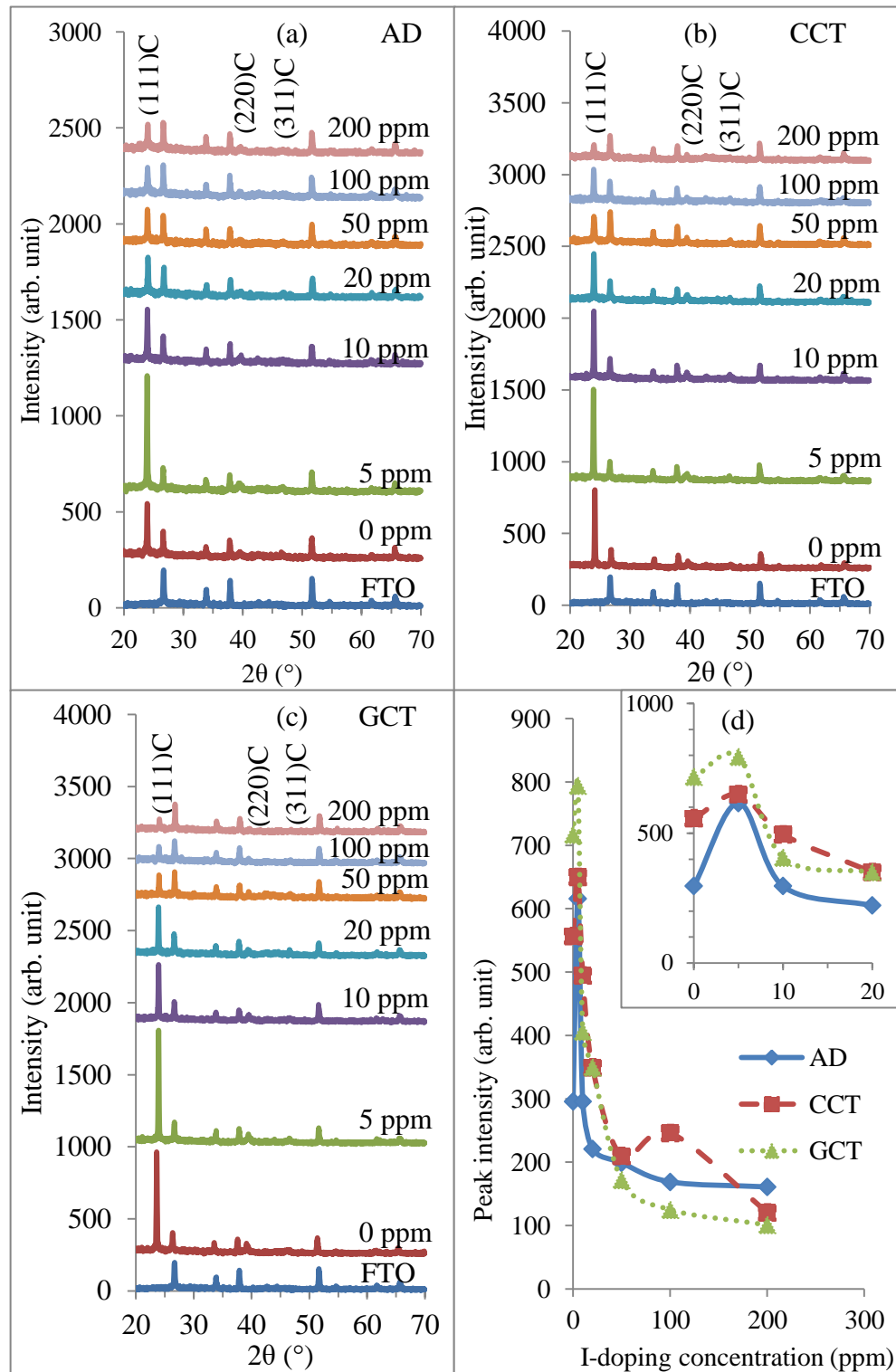
Figure 5.29: Typical XRD patterns of CdTe:I grown with different iodine doping concentration for (a) AD (b) CCT and (c) GCT, while (d) is the graph of (111) CdTe peak intensity against I doping concentration.

Under all treatment conditions, the CdTe (111) diffraction shows the highest diffraction intensity which is synonymous with the preferred orientation of CdTe:I layer under the growth conditions of this study. Comparative improvement in the CdTe:I layers was observed after CCT or GCT as shown by higher (111)C CdTe XRD intensity as compared to the AD CdTe:I layers. This observation can be attributed to Cd/Te stoichiometric improvement by sublimation of excess element or the formation of CdTe from excess elements [30]. As shown in Figure 5.29 (a), Figure 5.29 (b) and Figure 5.29 (c), under AD, CCT and GCT conditions an initial increase in the (111) cubic CdTe diffraction intensity was observed from 0 ppm to 5 ppm I-doping which signifies an improvement in the CdTe:I crystallinity, while a gradual decline in the diffraction intensity of CdTe:I was observed at I-doping concentration at 10 ppm and above as clearly shown by Figure 5.29 (d). The observed reduction in X-ray diffraction intensity of the (111)C peak at 10 ppm I-doping and above might be due to the formation of CdI_2 complexes such as CdI^+, CdI_2, CdI_3^- and CdI_4^{2-} in aqueous solution [216], which were not effective in non-aqueous electrolytic deposition of CdTe incorporating iodine [196]. The complexes CdI_2 formed hinder the deposition of Cd^{2+} ions on the surface of the working electrode and also the reduces the available Cd^{2+} with increasing CdI_2 concentration as suggested by Paterson et al. [216,217].
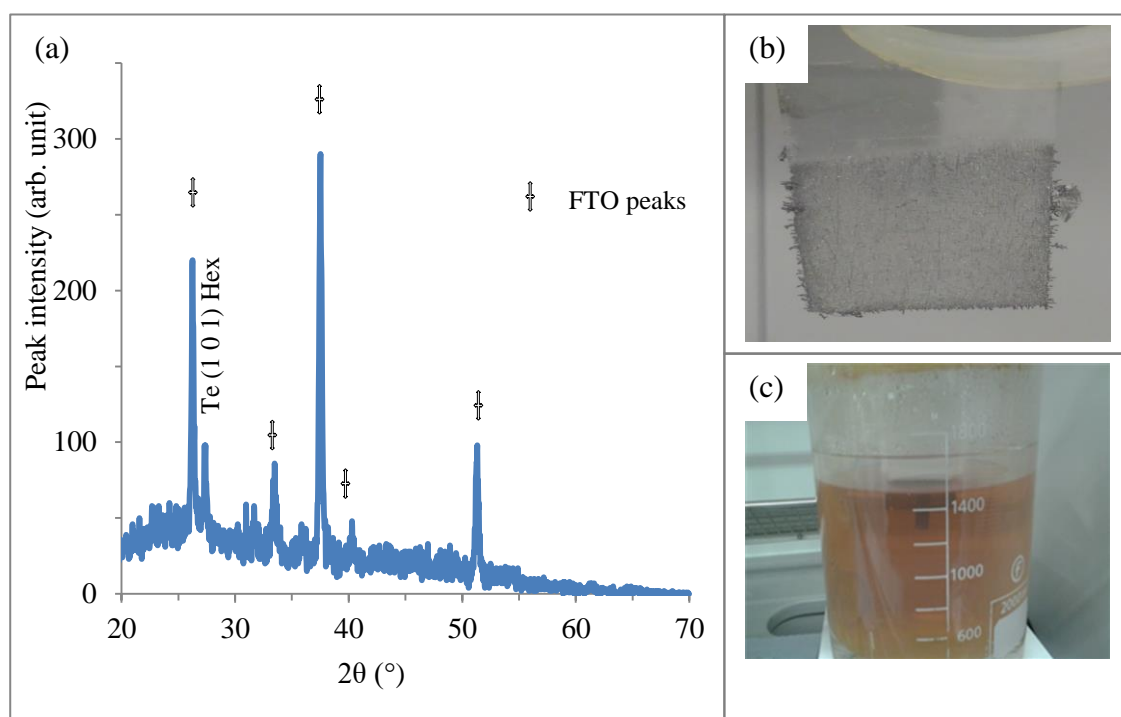
Figure 5.30: (a) Typical XRD pattern of Te grown at 1000 ppm I-doping of CdTe, (b) deposited Te layer and (c) unstable CdTe bath with 1000 ppm I-doping.

The explored I-doping concentration range was limited to 200 ppm due to further reduction in the cubic (111) CdTe intensity (without recrystallisation) and total elimination at ~1000 ppm with the appearance of the emergence of the hexagonal (101) Te peak as shown in Figure 5.30 (a), while the deposited layers are characterised with low adhesion as shown in Figure 5.30 (b). Figure 5.30 (c) depicts the colouration of the electrolyte due to the instability of the electrolytic bath. This observation signifies the non-deposition of Cd on the glass/FTO substrate at high I-doping concentration.

Table 5.9: Shows the X-ray diffraction analysis for cubic (111) CdTe diffraction.

AD				
Doping (ppm)	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)
0	23.92	3.71	0.1298	65.4
5	23.91	3.71	0.1298	65.4
10	23.97	3.70	0.1298	65.4
20	23.98	3.70	0.1298	65.4
50	23.97	3.70	0.1624	52.3
100	24.06	3.69	0.1624	52.3
200	24.03	3.69	0.1624	52.3
CCT				
Doping (ppm)	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)
0	23.94	3.71	0.1298	65.4
5	24.11	3.68	0.1298	65.4
10	23.89	3.72	0.1623	52.3
20	23.95	3.71	0.1623	52.3
50	23.94	3.71	0.1624	52.3
100	23.95	3.71	0.1623	52.3
200	23.95	3.71	0.2597	32.7
GCT				
Doping (ppm)	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)
0	23.9	3.72	0.1298	65.4
5	23.99	3.70	0.1298	65.4
10	24.07	3.69	0.1298	65.4
20	23.6	3.76	0.1623	52.3
50	23.92	3.71	0.1623	52.3
100	23.98	3.70	0.1623	52.3
200	23.92	3.71	0.1623	52.3

Table 5.9 shows the cubic (111) CdTe X-ray diffraction analysis for the AD, CCT, and GCT CdTe:I layers. The crystallite sizes were calculated using Scherrer's equation as

shown in Equation 3.8. For the as-deposited CdTe:I layer as shown in Table 5.9, a gradual reduction in the d-spacing was observed with increase in I-doping concentrations, while samples with a concentration above 100 ppm exhibit significant alteration in the d-spacing. This observation iterates the presence of tensile stress in the crystal plane due to the inclusion of I. Under AD conditions, a constant crystallite size of 65.38 nm was observed for CdTe:I doped layers with I-doping concentration ranging between 0 ppm and 20 ppm. Above this range, the crystallite size was reduced to ~52.26 nm. Similar trends of reduction in the crystallite sizes were observed under the CCT above 5 ppm I-doping and GCT above 10 ppm I-doping concentration. Alteration in crystallite stress distribution, compositional configuration, oxidation and grain growth amongst other factors may drastically affect the crystallite parameters as observed in Table 5.9. It should be noted that the stagnated crystallite sizes at 65.38 nm and 52.26 nm might be due to the limitation of the use of the Scherrer's equation for materials with larger grains as well as the XRD machine [115,218].

Optical properties analysis

The optical absorbance measurement of the CdTe:I under AD, CCT and GCT conditions were performed at room temperature. The bandgap of the CdTe:I layers was determined using the graphical plot of A^2 against photon energy (hv). Figure 5.31 (a), Figure 5.31 (b) and Figure 5.31 (c) show A^2 against hv plot of the AD, CCT, and GCT CdTe:I at different I-doping concentrations respectively. Figure 5.31 (d) shows a graph of absorption edge slope against I-doping concentrations of CdTe baths and Table 5.10 shows the optical absorption properties of the CdTe:I layer under all the conditions explored in this work. From observation, the bandgap for the explored I-doping concentration from 0 ppm to 200 ppm falls within the range of 1.52±0.05 eV for the AD CdTe:I layer with an increase in the I-doping concentration resulting into increase in the bandgap. For both the CCT and GCT layers falls within the bandgap range of 1.48±0.01 eV and 1.47±0.02 eV respectively. The improvement towards the acceptable CdTe bandgap range of (1.44 to 1.50) eV [219] and the narrowing of the bandgap range is due to the enhancement of material properties such as grain growth, crystallinity, and sublimation of excess element [30,39,160] amongst others.

Furthermore, the optical absorption edge slope which is a quantitative measure of defect and impurity energy levels [30,215] was explored as a function of I-doping concentration as shown in Figure 5.31 (d). Under all the post-growth treatment

conditions investigated in this work, the highest absorption edge slope was observed at 5 ppm I-doping concentration. This comparatively signifies that more incident photons can be absorbed in few nanometer of CdTe:I thickness and also the increased possibility of achieving higher solar to electricity conversion efficiency when incorporated in solar cell structures.
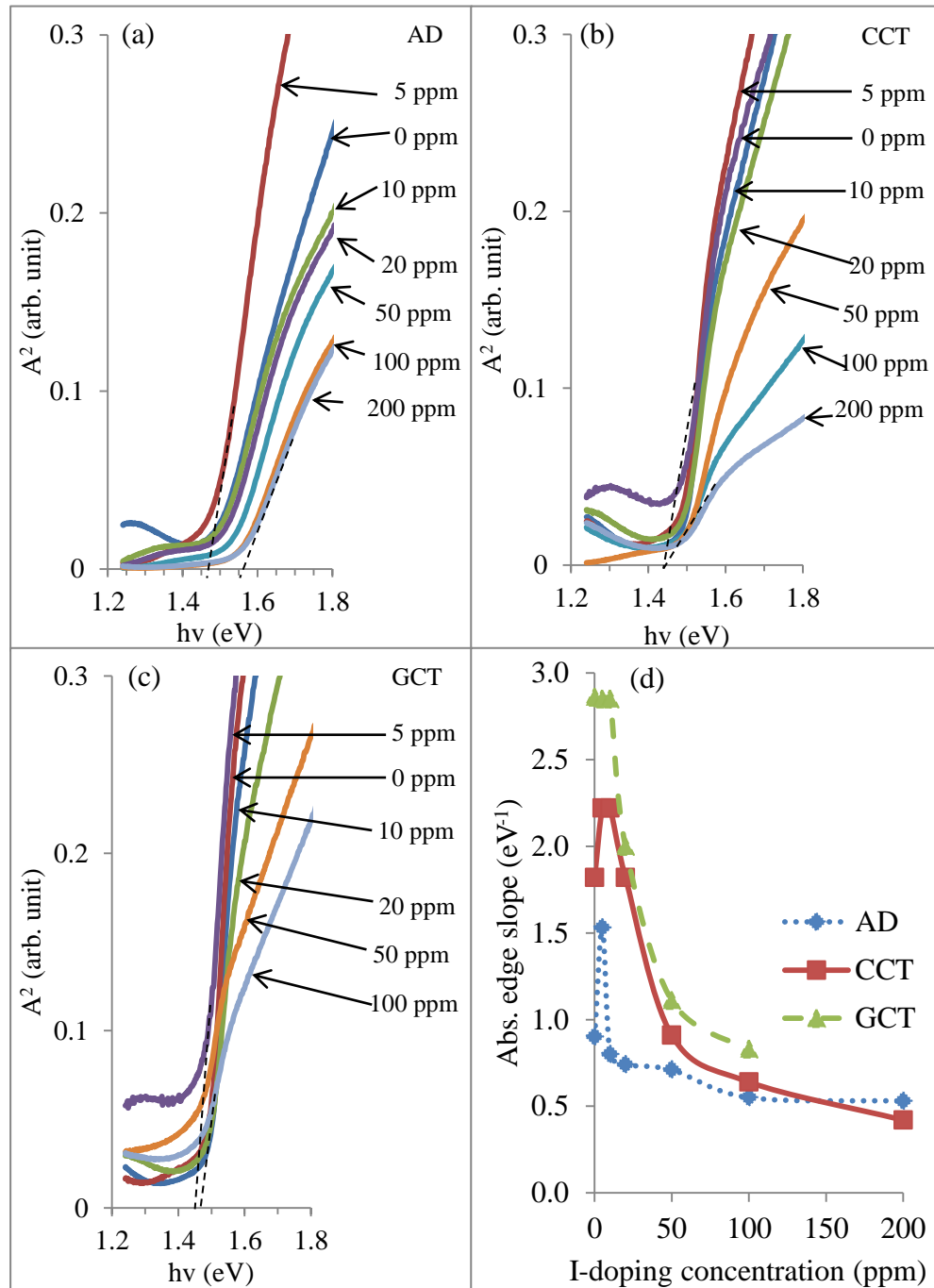
Figure 5.31: Optical absorption of CdTe:I with different doping concentrations of iodine under (a) AD, (b) CCT and (c) GCT conditions, while (d) is the absorption edge slope of CdTe:I under AD, CCT and GCT conditions against I-doping concentration.

Table 5.10: The optical bandgap and slope of absorption edge of CdTe layers grown from different CdTe baths with different I-doping concentration having undergone different post-growth treatments.

I-doping (ppm)	Bandgap (eV)			Abs. edge slope (eV^{-1})		
	AD	CCT	GCT	AD	CCT	GCT
0	1.47	1.47	1.46	0.90	1.82	2.86
5	1.47	1.48	1.49	1.53	2.22	2.85
10	1.49	1.49	1.49	0.80	2.22	2.85
20	1.50	1.49	1.48	0.74	1.82	2.00
50	1.53	1.49	1.45	0.71	0.91	1.11
100	1.55	1.49	1.45	0.55	0.64	0.83
200	1.56	1.49		0.53	0.42	

Morphological property analysis

Figure 5.32 shows the SEM micrographs of CdTe:I incorporating (a) 5 ppm I-doping under CCT and (b) under GCT, while (c) incorporating 100 ppm I-doping under CCT and (d) under GCT. The as-deposited CdTe:I and 0 ppm I-doped CdTe layers were not incorporated due to its triviality.
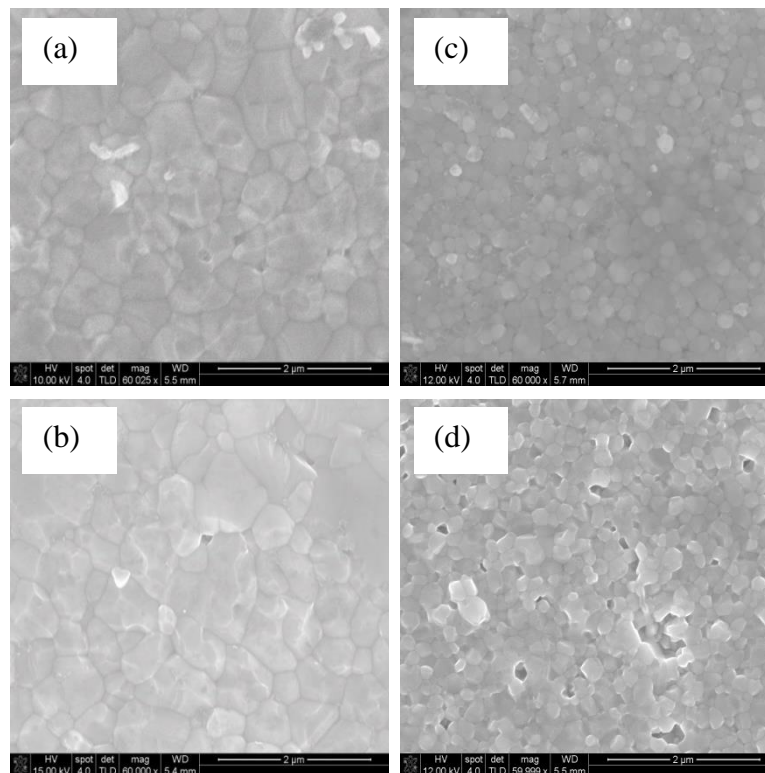
Figure 5.32: Typical SEM micrographs of CdTe:I (a) incorporating 5 ppm I-doping under CCT and (b) under GCT, while (c) incorporating 100 ppm I-doping under CCT and (d) under GCT.

In accord with the effect of CCT and GCT as documented in the literature, grain growths were observable as compared to the as-deposited CdTe:I layers. Comparatively, a reduction in the grain size was observed above 5 ppm I-doping of the CdTe bath which may be due to competing phases of CdI_2 complexes in aqueous solution as suggested in the literature [216,217]. This observation is corroborative with the structural and optical analytical observations.

Photoelectrochemical (PEC) cell measurement

Figure 5.33 shows the graph of PEC cell measurement against varying I-doping concentration from 0 ppm to 200 ppm in the CdTe:I bath. From observation, all the as-deposited CdTe:I layer at all the explored I-doping concentrations show *n*-type conductivity as it is well known that iodine along with other halogens is a known donor to CdTe due to the introduction of excess electrons into the conduction band [220]. For both the CCT and GCT treated CdTe:I layers, the initial *n*-type conductivity was retained from the as-deposited CdTe:I for layers between 0 ppm and 10 ppm I-doping concentration while the transition to *p*-type conductivity was observed above 10 ppm I-doping concentration. It should be noted that the conduction type of a semiconductor material depends on the domination of factors such as elemental composition, doping alteration due to annealing parameters, defect distribution amongst others [180,221].
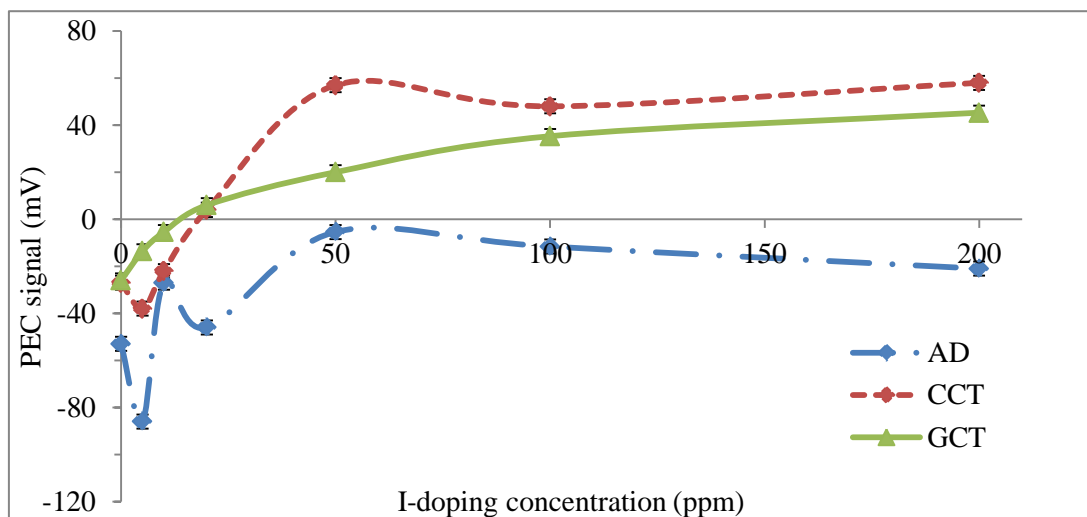
Figure 5.33: Photoelectrochemical cell measurement for AD, CCT and GCT CdTe:I layers.

DC properties analysis

The formation of Ohmic contacts with the CdTe:I was dependent on the conductivity type of the layers as discussed in the PEC section. Au was evaporated on *p*-type layers,

while In was evaporated on *n*-type layers. Figure 5.34 shows the graph of electrical conductivity against I-doping concentration in the CdTe bath. Relatively, a continuous reduction in the conductivity of the deposited layers with increasing I-doping concentration was observed with the exception of the CdTe:I layer grown at 5 ppm I-doping. This observation signifies a possible solubility of CdTe:I at 5 ppm in aqueous solution. Other factors to be considered for this trend includes the comparatively higher mobility and the conductivity of *n*-type semiconductors relative to their *p*-type counterpart as documented in the literature [222] and the possible effect of formation of complexes in aqueous solution [216,217].
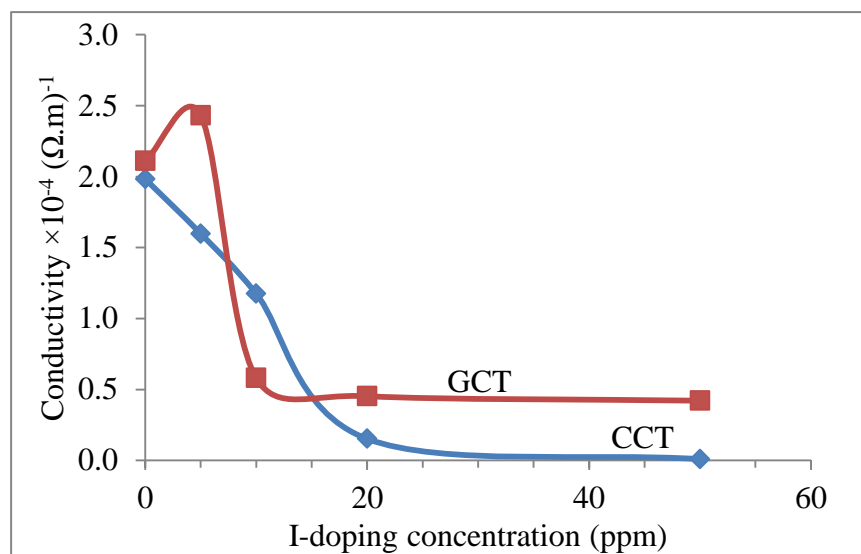
Figure 5.34: Graph of electrical conductivity against I-doping concentration in CdTe bath.

Summations

In this work, the effect of iodine doping in a CdTe electrolytic bath on the CdTe layer as it affects its structural, optical, morphological and compositional properties were explored. An optimal I-doping concentration of 5 ppm in the electrolytic bath was observed under all material characterisations explored in this work due to the possible solubility limit achieved at 5 ppm I-doping and deterioration in material property afterwards which is contrary to the improvement of material and electronic properties as documented in the literature for electrodeposited CdTe:I in non aqueous electrolytes [196].

5.6.4   Effect of Ga-doping on the material properties of CdTe

The motivation for the in-situ incorporation of Ga in CdTe is based on the possibility of the reduction of Te precipitation as demonstrated by the literature after post-growth treatment [181,192]. This has also been demonstrated by in the presence of Cd [192] and Cl [193] in the literature to reduce the Te precipitation [44]. Therefore, the effect of in-situ Ga-doping with different Ga-doping concentrations of CdTe:Ga will be explored.

5.6.4.1   Growth of Ga-doped CdTe layers

CdTe:Ga thin films were electrodeposited cathodically on glass/FTO substrates by a potentiostatic technique in which the anode was a high purity graphite rod (see Section 3.3). The main difference to the CdTe bath as described in Section 5.3 is the incorporation of varied concentration from 0 ppm to 200 ppm of gallium sulphate ($Ga_2(SO_4)_3$) with a purity of 99.99% to different CdTe baths containing the same measured salts of Cd and Te precursors. The setup and substrate preparation remains identical to the CdTe bath as described in Section 5.3. All the CdTe:Ga layers explored were grown at 1370 mV based on prior analysis as demonstrated in Section 5.3.

5.6.4.2   Material properties of CdTe:Ga

Structural analysis

The structural analysis was performed to determine the optimal Ga-doping concentration in the CdTe bath. This can be determined by observing the highest peak intensity, crystallinity, and crystallite size. Figure 5.35 (a), Figure 5.35 (b) and Figure 5.35 (c) show the X-ray diffraction (XRD) measured between $2\theta=20°$ and $2\theta=70°$ for CdTe layers doped with Ga between 0 ppm and 200 ppm under the AD, CCT and GCT conditions. Figure 5.35 (d) shows the cubic (111) CdTe XRD diffraction intensity of CdTe grown from CdTe bath containing different concentrations of Ga-doping ranging from 0 ppm to 200 ppm. Asides from the XRD diffraction associated with glass/FTO at ~26.64°, ~33.77°, ~37.85°, ~51.64° and ~65.62° 2θ angle, CdTe peaks associated with (111) cubic, (220) cubic and (311) cubic were observed at $2\theta\approx23.95°$, $2\theta\approx38.60°$ and $2\theta\approx45.80°$ respectively. From observation, the most intense diffraction, which signifies the preferred orientation of CdTe growth was observed at $2\theta\approx23.95°$ for all the post-growth treatment conditions explored in this work. Similarly, a gradual increase in the diffraction intensity was observed with increasing Ga-doping from 0 ppm to 20 ppm as shown in Figure 5.35 (a), Figure 5.35(b), Figure 5.35 (c) and Figure 5.35 (d). This observation can be associated with an increase in crystallinity of CdTe along the (111)C

plane due to the reduction and dissolution of Te precipitation [181] and the incorporation of Ga as a substitutional dopant. An increase in the doping of Ga above 20 ppm results in a reduction in diffraction intensity of the CdTe (111)C and a total collapse of the peak at 200 ppm Ga-doping and above.
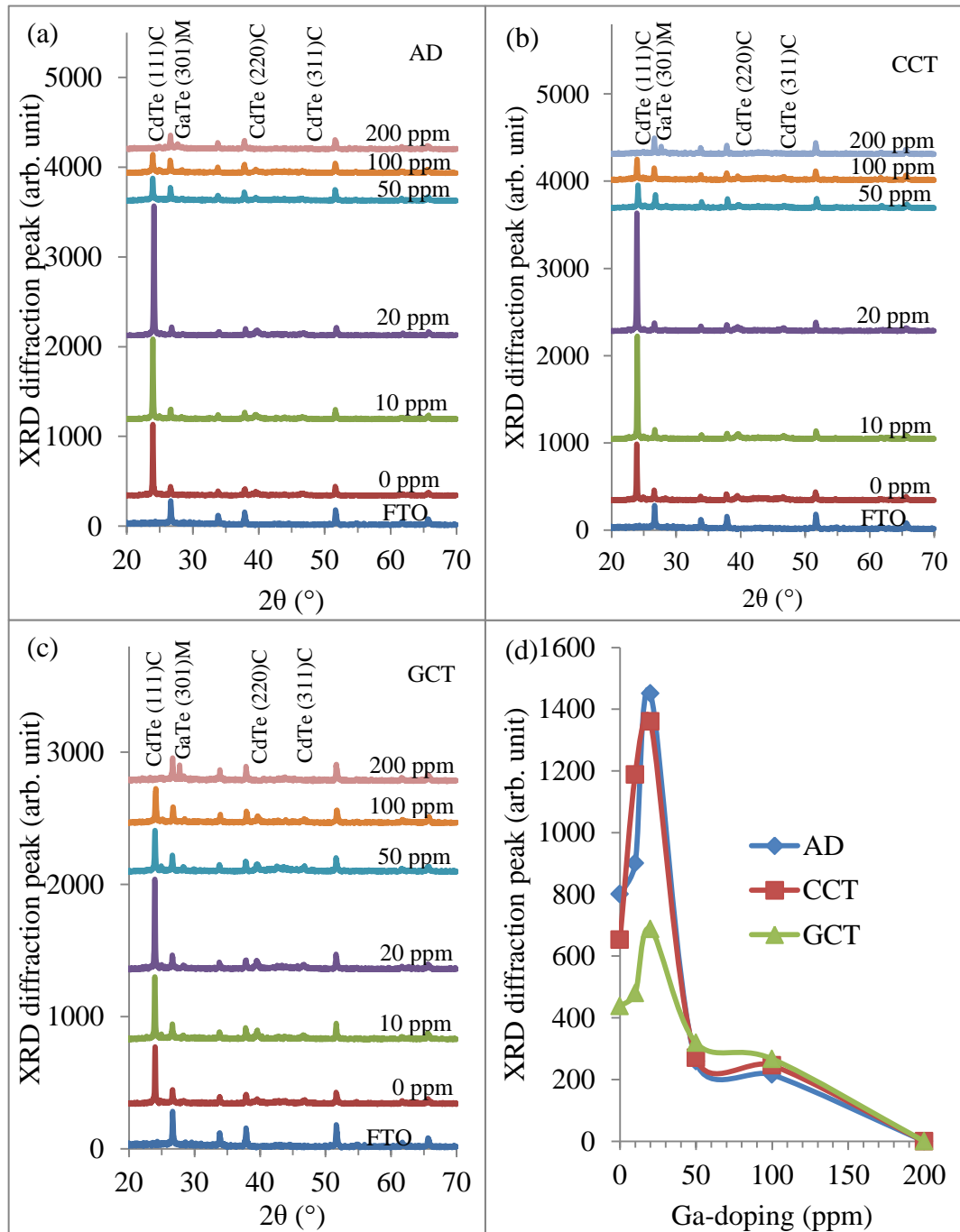
Figure 5.35: Typical XRD patterns of CdTe at different galium doping concentrations for (a) AD (b) CCT and (c) GCT-CdTe layers. (d) is a typical plot of CdTe:Ga (111) cubic peak intensity against Ga-doping of CdTe baths.

Subsequently, an emergence of a GaTe diffraction peak was observable above 20 ppm Ga-doping under all the conditions explored in this work. Furthermore, an increase in the GaTe peak intensity at $2\theta \approx 27.23°$ was noticeable with increasing Ga concentration. It should be noted that the reduction of CdTe (111)C diffraction intensity above 20 ppm Ga-doping in the CdTe bath can be attributed to competing for crystalline phases of CdTe and GaTe. Furthermore, this observation emphasises the replacement of Cd atoms with Ga atoms in the crystal lattice to form GaTe [192]. Only two valence electrons out of three available for bonding of Ga atoms were utilised in the formation of bonds with neighboring Te atoms while the excess electron is donated to the lattice to aid the *n*-type conduction (see Figure 5.36).
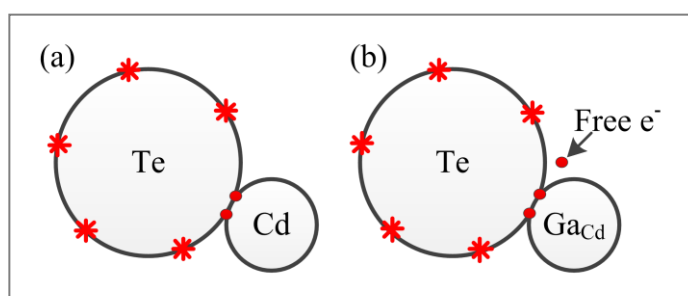
Figure 5.36: Covalent bond formation between (a) Cd and Te atoms and (b) Ga occupying Cd sites and bonding with Te as a result of surface treatment.

The extracted XRD data in this work matches the Joint Committee on Powder Diffraction Standards (JCPDS) reference file number 01-075-2086-cubic for CdTe and 01-075-2220 monoclinic for GaTe. Table 5.11 shows the XRD analysis of CdTe layers grown at different gallium concentrations. The crystallite sizes (*D*) of each of the CdTe layers at different Ga-doping was calculated using Scherrer's formula as shown in Equation 3.8.

Uniformity in both the FWHM and crystallite size was observed for the entire as-deposited CdTe layers as shown in Table 5.11. After CCT treatment of the CdTe layers, reduction in FWHM to 0.129° and resulting increase in crystallite sizes to 65.3 nm were observed for CdTe layers doped with Ga within the range of 0 ppm and 20 ppm. Subsequently, reductions in the crystallite size were observed for CdTe layers doped with Ga at 50 ppm and above. This observation is due to the reduction of crystallinity due to the formation of two phases; CdTe and GaTe. The replacement of Cd atoms which have an atomic radius of 1.61 Å with Ga atoms which has a comparatively lower

atomic radius of 1.36 Å may lead to contraction of the crystal lattice [39,204]. The same phenomenon was observed with the GCT treated CdTe:Ga layers.

Table 5.11: XRD analysis of CdTe layers grown at different Ga-doping concentrations.

AD				
Doping (ppm)	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)
0	23.95	3.712	0.162	52.3
10	23.95	3.712	0.162	52.3
20	24.12	3.688	0.162	52.3
50	23.94	3.714	0.162	52.3
100	23.95	3.712	0.162	52.3
CCT				
Doping (ppm)	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)
0	24.10	3.689	0.130	65.3
10	23.95	3.713	0.130	65.3
20	23.90	3.720	0.130	65.3
50	23.98	3.708	0.162	52.3
100	23.93	3.716	0.162	52.3
GCT				
Doping (ppm)	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)
0	23.94	3.714	0.130	65.3
10	23.99	3.707	0.162	52.3
20	23.94	3.714	0.162	52.3
50	23.96	3.710	0.162	52.3
100	24.08	3.693	0.195	43.6

Furthermore, it is appropriate to look at the stability of the two compounds; CdTe and GaTe at this stage. The stability of inorganic compounds is given by their heat of formation or the enthalpy value (ΔH) given by Equation 5.4 and Equation 5.5.

$$(\text{reactant})\,Cd + Te \rightarrow CdTe\,(\text{product}) + \Delta H \qquad \text{Equation 5.4}$$

$$(\text{reactant})\,Ga + Te \rightarrow GaTe\,(\text{product}) + \Delta H \qquad \text{Equation 5.5}$$

The product with the most significant negative value of ΔH is more stable and have a high tendency to proceed [223]. As depicted in Figure 5.37, the ΔH values of CdTe and GaTe are -50.6 kJmol^{-1} and -62.6 kJmol^{-1} [224,225] respectively, as reported in the literature. These values indicate that GaTe is more stable and therefore, as the Ga

concentration increases beyond 20 ppm, GaTe compound formation takes place within the layer. The presence of these two competing phases allows the deterioration of crystallinity and the complete collapse of the (111)C peak originating from CdTe.
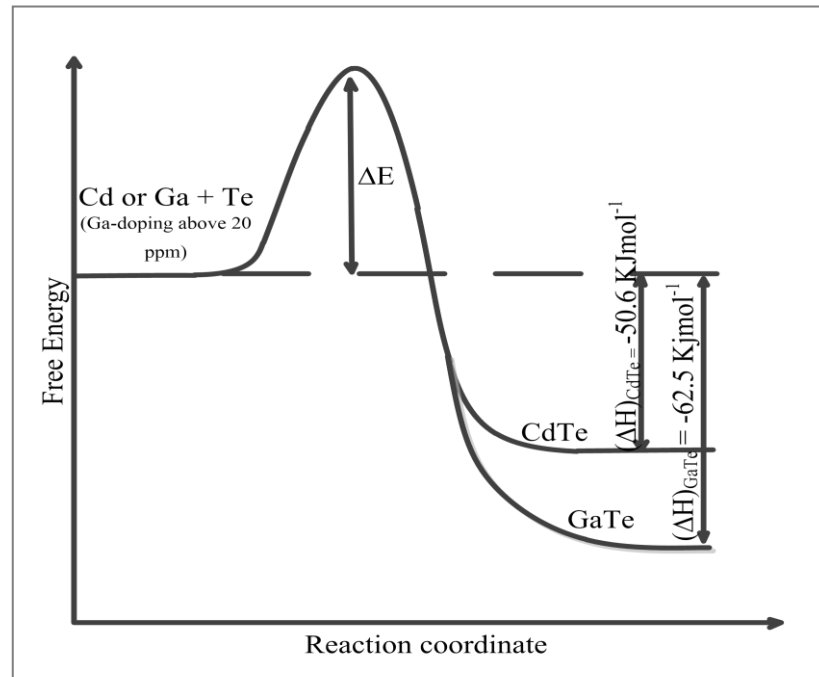
Figure 5.37: Free energy graph depicting the enthalpy ΔH_f at 298 K for both CdTe and GaTe compounds.

Optical properties analysis

Figure 5.38 (a), Figure 5.38 (b) and Figure 5.38 (c) show the optical absorption of CdTe:Ga layers under the AD, CCT, and GCT conditions respectively, while Figure 5.38 (d) shows the graph of absorption edge slope against Ga-doping concentration in CdTe bath. It should be noted that due to the removal of the effect of glass/FTO as explained in Section 3.4.6, only the absorption of the CdTe:Ga is captured. As observed in Figure 5.38 (a), Figure 5.38(b) and Figure 5.38 (c), the optical bandgaps of the entire deposited CdTe layer at varying Ga-doping concentration were within the range of 1.48±0.02 eV. This observation shows the dominance of CdTe even with the incorporation of Ga and formation of GaTe as observed in the structural analysis section. Alteration in the absorption edges of CdTe:Ga layers with varying Ga-doping concentration were also observed as shown in Figure 5.38 (d). The steepest absorption edge slope which signifies the best quality of semiconductor layer [30] was observed at a Ga-doping of 20 ppm, 10 ppm and 0 ppm under the AD, CCT and GCT conditions respectively (Figure 5.38 (d)). As reported in the literature, increase in steepness of the

semiconductor materials absorption edge signifies lesser defects and impurity energy levels in the thin film [125]. Furthermore, a sharp absorption edge also allows more photons to be absorbed even at low CdTe thickness of few a microns [30]. This optical result, therefore, shows the possibility of having better solar cell efficiency using 20 ppm gallium doped CdTe:Ga.
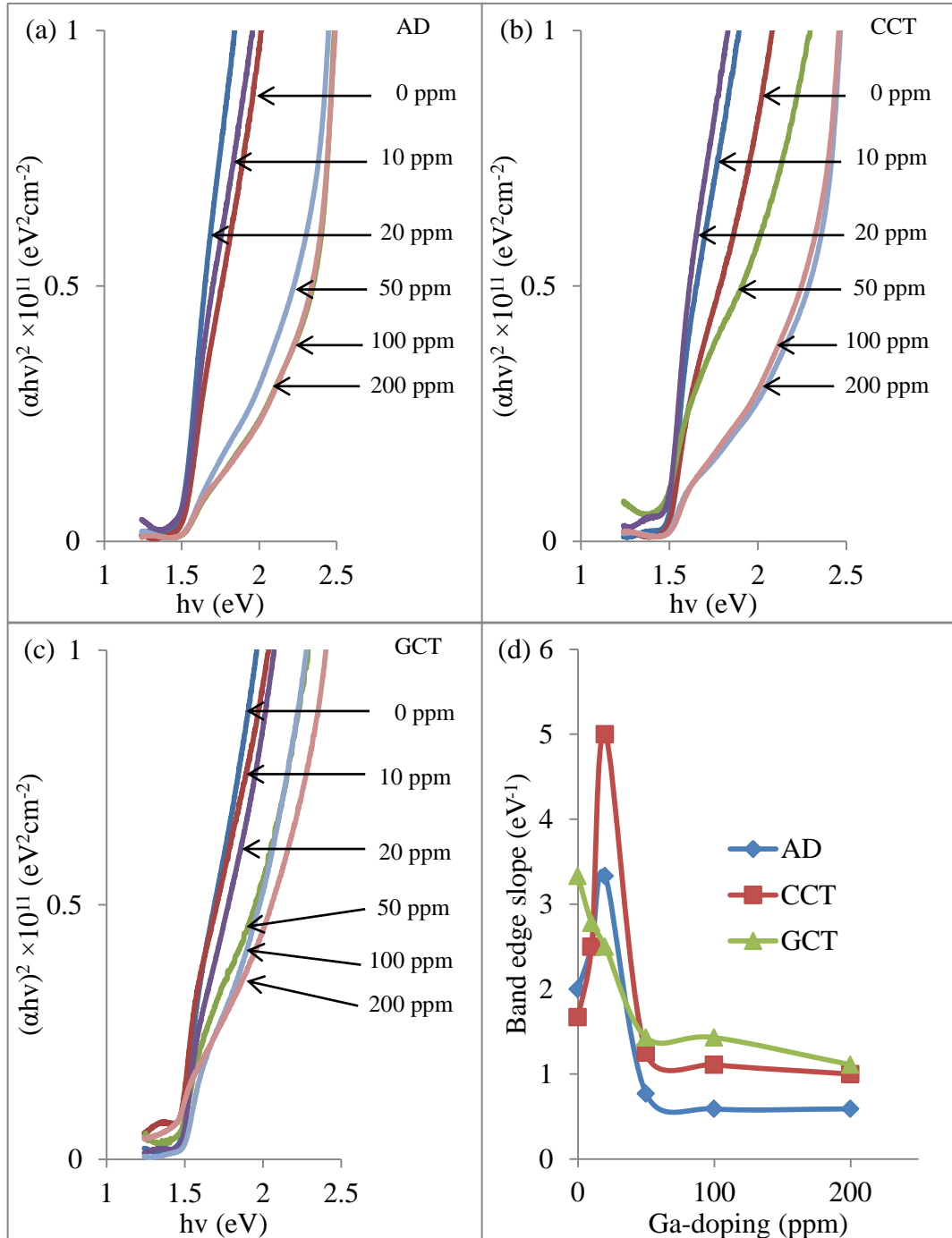
Figure 5.38: Optical absorption of CdTe:Ga with different doping concentrations of gallium under (a) AD, (b) CCT and (c) GCT conditions, while (d) is the absorption edge slope of CdTe:Ga under AD, CCT and GCT conditions against Ga-doping concentration.

This observation indicates an initial improvement in the material quality for CdTe:Ga layers with Ga-doping of 0 ppm to 20 ppm under AD and CCT conditions as shown in Figure 5.38 (d) and also suggest CdTe:Ga material quality saturation at 20 ppm Ga-doping under the conditions explored in this set of experiments. An increase in Ga-doping above 20 ppm for CdTe:Ga layers under AD and CCT shows the detrimental effect to the CdTe:Ga material quality as the reduction in the absorption edge slope suggests for Ga-doping of 50 ppm and above. This observation is in accord with the structural analysis as described earlier.

Furthermore, a dissimilar trend of absorption edge slope for the GCT treated CdTe:Ga layers was observed with undoped layers doped with 0 ppm giving the highest absorption edge slope. Although, it is well known that the treatment of CdTe in the presence of Ga melt improves the material properties of CdTe by dissolving Te precipitates [181,192], the incorporation of superfluous Ga into the CdTe lattice results in detrimental effects such as the formation of competing phases of CdTe and GaTe as observed in the structural analysis section. It should be noted that the effects of persistent photoconductivity and photo-induced persistent absorption associated with Ga-doped CdTe at 77 K [226] were not observed due to the room temperature at which the experiments were performed.

Morphological analysis

Figure 5.39 (a to l) shows the SEM micrographs of CdTe layers grown from electrolytes containing 0, 20, 50 and 100 ppm Ga-doping under the AD, CCT and GCT conditions. From observation, the initial incorporation of Ga-doping from 0 to 20 ppm under AD condition shows agglomeration of grains and full coverage of the underlying glass/FTO substrate. At 50 ppm Ga-doping, a reduction in grain and agglomeration sizes were observed, while, no clear grain boundaries were observed at 100 ppm and above. The deterioration in grain and agglomeration sizes can be attributed to competing crystalline phases of CdTe and GaTe. As expected, improvement after CCT and GCT post-growth treatment was observed with larger grain size at 0 to 20 ppm. The treatment of CdTe doped with Ga higher than 20 ppm shows detrimental effect such as comparatively smaller grains and high pinhole density. It should be noted that the pinholes observed in the 0 to 20 ppm Ga CdTe layers might be due to optimisation requirement for both heat treatment temperature and duration, Ostwald ripening, the thickness of the CdTe layer utilised and the utilisation of glass/FTO substrate. It is well known that CdTe grows

better on smooth semiconductor (with CdS being a preferred partner) surfaces due to its columnar growth configuration. Based on this observation, it could be said that the superfluous incorporation of Ga through in-situ Ga-doping of CdTe or GCT is detrimental to CdTe layer property.
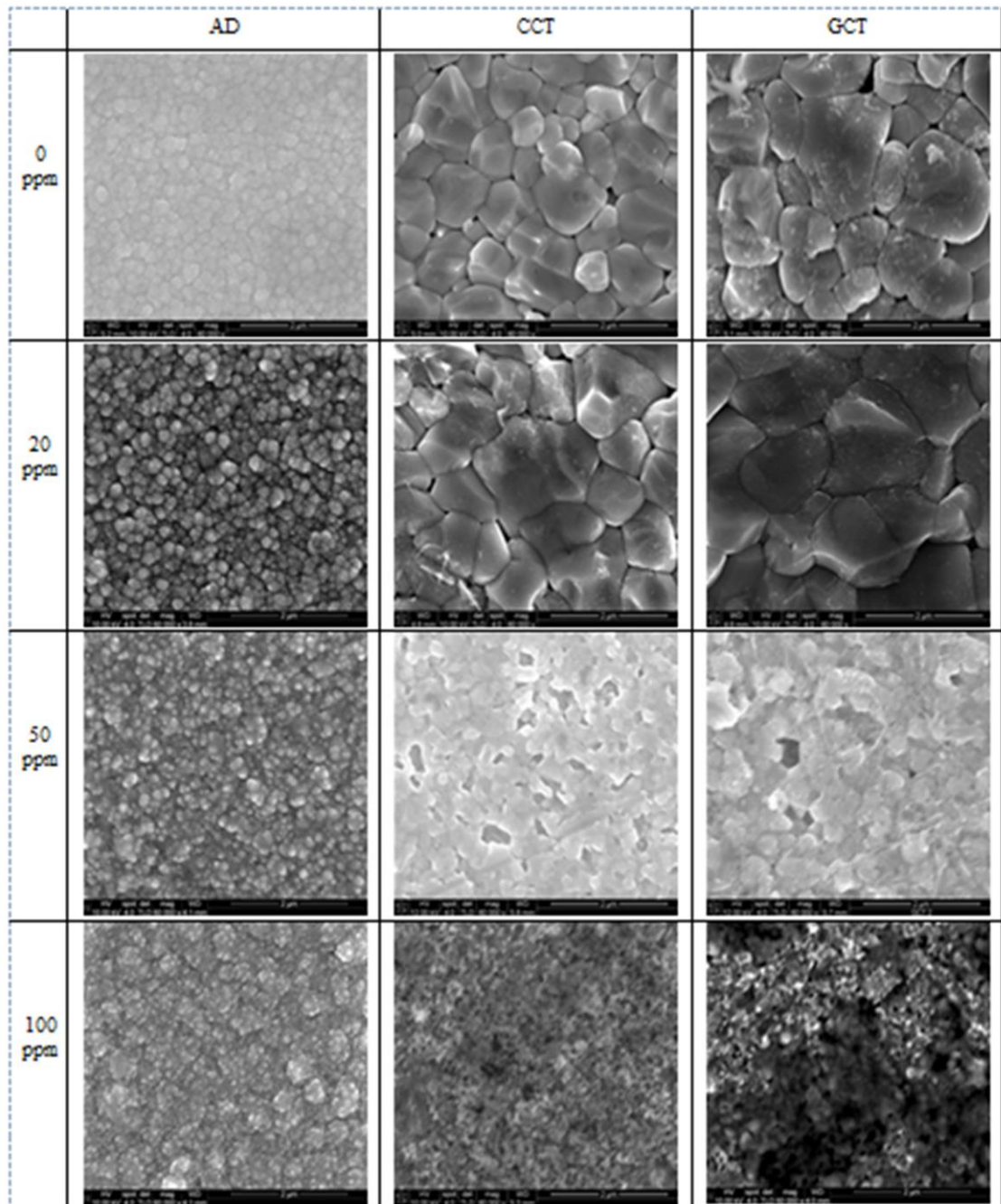
Figure 5.39: SEM micrographs for CdTe:Ga layers grown with Ga-doping concentrations between 0 and 100 ppm which have undergone AD, CCT and GCT treatments.

This observation is in accord with the structural and optical analyses discussed in the structural and optical analysis sections. It should be noted that the crystallite size as calculated using XRD does not correspond to the grain size as seen on the SEM micrograph but the grains are formed from the agglomeration of many crystallites.

Photoelectrochemical (PEC) cell measurement

Figure 5.40 shows the photoelectrochemical cell measurement against Ga-doping concentration in CdTe bath. The CdTe layers utilised for these experiments were grown at 1370 mV. For the as-deposited CdTe:Ga layers, a retention of the *n*-type conductivity was maintained from 0 to 20 ppm, while a transition from *n*- to *p*- type was observed at 50 ppm and above. The change from *n*- to *p*- type conductivity might be due to the excess replacement of Cd with Ga, whereby the doping effect is converted into an alloying effect with the complete alteration of the crystallite lattice and compound.
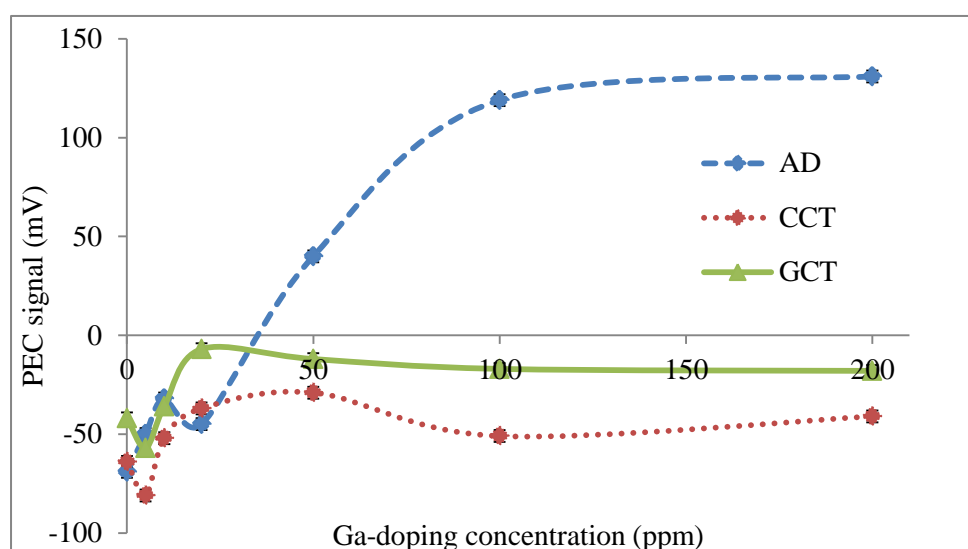
Figure 5.40: Photoelectrochemical cell measurements for AD, CCT and GCT treated Ga-doped CdTe thin films.

The excess incorporation of Ga at 50 ppm and above might either create an acceptor-like defects which might be more dominant than the *n*-doping characteristics of Ga in CdTe. Furthermore, the formation of GaTe which is typically a *p*-type semiconductor material [227,228] as observed in structural analysis section might also be the possible cause. After both CCT and GCT, the conductivity type of CdTe:Ga at all doping concentrations explored show an *n*-type electrical conductivity due to the changes occurring in the CdTe:Ga layers. This might be through the sublimation of excess element and the removal of acceptor-like defects during heat treatment. This

conductivity type change after heat treatment indicates that the *n*-doping is dominant rather than any *p*-like native defects.

DC conductivity properties analysis

Figure 5.41 (a) and Figure 5.41 (b) show the graph of both the resistance and conductivity against Ga-doping concentration of CdTe after CCT and GCT post-growth treatment conditions. For this experiment, ~1.5 μm thick CdTe:Ga layers grown from CdTe baths with varied Ga concentration from (0 to 100) ppm were utilised. The glass/FTO/CdTe:Ga layers were cut into two, and each half were either treated with CCT or GCT. 2 mm diameter indium Ohmic contacts with a thickness of ~100 nm were evaporated on the treated CdTe:Ga layers. It should be noted that only the CCT and the GCT post-growth treated CdTe:Ga was explored due to its significance in the determination of device properties.

The electrical resistance (R) of the structure was calculated from the Ohmic I-V data obtained under dark condition using a Rera Solution PV simulation system using the glass/FTO/CdTe:Ga/In. The resistivity values were obtained using Equation 3.19.
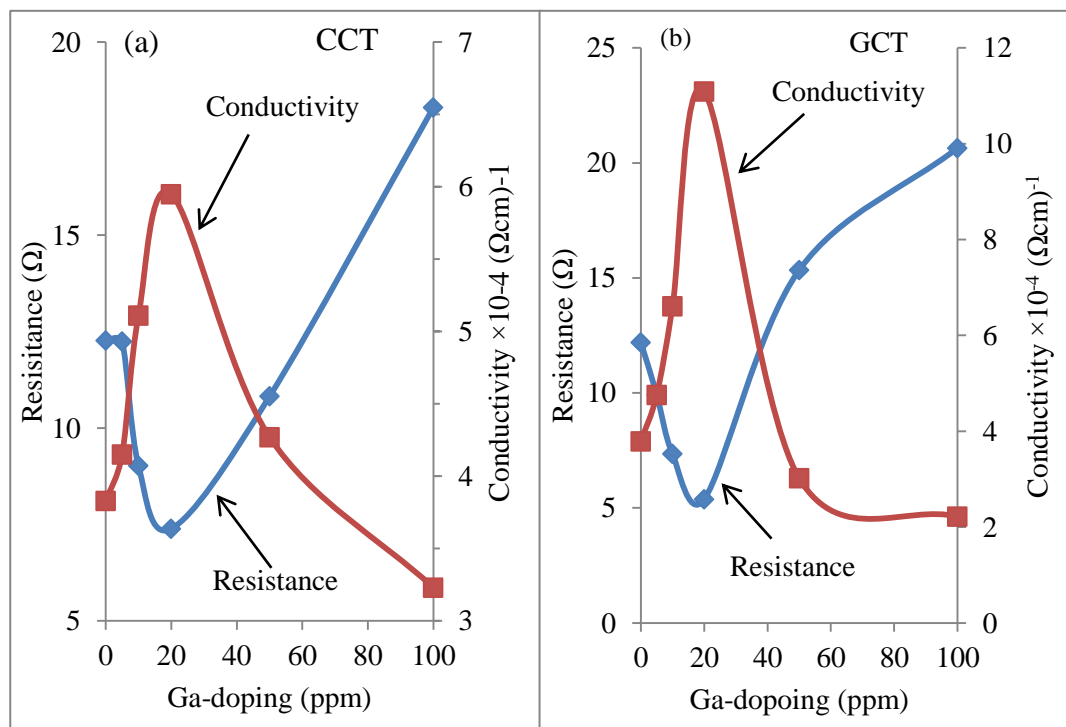
Figure 5.41: Electrical resistance and conductivity plotted against Ga-doping concentration in the CdTe bath after (a) CCT and (b) GCT treatments.

The comparable trend in the CCT and the GCT treated CdTe:Ga layers were observed as shown in Figure 5.41. The incorporation of Ga-doping from 0 ppm shows a gradual

increment in conductivity which can be attributed to the excess electrons donated from the replacement of Cd atoms with Ga atoms in the crystal lattice [192]. A possible solubility limit of CdTe:Ga was observed at ~20 ppm Ga-doping due to the gradual reduction in the conductivity [202] beyond 20 ppm doping in all conditions observed. The domination of *p*-type conductivity over the *n*-CdTe as discussed in the PEC analysis is due to the superfluous incorporation of Ga-incorporation above 20 ppm might also be a determining factor as it is well known that the mobility and the conductivity of *p*-type semiconductors are lower than that of their *n*-type counterpart [222].

Summations

The work presented in this section shows the successful exploration of the effect of in-situ Ga-doping concentration in the CdTe electrolytic bath and the inclusion of Ga in the regular $CdCl_2$ post-growth treatment on electrodeposited CdTe layers. The XRD results show an increase in the preferred (111) cubic CdTe peak from 0 to 20 ppm Ga-doping for all the post-growth treatments explored. A gradual reduction in the (111) cubic CdTe peak was observed with an emergence of the (301) monoclinic GaTe peak at 50 ppm Ga-doping and above, coupled with a reduction in crystallite size. The optical analysis shows improvement in the absorption edge with in-situ Ga-doping of CdTe from 0 to 20 ppm. Morphologically, a comparative reduction in the grain size was observed at high in-situ Ga-doping at 50 ppm and above. PEC cell measurement shows a transition of conductivity type from *n*-type to *p*-type at high Ga-doping of 50 ppm and above for the as-deposited CdTe layers.

5.7   Conclusions

The work presented in this chapter demonstrates the electrodeposition of CdTe using 2-electrode configuration from an electrolytic aqueous bath containing cadmium nitrate tetrahydrate $Cd(NO_3)_2 \cdot 4H_2O$ and tellurium oxide (TeO_2) as cadmium and tellurium precursors respectively. Based on the material characterisation techniques explored, 1370 mV was identified as the best cathodic potential in which stoichiometric CdTe is achieved. The XRD results show the presence of cubic CdTe both in the AD and post-growth treated CdTe layer with a preferred orientation along the (111) plane. Both the XRD and SEM results in this work indicate grain growth after $CdCl_2$ treatment with an increase in crystallite sizes and the formation of large grains within the range of (300 to

2000) nm. The optical absorption results showed a bandgap range of (1.45 and 1.50) eV after $CdCl_2$ treatment.

The effects of different dopants (F, I, Ga and Cl-based precursor) in the CdTe electrolytic bath were also explored.

Chapter 6 -   Solar cell fabrication and characterisation

6.1   Introduction

This chapter presents the characterisation of solar cell devices fabricated using the pre-characterised CdS and CdTe layers as documented in Chapter 4 and Chapter 5. For the fabricated PV devices as presented in this thesis, CdS is utilised as the main window layer, while CdTe is utilized as the main absorber layer in forming a heterojunction structure. Thus, the main solar cell structure explored incorporates a CdS/CdTe heterojunction core. This chapter systematically reports the effect of the incorporation of a buffer layer to base CdS/CdTe configuration, the effect of various window layer conditions on the device properties of PV devices. This is followed by the exploration of the effect of different conditions of CdTe absorber layer and post-growth treatment of the device properties. Further to this, the effect of the extrinsic doping of CdTe, metal contacts, various heat treatment temperatures, etching and the incorporation of pin-hole plugin layers into the CdS/CdTe-based PV devices were also discussed (see Figure 1.6).

6.2   Basic solar cell fabrication process: Post-growth treatment, etching process and device fabrication of CdS/CdTe-based photovoltaic devices

In this study, two aqueous solutions (A and B) were used to treat the material layers. Solution A contains 0.1 M $CdCl_2$ in 20 ml of DI water at room temperature, while solution B contains 0.1 M $CdCl_2$ and 0.05 M $Ga_2(SO_4)_3$ in 20 ml of DI water at room temperature. The solutions were stirred continuously for 1 hour to achieve homogeneity. The sample labeled AD was left as-deposited, while samples marked CCT and GCT were $CdCl_2$ treated in solution A and $CdCl_2$:Ga treated in solution B respectively.

The application of $CdCl_2$ or $CdCl_2+Ga_2(SO_4)_3$ on the grown CdTe single layers (such as glass/FTO/CdS/CdTe during material characterisation) or multilayer structure (such as glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe during device fabrication) was achieved by adding a few drops of relevant solution on their surface. The full coverage of the layers with the treatment solutions was achieved by spreading the solution using solution-damped cotton buds. Both the CCT and GCT treated glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers were allowed to air-dry before heat treatment.

The post-growth heat treatments were performed within the range of (350 to 450) °C for (60 to 20) minutes in an air atmosphere for samples undergoing each treatment based on previously optimised conditions [157,229–231]. The CCT and GCT treated layers were

then rinsed in DI water and dried in a stream of nitrogen afterward. It should be noted that the motivation for the incorporation of halides such as chlorine, fluorine and other elements such as gallium in the post-growth treatment have been well documented in the literature [30,157,181].

Characterisation of layers proceeds immediately for single semiconductor layers treated to explore their material property. While for device bound structures, the surfaces of the AD, CCT and GCT layers were etched using a solution containing $K_2Cr_2O_7$ and concentrated H_2SO_4 for acid etching and a solution containing NaOH and $Na_2S_2O_3$ for basic etching for 2 seconds and 2 minutes respectively, to improve the metal/semiconductor contact [61,214]. Immediately afterward, the (AD, CCT, and GCT) samples were transferred to a high vacuum system in order to deposit 2 mm diameter and 100 nm thick Au contacts on the device structure. The fabricated devices were analysed using characteristic device measurements (see Section 3.5) to determine their device parameters.

6.3   Effect of CdS thickness in glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au devices

Further to the effect of CdS thickness on its material properties as discussed in Section 4.4, glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au solar cell devices were fabricated using different CdS thicknesses. 1200 nm thick *n*-CdTe layers were electrodeposited at 1370 mV, followed by the deposition of ~30 nm *p*-CdTe at 1360 mV (see Section 5.3.8) in a continuous deposition process to achieve glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe configuration.

Figure 6.1 (a) shows the band diagram of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au device and Figure 6.1 (b) shows the I-V curve of a cell incorporating 150 nm thick CdS layer at AM1.5, while Figure 6.1 (c) and (d) shows the linear-linear and log-linear I-V curves of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au devices incorporating 150 nm CdS layer under dark condition.
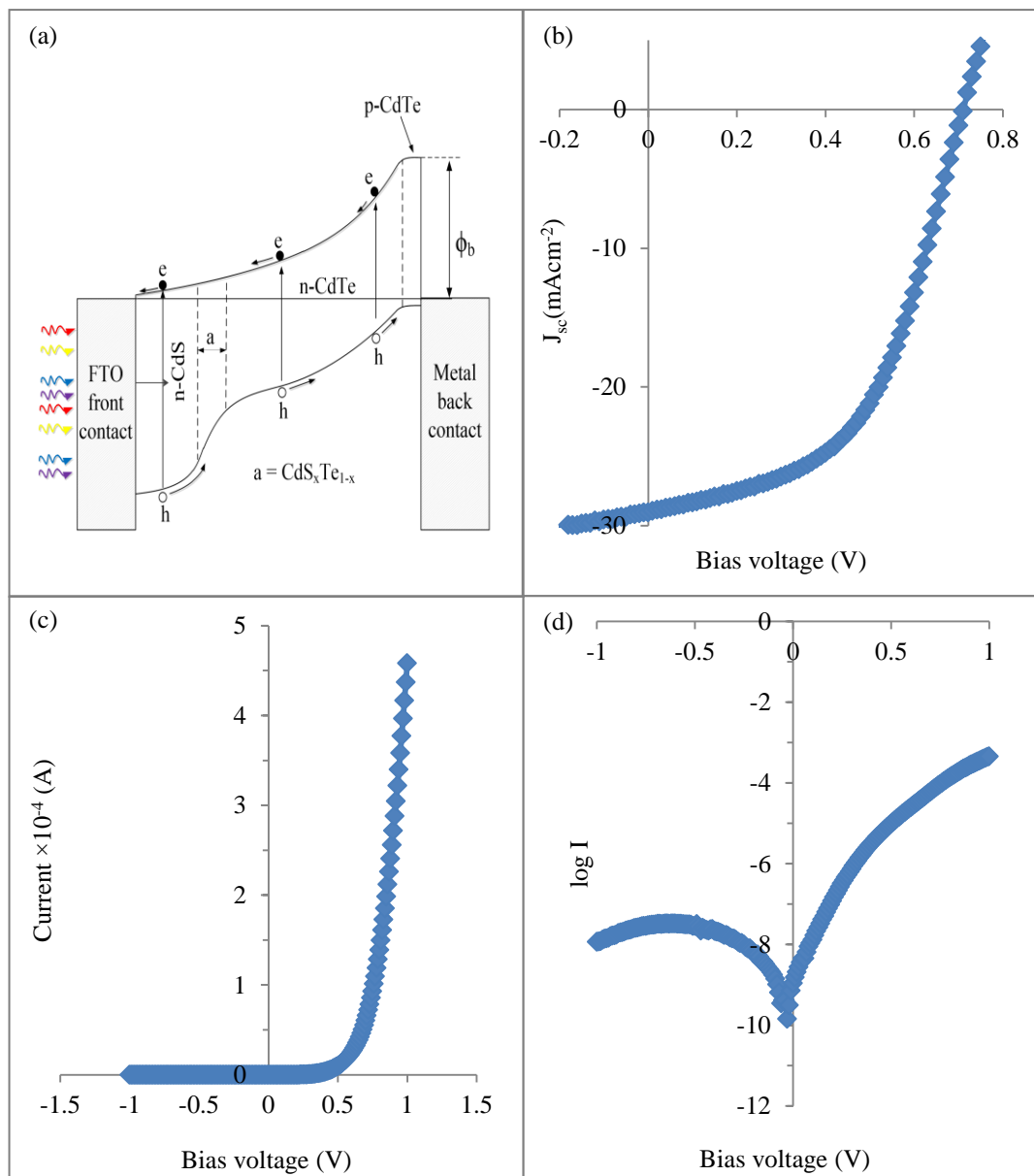
Figure 6.1: (a) The band diagram of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au thin film solar cell and (b) current-voltage curve of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au champion cell incorporating 150 nm CdS, while (c) and (d) are the linear-linear and log-linear I-V curves under dark condition.

The band diagram as depicted in Figure 6.1 (a) is a result of prior material investigation as reported in the literature by Salim et al. [170] that the conductivity type of electrodeposited CdTe layer is retained after CdCl$_2$ treatment, although, a shift towards the opposite conductivity type was observed.
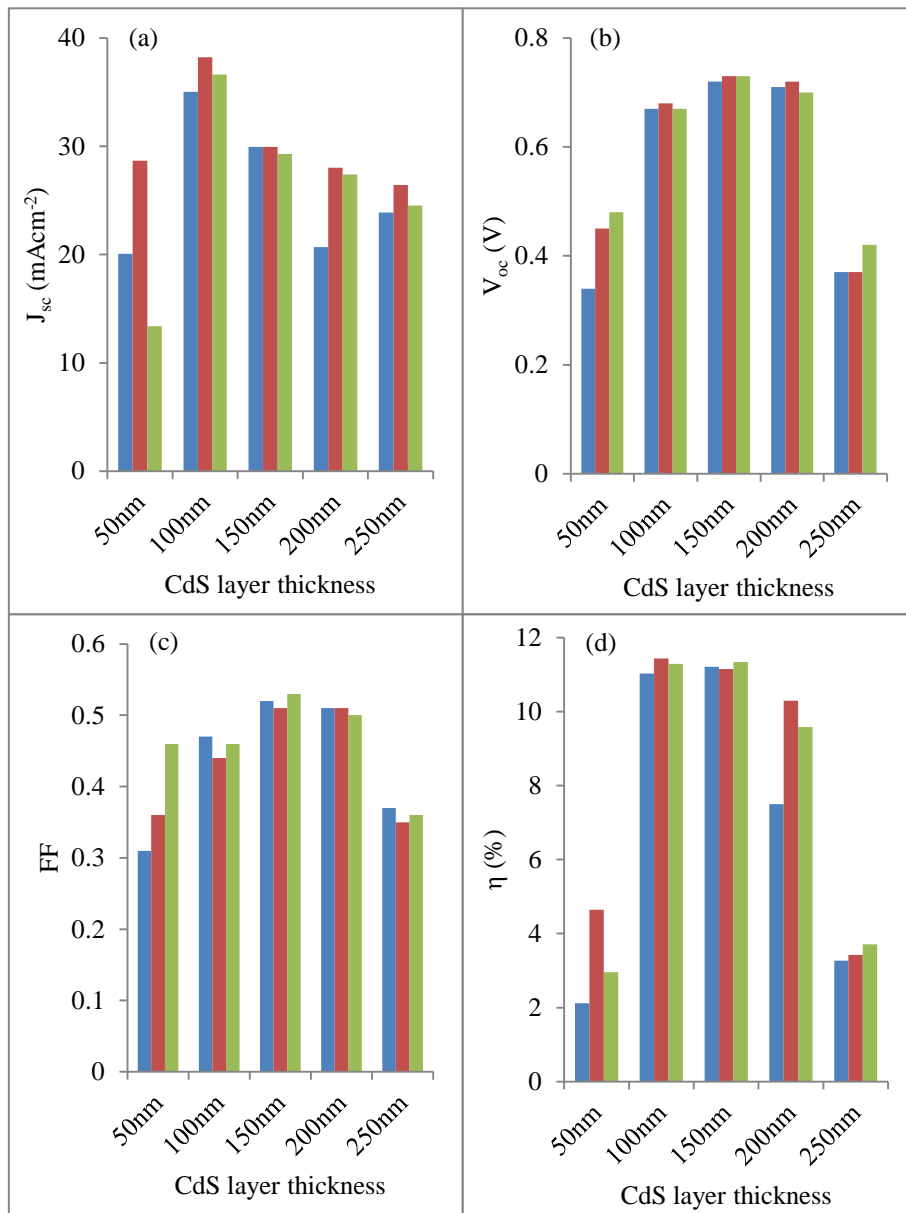
Figure 6.2: Histograms of three champion solar cell parameters from glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au with different CdS thicknesses measured at AM1.5 (a) J_{sc}, (b) V_{oc}, (c) FF and (d) η, against CdS thickness.

Figure 6.2 (a-d) shows the short-circuit current density (J_{sc}), open-circuit voltage (V_{oc}), fill factor (*FF*) and solar energy conversion efficiency (η) measured at AM1.5 against CdS layer thickness respectively, while Table 6.1 summarises the tabulated I-V parameters of the three champion cells from the solar devices with varied CdS thickness.

Table 6.1: Tabulated device parameters for three champion cells of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au incorporating different CdS thicknesses.

CdS (nm)	J_{sc} (mAcm^{-2})	V_{oc} (mV)	FF	Efficiency (%)
50	20.1	0.34	0.31	2.11
	28.7	0.45	0.36	4.64
	13.4	0.48	0.46	2.95
100	35.0	0.67	0.47	11.03
	38.2	0.68	0.44	11.43
	36.6	0.67	0.46	11.29
150	29.9	0.72	0.52	11.29
	29.9	0.73	0.51	11.15
	29.3	0.73	0.53	11.34
200	20.7	0.71	0.51	7.50
	28.0	0.72	0.51	10.29
	27.4	0.70	0.50	9.59
250	23.9	0.37	0.37	3.27
	26.4	0.37	0.35	3.42
	24.5	0.42	0.36	3.71

As shown in Figure 6.2 (a), the comparatively low J_{sc} observed in the device incorporating the 50 nm CdS layer was not expected due to the high transmittance in 50 nm thick CdS layer as discussed in Section 4.4.2. Hence, the high photocurrent is expected. But based on the incomplete coverage of the underlying glass/FTO substrate, the gaps will serve as shunting paths and thereby reducing the photo-generated current due to increased recombination of the electron-hole pairs and poor quality diode.

The increase in the CdS thickness in the device configuration to 100 nm shows higher J_{sc} due to better CdS layer coverage over the glass/FTO and high transmittance as discussed in Section 4.4.2. The devices incorporating CdS with thickness above 100 nm show a gradual reduction in J_{sc}. This might be as a result of the reduction in transmittance, photo-generated current and also increased parasitic absorption due to increased CdS thickness [30,130]. Ganata et al demonstrated low CdS thickness (40 nm) [130] to achieve the highest photocurrent using high temperature (600°C) closed-space-sublimation growth technique due to the unique qualities of CdS. However, electrodeposition at low temperature (~85°C) on the other hand, requires an increased thickness of CdS layer to suppress the effect of surface roughness and deposition/nucleation mechanism. It should be noted that the J_{sc} as observed in this work is higher than the Shockley–Queisser limit of ~26 mAcm^{-2} on single *p-n* junction

incorporating CdTe absorber layer [20] due to the incorporation of the multilayer *n-n-p* configuration [232].

An increase in both V_{oc} and *FF* with increasing CdS thickness up to 200 nm as shown in Figure 6.2 (b) and Figure 6.2 (c) is also observed. This observation can be associated with the reduction of shunts [131] and other defects relating to the early CdS nucleation stages. Ultimately, the efficiency of devices incorporating both the 100 nm and 150 nm thick CdS layer appears to be the highest with fairly similar efficiency values due to comparatively high J_{sc} observed in the 100 nm CdS and high V_{oc} plus *FF* in the device incorporating 150 nm thick CdS layer. It should be taken into account that shunt resistance is associated with semiconductor layer quality [233] which explains the low efficiency observed in the device incorporating the electrodeposited 50 nm thick CdS layer. While the gradual reduction in efficiency with increasing thickness is due to the low transmittance, reduced photocurrent as a result of increased parasitic absorption [131].

Table 6.2: Diode parameters extracted from dark I-V for champion cells of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au incorporating different CdS thicknesses.

CdS (nm)	$R_{sh} (\Omega)$	R_s (kΩ)	log (RF)	I_o (A)	n	ϕ_b (eV)
50	51.1	0.02	0.3	2.81×10^{-3}	>2.00	>0.42
100	4.3×10^6	0.50	4.1	1.02×10^{-9}	1.86	>0.80
150	6.2×10^6	0.57	4.4	1.26×10^{-9}	1.71	>0.80
200	3.5×10^6	0.80	3.5	3.98×10^{-9}	1.95	>0.77

Table 6.2 shows the diode parameters such as shunt resistance R_{sh}, series resistance R_s, rectification factor *RF*, saturated current I_o, ideality factor *n* and barrier height ϕ_b as obtained from the champion cells of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au devices incorporating different CdS thicknesses tabulated in Table 6.1. As observed in Table 6.2, the low R_{sh} observed for devices incorporating 50 nm thick CdS layer signifies the presence of shunt paths. The shunting might be due to the incomplete coverage of the glass/FTO with CdS as discussed in Section 4.4, thereby creating direct leakage paths between the glass/FTO substrate and the grown CdTe layers as further suggested by the comparatively high I_o value observed using the 50 nm thick CdS layer. From observation, the R_s under dark condition is high for layers incorporating CdS thickness of 100 nm and above. However, I-V measurements under illuminated condition show a reduction in R_s value to (100 – 200) Ω range. This reduction is due to the

photoconductivity of the material layer used. As iterated by Dharmadasa et al. [16], high-efficiency solar cells can only be achieved provided the *RF* value is $\geq 10^3$. The *RF* values as observed for devices incorporating CdS with thickness ≥ 100 nm shows the tendency of achieving high efficiency. Furthermore, the ideality factor *n* which depicts the charge carrier transportation mechanisms show that the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au devices incorporating CdS with a thickness between 100 nm and 200 nm are governed by both recombination and generation (R&G) centers and thermionic emission. The devices with the 50 nm CdS layers have the highest *n* values ($n > 2.00$). This is due to low-quality CdTe material deposited on FTO regions instead of the fully covered FTO layer with CdS. CdS provide a high quality substrate for growing superior CdTe layers with low defect densities. The lowest ideality factors observed for 100 & 150 nm shows the presence of low defects reducing R&G process. Therefore the J_{sc} values can be large for such devices as we experimentally observed in this work.

6.3.1   Photovoltaic (PV) device yield

Figure 6.3 shows the graph of the percentage yield of the active cells as against the CdS thickness incorporated in the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au structure. The number of cells in all the fabricated solar cell devices incorporating different CdS window layer thicknesses was 12. It was discovered that the percentage of PV active cell in the device incorporating 50 nm thick CdS was low. This observation can be related to the morphological analysis as discussed in Section 4.4.3.
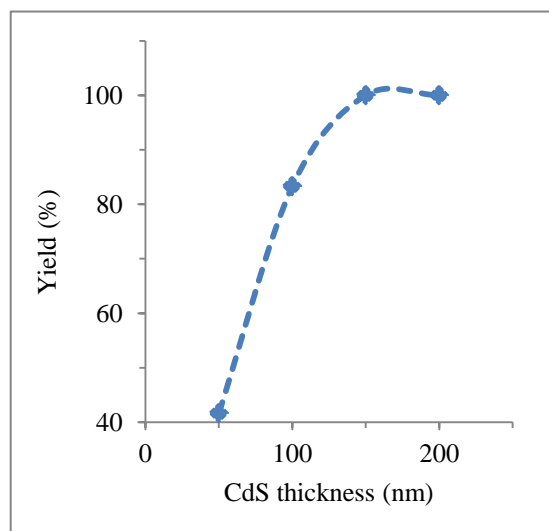
Figure 6.3: Graph of percentage yield against CdS thickness in a glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au device structure.

There is a high tendency that the non-functional cells are glass/FTO/n-CdTe/p-CdTe/Au due to the incomplete coverage of the underlying CdS layer. It should be noted that although a depletion layer is expected in-between the n-CdTe and p-CdTe, but, due to the characteristic large grains observed in CdTe after treatment, the increased grain growth of CdTe on a rough surface favours the inclusion of pores or pinholes in-between the grains after treatment. This leaves Au with the tendency of contacting directly with glass/FTO creating shunting paths and electron-hole pair recombination centers. An increase in the CdS thickness above 50 nm improves the percentage yield close to 100% at 150 nm CdS thickness.

6.3.2   Standard deviation

Figure 6.4 shows the normal distribution curve of both J_{sc} and η using standard deviation parameters as presented in Table 6.3. As stated in Section 6.3.1 only three champion cells from each fabricated device incorporating 50 nm, 100 nm and 150 nm thick CdS were considered in this work due to high parasitic absorption observed with higher CdS thickness.   Both the mean ($\bar{x}$) and the standard deviation (δ) were calculated as shown in Equation 6.1 and Equation 6.2 respectively, where n is the number of cells explored, and x is the value of the parameter of the explored cells.

$$\bar{x} = \frac{1}{n} \sum_{i=1}^{n} x_i \qquad\qquad \text{Equation 6.1}$$

$$\delta = \sqrt{\frac{\sum \left(x - \bar{x}\right)^2}{n-1}} \qquad\qquad \text{Equation 6.2}$$

It should be noted that the data utilised in the calculations shown in Table 6.3 is an extract from Table 6.2. The standard deviation as depicted using the normal distribution curve is used to measure the dispersion in a set of explored data. The horizontal axis represents the dependent variable which for the sake of the work is J_{sc} and η in Figure 6.4 (a) and (b) respectively, while the vertical axis shows the probability that the value of the standard deviation will occur.

Table 6.3: Table of mean and standard deviation of three champion cells device parameters incorporating different CdS thickness in glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration.

	Mean $\bar{x} = \dfrac{1}{n}\sum\limits_{i=1}^{n} x_i$				Standard deviation $\delta = \sqrt{\dfrac{\Sigma(x-\bar{x})^2}{n-1}}$			
CdS (nm)	J_{sc} (mAcm^{-2})	V_{oc} (V)	Fill factor	η (%)	J_{sc} (mAcm^{-2})	V_{oc} (V)	Fill factor	η (%)
50 nm	20.70	0.423	0.38	3.24	7.66	0.074	0.0764	1.2879
100 nm	36.62	0.673	0.46	11.25	1.59	0.006	0.0153	0.2039
150 nm	29.72	0.726	0.52	11.23	0.37	0.006	0.0100	0.0971
200 nm	25.37	0.710	0.51	9.12	4.06	0.010	0.0058	1.4537
250 nm	24.95	0.386	0.36	3.47	1.33	0.029	0.0100	0.2222

As shown in Figure 6.4 (a), the highest J_{sc} was observed in the device incorporating the 100 nm thick CdS layer with a 50% probability of achieving 36.62 mAcm^{-2} and ~30% probability of occurrence as compared to the devices incorporating 150 nm thick CdS layer with 50% probability of achieving a J_{sc} of 29.72 mAcm^{-2} and ~80% probability of occurrence. In both the devices incorporating 100 nm and 150 nm thick CdS interesting features such as high J_{sc} and high probability of occurrence can be explored by carefully optimising the CdS layer thickness to fall in-between 100 and 150 nm CdS thickness.
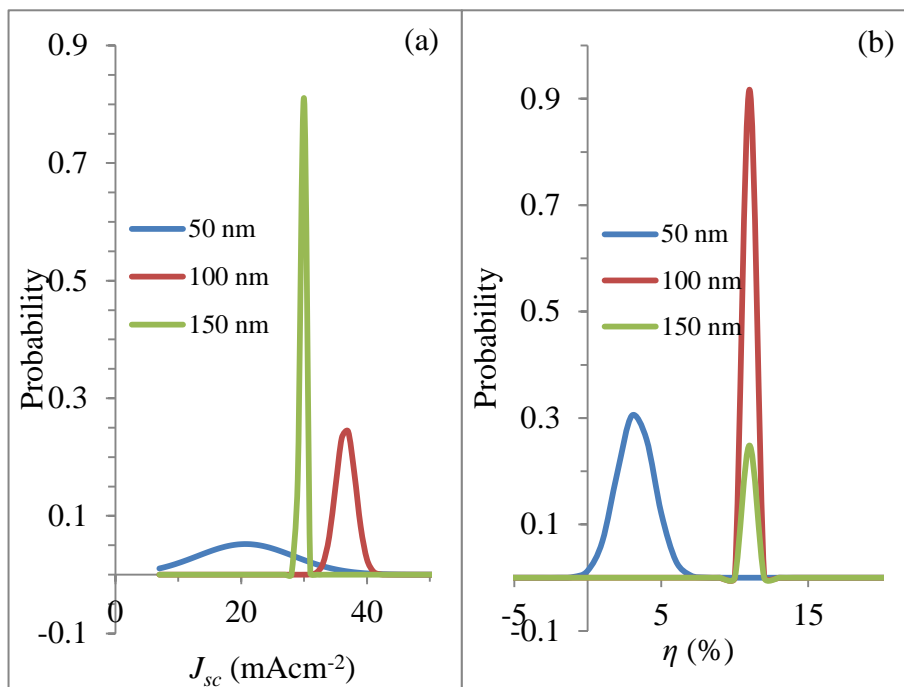
Figure 6.4: Normal curves of probability of occurrence against (a) J_{sc} and (b) η%.

It should be noted that one of the advantages related to an increase in the thickness of the CdS window layer is smoothening out the surface before absorber layers such as CdTe can be grown. Devices incorporating the 50 nm thick CdS layers show the largest dispersion of J_{sc}, lowest J_{sc} value range and less that 10% probability of achieving comparably high photocurrent based on the results obtained from this work. For example, based on the normal curve generated in Figure 6.4 (a), less than 5% of the fabricated cells in a device can achieve J_{sc} of 30 mAcm^{-2} and above for devices incorporating 50 nm CdS thickness. While devices incorporating 100 nm and 150 nm thick CdS show 100% and 50% probability of achieving 30 mAcm^{-2} short-circuit current density respectively. The effect of both pin-holes and parasitic absorption is annotated for the low (50 nm) and high (150 nm) CdS thickness in this work.

Furthermore, Figure 6.4 (b), shows that the highest η can be achieved with devices incorporating both 100 nm and 150 nm thick CdS with the high occurrence probability of ~90% observed at 100 nm and ~30% occurrence probability for the 150 nm thick CdS. It should be noted that the η of the device incorporating the 50 nm thick CdS shows the low η values range and low probability of occurrence.

6.3.3   Summations

In conclusion, this work supports the work done by other researchers on the optimisation of CdS thickness as related to CdS/CdTe cell but focuses on the iteration of the effect of deposition technique and nucleation mechanism of electroplated semiconductor materials. But contrarily, the proposed thin CdS window layer with thickness <50 nm by other authors cannot achieve comparatively high efficiency using electrodeposition technique without detrimental effect as demonstrated in this section.

From the observed results, optical properties such as transmittance favour the 50 nm CdS thickness while crystallinity favoured the highest CdS thickness with increase in both crystallite size and preferred orientation reflection intensity. But with a more critical observation on PV property and statistical analysis, the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au show better device property with the incorporation of 100 nm to 150 nm thick CdS layer relative to the optical, morphological, structural and electronic properties analyses of the incorporated CdS layer.

6.4   Effect of CdTe growth voltage on the efficiency of a simple CdS/CdTe-based solar cell

Further to the summations made on the effect of Cd/Te atomic composition in the determination of the conduction type of CdTe (see compositional and PEC analysis in Section 4.3.7 and Section 4.3.8), CdTe layers were grown on similar glass/FTO/n-CdS layers. The ~120 nm thick CdS layers incorporated were grown on a (6×5) cm^2 glass/FTO layer. The electrolytic bath setup was in accordance with the CdS growth parameters as discussed in Section 4.2.1. The CdS layers were CdCl$_2$ treated at 400°C for 20 minutes in the air. Prior to the deposition of CdTe, the glass/FTO/n-CdS layers were air-cooled and rinsed in DI water and cut into six (1×5) cm^2 glass/FTO/n-CdS strips. ~1200 nm thick CdTe layers were grown at cathodic voltages between 1340 mV and 1400 mV (see Figure 6.5) on the individual glass/FTO/n-CdS layers to give either glass/FTO/n-CdS/p-CdTe/Au (for $V_g < V_i$) or glass/FTO/n-CdS/n-CdTe/Au (for $V_g > V_i$) layers after metallisation. The band diagrams of both device configurations are shown in Figure 6.6, the I-V curves are shown in Figure 6.7, while the measured parameters are tabulated in Table 6.4.
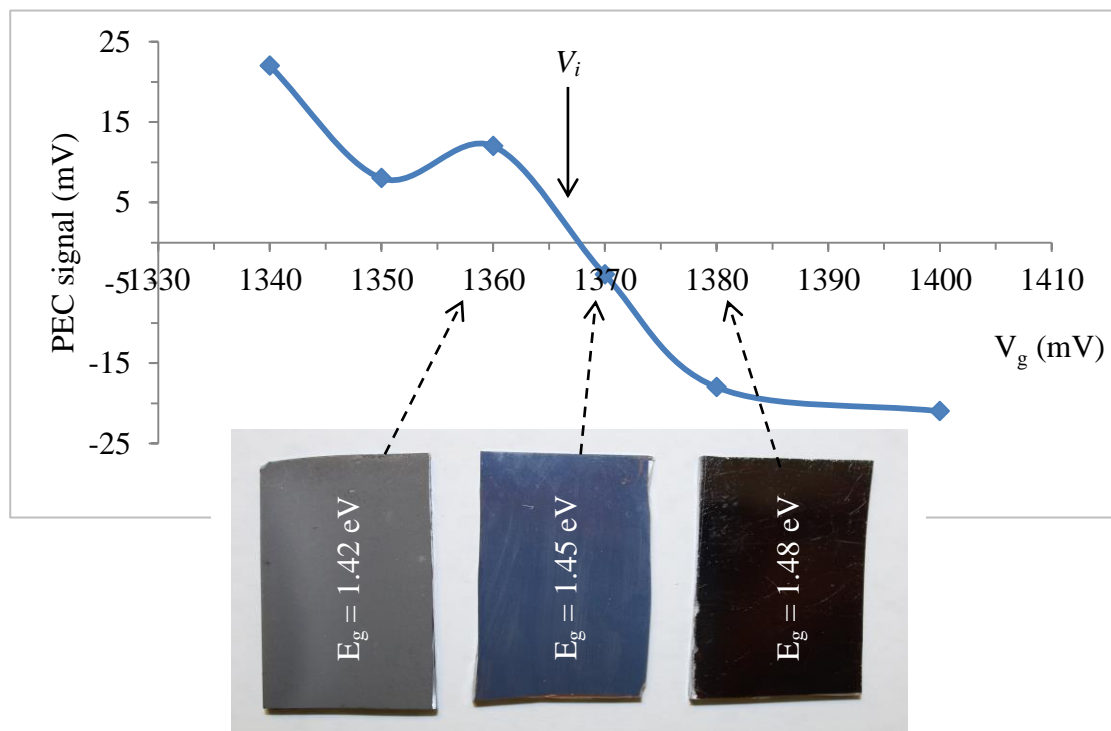
Figure 6.5: The physical appearance of CdTe layers grown close to the transition voltage (V_i=1.368 V). Colour of the CdTe layer varies from dark, light-dark to honey-colour and transparent when moved from Te-richness to Cd-richness. The average bandgap values of five measurements are also indicated for layers grown in this region.
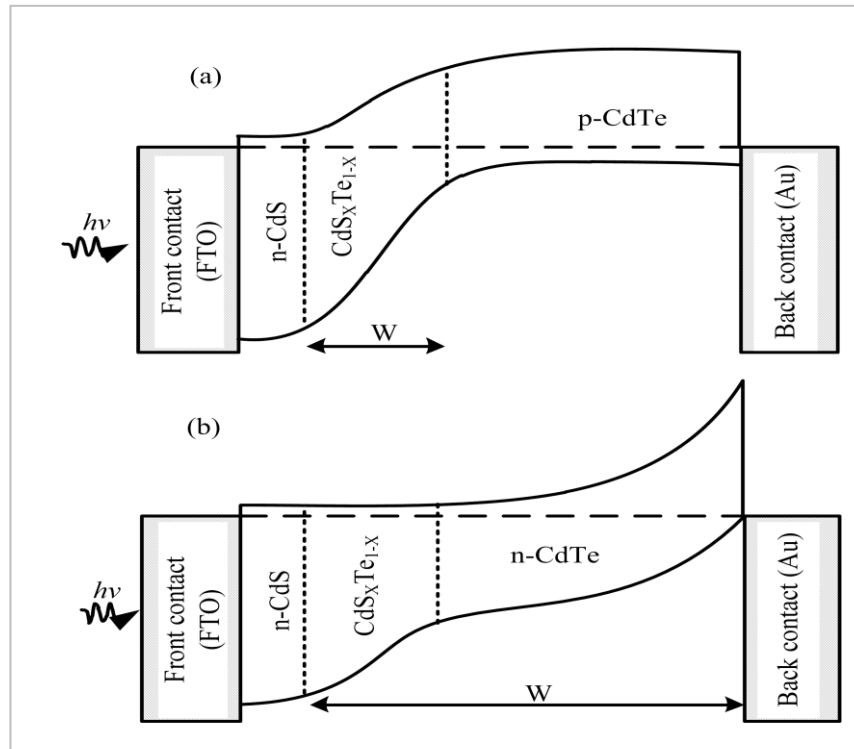
Figure 6.6: Typical schematic diagrams representing (a) glass/FTO/*n*-CdS/*p*-CdTe/Au and (b) glass/FTO/*n*-CdS/*n*-CdTe/Au device configurations.

It should be noted that due to the Fermi level (FL) pinning at the *n*-CdTe/metal interface for the device configuration as shown in Figure 6.6 (b) [52,61] a large Schottky barrier (SB) can be formed at this interface. Consequently, the CdS/CdTe/metal structure forms an *n*-*n*+SB structure with two PV active junctions. The photo-generated current components produced by these two rectifying interfaces (*n*-*n*+SB) add-up together, therefore, the two junctions are connected in parallel. Consequently, this configuration can be classified as a tandem solar cell with two junctions connected in parallel [14,15] and capable of producing improved performance such as J_{sc} above the Shockley–Queisser limit [20] on single p–n junction device.

The narrative of the effect of near-stoichiometric, Te-rich and Cd-rich can be better described using Table 6.4 which is further to the visual, optical and photoelectrochemical observations as shown in Figure 6.5. Due to brevity, a few crucial points will be focused on. The low R_{sh} as observed with devices incorporating *p*-CdTe grown at 1340 mV (~-30 mV away from V_i) is an indication of low material quality as inferred in the literature [135] and attributed to the presence of Te-precipitates, voids, gaps, high dislocation density within the semiconductor material.

On the other hand, slight reductions in R_{sh} were recorded for the devices incorporating n-CdTe grown at 1400 mV (~+30 mV away from V_i). Further observation of parameters including the RF, I_o, $n,$ and ϕ_b of the fabricated devices measured using I-V curves under dark condition show comparatively preferred electronic property for devices incorporating n-CdTe absorber layers. Taking into consideration that log(RF) of 3 is a requirement of high-efficiency solar cells [16] and the observed n values were within 1.00 and 2.00, this signifies that the current transport mechanisms consist of both thermionic emission and R&G for devices incorporating CdTe layers grown between 1360 mV and 1400 mV. The n-value of devices incorporating p-CdTe grown at 1340 mV (n>2.00) indicate the Te-rich CdTe layers have more defects contributing to R&G process. This observation may be the probable cause of the reduction in the barrier height ϕ_b, while the comparatively low depletion width of 187.6 nm (as shown in Table 6.4) may have aided additional tunneling in the fabricated devices as discussed in Section 2.3.4. It is therefore not surprising that the resulting I-V parameters measured under AM1.5 illuminated condition for 1340 mV incorporating p-CdTe are the lowest. This may either be due to the incorporation of midgap defects due to superfluous Te or sublimation of Te-precipitates during post-growth heat treatment increasing pinhole density. It should be noted that the fabricated devices incorporating p-CdTe grown at 1360 mV, which is possibly at ppm or ppb level doping of CdTe with Te, show high conversion efficiency as compared to the 1340 mV p-CdTe device due to the growth of CdTe at the vicinity of V_i. On the other hand, devices incorporating excess Cd within the explored cathodic voltage of (1370 to 1400) mV show minimal parameter alteration with the best conversion efficiency obtained with devices incorporating n-CdTe grown at 1370 mV. It should be noted that the inclusion of Te precipitates in the growth of CdTe notwithstanding the technique of growth is the main detriment of CdTe [181].
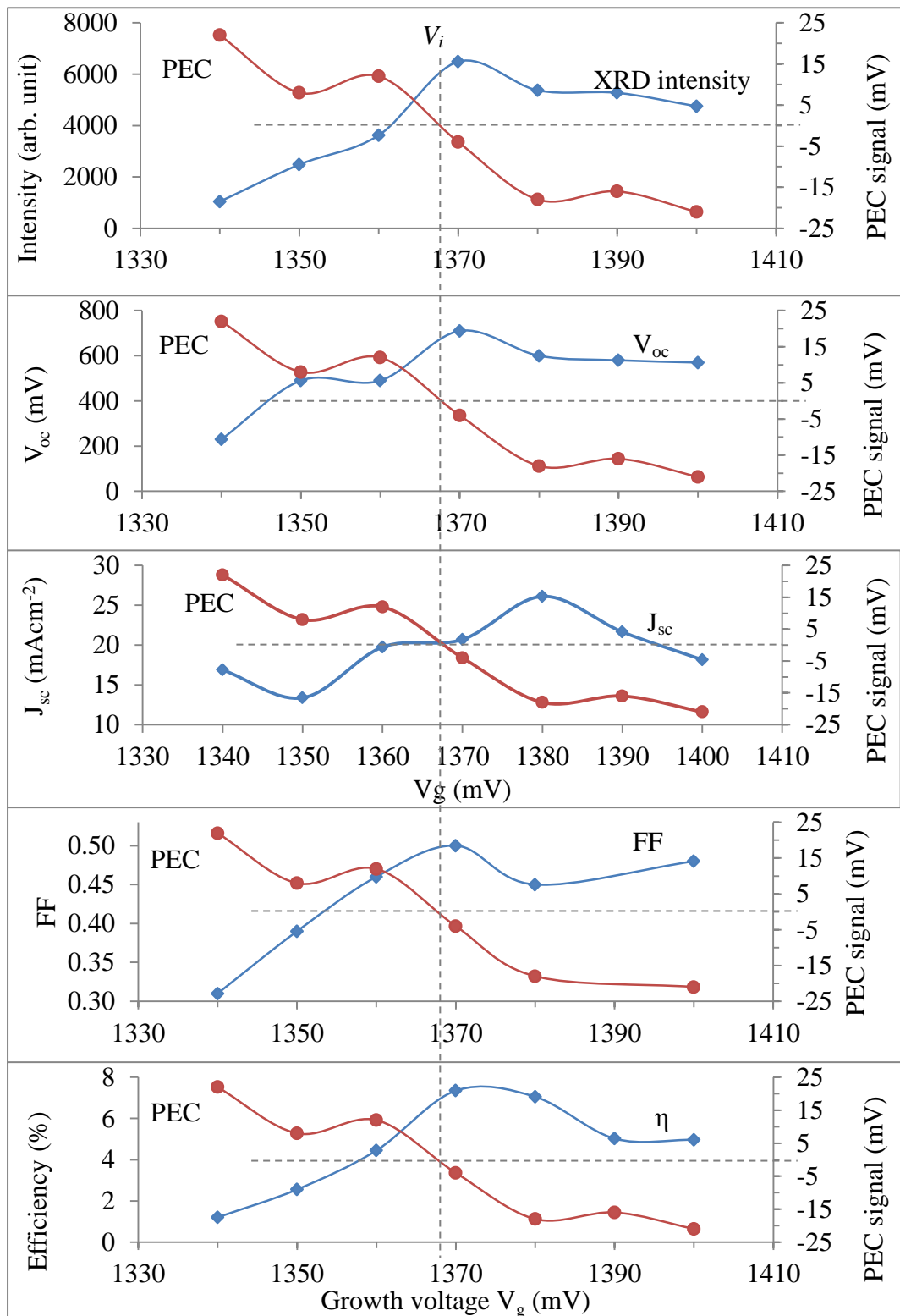
Figure 6.7: Typical variation of the PEC signal for CdCl$_2$ treated CdTe is shown in each frame to separate the *p*-type and *n*-type regions. The intensity of (111) XRD peak is shown in the first frame indicating best crystallinity around V_i. The device parameters for glass/FTO/CdS/CdTe/Au solar cells fabricated with the CdTe layers grown in the vicinity of the transition voltage, V_i=1368 mV are shown in the other four frames.

Table 6.4: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for simple CdS/CdTe-based solar cells grown at different growth voltages in the vicinity of V_i.

CdTe growth voltage (mV)	1340	1360	1370	1380	1400
I-V under dark condition					
R_{sh} (Ω)	1016	$>10^5$	$>10^5$	$>10^5$	$>10^5$
R_s (kΩ)	0.21	0.80	0.50	1.43	1.50
log (RF)	0.4	3.5	3.9	3.3	3.0
I_o (A)	2.5×10^{-5}	3.9×10^{-9}	1.0×10^{-9}	3.2×10^{-9}	5.0×10^{-9}
n	>2.00	1.95	1.86	1.58	1.86
Φ_b (eV)	>0.52	>0.76	>0.81	>0.77	>0.77
I-V under 1.5 AM illumination condition					
I_{sc} (mA)	0.53	0.62	0.65	0.82	0.57
J_{sc} (mAcm^{-2})	16.88	19.75	20.70	26.11	18.15
V_{oc} (V)	0.23	0.49	0.72	0.6	0.57
Fill factor	0.31	0.46	0.50	0.45	0.48
Efficiency (%)	1.20	4.45	7.50	7.05	4.97
C-V under dark condition					
$\sigma\times10^{-4}$ (Ω.cm)$^{-1}$	1.41		2.85		6.03
N_D (cm^{-3})	7.74×10^{16}		3.10×10^{14}		9.10×10^{14}
μ (cm^{2}V^{-1}s^{-1})	0.01		5.74		4.14
C_o (pF)	1630		330		370
W (nm)	187.6		926.7		826.5

6.5   Comparative analysis of *n*-CdS/*n*-CdTe and *n*-ZnS/*n*-CdS/*n*-CdTe devices

The incorporation of thin *n*-ZnS as a buffer layer into the *n*-CdS/*n*-CdTe device configuration (see Section 6.4) is mainly due to its wetting ability [234] and optoelectronic properties. ZnS with a bandgap of ~3.70 eV [235] shows high capability as a buffer layer due to its high transparency in the short wave length region (350 to 550) nm as compared to CdS with a bandgap of 2.42 eV. The 50 nm thick ZnS incorporated in the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device configuration was electroplated from an aqueous electrolytic bath containing 0.2 M ZnSO$_4$.H$_2$O and 0.2 M (NH$_4$)$_2$S$_2$O$_3$ as Zn and S precursor respectively [236]. Prior to the deposition of CdS, the *n*-ZnS was heat-treated at 300 °C and rinsed after being air-cooled. The procedure for the deposition of the *n*-CdS/*n*-CdTe layers for both device architectures under comparison is similar. The thicknesses of both glass/FTO/*n*-CdS/*n*-CdTe/Au and

glass/FTO/n-ZnS/n-CdS/n-CdTe/Au prior to any treatment is glass/FTO/120 nm/1200 nm/100 nm and glass/FTO/50 nm/65 nm/1200 nm/100 nm respectively.
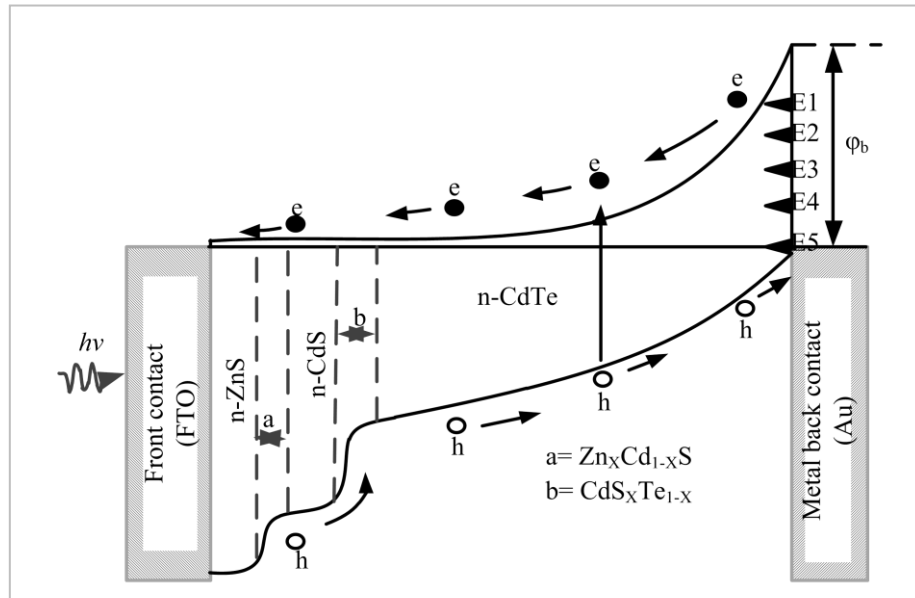
Figure 6.8: Typical band diagram of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device configuration.

The band diagram of the glass/FTO/n-CdS/n-CdTe/Au is similar to Figure 6.6 (b), while the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au configuration is shown in Figure 6.8. The presence of interfacial ternary compounds such as $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} were incorporated in Figure 6.8, as it is well documented in the literature that the formation of $Zn_xCd_{1-x}S$ is due to the interdiffusion of Zn and Cd between the ZnS and the CdS, while the formation of CdS_xTe_{1-x} is due to the interdiffusion of S and Te between the CdS and CdTe layers during post-growth annealing in the presence of $CdCl_2$ [28,237,238].

Apart from the advantages of graded bandgap configuration such as harnessing photons from UV, Visible and IR from the electromagnetic spectrum as discussed in Section 2.4.4, the incorporation of a large bandgap buffer layer as in the case of n-ZnS increases the possibility of absorbing high energy photons at the blue-end of the electromagnetic spectrum coupled with the prospect of the incorporation of the impurity PV effect and impact ionisation aiding photon absorption in the infrared (IR) region. The depletion region in this glass/FTO/n-ZnS/n-CdS/n-CdTe/Au structure may span across the whole device thickness when adequately optimised as depicted by the band bending (instigating potential difference and integrated electric field for e-h separation) shown in Figure 6.8.
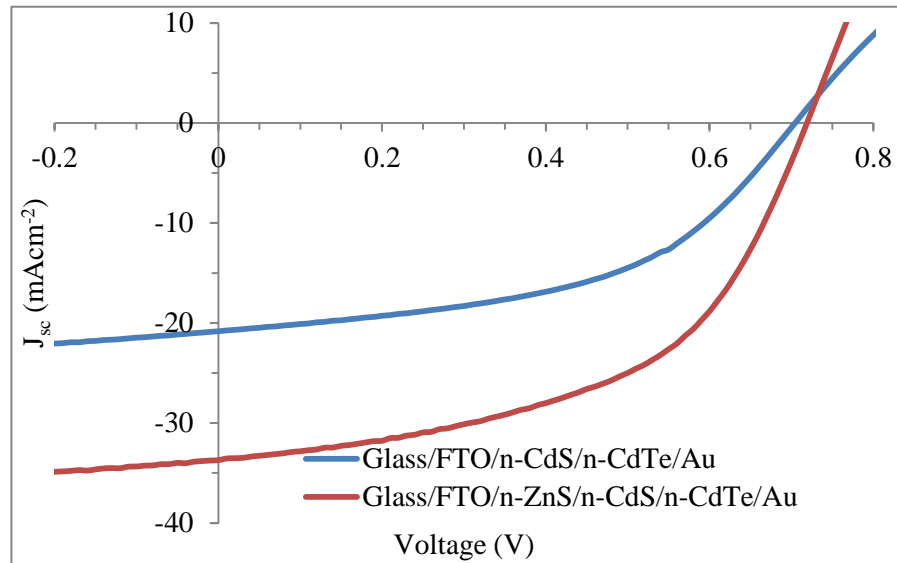
Figure 6.9: I-V characteristics of both glass/FTO/*n*-CdS/*n*-CdTe/Au and glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au structures under AM1.5 illumination condition.

Table 6.5: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for glass/FTO/*n*-CdS/*n*-CdTe/Au and glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au solar cells.

CdTe growth voltage (mV)	Glass/FTO/*n*-CdS/*n*-CdTe/Au (Two-layer device)	Glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au (Three-layer device)
I-V under dark condition		
R_{sh} (Ω)	$>10^5$	$>10^5$
R_s (kΩ)	0.50	0.47
log (*RF*)	3.9	4.8
I_o (A)	1.0×10^{-9}	1.0×10^{-9}
n	1.86	1.60
Φ_b (eV)	>0.81	>0.82
I-V under 1.5 AM illumination condition		
I_{sc} (mA)	0.65	1.07
J_{sc} (mAcm^{-2})	20.70	34.08
V_{oc} (V)	0.72	0.73
Fill factor	0.50	0.57
Efficiency (%)	7.50	14.18
C-V under dark condition		
$\sigma \times 10^{-4}$ (Ω.cm)$^{-1}$	2.85	8.82
N_D-N_A (cm^{-3})	3.10×10^{14}	7.79×10^{14}
μ (cm^{2}V^{-1}s^{-1})	5.74	7.07
C_o (pF)	330	280
W (nm)	926.7	1092.2

The I-V characteristics of both glass/FTO/*n*-CdS/*n*-CdTe/Au and glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au structure under AM1.5 illumination condition are shown in Figure 6.9 while Table 6.5 shows the summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition). As observed in Table 6.5, it is not surprising that higher J_{sc} above the Shockley–Queisser limit of a single *p–n* junction was observed for glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au as compared to the glass/FTO/*n*-CdS/*n*-CdTe/Au configuration. Further to this, is the improvement of the V_{oc}, *FF* and consequently the conversion efficiency (see Table 6.5). Likewise, both the mobility and the depletion width is comparatively higher owing to improved electronic properties.

6.6   Characterisation of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au solar cell

The motivation for the incorporation of thin *p*-CdTe layer to the glass/FTO/*n*-CdS/*n*-CdTe/Au configuration as discussed in Section 6.4 is for the formation of a depletion region and band bending at the *n*-CdTe/*p*-CdTe interface with very low lattice mismatch. Further to this, the minimisation of contact resistance [100,109], enhancement of band bending by pinning the Fermi level (FL) close to the valence band [61] and improvement of the reproducibility of the devices were all expected. This configuration is expected to increase photogenerated charge carriers by minimising recombination within the bulk of the configuration and enhance J_{sc}. It should be noted that pinning the FL close to the valence band of semiconductor materials such as CdTe can be achieved through surface etching as demonstrated in the literature [239,240], incorporation of p^+ dopant and other surface treatments [44].

Figure 6.10 (a) shows the schematic diagram of the preliminary device structure fabricated and tested in this work. The full device consisted of three semiconducting layers as in; glass/FTO/*n*-CdS (~150 nm)/*n*-CdTe (~1144 nm)/*p*-CdTe (~35 nm)/Au. The thicknesses used for different layers are also indicated, and a thick *n*-CdTe layer was primarily used due to our previous experimental observations reported in Section 6.4. This work indicated that superior solar cells arise from device configurations with *n*-type CdTe rather than *p*-type CdTe as the bulk of the layer. The energy band diagram of this device structure is shown in Figure 6.10 (b), and a thin *p*-CdTe (~35 nm) layer was used only to fix the Fermi level closer to the valence band maximum so that a healthy band bending occurs throughout the device structure. It should be noted that the *n*- and *p*-CdTe layers were grown very close to V_i using the same bath in order to keep

the crystallinity high, remove additional interface states and therefore to minimise native defects. After growing n-type CdTe at a $V_g > V_i$, the growth voltage was simply changed to $V_g < V_i$, to grow a thin p-type CdTe layer. This doping is simply achieved by changing the stoichiometry of the layers rather than using any external doping agent.
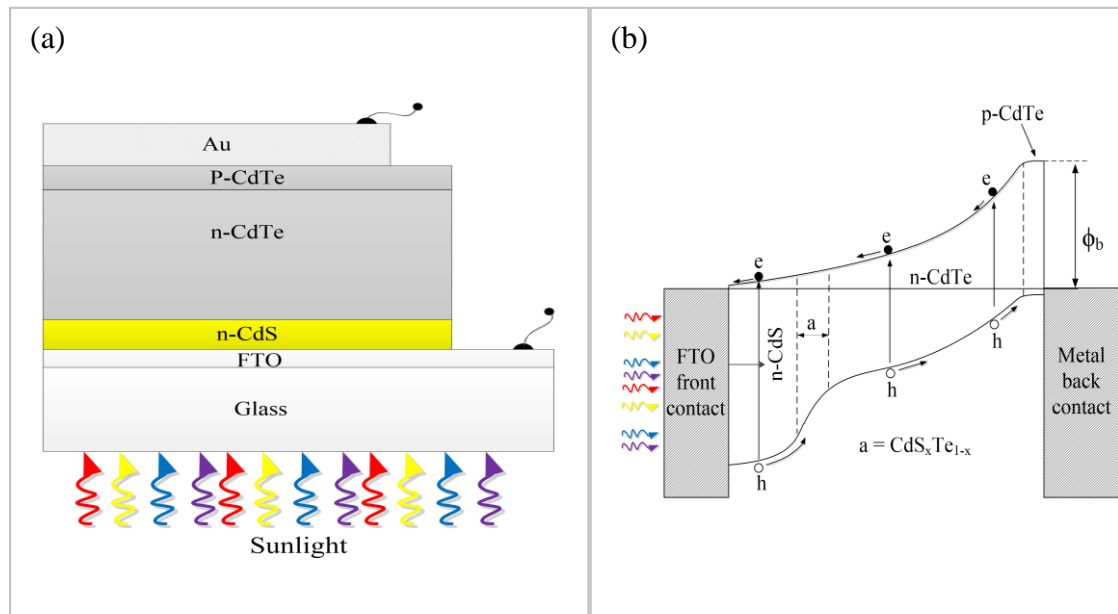
Figure 6.10: (a) Schematic diagram and (b) energy band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au thin film solar cell.

6.6.1 Results and discussion

In a typical experimental sample, about 36, 2 mm diameter Au contacts can be made. All these devices were measured using a commercially available fully automated I-V system. Solar cell measurements were carried out under AM1.5 illumination, and the system was calibrated using a standard reference cell RR267MON.
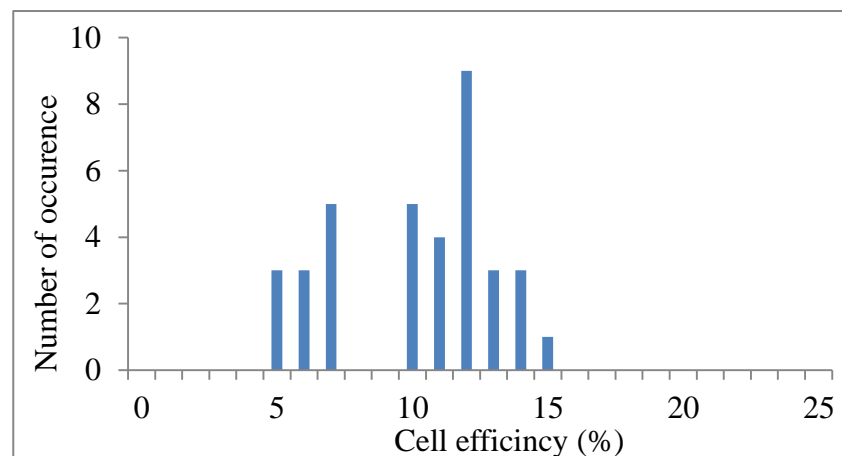
Figure 6.11: Statistics showing the cell efficiency distribution in this preliminary work.

The statistics of efficiency values are plotted in Figure 6.11, and the scatter of efficiency is wide for this preliminary work. While the work is progressing to improve reproducibility, consistency, and uniformity, the device parameters of the best device observed with the efficiency of 15.3% are studied in detail and presented in this section. Figure 6.12 shows the I-V characteristics of the best device measured under dark condition. These were plotted in both linear-linear and log-linear scales, in order to extract essential device properties, and these parameters are summarised in Table 6.6. Rectification factor (RF) at 1.00 V exceeds 4 orders of magnitude, indicating the excellent rectifying quality of this device. Potential barrier height available in this structure for electron transport is greater than 0.80 eV, but the real value is underestimated due to a large ideality factor of 1.86.
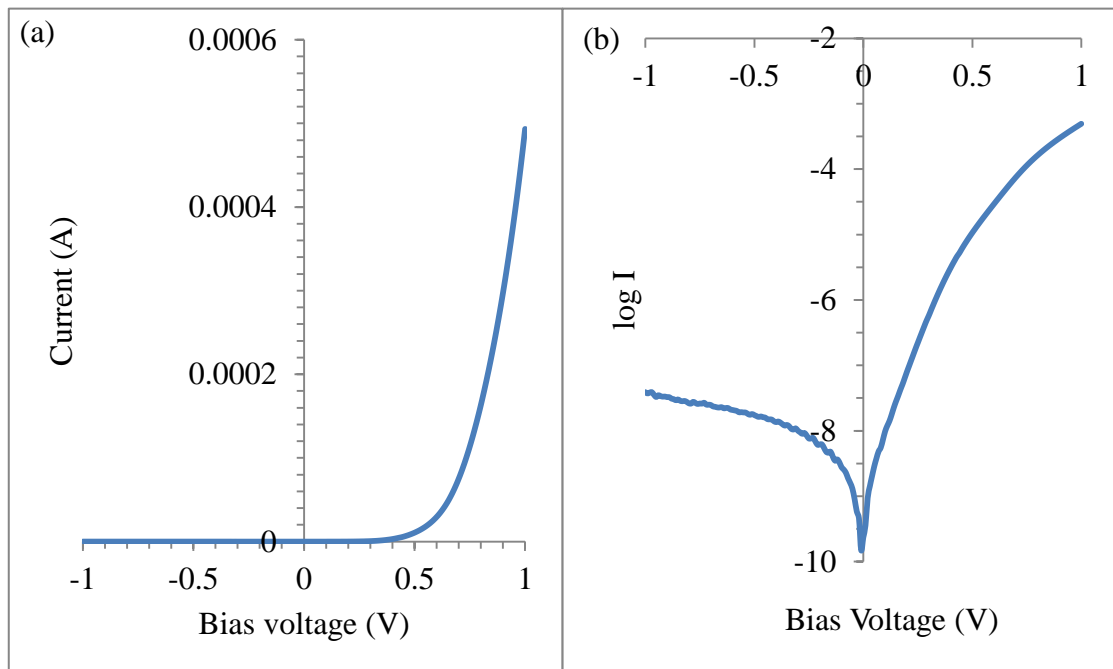
Figure 6.12: Current-Voltage curves plotted using (a) linear – linear and (b) log – linear scales for the best solar cell measured in the batch.

Table 6.6: Summary of the device parameters measured under dark condition for the highest efficiency solar cell.

RF	n	I_0(A)	φ_b(eV)	R_s(kΩ)	R_{sh}(Ω)
$10^{4.1}$	1.86	10^{-9}	>0.80	0.50	7.2×10^5

To further investigate the properties of the depletion region and the doping concentration of the material, dark C-V measurements were carried out at a signal

frequency of 1.0 MHz. Figure 6.13 shows the variation of capacitance as a function of bias voltage and corresponding Mott-Schottky plot for the highest performing device. It is clear from the shape of the C-V curve that the device is fully depleted at reverse biased and close to zero biased voltages. As the device is forward biased, and voltage is increased, the depletion width, W becomes equals to the thickness of the device which is ~1.2 μm, around a forward bias voltage of ~0.5 V. After this voltage, the capacitance varies with the increasing forward bias voltage, gradually reducing the depletion region. This variation behaves according to Mott-Schottky theory and provides estimates for V_{bi} and (N_D-N_A) for the n-CdTe layer. The data estimated are given in Table 6.7, and the V_{bi} of ~1.0 eV and (N_D-N_A) ~6.7×10^{14} cm^{-3} are most acceptable for this device. V_{bi} ~1.0 eV corresponds to a potential barrier height of ~1.10 eV and the doping concentration comes in the region corresponds to the high efficiency CdTe devices (~1.0×10^{14} - 5×10^{15} cm^{-3}) [100,241,242].
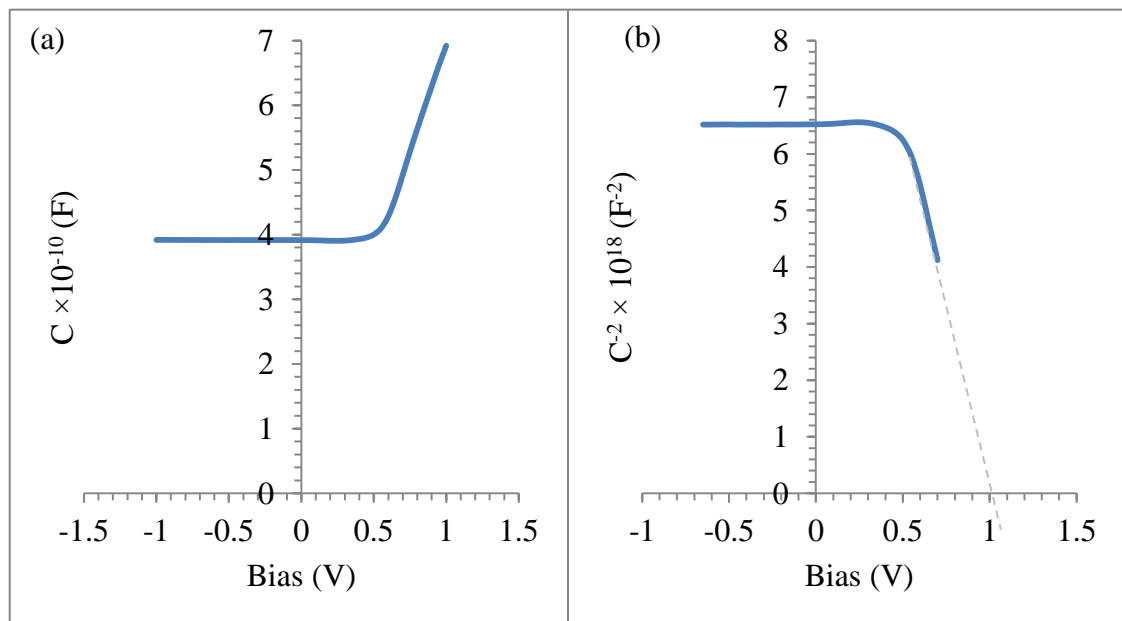
Figure 6.13: (a) Capacitance-voltage plot and (b) Mott-Schottky plot for the cell with highest conversion efficiency of 15.3%.

Table 6.7: Summary of materials and device parameters obtained for 15.3% efficiency solar cell.

Zero bias Capacitance (pF)	Geometrical Capacitance (pF)	Built-in Potential (V_{bi}) eV	Doping density (N_D-N_A) cm^{-3}
395	238	>1.00	6.67×10^{14}

Figure 6.14 (a) shows the I-V curve recorded under the AM1.5 condition for the best solar cell measured, giving V_{oc}=730 mV, J_{sc}=33.8 mAcm^{-2}, *FF*=0.62 and conversion efficiency of 15.3%. Figure 6.14 (b) shows an incident photon to charge carrier efficiency (IPCE) curve for a device with efficiency ~10% from this batch. This shows the PV active nature of these devices in the wavelength range between 300 nm and 880 nm, with a peak ~500 nm.

As indicated by the statistics shown in Figure 6.11, for these preliminary devices, it is clear that the uniformity of device parameters and consistency need improving. However, the best devices showing 15.3% efficiency for this three-layered *n-n-p* device shows the high potential of achieving further improvements in materials and processing optimisation. The series resistance of 500 Ω measured for the best device is high, and reduction of this should further improve the FF and the short-circuit current density.
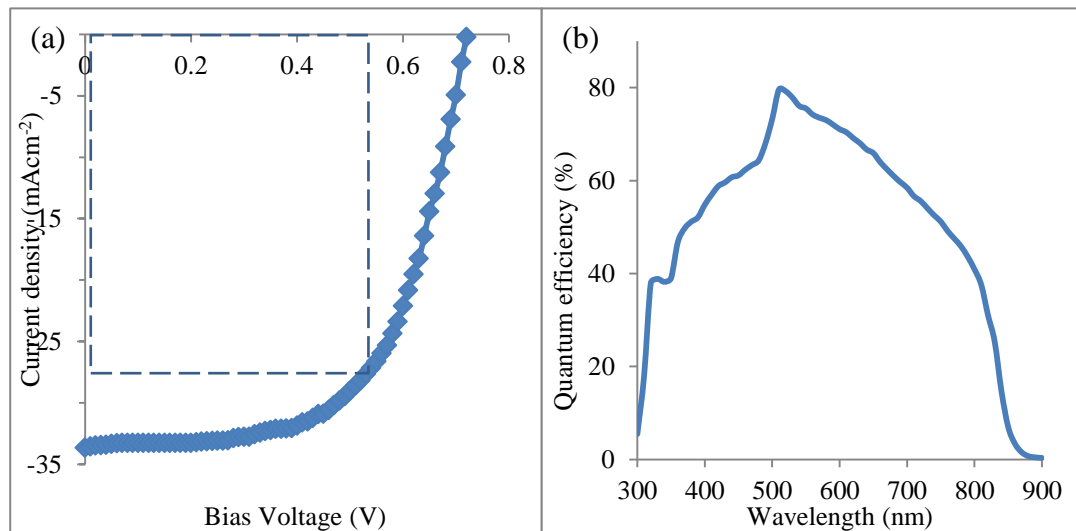
Figure 6.14: (a) I-V plot of the cell with highest efficiency under AM1.5 condition and (b) a typical IPCE curve for cells with efficiency of ~10%.

This work is only the first step towards the development of graded bandgap solar cells using only three layers. Bandgap grading takes place at only in the CdS/CdTe interface during CdCl$_2$ treatment. In view of increasing conversion efficiency and reducing the R_s copper-gold contacts were evaporated on a direct replica of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe to achieve glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Cu-Au devices. A champion efficiency of 18.5% was observed under AM1.5 conditions (see Figure 6.15 and Table 6.8). But due to instability and reproducibility issues, the results have not been published yet until the electronic parameters of the fabricated cells can be stabilised and further experimentation performed.
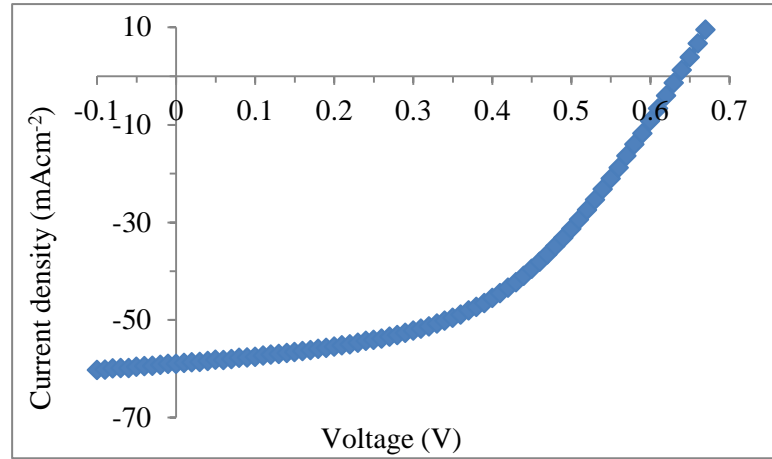
Figure 6.15: Typical I-V curve for the 18.5% conversion efficiency observed under both AM1.5 condition.

Table 6.8: Typical cell electronic property for the 18.5% conversion efficiency observed under both AM1.5 and dark conditions.

AM1.5 condition		I-V Dark condition		C-V Dark condition	
V_{oc} (V)	0.64	R_{sh} (Ω)	106	C_0 (F)	1.6×10^{-10}
J_{sc} (mAcm^{-2})	58.9	R_s (Ω)	925	V_{bi} (V)	> 0.65
FF	0.5	RF	3.5	slope C^{-2}	7.14×10^{19}
η (%)	18.5	I_o or I_s	3.16×10^{-9}	N_D (cm^{-3})	1.82×10^{14}
		n	1.68		
		Φ_b (eV)	> 0.80		

6.6.2   Summations

The work presented here successfully combined the knowledge acquired from two different research fronts; electrodeposition of semiconductors and the graded bandgap device structures. Without making any ambiguous assumptions, *n-n-p* device structures were fabricated using well studied electroplated *n*-CdS, *n*-CdTe, and *p*-CdTe layers. As expected, this preliminary study produced all PV active devices showing the best efficiency of 15.3%. Both I-V, C-V and IPCE measurements confirm promising devices capable of developing into multi-layer graded bandgap solar cells to harvest most of the photons available to achieve highest possible conversion efficiency.

6.7   Effect of fluorine doping of CdTe layer incorporated in glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au

After the structural, optical, morphological, compositional and electrical study on the CdTe layers whose baths were doped with different concentration of fluorine was completed (see Section 5.6.1), similar CdTe layers of ~1500 nm thick were grown from (0, 20 and 50) ppm F-doped baths on pre-treated glass/FTO/CdS substrate and capped with electrodeposited *p*-type CdTe from the 0 ppm F-doped bath.

The 120 nm thick CdS layer utilised in the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe configuration was electrodeposited from an electrolytic bath containing 0.03 M ammonium thiosulphate ($(NH_4)_2S_2O_3$) and 0.3 M cadmium chloride hydrate ($CdCl_2 \cdot xH_2O$) at an optimised cathodic voltage of 1200 mV based on morphological, compositional, structural, electronic and optical analysis [148]. The glass/FTO/CdS layer was $CdCl_2$ treated at 400°C in air prior to the deposition of CdTe layers. The incorporation of the *p*-CdTe layer is to force the Fermi level very close to the valence band. The schematic diagram and the band diagram of the fabricated solar cells are shown in Figure 6.16.
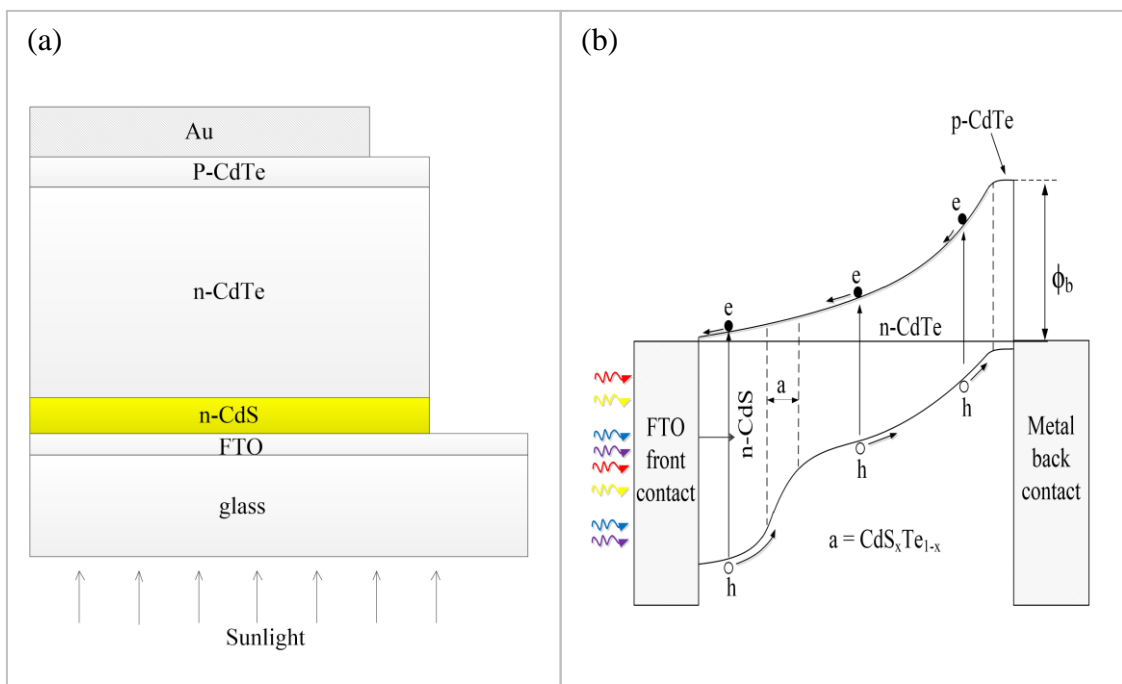
Figure 6.16: (a) Schematic diagram and (b) The band diagram of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au thin film solar cell.

It is important to note that during the $CdCl_2$ treatment of *n*-CdS/*n*-CdTe/*p*-CdTe structure, there is an inter-diffusion of Te and S which results in the formation of CdS_xTe_{1-x} intermediate material at the CdS/CdTe interface [243,244]. This intermediate

material is expected to have a bandgap between that of CdS and CdTe, thus causing a grading in bandgap between CdS and CdTe. The small bowing effects of the bandgap as reported in the literature [245] does not have considerable effect on the shape of the large band bending.

The structure (glass/FTO/n-CdS/n-CdTe/p-CdTe) was heat treated with CdCl$_2$ at 400°C for 20 min in air. The surface was etched using a solution containing K$_2$Cr$_2$O$_7$ and concentrated H$_2$SO$_4$ for acid etching and a solution containing NaOH and Na$_2$S$_2$O$_3$ for basic etching. 2 mm diameter Au contacts were evaporated at a vacuum pressure of ~10^{-4} Nm^{-2}. The glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices were analysed using both I-V and C-V characteristic measurements to determine their device parameters. Typical linear-linear and log-linear I-V curves measured under dark condition for a device incorporating CdTe from the 20 ppm F-doped CdTe bath is shown in Figure 6.17.
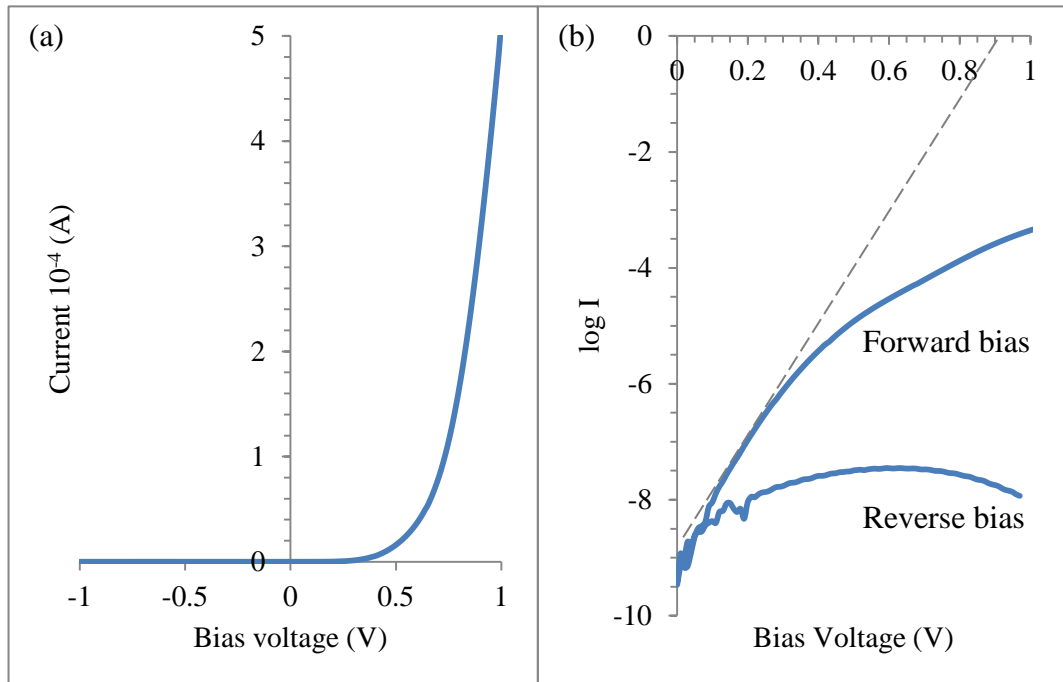
Figure 6.17: (a) Typical linear-linear I-V curve and (b) semi-logarithmic current vs. voltage curve measured under dark condition for glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices (CdTe was grown from 20 ppm doped CdTe bath).

The linear I-V curve under 1.5 AM illuminated condition is shown in Figure 6.18, the typical Mott-Schottky plot of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au layer is shown in Figure 6.19, while the device parameters are presented in Table 6.9 for comparison. The effective Richardson constant (A^*) has been calculated to be 13.22 Acm^{-2}K^{-2} for CdTe.

As observed in the dark I-V Section of Table 6.9, the shunt resistance (R_{sh}) were comparatively high across all F-doped CdTe devices but low for the 50 ppm F-doped materials. Low R_{sh} values of a solar device as explained by Soga, 2004 can be directly related to low semiconductor material quality which might be due to the inclusion of voids, gaps, high dislocation density within the semiconductor material [135]. It should be noted that R_{sh} is more dominant in low light conditions and may result in the reduction in Fill Factor (FF) and the open circuit voltage (V_{oc}) [246]. It is interesting to know that this observation correlates with the optical and morphological summaries on the CdTe material property presented in Sections 3.2 and 3.3 respectively.

The CdTe layers grown with (0, 5, 10 and 20) ppm F-doped baths show good rectification factor (RF) with values higher than three orders of magnitude, while a drastic reduction in the RF to ~ $10^{0.9}$ is recorded for device samples with a higher F-doping concentration above 20 ppm. As reported by Dharmadasa 2013, the minimum of ~10^3 RF value is sufficient for an efficient solar cell [16]. However, higher RF values show high quality rectifying property of the devices and are desirable for solar cells with very high efficiencies. The drastic reduction in the RF value can be attributed to the deterioration of the CdTe material at higher F-doping concentrations.

Furthermore, the device samples grown from baths containing 0 ppm to 20 ppm F-doping concentration shows an ideality factor (n) between 1.00 and 2.00, while higher n values are observed at higher F-doping concentration. This indicates that the current transport mechanism of devices grown from electrodeposition baths containing between 0 ppm to 20 ppm F-doping concentration is dominated by both thermionic emission and recombination & generation (R&G) processes in parallel [49]. The ideality factor value, >2.00, observed for devices grown from CdTe baths with an F-doping concentration above 20 ppm, shows that R&G process dominates the current transportation mechanism and in turn, causes a reduction in the barrier height ϕ_b as observed in Table 6.9.

Table 6.9: Device parameters from I-V (dark condition), I-V (illuminated at 1.5 AM) and C-V (dark condition) measurements.

F-doping concentration in CdTe bath (ppm)	0	5	10	20	30	50
I-V under dark condition						
R_{sh} (Ω)	~10^6	~10^6	~10^6	~10^6	~10^5	~10^3
R_s (kΩ)	0.52	2.07	5.33	0.50	2.63	0.22
log (RF)	4.8	4.4	3.2	4.2	2.2	0.9
I_o (A)	5.01×10^{-10}	3.16×10^{-10}	3.98×10^{-10}	1.58×10^{-9}	1.58×10^{-7}	7.94×10^{-6}
n	1.60	1.70	1.70	1.60	>2.00	>2.00
Φ_b (eV)	>0.82	>0.83	>0.83	>0.80	>0.67	>0.57
I-V under 1.5 AM illumination condition						
I_{sc} (mA)	0.80	0.89	0.92	1.06	1.06	1.06
J_{sc} (mAcm^{-2})	25.5	28.3	29.3	33.8	33.8	34.4
V_{oc} (V)	0.64	0.62	0.67	0.73	0.62	0.35
Fill factor	0.43	0.43	0.45	0.50	0.44	0.37
Efficiency (%)	7.01	7.56	8.83	12.32	9.21	4.37
C-V under dark condition						
$\sigma \times10^{-4}$ (Ω.cm)$^{-1}$	1.03	1.12	1.73	1.75	2.23	2.31
N_D-N_A (cm^{-3})	9.4×10^{14}	1.7×10^{14}	1.9×10^{14}	1.8×10^{14}	5.2×10^{15}	7.7×10^{16}
μ (cm^{2}V^{-1}s^{-1})	0.69	4.23	5.61	5.94	0.27	0.02

As observed in Figure 6.18 and the linear I-V curves (under 1.5 AM) Section of Table 6.9, high short-circuit current density (J_{sc}) was observed with increasing F-doping in all electrolytic baths. The observed J_{sc} value was higher than the Shockley–Queisser limit for a single *p-n* junction [20] due to the multi-layer and multi-junction *n-n-p* [232] device configuration. Further increase in the F-doping concentration above 20 ppm in the electrolytic bath shows increasing J_{sc} but also a reduction in the V_{oc}, *FF,* and the overall conversion efficiency (η).
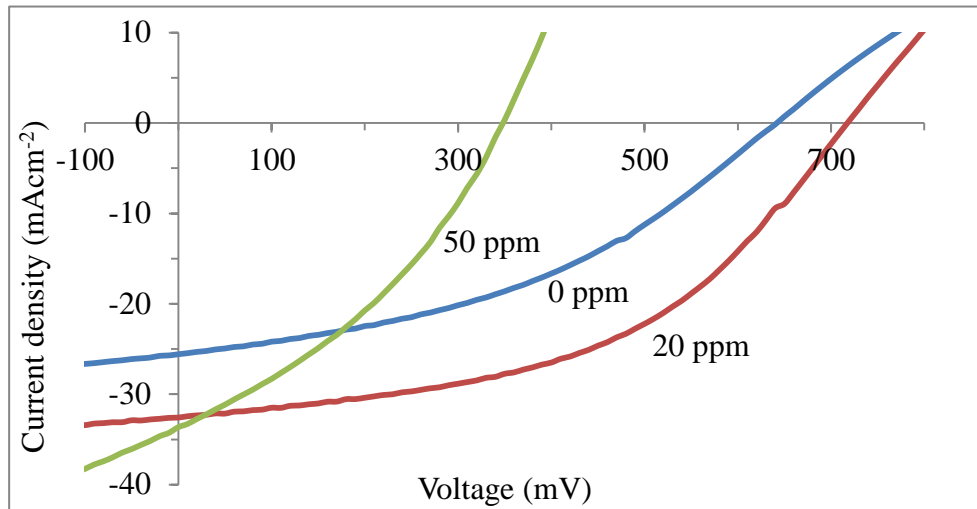
Figure 6.18: Linear I-V curves of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au under AM 1.5 for 0, 20 and 50 ppm florine doped CdTe baths.

Figure 6.19 shows a typical Mott-Schottky plot of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au layer using the 20 ppm F-doped CdTe bath for the growth of *n*-CdTe layer. The C-V measurements were performed in dark condition at a bias range of (-1.00 to 1.00) V with 1 MHz AC signal at 300 K. The built-in potential *(V$_{bi}$)*, and doping density (N_D) in this configuration were determined using the Mott-Schottky plot as shown in Figure 6.19 and described in Section 3.5.2. The carrier mobility $\mu_\perp$ was calculated with the assumption that all donor atoms (N_D) are ionised at room temperature, therefore, $n \approx N_D$ (see Equation 3.57). All the calculated parameters are shown in Table 6.9.
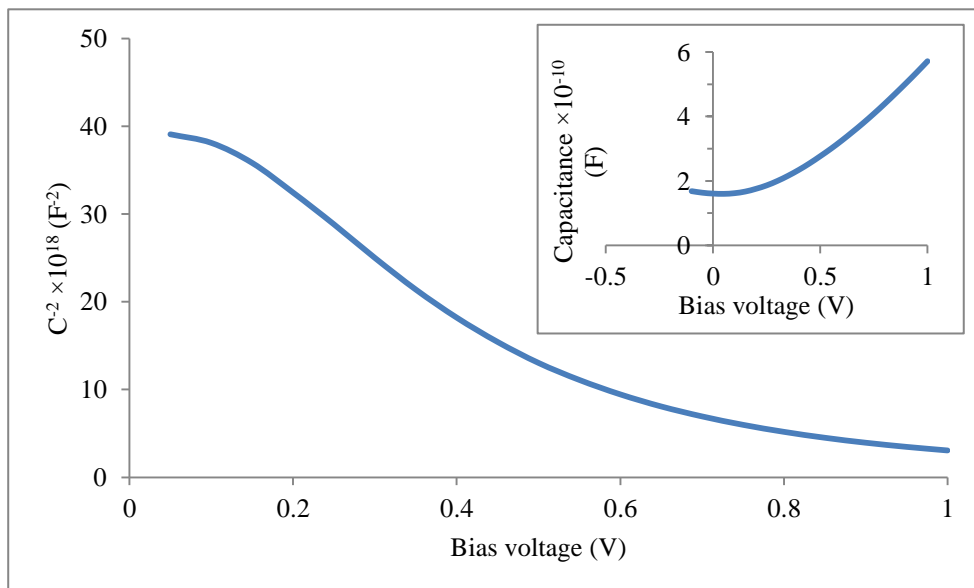
Figure 6.19: A typical Mott-Schottky plot of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au structure (the *n*-CdTe grown from 20 ppm F-doped CdTe bath). Inset shows the variation of capacitance as a function of bias voltage.

As observed in Table 6.9, the N_D for devices grown using the 0 to 20 ppm F-doping concentration was ~10^{14} cm^{-3}. An increase in the N_D to ~10^{17} cm^{-3} was observed above 20 ppm F-doping concentration. Investigation on the optimum N_D of CdTe has been reported in the literature to be ~10^{14} [15, 16, 17]. An increase in the mobility was observed within the range of 5 to 20 ppm F-doping concentration. Above this F-doping concentration range, a reduction in the mobility was observed. The reduction in mobility might be due to the presence of high concentration of defects (R&G centers) as depicted by the high ideality factor on the devices.

6.7.1   Summations

In this work, we have explored the effect of fluorine doping (in CdTe electrolytic bath) on CdTe layer as it affects it's structural, optical, morphological and compositional properties. Further investigation on the electronic property of the CdTe layer was also carried out by incorporating the layer into a glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au device configuration. An optimal F-doping concentration of ~20 ppm was observed under all material and device characterisation with a DC conductivity of 1.75×10^{-4} (Ω.cm)$^{-1}$, short circuit current density J_{sc} of 33.76 (mAcm^{-2}), doping density N_D of 1.8×10^{14}, mobility $\mu_\perp$ of 5.94 (cm^{2}V^{-1}s^{-1}) and conversion efficiency of 12.3%. These observed parameters can still be improved through more precise processing steps, improved material quality, and improved metal/semiconductor contact property amongst others. Development of multilayer graded bandgap devices is in progress towards achieving the highest possible efficiency.

6.8   Summary of the effects of fluorine, chlorine, iodine and gallium doping of CdTe

Further to the impact of F, Cl, I and Ga doping of CdTe on its material property as discussed in Section 5.6, ~1500 nm thick doped CdTe layers were incorporated in glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au. It should be noted that the optimal CdTe under all the explored doping were n-type, while the thicknesses of the *n*-CdS and *p*-CdTe were ~120 nm and ~30 nm respectively for this configuration. The processing steps and the measured electronic parameters for different dopings Cl, I and Ga were not presented in this thesis to avoid tautology following the explicit documentation for CdTe:F as presented in Section 6.6. Table 6.10 shows the summary of device parameters from I-V (dark conditions), I-V under dark and AM1.5 illuminated

conditions and C-V (dark condition) measurements incorporating F, Cl, I and Ga optimal doping of CdTe as n-CdTe.

Table 6.10: Summary of device parameters under I-V (dark conditions), I-V (AM1.5 illuminated condition) and C-V (dark condition) measurements incorporating F, Cl, I and Ga optimal doping of CdTe as *n*-CdTe in glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration.

Dopant	F	Cl	I	Ga
Opti. doping conc. (ppm)	20	1.5 M $CdCl_2$ (@ 1360 mV)	5	20
I-V under dark condition				
R_{sh} (Ω)	$>10^6$	$>10^6$	$>10^6$	$>10^6$
R_s (kΩ)	0.51	0.46	0.90	0.52
log (*RF*)	4.2	4.6	3.3	4.4
I_o (A)	1.58×10^{-9}	1.02×10^{-9}	3.16×10^{-9}	5.01×10^{-10}
n	1.60	1.60	1.80	1.61
Φ_b (eV)	>0.80	>0.81	>7.73	>0.82
I-V under 1.5 AM illumination condition				
I_{sc} (mA)	1.06	0.96	0.94	1.09
J_{sc} (mAcm^{-2})	33.76	30.57	29.94	34.71
V_{oc} (V)	0.73	0.71	0.66	0.73
Fill factor	0.50	0.56	0.5	0.57
Efficiency (%)	12.32	12.16	9.88	14.44
C-V under dark condition				
$\sigma \times10^{-4}$ (Ω.cm)$^{-1}$	1.75	1.09	2.43	1.22
N_D (cm^{-3})	1.80×10^{14}	3.90×10^{13}	6.69×10^{14}	2.01×10^{14}
μ (cm^{2}V^{-1}s^{-1})	6.07	17.45	2.27	37.83
C_o (pF)	160	280	400	170
W (nm)	1911.4	1092.2	774.2	1798.9

It should be noted that the Cl doping of CdTe was not in ppm level but rather as the precursor of the electrolyte from which CdTe was deposited. The optimum cathodic voltage is 1360 mV. As shown in Table 6.10, there is not much differences in the electronic properties of the fabricated devices except for few pointers since they all satisfy requirements of high-efficiency solar cells such as *RF* of 10^3 and above, *n* value <2.00 which signifies that the domination of the current transport mechanism by both thermionic emission and R&G. Relatively, current density J_{sc} across all the explored devices show values higher than the value for single *p-n* junction as suggested by Shockley-Queisser [20] due to the multilayer configuration of the explored devices [232]. Under AM1.5 illuminated condition, the lowest efficiency was observed with devices incorporating I-doped n-CdTe layer while the highest conversion efficiency was

recorded for the device incorporating Ga-doped n-CdTe with comparatively higher J_{sc}, *FF,* and V_{oc}. The high efficiency in the devices incorporating Ga-doped *n*-CdTe might be due to the improvement in both the material and electronic properties due to possible reduction or elimination of Te precipitation during growth which is a possible reason for the high mobility as shown in Table 6.10. It should also be noted that the comparatively low doping observed for the device incorporating Cl-doped *n*-CdTe devices might be because the *n*-CdTe layers were grown in proximity to stoichiometry as depicted in Section 5.6.2.

It is, therefore, safe to say that although there has been no clear evidence of the better devices, it could still be pointed out that Ga-doped CdTe shows the most promising electronic parameters.

6.9   Effect of cadmium chloride post-growth treatment pH

Although efficiency stagnation in the cadmium sulphide/cadmium telluride (CdS/CdTe) based solar cell has been reported in the literature for the past twenty years prior to the recent improvement in both material and processing issues, post-growth treatment (PGT) has been documented as one of the most crucial processing step towards enhancing solar to electrical energy conversion efficiency. With properties such as grain growth, recrystallisation, improved stoichiometry, grain boundary passivation, optimisation of doping concentration [157] among other advantages attributed to the PGT of CdS/CdTe, PGT has been the focus of many researchers. Research focus has been turned towards identifying the best chlorine-based gas or salt solution either in aqueous or methanol in which the highest efficiency can be achieved [30,180,194,247,248], the best application method [249] and also the optimisation of both annealing temperature and time [250]. So far, the effects of the pH values of the chlorine salt solution have been often overlooked. With an emphasis on cadmium chloride ($CdCl_2$) PGT, this set of experiments focuses on the effect of PGT solution treatment pH on both the material and device properties of CdS/CdTe-based solar cells.

6.9.1   Fabrication and treatment of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au

The initial preparation of the glass/FTO substrate (with 5×4 cm^2 dimension) was performed as described in Section 4.2.2. A 120 nm thick CdS layer was grown on the glass/FTO strip at 1200 mV cathodic voltage. After CdS deposition, the glass/FTO/CdS was rinsed in DI water, dried in a nitrogen stream and $CdCl_2$ was applied as described in Section 6.2. Within the experimental constrain of this work, stoichiometric CdTe was

observed at 1370 mV, while both the n-CdTe and p-CdTe for these set of experiments were grown at 1375 mV and 1365 mV respectively. Utilising a continuous deposition process, 1200 nm thick n-CdTe followed by a 30 nm thick p-CdTe were grown to achieve glass/FTO/n-CdS/n-CdTe/p-CdTe configuration. The incorporation of the comparatively thin p-CdTe layer was necessitated to force the Fermi level close to the valence band and also to reduce the contact resistance at the metal-semiconductor interface [100]. However, an increase in the p-CdTe thickness in this configuration causes a detrimental effect on the device parameters due to increase in defect density associated with p-CdTe layers [51]. Both the CdS and the CdTe layers were grown using optimised growth voltages explored in Chapter 4 and Chapter 5 respectively.

Post-growth-treatment commences immediately after the growth of CdTe resulting into glass/FTO/n-CdS/n-CdTe/p-CdTe configuration. The glass/FTO/n-CdS/n-CdTe/p-CdTe layer is rinsed in DI water to remove loose Cd, Te or CdTe and dried in a stream of nitrogen gas. The 5×4 cm^2 glass/FTO/n-CdS/n-CdTe/p-CdTe was cut into five strips (of the 1×4 cm^2 area) from the glass-side, rinsed thoroughly in running DI water to wash off the glass and dried in a stream of nitrogen gas. Prior to the application of CdCl$_2$ treatment, 0.1 M CdCl$_2$ was dissolved in 80 ml of DI water in a 100 ml glass beaker at room temperature. To achieve homogeneity, the solution was stirred for 60 minutes, and 20 ml of the solution was poured into 4 different 25 ml glass beaker. The beakers were labeled A to D with the solution contained in beaker A being the most acidic with a pH of 1.00±0.02, beaker B with pH 2.00±0.02, beaker C with pH 3.00±0.02 and beaker D was left as-prepared with pH of ~4.02±0.02. It should be noted that the acidity level of the CdCl$_2$ solution contained in the 25 ml beaker was adjusted using dilute HCl.

The CdCl$_2$ solution with different pH treatment was applied by adding few droplets on each strip labeled A to D at this point based on the pH of the solution in which they were treated while the fifth strip E was left as-deposited. Each strip was allowed to air dry before heat treating at 420°C for 20 minutes in air except the as-deposited strip E. Afterwards, each strip of glass/FTO/n-CdS/n-CdTe/p-CdTe layers was rinsed in running DI water, dried in stream of nitrogen gas and etched in accordance with the description made in Section 6.2. 100 nm thick gold (Au) contacts were evaporated on the glass/FTO/n-CdS/n-CdTe/p-CdTe using a 3 mm diameter mask. The fabricated devices were analysed using both current-voltage and capacitance-voltage characteristic measurements to determine their device parameters. (It should be noted that the CdCl$_2$

post-growth-treatment referred to in this section denotes $CdCl_2$ treatment and heat treatment at 420°C for 20 minutes in the air.)

6.9.2 Effect of CdCl$_2$ treatment pH on the material properties of glass/FTO/n-CdS/n-CdTe/p-CdTe layers

Optical property analysis

Further to the experimental details as discussed in Section 3.4.6, Figure 6.20 (a) shows the plot of A^2 against photon energy hv. Figure 6.20 (b) shows the graph of absorption edge slope against the $CdCl_2$ post-growth-treatment pH. The optical energy bandgap of the as-deposited and the $CdCl_2$ treated CdTe layers were obtained by extrapolating the linear portion of the curve to $A^2 = 0$. From observation, it could be said that the optical bandgap lies within the 1.45 ± 0.01 eV for the as-deposited and all the $CdCl_2$ treated CdTe layers. This observed bandgap shows comparability with the standard bulk CdTe bandgap of 1.45 eV. More importantly, the absorption edge slope as shown in Figure 6.20 (b) can be related to semiconductor layer quality as discussed in the literature [30,251]. As expected, an improvement in the absorption edge of the as-deposited glass/FTO/n-CdS/n-CdTe was observed after $CdCl_2$ treatment at different pH. This improvement in attributes has been well documented in the literature [157,194,249].
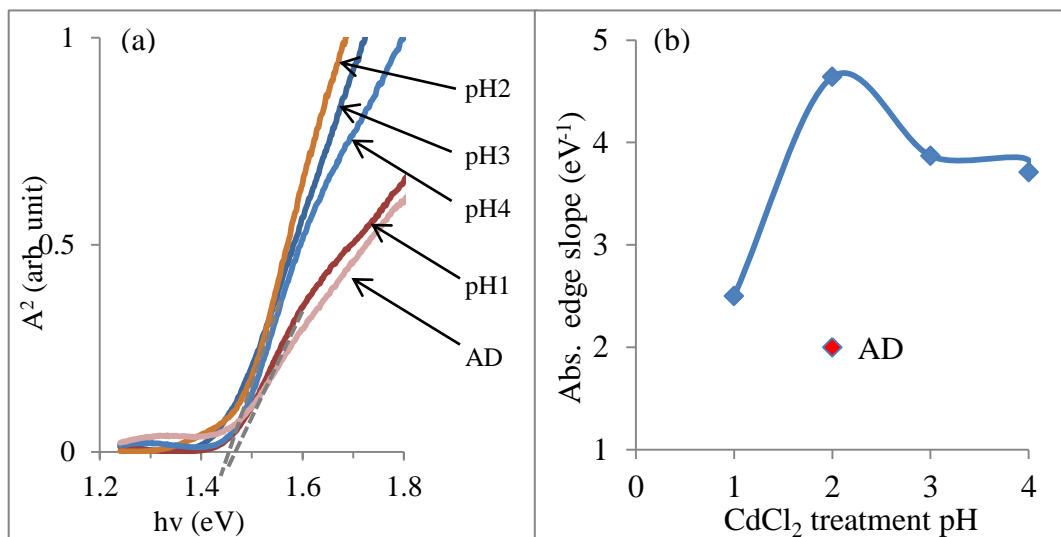
Figure 6.20: (a) Optical absorption spectra for electrodeposited glass/FTO/n-CdS/n-CdTe thin-films treated with different $CdCl_2$ at different pH values (b) absorption edge slope against PGT $CdCl_2$ pH CdTe thin films.

The steepest absorption edge slope was observed at pH2 while the lowest absorption edge slope was observed at pH1. This reduction in the absorption edge slope might be due to the reduction in the quality of the glass/FTO/n-CdS/n-CdTe layer as a result of

the harshness of the acidic $CdCl_2$ treatment by possible dissolution of Cd from CdTe at high acidity. It should be noted that only the bandgap of CdTe was observable rather than that of the incorporated n-CdS layer nor the bowing CdS/CdTe effect [252] due to the thickness of the CdTe layer.

Morphological and compositional analysis

Figure 6.21 (a), Figure 6.21 (b), Figure 6.21 (c) and Figure 6.21 (d) show the scanning electron microscope (SEM) micrographs of glass/FTO/n-CdS/n-CdTe in the as-deposited, $CdCl_2$ treated at pH1, pH2 and pH4 respectively, while, Figure 6.21 (e) and Figure 6.21 (f) show the energy-dispersive X-ray (EDX) spectra of point identification on the glass/FTO/n-CdS/n-CdTe treated with pH1 $CdCl_2$ solution. The layer treated with pH3 $CdCl_2$ was excluded due to its high comparability of morphological properties with pH4. The as-deposited glass/FTO/n-CdS/n-CdTe layer as depicted in Figure 6.21 (a) shows cauliflower-type morphology which is formed by the agglomerations of small grains. Most importantly, full coverage of the underlying glass/FTO/n-CdS layers was observed.

After CdTe treatment at all the explored pH in this work, an increase in grain growth was observed, which is in accord with the literature. The layers treated with pH2 $CdCl_2$ showed a slightly bigger grain size as compared to the layers treated with pH4 $CdCl_2$ as shown in Figure 6.21. The glass/FTO/n-CdS/n-CdTe layers treated with pH1 $CdCl_2$ as illustrated in Figure 6.21 (b) show deterioration of the glass/FTO/n-CdS/n-CdTe layer with the presence of pinholes and the accumulation of non-uniform strands on the grains.

With further investigation on the composition of the strands using EDX as shown in Figure 6.21 (e) and Figure 6.21 (f), it was observed that the strands show an atomic composition of 75.6% for Te and 24.4% for Cd. The presence of the Te-rich strands has also been documented in the literature [253,254], and it is well known that an introduction of an acidic media to CdTe attacks Cd preferentially leaving rich Te surface [61,255]. The unidentified EDX peaks in Figure 6.21 (e) and Figure 6.21 (f) at ~(2.5, 3.5 and 4.5) keV are for S, Cd and Te respectively [188,256]
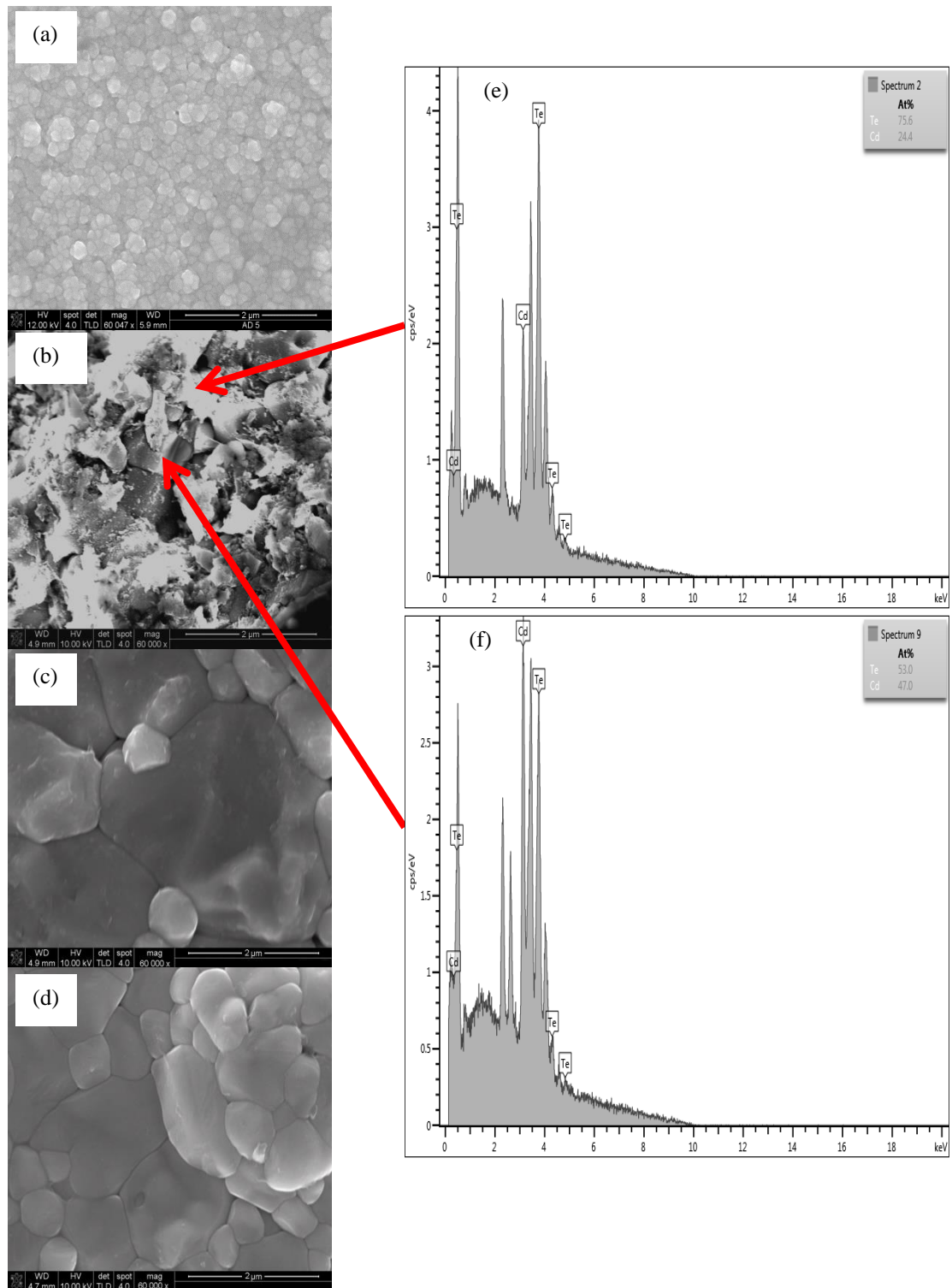
Figure 6.21: (a) SEM micrograph of as-deposited *n*-CdTe grown on glass/FTO/*n*-CdS, (b-d) SEM micrographs for glass/FTO/*n*-CdS/*n*-CdTe layers treated with PGT treated with CdCl$_2$ at pH1, pH2 and pH4 respectively, while (e-f) are the EDX point micrograph on layers treated at pH1.

This observation signifies the detrimental effect of pH1 $CdCl_2$ for post-growth-treatment on the material quality of the glass/FTO/n-CdS/n-CdTe all-electrodeposited layers and may result in the reduction in the device quality.

Figure 6.22 shows the graph of Cd/Te atomic composition against the acidity of the $CdCl_2$ PGT of glass/FTO/n-CdS/n-CdTe on a 6×6 μm^2 area obtained using EDX. As shown in Figure 6.22, reduction in the atomic concentration of Cd with respect to AD material was observed after $CdCl_2$ treatment at all the pH explored. The reduction in the Cd atomic concentration and shift towards 1:1 ratio of Cd to Te can be attributed to $CdCl_2$ treatment at favourable pH [157]. At pH1, an increase in the Te atomic concentration was observed due to harsh effect of highly acidic $CdCl_2$ on elemental Cd. This observation can be related to the Te-richness obtained after wet acid etching of CdTe layer as reported in the literature [61].
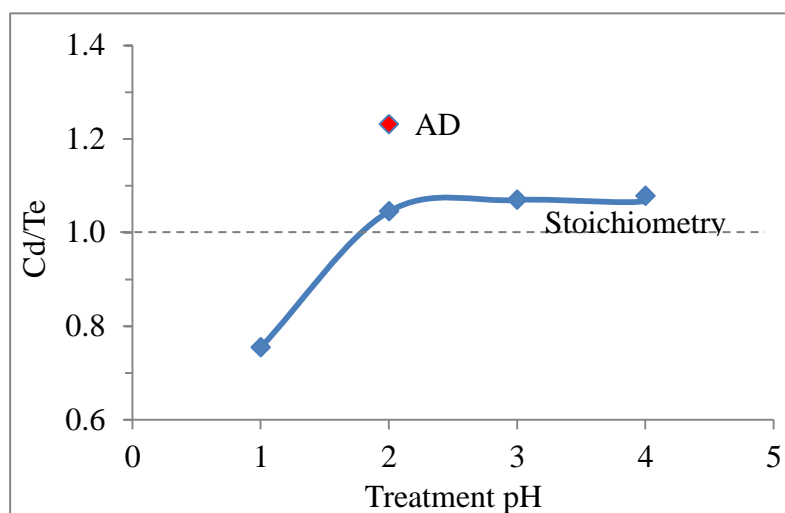
Figure 6.22: Graphical representation of percentage atomic composition ratio of Cd to Te atoms for $CdCl_2$ treated CdTe layer after different PGT pH as obtained from EDX micrographs.

Structural analysis

The analysis was aimed at identifying the effect of $CdCl_2$ post-growth-treatment pH on XRD peak intensity, crystallinity, crystallite size, preferred phase and orientation of the glass/FTO/n-CdS/n-CdTe layers. Figure 6.23 (a) shows the graph of XRD diffraction intensity of the glass/FTO/n-CdS/n-CdTe layers treated at different $CdCl_2$ pH against 2θ angle. Figure 6.23 (b) shows the graph of XRD peak intensity and crystallite size against the $CdCl_2$ post-growth-treatment pH. It should be noted that the stacked XRD micrographs as presented in Figure 6.23 (a) are to aid the comparability of the peak intensity. From observation, XRD peaks associated with CdTe in their cubic phase

((111)C, (220)C, (311)C) were observed at angle $2\theta \approx 23.8$, $2\theta \approx 38.6°$ and $2\theta \approx 45.8°$ respectively, asides the FTO peaks at $2\theta = 25.42$, $2\theta = 33.11$, $2\theta = 36.57$, $2\theta = 55.06$, $2\theta = 61.12$ and $2\theta = 65.06$ at all the $CdCl_2$ pH treatment explored.
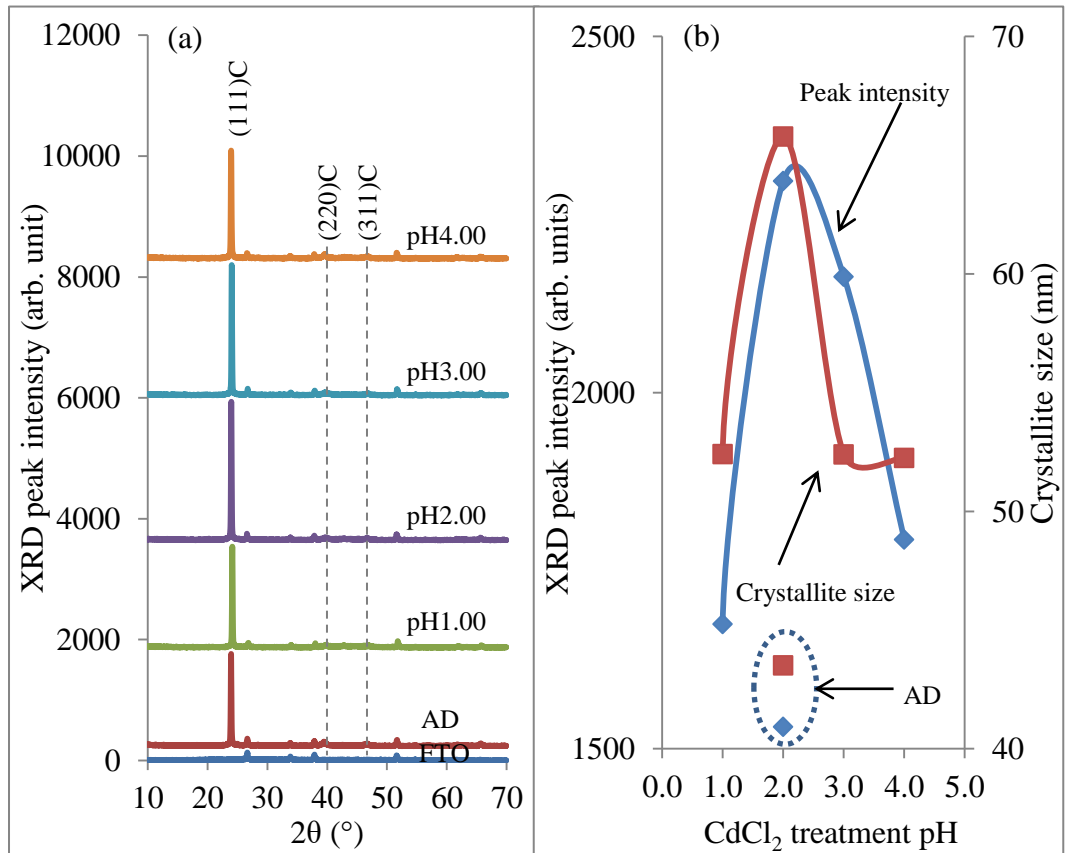
Figure 6.23: (a) Typical XRD patterns of glass/FTO/n-CdS/n-CdTe layers treated at different $CdCl_2$ pH value (b) typical plot of CdTe (111) cubic peak intensity and crystallite size against $CdCl_2$ post-growth treatment pH value.

As shown in Figure 6.23 (a), it is clear that the preferred orientation of CdTe at all the pH explored is along the cubic (111) plane based on the intensity of its diffraction. Furthermore, an increase in diffraction intensity of the (111)C peak was observed with increasing $CdCl_2$ post-growth-treatment pH. The highest diffraction intensity observed at pH2 and the lowest intensity observed at pH1 as shown in Figure 6.23 (b). This detrimental effect can be further related to harsh etching and sublimation of the CdTe surface, the formation of pinholes, voids, and the formation of a CdTe layer rich in Cd or Te with competing phases with CdTe. From observation, no elemental Cd and Te peaks were observable in Figure 6.23 (a) which might be due to possible overlap with the FTO peaks, although the formation of elemental Te is most likely as suggested by the compositional analysis as will be discussed later in this section. Based on the

preferred cubic (111) CdTe peaks, the crystallite size was calculated using Scherrer's equation addressed in Section 3.4.2 and Equation 3.8.

Table 6.11 shows the calculated crystallite size and other related properties as obtained from XRD diffraction. From observation, the minimum value of the FWHM and the maximum crystallite sizes were attained at pH2. Away from this pH value, a gradual increase in the FWHM and decrease in the crystallite size was observed. This shows further superior quality of $CdCl_2$ post-growth-treatment at pH2 as compared to the other pH values explored. It should be noted that the extracted XRD data from this CdTe work matches the International Center for Diffraction Data (JCPDS) reference file No. 01-775-2086.

Table 6.11: The XRD analysis of glass/FTO/n-CdS/n-CdTe layers treated with $CdCl_2$ at different pH values.

Sample	2θ (°)	Lattice Spacing (Å)	FWHM (°)	XRD Peak intensity	Crystallite Size D (nm)	Assignments
AD	23.95	3.716	0.195	1531	43.52	Cubic
pH1.00	24.15	3.681	0.162	1675	52.41	Cubic
pH2.00	23.99	3.707	0.129	2297	65.79	Cubic
pH3.00	24.05	3.696	0.162	2163	52.40	Cubic
pH4.00	23.95	3.7149	0.162	1794	52.26	Cubic

Photoelectrochemical (PEC) cell study

For this experiment, 1200 nm thick n-CdTe was grown at 1370 mV on 4×5 cm^2 glass/FTO. This experiment was performed to ascertain the effect of $CdCl_2$ post-growth-treatment at different pH on the conductivity type of the n-CdTe layer utilised in this work. After growth, the glass/FTO/n-CdTe layer was cut into five 1×5 cm^2 pieces and treated with $CdCl_2$ at different pH prior to heat treatment at 420°C for 20 minutes as described in Section 6.9.1. Figure 6.24 shows the graph of PEC signal against as-deposited and post-growth-treated n-CdTe at different pH values. As observed from Figure 6.24, the conductivity type of the as-deposited n-CdTe was retained after $CdCl_2$ treatment at pH2, pH3 and pH4 explored in this work with a slight shift towards the opposing conductivity type except for the layers treated with $CdCl_2$ at pH1. The glass/FTO/n-CdTe layer treated with pH1 shows a conductivity type transition into p-type. It should be noted that conductivity type conversion after $CdCl_2$ treatment may be due to doping effect caused by heat treatment temperature, duration of treatment, initial

atomic composition of Cd and Te, the concentration of $CdCl_2$ utilised in treatment, defect structure present in the starting CdTe layer and the material's initial conductivity type as documented in the literature [152,157,170,180]. Based on these observations, coupled with the analysis on composition as discussed earlier in this section, it could be said that the compositional alteration of the initial n-CdTe after pH1 $CdCl_2$ treatment might be one of the determining factors in the conductivity type conversion of the CdTe layers explored in this work. This observation is in accord with the compositional analysis discussed earlier.
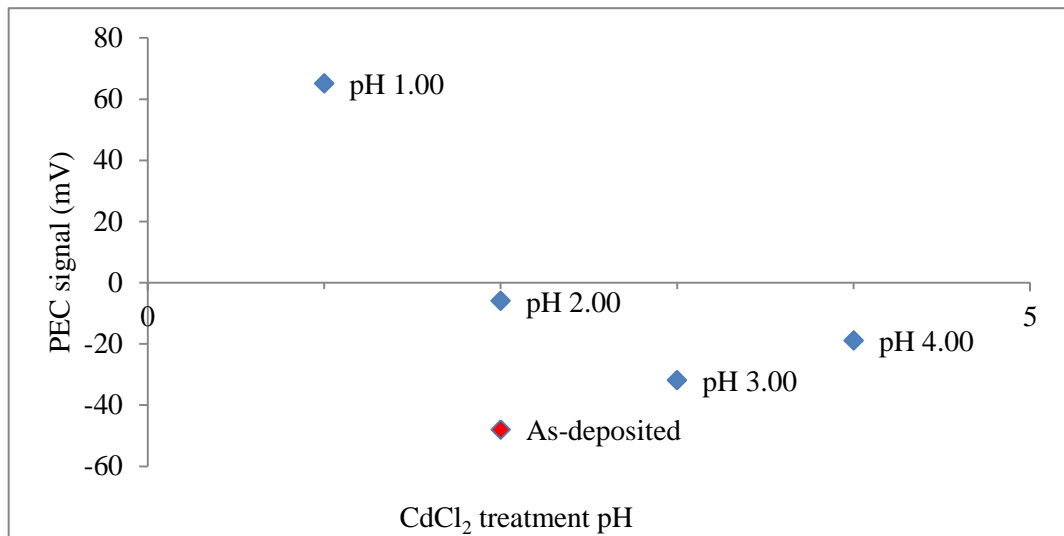
Figure 6.24: PEC signals for glass/FTO/n-CdTe layers treated with $CdCl_2$ at different pH values.

DC conductivity study

For this experiment, a 1200 nm thick n-CdTe layer was grown on glass/FTO, treated with $CdCl_2$ at different pH after growth and heat treated at 420°C for 20 minutes. On the basis of conductivity type as discussed under PEC cell measurement section, gold (Au) contacts were evaporated on the glass/FTO/p-CdTe layers, while indium (In) was evaporated on the glass/FTO/n-CdTe to form Ohmic contacts prior to the I-V characterisation of the fabricated cells. From the I-V curve generated using Rera Solution PV simulation system, the resistance was calculated as the inverse of the I-V slope and resistivity was calculated as described in Section 3.4.8.

Table 6.12 shows the tabulation of properties of the CdTe layers grown on glass/FTO layers and Figure 6.25 is an illustration of conductivity and resistance against $CdCl_2$ treatment pH. It was observed that an increase in the acidity of the $CdCl_2$ post-growth-

treatment solution increases the conductivity of the CdTe layer with saturation observed at ~pH2.

Table 6.12: Summary of electrical properties of glass/FTO /n-CdTe layers after CdCl$_2$ treatment at different pH values.

pH	Resistance R (Ω)	Resistivity ρ $\times 10^4$ ($\Omega \cdot$cm)	Conductivity σ $\times 10^{-5}$ ($\Omega \cdot$cm)$^{-1}$
1.00	42.6	1.12	8.97
2.00	9.4	0.25	40.63
3.00	11.3	0.30	33.80
4.00	15.7	0.41	24.33

Increase in the acidity above pH2 shows a reduction in the conductivity which might be due to the p-type conductivity as observed after pH1 CdCl$_2$ treatment as compared to the n-type conductivity as observed after pH2, pH3 and pH4 treatment (see PEC cell measurement result). It is well known that the conductivity and mobility of an n-type semiconductor material are higher than its p-type counterpart [222]. Furthermore, reduction in the conductivity of the CdTe layer might also be due to CdTe layer deterioration as discussed earlier in this section.
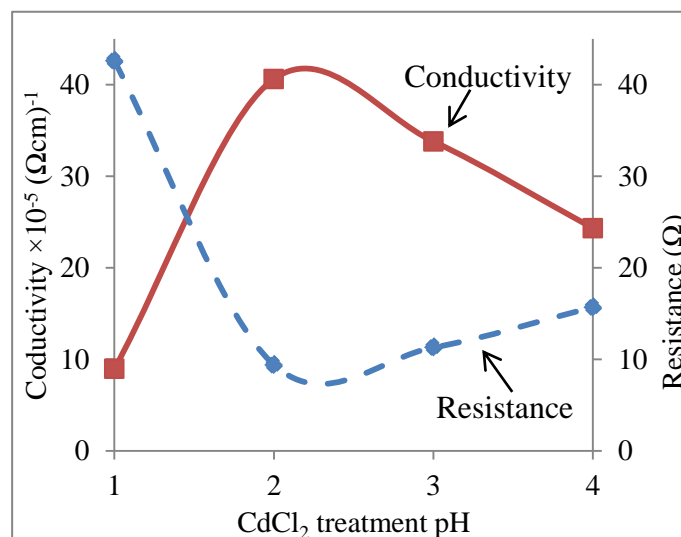
Figure 6.25: Typical graphs of electrical conductivity and resistance against PGT CdCl$_2$ pH value.

6.9.3   The effect of CdCl$_2$ treatment pH on solar cell device parameters

After the optical, morphological, structural and photoelectrochemical properties of the CdTe layers had been analysed, glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices were fabricated as discussed in Section 6.9.1.

Current-voltage characteristics with rectifying contacts

The I-V measurements for the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices were performed under both dark and AM1.5 illuminated conditions. Figure 6.26 (a) shows a typical band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au thin film solar cell, while, Figure 6.26 (b) and Figure 6.26 (c) show both the linear-linear and log-linear I-V curve of the pH2 CdCl$_2$ treated glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices respectively. Figure 6.26 (d) shows the I-V curves taken under AM1.5 illumination condition for the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices treated with different pH of CdCl$_2$. While Table 6.13 shows the summary of the electronic properties of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices fabricated. From the I-V data obtained under dark condition, electrical properties such as the shunt resistance R_{sh}, series resistance R_s, rectification factor RF, reverse saturation current I_o, ideality factor n, and the barrier height ϕ_b were derived, while the effective Richardson constant (A^*) for CdTe was calculated using Equation 3.31. As observed in Table 6.13, the R_{sh} was comparatively high for all the pH values explored in this work, but a noticeable reduction of about two orders of magnitude was observed at pH1.

It is well known that low R_{sh} can be attributed to the low quality of the semiconductor material [135] which might be due to the inclusion of gaps, voids, pinholes, high dislocation density within the semiconductor layer [135]. Based on this, it can be deduced that the semiconductor material quality at pH1 has been reduced. Interestingly, this observation is in accord with the analytical studies as discussed earlier in Section 6.9.2. Furthermore, the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device activated using CdCl$_2$ at pH2, pH3 and pH4 show *log RF* values of above 3 with a tendency for achieving highly efficient solar cells [16]. On the contrary, the low *log RF* values observed for glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device activated using CdCl$_2$ at pH1 shows a lower *log RF* value of 1.27 which indicates the inability of the fabricated device to achieve high efficiencies. This observation might be due to the dominance of the current transport mechanism by recombination and generation (R&G) centers as indicated by an *n* value >2.00.
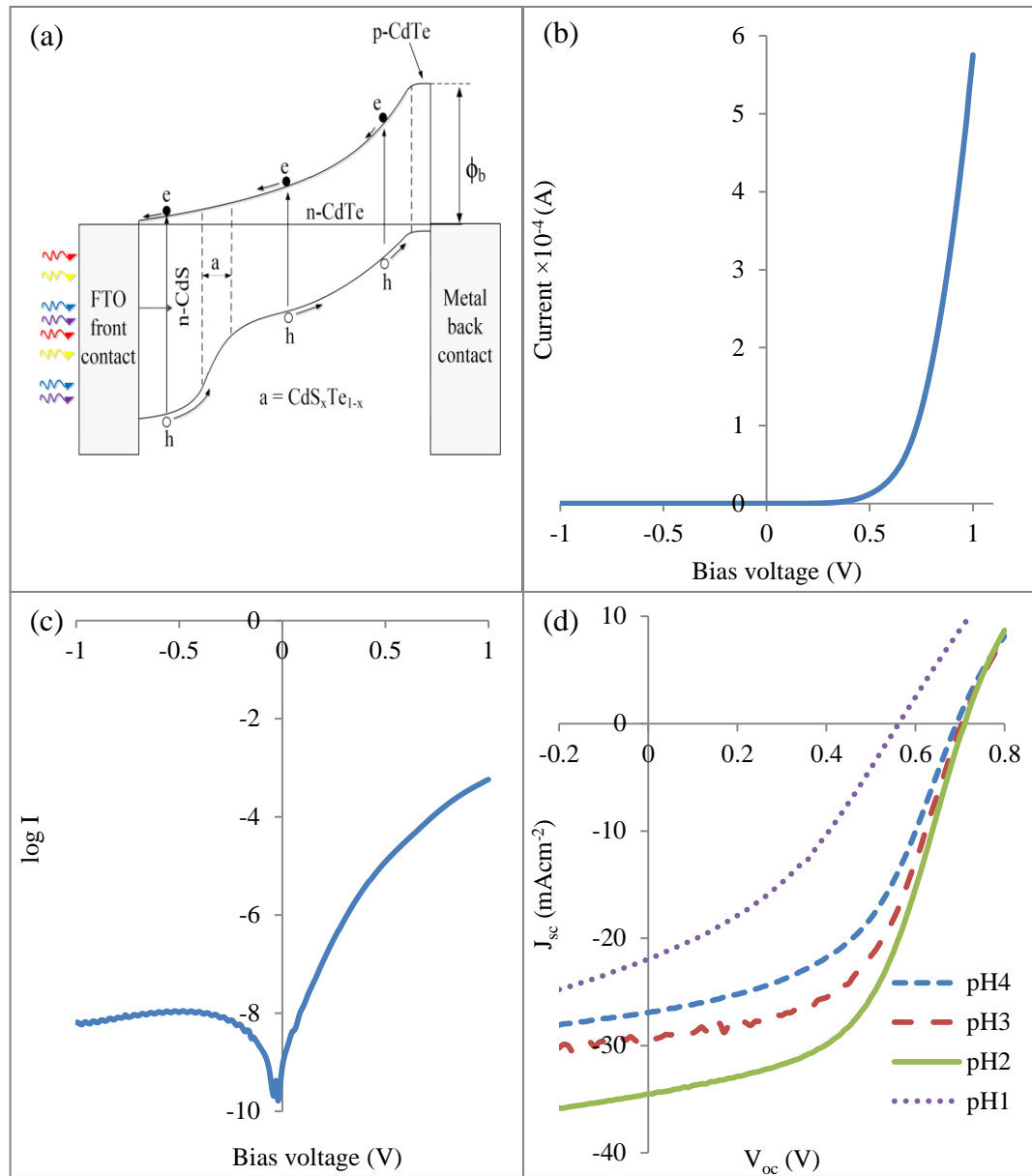
Figure 6.26: (a) The band diagram of the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au thin film solar cell (b) Typical linear–linear I–V curve and (c) semi-logarithmic current versus voltage curve measured under dark conditions for glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au devices. (the layers were treated with pH2 CdCl$_2$). (d) Linear I–V curves of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au under AM 1.5 for devices treated with CdCl$_2$ at different pH values.

It should be noted that for an ideal diode, the ideality factor *n* is 1.00 indicating the dominance of the current transport mechanism by thermionic emission. But if the ideality factor falls between 1.00 and 2.00, the current transport mechanism is dominated by both thermionic emission and R&G centers. As reported by Verschraegen et al., the current transport mechanism of a diode with an ideality factor above 2.00 is

dominated by high-energy electrons tunneling through the barrier in addition to both thermionic emission and R&G mechanisms [137]. The current transport mechanism of $n>2.00$ might result in barrier height ϕ_b reduction as observed in Table 6.13 for the pH1 $CdCl_2$ activated the device.

Table 6.13: Summary of Device parameters from I–V characteristics under dark and illuminated (at AM1.5) conditions and C–V measurements under dark conditions.

CdCl$_2$ post-growth treatment pH	1.00	2.00	3.00	4.00
I-V under Dark condition				
$R_{sh} \times 10^5$ (Ω)	0. 08	10.13	5.72	5.28
$R_s \times 10^3$ (Ω)	1.27	0.47	0.87	0.89
log RF	1.40	4.80	3.50	3.50
$I_o \times 10^{-9}$ (A)	158.49	1.00	3.98	3.16
n	>2.00	1.60	1.86	1.91
Φ_b (eV)	>0.67	>0.80	>0.77	>0.77
I-V under AM1.5 illuminated condition				
J_{sc} (mAcm^{-2})	21.66	35.03	29.62	27.39
V_{oc} (V)	0.58	0.72	0.71	0.70
FF	0.40	0.52	0.55	0.52
η (%)	5.00	13.10	11.60	10.00
C-V under dark condition				
$\sigma \times 10^{-5}$ (Ω.cm)$^{-1}$	8.97	40.63	33.80	24.33
$N_D \times 10^{14}$ (cm^{-3})	254.00	1.95	3.66	6.67
μ (cm^{2}V^{-1}s^{-1})	0.02	13.00	5.76	2.28

Under AM1.5 condition as shown in Figure 6.26 (d) and Table 6.13, the observed J_{sc} of the cell treated using pH1 CdTe post-growth-treatment is relatively lower than that of the devices made using pH2, pH3, and pH4. This observation can be related to the high ideality factor as a result of high R&G center intensity. It should be noted that the J_{sc} observed in this work is higher than the Shockley–Queisser limit of a single p–n junction [20] due to the multi-layer and multi-junction n–n–p device configuration [232]. The explored glass/FTO/n-CdS/n-CdTe/p-CdTe/Au cells were isolated by carefully removing surrounding materials to ensure that there was no peripheral collection as suggested by Godfrey et al. [69]. Using the multilayer configuration, the

SHU group has reported 140% IPCE measurement value owing to the incorporation of impurity PV effect and impact ionisation [22], while, other independent researchers have also report EQE values above 100% [257,258]. Comparatively, similar V_{oc} was observed for glass/FTO/n-CdS/n-CdTe/p-CdTe/Au layers treated with CdCl$_2$ at pH2 to pH4 while a reduction in the V_{oc}, FF, and η of the layers treated with pH1 CdTe was observed. These observations were anticipated due to the degradation of the material quality, reduction in crystallinity, conductivity type transition and high resistivity based on the analysis presented in Section 6.9.2.

Capacitance-voltage characteristics of rectifying contacts

Figure 6.27 (a) and Figure 6.27 (b) show the capacitance-voltage (C-V) and the Mott-Schottky (C^{-2} versus V) plot of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device respectively with pH2 CdCl$_2$ treated CdTe layers. The properties such as the doping density N_D and mobility μ for glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices treated with pH1 to pH4 are tabulated in Table 6.13. For this sets of experiments, the measurements were carried out at a frequency of 1.0 MHz, between the bias voltage range of -1.00 V to 1.00 V at 300 K. The reported doping density N_D in this work was obtained using the Mott-Schottky plot as described in Section 3.5.2. The ε_r value was taken to be 11 [145], while, the slope obtained from the intercept of the Mott-Schottky plot as shown in Figure 6.27 (b).
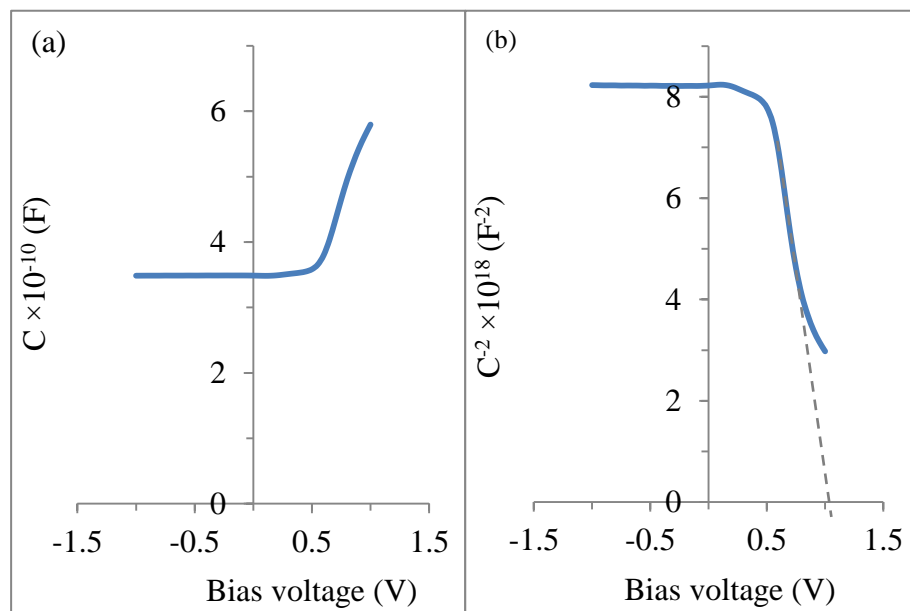
Figure 6.27: A typical (a) Capacitance-voltage and (b) Mott-Schottky plot of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au layer treated with pH2 CdCl$_2$.

Using Equation 3.53 the effective density of states N_c was calculated to be 9.15×10^{17} cm^3, where h is the Plank's constant, m_e^* is the effective electron mass, T is the temperature at 300 K, and k is the Boltzmann's constant. The electron mobility $\mu_\perp$ was calculated using Equation 3.57.

As observed in Figure 6.27, the fabricated devices treated with CdCl$_2$ at pH2 was fully depleted at the reverse bias through the zero voltage and towards ~0.5 V in the forward bias with the depletion width W equalling the fabricated device thickness of ~1350 nm. Increasing the voltage in the forward bias to ~0.5 V and above, a gradual reduction in the depletion width was observed with a corresponding increase in capacitance. This observation was similar for glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices treated with CdCl$_2$ at pH3 and pH4. Furthermore, the calculated N_D (see Table 6.13) for the devices treated with CdCl$_2$ at pH2 - pH4 are of the same order of magnitude (10^{14} cm^{-3}). High-efficiency solar cells have been reported to have N_D values within the (~1.0×10^{14} – 5×10^{15} cm^{-3}) [259,260]. The N_D value of the devices activated with CdCl$_2$ at pH1 signifies high doping which might result in a loss of J_{sc}, incorporation of defects within the crystal lattice, shrinkage of the depletion width and the consequent reduction in the photo-generated current collection efficiency [261]. These observations coupled with the high defect density (R&G) centers might be the cause of the reduction in the charge carrier mobility of the devices activated with pH1 CdCl$_2$ as compared to pH2 – pH4 CdCl$_2$ treatment.

6.9.4   Summations

In conclusion, this experimental work has explored the effect of CdCl$_2$ post-growth-treatment pH on both material and fabricated CdS/CdTe device properties. It was observed that better material and device properties could be achieved at pH2 CdCl$_2$ activation treatment. Although the device parameters such as the V_{oc} show no distinct difference after treatment with pH2 to pH4 CdCl$_2$, the CdCl$_2$ treatment at pH1 shows low-quality material quality as observed in the structural, morphological and compositional properties while the overall fabricated device photon-to-electron efficiency was low.

6.10 Effect of the inclusion of gallium in the normal CdCl$_2$ treatment o of CdS/CdTe-based solar cells

Post-growth treatment (PGT) has been considered as an integral part of achieving highly efficient solar cells [157]. This is justified by recrystallisation and grain growth,

optimisation of electrical conductivity and doping concentration, passivation of grain boundaries, optimisation of the CdS/CdTe interface morphology, improvement in Cd:Te stoichiometric composition, reduction of Te precipitation amongst other advantages observed after PGT in the presence of some halogen based salts and gases [30,44,180,262,263]. As documented in the literature, it is challenging to avoid the presence of Te precipitates completely in CdTe by modifying the growth technique, growth process or post-growth treatment [183,192,264]. The inclusion of gallium in the normal $CdCl_2$ treatment of CdTe is due to its unique property of dissolving Te-richness in CdTe material as suggested in the literature [181,192].

6.10.1 Effect of the inclusion of gallium in the normal $CdCl_2$ treatment on the material property of CdS/CdTe-based solar cell

Optical absorption analysis

Figure 6.28 (a) shows the optical absorption curves and Figure 6.28 (b) shows the plot of absorption edge slopes and bandgaps against the AD, CCT and GCT - glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers, while the numerical values are shown in Table 6.14. As observed in Figure 6.28 (a) and Figure 6.28 (b), the bandgaps of all the AD, CCT and GCT layers fall within the CdTe bulk bandgap range of (1.45 to 1.50) eV [28], even for the as-deposited layers without any PGT to modify its optical parameters. Although there were no clear differences in the bandgap due to the material quality of the as-deposited CdTe layer, the difference in the absorption edge is clearly observed in Figure 6.28 (b).
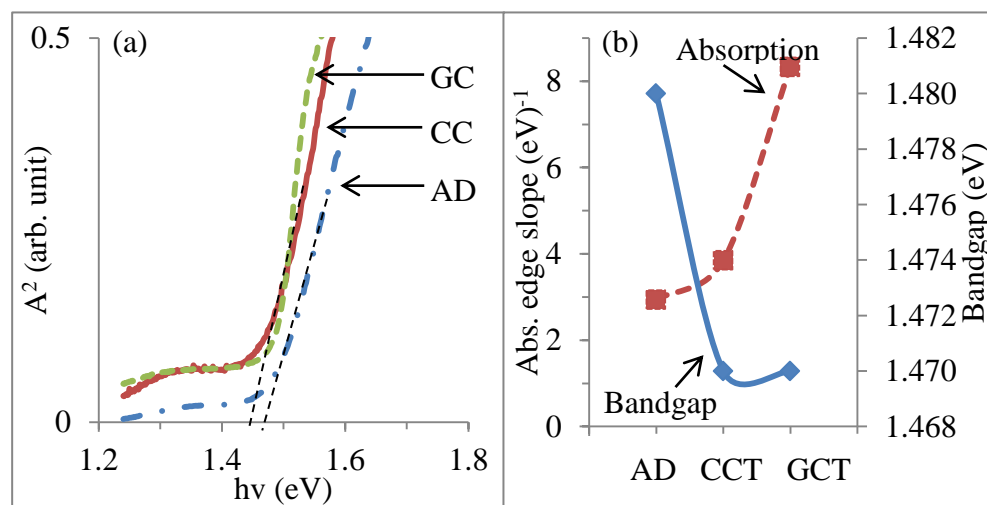
Figure 6.28: Graphs of (a) Square of absorption against photon energy and (b) Optical bandgap and slope of absorption edge against treatment conditions for AD, CCT and GCT - glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers.

It is well documented in the literature that the sharpness of the absorption edge signifies superior semiconductor layer optical property based on lesser impurity energy levels and defects in the thin film [28,30,125]. Based on this submission, it could be interpreted that the layer with the superior optical quality is the GCT layer and the least is the as-deposited CdTe layer. It is interesting to observe an inverse relationship (see Figure 6.28 (b)) between the bandgap and the absorption edge slope which further buttresses the GCT - glass/FTO/n-CdS/n-CdTe/p-CdTe material superiority.

Table 6.14: Summary of the effect of different treatments on bandgap and the slope of absorption edges.

Sample	Bandgap (eV)	Absorption edge slope (eV^{-1})
AD	1.48	2.94
CCT	1.47	3.85
GCT	1.47	8.33

Morphological analysis

Figure 6.29 (a), Figure 6.29 (b) and Figure 6.29 (c) show the morphology of AD, CCT and GCT - glass/FTO/n-CdS/n-CdTe/p-CdTe thin films. As observed in Figure 6.29, the underlying substrates are fully covered by the CdTe layer before and after different treatments.

The as-deposited glass/FTO/n-CdS/n-CdTe/p-CdTe layer shows agglomeration of small crystallites to form cauliflower-like larger grains. After post-growth treatment such as CCT and GCT, grain growths within the range of (100 to 2000) nm and (200 to 2600) nm were observed respectively. The influence of $CdCl_2$ in PGT of CdTe has been explicitly explored in the literature as it affects the improvement of material and device quality of CdTe-based solar cells [30,157,180]. Further improvements in grain size can be observed in morphological property of the GCT treated glass/FTO/n-CdS/n-CdTe/p-CdTe layer as shown in Figure 6.29 (c) as compared with the CCT in Figure 6.29 (b) in this work. This improvement signals the positive effect of the inclusion of Ga in the usual CCT of CdTe.
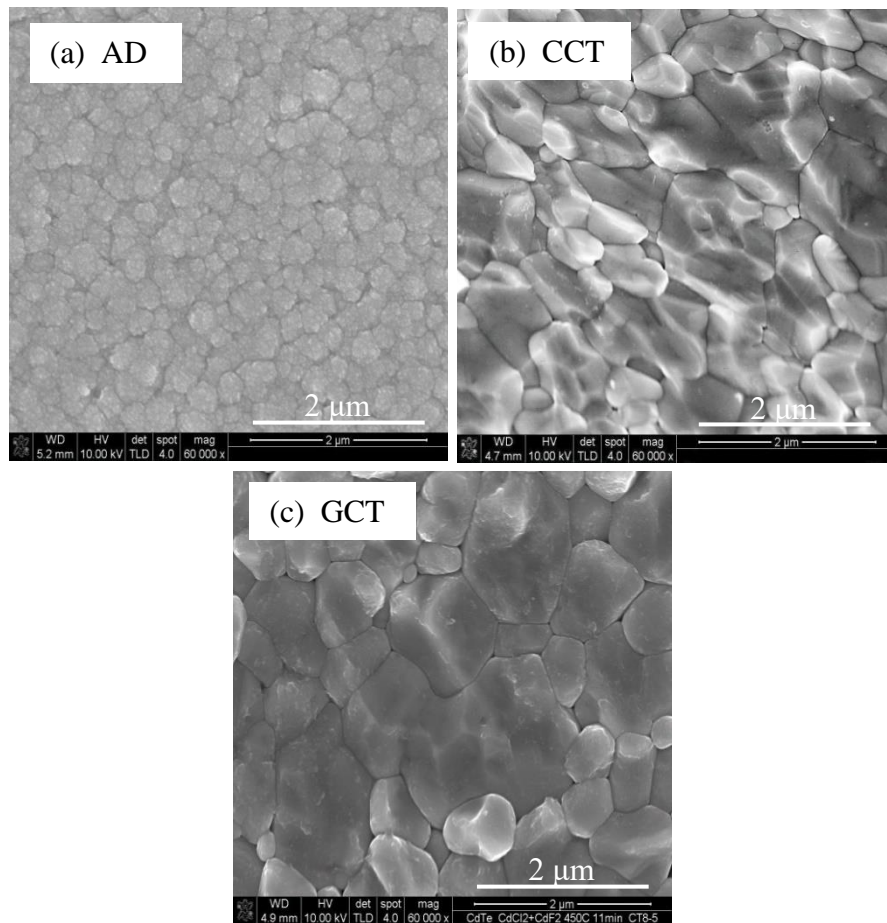
Figure 6.29: Typical SEM micrographs of (a) AD, (b) CCT and (c) GCT CdTe thin films electrodeposited on CdS layer at 1370 mV.

Compositional analysis

Figure 6.30 shows the atomic composition of a typical glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe multilayer configuration as detected by EDX technique. It should be noted that in addition to Cd and Te, the presence of S, Si, Sn, and F may also be observed due to underlying glass/FTO/CdS substrate, Cl or Ga due to the PGT utilised and O due to layer oxidation. As expected, a low Cd/Te composition ratio was observed for the AD layer due to the Te-richness during the growth of the top *p*-CdTe layer at lower cathodic potential. This observation further bolsters the fact that provided CdTe is not subjected to any extrinsic doping, the conductivity type of CdTe is composition dependent for the as-deposited layer. A shift towards unity of the Cd/Te ratio was observed after CCT and GCT.
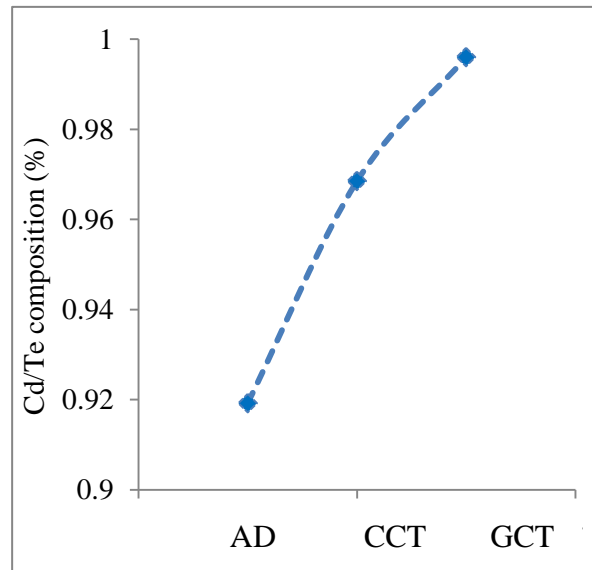
Figure 6.30: Percentage composition ratio of Cd to Te atoms in a glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe configuration after different PGT.

This observation has been reported in the literature [30,157,170,180] as one of the advantages of PGT of CdTe. It should be noted that in addition to elemental composition, self-compensation and doping effect can take place during PGT. In the case of GCT, the presence of gallium can also remove Te-precipitate during the heat treatment [100,181]. Therefore, the combination of all these processes seems to produce beneficial properties for the CdTe layer and the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe structure.

Structural analysis

Figure 6.31 shows the structural analysis of electrodeposited glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers under different conditions and Table 6.15 summarises the results of X-ray diffraction (XRD) analysis on the effect of different post-growth treatments on glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers. It was observed that no reflection could be attributed to the underlying CdS layer [265] except for the hexagonal CdS (002) which coincides with the FTO peak at angle $2\theta=26.68°$ and cannot be ascertained. Other reflections attributed to FTO were observable at $2\theta=32.9°$, $37.1°$, and $51.6°$. XRD reflections assigned to cubic (111), (220) and (311) CdTe phases at $2\theta=23.88°$, $38.65°$, and $45.84°$ were also observed. It can be deduced from Figure 6.31 that under all conditions explored in this work, the most intense XRD reflection is observed at $2\theta=23.85°$. For the CCT -glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layer, an increase in the cubic (111)C orientation was observed as compared to the AD without any observable change in the other CdTe reflections. However, for GCT - glass/FTO/*n*-CdS/*n*-CdTe/*p*-

CdTe layer, randomisation of crystallite orientation was observed. This is usually seen with the collapse of (111) peak and increase in (220) and (311) peaks. As reported recently [106], these changes suddenly occur when the grain boundaries are melted due to the presence of impurities such as excess Cd, Cl, O, and Ga. The presence of Ga seems to enhance the decrease in the (111) peak and increasing the (220) and (311) peak intensities due to increased randomisation of crystal orientations.

From the comparison between the AD, CCT and GCT glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers, it could be inferred that the inclusion of gallium in the normal cadmium chloride treatment PGT may have triggered the re-crystallisation and reorientation of the crystalline planes in this work. It should be noted that alterations in XRD patterns also depends on the underlying substrates and heat treatment conditions used [106].

As shown in Table 6.15, there was no clear distinction between the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layers explored in this work as concerning the full-width-at-half-maximum (FWHM), lattice spacing and crystallite size calculated using Scherrer's equation. This observation might be due to the limitations of the use of Scherrer's equation [115] or the XRD analysis software on polycrystalline material layers with large crystals.
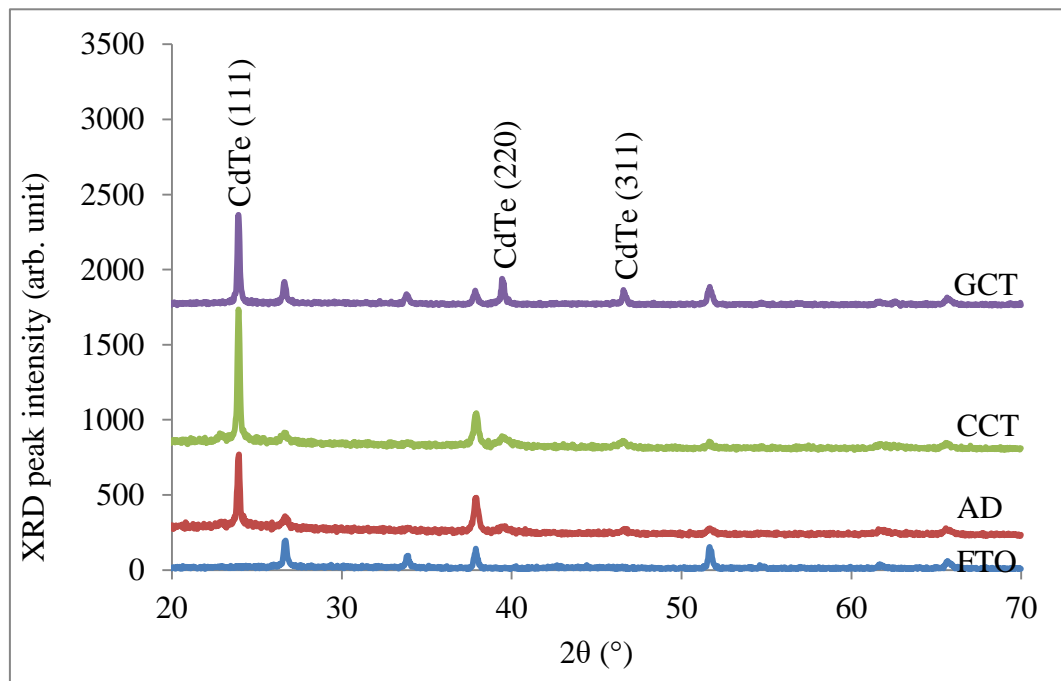
Figure 6.31: XRD spectra of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe structures for different conditions (AD, CCT and GCT).

Table 6.15: The XRD analysis on the effect of PGT on CdTe layers.

Treatment	2θ (°)	Lattice spacing (Å)	FWHM (°)	Crys. size D (nm)	Plane (hkl)	Assignments
AD	23.94	3.72	0.162	52.3	(111)	Cubic
CCT	23.92	3.72	0.162	52.3	(111)	Cubic
GCT	23.92	3.72	0.162	52.3	(111)	Cubic

Photoelectrochemical (PEC) cell study

Table 6.16 shows the PEC signal of glass/FTO/*p*-CdTe layer after different PGTs. It was observed that the *p-* conduction type of the as-deposited CdTe layer was retained after different treatments. Although, a shift in the PEC signal towards the *n*-type conduction region was also observable in both the CCT and GCT *p*-CdTe layers.

This observation depicts the movement of the FL which was close to the valence band towards the middle of the bandgap due to the alteration in doping as a result of the heat treatment condition [180], Cd/Te compositional changes [221] amongst other factors. Other incorporated layers such as *n*-CdS and *n*-CdTe have been known to retain their conductivity type with a slight shift towards the opposite conductivity type [148,170].

Table 6.16: PEC cell measurements on p-CdTe layers after different treatments.

Treatment	V_L (mV)	V_D (mV)	$(V_L$-$V_D)$ (mV)	Conduction type
AD	-61	-84	23	P
CCT	-78	-96	18	p
GCT	-42	-47	5	p

6.10.2 The effect of the inclusion of gallium in the normal CdCl$_2$ treatment on solar cell device parameters

Based on the analysis as discussed in Sections 0 to 0, the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe layer schematics and the band diagram can be represented by Figure 6.32 (a) and Figure 6.32 (b) respectively.
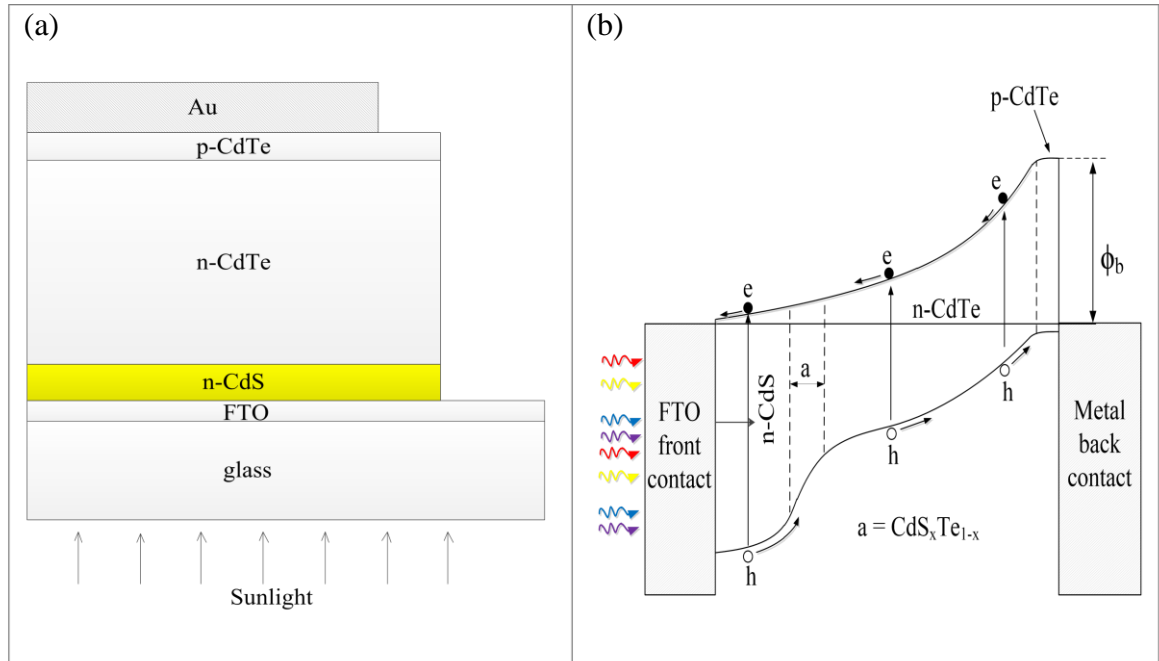
Figure 6.32: (a) Schematic diagram and (b) The band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au thin film solar cell.

Figure 6.33 (a), Figure 6.33 (b) and Figure 6.33 (c) show the current-voltage (I-V) curves of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au layers with different PGT conditions, measured under AM1.5 as discussed in Section 3.5.1.2. From these I-V curves measured under the illuminated AM1.5 condition, solar cell parameters can be determined. Experimentally observed solar cell parameters for the different conditions are summarised in Table 6.17 for three champion cells. Both the series resistance R_s and shunt resistance R_{sh} were calculated from the inverse slopes of the linear-linear I-V curve in the forward and reverse bias respectively under AM 1.5 illuminated conditions. The high R_s and low R_{sh} values as observed in the fabricated solar cell incorporating AD - CdTe can be directly attributed to low semiconductor material quality as described by Soga, 2004 [135]. It is clearly observed in Figure 6.33 and Table 6.17 that the improvement in the electrical properties of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices can be achieved after some chlorine-based treatment [266].
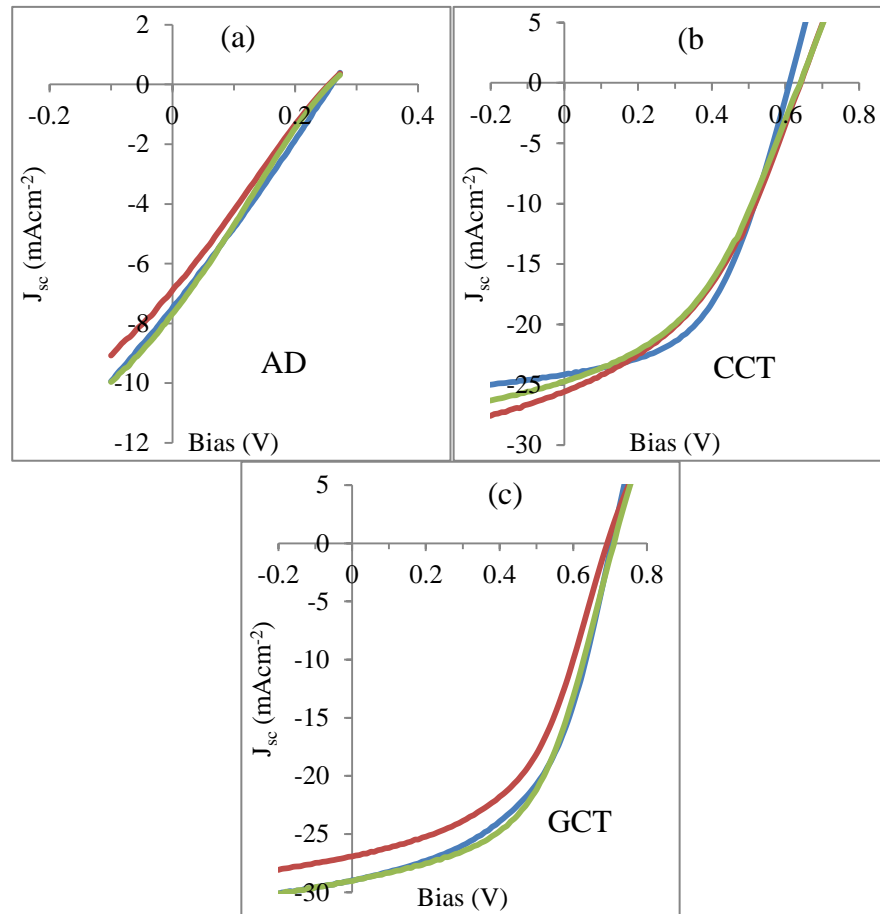
Figure 6.33: Current-voltage characteristics of glass/FTO/*n*-CdS/*n*-CdTe/p-CdTe/Au devics with AD, CCT and GCT conditions.

The addition of gallium into the regular CdCl$_2$ treatment further enhances the device performance. This enhancement can be attributed to the material properties improvement after treatment as discussed in Section 6.10.1. It should be noted that the short-circuit current density as observed in this work is higher than the Shockley–Queisser limit for a single *p-n* junction [20] as a result of the incorporation of the multilayer *n-n-p* configuration [232]. The structure represents an early stage of the graded bandgap, multilayer devices configuration.

Furthermore, the comparatively higher *FF*, *J$_{sc}$,* and *V$_{oc}$* observed with cells fabricated using GCT-CdTe can be attributed to the incorporation of *n*-dopant treatment such as gallium in CdTe by the introduction of excess electrons into the crystal lattice to boost conductivity and also further improvement in the material quality as observed in Sections 0 to 0. Similar observations have been recorded in the literature with the incorporation of *n*-dopant to CdTe [53,194,267]. Although the effect of the

incorporation of gallium on bandgap defects cannot be depicted from the I-V results, the improvement in the overall electronic properties of the fabricated devices is observable.

Table 6.17: Tabulated device parameters obtained from I-V measurements under AM1.5 illuminated condition.

Treatment	R_s (Ω)	R_{sh} (kΩ)	J_{sc} (mAcm^{-2})	V_{oc} (V)	FF	Efficiency (%)
AD	1027	1.4	7.1	0.25	0.24	0.43
	1062	1.5	7.8	0.26	0.24	0.49
	1180	1.3	7.6	0.25	0.24	0.46
CCT	302	6.4	24.2	0.61	0.50	7.50
	353	3.8	25.5	0.64	0.43	7.01
	354	3.2	24.8	0.64	0.43	6.84
GCT	273	8.0	29.9	0.72	0.52	11.21
	319	7.1	27.4	0.70	0.52	9.97
	276	8.0	29.3	0.73	0.52	11.12

6.10.3 Summations

The effect of the inclusion of Ga to the regular $CdCl_2$ post-growth treatment on the material and electronic properties of CdS/CdTe-based layers has been explored in this work. The optical analysis shows that the grown CdTe layer is within the standard bulk CdTe bandgap range with material superiority after $CdCl_2$:Ga treatment due to the steeper absorption edge slope - lesser impurity energy levels and defects in the thin fil. The morphological studies show full material coverage and grain growth after both CCT and GCT. The compositional analysis shows the improvement of stoichiometry when treated with GCT. The structural analysis shows improvement in the XRD peak intensity reflection of the as-deposited glass/FTO/n-CdS/n-CdTe/p-CdTe after both CCT and GCT with the preferred orientation along the cubic (111) plane. Although, more pronounced recrystallisation was observed after GCT with a comparative reduction in the (111)C peak and an increase in the (220)C reflection, showing improvement of grain boundary enhanced PV effect. Improvement in the electrical properties of the fabricated glass/FTO/n-CdS/n-CdTe/p-CdTe/Au was observed after PGT with GCT showing better results than CCT owing to the gallium inclusion in the treatment. With further material optimisation of gallium doping in the CdTe treatment, improved electronic properties can be achieved. Work is on-going on the optimisation of Ga concentration and treatment parameters required for this inclusion.

6.11 Summary of the effect of gallium chloride treatment pH

Similar to the experimental processes as discussed in Section 6.9, the effects of the pH of $CdCl_2+Ga_2(SO_4)_3$ (or GCT) on glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices were explored and are summarised in this section. Due to brevity and the significance of the importance of the study, only pH1 and pH2 data are presented.
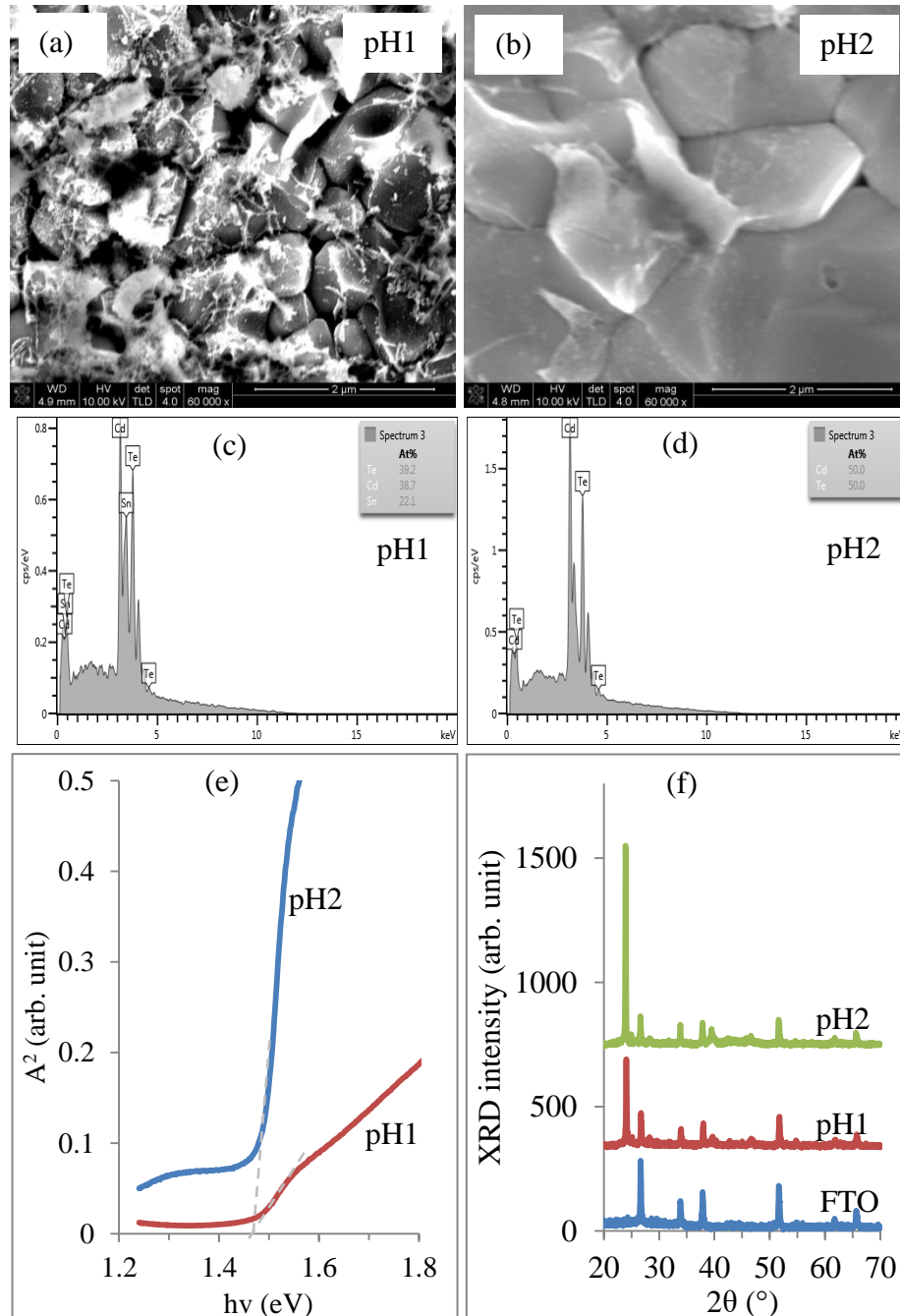
Figure 6.34: Typical SEM of CdTe after GCT at (a) pH1 and (b) pH2. Typical EDX spectra of CdTe after GCT at (c) pH1 and (d) pH2. (e) Typical absorption curve of CdTe treated with GCT at pH1 and pH2 and (f) Typical XRD peak of CdTe treated with GCT at pH1 and pH2.

Figure 6.34 shows the typical SEM, EDX, optical absorption and XRD peak patterns for CdTe post-growth treated with pH1 and pH2 GCT. The I-V and C-V characteristic properties of a typical device which have undergone GCT of pH1 and pH2 are presented in Table 6.18.

Table 6.18: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for glass/FTO/n-CdS/n-CdTe/p-CdTe/Au solar cells treated with pH1 and pH2 $CdCl_2+Ga_2(SO_4)_3$.

GCT pH	pH1	pH2
I-V under dark condition		
R_{sh} (Ω)	9230.70	$>10^6$
R_s (kΩ)	1.25	0.66
log (RF)	0.60	4.00
I_o (A)	3.16×10^{-6}	1.25×10^{-9}
n	>2	1.67
Φ_b (eV)	0.56	>0.81
I-V under 1.5 AM illumination condition		
I_{sc} (mA)	0.63	0.96
J_{sc} (mAcm^{-2})	20.06	30.57
V_{oc} (V)	0.34	0.71
Fill factor	0.31	0.56
Efficiency (%)	2.11	12.16
C-V under dark condition		
$\sigma \times10^{-4}$ (Ω.cm)$^{-1}$	11.39	0.36
N_D (cm^{-3})	6.22×10^{16}	1.12×10^{15}
μ (cm^{2}V^{-1}s^{-1})	0.11	20.06
C_o (pF)	150	350
W (nm)	203.9	873.8

As shown in the SEM micrographs (see Figure 6.34 (a) and Figure 6.34 (b)), an erosion of the CdTe layer morphology was observable at pH1 while the morphology of the CdTe treated with pH2 appears intact with low pinhole density and good coverage of the underlying layers. It should be noted that the eroded CdTe surface at pH1 is due to high acidity (low pH) and the dissolution of Cd whereby making the CdTe surface Te-rich [61] as observed in Figure 6.34 (c) and Figure 6.34 (d). Furthermore, due to the thinness of the films (within nano-scale), the nucleation mechanism of electrodeposited materials and the columnar growth nature of the electroplated materials, the erosion of the CdTe surface will result in opening pores along the grain boundaries which may

result into shunt paths for charge carriers. The optical absorbance measurements (Figure 6.34 (e)) show that both the CdTe layers treated with pH1 and pH2 GCT have bandgaps close to the 1.45 eV standard bandgap for bulk CdTe. The deviation of the bandgap away from the standard and the reduction in the absorption edge is due to compositional alteration away from stoichiometry [30,268]. This observation is further corroborated with higher XRD peak intensity as shown in Figure 6.34 (f) which signifies higher crystallinity for the pH2 treated sample.

With reference to Table 6.18, the effect of material deterioration due to the harsh erosion at GCT pH1 is summed up by the low R_{sh} [135]. Furthermore, lower conversion efficiency was observed for the pH1 GCT devices which might be due to the low R_{sh} which creates an alternative path for charge carriers and reduction in both the current density (J_{sc}) and charge carrier mobility (μ) as it is observed in the pH1 GCT devices.

6.12 Conclusions

Solar cells of different configurations, material layers, thicknesses and post-growth treatment conditions were successfully fabricated and explored using both I-V and C-V techniques. The results were systematically presented starting with the optimisation of the *n*-CdS window layer thickness. Based on observed electronic parameters, the optimised thickness of *n*-CdS in all-electrodeposited glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration was determined to be between (100 and 150) nm.

The optimised n-CdS thickness was utilised as a substrate for CdTe grown at different cathodic voltages around the cathodic voltage in which stoichiometric CdTe layers were grown. This resulted into either glass/FTO/*n*-CdS/*p*-CdTe/Au (an *n-p* junction) or glass/FTO/*n*-CdS/*n*-CdTe/Au (an *n-n*+SB) configurations in which better electronic parameters were observed in the *n-n*+SB architecture. In a view to further reduce CdS thickness, *n*-ZnS of 50 nm and CdS of 65 nm were incorporated in glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au structures and compared with the base glass/FTO/*n*-CdS/*n*-CdTe/Au. Higher efficiency and improvement in other parameters were obtained for the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au owing to the multilayer configuration based on the advantages of graded bandgap configuration. Further to this, the effect of F, Cl, I and Ga doped CdTe to give *n*-CdTe incorporated into the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration were also explored. Better prospects for achieving high efficiency were recorded for the devices incorporating F, Cl and most especially the Ga doped *n*-CdTe layers.

Also explored in this chapter is the effect of the incorporation of Ga in the normal CdCl$_2$ post-growth treatment and the effect of pH in both the CCT and GCT treatments of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au configuration. Further to this, the effect of p-CdTe in the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au configuration was also explored with the optimised thickness of ~35 nm. In addition, the variation as a function of batch and stability as a function of time was also explored. Conclusively, both the n-n-p and the n-n-n+SB multilayer architecture show great prospects for further exploration and development. In this research work, the highest efficiencies obtained in the glass/FTO/n-CdS/p-CdTe/Au (an n-p junction) and glass/FTO/n-CdS/n-CdTe/Au (an n-n+SB) are 7.5% and 4.5% respectively. The highest efficiency for the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au and glass/FTO/n-CdS/n-CdTe/p-CdTe/Cu-Au are 15.3% and 18.5% respectively, while the highest conversion efficiency obtained for the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au configuration was 14.1%.

Chapter 7 -   Conclusions, challenges encountered and future work

7.1   Conclusions

The work presented in this thesis puts together the chemistry, physics, material science, device physics and engineering involved in electroplated semiconductor material deposition and photovoltaic device fabrication. The observation and results are systematically reported in Chapter 4 to Chapter 6 of this thesis. The main semiconductor materials explored and presented in this thesis include CdS (which is the main window layer utilised) in Chapter 4 and CdTe (which is the main absorber layer utilised) in Chapter 5. Also included in Chapter 5 is the synthesis of doped CdTe layers (CdTe:F, CdTe:Cl, CdTe:I and CdTe:Ga). The electronic parameters of fabricated photovoltaic devices as reported in Chapter 4 and Chapter 5 are reported in Chapter 6. Other semiconductor materials such as ZnS utilised in the development of multilayer graded bandgap solar cell in this work were outsourced from other researchers within the Solar Energy Research Group at Sheffield Hallam University.

The CdS layer growth and characterisation documented in this thesis have been published in the literature (see references [36,37]), the CdTe work has also been published (see references [39–41,44,269,270]), while the work based on device fabrication was published in references [24,38,42,43,103,271].

The following summations can be made based on the results presented in this thesis:

i.   CdS layers were successfully electroplated using thiourea (NH_2CSNH_2) precursor in which there was no S precipitation during CdS growth. The optimum thickness of electroplated CdS window layers incorporated in the CdS/CdTe heterojunction layers is between (100 and 150) nm.

ii.   CdTe layers were successfully electroplated using both nitrate and chloride based precursors which are different from the sulphate based norm.

iii.   Doping of CdTe with F, Cl, I and Ga were achieved with optimal electrolytic bath doping of 20 ppm, 1.5 M $CdCl_2$ (base precursor), 5 ppm and 20 ppm respectively, based on optoelectronic material properties.

iv.   Glass/FTO/n-CdS/n-CdTe/Au (n-n+large Schottky barrier) show better prospect as compared to glass/FTO/n-CdS/p-CdTe/Au (n-p) junctions of the same CdS/CdTe heterojunction. This was iterated with the effect of growth voltage of CdTe on the fabricated device conversion efficiency.

v.   The basic multi-layer graded configurations explored in this work include glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au and glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au with the highest efficiency being 14.1% and 15.3% respectively. It should be noted that the highest efficiency of 18.4% was observed for glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au devices but due to instability and reproducibility issues, the results have not been published yet until the electronic parameters of the fabricated cells can be stabilised and further experimentations performed.

vi.   The effect of the *p*-layer thickness of glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au was also explored. It was observed that *p*-layer thickness within the range of ~35 nm gives good rectifying behaviours under dark and better solar cells with higher efficiency.

vii. The effects of the inclusion of $GaCl_3$ in the usual $CdCl_2$ treatments was explored and compared to the normal $CdCl_2$ treatment relative to the material and optoelectronic properties of CdTe thin films and fabricated devices. Comparatively, better parameters were observed in the optoelectronic properties of $GaCl_3+CdCl_2$ treated CdTe layers and associated devices.

viii. The effects of post-growth treatment pH of the normal $CdCl_2$ and $GaCl_3+CdCl_2$ were also explored with preferred optoelectronic parameters observed at pH2 on both counts.

ix.   The incorporated optimal F, Cl, I and Ga doping concentration in CdTe show interesting results with Ga doping showing more promising results.

Based on the iterated points, the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration incorporating ~120 nm *n*-CdS, ~1200 nm *n*-CdTe and 35 nm *p*-CdTe and post-growth treated with $GaCl_3+CdCl_2$ shows better electronic properties (V_{oc} = 730 mV, J_{sc} = 33.8 mAcm^2, FF = 0.62 and conversion efficiency of 15.3%) and stability. Therefore, the glass/FTO/*n*-CdS/*n*-CdTe/*p*-CdTe/Au configuration is deemed more promising for continued exploration and optimisation.

7.2   Challenges encountered in the course of this research

The major challenge encountered in this work was achieving high-efficiency photovoltaic devices and reproducibility. This can be attributed to several factors including:

i. The control of the electrodeposition process due to the alteration of current density as an increase in the deposition layer thickness increases its resistance.

ii. Control and regulation of ions within the electrolytic bath – as a result of depletion in the ionic concentration and the inability to gauge/measure ionic concentration in the electrolyte during layer deposition. Thereby reducing reproducibility tendencies.

iii. Control of purity throughout the electrolytic bath lifespan – as there has been an observation of increased carbon concentration in deposited semiconductor layers. The incorporation of carbon into the electrolytic bath is due to the deterioration of the anode electrode utilised in the electrolytic cell setup.

iv. Non-uniformity of electrodeposited semiconductor layers – this is due to the nucleation mechanism of electroplated materials.

7.3   Suggestions for future work

To further improve the achieved conversion efficiency, the following itemised suggestions are proposed:

i. Control of concentration of ions in the electrolytic bath using a composition analyser and automated feed pump for replenishing utilised ions in the deposition electrolytes.

ii. Explore other graded bandgap solar cell configurations by incorporating suitable wide bandgap *p*-type window materials as shown in Figure 2.13 (a).

iii. Explore further alternatives to the reduction of resistivity in both the CdS and CdTe-base materials.

iv. Reduction of series resistances of fabricated devices.

References

[1]   J.P. Holdren, Population and the energy problem, Popul. Environ. 12 (1991) 231–255. doi:10.1007/BF01357916.

[2]   World population projected to reach 9.7 billion by 2050 | UN DESA | United Nations Department of Economic and Social Affairs, (n.d.). http://www.un.org/en/development/desa/news/population/2015-report.html (accessed April 9, 2017).

[3]   E.E. Michaelides, Alternative Energy Sources, Springer Berlin Heidelberg, Berlin, Heidelberg, 2012. doi:10.1007/978-3-642-20951-2.

[4]   A.M. Omer, Energy use and environmental impacts: A general review, J. Renew. Sustain. Energy. 1 (2009) 53101. doi:10.1063/1.3220701.

[5]   BP, BP Energy Outlook 2017, 2017. https://www.bp.com/content/dam/bp/pdf/energy-economics/energy-outlook-2017/bp-energy-outlook-2017.pdf (accessed April 9, 2017).

[6]   M. Dale, Meta-analysis of non-renewable energy resource estimates, Energy Policy. 43 (2012) 102–122. doi:10.1016/j.enpol.2011.12.039.

[7]   N.S. Lewis, D.G. Nocera, Powering the planet: Chemical challenges in solar energy utilization, Proc. Natl. Acad. Sci. 103 (2006) 15729–15735. doi:10.1073/pnas.0603395103.

[8]   NASA/Marshall Solar Physics, (n.d.). https://solarscience.msfc.nasa.gov/interior.shtml (accessed April 11, 2017).

[9]   D. Chiras, Solar Electricity Basics: A Green Energy Guide, New Society Publishers, 2010. https://books.google.co.uk/books?id=_2brYQqb_RYC.

[10]   O. Morton, Solar energy: Silicon Valley sunrise, Nature. 443 (2006) 19–22. doi:10.1038/443019a.

[11]   Global Energy Budget | Precipitation Education, (n.d.). https://pmm.nasa.gov/education/lesson-plans/global-energy-budget (accessed October 25, 2017).

[12]   C.J. Riordan, Spectral solar irradiance models and data sets, Sol. Cells. 18 (1986) 223–232. doi:10.1016/0379-6787(86)90121-3.

[13]   The Greenhouse Effect and the Global Energy Budget | EARTH 103: Earth in the Future, (n.d.). https://www.e-education.psu.edu/earth103/node/1006 (accessed October 25, 2017).

[14]   I.M. Dharmadasa, Third generation multi-layer tandem solar cells for achieving high conversion efficiencies, Sol. Energy Mater. Sol. Cells. 85 (2005) 293–300. doi:10.1016/j.solmat.2004.08.008.

[15]   I.M. Dharmadasa, A.P. Samantilleke, N.B. Chaure, J. Young, New ways of developing glass/conducting glass/CdS/CdTe/metal thin-film solar cells based on a new model, Semicond. Sci. Technol. 17 (2002) 1238–1248. doi:10.1088/0268-1242/17/12/306.

[16]   I.M. Dharmadasa, Advances in thin-film solar cells, Pan Stanford, Singapore, 2013.

[17]   K. Masuko, M. Shigematsu, T. Hashiguchi, D. Fujishima, M. Kai, N. Yoshimura, T. Yamaguchi, Y. Ichihashi, T. Mishima, N. Matsubara, T. Yamanishi, T. Takahama, M. Taguchi, E. Maruyama, S. Okamoto, Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell, IEEE J. Photovoltaics. 4 (2014) 1433–1435. doi:10.1109/JPHOTOV.2014.2352151.

[18]   First Solar raises bar for CdTe with 21.5% efficiency record: pv-magazine, (n.d.). http://www.pv-magazine.com/news/details/beitrag/first-solar-raises-bar-for-cdte-with-215-efficiency-record_100018069/#axzz3rzMESjUl (accessed November 20, 2015).

[19]   K. Ramanathan, M.A. Contreras, C.L. Perkins, S. Asher, F.S. Hasoon, J. Keane, D. Young, M. Romero, W. Metzger, R. Noufi, J. Ward, A. Duda, Properties of 19.2% efficiency ZnO/CdS/CuInGaSe2 thin-film solar cells, Prog. Photovoltaics Res. Appl. 11 (2003) 225–230. doi:10.1002/pip.494.

[20]   W. Shockley, H.J. Queisser, Detailed Balance Limit of Efficiency of p-n Junction Solar Cells, J. Appl. Phys. 32 (1961) 510. doi:10.1063/1.1736034.

[21]   G. Conibeer, Third-generation photovoltaics, Mater. Today. 10 (2007) 42–50. doi:10.1016/S1369-7021(07)70278-X.

[22]   I.M. Dharmadasa, A.A. Ojo, H.I. Salim, R. Dharmadasa, Next Generation Solar Cells Based on Graded Bandgap Device Structures Utilising Rod-Type Nano-Materials, Energies. 8 (2015) 5440–5458. doi:10.3390/en8065440.

[23]   M.A. Green, Third generation photovoltaics: Ultra-high conversion efficiency at low cost, Prog. Photovoltaics Res. Appl. 9 (2001) 123–135. doi:10.1002/pip.360.

[24]   A.A. Ojo, I.M. Dharmadasa, 15.3% efficient graded bandgap solar cells fabricated using electroplated CdS and CdTe thin films, Sol. Energy. 136 (2016) 10–14. doi:10.1016/j.solener.2016.06.067.

References

[25] M.A. Green, Solar cell efficiency tables (version 49), Prog. Photovoltaics Res. Appl. 25 (2017) 3–13. doi:10.1002/pip.2876.

[26] A. Romeo, M. Terheggen, D. Abou-Ras, D.L. Bätzner, F.-J. Haug, M. Kälin, D. Rudmann, A.N. Tiwari, Development of thin-film Cu(In,Ga)Se2 and CdTe solar cells, Prog. Photovoltaics Res. Appl. 12 (2004) 93–111. doi:10.1002/pip.527.

[27] B.E. McCandless, J.R. Sites, Cadmium Telluride Solar Cells, in: Handb. Photovolt. Sci. Eng., John Wiley & Sons, Ltd, Chichester, UK, 2011: pp. 600–641. doi:10.1002/9780470974704.ch14.

[28] T.L. Chu, S.S. Chu, Thin film II–VI photovoltaics, Solid. State. Electron. 38 (1995) 533–549. doi:10.1016/0038-1101(94)00203-R.

[29] B.L. Williams, J.D. Major, L. Bowen, L. Phillips, G. Zoppi, I. Forbes, K. Durose, Challenges and prospects for developing CdS/CdTe substrate solar cells on Mo foils, Sol. Energy Mater. Sol. Cells. 124 (2014) 31–38. doi:10.1016/j.solmat.2014.01.017.

[30] A. Bosio, N. Romeo, S. Mazzamuto, V. Canevari, Polycrystalline CdTe thin films for photovoltaic applications, Prog. Cryst. Growth Charact. Mater. 52 (2006) 247–279. doi:10.1016/j.pcrysgrow.2006.09.001.

[31] X. Wu, High-efficiency polycrystalline CdTe thin-film solar cells, Sol. Energy. 77 (2004) 803–814. doi:10.1016/j.solener.2004.06.006.

[32] L. Kranz, C. Gretener, J. Perrenoud, R. Schmitt, F. Pianezzi, F. La Mattina, P. Blösch, E. Cheah, A. Chirilă, C.M. Fella, H. Hagendorfer, T. Jäger, S. Nishiwaki, A.R. Uhl, S. Buecheler, A.N. Tiwari, Doping of polycrystalline CdTe for high-efficiency solar cells on flexible metal foil, Nat. Commun. 4 (2013) 2306. doi:10.1038/ncomms3306.

[33] F. Shuman, Power from Sunshine, Sci. Am. 105 (1911) 291–292. doi:10.1038/scientificamerican09301911-291.

[34] M.A. Green, Y. Hishikawa, W. Warta, E.D. Dunlop, D.H. Levi, J. Hohl-Ebinger, A.W.H. Ho-Baillie, Solar cell efficiency tables (version 50), Prog. Photovoltaics Res. Appl. 25 (2017) 668–676. doi:10.1002/pip.2909.

[35] I. DHARMADASA, J. ROBERTS, G. HILL, Third generation multi-layer graded band gap solar cells for achieving high conversion efficiencies—II: Experimental results, Sol. Energy Mater. Sol. Cells. 88 (2005) 413–422. doi:10.1016/j.solmat.2005.05.008.

[36] A.A. Ojo, I.M. Dharmadasa, Investigation of electronic quality of

electrodeposited cadmium sulphide layers from thiourea precursor for use in large area electronics, Mater. Chem. Phys. 180 (2016) 14–28. doi:10.1016/j.matchemphys.2016.05.006.

[37] H.I. Salim, O.I. Olusola, A.A. Ojo, K.A. Urasov, M.B. Dergacheva, I.M. Dharmadasa, Electrodeposition and characterisation of CdS thin films using thiourea precursor for application in solar cells, J. Mater. Sci. Mater. Electron. 27 (2016) 6786–6799. doi:10.1007/s10854-016-4629-8.

[38] A.A. Ojo, H.I. Salim, O.I. Olusola, M.L. Madugu, I.M. Dharmadasa, Effect of thickness: a case study of electrodeposited CdS in CdS/CdTe based photovoltaic devices, J. Mater. Sci. Mater. Electron. 28 (2017) 3254–3263. doi:10.1007/s10854-016-5916-0.

[39] A.A. Ojo, I.M. Dharmadasa, The Effect of Fluorine Doping on the Characteristic Behaviour of CdTe, J. Electron. Mater. 45 (2016) 5728–5738. doi:10.1007/s11664-016-4786-9.

[40] A.A. Ojo, I.M. Dharmadasa, Electrodeposition of fluorine-doped cadmium telluride for application in photovoltaic device fabrication, Mater. Res. Innov. 19 (2015) 470–476. doi:10.1080/14328917.2015.1109215.

[41] A.A. Ojo, I.M. Dharmadasa, Effect of In-Situ Fluorine Doping on Electroplated Cadmium Telluride Thin Films for Photovoltaic Device Application, in: 31st Eur. Photovolt. Sol. Energy Conf., 2015: pp. 1249–1255. doi:10.4229/EUPVSEC20152015-3DV.1.40.

[42] A.A. Ojo, I.M. Dharmadasa, Optimisation of pH of cadmium chloride post-growth-treatment in processing CdS/CdTe based thin film solar cells, J. Mater. Sci. Mater. Electron. 28 (2017) 7231–7242. doi:10.1007/s10854-017-6404-x.

[43] O.I. Olusola, M.L. Madugu, A.A. Ojo, I.M. Dharmadasa, Investigating the effect of GaCl3 incorporation into the usual CdCl2 treatment on CdTe-based solar cell device structures, Curr. Appl. Phys. 17 (2017) 279–289. doi:10.1016/j.cap.2016.11.027.

[44] I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, O.I. Olusola, H.I. Salim, M.L. Madugu, A.A. Ojo, Improvement of composition of CdTe thin films during heat treatment in the presence of CdCl2, J. Mater. Sci. Mater. Electron. 28 (2017) 2343–2352. doi:10.1007/s10854-016-5802-9.

[45] J. Singh, Electronic and Optoelectronic Properties of Semiconductor Structures, Cambridge University Press, Cambridge, 2003.

doi:10.1017/CBO9780511805745.

[46] I.A. Sukhoivanov, I. V. Guryev, Photonic Crystals, Springer Berlin Heidelberg, Berlin, Heidelberg, 2009. doi:10.1007/978-3-642-02646-1.

[47] D. Neamen, Semiconductor physics and devices, Mater. Today. 9 (2006) 57. doi:10.1016/S1369-7021(06)71498-5.

[48] W.H. Strehlow, E.L. Cook, Compilation of Energy Band Gaps in Elemental and Binary Compound Semiconductors and Insulators, J. Phys. Chem. Ref. Data. 2 (1973) 163–200. doi:10.1063/1.3253115.

[49] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, John Wiley & Sons, Inc., Hoboken, NJ, USA, 2006. doi:10.1002/0470068329.

[50] S.D. Sathaye, A.P.B. Sinha, Studies on thin films of cadmium sulphide prepared by a chemical deposition method, Thin Solid Films. 37 (1976) 15–23. doi:10.1016/0040-6090(76)90531-9.

[51] I.M. Dharmadasa, J.M. Thornton, R.H. Williams, Effects of surface treatments on Schottky barrier formation at metal/n-type CdTe contacts, Appl. Phys. Lett. 54 (1989) 137. doi:10.1063/1.101208.

[52] I.M. Dharmadasa, J.D. Bunning, A.P. Samantilleke, T. Shen, Effects of multi-defects at metal/semiconductor interfaces on electrical properties and their influence on stability and lifetime of thin film solar cells, Sol. Energy Mater. Sol. Cells. 86 (2005) 373–384. doi:10.1016/j.solmat.2004.08.009.

[53] T.L. Chu, S.S. Chu, C. Ferekides, J. Britt, C.Q. Wu, Thin-film junctions of cadmium telluride by metalorganic chemical vapor deposition, J. Appl. Phys. 71 (1992) 3870–3876. doi:10.1063/1.350852.

[54] L. Huang, Y. Zhao, D. Cai, Homojunction and heterojunction based on CdTe polycrystalline thin films, Mater. Lett. 63 (2009) 2082–2084. doi:10.1016/j.matlet.2009.06.028.

[55] M.P. Mikhailova, a N. Titkov, Type II heterojunctions in the GaInAsSb/GaSb system, Semicond. Sci. Technol. 9 (1994) 1279–1295. doi:10.1088/0268-1242/9/7/001.

[56] P. Hofmann, Solid State Physics: An Introduction, 2nd ed., Wiley-VCH Berlin, 2015.

[57] P. V. Meyers, Advances in CdTe n-i-p photovoltaics, Sol. Cells. 27 (1989) 91–98. doi:10.1016/0379-6787(89)90019-7.

[58] W.G. Oldham, a. G. Milnes, n-n Semiconductor heterojunctions, Solid. State.

Electron. 6 (1963) 121–132. doi:10.1016/0038-1101(63)90005-4.

[59] E.H. Rhoderick, Metal-semiconductor contacts, IEE Proc. I Solid State Electron Devices. 129 (1982) 1. doi:10.1049/ip-i-1.1982.0001.

[60] J.P. Ponpon, A review of ohmic and rectifying contacts on cadmium telluride, Solid. State. Electron. 28 (1985) 689–706. doi:10.1016/0038-1101(85)90019-X.

[61] I.M. Dharmadasa, Recent developments and progress on electrical contacts to CdTe, CdS and ZnSe with special reference to BARRIER contacts to CdTe, Prog. Cryst. Growth Charact. Mater. 36 (1998) 249–290. doi:10.1016/S0960-8974(98)00010-2.

[62] J. Bardeen, Surface States and Rectification at a Metal Semi-Conductor Contact, Phys. Rev. 71 (1947) 717–727. doi:10.1103/PhysRev.71.717.

[63] E.H. Rhoderick, The physics of Schottky barriers?, Rev. Phys. Technol. 1 (1970) 81–95. doi:10.1088/0034-6683/1/2/302.

[64] J. Singh, Semiconductor Devices: Basic Principles, 2001.

[65] W.E. Spicer, I. Lindau, P. Skeath, C.Y. Su, P. Chye, Unified mechanism for schottky-barrier formation and III-V oxide interface states, Phys. Rev. Lett. 44 (1980) 420–423. doi:10.1103/PhysRevLett.44.420.

[66] R. Schlaf, R. Hinogami, M. Fujitani, S. Yae, Y. Nakato, Fermi level pinning on HF etched silicon surfaces investigated by photoelectron spectroscopy, J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. 17 (1999) 164. doi:10.1116/1.581568.

[67] I.M. Dharmadasa, O. Elsherif, G.J. Tolan, Solar Cells Active in Complete Darkness, J. Phys. Conf. Ser. 286 (2011) 12041. doi:10.1088/1742-6596/286/1/012041.

[68] H.J. Queisser, Defects in Semiconductors: Some Fatal, Some Vital, Science (80-.). 281 (1998) 945–950. doi:10.1126/science.281.5379.945.

[69] R.B. Godfrey, M.A. Green, Enhancement of MIS solar-cell ''efficiency'' by peripheral collection, Appl. Phys. Lett. 31 (1977) 705–707. doi:10.1063/1.89487.

[70] W.A. Nevin, G.A. Chamberlain, Effect of oxide thickness on the properties of metal-insulator-organic semiconductor photovoltaic cells, IEEE Trans. Electron Devices. 40 (1993) 75–81. doi:10.1109/16.249427.

[71] V.M. Fthenakis, Life cycle impact analysis of cadmium in CdTe PV production, Renew. Sustain. Energy Rev. 8 (2004) 303–334. doi:10.1016/j.rser.2003.12.001.

[72] J. Nelson, Polymer:fullerene bulk heterojunction solar cells, Mater. Today. 14 (2011) 462–470. doi:10.1016/S1369-7021(11)70210-3.

[73] J. Nelson, Organic photovoltaic films, Curr. Opin. Solid State Mater. Sci. 6 (2002) 87–95. doi:10.1016/S1359-0286(02)00006-2.

[74] S. Gunes, N.S. Sariciftci, Hybrid solar cells, Inorganica Chim. Acta. 361 (2008) 581–588. doi:10.1016/j.ica.2007.06.042.

[75] M. Wright, A. Uddin, Organic-inorganic hybrid solar cells: A comparative review, Sol. Energy Mater. Sol. Cells. 107 (2012) 87–111. doi:10.1016/j.solmat.2012.07.006.

[76] W. Xu, F. Tan, X. Liu, W. Zhang, S. Qu, Z. Wang, Z. Wang, Efficient Organic/Inorganic Hybrid Solar Cell Integrating Polymer Nanowires and Inorganic Nanotetrapods, Nanoscale Res. Lett. 12 (2017) 11. doi:10.1186/s11671-016-1795-9.

[77] P.-L. Ong, I.A. Levitsky, Organic / IV, III-V Semiconductor Hybrid Solar Cells, Energies. 3 (2010) 313–334. doi:10.3390/en3030313.

[78] NREL efficiency chart, (n.d.). https://www.nrel.gov/pv/assets/images/efficiency-chart.png (accessed June 19, 2017).

[79] O. Ergen, S.M. Gilbert, T. Pham, S.J. Turner, M.T.Z. Tan, M.A. Worsley, A. Zettl, Graded bandgap perovskite solar cells, Nat. Mater. 16 (2016) 522–525. doi:10.1038/nmat4795.

[80] J. Tauc, Generation of an emf in Semiconductors with Nonequilibrium Current Carrier Concentrations, Rev. Mod. Phys. 29 (1957) 308–324. doi:10.1103/RevModPhys.29.308.

[81] M. Wolf, Limitations and Possibilities for Improvement of Photovoltaic Solar Energy Converters: Part I: Considerations for Earth's Surface Operation, Proc. IRE. 48 (1960) 1246–1263. doi:10.1109/JRPROC.1960.287647.

[82] P.R. Emtage, Electrical Conduction and the Photovoltaic Effect in Semiconductors with Position-Dependent Band Gaps, J. Appl. Phys. 33 (1962) 1950–1960. doi:10.1063/1.1728874.

[83] M. Konagai, K. Takahashi, Graded-band-gap pGa1-xAlxAs-nGaAs heterojunction solar cells, J. Appl. Phys. 46 (1975) 3542–3546. doi:10.1063/1.322083.

[84] H.J. Hovel, J.M. Woodall, Ga[sub 1−x]Al[sub x]As-GaAs P-P-N Heterojunction Solar Cells, J. Electrochem. Soc. 120 (1973) 1246. doi:10.1149/1.2403671.

[85] A.S. Brown, M.A. Green, Impurity photovoltaic effect: Fundamental energy conversion efficiency limits, J. Appl. Phys. 92 (2002) 1329–1336.

doi:10.1063/1.1492016.

[86]   K.W.J. Barnham, G. Duggan, A new approach to high-efficiency multi-band-gap solar cells, J. Appl. Phys. 67 (1990) 3490–3493. doi:10.1063/1.345339.

[87]   T. Trupke, M.A. Green, P. Würfel, Improving solar cell efficiencies by down-conversion of high-energy photons, J. Appl. Phys. 92 (2002).

[88]   Y.Y. Lee, W.J. Ho, Y.T. Chen, Performance of plasmonic silicon solar cells using indium nanoparticles deposited on a patterned TiO2 matrix, Thin Solid Films. 570 (2014) 194–199. doi:10.1016/j.tsf.2014.05.022.

[89]   Y. Takeda, T. Motohiro, Highly efficient solar cells using hot carriers generated by two-step excitation, Sol. Energy Mater. Sol. Cells. 95 (2011) 2638–2644. doi:10.1016/j.solmat.2011.05.023.

[90]   J.F. Geisz, D.J. Friedman, J.S. Ward, A. Duda, W.J. Olavarria, T.E. Moriarty, J.T. Kiehl, M.J. Romero, A.G. Norman, K.M. Jones, 40.8% efficient inverted triple-junction solar cell with two independently metamorphic junctions, Appl. Phys. Lett. 93 (2008) 123505. doi:10.1063/1.2988497.

[91]   A.B.F. Martinson, M.S. Góes, F. Fabregat-Santiago, J. Bisquert, M.J. Pellin, J.T. Hupp, Electron Transport in Dye-Sensitized Solar Cells Based on ZnO Nanotubes: Evidence for Highly Efficient Charge Collection and Exceptionally Rapid Dynamics, J. Phys. Chem. A. 113 (2009) 4015–4021. doi:10.1021/jp810406q.

[92]   T. Stelzner, M. Pietsch, G. Andrä, F. Falk, E. Ose, S. Christiansen, Silicon nanowire-based solar cells, Nanotechnology. 19 (2008) 295203. http://stacks.iop.org/0957-4484/19/i=29/a=295203.

[93]   F.V. Wald, Applications of CdTe. A review, Rev. Phys. Appliquée. 12 (1977) 277–290. doi:10.1051/rphysap:01977001202027700.

[94]   R. Frerichs, The Photo-Conductivity of "Incomplete Phosphors," Phys. Rev. 72 (1947) 594–601. doi:10.1103/PhysRev.72.594.

[95]   J.J. Loferski, Theoretical Considerations Governing the Choice of the Optimum Semiconductor for Photovoltaic Solar Energy Conversion, J. Appl. Phys. 27 (1956) 777–784. doi:10.1063/1.1722483.

[96]   S. Luque, Antonio; Hegedus, Handbook of Photovoltaic Science and Engineering, John Wiley & Sons, Ltd, Chichester, UK, 2010. doi:10.1002/9780470974704.

[97]   K.L. Chopra, P.D. Paulson, V. Dutta, Thin-film solar cells: an overview, Prog.

Photovoltaics Res. Appl. 12 (2004) 69–92. doi:10.1002/pip.541.

[98] R.A. Street, Thin-Film Transistors, Adv. Mater. 21 (2009) 2007–2022. doi:10.1002/adma.200803211.

[99] W. Kern, K.K. Schuegraf, Deposition Technologies and Applications, in: Handb. Thin Film Depos. Process. Tech., Elsevier, 2001: pp. 11–43. doi:10.1016/B978-081551442-8.50006-7.

[100] J.M. Woodcock, A.K. Turner, M.E. Ozsan, J.G. Summers, Thin film solar cells based on electrodeposited CdTe, in: Conf. Rec. Twenty-Second IEEE Photovolt. Spec. Conf. - 1991, IEEE, 1991: pp. 842–847. doi:10.1109/PVSC.1991.169328.

[101] D. Cunningham, M. Rubcich, D. Skinner, Cadmium telluride PV module manufacturing at BP Solar, Prog. Photovoltaics Res. Appl. 10 (2002) 159–168. doi:10.1002/pip.417.

[102] I.M. Dharmadasa, J. Haigh, Strengths and Advantages of Electrodeposition as a Semiconductor Growth Technique for Applications in Macroelectronic Devices, J. Electrochem. Soc. 153 (2006) G47. doi:10.1149/1.2128120.

[103] A.A. Ojo, I.M. Dharmadasa, Progress in development of graded bandgap thin film solar cells with electroplated materials, J. Mater. Sci. Mater. Electron. 28 (2017) 6359–6365. doi:10.1007/s10854-017-6366-z.

[104] M.P.R. Panicker, M. Knaster, F.A. Kroger, Cathodic Deposition of CdTe from Aqueous Electrolytes, J. Electrochem. Soc. 125 (1978) 566. doi:10.1149/1.2131499.

[105] J. McHardy, F. Ludwig, Electrochemistry of Semiconductors and Electronics: Processes and Devices, Noyes Publications, 1992. https://books.google.co.uk/books?id=cSEt5W3vmdIC.

[106] I.M. Dharmadasa, P. Bingham, O.K. Echendu, H.I. Salim, T. Druffel, R. Dharmadasa, G. Sumanasekera, R. Dharmasena, M.B. Dergacheva, K. Mit, K. Urazov, L. Bowen, M. Walls, A. Abbas, Fabrication of CdS/CdTe-Based Thin Film Solar Cells Using an Electrochemical Technique, Coatings. 4 (2014) 380–415. doi:10.3390/coatings4030380.

[107] J. Pandey, ISSN: 2278-6252 SOLAR CELL HARVESTING: GREEN RENEWABLE TECHNOLOGY OF FUTURE INTRODUCTION, 4 (n.d.) 93–103.

[108] S. Dennison, Dopant and impurity effects in electrodeposited CdS/CdTe thin films for photovoltaic applications, J. Mater. Chem. 4 (1994) 41.

doi:10.1039/jm9940400041.

[109] K. Zanio, Semiconductors and semimetals, Academic Press, New York, 1978. http://shu.summon.serialssolutions.com/2.0.0/link/0/eLvHCXMwdV3JCsIwEB1c EAQPrrgV-gNKmyZNPYvFu94l6bQ3K1j_HydDXXA5Zg7DJJB5me0FIBLrYPXhE8LEUZ 8lRggjsgBlgBuptSqw0Chzrsy80Rg848ZXCuObQZ_iCKmCyN3HJjQJON2LqO aiYzdM7pnQiml0hCaUCiNVM-481sn7lwYMKGkfWm7IYACNvBxCh9sws2o.

[110] E.A. Meulenkamp, L.M. Peter, Mechanistic aspects of the electrodeposition of stoichiometric CdTe on semiconductor substrates, J. Chem. Soc. Trans. 92 (1996) 4077–4082. doi:10.1039/ft9969204077.

[111] A.Y. Shenouda, E.S.M. El Sayed, Electrodeposition, characterization and photo electrochemical properties of CdSe and CdTe, Ain Shams Eng. J. 6 (2014) 341–346. doi:10.1016/j.asej.2014.07.010.

[112] H.Y.R. Atapattu, D.S.M. De Silva, K.A.S. Pathiratne, I.M. Dharmadasa, Effect of stirring rate of electrolyte on properties of electrodeposited CdS layers, J. Mater. Sci. Mater. Electron. 27 (2016) 5415–5421. doi:10.1007/s10854-016-4443-3.

[113] P.T. Kissinger, W.R. Heineman, Cyclic voltammetry, J. Chem. Educ. 60 (1983) 702. doi:10.1021/ed060p702.

[114] C.W. Siders, Detection of Nonthermal Melting by Ultrafast X-ray Diffraction, Science (80-.). 286 (1999) 1340–1342. doi:10.1126/science.286.5443.1340.

[115] A. Monshi, Modified Scherrer Equation to Estimate More Accurately Nano-Crystallite Size Using XRD, World J. Nano Sci. Eng. 2 (2012) 154–160. doi:10.4236/wjnse.2012.23020.

[116] H.J. Butler, L. Ashton, B. Bird, G. Cinque, K. Curtis, J. Dorney, K. Esmonde-white, N.J. Fullwood, B. Gardner, P.L. Martin-Hirsch, M.J. Walsh, M.R. Mcainsh, N. Stone, F.L. Martin, Using Raman spectroscopy to characterise biological materials, Nat. Protoc. 11 (2016) 664–687. doi:10.1038/nprot.2016.036.

[117] A.K. Yadav, P. Singh, A review of the structures of oxide glasses by Raman spectroscopy, RSC Adv. 5 (2015) 67583–67609. doi:10.1039/C5RA13043C.

[118] W. a. Mackie, G.G. Magera, Defined emission area and custom thermal electron sources, J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom. 29 (2011) 06F601. doi:10.1116/1.3656350.

[119] D.N. Leonard, G.W. Chandler, S. Seraphin, Scanning Electron Microscopy, in:

Charact. Mater., John Wiley & Sons, Inc., Hoboken, NJ, USA, 2012: pp. 1721–1735. doi:10.1002/0471266965.com081.pub2.

[120] D.A. Moncrieff, P.R. Barker, Secondary electron emission in the scanning electron microscope, Scanning. 1 (1978) 195–197. doi:10.1002/sca.4950010307.

[121] K. Kanaya, S. Okayama, Penetration and energy-loss theory of electrons in solid targets, J. Phys. D. Appl. Phys. 5 (1972) 308. doi:10.1088/0022-3727/5/1/308.

[122] P.J. Statham, Limitations to accuracy in extracting characteristic line intensities from x-ray spectra, J. Res. Natl. Inst. Stand. Technol. 107 (2002) 531. doi:10.6028/jres.107.045.

[123] H.C. Allen, T. Brauers, B.J. Finlayson-Pitts, Illustration of Deviations in the Beer-Lambert Law in an Instrumental Analysis Laboratory: Measuring Atmospheric Pollutants by Differential Optical Absorption Spectrometry, J. Chem. Educ. 74 (1997) 1459. doi:10.1021/ed074p1459.

[124] J. Tauc, Optical properties and electronic structure of amorphous Ge and Si, Mater. Res. Bull. 3 (1968) 37–46. doi:10.1016/0025-5408(68)90023-8.

[125] J. Han, C. Spanheimer, G. Haindl, G. Fu, V. Krishnakumar, J. Schaffner, C. Fan, K. Zhao, a. Klein, W. Jaegermann, Optimized chemical bath deposited CdS layers for the improvement of CdTe solar cells, Sol. Energy Mater. Sol. Cells. 95 (2011) 816–820. doi:10.1016/j.solmat.2010.10.027.

[126] D.T.F. Marple, Optical absorption edge in CdTe: Experimental, Phys. Rev. 150 (1966) 728–734. doi:10.1103/PhysRev.150.728.

[127] V.Y. Roshko, L. a Kosyachenko, E. V Grushko, Theoretical Analysis of Optical Losses in CdS / CdTe Solar Cells, Acta Phys. Pol. A. 120 (2011) 954–956. http://przyrbwn.icm.edu.pl/APP/PDF/120/a120z5p39.pdf.

[128] H.A. Mohamed, Dependence of efficiency of thin-film CdS/CdTe solar cell on optical and recombination losses, J. Appl. Phys. 113 (2013). doi:10.1063/1.4794201.

[129] H.A. Mohamed, Influence of the optical and recombination losses on the efficiency of CdS/CdTe solar cell at ultrathin absorber layer, Can. J. Phys. 92 (2014) 1350–1355. doi:10.1139/cjp-2013-0477.

[130] J.E. Granata, J.R. Sites, Effect of CdS thickness on CdS/CdTe quantum efficiency, Conf. Rec. Twenty Fifth IEEE Photovolt. Spec. Conf. 1996. (2000) 853–856. doi:10.1109/PVSC.1996.564262.

[131] J.S. Lee, Y.K. Jun, H.B. Im, Effects of CdS Film Thickness on the Photovoltaic

Properties of Sintered CdS / CdTe Solar Cells, J. Electrochem. Soc. . 134 (1987) 248–251. doi:10.1149/1.2100417.

[132] P.M. Kaminski, F. Lisco, J.M. Walls, Multilayer broadband antireflective coatings for more efficient thin film CdTe solar cells, IEEE J. Photovoltaics. 4 (2014) 452–456. doi:10.1109/JPHOTOV.2013.2284064.

[133] Krishnan Rajeshwar, Fundamentals of Semiconductor Electrochemistry and Photoelectrochemistry, in: Encycl. Electrochem., Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany, 2007: pp. 1–51. doi:10.1002/9783527610426.bard060001.

[134] M. Chegaar, A. Hamzaoui, A. Namoda, P. Petit, M. Aillerie, A. Herguth, Effect of illumination intensity on solar cells parameters, Energy Procedia. 36 (2013) 722–729. doi:10.1016/j.egypro.2013.07.084.

[135] T. Soga, Nanostructured Materials for Solar Energy Conversion, Elsvier Sci. 2030 (2004) 614. http://www.amazon.co.uk/Nanostructured-Materials-Solar-Energy-Conversion/dp/044452844X/ref=sr_1_1?ie=UTF8&s=books&qid=1269872661&sr=1-1.

[136] M. Dadu, A. Kapoor, K.N. Tripathi, Effect of operating current dependent series resistance on the fill factor of a solar cell, Sol. Energy Mater. Sol. Cells. 71 (2002) 213–218. doi:10.1016/S0927-0248(01)00059-9.

[137] J. Verschraegen, M. Burgelman, J. Penndorf, Temperature dependence of the diode ideality factor in CuInS2-on-Cu-tape solar cells, Thin Solid Films. 480–481 (2005) 307–311. doi:10.1016/j.tsf.2004.11.006.

[138] S. Geyer, V.J. Porter, J.E. Halpert, T.S. Mentzel, M.A. Kastner, M.G. Bawendi, Charge transport in mixed CdSe and CdTe colloidal nanocrystal films, Phys. Rev. B - Condens. Matter Mater. Phys. 82 (2010). doi:10.1103/PhysRevB.82.155201.

[139] O. Madelung, U. Rössler, M. Schulz, eds., Cadmium telluride (CdTe) effective masses, in: II-VI I-VII Compd. Semimagn. Compd., Springer-Verlag, Berlin/Heidelberg, 1999: pp. 1–2. doi:10.1007/10681719_625.

[140] G.G. Roberts, M.C. Petty, I.M. Dharmadasa, Photovoltaic properties of cadmium-telluride/langmuir-film solar cells, IEE Proc. I Solid State Electron Devices. 128 (1981) 197. doi:10.1049/ip-i-1.1981.0049.

[141] T.Y. Chang, C.L. Chang, H.Y. Lee, P.T. Lee, A metal-insulator-semiconductor

solar cell with high open-circuit voltage using a stacking structure, IEEE Electron Device Lett. 31 (2010) 1419–1421. doi:10.1109/LED.2010.2073437.

[142] S. Chander, A. Purohit, A. Sharma, S.P. Nehra, M.S. Dhaka, Impact of temperature on performance of series and parallel connected mono-crystalline silicon solar cells, Energy Reports. 1 (2015) 175–180. doi:10.1016/j.egyr.2015.09.001.

[143] W.L. Liu, Y.L. Chen, a. a. Balandin, K.L. Wang, Capacitance–Voltage Spectroscopy of Trapping States in GaN/AlGaN Heterostructure Field-Effect Transistors, J. Nanoelectron. Optoelectron. 1 (2006) 258–263. doi:10.1166/jno.2006.212.

[144] S.W. Lin, J. Du, C. Balocco, Q.P. Wang, A.M. Song, Effects of bias cooling on charge states in heterostructures embedding self-assembled quantum dots, Phys. Rev. B. 78 (2008) 115314. doi:10.1103/PhysRevB.78.115314.

[145] I. Strzalkowski, S. Joshi, C.R. Crowell, Dielectric constant and its temperature dependence for GaAs, CdTe, and ZnSe, Appl. Phys. Lett. 28 (1976) 350–352. doi:10.1063/1.88755.

[146] N.B. Chaure, S. Bordas, A.P. Samantilleke, S.N. Chaure, J. Haigh, I.M. Dharmadasa, Investigation of electronic quality of chemical bath deposited cadmium sulphide layers used in thin film photovoltaic solar cells, Thin Solid Films. 437 (2003) 10–17. doi:10.1016/S0040-6090(03)00671-0.

[147] K.R. Murali, S. Kumaresan, J. Joseph Prince, Characteristics of CdS films brush electrodeposited on low-temperature substrates, Mater. Sci. Semicond. Process. 10 (2007) 56–60. doi:http://dx.doi.org/10.1016/j.mssp.2006.11.002.

[148] N.A. Abdul-Manaf, A.R. Weerasinghe, O.K. Echendu, I.M. Dharmadasa, Electro-plating and characterisation of cadmium sulphide thin films using ammonium thiosulphate as the sulphur source, J. Mater. Sci. Mater. Electron. 26 (2015) 2418–2429. doi:10.1007/s10854-015-2700-5.

[149] K. Yamaguchi, P. Mukherjee, T. Yoshida, H. Minoura, Multiple Fabrications of Crystalline CdS Thin Films from a Single Bath by EICD in Acidic Aqueous Solution of Cd2+ and Thiourea Complex., Chem. Lett. (2001) 864–865. doi:10.1246/cl.2001.864.

[150] M. Rami, E. Benamar, M. Fahoume, A. Ennaoui, Growth analysis of electrodeposited CdS on ITO coated glass using atomic force microscopy, Phys. Status Solidi a-Applied Res. 172 (1999) 137–147. doi:10.1002/(SICI)1521-

396X(199903)172:1<137::AID-PSSA137>3.0.CO;2-V.

[151] A. Izgorodin, O. Winther-Jensen, B. Winther-Jensen, D.R. MacFarlane, CdS thin-film electrodeposition from a phosphonium ionic liquid, Phys. Chem. Chem. Phys. 11 (2009) 8532. doi:10.1039/b906995j.

[152] N.A. Abdul-Manaf, H.I. Salim, M.L. Madugu, O.I. Olusola, I.M. Dharmadasa, Electro-Plating and Characterisation of CdTe Thin Films Using CdCl2 as the Cadmium Source, Energies. 8 (2015) 10883–10903. doi:10.3390/en81010883.

[153] A. Chandran, K.C. George, Phase instability and defect induced evolution of optical properties in Cd rich-CdS nanoparticles, J. Appl. Phys. 115 (2014) 164309. doi:10.1063/1.4873961.

[154] A. Abdolahzadeh Ziabari, F.E. Ghodsi, Growth, characterization and studying of sol–gel derived CdS nanoscrystalline thin films incorporated in polyethyleneglycol: Effects of post-heat treatment, Sol. Energy Mater. Sol. Cells. 105 (2012) 249–262. doi:http://dx.doi.org/10.1016/j.solmat.2012.05.014.

[155] A. Tanaka, S. Onari, T. Arai, One Phonon Raman Scattering of CdS Microcrystals Embedded in a Germanium Dioxide Glass Matrix, J. Phys. Soc. Japan. 61 (1992) 4222–4228. doi:10.1143/JPSJ.61.4222.

[156] J. Sun, D.K. Zhong, D.R. Gamelin, Composite photoanodes for photoelectrochemical solar water splitting, Energy Environ. Sci. 3 (2010) 1252. doi:10.1039/c0ee00030b.

[157] I.M. Dharmadasa, Review of the CdCl2 Treatment Used in CdS/CdTe Thin Film Solar Cell Development and New Evidence towards Improved Understanding, Coatings. 4 (2014) 282–307. doi:10.3390/coatings4020282.

[158] C. Wu, J. Jie, L. Wang, Y. Yu, Q. Peng, X. Zhang, J. Cai, H. Guo, D. Wu, Y. Jiang, Chlorine-doped n-type CdS nanowires with enhanced photoconductivity., Nanotechnology. 21 (2010) 505203. doi:10.1088/0957-4484/22/6/069801.

[159] N.S. Das, P.K. Ghosh, M.K. Mitra, K.K. Chattopadhyay, Effect of film thickness on the energy band gap of nanocrystalline CdS thin films analyzed by spectroscopic ellipsometry, Phys. E Low-Dimensional Syst. Nanostructures. 42 (2010) 2097–2102. doi:10.1016/j.physe.2010.03.035.

[160] M.A. Redwan, E.H. Aly, L.I. Soliman, A.A. El-Shazely, H.A. Zayed, Characteristics of n-Cd0.9 Zn0.1S/p-CdTe heterojunctions, Vacuum. 69 (2003) 545–555. doi:10.1016/S0042-207X(02)00604-8.

[161] A.K. Mohsin, N. Bidin, Effect of CdS Thickness on the Optical and Structural

Properties of TiO2/CdS Nanocomposite Film, Adv. Mater. Res. 1107 (2015) 547–552. doi:10.4028/www.scientific.net/AMR.1107.547.

[162] M.A. Tashkandi, W.S. Sampath, Eliminating pinholes in CSS deposited CdS films, in: Photovolt. Spec. Conf. (PVSC), 2012 38th IEEE, 2012: pp. 143–146. doi:10.1109/PVSC.2012.6317587.

[163] G. Mustafa, M.R.I. Chowdhury, D.K. Saha, S. Hussain, O. Islam, Annealing Effects on the Properties of Chemically Deposited CdS Thin Films at Ambient Condition, Dhaka Univ. J. Sci. 60 (2012) 283–288.

[164] A. - Taleb, F. - Mesguich, T. - Onfroy, X. - Yanpeng, - Design of TiO2/Au nanoparticle films with controlled crack formation and different architectures using a centrifugal strategy, - RSC Adv. (n.d.) 7007. doi:-10.1039/C4RA13829E.

[165] T.M. Razykov, C.S. Ferekides, D. Morel, E. Stefanakos, H.S. Ullal, H.M. Upadhyaya, Solar photovoltaic electricity: Current status and future prospects, Prog. Sol. Energy 1. 85 (2011) 1580–1608. doi:http://dx.doi.org.lcproxy.shu.ac.uk/10.1016/j.solener.2010.12.002.

[166] C.S. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D.L. Morel, CdTe thin film solar cells: device and technology issues, Sol. Energy. 77 (2004) 823–830. doi:10.1016/j.solener.2004.05.023.

[167] O.K. Echendu, F. Fauzi, A.R. Weerasinghe, I.M. Dharmadasa, High short-circuit current density CdTe solar cells using all-electrodeposited semiconductors, Thin Solid Films. 556 (2014) 529–534. doi:10.1016/j.tsf.2014.01.071.

[168] P. V. Braun, P. Osenar, M. Twardowski, G.N. Tew, S.I. Stupp, Macroscopic nanotemplating of semiconductor films with hydrogen-bonded lyotropic liquid crystals, Adv. Funct. Mater. 15 (2005) 1745–1750. doi:10.1002/adfm.200500083.

[169] T. Nishio, M. Takahashi, S. Wada, T. Miyauchi, K. Wakita, H. Goto, S. Sato, O. Sakurada, Preparation and characterization of electrodeposited in-doped CdTe semiconductor films, Electr. Eng. Japan. 164 (2008) 12–18. doi:10.1002/eej.20673.

[170] H.I. Salim, V. Patel, a. Abbas, J.M. Walls, I.M. Dharmadasa, Electrodeposition of CdTe thin films using nitrate precursor for applications in solar cells, J. Mater. Sci. Mater. Electron. 26 (2015) 3119–3128. doi:10.1007/s10854-015-2805-x.

[171] S. Bonilla, E.A. Dalchiele, Electrochemical deposition and characterization of CdTe polycrystalline thin films, Thin Solid Films. 204 (1991) 397–403.

doi:10.1016/0040-6090(91)90078-C.

[172] C.G. Morris, Academic Press dictionary of science and technology, Academic Press, San Diego, 1991.

[173] V. Petr, Electrochemical series, CRC Handb. Chem. Physics, 87th Ed. (2005) 1–10. doi:10.1136/oem.53.7.504.

[174] F.A. Kröger, Cathodic Deposition and Characterization of Metallic or Semiconducting Binary Alloys or Compounds, J. Electrochem. Soc. 125 (1978) 2028–2034. doi:10.1149/1.2131357.

[175] J.H. Chen, C.C. Wan, Dependence of the composition of CdTe semiconductor on conditions of electrodeposition, J. Electroanal. Chem. 365 (1994) 87–95. http://www.scopus.com/inward/record.url?eid=2-s2.0-0040171133&partnerID=40&md5=7f6ef88803b168878b60e48117cc31a6.

[176] T.L. Chu, S.S. Chu, F. Firszt, H. a. Naseem, R. Stawski, Deposition and characterization of p -type cadmium telluride films, J. Appl. Phys. 58 (1985) 1349–1355. doi:10.1063/1.336106.

[177] Y. Jung, G. Yang, S. Chun, D. Kim, J. Kim, Post-growth CdCl2 treatment on CdTe thin films grown on graphene layers using a close-spaced sublimation method, Opt. Express. 22 (2014) A986–A991. http://www.scopus.com/inward/record.url?eid=2-s2.0-84899786471&partnerID=40&md5=2f630c658c679ff9e4e38e7b57ea7243.

[178] C. Frausto-Reyes, J.R. Molina-Contreras, C. Medina-Gutiérrez, S. Calixto, CdTe surface roughness by Raman spectroscopy using the 830 nm wavelength, Spectrochim. Acta Part A Mol. Biomol. Spectrosc. 65 (2006) 51–55. doi:http://dx.doi.org/10.1016/j.saa.2005.07.082.

[179] M. Ichimura, F. Goto, E. Arai, Structural and optical characterization of CdS films grown by photochemical deposition, J. Appl. Phys. 85 (1999) 7411. doi:10.1063/1.369371.

[180] B.M. BAŞOL, PROCESSING HIGH EFFICIENCY CdTe SOLAR CELLS, Int. J. Sol. Energy. 12 (1992) 25–35. doi:10.1080/01425919208909748.

[181] P. Fernández, Defect structure and luminescence properties of CdTe based compounds, J. Optoelectron. Adv. Mater. 5 (2003) 369–388.

[182] H.-G. Junginger, Electronic band structure of tellurium, Solid State Commun. 5 (1967) 509–511. doi:10.1016/0038-1098(67)90534-0.

[183] I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, H.I. Salim, T.

Druffel, R. Dharmadasa, B. Lavery, Effects of CdCl2 treatment on deep levels in CdTe and their implications on thin film solar cells: a comprehensive photoluminescence study, J. Mater. Sci. Mater. Electron. 26 (2015) 4571–4583. doi:10.1007/s10854-015-3090-4.

[184] M. Bugar, E. Belas, R. Grill, J. Prochazka, S. Uxa, P. Hlidek, J. Franc, R. Fesh, P. Hoschl, Inclusions elimination and resistivity restoration of CdTe:Cl Crystals by two-step annealing, IEEE Trans. Nucl. Sci. 58 (2011) 1942–1948. doi:10.1109/TNS.2011.2159394.

[185] M.R. Murti, K. V Reddy, Grain Boundary Effects on the Carrier Mobility of Polysilicon, Phys. Status Solidi. 119 (1990) 237–240. doi:10.1002/pssa.2211190128.

[186] R. V. Muniswami Naidu, A. Subrahmanyam, A. Verger, M.K. Jain, S.V.N. Bhaskara Rao, S.N. Jha, D.M. Phase, Grain boundary carrier scattering in ZnO thin films: A study by temperature-dependent charge carrier transport measurements, J. Electron. Mater. 41 (2012) 660–664. doi:10.1007/s11664-012-1907-y.

[187] E. Regalado-Pérez, M.G. Reyes-Banda, X. Mathew, Influence of oxygen concentration in the CdCl2 treatment process on the photovoltaic properties of CdTe/CdS solar cells, Thin Solid Films. 582 (2015) 134–138. doi:10.1016/j.tsf.2014.11.005.

[188] Z.H. Chen, C.P. Liu, H.E. Wang, Y.B. Tang, Z.T. Liu, W.J. Zhang, S.T. Lee, J.A. Zapien, I. Bello, Electronic structure at the interfaces of vertically aligned zinc oxide nanowires and sensitizing layers in photochemical solar cells, J. Phys. D. Appl. Phys. 44 (2011) 325108. doi:10.1088/0022-3727/44/32/325108.

[189] S. Lalitha, R. Sathyamoorthy, S. Senthilarasu, a. Subbarayan, K. Natarajan, Characterization of CdTe thin film - Dependence of structural and optical properties on temperature and thickness, Sol. Energy Mater. Sol. Cells. 82 (2004) 187–199. doi:10.1016/j.solmat.2004.01.017.

[190] T.L. Chu, S.S. Chu, Y. Pauleau, K. Murthy, E.D. Stokes, P.E. Russell, Cadmium telluride films on foreign substrates, J. Appl. Phys. 54 (1983) 398. doi:10.1063/1.331717.

[191] K. Peters, A. Wenzel, P. Rudolph, The p-T-x projection of the system Cd-Te, Cryst. Res. Technol. 25 (1990) 1107–1116. doi:10.1002/crat.2170251002.

[192] N.V. V Sochinskii, V.N.N. Babentsov, N.I.I. Tarbaev, M.D. Serrano, E. Dieguez,

The low temperature annealing of p-cadmium telluride in gallium-bath, Mater. Res. Bull. 28 (1993) 1061–1066. doi:http://dx.doi.org/10.1016/0025-5408(93)90144-3.

[193] H.N. Jayatirtha, D.O. Henderson, a. Burger, M.P. Volz, Study of tellurium precipitates in CdTe crystals, Appl. Phys. Lett. 62 (1993) 573–575. doi:10.1063/1.108885.

[194] S. Mazzamuto, L. Vaillant, A. Bosio, N. Romeo, N. Armani, G. Salviati, A study of the CdTe treatment with a Freon gas such as CHF2Cl, Thin Solid Films. 516 (2008) 7079–7083. doi:10.1016/j.tsf.2007.12.124.

[195] A. Romeo, S. Buecheler, M. Giarola, G. Mariotto, A.N. Tiwari, N. Romeo, A. Bosio, S. Mazzamuto, Study of CSS- and HVE-CdTe by different recrystallization processes, Thin Solid Films. 517 (2009) 2132–2135. doi:10.1016/j.tsf.2008.10.129.

[196] N.B. Chaure, A.P. Samantilleke, I.M. Dharmadasa, The effects of inclusion of iodine in CdTe thin films on material properties and solar cell performance, Sol. Energy Mater. Sol. Cells. 77 (2003) 303–317. doi:10.1016/S0927-0248(02)00351-3.

[197] M.A. Green, K. Emery, Y. Hishikawa, W. Warta, E.D. Dunlop, Solar cell efficiency tables (version 46), Prog. Photovoltaics Res. Appl. 23 (2015) 805–812. doi:10.1002/pip.2637.

[198] a. Rios-Flores, O. Arés, J.M. Camacho, V. Rejon, J.L. Peña, Procedure to obtain higher than 14% efficient thin film CdS/CdTe solar cells activated with HCF 2Cl gas, Sol. Energy. 86 (2012) 780–785. doi:10.1016/j.solener.2011.12.002.

[199] O.K. Echendu, I.M. Dharmadasa, The effect on CdS/CdTe solar cell conversion efficiency of the presence of fluorine in the usual CdCl2 treatment of CdTe, Mater. Chem. Phys. 157 (2015) 39–44. doi:10.1016/j.matchemphys.2015.03.010.

[200] R.J. Deokate, S.M. Pawar, a. V. Moholkar, V.S. Sawant, C. a. Pawar, C.H. Bhosale, K.Y. Rajpure, Spray deposition of highly transparent fluorine doped cadmium oxide thin films, Appl. Surf. Sci. 254 (2008) 2187–2195. doi:10.1016/j.apsusc.2007.09.006.

[201] P. Ghosh, Electrical and optical properties of highly conducting CdO:F thin film deposited by sol–gel dip coating technique, Sol. Energy Mater. Sol. Cells. 81 (2004) 279–289. doi:10.1016/j.solmat.2003.11.021.

[202] E. Elangovan, K. Ramamurthi, Studies on micro-structural and electrical

properties of spray-deposited fluorine-doped tin oxide thin films from low-cost precursor, Thin Solid Films. 476 (2005) 231–236. doi:10.1016/j.tsf.2004.09.022.

[203] V.D. Popovych, I.S. Virt, F.F. Sizov, V.V. Tetyorkin, Z.F. Tsybrii (Ivasiv), L.O. Darchuk, O.A. Parfenjuk, M.I. Ilashchuk, The effect of chlorine doping concentration on the quality of CdTe single crystals grown by the modified physical vapor transport method, J. Cryst. Growth. 308 (2007) 63–70. doi:10.1016/j.jcrysgro.2007.07.041.

[204] L. Jin, Y. Linyu, J. Jikang, Z. Hua, S. Yanfei, Effects of Sn-doping on morphology and optical properties of CdTe polycrystalline films, J. Semicond. 30 (2009) 112003. doi:10.1088/1674-4926/30/11/112003.

[205] M. Kul, A.S. Aybek, E. Turan, M. Zor, S. Irmak, Effects of fluorine doping on the structural properties of the CdO films deposited by ultrasonic spray pyrolysis, Sol. Energy Mater. Sol. Cells. 91 (2007) 1927–1933. doi:10.1016/j.solmat.2007.07.014.

[206] B.G. Yacobi, Semiconductor materials : an introduction to basic principles, 1st ed., Springer US, 2003. doi:10.1007/b105378.

[207] T. Schulmeyer, J. Fritsche, A. Thißen, A. Klein, W. Jaegermann, M. Campo, J. Beier, Effect of in situ UHV CdCl2-activation on the electronic properties of CdTe thin film solar cells, Thin Solid Films. 431–432 (2003) 84–89. doi:10.1016/S0040-6090(03)00207-4.

[208] I.M. Dharmadasa, W.G. Herrenden-Harker, R.H. Williams, Metals on cadmium telluride: Schottky barriers and interface reactions, Appl. Phys. Lett. 48 (1986) 1802. doi:10.1063/1.96792.

[209] J.M. Burst, J.N. Duenow, D.S. Albin, E. Colegrove, M.O. Reese, J.A. Aguiar, C.-S. Jiang, M.K. Patel, M.M. Al-Jassim, D. Kuciauskas, S. Swain, T. Ablekim, K.G. Lynn, W.K. Metzger, CdTe solar cells with open-circuit voltage breaking the 1 V barrier, Nat. Energy. 1 (2016) 16015. doi:10.1038/nenergy.2016.15.

[210] M.O. Reese, C.L. Perkins, J.M. Burst, S. Farrell, T.M. Barnes, S.W. Johnston, D. Kuciauskas, T.A. Gessert, W.K. Metzger, Intrinsic surface passivation of CdTe, J. Appl. Phys. 118 (2015) 155305. doi:10.1063/1.4933186.

[211] D.G. Diso, F. Fauzi, O.K. Echendu, O.I. Olusola, I.M. Dharmadasa, Optimisation of CdTe electrodeposition voltage for development of CdS/CdTe solar cells, J. Mater. Sci. Mater. Electron. 27 (2016) 12464–12472. doi:10.1007/s10854-016-4844-3.

[212] M.K. Rabinal, I. Lyubomirsky, E. Pekarskaya, V. Lyakhovitskaya, D. Cahen, Low Resistance Contacts to p-CuInSe2 and p-CdTe Crystals, J. Electron. Mater. 26 (1997) 893–897. doi:10.1007/s11664-997-0270-x.

[213] S. Nozaki, A.G. Milnes, Specific contact resistivity of indium contacts to n-type CdTe, J. Electron. Mater. 14 (1985) 137–155. doi:10.1007/BF02656672.

[214] I.M. Dharmadasa, C.J. Blomfield, C.G. Scott, R. Coratger, F. Ajustron, J. Beauvillain, Metal/n-CdTe interfaces: A study of electrical contacts by deep level transient spectroscopy and ballistic electron emission microscopy, Solid. State. Electron. 42 (1998) 595–604. doi:10.1016/S0038-1101(97)00296-7.

[215] H. Metin, R. Esen, Annealing effects on optical and crystallographic properties of CBD grown CdS films, Semicond. Sci. Technol. 18 (2003) 647–654. doi:10.1088/0268-1242/18/7/308.

[216] R. Paterson, J. Anderson, S.S. Anderson, Lutfullah, Transport in aqueous solutions of group IIB metal salts at 298.15 K. Part 2.-Interpretation and prediction of transport in dilute solutions of cadmium iodide: an irreversible thermodynamic analysis, J. Chem. Soc. Faraday Trans. 1 Phys. Chem. Condens. Phases. 73 (1977) 1773–1788. http://www.scopus.com/inward/record.url?eid=2-s2.0-37049112678&partnerID=40&md5=362273ab1bc417a0d71d9355a1002c40.

[217] R. Paterson, C. Devine, Transport in aqueous solutions of Group IIB metal salts. Part 7.—Measurement and prediction of isotopic diffusion coefficients for iodide in solutions of cadmium iodide, J. Chem. Soc. Faraday Trans. 1 Phys. Chem. Condens. Phases. 76 (1980) 1052. doi:10.1039/f19807601052.

[218] A. Bouraiou, M.S. Aida, O. Meglali, N. Attaf, Potential effect on the properties of CuInSe2 thin films deposited using two-electrode system, Curr. Appl. Phys. 11 (2011) 1173–1178. doi:10.1016/j.cap.2011.02.014.

[219] C. Ferekides, J. Britt, CdTe solar cells with efficiencies over 15%, Sol. Energy Mater. Sol. Cells. 35 (1994) 255–262. doi:10.1016/0927-0248(94)90148-1.

[220] B.M. Basol, Electrodeposited CdTe and HgCdTe solar cells, Sol. Cells. 23 (1988) 69–88. doi:10.1016/0379-6787(88)90008-7.

[221] T.M. Razykov, N. Amin, B. Ergashev, C.S. Ferekides, D.Y. Goswami, M.K. Hakkulov, K.M. Kouchkarov, K. Sopian, M.Y. Sulaiman, M. Alghoul, H.S. Ullal, Effect of CdCl2 treatment on physical properties of CdTe films with different compositions fabricated by chemical molecular beam deposition, Appl.

Sol. Energy. 49 (2013) 35–39. doi:10.3103/S0003701X1301009X.

[222] P.J. Sellin, A.W. Dazvies, A. Lohstroh, M.E. Özsan, J. Parkin, Drift mobility and mobility-lifetime products in CdTe:Cl grown by the travelling heater method, IEEE Trans. Nucl. Sci. 52 (2005) 3074–3078. doi:10.1109/TNS.2005.855641.

[223] M.A. Cengel, Y. A. and Boles, Thermodynamics: An Engineering approach, 5th ed., McGraw-Hill, 2006.

[224] V.P. Vasil'ev, Correlations between the thermodynamic properties of II--VI and III--VI phases, Inorg. Mater. 43 (2007) 115–124. doi:10.1134/S0020168507020045.

[225] O. Chang-Seok, L.D. Nyung, C. Oh, Thermodynamic assessment of the Ga☐Te system, Calphad. 16 (1992) 317–330. doi:http://dx.doi.org/10.1016/0364-5916(92)90029-W.

[226] E. PŁaczek-Popko, Z. Gumienny, J. Trzmiel, J. Szatkowski, Evidence for metastable behavior of Ga-doped CdTe, Opt. Appl. 38 (2008) 559–565.

[227] K.C. Mandal, R.M. Krishna, T.C. Hayes, P.G. Muzykov, S. Das, T.S. Sudarshan, S. Ma, Layered GaTe crystals for radiation detectors, IEEE Trans. Nucl. Sci. 58 (2011) 1981–1986. doi:10.1109/TNS.2011.2140330.

[228] A.M. Mancini, C. Manfredotti, A. Rizzo, G. Micocci, Vapour growth of GaTe single crystals, J. Cryst. Growth. 21 (1974) 187–190. doi:10.1016/0022-0248(74)90003-7.

[229] O.I. Olusola, Optoelectronic devices based on graded bandgap structures utilising electroplated semiconductors, Sheffield Hallam University, UK., 2016.

[230] H.I. Salim, Multilayer Solar Cells Based on CdTe Grown From Nitrate Precursor., Sheffield Hallam University, UK, 2016.

[231] O.K. Echendu, Thin film solar cells using all-electrodeposited ZnS , CdS and CdTe materials, Sheffield Hallam University, UK., 2014.

[232] A. De Vos, Detailed balance limit of the efficiency of tandem solar cells, J. Phys. D. Appl. Phys. 13 (2000) 839–846. doi:10.1088/0022-3727/13/5/018.

[233] S.G. Kumar, K.S.R.K. Rao, Physics and chemistry of CdTe/CdS thin film heterojunction photovoltaic devices: fundamental and critical aspects, Energy Environ. Sci. 7 (2014) 45–102. doi:10.1039/C3EE41981A.

[234] C. Ni, P. Shah, A.M. Sarangan, Effects of different wetting layers on the growth of smooth ultra-thin silver thin films, in: E.M. Campo, E.A. Dobisz, L.A. Eldada (Eds.), 2014: p. 91700L. doi:10.1117/12.2061256.

[235] T. Yasuda, K. Hara, H. Kukimoto, Low resistivity Al-doped ZnS grown by MOVPE, J. Cryst. Growth. 77 (1986) 485–489. doi:10.1016/0022-0248(86)90341-6.

[236] M.L. Madugu, O.I.-O. Olusola, O.K. Echendu, B. Kadem, I.M. Dharmadasa, Intrinsic Doping in Electrodeposited ZnS Thin Films for Application in Large-Area Optoelectronic Devices, J. Electron. Mater. 45 (2016) 2710–2717. doi:10.1007/s11664-015-4310-7.

[237] O. Echendu, I. Dharmadasa, Graded-Bandgap Solar Cells Using All-Electrodeposited ZnS, CdS and CdTe Thin-Films, Energies. 8 (2015) 4416–4435. doi:10.3390/en8054416.

[238] X. Liu, Y. Jiang, F. Fu, W. Guo, W. Huang, L. Li, Facile synthesis of high-quality ZnS, CdS, CdZnS, and CdZnS/ZnS core/shell quantum dots: Characterization and diffusion mechanism, Mater. Sci. Semicond. Process. 16 (2013) 1723–1729. doi:10.1016/j.mssp.2013.06.007.

[239] I.M. Dharmadasa, a B. McLean, M.H. Patterson, R.H. Williams, Schottky barriers and interface reactions on chemically etched n-CdTe single crystals, Semicond. Sci. Technol. 2 (1987) 404–412. doi:10.1088/0268-1242/2/7/003.

[240] S. Tanaka, J.A. Bruce, M.S. Wrighton, Deliberate modification of the behavior of n-type cadmium telluride/electrolyte interfaces by surface etching. Removal of Fermi level pinning, J. Phys. Chem. 85 (1981) 3778–3787. doi:10.1021/j150625a015.

[241] T. Potlog, L. Ghimpu, P. Gashin, a. Pudov, T. Nagle, J. Sites, Influence of annealing in different chlorides on the photovoltaic parameters of CdS/CdTe solar cells, Sol. Energy Mater. Sol. Cells. 80 (2003) 327–334. doi:10.1016/j.solmat.2003.08.007.

[242] J. Britt, C. Ferekides, Thin-film CdS/CdTe solar cell with 15.8% efficiency, Appl. Phys. Lett. 62 (1993) 2851–2852. doi:10.1063/1.109629.

[243] B.E. McCandless, K.D. Dobson, Processing options for CdTe thin film solar cells, Sol. Energy. 77 (2004) 839–856. doi:10.1016/j.solener.2004.04.012.

[244] D.W. Lane, A review of the optical band gap of thin film CdSxTe 1-x, Sol. Energy Mater. Sol. Cells. 90 (2006) 1169–1175. doi:10.1016/j.solmat.2005.07.003.

[245] D.A. Wood, K.D. Rogers, D.W. Lane, D.A. Wood, K.D. Rogers, J.A. Coath, Optical and structural characterization of CdS x Te 1- x thin films for solar cell

applications, J. Phys. Condens. Matter. 12 (2000) 4433–4450. doi:10.1088/0953-8984/12/19/312.

[246] E.Q.B. Macabebe, E.E. van Dyk, Parameter extraction from dark current–voltage characteristics of solar cells, S. Afr. J. Sci. (2008) 401–404. http://www.scielo.org.za/scielo.php?script=sci_arttext&pid=S0038-23532008000500017.

[247] J.D. Major, L. Bowen, R.E. Treharne, L.J. Phillips, K. Durose, NH 4 Cl Alternative to the CdCl 2 Treatment Step for CdTe Thin-Film Solar Cells, IEEE J. 5 (2015) 386–389. doi:10.1109/JPHOTOV.2014.2362296.

[248] B. Maniscalco, A. Abbas, J.W. Bowers, P.M. Kaminski, K. Bass, G. West, J.M. Walls, The activation of thin film CdTe solar cells using alternative chlorine containing compounds, Thin Solid Films. 582 (2015) 115–119. doi:10.1016/j.tsf.2014.10.059.

[249] B.E. McCandless, I. Youm, R.W. Birkmire, Optimization of vapor post-deposition processing for evaporated CdS/CdTe solar cells, Prog. Photovoltaics Res. Appl. 7 (1999) 21–30. doi:10.1002/(SICI)1099-159X(199901/02)7:1<21::AID-PIP244>3.0.CO;2-D.

[250] H. Bayhan, C. Ercelebi, Effects of Post Deposition Treatments on Vacuum Evaporated CdTe Thin Films and CdS/CdTe Heterojunction Devices, Turkish J. Phys. 22 (1998) 441–451. http://www.scopus.com/scopus/inward/record.url?eid=2-s2.0-0347537252&partnerID=40&rel=R6.5.0.

[251] V. Krishnakumar, J. Han, A. Klein, W. Jaegermann, CdTe thin film solar cells with reduced CdS film thickness, Thin Solid Films. 519 (2011) 7138–7141. doi:10.1016/j.tsf.2010.12.118.

[252] D.A. Wood, K.D. Rogers, D.W. Lane, D.A. Wood, K.D. Rogers, J.A. Coath, Optical and structural characterization of CdS x Te 1- x thin films for solar cell applications, J. Phys. Condens. Matter. 12 (2000) 4433. http://stacks.iop.org/0953-8984/12/i=19/a=312.

[253] G. Carotenuto, M. Palomba, S. De Nicola, G. Ambrosone, U. Coscia, Structural and Photoconductivity Properties of Tellurium/PMMA Films., Nanoscale Res. Lett. 10 (2015) 1007. doi:10.1186/s11671-015-1007-z.

[254] B. Abad, M. Rull-Bravo, S.L. Hodson, X. Xu, M. Martin-Gonzalez, Thermoelectric properties of electrodeposited tellurium films and the sodium

lignosulfonate effect, Electrochim. Acta. 169 (2015) 37–45. doi:10.1016/j.electacta.2015.04.063.

[255] S. Chun, S. Lee, Y. Jung, J.S. Bae, J. Kim, D. Kim, Wet chemical etched CdTe thin film solar cells, Curr. Appl. Phys. 13 (2013) 211–216. doi:10.1016/j.cap.2012.07.015.

[256] Y. Shan, J.-J. Xu, H.-Y. Chen, Enhanced electrochemiluminescence quenching of CdS:Mn nanocrystals by CdTe QDs-doped silica nanoparticles for ultrasensitive detection of thrombin, Nanoscale. 3 (2011) 2916. doi:10.1039/c1nr10175g.

[257] D. Congreve, J. Lee, N. Thompson, E. Hontz, External Quantum Efficiency Above 100% in a Singlet-Exciton-Fission–Based Organic Photovoltaic Cell, Science (80-.). 340 (2013) 334–337. doi:10.1126/science.1232994.

[258] N.J.L.K. Davis, M.L. Bohm, M. Tabachnyk, F. Wisnivesky-Rocca-Rivarola, T.C. Jellicoe, C. Ducati, B. Ehrler, N.C. Greenham, Multiple-exciton generation in lead selenide nanorod solar cells with external quantum efficiencies exceeding 120%, Nat Commun. 6 (2015) 81–87. doi:10.1007/s13398-014-0173-7.2.

[259] B.M. Basol, B. McCandless, Brief review of cadmium telluride-based photovoltaic technologies, J. Photonics Energy. 4 (2014) 40996. doi:10.1117/1.JPE.4.040996.

[260] M. Gloeckler, I. Sankin, Z. Zhao, CdTe solar cells at the threshold to 20% efficiency, IEEE J. Photovoltaics. 3 (2013) 1389–1393. doi:10.1109/JPHOTOV.2013.2278661.

[261] T.J. Coutts, S. Naseem, High Efficiency Indium Tin Oxide/Indium Phosphide Solar Cells., Appl. Phys. Lett. 46 (1985) 164–166. doi:10.1063/1.95723.

[262] H. Liu, Y. Tian, Y. Zhang, K. Gao, K. Lu, R. Wu, D. Qin, H. Wu, Z. Peng, L. Hou, W. Huang, Solution processed CdTe/CdSe nanocrystal solar cells with more than 5.5% efficiency by using an inverted device structure, J. Mater. Chem. C. 3 (2015) 4227–4234. doi:10.1039/C4TC02816C.

[263] H. Xue, R. Wu, Y. Xie, Q. Tan, D. Qin, H. Wu, W. Huang, Recent Progress on Solution-Processed CdTe Nanocrystals Solar Cells, Appl. Sci. 6 (2016) 197. doi:10.3390/app6070197.

[264] J.C. Tranchart, P. Bach, A gas bearing system for the growth of CdTe, J. Cryst. Growth. 32 (1976) 8–12. doi:10.1016/0022-0248(76)90003-8.

[265] T. Toyama, K. Matsune, H. Oda, M. Ohta, H. Okamoto, X-ray diffraction study of CdS/CdTe heterostructure for thin-film solar cell: Influence of CdS grain size

on subsequent growth of (111)-oriented CdTe film, J. Phys. D. Appl. Phys. 39 (2006) 1537–1542. doi:10.1088/0022-3727/39/8/013.

[266] J.D. Major, R.E. Treharne, L.J. Phillips, K. Durose, A low-cost non-toxic post-growth activation step for CdTe solar cells, Nature. 511 (2014) 334–337. doi:10.1038/nature13435.

[267] T. Ferid, M. Saji, Transport properties in gallium doped CdTe MOVPE layers, J. Cryst. Growth. 172 (1997) 83–88. doi:10.1016/S0022-0248(96)00740-3.

[268] I.M. Dharmadasa, A.A. Ojo, Unravelling complex nature of CdS/CdTe based thin film solar cells, J. Mater. Sci. Mater. Electron. 28 (2017) 16598–16617. doi:10.1007/s10854-017-7615-x.

[269] A.A. Ojo, I.M. Dharmadasa, Analysis of electrodeposited CdTe thin films grown using cadmium chloride precursor for applications in solar cells, J. Mater. Sci. Mater. Electron. 28 (2017) 14110–14120. doi:10.1007/s10854-017-7264-0.

[270] A.A. Ojo, I.M. Dharmadasa, Effect of Gallium Doping on the Characteristic Properties of Polycrystalline Cadmium Telluride Thin Film, J. Electron. Mater. 46 (2017) 5127–5135. doi:10.1007/s11664-017-5519-4.

[271] A.A. Ojo, I.O. Olusola, I.M. Dharmadasa, Effect of the inclusion of gallium in normal cadmium chloride treatment on electrical properties of CdS/CdTe solar cell, Mater. Chem. Phys. 196 (2017) 229–236. doi:10.1016/j.matchemphys.2017.04.053.

[272] N.M. Forsyth, I.M. Dharmadasa, Z. Sobiesierski, R.H. Williams, Schottky barriers to CdS and their importance in Schottky barrier theories, Semicond. Sci. Technol. 4 (1989) 57–59. doi:10.1088/0268-1242/4/1/011.

[273] N. Forsyth, I. Dharmadasa, Z. Sobiesierski, R. Williams, An investigation of metal contacts to II–VI compounds: CdTe and CdS, Vacuum. 38 (1988) 369–371. doi:10.1016/0042-207X(88)90081-4.