Analysis of the Electronic Properties of All-electroplated ZnS, CdS and CdTe Graded Bandgap Photovoltaic Device Configuration

OJO, A. A. and DHARMADASA, I <http://orcid.org/0000-0001-7988-669X>

Analysis of the Electronic Properties of All-electroplated ZnS, CdS and CdTe Graded Bandgap Photovoltaic Device Configuration

A. A. Ojo* and I. M. Dharmadasa

Electronic Materials and Sensors Group, Materials and Engineering Research Institute (MERI), Sheffield Hallam University, Sheffield S1 1WB, UK.

*Email: chartell2006@yahoo.com; Tel: +44 114 225 6910 Fax: +44 114 225 6930

Abstract

All-electrodeposited ZnS, CdS and CdTe thin layers have been incorporated in a graded bandgap solar cell structure of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au have been fabricated and an average conversion efficiency of 14.18% was achieved under AM1.5 illuminated condition. Based on former work in which 10% conversion efficiency was reported, optimisation has been made to the semiconductor layers, precursors, thicknesses and the post-growth treatment. These results demonstrate the advantages of multi-layer graded bandgap device configuration and the inclusion of gallium based post-growth treatment ($CdCl_2$+$Ga_2(SO_4)_3$) on the CdS/CdTe-based device structure. The fabricated devices were characterised using both current-voltage (I-V) and capacitance-voltage (C-V) techniques. Under dark I-V condition, a rectification factor (*R.F.*) of $10^{4.8}$, ideality factor (*n*) of 1.60 and a barrier height (ϕ_b) >0.82 eV were observed. Under AM1.5 illuminated I-V condition, short-circuit current density (J_{sc}) of 34.08 mAcm^{-2}, open-circuit voltage (V_{oc}) of 730 mV, fill-factor (*FF*) of 0.57 and conversion efficiency of 14.18% were observed. Under dark C-V condition, doping density (N_D) of 7.79×10^{14} cm^{-3} and a depletion width (*W*) of 1092 nm were achieved. In addition, the work demonstrates the capability of two-electrode system as a simplification to the conventional three-electrode system in the electrodeposition of semiconductors.

Keywords: ZnS; CdS; CdTe; $CdCl_2$+$Ga_2(SO_4)_3$; graded bandgap.

1 Introduction

With a focus on effective cost reduction and increase in photovoltaic device efficiency, electrodeposition emerges as one of the semiconductor deposition techniques that show such potential (Basol, 1984; Dharmadasa, 2013; Lincot, 2005). Electrodeposition (ED) of II-VI semiconductor heterojunctions such as the well-known CdS/CdTe have been well explored and published in the literature (Basol, 1984; Ou et al., 1984) with one of its characteristics being its nucleation process. The nucleation of electroplated semiconductor on a conducting substrate starts at the peaks of the rough surface and spreads out through to the lowest valley resulting into layers with columnar nature (Dharmadasa et al., 2014). With main emphasis on CdS window material, literature shows the detrimental effect of low ED-CdS thickness (~50 nm) on the electronic properties of fabricated CdS/CdTe based solar cell (A A Ojo et al., 2017) as compared to the other deposition techniques (Granata and Sites, 2000; Lee et al., 1987). Due to the parasitic absorption relative to increasing thickness (Ferekides et al., 2005; Granata and Sites, 2000) and increase in pinhole density associated with thinner CdS layers (Granata and Sites, 2000; A A Ojo et al., 2017), the incorporation of a wider bandgap buffer layer is necessitated. As documented in the literature, buffer layers such as ZnO, ZnS, $Zn_{1-X}Sn_XO$, Zn_2SnO_4, SnO_2 (Colegrove et al., 2012; Echendu and Dharmadasa, 2015; Gupta and Compaan, 2004; Major and Durose, 2013; Manzoli et al., 2007; Wu et al., 1999) amongst others have been explored. Focusing on electrodeposition technique, the incorporation of ZnS buffer layer has been demonstrated in glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device configuration using all-electrodeposited ZnS, CdS and CdTe layers, which resulted in a conversion efficiency of 10.4% (Echendu and Dharmadasa, 2015). Based on the optimisation of layer thickness and post-growth treatment, the work presented in this communication is an improvement on the previous work and conversion efficiency up to ~14.18% was achieved.

2 Experimental details

2.1 Sample preparation

All the chemicals, substrates and electrodes used in this study were procured from Sigma Aldrich Ltd, UK. To achieve the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device, all the semiconductor layers were cathodically electroplated using a 2-electrode configuration incorporating high purity carbon anode and glass/FTO cathode (Dharmadasa et al., 2017). The working electrode is graded TEC7 with sheet resistance ~7 Ω/sq. Prior to electroplating, the glass/FTO substrates were ultrasonic cleaned in soap solution bath for ~15 min.

Afterwards, the substrates were rinsed with deionised (DI) water, dried in a stream of nitrogen gas and degreased using acetone and methanol. The substrates were immediately rinsed in DI water and attached to the cathode rod using polytetrafluoroethylene tape and finally rinsed in DI water prior to its transfer to the electrodeposition bath.

50 nm thick *n*-ZnS buffer layer was electroplated on the glass/FTO substrates from an electrolytic bath containing zinc sulphate monohydrate ($ZnSO_4 \cdot H_2O$) of 99.9% purity and ammonium thiosulphate ($(NH_4)_2S_2O_3$) of 98% purity as zinc and sulphur precursors respectively. The electrolytic bath was prepared by dissolving 0.2 M $ZnSO_4 \cdot H_2O$ and 0.2 M $(NH_4)_2S_2O_3$ in 400 ml DI water. For this work, the *n*-ZnS layers were grown at 1425 mV close to the *p*-to-*n* conduction type transition voltage (V_i) at a bath temperature of 30±2℃ and pH of 4.00±0.02. The full details of similar ZnS electrodeposition is documented in reference (Madugu et al., 2016). The glass/FTO/*n*-ZnS layers were heat treated in air at 300℃ and air-cooled afterwards. It should be noted that the *n*-ZnS conduction type which is retained after heat treatment (Madugu et al., 2016).

The CdS window layers were electrodeposited on the post-growth treated glass/FTO/*n*-ZnS layers. An electrolytic bath containing 0.3 M hydrated cadmium chloride ($CdCl_2 \cdot xH_2O$) with 99.99% purity and 0.03 M ammonium thiosulphate ($(NH_4)_2S_2O_3$) with 98% purity in 400 ml of DI water. 65 nm thick CdS was deposited at a pre-optimised cathodic voltage of 1200 mV at a bath temperature of 85±2℃ and pH of 2.50±0.02. The deposited glass/FTO/*n*-ZnS/*n*-CdS configuration was $CdCl_2$ treated at 400℃ in air, air-cooled and rinsed afterwards prior to *n*-CdTe layer deposition. Details of similar CdS layer deposition and optimisation has been published in the literature (Abdul-Manaf et al., 2015). It should be noted that provided CdS is not extrinsically dope *p*-type, CdS remains *n*-type due defects related to Cd interstitials and S vacancies in CdS layers (Sathaye and Sinha, 1976; Wu et al., 2010) under intrinsic conditions.

From the electrolytic bath containing 1.5 M cadmium nitrate tetrahydrate ($Cd(NO_3)_2 \cdot 4H_2O$) of 99.0 % purity and 0.0023 M tellurium dioxide (TeO_2) in 400 ml of DI water. 1150 nm thick *n*-CdTe layers were electrodeposited at 1400 mV on the glass/FTO/*n*-ZnS/*n*-CdS substrate at a bath temperature of 85±2℃ and pH of 2.00±0.02. Details of full characterisation of similar CdTe layers has been documented in the literature (Salim et al., 2015). After growth, the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe configuration was treated using $CdCl_2$+$Ga_2(SO_4)_3$ (GCT) at 430℃ for 20 min in air atmosphere (A.A. Ojo et al., 2017). Prior to the GCT, the $CdCl_2$+$Ga_2(SO_4)_3$ solution was prepared using aqueous solution containing

0.1 M $CdCl_2$ and 0.05 M $Ga_2(SO_4)_3$ in 20 ml plus 2.5 ml of concentrated HCl acid to initiate a reaction leading to gallium chloride ($GaCl_3$).

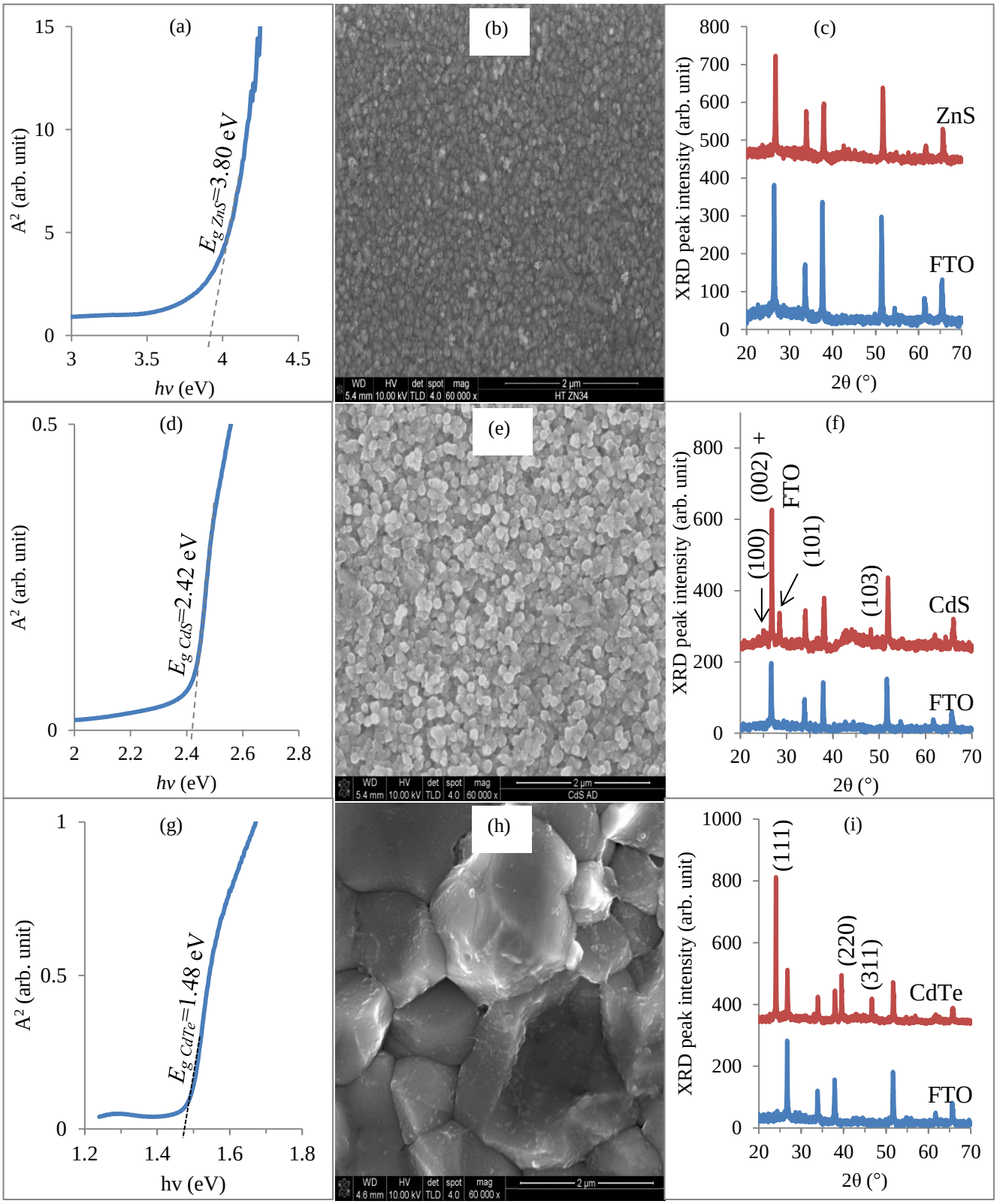

Figure 1: Typical optical absorption curves, SEM micrographs and XRD diffractions for post-growth treated (a-c) ZnS, (d-f) CdS and (g-i) CdTe layers produced by electrodeposition.

The main highlights of the gallium incorporation are the dissolution and out-diffusion of tellurium precipitation in CdTe (Fernández, 2003; Sochinskii et al., 1993). Further to this, increase in donor concentration with the incorporation of Ga atoms in Cd sites (Ga_{Cd}) plus release of free electrons and further improvement in fabricated device properties, recrystallization of the crystal lattice were documented amongst others (A.A. Ojo et al., 2017; Ojo and Dharmadasa, 2017; Olusola et al., 2017).

Figure 1 (a-c) shows the graph of absorbance square against photon energy, SEM micrograph and XRD diffraction of ZnS, (d-f) for CdS and (g-i) for CdTe. Prior to metallisation, acid etching of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were performed using a solution containing $K_2Cr_2O_7$ and concentrated H_2SO_4 for acid etching and an aqueous solution containing NaOH and $Na_2S_2O_3$ was utilised for alkaline etching for 2 s and 2 min respectively to improve the metal/semiconductor contact (Dharmadasa et al., 1987). The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were rinsed in DI-water in-between etching and afterwards. The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were transferred to a high vacuum system in order to deposit 100 nm thick Au contacts of 2 mm diameter on the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe configuration.

2.2 Graded bandgap configuration

Figure 2 shows the resulting glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device band diagram based on the knowledge harnessed from the literature on the conduction type of incorporated semiconductor layers after post-growth treatment (Abdul-Manaf et al., 2015; Madugu et al., 2016; Salim et al., 2015). Also incorporated in Figure 2 is the Fermi level pinning position at the *n*-CdTe/metal interfaces (Dharmadasa et al., 1998).

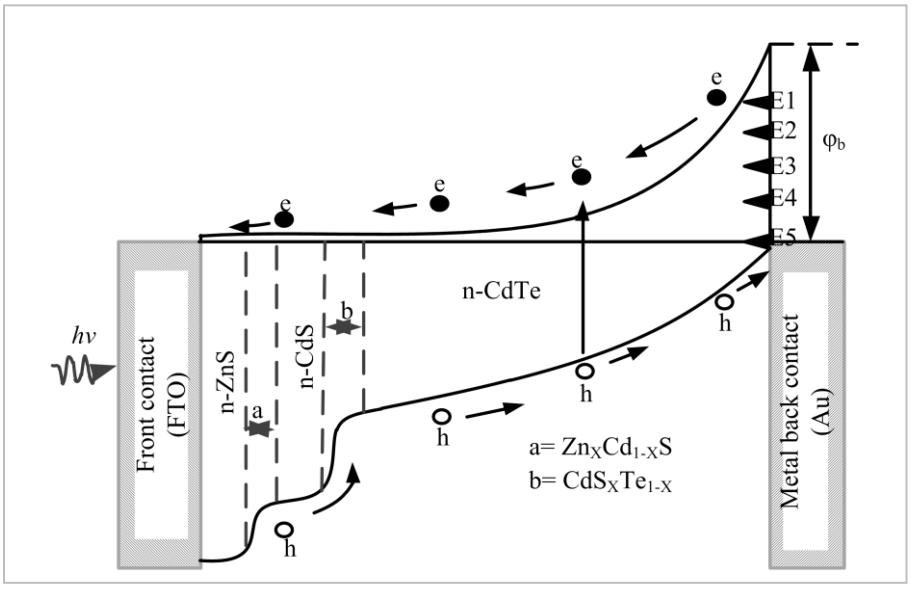

Figure 2: A typical band diagram of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device configuration.

As shown in Figure 2, the incorporation of ZnS buffer layer to the CdS/CdTe architecture results in the formation of *n*-ZnS/*n*-CdS/*n*-CdTe graded bandgap (GBG) device structure in addition to providing a smoother surface for CdS to grow. It should be noted that in-between successively deposited semiconductor layers the formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} is attributed to the interdiffusion of elemental Zn & Cd (Oladeji and Chow, 2005) and S & Te (Li et al., 2014) respectively during the annealing process.

Asides from the incorporation of semiconductor layers with different bandgap energies, the formation of the ternary compounds also participate in the bandgap grading due to the continuous band bending. It should be noted that the main electric field in the explored glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device architecture is formed at the large Schottky barrier (SB) at the *n*-CdTe/Au (semiconductor/metal) interface. The depletion region which propagates across all the layers as depicted by the continuous band bending in Figure 2 is responsible for the effective separation of the photogenerated e-h pairs to avoid recombination. Other advantages of the GBG configuration includes increase in the possibility of harnessing photons across the UV, Vis and IR regions of the solar spectrum, reduction/elimination of thermalisation of "hot carriers" due to shared photon absorption at different regions of the solar cell (Dharmadasa et al., 2011) and the improvement of electron-hole (e-h) pairs collection due to the presence of continuous electric field (or depletion width) spanning the whole width of the entire thickness of the solar cell to reduce recombination and generation (R&G) process (Dharmadasa, 2013). Additionally, Dharmadasa et al (Dharmadasa et al., 2015, 2011) also demonstrated the possible incorporation of impurity photovoltaic (PV) effect and impact ionisation in GBG solar cell configuration to reduce R&G and further increase photo-generated current density.

One of the major challenges of the *n*-CdTe/Au junction is the presence of defect levels (Dharmadasa et al., 1989; Sobiesierski et al., 1988) within the CdTe bandgap and the pinning of the Fermi level at one of the five experimentally observed defect levels (Dharmadasa et al., 1998). Literature shows that the richness of Cd in CdTe pins the Fermi level close to the valence band and resulting into higher barrier heights (Williams and Patterson, 1982).

2.3 Experimental technique

The main characterisation techniques utilised for the exploration of the electronic properties of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices are the current-voltage (I-V) and the capacitance-voltage (C-V) characteristic curves. It should be noted that robust technique such as Hall-effect measurement could not be utilised due to the presence of lower resistance path

of the underlying FTO substrate. The I-V characterisations under both dark and illuminated condition were carried out using fully automated Rera Solution PV simulation system. The system was calibrated using a standard reference cell RR267MON prior to measurements. The C-V measurements were carried out using fully automated HP system at a detector signal frequency of 1 MHz. For both the I-V and C-V measurements, the explore bias range was set between -1.0 V and +1.0 V at 300 K.

3 Assessment of fabricated devices

For the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices under investigation, the I-V measurements were performed under both dark and AM1.5 illuminated conditions.

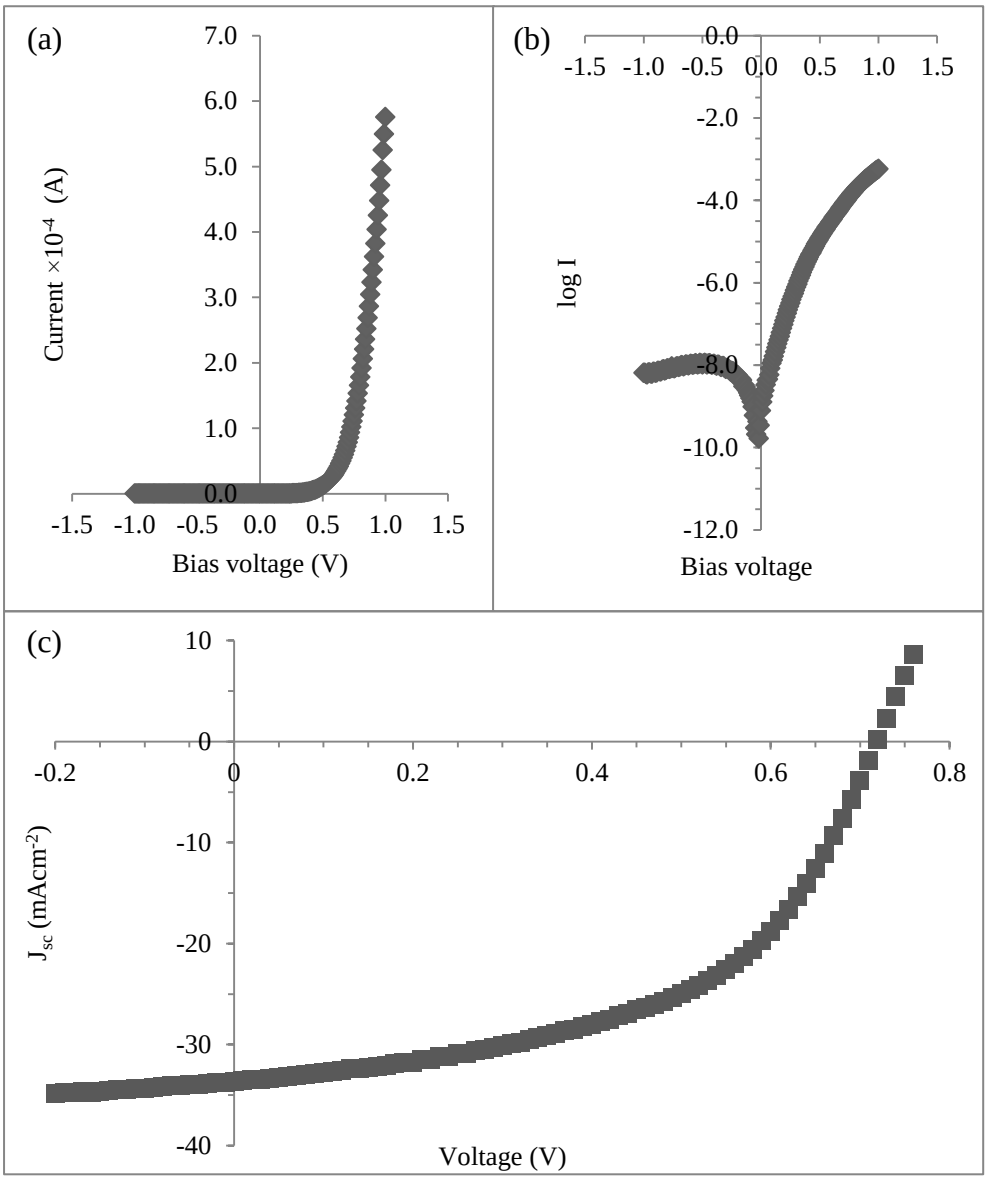

Figure 3: I-V characteristics of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device architecture under dark condition plotted in (a) Log-linear and (b) Linear-linear scales and (c) I-V plotted under AM1.5 condition for the cell with a conversion efficiency of 14.18%.

Under I-V dark condition, parameters such as the shunt resistance R_{sh}, series resistance R_s, rectification factor *RF*, reverse saturation current I_o, ideality factor *n*, and the barrier height ϕ_b were derived, while the effective Richardson constant (*A**) for CdTe was calculated to be 12 $Acm^{-2}K^{-2}$. While under AM1.5 illuminated condition, parameters such as short-circuit current density J_{sc}, open-circuit voltage V_{oc}, fill-factor *FF* and efficiency η were determined.

Figure 3 (a-b) shows the I-V curve of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device architecture under dark condition plotted in log-linear and linear-linear scales, while Figure 3 (c) shows the I-V plotted under AM1.5 condition. The summary of the obtained electronic parameters of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device is summarised in Table 1. From observation, the dark I-V section of Table 1 shows high R_{sh} value for the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device under consideration. This observation indicates the absence of shunt path which might be due to the incorporation of the ZnS and/or the quality of the electroplated semiconductor layer as regards to the inclusion of voids, gaps, high dislocation density within the semiconductor material (Soga, 2004).

Table 1: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cell.

I-V measurement under dark condition	
R_{sh} (kΩ)	>100
R_s (Ω)	470
log (R.F.)	4.8
I_o (A)	1.0×10^{-9}
n	1.60
Φ_b (eV)	>0.82
I-V measurement under AM1.5 illuminated condition	
I_{sc} (mA)	1.07
J_{sc} ($mAcm^{-2}$)	34.08
V_{oc} (mV)	730
Fill-factor	0.57
Efficiency (%)	14.18
DC and C-V measurements under dark condition	
$\rho\times10^3$ (Ω.cm)	1.13
(N_D-N_A) (cm^{-3})	7.79×10^{14}
(E_C-E_F) eV	~0.17
V_{bi} (eV)	1.1
C_o (pF)	280
W (nm)	1092.2
μ ($cm^2V^{-1}s^{-1}$)	7.07

The observed R_s value of 470 Ω is still considered quite high for this device. Further reduction is required to further increase the FF and the resulting conversion efficiency. The device also shows excellent log(*RF*) value greater than 3 orders of magnitude which is one of the characteristic property of high-efficiency solar cell (Dharmadasa, 2013). Furthermore, the observed *n* which lies in-between 1.00 and 2.00, which indicates that the current transport mechanism of the device is dominated by both thermionic emission and recombination & generation (R&G) processes in parallel (Sze and Ng, 2006). It should be noted that the *n* value of 1.00 and 2.00 indicate the domination of the current transport mechanism with thermionic emission and R&G respectively. While for n>2.00, the current transportation mechanism is not limited to thermionic emission and (R&G) but also due to the tunnelling of high energy electron through the barrier height (Verschraegen et al., 2005), which in turn causes a reduction in the barrier height ϕ_b. It should be noted that the actual potential barrier height may exceed the estimated ϕ_b of >0.82 eV which is being influenced by the high *n* of 1.60.

Under AM1.5 illumination condition, the calculated highest conversion efficiency η observed was 14.18% owing to the J_{sc} of 34 mAcm^{-2}, V_{oc} of 730 mV and *FF* of 0.57 obtained from the I-V curve. It should be noted that the high Shockley–Queisser limit of J_{sc} for single *p*-*n* junction (Shockley and Queisser, 1961) has been exceeded due to the multilayer graded bandgap configuration (Vos, 2000).

The capacitance-voltage (C-V) technique was performed to determine important device and material characteristics such as capacitance at zero bias C_o, depletion layer width at zero bias (*W*), Fermi level position (E_C-E_F), built-in potential (V_{bi}), doping concentration of the material (N_D-N_A), barrier height Φ_b and charge carrier mobility ($\mu_\perp$) of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device.

Figure 4 (a) shows the C-V characteristics of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device architecture under dark condition and Figure 4 (b) show the Mott-Schottky plot under dark conditions for the cell with a conversion efficiency of 14.18%. With reference to Figure 4 (a), a fairly constant capacitance of ~280 pF was observed along the reverse bias region, through the C_o up to ~0.5 V in the forward bias region. The fairly constant capacitance of the C-V curve is a clear indication that the device is fully depleted, in other words, the depletion width *W* is fairly similar to the thickness of the device at reverse bias region up to ~0.5 V in the forward bias region. For the device under investigation, the depletion width of 1092 nm at zero bias was calculated using equation (1) which is comparable to the device thickness of

~1150 nm. Above 0.5 V in the forward bias region, the capacitance increases with increase in forward bias voltage, resulting in a gradual reduction of the depletion width.

From the Mott-Schottky plot (see Figure 4 (b)) and equations (2)-(4), both the V_{bi} and (N_D-N_A) can be determined. Similar to the C-V plot, a fairly constant C^{-2} capacitance was also noticeable in the Mott-Schottky plot (see Figure 4 (b)) from which the doping of the semiconductor layer cannot be evaluated. But above the ~0.5 V under forward bias condition, the calculated (N_D-N_A) of 7.79×10^{14} (cm^{-3}) is mainly within the *n*-CdTe layer.

$$C_0 = \frac{\varepsilon_r \varepsilon_0}{W} \tag{1}$$

$$C^{-2} = \frac{2}{\varepsilon_s e A^2 N_D}(V_R + V_{bi}) \tag{2}$$

$$N_D = \frac{2}{\varepsilon_r \varepsilon_o e A^2 * slope} \tag{3}$$

$$slope = \frac{2}{\varepsilon_s e N_D A^2} \tag{4}$$

where capacitance is C, built-in potential is V_{bi}, reverse bias voltage is V_R, the contact area is A, the electronic charge is e, the permittivity of free space is ε_o, semiconductor permittivity is ε_s and relative permittivity (or dielectric constant) is ε_r. The ε_r value was taken to be 11 (Strzalkowski et al., 1976), while, the obtained gradient from the intercept of the Mott-Schottky plot shown in Figure 4 (b) was incorporated into equation (3).

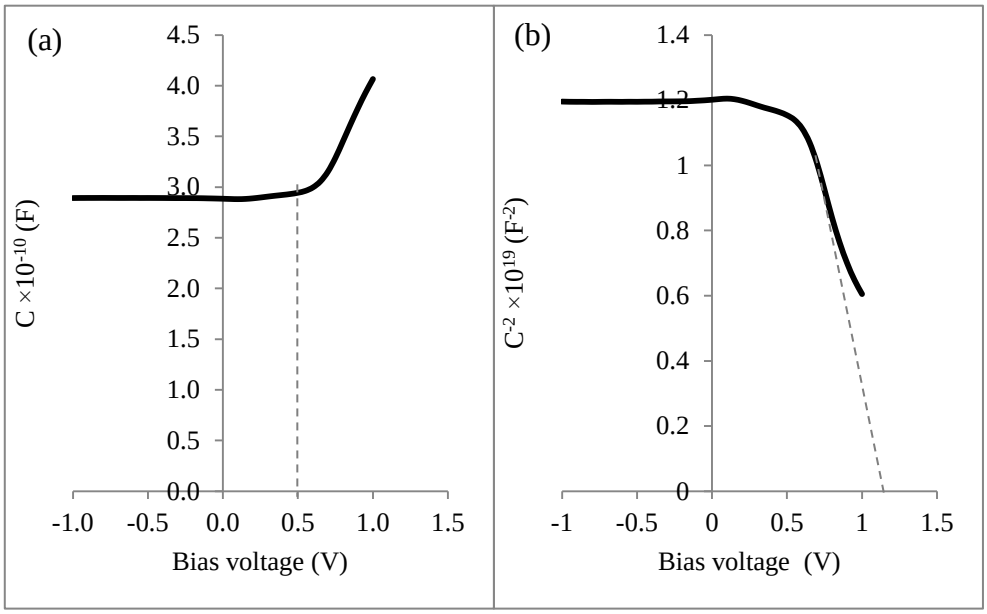

Figure 4: (a) C-V characteristics of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device architecture under dark condition and (b) Mott-Schottky plot under dark conditions for the cell with a conversion efficiency of 14.18%.

The calculated N_D of 7.79×10^{14} cm^{-3} and V_{bi} of ~1.1 eV falls within the region corresponding to the high-efficiency CdTe devices (~1.0×10^{14} to 5×10^{15}) cm^{-3} as documented in the literature (Britt and Ferekides, 1993; Ojo and Dharmadasa, 2016; Potlog et al., 2003).

The effective density of states in the conduction band (N_c) was calculated to be 7.92×10^{17} cm^{-3} using equation (5), where, k represents the Boltzmann's constant, m_e^* represent the effective electron mass, T represents the temperature, and h represents the Plank's constant. With the assumption that all donor atoms (N_D) are ionised ($n \approx N_D$) at room temperature, the charge carrier mobility $\mu_\perp$ calculated using equation (6) is 7.07 $cm^2V^{-1}s^{-1}$.

$$N_c = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{\frac{3}{2}} \tag{5}$$

$$\mu_\perp = \frac{\sigma}{N_D e} \tag{6}$$

4 Conclusion

The work presented in this communication successfully demonstrate the improvement of conversion efficiency by further optimisation of ZnS and CdS layer thicknesses and post-growth treatment with respect to the reference (Echendu and Dharmadasa, 2015). The

explored *n-n-n+SB* architecture incorporating *n*-ZnS buffer layer for CdS/CdTe- based devices show prospect of achieving even higher conversion efficiency. The utilisation of graded bandgap configuration and incorporation of large bandgap ZnS buffer layer increases the possibility of harnessing high energy photons both from the blue-end the red-end of the solar spectrum. The main highlight of graded bandgap solar cells is the short-circuit current density. It is therefore evident that improvements in other device parameters such as the reduction in R_s which will further improve the *FF* and $\eta\%$ are still required. Work is ongoing on the exploration of CdTe layer doping and other graded bandgap structure incorporating *p*-type buffer layer to further improve the electronic property of fabricated GBG devices.

Acknowledgement

The authors would like to acknowledge H. I. Salim, O. I. Olusola and M. L. Madugu for their contributions. The principal author wishes to thank Ekiti State University, Ado Ekiti Tertiary Education Fund (TETFund) Nigeria and Sheffield Hallam University for their support in undertaking this research. Nigeria is also acknowledged for their financial support.

References

Abdul-Manaf, N.A., Weerasinghe, A.R., Echendu, O.K., Dharmadasa, I.M., 2015. Electro-plating and characterisation of cadmium sulphide thin films using ammonium thiosulphate as the sulphur source. J. Mater. Sci. Mater. Electron. 26, 2418–2429. doi:10.1007/s10854-015-2700-5

Basol, B.M., 1984. High- efficiency electroplated heterojunction solar cell. J. Appl. Phys. 55, 601–603. doi:10.1063/1.333073

Britt, J., Ferekides, C., 1993. Thin-film CdS/CdTe solar cell with 15.8% efficiency. Appl. Phys. Lett. 62, 2851–2852. doi:10.1063/1.109629

Colegrove, E., Banai, R., Blissett, C., Buurma, C., Ellsworth, J., Morley, M., Barnes, S., Gilmore, C., Bergeson, J.D., Dhere, R., Scott, M., Gessert, T., Sivananthan, S., 2012. High-Efficiency Polycrystalline CdS/CdTe Solar Cells on Buffered Commercial TCO-Coated Glass. J. Electron. Mater. 41, 2833–2837. doi:10.1007/s11664-012-2100-z

Dharmadasa, I., Madugu, M., Olusola, O., Echendu, O., Fauzi, F., Diso, D., Weerasinghe, A., Druffel, T., Dharmadasa, R., Lavery, B., Jasinski, J., Krentsel, T., Sumanasekera, G., 2017. Electroplating of CdTe Thin Films from Cadmium Sulphate Precursor and Comparison of Layers Grown by 3-Electrode and 2-Electrode Systems. Coatings 7, 17. doi:10.3390/coatings7020017

Dharmadasa, I.M., 2013. Advances in thin-film solar cells. Pan Stanford, Singapore.

Dharmadasa, I.M., Bingham, P., Echendu, O.K., Salim, H.I., Druffel, T., Dharmadasa, R., Sumanasekera, G., Dharmasena, R., Dergacheva, M.B., Mit, K., Urazov, K., Bowen, L., Walls, M., Abbas, A., 2014. Fabrication of CdS/CdTe-Based Thin Film Solar Cells Using an Electrochemical Technique. Coatings 4, 380–415. doi:10.3390/coatings4030380

Dharmadasa, I.M., Blomfield, C.J., Scott, C.G., Coratger, R., Ajustron, F., Beauvillain, J., 1998. Metal/n-CdTe interfaces: A study of electrical contacts by deep level transient spectroscopy and ballistic electron emission microscopy. Solid. State. Electron. 42, 595–604. doi:10.1016/S0038-1101(97)00296-7

Dharmadasa, I.M., Elsherif, O., Tolan, G.J., 2011. Solar Cells Active in Complete Darkness. J. Phys. Conf. Ser. 286, 12041. doi:10.1088/1742-6596/286/1/012041

Dharmadasa, I.M., McLean, a B., Patterson, M.H., Williams, R.H., 1987. Schottky barriers and interface reactions on chemically etched n-CdTe single crystals. Semicond. Sci. Technol. 2, 404–412. doi:10.1088/0268-1242/2/7/003

Dharmadasa, I.M., Ojo, A.A., Salim, H.I., Dharmadasa, R., 2015. Next Generation Solar

Cells Based on Graded Bandgap Device Structures Utilising Rod-Type Nano-Materials. Energies 8, 5440–5458. doi:10.3390/en8065440

Dharmadasa, I.M., Thornton, J.M., Williams, R.H., 1989. Effects of surface treatments on Schottky barrier formation at metal/n-type CdTe contacts. Appl. Phys. Lett. 54, 137. doi:10.1063/1.101208

Echendu, O., Dharmadasa, I., 2015. Graded-Bandgap Solar Cells Using All-Electrodeposited ZnS, CdS and CdTe Thin-Films. Energies 8, 4416–4435. doi:10.3390/en8054416

Ferekides, C.S., Mamazza, R., Balasubramanian, U., Morel, D.L., 2005. Transparent conductors and buffer layers for CdTe solar cells. Thin Solid Films 480–481, 224–229. doi:10.1016/j.tsf.2004.11.094

Fernández, P., 2003. Defect structure and luminescence properties of CdTe based compounds. J. Optoelectron. Adv. Mater. 5, 369–388.

Granata, J.E., Sites, J.R., 2000. Effect of CdS thickness on CdS/CdTe quantum efficiency. Conf. Rec. Twenty Fifth IEEE Photovolt. Spec. Conf. 1996 853–856. doi:10.1109/PVSC.1996.564262

Gupta, A., Compaan, A.D., 2004. All-sputtered 14% CdS/CdTe thin-film solar cell with ZnO: Al transparent conducting oxide. Appl. Phys. Lett. 85, 684–686. doi:10.1063/1.1775289

Lee, J.S., Jun, Y.K., Im, H.B., 1987. Effects of CdS Film Thickness on the Photovoltaic Properties of Sintered CdS / CdTe Solar Cells. J. Electrochem. Soc. 134, 248–251. doi:10.1149/1.2100417

Li, C., Poplawsky, J., Paudel, N., Pennycook, T.J., Haigh, S.J., Al-Jassim, M.M., Yan, Y., Pennycook, S.J., 2014. S-Te Interdiffusion within Grains and Grain Boundaries in CdTe Solar Cells. IEEE J. Photovoltaics 4, 1636–1643. doi:10.1109/JPHOTOV.2014.2351622

Lincot, D., 2005. Electrodeposition of semiconductors. Thin Solid Films 487, 40–48. doi:10.1016/j.tsf.2005.01.032

Madugu, M.L., Olusola, O.I.-O., Echendu, O.K., Kadem, B., Dharmadasa, I.M., 2016. Intrinsic Doping in Electrodeposited ZnS Thin Films for Application in Large-Area Optoelectronic Devices. J. Electron. Mater. 45, 2710–2717. doi:10.1007/s11664-015-4310-7

Major, J.D., Durose, K., 2013. Co-sputtered Zn1-xSnXO buffer layers for CdTe thin film solar cells, in: 2013 IEEE 39th Photovoltaic Specialists Conference (PVSC). IEEE, pp. 1146–1149. doi:10.1109/PVSC.2013.6744342

Manzoli, a, Santos, M., Machado, S., 2007. A voltammetric and nanogravimetric study of ZnSe electrodeposition from an acid bath containing Zn(II) and Se(IV). Thin Solid

Films 515, 6860–6866. doi:10.1016/j.tsf.2007.02.030

Ojo, A.A., Dharmadasa, I.M., 2017. Effect of Gallium Doping on the Characteristic Properties of Polycrystalline Cadmium Telluride Thin Film. J. Electron. Mater. 46, 5127–5135. doi:10.1007/s11664-017-5519-4

Ojo, A.A., Dharmadasa, I.M., 2016. 15.3% efficient graded bandgap solar cells fabricated using electroplated CdS and CdTe thin films. Sol. Energy 136, 10–14. doi:10.1016/j.solener.2016.06.067

Ojo, A.A., Olusola, I.O., Dharmadasa, I.M., 2017. Effect of the inclusion of gallium in normal cadmium chloride treatment on electrical properties of CdS/CdTe solar cell. Mater. Chem. Phys. 196, 229–236. doi:10.1016/j.matchemphys.2017.04.053

Ojo, A.A., Salim, H.I., Olusola, O.I., Madugu, M.L., Dharmadasa, I.M., 2017. Effect of thickness: a case study of electrodeposited CdS in CdS/CdTe based photovoltaic devices. J. Mater. Sci. Mater. Electron. 28, 3254–3263. doi:10.1007/s10854-016-5916-0

Oladeji, I.O., Chow, L., 2005. Synthesis and processing of CdS/ZnS multilayer films for solar cell application. Thin Solid Films 474, 77–83. doi:10.1016/j.tsf.2004.08.114

Olusola, O.I., Madugu, M.L., Ojo, A.A., Dharmadasa, I.M., 2017. Investigating the effect of GaCl3 incorporation into the usual CdCl2 treatment on CdTe-based solar cell device structures. Curr. Appl. Phys. 17, 279–289. doi:10.1016/j.cap.2016.11.027

Ou, S.S., Stafsudd, O.M., Basol, B.M., 1984. Current transport mechanisms of electrochemically deposited CdS/CdTe heterojunction. Solid. State. Electron. 27, 21–25. doi:10.1016/0038-1101(84)90088-1

Potlog, T., Ghimpu, L., Gashin, P., Pudov, a., Nagle, T., Sites, J., 2003. Influence of annealing in different chlorides on the photovoltaic parameters of CdS/CdTe solar cells. Sol. Energy Mater. Sol. Cells 80, 327–334. doi:10.1016/j.solmat.2003.08.007

Salim, H.I., Patel, V., Abbas, a., Walls, J.M., Dharmadasa, I.M., 2015. Electrodeposition of CdTe thin films using nitrate precursor for applications in solar cells. J. Mater. Sci. Mater. Electron. 26, 3119–3128. doi:10.1007/s10854-015-2805-x

Sathaye, S.D., Sinha, A.P.B., 1976. Studies on thin films of cadmium sulphide prepared by a chemical deposition method. Thin Solid Films 37, 15–23. doi:10.1016/0040-6090(76)90531-9

Shockley, W., Queisser, H.J., 1961. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. J. Appl. Phys. 32, 510. doi:10.1063/1.1736034

Sobiesierski, Z., Dharmadasa, I.M., Williams, R.H., 1988. Correlation of photoluminescence measurements with the composition and electronic properties of chemically etched CdTe

surfaces. Appl. Phys. Lett. 53, 2623–2625. doi:10.1063/1.100178

Sochinskii, N.V. V, Babentsov, V.N.N., Tarbaev, N.I.I., Serrano, M.D., Dieguez, E., 1993. The low temperature annealing of p-cadmium telluride in gallium-bath. Mater. Res. Bull. 28, 1061–1066. doi:http://dx.doi.org/10.1016/0025-5408(93)90144-3

Soga, T., 2004. Nanostructured Materials for Solar Energy Conversion. Elsvier Sci. 2030, 614.

Strzalkowski, I., Joshi, S., Crowell, C.R., 1976. Dielectric constant and its temperature dependence for GaAs, CdTe, and ZnSe. Appl. Phys. Lett. 28, 350–352. doi:10.1063/1.88755

Sze, S.M., Ng, K.K., 2006. Physics of Semiconductor Devices. John Wiley & Sons, Inc., Hoboken, NJ, USA. doi:10.1002/0470068329

Verschraegen, J., Burgelman, M., Penndorf, J., 2005. Temperature dependence of the diode ideality factor in CuInS2-on-Cu-tape solar cells. Thin Solid Films 480–481, 307–311. doi:10.1016/j.tsf.2004.11.006

Vos, A. De, 2000. Detailed balance limit of the efficiency of tandem solar cells. J. Phys. D. Appl. Phys. 13, 839–846. doi:10.1088/0022-3727/13/5/018

Williams, R.H., Patterson, M.H., 1982. Fermi level pinning at metal- CdTe interfaces. Appl. Phys. Lett. 40, 484–486. doi:10.1063/1.93151

Wu, C., Jie, J., Wang, L., Yu, Y., Peng, Q., Zhang, X., Cai, J., Guo, H., Wu, D., Jiang, Y., 2010. Chlorine-doped n-type CdS nanowires with enhanced photoconductivity. Nanotechnology 21, 505203. doi:10.1088/0957-4484/22/6/069801

Wu, X., Sheldon, P., Mahathongdy, Y., Ribelin, R., Mason, a, Moutinho, H.R., Coutts, T.J., 1999. CdS/CdTe thin-film solar cell with a zinc stannate buffer layer. Aip Conf. Proc. 37–41. doi:10.1063/1.57910