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An investigation of the influence of different transparent conducting oxide substrates/front contacts on the performance of CdS/CdTe thin-film solar cells

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Abstract

CdS/CdTe/Au thin film solar cells have been fabricated on different transparent conducting oxide (TCO) substrates/front contacts to study the influence of these different TCOs on the performance of the devices. The TCOs used were ZnO, ZnO:Al and SnO_2:F. Under dark condition, all three device structures of the type glass/TCO/n-CdS/n-CdTe/Au n-n heterojunction+Schottky barrier, show interesting rectifying behaviors with rectification factors (RF) in the range ($10^{2.5} - 10^{5.0}$), Schottky barrier heights (Φ_B) greater than ($0.69 - 0.81$) eV, diode ideality factors (n) in the range ($1.85 - 2.12$), reverse saturation current densities (J_0) in the range ($3.18\times10^{-6} - 3.18\times10^{-8}$) Acm^{-2}, series resistances (R_s) in the range ($507 - 1114$) Ω and shunt resistances (R_{sh}) in the range ($0.84 - 271$) MΩ. The device structures glass/SnO_2:F/n-CdS/n-CdTe/Au and glass/FTO/ZnO:Al/n-CdS/n-CdTe/Au show the best performance with equal J_0 of 3.18×10^{-8} Acm^{-2}, equal $\Phi_B > 0.81$ eV, RF of $10^{4.9}$ and $10^{5.0}$, n value of 2.01 and 2.12, R_s of 615 Ω and 507 Ω and R_{sh} of 197 and 271 MΩ respectively. The device structure with ZnO shows the least performance. Under AM1.5 illumination, the device structure glass/SnO_2:F/n-CdS/n-CdTe/Au shows the best solar cell performance with open-circuit voltage of 630 mV, short-circuit current density of 23.5 mAcm^{-2}, fill factor of 0.44 and conversion efficiency of 6.5%, and is followed by the device structure with ZnO:Al showing a conversion efficiency of 6.0%. Suggested energy band diagrams of the devices as well as possible reasons for the observed trends in performance are presented and discussed.

1.0 Introduction

Thin-film CdS/CdTe solar cell and CdTe-based devices in general have continued to attract research interest, owing to the recent breakthroughs recorded by First Solar Company in drastically taking the conversion efficiency of CdTe-based solar cells from 16.5% where it stagnated for a long time to a record 22.1% recently for laboratory-scale cell [1]. This situation has been made possible because of the interesting qualities ascribed to CdTe which includes its good absorption coefficient of 10^4 - 10^5 cm^{-1}, its optimum bandgap of 1.45 eV, for one bandgap p-n junction, which matches the solar spectrum for effective photovoltaic conversion [2, 3], its ability to be made in both n-type and p-type electrical conductivity modes [4, 5], as well as its ability to be grown by a wide range of techniques [2, 3]. CdTe is not only employed in photovoltaic solar energy conversion, it also finds prominent application in radiation detection [6] due to its good carrier mobility-lifetime product.

For some time now, authors have been interested in the use of n-CdTe in CdS/CdTe solar cells instead of the conventionally used p-CdTe. What is needed in this case however, is a good Schottky barrier contact at the n-CdTe/metal interface. The major motivation here is the fact that Schottky barrier heights on n-CdTe/metal interfaces are known to be larger than those on p-CdTe/metal interfaces for a given metal [7]. This has also been reported to produce CdTe-based solar cells with reasonable conversion efficiencies [8 - 10]. Aside solar cell application, Schottky barrier device structures have other important technological applications because of their unique properties. For example, their low cut-in voltages (or threshold voltage) compared to those of p-n junction structures make them useful in low voltage applications, although this can be improved by making metal-insulator-semiconductor structures. Also, their low charge accumulation effect makes them useful in transistor-transistor logic (TTL) circuits to prevent the p-n junction transistor from going into deep saturation [7]. This makes for high speed circuits such as in detectors and fast switching devices [11]. They are also used for making metal-semiconductor field effect transistors (MESFETs) in which case, instead of using a p-n junction for a gate, a Schottky junction is used [12], as well as high electron mobility transistors (HEMTs) which exploit the difference in bandgap of two semiconductors of the same conductivity type in creating device active heterojunction [13] instead of p-n junction. Other characteristics include the fact that the current transport is by majority charge carriers [7]. For CdTe in particular, it has wider bandgap than Si and therefore produces higher Schottky barrier height than Si. Consequently, CdTe Schottky barrier device produces higher cut-in or threshold voltage compared to Si. The n-CdS/n-CdTe/metal n-n heterojunction+Schottky barrier devices can therefore be used not only as solar cells but also as fast switching diodes by properly encapsulating them to avoid light incidence.

In fabricating CdS/CdTe solar cells, a transparent conducting oxide (TCO) substrate is used as an ohmic front contact to the n-CdS with CdS/CdTe-based solar cells mostly operated in superstrate structure configuration. Major TCOs that have been used as front contacts are fluorine-doped tin oxide (SnO$_2$:F or simply FTO) and tin-doped indium oxide (ITO). Wu *et al.* have also used

cadmium stannate ($Cd_2Sn_2O_4$) as front contact [14]. The nature of front contact made on the CdS window material is known to have a profound effect on the I-V characteristics of a solar cell [15]. Sometimes CdS/CdTe solar cell researchers have introduced different TCOs as buffer layers between the front contact and CdS in pursuit of improvement in solar cell conversion efficiency. One major advantage of the buffer layer is that it provides a less spiky surface morphology for the growth of the usually thin CdS window layer to avoid possible short-circuit between the CdTe absorber material and the front contact. In addition, buffer layers are used to reduce lattice mismatch between two semiconducting layers. The different buffer layers used so far by researchers include $ZnSnO_x$ [14], ZnO [16], ZnO:Al [17] and SnO_2 [18]. With the buffer layer, photo-generated electrons will have to pass through the buffer layer before getting to the front contact and into an external circuit, thereby encountering certain resistance due to the resistivity of the buffer layer. This can reduce the fill factor and the short-circuit current density obtained from the solar cell. Therefore, in order to apply the buffer layer effectively, its resistivity must be as low as that of the front ohmic contact. Otherwise, the fill factor and the short-circuit current density of the device will be compromised. There is also an added advantage of introducing a buffer later. A wide bandgap semiconductor like ZnO helps in the gradual grading of the device bandgap, thus improving the charge carrier collection within the device.

In this paper, we rather consider using these buffer layers as front transparent contacts for the CdS/CdTe devices in order to determine which of the TCOs will produce the best device results which depends on the nature of contact they make with n-CdS window layer. This is aimed at revealing exactly how effective these TCOs can be when used as buffer layers. The TCOs under consideration here are ZnO, ZnO:Al and SnO_2:F all of which are also n-type materials.

Under dark condition, the current-voltage (I-V) characteristics of a Schottky barrier diode can be analyzed to obtain the various device parameters using the relevant equations (1) − (6) [7, 19]. By the thermionic emission theory for Schottky barrier diodes, the dark current density, J is given by

$$J = J_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{1}$$

where J_0 is the reverse saturation current density, V is the applied bias voltage, n is the diode ideality factor, q is electronic charge, k is Boltzmann constant and T is the absolute temperature. The reverse saturation current density is also given by

$$J_0 = A^* T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{2}$$

where Φ_B is the Schottky barrier height at the semiconductor/metal interface and A^* is the Richardson constant, generally given by

$$A^* = \frac{4\pi m_0 q k^2}{h^3} \frac{m_n^*}{m_0} = 120 \left(\frac{m_n^*}{m_0}\right) Acm^{-2}K^{-2} \tag{3}$$

where m_0 is electron rest mass, m_0^* is effective electron mass in the semiconductor and h is Planck's constant.

For CdTe, $\left(\frac{m_n^*}{m_0}\right)$ is taken to be 0.1, so that Eq.(3) yields $A^* = 12$ Acm^{-2}K^{-2}.

The reverse saturation current density (J_0) is experimentally obtained from the $\log J$ - V graph by extrapolating the linear part of the forward $\log J$ - V curve to the $\log J$ axis. The resulting intercept gives $\log J_0$. The Schottky barrier height (Φ_B) is obtained from Eq. (2) once J_0 is known. For forward bias greater than 75 mV, the exponential term $e^{\frac{qV}{nkT}} \gg 1$, in which case, Eq. (1) reduces to

$$J = J_0 \exp\left(\frac{qV}{nkT}\right) \tag{4}$$

By taking the natural logarithm of both sides of Eq. (4), we have

$$\ln J = \ln J_0 + \frac{qV}{nkT} \tag{5a}$$

Since J_0 is usually a very small value, of the order of 10^{-6} and below, the term $\ln J_0$ can be dropped so that

$$\ln J \cong \frac{qV}{nkT} \tag{5b}$$

Taking the derivative of Eq. (5b) with respect to V, then yield

$$n = \frac{q}{kT}\left(\frac{dV}{d \ln J}\right) \tag{6}$$

Thus from the graph of $\ln J$ vs. V, in the forward bias, the value of n can be obtained from the slope, $\left(\frac{d \ln J}{dV}\right)$.

From the graph of $\log J$ vs. V also, the diode rectification factor, RF, is obtained as a ratio of the forward current to the reverse current at a bias voltage of 1 V. From the linear – linear J-V curve, the series resistance, R_s, and shunt resistance, R_{sh}, are also obtained by taking the slope of the straight line portion of the forward and reverse current respectively.

Under illumination, the total diode (solar cell) current density, J_L is given by Eq. (7) [9], thus

$$J_L = J + J_R - J_{sc} \tag{7}$$

where J_R is the recombination current density and J_{sc} is the short-circuit current density.

If recombination is neglected under thermionic emission theory, then under short-circuit condition, we can combine Eqs. (4) and (7) to get

$$J_L = J - J_{sc} = J_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] - J_{sc} \tag{8}$$

In open-circuit condition, $V = V_{oc}$ and $J_L = 0$. Then, the open-circuit voltage, V_{oc} is obtained from Eq. (8) as

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_0} + 1\right) \tag{9}$$

The fill factor, FF of the solar cell is obtained from the 'squareness' of the $J - V$ curve in the fourth quadrant (for the form presented in this work in section 3) under illumination, while the conversion efficiency EFF is obtained from the relation:

$$EFF = \frac{V_{oc} \times J_{sc} \times FF}{P_{in}} \times 100\% \tag{10}$$

where $P_{in} = 100 \ mW\,cm^{-2}$ is the input power provided by the AM1.5 irradiation.

2.0 Experimental details

Cathodic electrodeposition of CdS and CdTe thin film layers used in this work was carried out from aqueous electrolytes containing appropriate precursors and in two-electrode configuration using graphite as the counter electrode. All chemicals used were laboratory reagent grade purchased from Sigma-Aldrich. For CdS films, the deposition electrolyte contained 0.3 M $CdCl_2$ and 0.03 M $Na_2S_2O_3$ in 800 ml of de-ionised water with pH adjusted to 1.80 ± 0.02 using dilute HCl. For CdTe deposition, the electrolyte contained 1.0 M $CdSO_4$, 0.001 M TeO_2 with 0.001 M each of high purity $CdCl_2$ and CdF_2, as sources of Cl and F for n-type doping. The pH of the electrolyte was adjusted to 2.00 ± 0.02 using dilute H_2SO_4. Each of the two films was first deposited on glass/SnO_2:F (g/SnO_2:F) substrate and then optimized before their use in device fabrication. Full details of preparation of deposition electrolytes, two-electrode deposition and characterization of CdS and CdTe thin films for device fabrication have been reported in recent publications [20 - 23]. CdS films were then deposited under the same conditions on the three different commercially available transparent conducting oxides (ZnO, ZnO:Al and SnO_2:F) whose influence on CdS/CdTe/Au devices is being investigated. The g/TCO/CdS structures were each dipped in an aqueous saturated solution of $CdCl_2$, allowed to dry and then annealed at 400 °C for 20 minute in air atmosphere. After cooling, the CdS films were washed in de-ionised

water and dried in a flow of nitrogen. CdTe thin films were in turn deposited, under similar conditions, on the annealed CdS films. Then the different g/TCO/CdS/CdTe were then dipped in saturated $CdCl_2$ aqueous solution, but this time with additional small amount of CdF_2, allowed to dry and then annealed at 450 °C for 15 minutes. This ($CdCl_2$+CdF_2) treatment has recently been reported to drastically improve the device quality of electrodeposited CdTe films [23]. After cooling, the samples were washed in de-ionised water.

To complete the device fabrication, the CdTe surfaces were etched in aqueous solutions of $K_2Cr_2O_7$ and ($NaOH$+$Na_2S_2O_3$) with rinsing in de-ionised water in-between, dried in a flow of N_2 and metallised with Au in vacuum, as has been reported recently [10, 22, 23]. The evaporated gold dots were 2 mm in diameter. The resulting g/TCO/n-CdS/n-CdTe/Au n-n heterojunction + Schottky barrier diodes were then characterized for their performance using current-voltage (I-V) measurement under dark and AM1.5 illumination conditions. The I-V characteristics of the diodes were recorded using a computerized Keithley 619 electrometer/multimeter (Keithley Instruments, Inc. OH, USA) and a solar simulator with a power density of 100 $mWcm^{-2}$.

The results of the performance of these device structures are presented and discussed in the following section.

3.0 Results and discussion

The graphs of *logI* vs. bias voltage for the three Schottky barrier devices under dark condition are shown in figure 1. Figure 1(a) clearly shows that the device structure with ZnO front contact has poor performance compared to the devices with ZnO:Al and SnO_2:F in figures 1(b) and 1(c) respectively. From the *logI* axis, one sees that this particular device structure with ZnO has reverse saturation current that is about two orders of magnitude higher than those of the other two device structures.

The rectification factor is also observed from figure 1(a) to be lowest for the g/ZnO/n-CdS/n-CdTe/Au device with about two orders of magnitude lower than those of the other two devices. The highest value of J_0 and lowest value of *RF* for this device with ZnO front contact indicates also the lowest Schottky barrier height, Φ_B (using Eq (2)), for the device compared to the g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO_2:F/n-CdS/n-CdTe/Au devices in figures 1(b) and 1(c). The values of Φ_B, J_0 and *RF* obtained from figure 1 for the three different device structures are presented in Table 1 for easy comparison. From the graph of $\ln J$ vs. V (where $\ln J = 2.303 \log J$ and $J = I/A$, with A as the device active area), the values of the diode ideality factor, n. for the three device structures were obtained using Eq (6). The results are also shown in Table 1. The *n*-values obtained are 1.85, 2.12 and 2.01 for the g/ZnO/n-CdS/n-CdTe/Au, g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO_2:F/n-CdS/n-CdTe/Au devices, respectively. The n values close to 2.00 show considerable recombination and generation process within the device structure. These large n values underestimate the potential barrier height present within the

device. Therefore the actual potential barrier present is greater than the calculated Φ_B values from the above equations.

Table 1: Device parameters in dark condition, for the g/TCO/n-CdS/n-CdTe/Au Schottky barrier diodes.

Device structure	Parameters under dark condition						
	Φ_B (eV)	n	J_0 (Acm^{-2})	RF	R_s (Ω)	R_{sh} (MΩ)	Threshold Voltage (V)
g/ZnO/n-CdS/n-CdTe/Au	> 0.69	1.85	3.18×10^{-6}	$10^{2.5}$	1114	0.843	0.60
g/ZnO:Al/n-CdS/n-CdTe/Au	> 0.81	2.12	3.18×10^{-8}	$10^{5.0}$	507	271	0.73
g/SnO$_2$:F/n-CdS/n-CdTe/Au	> 0.81	2.01	3.18×10^{-8}	$10^{4.9}$	615	197	0.72

Figures 2(a), (b) and (c) show the dark linear *J-V* graphs of g/ZnO/n-CdS/n-CdTe/Au, g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO$_2$:F/n-CdS/n-CdTe/Au Schottky diodes respectively. As described earlier, the series resistance, R_s, and shunt resistance, R_{sh}, of these diodes are obtained from these graphs. These values are also shown in Table 1 for comparison. A close look at the shapes of the forward currents in figure 2 shows that the g/ZnO/n-CdS/n-CdTe/Au diode has higher series resistance compared to the other two device structures. This diode also has the lowest threshold voltage, which is the voltage beyond which a sharp increase in forward current is observed. The respective threshold voltages estimate from figures 2(a), (b) and (c) are also given in Table 1. When the reverse bias currents are zoomed into, the shunt resistances of the three devices were obtained with values of 0.843 MΩ, 271 MΩ and 197 MΩ for the g/ZnO/n-CdS/n-CdTe/Au, g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO$_2$:F/n-CdS/n-CdTe/Au Schottky diodes respectively. It is clear that when R_s increases and R_{sh} decreases, the rectifying quality of the diodes deteriorates. Therefore the TCOs and any other buffer layers should be added to minimize R_s and maximize R_{sh} values. The processing steps should also be optimized to minimize recombination within the device and hence reduce the n values.

To critically and comprehensively analyse the behavior and performance of the three device structures under dark condition, we look closely at the device parameters in Table 1 as well as some of the important parameters of the three different TCOs and CdS as shown in Table 2. From Tables 1 and 2, one observes that the device with ZnO front contact has the lowest values of barrier height, rectification factor, shunt resistance, threshold voltage and conductivity compared to the devices with ZnO:Al and SnO$_2$:F front contacts. These lowest values of device parameters give a hint to the poor performance of this device as they indicate poor rectification property of the device. They are all related and principally arise from the lowest Schottky barrier height (Φ_B). The device is therefore leaky with very low shunt resistance. ZnO also introduces the highest R_s and hence degrades the solar cell performance. For the devices with ZnO:Al and SnO$_2$:F, these device parameters have improved resulting in their enhanced performance in

comparison. From Tables 1 and 2 again, one notices that this same device structure (with ZnO) shows the highest values of reverse saturation current density, series resistance and resistivity.

Table 2: Some reported important parameters of ZnO, ZnO:Al, SnO$_2$:F and CdS material layers.

Material layer	Bandgap, E_g (eV)	Electrical conductivity, σ (Ωcm)$^{-1}$	Electrical resistivity, ρ (Ωcm)	Work function, ϕ (eV)	Electron affinity, χ (eV)
ZnO	3.20 - 3.37 [24]	6.13×10^{-2} [24]	1.63×10^{1} [24]	4.71 [25]	4.20-4.60 [26]
ZnO:Al	3.31 - 3.37 [24]	1.06 – 11.23 [24]	$8.90 \times 10^{-2} - 9.43 \times 10^{-1}$ [24]	4.62 [25,27]	--
SnO$_2$:F	3.80-4.00 [28,29]	3.40×10^{2}-5.7×10^{3} [29,30]	$1.75 \times 10^{-4} - 2.94 \times 10^{-3}$ [29,30]	4.40 – 5.70 [31,32]	--
CdS	2.42 [20]	$2.04 \times 10^{-5} - 4.76 \times 10^{-5}$ [33]	$2.10 \times 10^{4} - 4.90 \times 10^{4}$ [33]	4.40-5.20 [34]	--

The highest leakage current (J_0) value of course arises from the observed lowest barrier height, lowest rectification factor and lowest shunt resistance all of which leads to current leakage in a diode. The highest series resistance in this device derives partly from the highest reported resistivity (ρ). A close look at the reported work function (ϕ) of these three TCOs and CdS in Table 2, indicates that ZnO and ZnO:Al have particular ϕ values compared to SnO$_2$:F and CdS with a range of reported values. This suggest that SnO$_2$:F and CdS have more easily adjustable work function compared to ZnO and ZnO:Al. Again the range of values of work function for SnO$_2$:F and CdS is similar. This also indicates that it is possible to have these two materials with equal or nearly equal work functions in a device. Considering the importance of work function in the formation of ohmic contacts to semiconductor surfaces, one could obtain a very good ohmic contact between SnO$_2$:F and CdS. This is most likely the case in these device structures under study if we consider the lowest work function values for SnO$_2$:F and CdS in Table 2. In this case, these two semiconductors have similar work function of 4.40 eV.

With this, we can then see what happens at the TCO/CdS interface in terms of the nature of electrical contact formed there with the aid of the energy band diagrams shown in figure 3. The difference in work function ($\Delta\phi$) between ZnO and CdS then becomes $\Delta\phi \approx 0.31$ eV and with the largest band offset. Between ZnO:Al and CdS we have $\Delta\phi \approx 0.22$ eV, and between SnO$_2$:F and CdS we have $\Delta\phi \approx 0$ eV. Thus with $\Delta\phi \approx 0.31$eV, the ZnO/CdS interface is not sufficiently ohmic and therefore exhibits a weak Schottky barrier, which competes with the main Schottky barrier at the n-CdTe/Au interface, and displaying high contact resistance. This may have resulted in the lowering of the "effective" barrier height in the device, hence the observed lowest barrier height in Table 1.

This contributes to the series resistance of the device with ZnO front contact as seen in Table 1. For the ZnO:Al front contact, $\Delta\phi$ and the band offset between ZnO:Al and CdS are lower compared to the case of ZnO. As a result the ZnO:Al/CdS interface has a better ohmic contact with low contact resistance resulting in reduced value of R_s in this device as seen in Table 1. The SnO_2:F/CdS interface also produces a good ohmic contact with low contact resistance as seen in Table 1. Thus one observes the two devices involving ZnO:Al and SnO_2:F showing very close device parameters in Table 1. The above situation therefore gives rise to two possible device structures for these three devices in terms of what happens at the TCO/CdS interface. The energy band diagrams of these two possible device structures are shown in figure 3.

Figure 4 shows the current density-voltage graphs of the same three devices under AM1.5 illumination condition. The solar cell device parameters extracted from these graphs are also presented in Table 3 for easy comparison. A look at the J-V graphs in figure 4 immediately shows the lowest V_{oc} and FF values produced by the device involving ZnO. The shape of the graph also indicates the high series resistance characterizing this same device. The reasons for these poor device parameters have already been given earlier based on the lowest "effective" Schottky barrier height, lowest rectification factor and highest resistivity of ZnO in this device. However, the J_{sc} is highest indicating the existence of low defects in the material of the device. In all, the device involving SnO_2:F (i.e. g/SnO_2:F/n-CdS/n-CdTe/Au) produces solar cell with the highest conversion efficiency as shown in Table 3, with V_{oc} = 630 mV, J_{sc} = 23.5 mAcm^{-2}, FF = 0.44, EFF = 6.5%, R_s = 221 Ω and R_{sh} = 8136 Ω. The next best solar cell is produced by the device structure g/ZnO:Al/n-CdS/n-CdTe/Au employing ZnO:Al with efficiency of 6.0%, V_{oc} = 610 mV, J_{sc} = 24.0 mAcm^{-2}, FF = 0.41, R_s = 225 Ω and R_{sh} = 8843 Ω. The device structure with ZnO produced an efficiency of 4.1%.

Table 3: AM 1.5 device parameters of the g/TCO/n-CdS/n-CdTe/Au Schottky barrier solar cells.

Device structure	Parameters under illumination					
	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	EFF (%)	R_s (Ω)	R_{sh} (Ω)
g/ZnO/n-CdS/n-CdTe/Au	410	31.5	0.32	4.1	221	5195
g/ZnO:Al/n-CdS/n-CdTe/Au	610	24.0	0.41	6.0	225	8843
g/SnO$_2$:F/n-CdS/n-CdTe/Au	630	23.5	0.44	6.5	221	8136

The highest J_{sc} value of 31.5 mAcm^{-2} and corresponding low series resistance of this device with ZnO is worthy of note even though it produced the overall lowest device performance. This high J_{sc} value with the corresponding low value of R_s suggests that ZnO is very photoactive (or photoconductive), such that its resistivity reduces drastically from 1114 Ω to 221 Ω under illumination. However, this gain in J_{sc} and the associated low R_s could not compensate for the low V_{oc}, low shunt resistance and low fill factor, all of which arise mainly from low Schottky barrier height and poor rectification factor, hence the observed overall poor device performance. This is important to note because what suffices at the end is the overall performance of the

device and not just a single device parameter. The observation of very high J_{sc} values in some solar cells but with overall low conversion efficiency is a common phenomenon from authors' experience. It should also be noted that these device structures are not ideal structures and therefore can deviate from normal ideal device behavior.

4.0 Conclusion

Fabrication of three n-n heterojunction+Schottky barrier devices of general structure g/TCO/n-CdS/n-CdTe/Au, using electrodeposited CdS and CdTe thin films and commercially available TCOs has been reported. The three different commercially available TCOs used were ZnO, ZnO:Al and SnO_2:F. Assessment of the resulting device structures under dark condition shows that all three devices show good diode rectification properties. However, the device structure involving ZnO resulted in diode with the lowest Schottky barrier height (Φ_B), lowest rectification factor (RF) and lowest threshold voltage. The two devices that involve ZnO:Al and SnO_2:F showed better device performance with closely similar device parameters. Under AM 1.5 illumination condition, the resulting solar cell with SnO_2:F produced the best cell efficiency of 6.5% and is followed by the device with ZnO:Al with an efficiency of 6.0%. The device made with ZnO still produced the lowest solar cell efficiency of 4.1%. The poor overall performance of the device structure g/ZnO/n-CdS/n-CdTe/Au compared to g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO_2:F/n-CdS/n-CdTe/Au is attributed to possible formation of undesired weak Schottky barrier at the ZnO/n-CdS interface (due to the relatively largest work function difference between ZnO and CdS) as well as to the highest reported resistivity of ZnO. These results will provide insight to device developers who employ TCOs either as buffer materials or as electrodes in choosing their desired TCOs for optimum device performance.

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Conflict of interest: The authors declare that they have no conflict of interest.

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Fig. 1: Dark *logI* vs. *V* graphs of (a) g/ZnO/n-CdS/n-CdTe/Au, (b) g/ZnO:Al/n-CdS/n-CdTe/Au and (c) g/SnO$_2$:F/n-CdS/n-CdTe/Au Schottky diodes respectively.

Fig. 2: Dark *J-V* graphs of g/ZnO/n-CdS/n-CdTe/Au, g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO$_2$:F/n-CdS/n-CdTe/Au Schottky diodes respectively.

Fig. 3: Proposed energy band diagrams of the TCO/n-CdS/-CdTe/Au Schottky barrier device (a) with low-resistance ohmic contact at the TCO/n-CdS interface and (b) with possible weak Schottky barrier at the TCO/n-CdS interface. The weak Schottky barrier junction is indicated with a pink circle in figure 3 (b).

Fig. 4: *J-V* graphs of g/ZnO/n-CdS/n-CdTe/Au, g/ZnO:Al/n-CdS/n-CdTe/Au and g/SnO$_2$:F/n-CdS/n-CdTe/Au Schottky barrier solar cells respectively, under AM 1.5 illumination.