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DHARMADASA, I <<http://orcid.org/0000-0001-7988-669X>> and OJO, A. A.

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# Unravelling complex nature of CdS/CdTe based thin film solar cells

I. M. Dharmadasa<sup>1</sup> · A. A. Ojo<sup>1</sup>

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**Abstract** Thin film solar cells based on CdS/CdTe hetero-structure has shown a drastic improvement changing from 16.5 to 22.1% efficiency during a short period of time from ~2013 to ~2016. This has happened in the industrial environment and the open research in this field has stagnated over a period of two decades prior to ~2013. Most of the issues of this hetero-structure were not clear to the photovoltaic (PV) community and research efforts should be directed to unravel its complex nature. Issues related to materials, post-growth treatment, chemical etching prior to metallisation and associated device physics are the main areas needing deeper understanding in order to further develop this device. After a comprehensive research programme in both academia and in industry on these materials, surfaces and interfaces and fully fabricated devices over a period of over three decades by the main author, the current knowledge as understood today, on all above mentioned complex issues are presented in this paper. Full understanding of this structure will enable PV developers to further improve the conversion efficiency beyond 22.1% for CdS/CdTe based solar cells.

## 1 Introduction

The use of CdS/CdTe hetero-structure as a thin film solar cell has attracted intense research from the photovoltaic (PV) community over a period of nearly four decades. Both materials have been grown using variety of low-temperature

and high-temperature growth techniques. The wide bandgap ( $E_g = 2.42$  eV) window material, CdS was mainly grown by chemical bath deposition (CBD) and narrow bandgap ( $E_g = 1.45$  eV) absorber material, CdTe was grown by over 14 different methods [1]. High efficiencies were achieved by the combination of CdS with CdTe layers grown by high temperature growth methods such as closed space sublimation (CSS) or close spaced vapour transport (CSVT) for a long period. Depending on the growth technique, material growth mechanisms, micro-structure and impurity inclusions are going to vary. Although there are a large number of publications reporting material characterisation, deep understanding is required on material issues such as defects and doping concentrations.

The next area needing deeper understanding is the post-growth chemical and heat treatment. The devices fabricated using as-made CdTe materials show poor device performance in the range ~ (0–6)% depending on the growth technique used. However, from 1976 [2], the researchers were aware of the drastic improvement of the device performance after heat treatment around 450 °C in air, in the presence of CdCl<sub>2</sub>. This was known as “CdCl<sub>2</sub> treatment” and device efficiencies improved to mid-teens achieving good solar cell performance. Although there were tremendous efforts to explore the complexity of changes during this treatment, full understanding has not yet been achieved.

The third main area of complexity comes from the CdTe/electrical back contact formation. It is essential to clean the CdTe surface after CdCl<sub>2</sub> treatment, and researchers were using different chemicals to clean the surface prior to metallisation. Various electrical contacts have been used to complete the devices and varying results have been reported in the literature [3]. Initial high efficiency, reproducibility and yield, stability and lifetime are main features of fully fabricated devices to establish. Some of these

✉ I. M. Dharmadasa  
Dharme@shu.ac.uk

<sup>1</sup> Materials and Engineering Research Institute, Sheffield Hallam University, Sheffield S1 1WB, UK

complex issues have been researched and reported [4] in the past and require full understanding in order to further develop the device.

All the three areas as mentioned above can be observed by experimentation, but the final stage consists of the most important interpretation of experimentally measured device results. These need deep consideration of solid state physics principles. Once the device structure is fabricated, it is a matter of routing measurements of devices using fully automated current–voltage ( $I$ – $V$ ), capacitance–voltage ( $C$ – $V$ ) and photo-response methods. These measurements allow the determination of device parameters including efficiency, but the recognition of the existing device and current transport mechanisms can be extremely challenging. In the past, CdS/CdTe hetero-structure was assumed as a simple p–n junction, and all device results were described accepting this device concept. However, since the CdTe material can easily exist in both n- and p-type electrical conduction, the situation is very complex. If the CdTe layer after post-growth treatment remains as a p-layer, then the simple p–n junction device is formed. However, when the CdTe layer remains n-type after growth and post-growth treatment, a very different device is formed. Because of the Fermi level (FL) pinning at n-CdTe/metal interface [3, 5] a large Schottky barrier (SB) can be formed at this interface. As a result, a CdS/CdTe/metal structure forms an n–n+SB structure with two PV active junctions. The photo-generated current components produced by these two rectifying interfaces (n–n and SB) add-up together, and therefore these two junctions are connected in parallel. Then, this is a tandem solar cell with two rectifying junctions [6, 7] and capable of producing improved performance when compared to a simple p–n junction device. This was first published in 2002 [7], and it is now becoming clearer from the latest research [8]. All the existing and relevant knowledge from the literature and new experimental results are combined to present in this paper.

## 2 Material issues

Thin CdS window layer, usually less than ~100 nm thick can be grown by various methods. Chemical bath deposition [9, 10], spray pyrolysis [11], sputtering [12, 13], close spaced sublimation [14] and electrodeposition [15] are some of the techniques frequently used in the PV solar cell development.

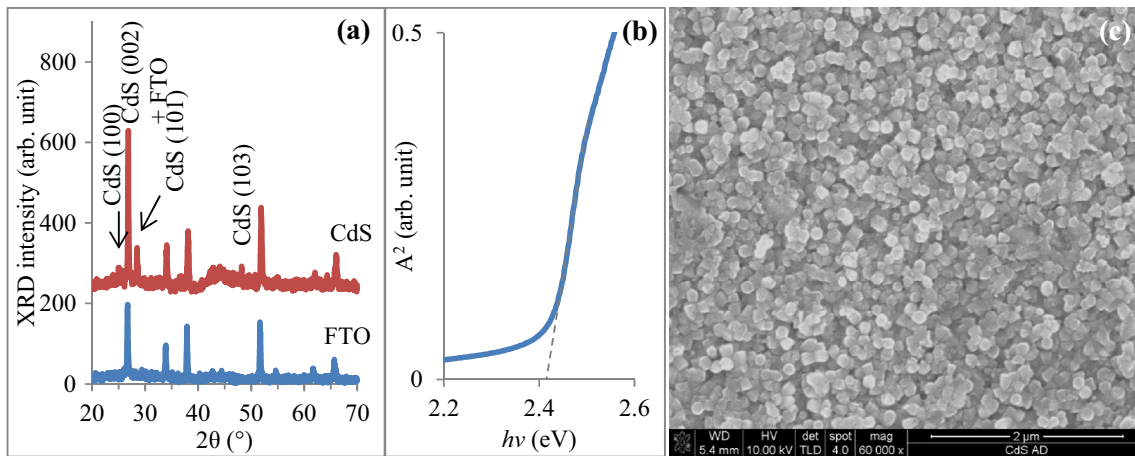
The CdTe absorber layer, is usually ~(1–4)  $\mu\text{m}$  thick and can be grown by many different techniques as reported in the literature [1]. Some of the most popular methods for growing CdTe layer are CSS [16], CSVT [17], sputtering [18] and electrodeposition [19, 20].

One of the main aims of PV research is to reduce the manufacturing cost. In order to achieve this, any research programme should be focused on low-cost, scalable and manufacturable growth method. During the late 1990s, BP Solar successfully demonstrated this by manufacturing nearly 1.0 m<sup>2</sup> solar panels with conversion efficiencies greater than 10% [21]. Since the electrodeposition of semiconductors fulfils all these three criteria, authors' work is mainly based on electroplated semiconductors and the work presented in this paper is on electroplated CdS and CdTe materials and devices. However, most of the ideas discussed in this paper are applicable to these two materials grown by other growth techniques, with some changes expected due to different growth conditions.

### 2.1 Growth of CdS by electrodeposition

Growth of CdS by electrodeposition has been carried out in the past and published widely in the literature [15, 22, 23]. This is usually carried out in an aqueous electrolyte containing cadmium source and sulphur source. Cadmium source is usually an aqueous solution of CdCl<sub>2</sub>, and the sulphur source can be Na<sub>2</sub>S<sub>2</sub>O<sub>3</sub> [23, 24], NH<sub>4</sub>S<sub>2</sub>O<sub>3</sub> [25] or NH<sub>2</sub>CSNH<sub>2</sub> [26, 27]. Both 3-electrode and 2-electrode systems have been used to deposit CdS layers on glass/conducting glass (CG) substrates which is the starting base for development of the CdS/CdTe solar cell. Both indium tin oxide (ITO) and fluorine doped tin oxide (FTO) have been used as the conducting glass, but most of the work is focused on less expensive and more stable glass/FTO surfaces. Electrodeposition provides a convenient and continuous process in a production line to produce CdS layers with any desired thickness. In electrodeposition, material use is highly efficient and the Cd-containing waste solution production is minimal as compared to other methods like chemical bath deposition.

The CdS layers electroplated on glass/FTO surfaces show uniform cover and well adhesive properties. Since the material is usually grown at temperatures below 85 °C, these layers need to undergo heat treatment in air at ~400 °C for ~20 min, before using in device fabrication. As-deposited layers have a mixture of both cubic and hexagonal CdS phases, but after heat treatment, materials show only the hexagonal structure [28]. Typical examples of XRD patterns, optical absorption curves and SEM images of electrodeposited CdS thin films are shown in Fig. 1. Heat treated CdS layers with the thicknesses of ~100 nm consist of ~(20–40) nm crystallites covering FTO surface. These crystallites cluster together to form large agglomerations in these layers. The bandgap of the electroplated CdS layer is 2.42 eV, and SEM shows grains of ~(50–70) nm. In fact, because of the high electric fields present at FTO spikes during electroplating, the nucleation take place at



**Fig. 1** Typical **a** XRD spectrum, **b** optical absorption curve and **c** SEM micrograph of heat treated CdS layers grown by electroplating

these peak points first and grow as columns. The low temperature growth below  $\sim 85^\circ\text{C}$  also enhances the columnar growth due to lack of ionic motion in the lateral directions. Columnar growth formation has many advantages but it also create a disadvantage such as possible formation of pinholes at the grain boundaries. Photo-electro-chemical (PEC) cell measurements show [23, 25, 27] n-type electrical conductivity for all electroplated CdS layers.

## 2.2 Growth of CdTe by electrodeposition

The CdTe absorber layer has been electrodeposited widely in the past [19–21, 29, 30] from aqueous solutions of  $\text{CdSO}_4$  as the Cd source and  $\text{TeO}_2$  as the Te source. More recently,  $\text{Cd}(\text{NO}_3)_2$  [31] and  $\text{CdCl}_2$  [32] has also been used as the Cd source for electroplating CdTe. Both 3-electrode and 2-electrode systems have been used to deposit CdTe and it has been proven that CdTe layers grown from 2-electrode systems produce better devices [33]. The main reason to remove the reference electrode from the 3-electrode system is to avoid contamination of detrimental group-I impurities such as K and Ag. Commercial reference electrodes have an outer jacket of saturated KCl solution, and leakage of any K ions into the electrolyte in ppb and ppm levels drastically reduces the efficiency of the CdS/CdTe solar cell, very similar to the effect of Na, Cu and Ag [34].

Electroplated CdTe at  $\sim 85^\circ\text{C}$  and pH  $\sim 2.00$ , on glass/FTO/CdS surfaces show columnar growth of material. As-deposited CdTe consists of crystallites varying in size in the range (20–65) nm. These smaller crystallites gather together to form larger grains. As-deposited CdTe layers are cubic and show (111) preferential orientation. In order to use these layers in PV active devices, post growth heat treatment at  $400\text{--}450^\circ\text{C}$  for 20–10 min in air, in the presence of  $\text{CdCl}_2$  is essential. This process, the  $\text{CdCl}_2$

treatment, converts CdTe material into large columnar shaped crystals with few microns ( $\sim 1.0\text{--}4.0$ ) in size. During heat treatment, a drastic structural change occurs at  $385 \pm 5^\circ\text{C}$ , due to sudden melting of grain boundaries [35].

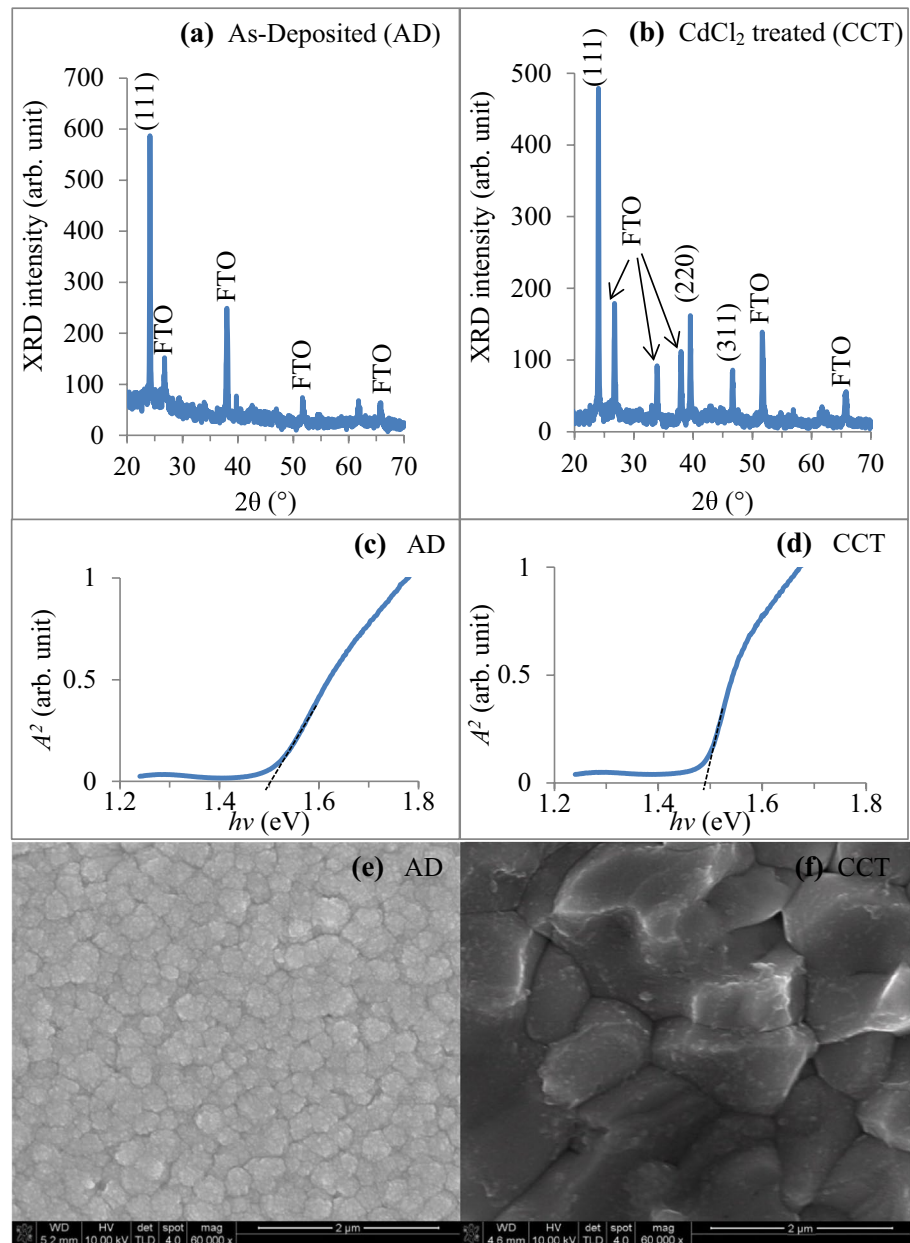
At this point the (111) peak collapse and other CdTe peaks appear showing random nature of CdTe crystals. Electroplated CdTe material show bandgap values varying in the range  $\sim (1.40\text{--}1.50)$  eV. The exact  $E_g$  value depends on the growth conditions, and the electrical conductivity can be easily changed to p-type or n-type by varying the growth conditions. Figure 2 shows typical XRD patterns, optical absorption curves and SEM images for as deposited and  $\text{CdCl}_2$  treated CdTe layers grown by electroplating. Figure 3 summarises the results of a comprehensive work carried out on electroplated CdTe, and these features are described in the following sections.

### 2.2.1 Stoichiometry of CdTe

Electroplating of CdTe layers are usually carried out with high concentration of Cd ions ( $\sim 0.5\text{--}2.0$  M) and very low concentrations of Te ( $\sim 1.0\text{--}5.0$  mM) in aqueous solutions. Typical temperature and pH values are  $\sim 85^\circ\text{C}$  and 2.00, and the solution is stirred with a moderate rate. With these conditions, stoichiometry of the CdTe layer can be changed drastically by varying the growth voltage ( $V_g$ ) applied to the cathode (glass/FTO/CdS) with respect to a graphite anode. The standard reduction potential ( $E_0$ ) values of Te and Cd are  $+0.551$  and  $-0.434$  V versus NHE respectively. This means that Te is easily discharged and deposited on the cathode than Cd. This is the main reason to maintain a very low concentration of Te with high concentration of Cd in the electrolyte.

As a result of the above property, Te or Te-rich CdTe layers are deposited at low cathodic voltages ( $V_g$ ). As the

**Fig. 2** Typical XRD patterns, optical absorption curves and SEM images for as-deposited and CdCl<sub>2</sub> treated CdTe layers produced by electroplating

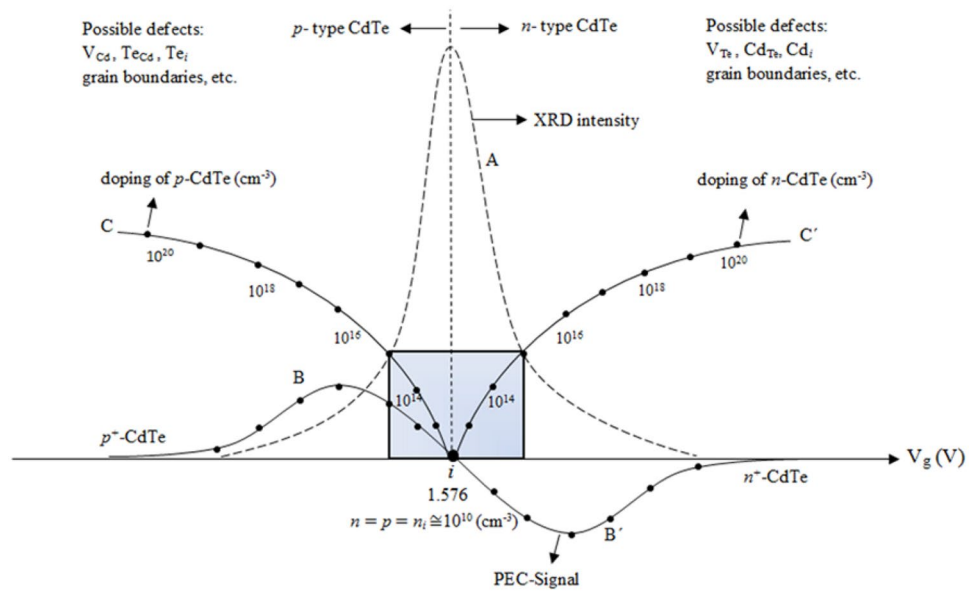


$V_g$  is gradually increased, more Cd is attracted to the cathode and CdTe is formed. Therefore, when  $V_g$  is increased from low values to high values, Te or Te-rich CdTe layers are deposited first. At a particular cathodic voltage ( $V_i$ ), the layer will pass through a 50:50 (Cd:Te) stoichiometric condition and move into the Cd-rich CdTe region. This has been experimentally observed using the highest intense (111) peak in XRD spectra. The curve A in Fig. 3 shows the intensity variation of CdTe (111) peak and the intensity is highest at the stoichiometric point ( $V_i$ ). As the  $V_g$  is moved away from i-point, the material becomes either Te-rich or Cd-rich. In both cases, CdTe crystallinity drastically reduces due to competing effects of crystallisation of two

phases in the layer. The position of the transition point ( $V_i$ ) is sensitive to the rate of Te ions addition to the electrolyte when other conditions are kept constant. As the Te addition rate is reduced, the i-point moves towards smaller  $V_g$  values. Under the experimental conditions used in this series of experiments,  $V_i$  value remained at 1.576 V with respect to the graphite anode.

The highest crystalline and stoichiometric CdTe layers are therefore obtained at  $V_i = 1.576$  V from this particular electrolytic bath. Therefore, the native defects present in these layers highly depend on the growth voltage. The materials grown at voltages below  $V_i$  are Te-rich and hence possible defects are cadmium vacancies ( $V_{Cd}$ ), tellurium

**Fig. 3** Graphical presentation of the summary of results obtained for electrodeposited CdTe layers. The inversion point, *i* at  $V_g = 1.576$  V produces stoichiometric and highly crystalline CdTe. The variation of electrical conduction type and doping concentration are shown by the curves BiB' and CiC' respectively. Electronic device quality materials can be grown in the shaded region and possible native defects in both p- and n-CdTe layers are also indicated on the two main regions



in cadmium sites ( $Te_{Cd}$ ) and tellurium interstitials ( $Te_i$ ). The layers grown at voltages above  $V_i$ , are Cd-rich and the expected defects are tellurium vacancies ( $V_{Te}$ ), cadmium in tellurium sites ( $Cd_{Te}$ ) and cadmium interstitials ( $Cd_i$ ). All electroplated materials are polycrystalline, and hence grain boundaries are common for all layers. Since the material discharge and deposition depends on the  $V_g$  value, the impurity profiles in deposited layers will be different. Therefore, optical and electrical properties can be very different in these Te-rich, stoichiometric and Cd-rich CdTe layers. For obvious reasons, the material should be highly crystalline and more suitable for fabricating better solar cells, when CdTe layers are grown in the vicinity of  $V_i$ , within the shaded region in Fig. 3. However, it should also be noted that the electrical conductivity is low for undoped CdTe grown close to  $V_i$ .

2.2.2 Electrical conductivity type of CdTe

Electrical conductivity type changes have been carefully explored and the natural trend has been established for un-doped CdTe layers. Conventional Hall Effect experiments cannot be performed on thin films grown on conducting glasses due to electric current passing through the lowest resistive path, the conducting glass. Therefore, the only alternative to determine electrical conductivity type is using photoelectrochemical (PEC) cell measurements. In this method, the required layer is immersed in a suitable electrolyte to form a solid/liquid junction. These junctions are equivalent to weak Schottky diodes and the open circuit voltage (OCV) of the junction can be measured observing the potential of the junction under dark and illuminated conditions. These voltages with respect

to a second electrode (graphite rod) immersed in the same electrolyte can be measured using a digital voltmeter. The difference between these two voltages provides the OCV of the solid/liquid junction or the PEC signal. The sign of the PEC signal measured depends on the direction of band bending at solid/liquid interface and provides information on the electrical conductivity type of the solid material. This system can be easily calibrated using known materials such as n-CdS and n-type or p-type Si wafer. The knowledge of electrical conductivity type is essential in designing and fabricating PV solar cells and especially in interpreting experimentally observed device characteristics.

The graph BiB' in Fig. 3 shows the conductivity type variation of un-doped CdTe layers grown by electroplating as determined by PEC measurements. This conductivity type variation is mainly due to composition changes within the layer. At lower  $V_g$  values, Te-rich CdTe is deposited and show p-type electrical conduction. As the  $V_g$  value increases, more Cd is deposited and the Cd-rich CdTe layer becomes n-type in electrical conduction. At the transition voltage ( $V_i$ ), intrinsic CdTe layers are produced and this  $V_i$  is sensitive to the Te concentration in the solution. For low concentration of Te, (i) point moves to the low  $V_g$  values, but for a particular method of Te addition,  $V_i$  remains constant. CdTe layers grown in two regions should have very different defect distributions as described above and indicated in Fig. 3. Therefore, their optical and electrical properties are different and behave differently after heat treatment in the presence of  $CdCl_2$ .

Addition of external n-type dopants such as halogens (Cl, F, I) and group-III elements (Ga, In), and p-type dopants such as group-I and group-V elements [36], into the electrolyte can make the situation more complex. The

n-type or p-type external doping combined with intrinsic composition dependent doping could produce un-predictable final doping profile depending on dopants' relative concentrations and heat treatment conditions used. Self-compensation can play a dominant role in CdTe [36].

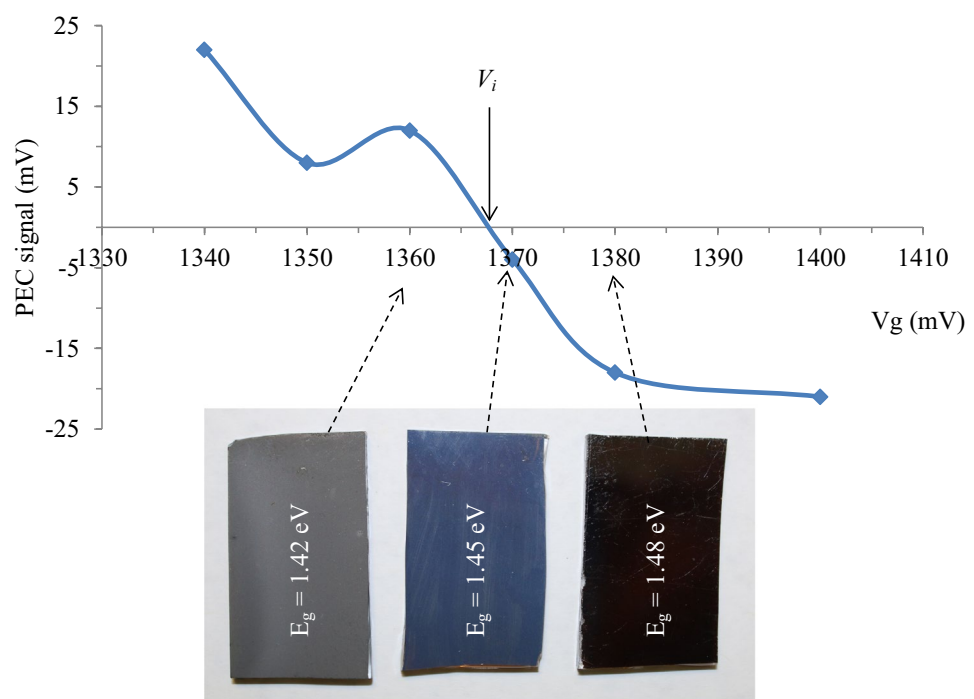
### 2.2.3 Doping variation in CdTe

The electrical conductivity type changes as described above, using composition variation in un-doped CdTe is an excellent in-built method for variation of the doping concentration. Possible trend in doping concentrations are given by the curve CiC' in Fig. 3. At the i-point, the material is stoichiometric and insulating since the PEC signal becomes zero. This material can be considered as an intrinsic CdTe, but material is not 100% pure CdTe according to the definition of intrinsic semiconductors. At this point, available number of acceptors and donors are equal in number and therefore material shows insulating properties due to compensation. As the material changes, its composition towards Te-rich or Cd-rich conditions, the p-type or n-type doping is increased. The numerical figures shown on the curve CiC' are some possible examples and  $10^{13}$ – $10^{15}$   $\text{cm}^{-3}$  doping range could arise within the shaded region. All high efficiency CdTe solar cells have experimentally measured doping concentrations in this range [8, 37, 38]. Therefore electroplating provides a good method of controlling doping concentrations in CdTe without adding any external dopant to the material.

### 2.2.4 Fine tuning of CdTe growth conditions

It is now highly relevant to explore the preparation of CdTe layers grown very close to the  $V_i$ . The appearance of CdTe layers grown at  $(V_i - \Delta V)$ ,  $V_i$  and  $(V_i + \Delta V)$  are presented in Fig. 4. These results are produced from a different electrolytic bath with less Te concentration and therefore, as mentioned earlier  $V_i$  has reduced to 1.368 V. The colour of the layers changes from dark to light–dark and honey-colour and transparent. As described later in Sect. 5 these layers produce varying solar cell efficiencies. The best devices come from Cd-rich, honey-colour and transparent layers. Accurate bandgap measurements also show that the  $E_g$  values vary in the range  $\sim 1.42$  to  $\sim 1.48$  eV in this narrow region. These bandgap values are also indicated in Fig. 4, with their physical appearance. The darker colour comes from Te-richness when grown at  $(V_i - \Delta V)$  cathodic voltages. Since the Te has the ease of deposition during electroplating, elemental Te precipitation at nm scale takes place creating the darker colour to thin film CdTe. Te precipitation has been observed and reported by many researchers from X-ray and  $\gamma$ -ray detector community [39–41] for melt-grown CdTe bulk material. Therefore, this must be a unique property of CdTe, and Te precipitation should be common during any growth method. The level of precipitation may vary according to growth conditions used and may not be possible to detect this nm scale precipitations using commonly used analytical techniques. As described later, this Te precipitation during CdTe growth should be avoided to produce high efficiency solar cells.

**Fig. 4** The physical appearance of CdTe layers grown at the vicinity of the transition voltage ( $V_i = 1.368$  V). Colour of the CdTe layer varies from dark, light–dark to honey-colour and transparent when moved from Te-richness to Cd-richness. Average bandgap values of five measurements are also indicated for layers grown in this region



### 3 Post-growth heat treatment

According to the theoretical calculations carried out by Schockley and Queisser [42] in the early 1960s, based on one bandgap p–n junctions, materials with bandgaps close to 1.45 eV have the potential of achieving highest efficiencies ~30%. CdTe is one of the materials with this capability and hence worldwide research was focused on this material. Research work was mainly directed towards hetero-junctions based on CdS window material and CdTe absorber material. CdS material is always n-type in electrical conduction, but CdTe can be easily grown with either p-type or n-type electrical conduction. The research focus was to develop n-CdS/p-CdTe hetero-junctions and the observation of high efficiencies after post-growth heat treatment at ~450 °C in air, in the presence of CdCl<sub>2</sub> in 1976 [2] attracted renewed interest of the wider PV community. This treatment was known as “CdCl<sub>2</sub> treatment” and continuously used in different forms to develop CdS/CdTe solar cells. Research was also aimed at understanding what really happens to the material during this treatment.

CdCl<sub>2</sub> addition to the thin films of CdTe was carried out in many different ways. One method was to add CdCl<sub>2</sub> into the CdSO<sub>4</sub> electrolyte in the case of electroplating [21]. For many other growth methods, CdTe thin films were immersed in a CdCl<sub>2</sub> solution and allowed to dry before heat treatment. The CdCl<sub>2</sub> solution was prepared with varying concentrations and with methanol or water [4] as the solvent. Some researchers deposited solid CdCl<sub>2</sub> layers on top of CdTe surfaces using many different techniques such as vacuum evaporation [43], and in some cases CdCl<sub>2</sub> layer thickness was comparable to that of CdTe layer [44]. Literature also shows the use of Freon gas (CHF<sub>2</sub>Cl) to introduce Cl and F during post growth heat treatment of CdTe layer [45]. Other methods such as the use of HCl vapour to introduce Cl [46] during growth have also been reported.

#### 3.1 Summary of reported results on CdCl<sub>2</sub> treatment

Although the method of addition of CdCl<sub>2</sub> was very different, the improvement of the conversion efficiencies was always observed. Researchers have heat treated these layers in ambient like vacuum, air atmosphere, controlled oxygen atmosphere and in inert Ar, N or He atmospheres. It was found that the presence of O<sub>2</sub> is helpful in achieving high efficiencies after this heat treatment [47]. Research community has tried many other chlorides to replace CdCl<sub>2</sub> but the closest result was found only with MgCl<sub>2</sub> [48]. Researchers have also spent lot of time in optimising both the heat treatment temperature and treatment duration. This temperature varies in the range of ~400–450 °C with the duration of heating between ~20 and 10 min respectively [4].

There are numerous studies on the CdCl<sub>2</sub> treatment of CdTe layers and both material changes and device improvements have been reported [35, 49–51]. Depending on the studies carried out, various changes such as (a) re-crystallisation and grain growth, (b) interactions at CdS/CdTe interface, (c) enhancement of lifetime of charge carriers, (d) passivation of grain boundaries and (e) enhancement of device efficiencies are reported in the literature [4, 52].

Although there are some attempts to study the changes of electrical conductivity, doping concentrations and defects in CdTe layers, full understanding is still lacking. Consistent results on electrical conductivity and doping concentrations cannot be obtained for CdTe due to reasons discussed in Sect. 2.2.2 and 2.2.3. These are most important in critically analysing device characteristics, but the complications arise due to different material growth techniques. There are some recent efforts to understand CdCl<sub>2</sub> treatment, and these results are discussed in Sect. 3.2 to 3.4.

#### 3.2 Improvement of composition of CdTe layers

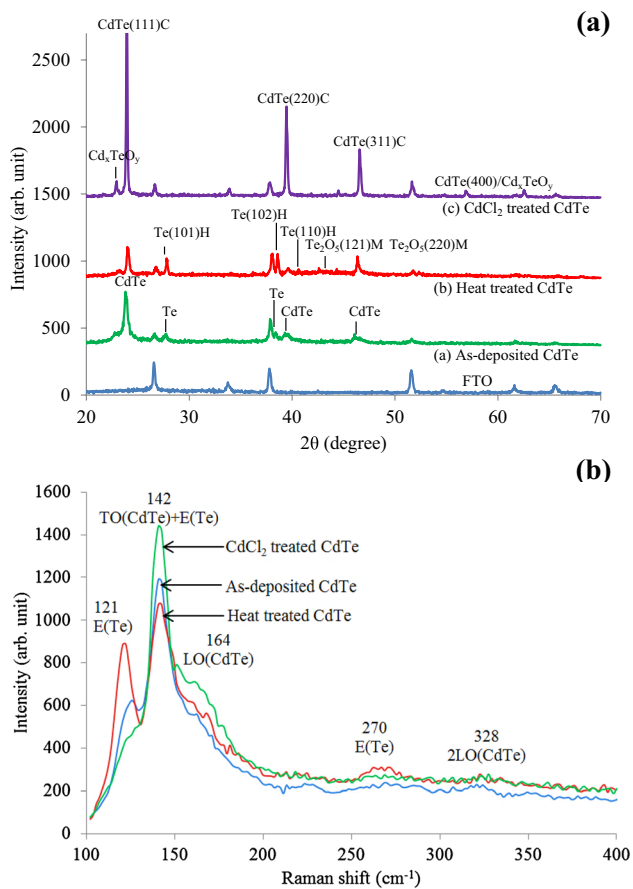
As described in Sect. 2.2.1, stoichiometry of CdTe material suffers from unique Te-precipitation taking place at nm scale. The level of precipitation will depend on the growth conditions used, and these excess Te is detrimental to device performance. Therefore, a recent project was carried out to study the variation of composition of CdTe during CdCl<sub>2</sub> treatment [53]. Both XRD and Raman studies have been used for this work and details are published in a recent paper [54]. Summary of these results are shown in Fig. 5.

For this work Te-rich CdTe layers were electroplated below the transition point ( $V_i$ ) and XRD and Raman studies were carried out to characterise the material. For as-deposited layers both XRD and Raman show presence of elemental Te in the layers. Heat treatment in air without CdCl<sub>2</sub> enhances the crystallisation of precipitated Te indicated by increasing elemental Te related XRD and Raman peaks as shown in Fig. 5. However, when the layers are heat treated in the presence of CdCl<sub>2</sub>, elemental Te is completely removed as detected by both XRD and Raman studies. In this case elemental Te, reacts with Cd from CdCl<sub>2</sub> to form CdTe, improving the stoichiometry of the CdTe layer. Furthermore, the presence of CdCl<sub>2</sub> during heat treatment, the CdTe layer converts from Te-richness towards Cd-richness, in order to produce high efficiency devices.

#### 3.3 Removal of defects from the material

A comprehensive photoluminescence (PL) study was also carried out in order to observe removal of defects during CdCl<sub>2</sub> treatment. The detailed results of this study are reported in a recent publication [55]. One example is





**Fig. 5** XRD and Raman spectra recorded for as-deposited, heat treated in air and CdCl<sub>2</sub> treated CdTe layers to demonstrate removal of excess Te during CdCl<sub>2</sub> treatment [54]

shown in Fig. 6, to highlight these effects for electroplated CdTe layers.

This work examined the defects distribution in the CdTe bandgap over the range of 0.55–eV (eV) below the conduction band minimum. The CdTe material was grown using a CdCl<sub>2</sub> aqueous solution and by electroplating. The first curve in Fig. 6a provides the defects structure for as-grown material with four main defects T1, T2, T3 and T4, and E<sub>g</sub> related peak. Material was CdCl<sub>2</sub> treated twice to observe the trends of removal of defects. First CdCl<sub>2</sub> treatment (treating the sample in 1% CdCl<sub>2</sub> aqueous solution, dry and heat treat at 440 °C for 8 min) followed by a second CdCl<sub>2</sub> treatment (treating the same sample in 1% CdCl<sub>2</sub> aqueous solution, dry and heat treat at 440 °C for 16 min) removes T1 and T3 completely and drastically reduce the distribution of T2 to a comparatively narrow PL peak. Similarly, CdCl<sub>2</sub> treatment produces a sharper E<sub>g</sub> peak ~1.51 eV, and reduces the defect concentration at T4 (1.39 eV). Figure 6b compares the final PL spectra for electroplated CdTe thin films to that of a commercially available CdTe wafer. This shows the capability of electroplating

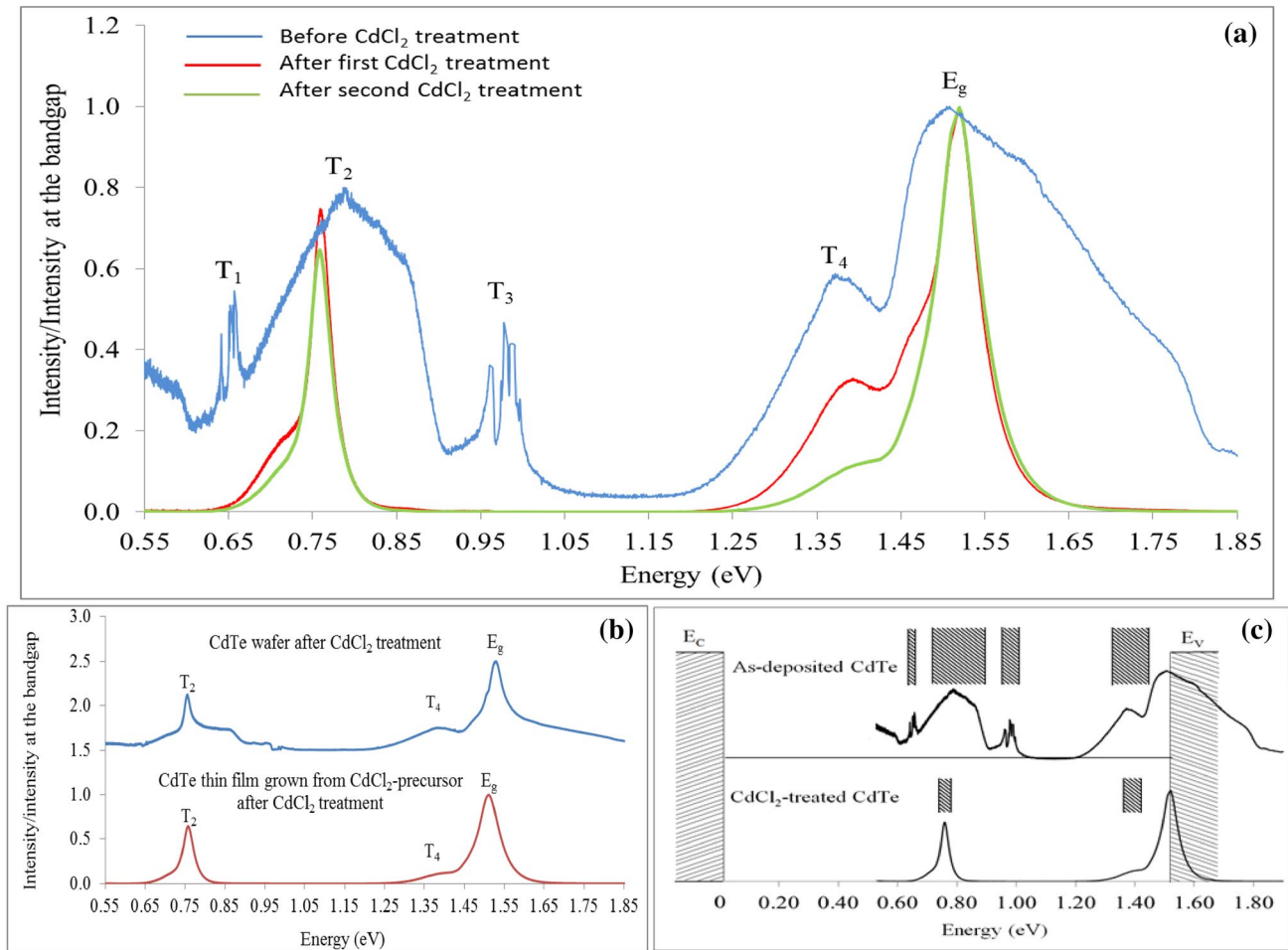
to produce high quality CdTe thin films comparable to commercially available bulk CdTe wafers. Figure 6c shows the defects distribution in the bandgap of as-deposited and CdCl<sub>2</sub> treated CdTe layers. Annealing out of defects is clear from these spectra during CdCl<sub>2</sub> treatment.

This shows the high quality of CdTe layers obtained from electroplating to fabricate thin film solar cells. One clear comment to make is the presence of defect level at  $0.74 \pm 0.02$  eV (T2), exactly at the mid-gap of CdTe. For PV applications, this is a detrimental defect in recombination and generation process, acting as a stepping stone. This should be completely removed in order to produce high performance devices. These defects are also related to the Te-richness [55, 56], and therefore to reduce these defects, material should be grown with Cd-richness, without Te-precipitation.

### 3.4 Enhancement of columnar nature of grains

Combining the knowledge available in the literature and the results observed within this comprehensive research programme, the latest understanding of the CdTe material is summarised in Fig. 3 [35]. CdTe thin films grown on glass/FTO/CdS surfaces, by low-temperature techniques such as electroplating and sputtering produce small crystallites in the range ~ (20–65) nm. These values are estimated using XRD results and Scherrer equation. The crystallites show preferential orientation along (111) and aggregate to form larger grains. These grains are usually arranged as columns, and grow normal to the glass/FTO/CdS surface. This growth temperature region has labelled as “Region-1” in Fig. 7 [35], and these materials can produce conversion efficiencies up to ~10% [57].

During the heat treatment in the presence of CdCl<sub>2</sub>, crystallinity of CdTe gradually increases in “Region-1” due to coalescing of crystalline nano-particles due to their large surface to volume ratio. Then, as the temperature gradually increase, a sudden structural change has been identified ~385 °C due to melting of grain boundaries of crystalline grains [35]. This happens due to presence of impurities such as excess Cd, Cl and O along grain boundaries and CdTe crystals remain as solids due to their high melting point of ~1093 °C. Melted grain boundaries allow CdTe crystals to change their orientations suddenly at ~385 °C, showing random orientations. The material solidified after this temperature shows a collapse of (111) peak and enhancement of other CdTe related peaks (220), (311) and (400). Relative intensities vary from sample to sample depending on the heat treatment conditions used. During heating, grains grow mainly upwards due to Oswald ripening, and pinholes can form due to formation of large grains. Therefore in “Region-2”, device efficiencies reduce due to short circuiting of devices through pinholes.



**Fig. 6** **a** PL spectra of as-deposited CdTe layers, grown from CdCl<sub>2</sub> precursor and the effects of subsequent CdCl<sub>2</sub> treatment in two steps [55]. **b** PL spectra of bulk CdTe wafers and electroplated CdTe after

CdCl<sub>2</sub> treatment and **c** the representation of defects distribution in as-made and CdCl<sub>2</sub> treated CdTe thin films. Note the drastic removal of defects from the bandgap of CdTe [55]

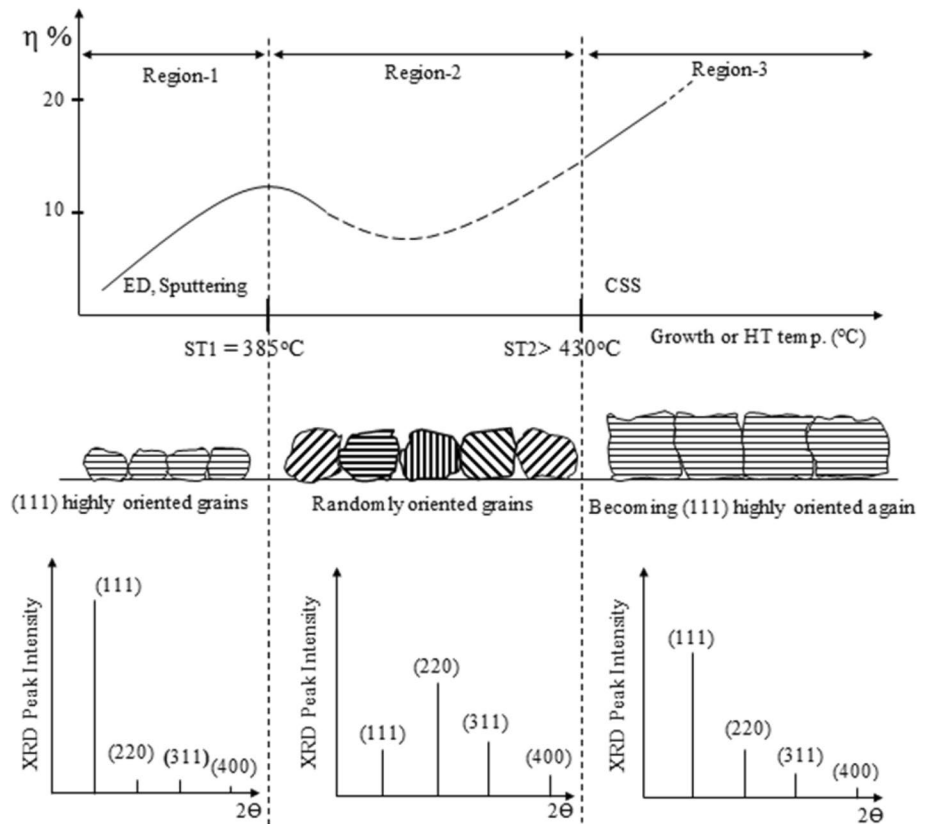
If the heat treatment continues, large crystalline grains grow continuously and gradually show again the (111) naturally preferred orientation. This does not show a sharp transition, but slowly change, increasing the crystal size and reducing pinholes at grain boundaries. A typical XRD spectrum will show, (111) preferred orientation returning back. These are the kind of layers produced by high temperature growth techniques such as CSS and CSVT. During CdCl<sub>2</sub> treatment, many changes occurs as described in Sect. 3.1, and the material at grain boundaries solidify with a different electronic quality from the CdTe material exist within crystalline grains. These CdTe layers are labelled as “Region-3” and capable of producing highest efficient solar cells.

#### 4 Chemical etching prior to metallisation

The next step of the processing of devices is the cleaning of glass/FTO/CdS/CdTe surface after post-growth CdCl<sub>2</sub> treatment. CdCl<sub>2</sub> residues and native oxides of CdTe can be present after this heat treatment, and usually cleaned by washing with de-ionized water and chemical etching, prior to deposition of the back electrical contacts.

Detailed studies on chemical etching have been carried out using CdTe wafers [3, 56, 58, 59]. Review articles show that acidic etchants preferentially removes metallic element, Cd and leave Te-rich CdTe surface. Bromine-methanol, nitric acid and phosphoric acid containing solutions (NP etch) are good examples for this type of etchants.

**Fig. 7** Schematic diagrams summarising CdTe grain growth patterns, corresponding XRD spectra and approximate solar cell efficiencies against growth or heat treatment temperature. Note the three regions identified with a sudden phase transition at  $ST1 = 385^\circ\text{C}$ , and a slow phase transition taking place after  $ST2 > 430^\circ\text{C}$  [35]



On the other hand alkaline solutions preferably removes non-metallic element, Te and leave Cd-rich CdTe surface. NaOH, KOH, hydrazine hydrate etc are good examples of these etchants. A few seconds etch in oxidizing etch (dilute  $\text{K}_2\text{Cr}_2\text{O}_7$  in  $\text{H}_2\text{SO}_4$ ) followed by  $\sim 2$  min treatment in reducing etch (aqueous solution of NaOH +  $\text{Na}_2\text{S}_2\text{O}_3$ ) proved to produce Cd-rich surfaces, leading to high Schottky barrier formation at n-CdTe/metal interfaces [3, 58–61].

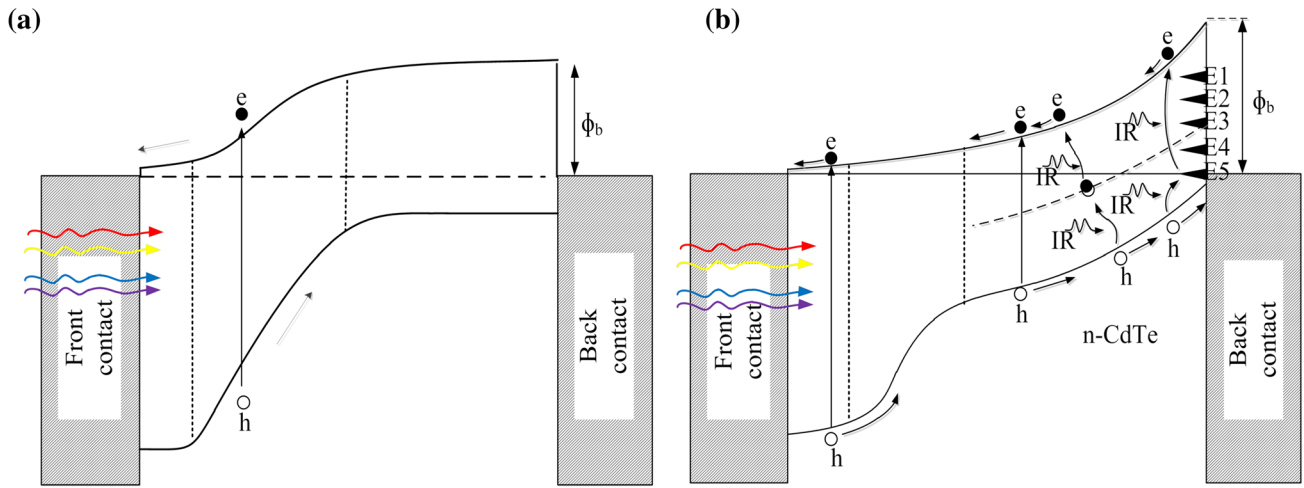
Bulk CdTe wafers and thin films should have very similar chemical reactions, except minor differences introduced by grain boundaries and less material etc. in the case of thin films. The literature is rich with etching of CdTe surfaces, and Br-methanol and NP etches are used to produce Te-rich surfaces [56, 62]. In order to produce Cd-rich surfaces, oxidised etch followed by reducing etch is used. Although hydrazine hydrate is effective in producing Cd-rich CdTe surfaces, its use is normally avoided due to its toxic nature. Surface science work has clearly shown these surface modifications and these results can be found in the literature [56]. It should be noted that only surface sensitive techniques such as Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and soft X-ray photoelectron spectroscopy (SXPS) should be used to examine the changes in chemically etched surfaces of CdTe. The thickness of these etched surfaces are in the order of  $\sim 100$  nm [3] or less and therefore less surface sensitive

techniques like EDX could produce inaccurate results and confusing conclusions on surface layers. This has been one of the reasons for misunderstanding of etched CdTe layers in the past. Due to these reasons, there was a controversy in this surface science area for a long time. Some groups reported that Te-rich surfaces produce high efficiencies, while others reported Cd-rich CdTe surfaces are needed to produce highest efficiencies. This has been re-visited and a recent publication [63, 64] has confirmed the requirement of Cd-rich surfaces to produce high efficiencies from CdS/CdTe system.

## 5 CdS/CdTe device Issues

Since the CdS window layer is always n-type and CdTe absorber layer can be either p-type or n-type in electrical conduction, it is highly relevant to discuss the complications could arise in this device structure. At the early stage of CdS/CdTe solar cell development, it is reasonable to assume this device as a simple n–p type rectifying heterojunction. Therefore, most of the published papers analysed and described the device characteristics based on an n–p junction as shown in Fig. 8a.

In parallel to the CdS/CdTe solar cell work, electrical contacts to n-type CdTe bulk materials were carried out



**Fig. 8** Energy band diagrams of two possible device configurations arising from glass/FTO/CdS/CdTe/metal system due to existence of CdTe in p-type and n-type conduction forms [7, 35, 63]

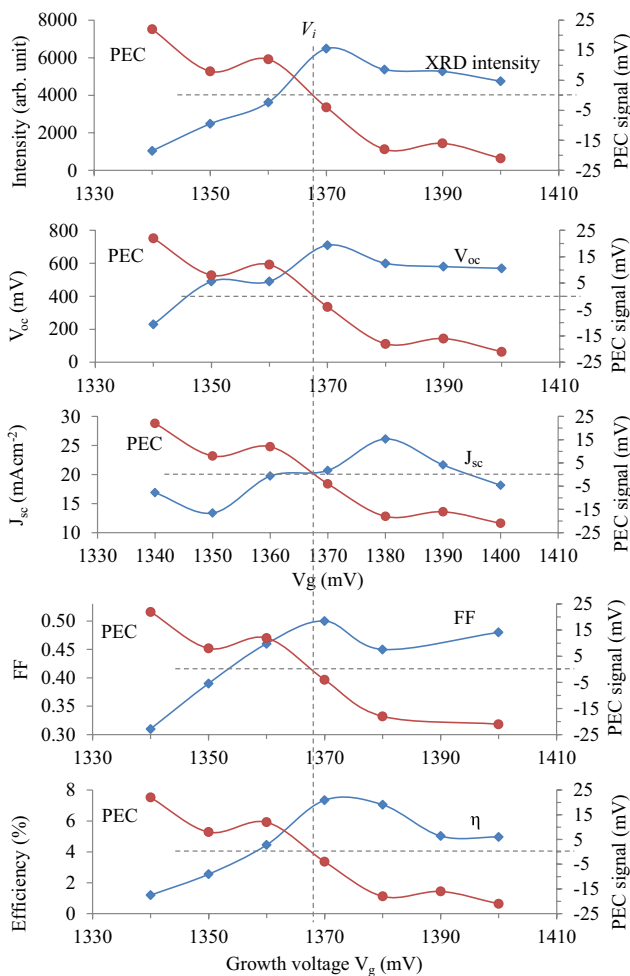
in a comprehensive research programme [3, 56, 58, 59] and a peculiar effect based on fermi level (FL) pinning at n-CdTe/metal interfaces was observed. This work confirmed Schottky barrier formation at the above interface is heavily dependent on Fermi level pinning at one of the five experimentally observed defect levels E1, E2,... E5 (see Fig. 8b). Furthermore, it was found that E1, E2 and E3 dominate when the CdTe surface is rich in Te, and E4 and E5 dominate when the CdTe surface is rich in Cd [56, 58]. Therefore, in order to form large Schottky barriers, Fermi level should be pinned at E5, closer to the valence band maximum. Combining these results and the existence of CdTe as n-type material after CdCl<sub>2</sub> treatment led to the formation of a new model for CdS/CdTe solar cell structure. This was first published in 2002, and the relevant energy band diagram is shown in Fig. 8b [7]. Clearly the two device concepts produced another controversy in the solid state physics area of this device. Many experimental results could be explained by both device structures, but the second device model satisfactorily explains almost all device characteristics [7]. This situation had created confusion in understanding and describing properties of CdS/CdTe based PV device characteristics for a long period of time over three decades.

As described in numerous publications afterwards [8, 60, 61] and summarised in this review, CdTe can be prepared to form both p-type (when Te rich) and n-type (when Cd rich) material after CdCl<sub>2</sub> treatment. Therefore, the CdS/CdTe device structures were fabricated and studied in this research programme, in the vicinity of  $V_i$  producing both p-CdTe and n-CdTe for fabrication of devices. The summary of these results are shown in Fig. 9. The vertical dashed line shows the transition growth voltage,  $V_i$  at 1368 mV for this electrolyte. Materials grown at voltages

below  $V_i$  are Te-rich and p-type in electrical conduction, while the layers grown at voltages above  $V_i$  are Cd-rich and n-type in electrical conduction. Therefore, the formation of both n-p type devices when  $V_g < V_i$  (as shown in Fig. 8a) and n-n+ SB type devices when  $V_g > V_i$  (as shown in Fig. 8b) are possible under different growth conditions of CdTe thin films.

The XRD intensity variation of (111) peak and the PEC results shown in frame 1 of Fig. 9 shows the highest crystallinity at  $\sim V_i$  and the formation of both p- and n-type CdTe layers for CdCl<sub>2</sub> treated CdTe. Rest of the frames show the variation of experimentally observed  $V_{oc}$ ,  $J_{sc}$ , FF and efficiency of solar cells as a function of growth voltage of CdTe layers. PEC results are shown in every frame to indicate both p- and n-type CdTe thin films. It is clear that high performance is achieved when CdTe is Cd-rich and n-type in electrical conduction. It should be noted that these Te and Cd richnesses take place in doping levels (ppb and ppm levels) and not possible to detect from many available analytical techniques. Since the n-n+ SB is a tandem solar cell comprising two junctions connected in parallel (see Fig. 8b), it must produce superior devices. Both rectifying junctions embedded in this structure (n-n and SB) create photo-generated currents and these currents are added in the external circuit. According to the simple definition of “addition of electric currents is provided in parallel connections”, these two junctions are naturally connected in parallel.

Furthermore, when the FL pinning takes place at E5  $\sim 1.20$  eV [7, 59], the potential barrier height created in the device is comparable with that of n-p type devices. Therefore both devices are capable of producing similar  $V_{oc}$  values, since  $V_{oc}$  is a function of potential barrier height. Since the two junctions are connected in parallel, the currents add



**Fig. 9** Typical variation of the PEC signal for CdCl<sub>2</sub> treated CdTe is shown in each frame to separate the p-type and n-type regions. The intensity of (111) XRD peak is shown in the first frame indicating best crystallinity around  $V_i$ . The device parameters for glass/FTO/CdS/CdTe/Au solar cells fabricated with CdTe layers grown in the vicinity of the transition voltage,  $V_i = 1368$  mV are shown in the other four frames. Note that all device parameters are higher when the CdTe layers are rich in Cd and n-type in electrical conduction

up producing devices with very high currents when conditions are optimum. In a situation without full understanding of the device physics, and during an experimentally optimising the device efficiency in a trial and error method, it is possible to form n–n+ SB configuration. But explaining the device characteristics using the simple n–p junction created a serious confusion over the past few decades hindering the continuous progress of this solar cell.

## 6 Grain boundary enhanced PV effect

The first semiconducting layer of CdS is essential to provide the n-type window material in this device structure.

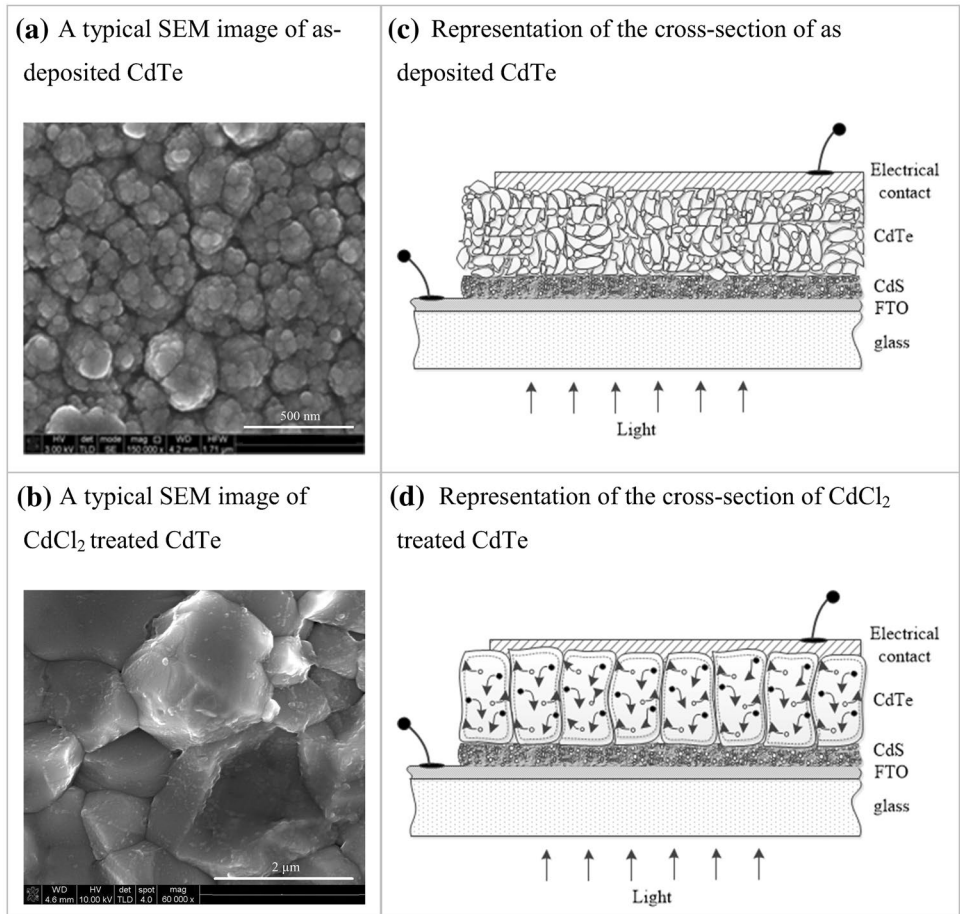
Most researchers use CBD–CdS, and the grain size varies in the range ~5.0–35 nm. This material smoothens out the spiky FTO surface to a certain extent and provides a suitable substrate for growth of high quality CdTe. Although CBD growth method seems to be a low-cost technique, this batch process produces large volumes of Cd-containing toxic waste solutions each time, adding high cost of manufacturing in a production line. Because of this reason, this research programme is focussing on electroplated CdS layers [23, 25–27]. All electro-deposited layers from a continuous process is more attractive in commercial production lines. ED also provides an excellent technique for fine controlling of the CdS layer thickness. High efficiency solar cells are produced with ~50–100 nm thick CdS layers [65]. This layer undergoes a heat treatment in air at ~400 °C for 20 min before depositing CdTe layers.

CdTe absorber layer is next deposited on clean CdS surface. ED–CdTe layer thickness is ~1.50–2.00  $\mu\text{m}$ , but different growth techniques deposit varying thicknesses of up to ~4.00–6.00  $\mu\text{m}$ . These layers consist of small “crystallites” or nano-particles of ~20–65 nm, as estimated by Scherrer equation using XRD patterns. SEM and AFM show that large “clusters” or “grains” formed by agglomerations of these crystallites. This is clearly shown by the SEM picture given in Fig. 10a. Most of these agglomerations show columnar growth due to low growth temperature and the influence of electric field present during the growth of material using electroplating. XRD measurements show that (111) preferred orientation for CdTe grown by low temperature techniques like ED and sputtering. Literature also reports columnar growth of CdTe when other growth techniques are used [49, 66]. This must be due to the natural preference of the FTO/CdTe or FTO/CdS/CdTe interfaces, or the preferred CdTe growth direction.

As described in Sect. 3.4, heat treatment in air with CdCl<sub>2</sub> on the surface makes CdTe undergo some amazing changes. When the heat treatment temperature gradually increases, the (111) peak intensity increases gradually until  $385 \pm 5$  °C (ST1) due to coalescence of nano-materials due to their large surface to volume ratio. At ~385 °C, there is a sudden collapse of the (111) peak and other CdTe related XRD peaks; (220) and (311) increase. This shows the loss of preferred orientation along (111) and randomisation of the crystallites. This can be explained as the melting of material boundaries due to presence of impurities (Cl, O and excess Cd and Te) and free movement of crystallites showing random orientations. When the material is kept at a temperature greater than ST1 (~385 °C), coalescence of crystalline grains takes place to form grains.

The nature of CdTe is to form columnar type large grains and at ~450 °C, these grains can take the size of several  $\mu\text{m}$  (see Fig. 10b). At these higher temperatures, CdTe crystals gradually returns back to its naturally preferred

**Fig. 10** SEM top views of as-deposited CdTe (a), and CdCl<sub>2</sub> treated CdTe layers (b). Note the presence of small crystallites ~20–65 nm in large clusters or agglomerations. c and d illustrate the visualisation of cross-sections based on SEM and TEM observations [35]



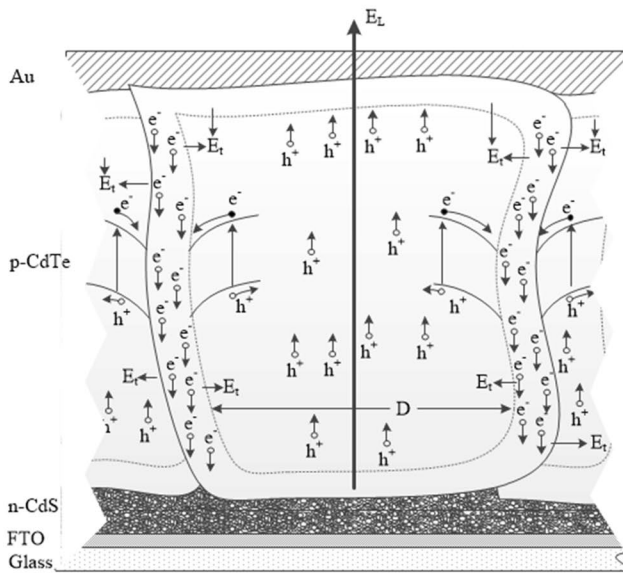
(111) orientation due to increased mobility of atoms/ions. Therefore depending on the heat treatment temperature and duration, XRD peaks can show varying intensities as shown in Fig. 7 [35]. Heating at temperatures ~450 °C and beyond leads to evaporation of excess elements present (elemental Cd or Te) and sublimation of CdTe. This also leads to increase the size of columnar type grains, and produce pinholes between grains due to upward growth rather than sideways growth. These films are not suitable for fabrication of devices due to short circuiting through these pinholes.

During heat treatment, grain boundary areas are liquids and CdTe grains are solids. All impurities like Cl and O could freely move through convection currents around and flow down to the CdS layer. At these high temperatures, impurities like Cl will diffuse into solid CdTe grains forming a thin skin, changing the doping concentration of that skin. When heating is terminated, grain boundaries freeze and form a solid with different electronic property to the CdTe in the large crystalline grains. This situation is shown in Fig. 10d and the enlarged version in Fig. 11. These different electronic properties between the two materials lead to show grain boundary enhanced PV effect.

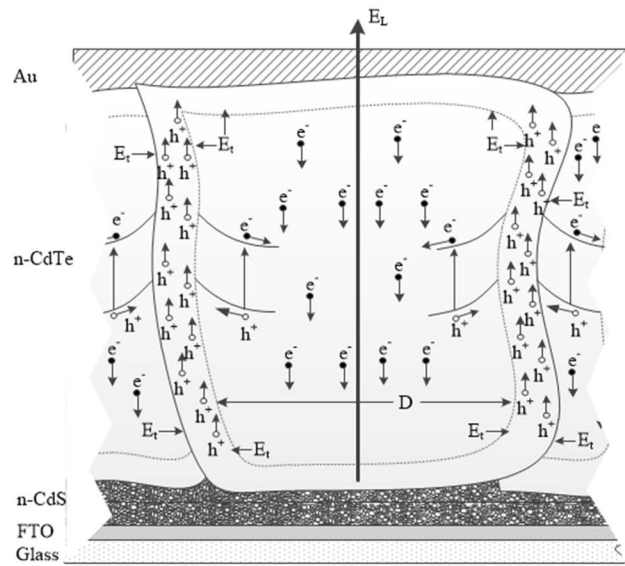
Figure 11 shows the band bending at grain boundaries for two possible cases. Therefore, the photo-generated electrons flow towards grain boundaries in the case of p–n junction solar cell. In the case of n–n + SB solar cells, photo-generated electrons flow towards the middle of CdTe grains. In both cases, the main electric field ( $E_T$ ) is towards the back electrical contact (Au). The transverse electric field ( $E_T$ ) created at grain boundaries separate photo-generated e–h pairs to move in separate paths, minimising recombination process.

The number of photo-generated electrons and holes are equal but the cross-sectional areas for flow of two types of charge carriers are very different. Therefore, this minimise the recombination mechanism in these devices and the density of photo-generated currents are high in grain boundaries. This has been clearly demonstrated by recent EBIC results of the cross-sections of CdS/CdTe solar cells [67, 68]. In this type of grain boundary enhanced PV actions, only one type of charge carriers flow along the grain boundaries and any defects present will be saturated instantaneously upon illumination and then show high quality electrical conduction. This is also true for charge carriers flowing through crystalline CdTe grains.

(a) n-CdS/p-CdTe solar cells



(b) n-CdS/n-CdTe/Schottky barrier solar cells



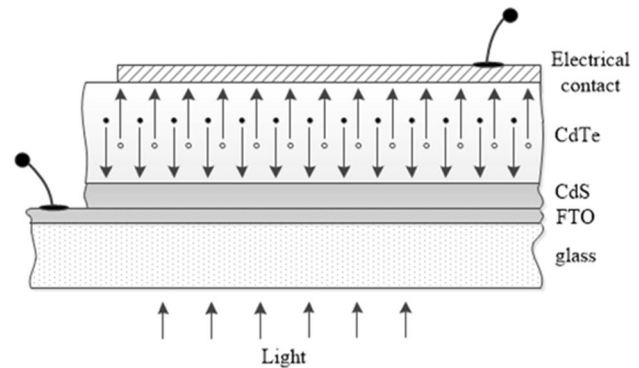
**Fig. 11** Expanded schematic diagrams to show grains and grain boundaries of two possible CdS/CdTe solar cells; **a** for n-CdS/p-CdTe devices and **b** for n-CdS/n-CdTe devices. Note the directions of main

internal electric field (EL), transverse electric fields (Et) and directions of motion of photo-generated charge carriers

In this type of charge carrier motions normal to the FTO substrate, mobility of charge carriers ( $\mu_{\perp}$ ) can be extremely high. For example, electrons or holes flowing along the crystalline grain, has minimum scattering from grain boundaries. In the conventional Hall Effect measurements, the electric current flow is parallel to the FTO surface and undergoes millions of scattering at grain boundaries. These measurements estimate the mobility parallel to the FTO surface ( $\mu_{\parallel}$ ) and can be several orders of magnitude low. Therefore, the theoretical modelling carried out in the past with mobility values obtained from Hall Effect measurements need re-visiting those calculations. In the CdS/CdTe solar cell, the actual charge carrier mobilities ( $\mu_{\perp}$ ) can take extremely high values. With grain boundary enhanced PV effect present, the recombination of photo-generated charge carriers will also be at minimum level.

There are also other implications on the analysis of depth profiling results of CdCl<sub>2</sub> treated poly-crystalline CdTe layers [69]. As described above, the impurities like Cl and O can freely flow along the melted grain boundaries down to the CdS layer. Also, Cl could diffuse into a thin skin around large CdTe grains. In this situation, depth profiling experiments could produce Cl and O signals from grain boundaries, but the information may lead to draw incorrect conclusions about the impurity distribution in poly-crystalline CdTe layers.

For comparison, a CdS/CdTe solar cell made out of epitaxial materials is shown in Fig. 12. Epitaxial materials



**Fig. 12** Schematic diagram showing the motion of photo-generated charge carriers in a device fabricated with epitaxial layers. The e-h recombination is high in these devices due to lack of separate paths for two different charge carriers

are layer-by-layer grown fully crystalline materials. In this case, only the main electric field is present normal to the FTO surface and the transverse electric fields are not present to provide different paths for photo-generated charge carriers. Therefore, e-h recombination can take place and the resultant current will be comparatively low. Due to these reasons, the poly-crystalline layers when produced with optimum conditions could show superior PV properties than those fabricated using epitaxial materials. These effects can be equally applicable to CIGS, Kesterite and Perovskite based thin film poly-crystalline solar cells also,

since the literature shows their columnar growth patterns [70–72]. This effect could also take place in poly-crystalline silicon solar cells when rod-type crystals are formed normal to the wafer surface.

Following above discussions, poly-crystalline materials with grain boundary enhanced PV effect could perform with higher efficiencies than amorphous and epitaxial layers. Hence an optimum grain size exists for superior performance. This depends on the charge carrier separation capabilities within a grain and therefore the optimum diameter of a cylindrical grain should be  $\sim 2L$ , where  $L$  represents the electron diffusion length in that particular material. Therefore, the optimum value of the grain size depends on the electronic material quality. For example, if the electron diffusion length in a particular semiconductor is  $1\ \mu\text{m}$ , then the optimum diameter of the grain should be  $\sim 2\ \mu\text{m}$ .

This understanding also enables us to describe the difference between the addition of Cl during growth of the material and the post-growth  $\text{CdCl}_2$  treatment. The addition of Cl during growth changes the electrical conductivity of large grains, while  $\text{CdCl}_2$  treatment changes the doping concentration of the skin around the large grain and the properties of the materials in the grain boundary. Therefore,  $\text{CdCl}_2$  treatment is essential to create the most necessary transverse electric field  $E_t$  at grain boundaries. This has been clearly shown by growing CdTe using  $\text{CdCl}_2$  precursor [32] in which  $\text{CdCl}_2$  post-deposition treatment was still necessary to increase the efficiency of the devices fabricated.

## 7 Progress to date on graded bandgap devices

As the new direction of this research programme, it is appropriate to discuss the progress of next generation solar cells based on graded bandgap devices. The main author of this article designed and published a paper on fully graded bandgap solar cell device in 2005 [6] in order to harvest all photons from UV, Visible and Infra-Red (IR) regions. This device structure also included the impurity PV effect and impact ionisation in order to create and enhance the number of charge carriers within the same device. This idea was experimentally tested during the same year [73] using well-established metal organic vapour phase epitaxy (MOVPE) grown semiconductor system, GaAs/AlGaAs. Using only two growth runs, the experimental results demonstrated high device parameters such as  $V_{oc} = 1175\ \text{mV}$ ,  $\text{FF} = 0.85$  [73] and experimental evidence for impurity PV effect [74] and impact ionisation [75]. These devices were capable of producing  $V_{oc}$  values in excess of  $750\ \text{mV}$  in complete darkness [74], demonstrating the harvesting of IR radiation from the surroundings. Since the design idea was experimentally proven, the authors' present focus is to fabricate these types of novel devices using low-cost, scalable and manufacturable electroplated semiconducting materials.

Solar energy group at Sheffield Hallam University (SHU) has been exploring electroplating of semiconductors over the past two decades, and examined a large number of semiconductors as summarised in Table 1. It is becoming clear that the electroplating is a low-cost but very powerful

**Table 1** Summary of explored electronic materials to date at author's research group using electroplating from aqueous solutions

Material electroplated	$E_g$ (eV)	Precursors used for electroplating	Comments	References
CuInSe <sub>2</sub>	$\sim 1.00$	CuSO <sub>4</sub> for Cu ions, In <sub>2</sub> (SO <sub>4</sub> ) <sub>3</sub> for In ions and H <sub>2</sub> SeO <sub>3</sub> for Se ions	Ability to grow both p- and n-type material	[76]
CdTe	1.45	CdSO <sub>4</sub> or Cd(NO <sub>3</sub> ) <sub>2</sub> or CdCl <sub>2</sub> for Cd ions and TeO <sub>2</sub> for Te ions	Ability to grow both p- and n-type CdTe using Cd-Sulphate, Nitrate and Chloride precursors	[31, 32]
CuInGaSe <sub>2</sub>	1.00–1.70	CuSO <sub>4</sub> for Cu ions, In <sub>2</sub> (SO <sub>4</sub> ) <sub>3</sub> for In ions, Ga <sub>2</sub> (SO <sub>4</sub> ) <sub>3</sub> for Ga ions and H <sub>2</sub> SeO <sub>3</sub> for Se ions	Ability to grow both p- and n-type material	[77]
CdSe	1.90	CdCl <sub>2</sub> for Cd ions and SeO <sub>2</sub> for Se ions	Work is in progress	[78]
InSe	1.90	InCl <sub>3</sub> for In ions and SeO <sub>2</sub> for Se ions	Work is in progress	[79]
GaSe	2.00	Ga <sub>2</sub> (SO <sub>4</sub> ) <sub>2</sub> for Ga ions and SeO <sub>2</sub> for Se ions	Work is in progress	
ZnTe	1.90–2.60	ZnSO <sub>4</sub> for Zn ions and TeO <sub>2</sub> for Te ions	Ability to grow both p- and n-type material	[80]
CdS	2.42	CdCl <sub>2</sub> for Cd ions and Na <sub>2</sub> S <sub>2</sub> O <sub>3</sub> , NH <sub>4</sub> S <sub>2</sub> O <sub>3</sub> or NH <sub>2</sub> C <sub>2</sub> SNH <sub>2</sub>	Conductivity type is always n-type	[23, 25, 27]
CdMnTe	1.57–2.50	CdSO <sub>4</sub> for Cd ions, MnSO <sub>4</sub> for Mn ions and TeO <sub>2</sub> for Te ions	Work is in progress	
ZnSe	2.70	ZnSO <sub>4</sub> for Zn ions and SeO <sub>2</sub> for Se ions	Ability to grow both p- and n-type material	[81]
ZnO	3.30	Zn(NO <sub>3</sub> ) <sub>2</sub> for Zn ions		[82]
ZnS	3.75	ZnSO <sub>4</sub> for Zn and (NH <sub>4</sub> ) <sub>2</sub> S <sub>2</sub> O <sub>3</sub> for S ions	Ability to grow both p- and n-type material	[83]
Poly aniline (PAni)	–	C <sub>6</sub> H <sub>5</sub> NH <sub>2</sub> and H <sub>2</sub> SO <sub>4</sub>	To use as a pinhole plugging layer	[84]



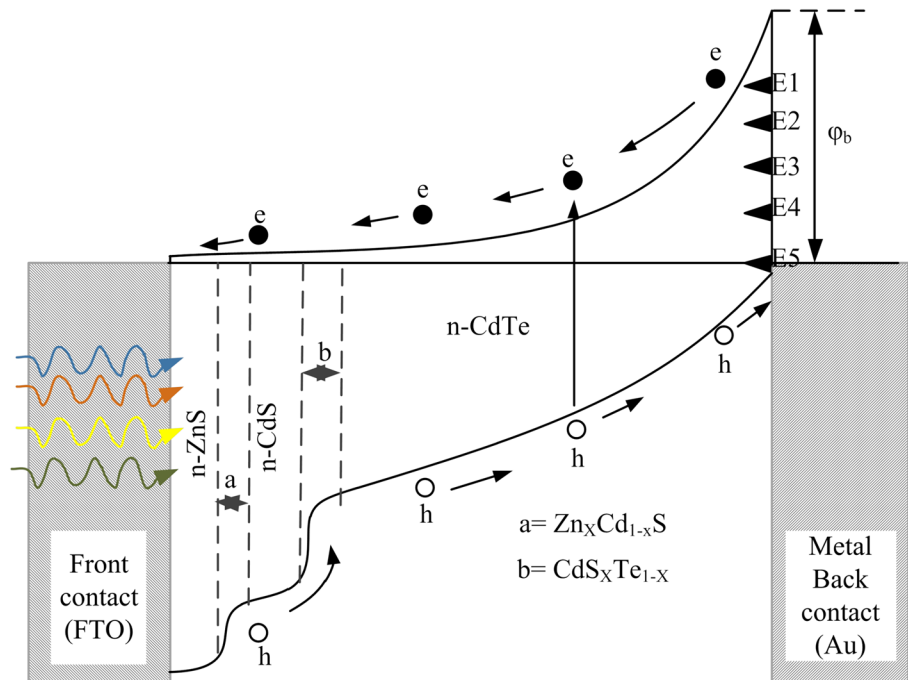
technique for growing semiconductors and nano-materials suitable for both micro- and macro-scale electronic devices. This method is particularly suitable for manufacturing large area electronic devices such as PV solar panels and display devices. The CdS/CdTe project completed by BP Solar successfully proved the manufacturability of large solar panels in the 1980s and 1990s by producing ~1.0 m<sup>2</sup> solar panels with efficiencies over 10% using electroplated CdTe [21]. The current aim of the research at SHU solar energy group is to develop next generation solar cells based on graded bandgap device structures utilising electroplated materials. The efforts are also directed to gain optimum benefits from grain boundary enhanced PV effects, as described above.

One device structure tested using already established materials, glass/FTO/n-ZnS/n-CdS/n-CdTe/Au has shown 10.4% efficiency [60], exhibiting extremely high J<sub>sc</sub> values as expected. Its energy band diagram is shown in Fig. 13 and consists of three rectifying junctions

connected in parallel. Therefore, the electric currents produced in all three junctions add up to yield large short circuit current density. These devices are capable of harvesting IR radiation from the solar spectrum and from the surroundings, and enhances the number of charge carriers using impurity PV effect and impact ionisation [59, 75].

This initial work shows the high potential of developing graded bandgap devices using electroplated materials. In order to produce high efficiency devices, the Fermi level should be pinned at E5 defect level. However, the presence of other pinning positions (E4, ..., E1) could create a serious reproducibility issues [7]. The subsequent work and the best devices produced to date are summarised in Table 2. The most noteworthy is the 15.3% graded bandgap device produced by glass/FTO/n-CdS/n-CdTe/p-CdTe/Au structures. Graded bandgap device nature of this structure is shown in Fig. 14 [8] and there is a huge potential to develop this device to achieve

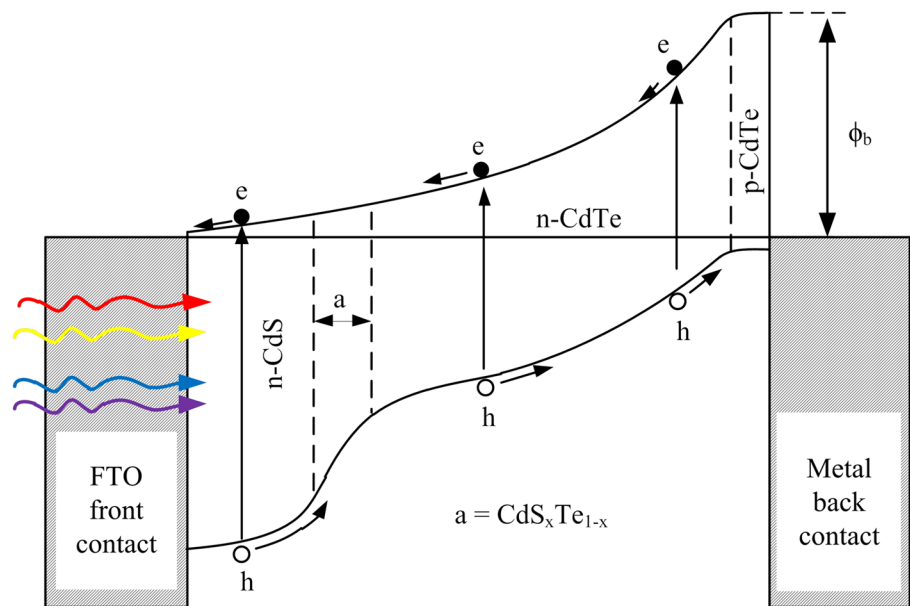
**Fig. 13** Energy band diagram of a 3-layer graded bandgap device containing n-ZnS, n-CdS and n-CdTe showing 10.4% efficient solar cells [59, 61]. Note the Fermi level pinning requirement at E5 defect level for achieving high efficiency devices



**Table 2** Graded bandgap device parameters reported under both AM1.5 illuminated condition and dark condition for lab-scale 2 mm diameter devices

Device Configuration	Parameters under AM1.5 illuminated condition				Parameters under dark condition			Ref.
	$\eta$ (%)	$J_{sc}$ (mA cm <sup>-2</sup> )	$V_{oc}$ (mV)	FF	$R_s$ ( $\Omega$ )	$R_{sh}$ ( $\Omega$ )	$N_D$ (cm <sup>-3</sup> )	
Glass/FTO/n-ZnS/n-CdS/n-CdTe/Au	10.4	40.8	640	0.40	175	$4.6 \times 10^3$	$8.1 \times 10^{14}$	[85]
Glass/FTO/n-ZnS/ZnCdS <sub>x</sub> Te <sub>1-x</sub> /n-CdTe/Au	12.0	47.8	646	0.39	–	–	–	[60]
Glass/FTO/n-ZnS/n-CdS/n-CdTe/Au	12.8	41.5	670	0.46	1351	$8.1 \times 10^6$	$5.2 \times 10^{15}$	[86]
Glass/FTO/n-In <sub>x</sub> Se <sub>y</sub> /n-CdS/n-CdTe/Au	10.0	38.1	640	0.41	309	$4.5 \times 10^3$	$2.0 \times 10^{14}$	[87]
n-CdS/n-CdTe/p-CdTe/Au	15.3	33.8	730	0.62	500	$7.2 \times 10^6$	$6.6 \times 10^{14}$	[8]

**Fig. 14** Energy band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au structure showing its graded bandgap nature, enhancing charge carrier creation, separation and collection. Measured conversion efficiency is 15.3% [8]



highest possible efficiencies. Work is continuing in this direction.

## 8 Conclusions

To understand and unravel many issues on CdS/CdTe solar cell, electrodeposition has been used as the growth technique for both materials.

About 50–100 nm thick CdS layer consists of nano-materials, cover FTO layer providing a better substrate for CdTe growth and always show n-type electrical conduction. Its bandgap after heat treatment at  $\sim 400$  °C for 20 min in air is 2.42 eV, and close to that of bulk CdS material. Electroplating of CdTe layer at  $\sim 85$  °C forms a nano-material layer consisting of  $\sim 20$ –65 nm crystallites grouped together to form large grains. Material can be easily grown as p-type when Te-rich, and n-type when Cd-rich, by varying its composition. Growth is highly preferential along (111) and the usual layer thickness is  $\sim 1.50$ – $2.00$   $\mu\text{m}$ .

Post growth heat treatment at  $\sim 430$  °C for  $\sim 10$  min in the presence of  $\text{CdCl}_2$  is essential for improving the structural, morphological, electrical and optical properties of CdTe layer. As temperature increases small crystallites (nano-materials) first coalesce into large crystals showing a sharp structural change at  $385 \pm 5$  °C, due to their large surface to volume ratio. At 385 °C, the grain boundaries melt due to the lowering of melting point due to impurities and CdTe crystals remain as solids. At this temperature, (111) preferred orientation change into random nature, but further heat treatment slowly brings back the naturally preferred (111) orientation. In this process, few microns diameter columnar type grains are formed with materials

frozen in grain boundaries having different electronic properties. This provides band bending at grain boundaries and the transverse internal electric fields in addition to the main electric field normal to FTO surface. This is the key activation process providing grain boundary enhanced PV effect, and the optimum diameter of crystalline grains is  $\sim 2L$ , where  $L$  is the diffusion length of electrons in CdTe material. This effect seems to be valid for thin film solar cells fabricated with columnar grown materials of CdTe, CIGS, poly-Si and Perovskites.

Experimental results show that the best performing devices arise when the material is Cd-rich and n-type in electrical conduction. The same is true when the CdTe surface is chemically etched to produce Cd-richness prior to metallisation. Acidic etchants produce Te-rich surfaces and alkaline etchants produce Cd-rich surfaces. The trend observed is that the Cd-rich surfaces produce high performing devices.

The CdTe exists as both p-type and n-type materials and the conductivity change could happen easily depending on its composition. Therefore, two types of electronic devices are possible from CdS/CdTe structure. One is the simple n–p junction when CdTe is p-type and the back electrical contact should form a low-resistance ohmic contact. The second is more complex to identify and involve an n–n junction combined with a large SB at the back metal contact, when the  $\text{CdCl}_2$  treated CdTe remains n-type. The SB formation is also has a complex situation, depending on five possible pinning positions identified. This causes the reproducibility problems, and for best devices the Fermi level should be pinned close to the VB edge. In this case the device is a tandem cell comprising n–n junction and n-CdTe/metal SB at the back contact, connected in parallel.

Since the largest SB achievable is  $\sim 1.20$  eV (when the Fermi level is pinned at E5), and comparable to the potential barrier of the p–n junction, this device perform better than the simple n–p device. Because of this complexity, the solar cell development based on CdS/CdTe should take extreme care knowing the electrical conductivity type of CdTe used in the device, especially before interpreting device characteristics.

Next generation solar cells based on graded bandgap structures have very high potential in achieving better conversion efficiencies. This work demonstrated the achievement of 15.3% for initial three-layer graded bandgap solar cells based on electroplated materials, and the research along this line has a great future.

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