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**EFFECT OF THICKNESS: A CASE STUDY OF ELECTRODEPOSITED CdS IN CdS/CdTe BASED
PHOTOVOLTAIC DEVICES**

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ABSTRACT

The effect of electrodeposition technique on CdS thickness incorporated in CdS/CdTe-based solar cell has been investigated using all-electrodeposited g/FTO/n-CdS/n-CdTe/p-CdTe multilayer device configuration. The optical, morphological and structural properties of the electroplated CdS were investigated for CdS thicknesses between 50nm and 200 nm. The observed CdS bandgap ranges between 2.42 and 2.46 eV. The morphological analysis shows full coverage of underlying g/FTO substrate for all CdS thicknesses except for the 50 nm which shows the presence of gap in-between grains. The structural analysis shows a preferred orientation of H(101) for all the CdS thicknesses except the 50 nm thick CdS which shows either a weak crystallinity or an amorphous nature. The fabricated solar cell shows a maximum conversion efficiency of ~11% using CdS thickness ranging between 100 and 150 nm. These results show that although low CdS thickness is desirable for photovoltaic application, the effect of nucleation mechanism of deposition technique should be taken into consideration.

KEYWORD: Electrodeposition, Window layer, Cadmium Sulphide, Cadmium telluride, Multilayer graded bandgap.

1 INTRODUCTION

Electrochemical deposition emerges as one of the most advantageous semiconductor growth techniques for binary, ternary and quaternary compounds due to its cost effectiveness, scalability, self-purification ability, simplicity in layer and device fabrication, columnar growth pattern amongst other advantages [1].

Electrodeposition of semiconductors on conducting substrates commence by the nucleation of the most electropositive element on the points on the conducting substrates with the highest electric field. Due to the unevenness of the underlying conducting substrate such as glass/fluorine doped tin oxide (g/FTO), the highest electric field is experienced at the peaks of the rough conducting substrate surfaces. Nucleation starts at the peaks and spreads out through to the lowest valley resulting into layers with columnar nature [2]. This phenomenon results in an uneven thickness of the electrodeposited semiconducting layers at the early stages of nucleation. It should be noted that columnar growth can also be achieved through low growth temperature and layer-by-layer growth on preferred self-substrates. The effect of substrate roughness is much more observable on the first semiconductor layer deposited on the conducting substrate. With respect to cadmium sulphide window layer in the cadmium sulphide/cadmium telluride (CdS/CdTe) based solar cell, it is well known that the reduction of CdS layer thickness is required for increased photocurrent. Researchers such as Granata et al, 2000 [3] and Lee et al, 1987 [4] amongst other authors have emphasised the effect of CdS thickness without taking into consideration the deposition technique, deposition mechanism and the effect of the roughness of the underlying substrate as iterated by Dedova, 2013 [5] on g/FTO/ZnO layer. Based on mechanism of deposition in electroplating, this work focuses on the effect of deposition mechanism and underlying substrate roughness on electrodeposited CdS thickness optimisation in its integration into CdS/CdTe solar cell.

2 EXPERIMENTAL PROCEDURE

2.1 SUBSTRATE PREPARATION

For this work, all the chemicals and conducting substrates were procured from Sigma Aldrich, UK. Computerised GillAC potentiostat was utilised as the power source, while, TEC-7 g/FTO substrate with a sheet resistance of $\sim 7 \Omega/\text{sq}$ were utilised as the cathodes in the electrolytic bath. The g/FTO substrates were attached to the cathodes' pure graphite rod using polytetrafluoroethylene (PTFE) tapes while a high purity graphite rod was utilised as the anode. The g/FTO substrates were cut into $2 \times 4 \text{ cm}^2$ area samples. Prior to deposition, the g/FTO substrates were washed in an ultrasonic tank containing soap solution for 15 minutes and rinsed in deionised (DI) water. Afterwards, the substrates were degreased using organic solvents such as methanol and

acetone respectively, rinsed in DI water, dried in a stream of nitrogen gas and immediately transferred into the electrolytic bath.

2.1.1 CdS LAYER GROWTH

Cadmium sulphide was electrodeposited from a 400 ml aqueous electrolytic bath containing 0.03 M of ammonium thiosulphate ($(\text{NH}_4)_2\text{S}_2\text{O}_3$) with 99% purity and 0.3 M cadmium chloride hydrate ($\text{CdCl}_2 \cdot x\text{H}_2\text{O}$) with purity of 98% as the precursors of sulphur (S) and cadmium (Cd) respectively. Prior to deposition, the electrolytic bath pH was set to 2.50 ± 0.02 , stirring rate to ~ 300 rpm and temperature to 85°C . The 400 ml aqueous electrolytic solution was contained in a 500 ml polypropylene beaker. The polypropylene beaker was placed inside an 800 ml glass beaker containing DI water. The external water jacket (water/glass beaker) helps in the homogenous heating of the electrolyte contained within the polypropylene beaker. The optimisation of electrodeposited CdS based on structural, morphological, compositional optical and electrical properties has been documented in the literature [6]. CdS was electrodeposited at 1200 mV in a two-electrode configuration with respect to a graphite anode. The thickness of the CdS layer utilised in this set of experiments is varied between 50 nm and 200 nm at a step of 50 nm. After growth, the g/FTO/CdS layers were rinsed in DI so as to washoff any loose particles. The g/FTO/CdS layer was dried in a stream nitrogen gas. Afterwards, post growth treatment of the CdS layer was performed by adding droplets of solution containing 0.1M CdCl_2 in 20 ml of DI water at room temperature to the g/FTO/CdS layers. Full coverage of the layer was achieved by the use of solution damped cotton bud. The layer was allowed to air dry prior to heat treatment at 400°C for 20 minutes in air to enhance both the material and electronic properties of CdS [7]. Subsequently, the treated g/FTO/CdS was washed in DI water and transferred directly into the cadmium telluride (CdTe) bath. It should be noted, that intrinsically CdS is always n- conduction due to the presence of Cd interstitials and S vacancies in the crystal lattice [8]–[10].

2.1.2 CdTe LAYER GROWTH

Cadmium telluride layers were electrodeposited from an 800 ml aqueous solution containing 1.5 M cadmium nitrate tetrahydrate ($\text{Cd}(\text{NO}_3)_2 \cdot 4\text{H}_2\text{O}$) with purity of 99.98% and 5ml of dilute tellurium dioxide (TeO_2) solution with purity of 99.999%. Prior to the introduction of TeO_2 into the electrolytic bath, 0.03M of TeO_2 solution was prepared by dissolving $\sim 2\text{g}$ of TeO_2 in 30 ml of concentrated nitric acid. The solution was stirred for 60 minutes to achieve homogeneity and gently diluted with 400 ml of DI water in a polypropylene conical flask. It should be noted that the concentration of tellurium is kept low due to the high positive reduction potential of Te (+593

mV) as compared to Cd (-403 mV) with reference to standard H₂ electrode [11]. As documented in the literature, the conductivity type of as-deposited CdTe is dependent on the atomic compositional ratio of cadmium to tellurium provided there is no introduction of external dopant [12]. It is well known that higher atomic concentration of Te as compared to Cd in CdTe give p-CdTe while higher atomic ratio of Cd to Te gives n-CdTe [13].

Before the inclusion of TeO₂ solution, the 800 ml containing the 1.5M of Cd(NO₃)₂·4H₂O was electropurified at a cathodic voltage below the cathodic voltage in which Cd is reduced for ~50 hours to reduce the impurity level. After the inclusion of 5 ml of pre-prepared TeO₂, the solution was stirred continuously for 2 hours before the deposition of CdTe. The pH, stirring rate and bath temperature were adjusted to 2.00±0.02, ~300 rpm and ~85°C respectively. With g/FTO/CdS as the cathode and pure graphite rod as the anode, 1200 nm thick n-CdTe layers were electrodeposited at 1380 mV, followed by the deposition of ~30 nm p-CdTe at 1360 mV in a continuous deposition process to achieve g/FTO/n-CdS/n-CdTe/p-CdTe configuration. The CdTe thicknesses were kept constant for all the CdS thickness explored. It should be noted that all the structural, compositional, morphological optical and electrical property analyses of electrodeposited CdTe layers from cadmium nitrate bath has been well documented by Salim et al, 2015 [14]. The incorporation of the thin p-CdTe layer is to minimise the electrical resistance between the metal-semiconductor interface [15] and also pin the Fermi level close to the conduction band.

2.1.3 DEVICE FABRICATION

After the growth of both the 1200 nm n-CdTe and 30 nm p-CdTe layers on the g/FTO/n-CdS to give g/FTO/n-CdS/n-CdTe/p-CdTe configuration as described in Section 2.1.2, all the layers were heat treated at 420°C for 20 minutes in air in the presence of CdCl₂. After the CdCl₂ treatment, the layers were washed and etched using solutions containing concentrated H₂SO₄ and K₂Cr₂O₇ for acid etching and solution containing NaOH and Na₂S₂O₃ for alkaline etching for 5 seconds and 2 minutes respectively to improve the metal/semiconductor contact [23], [24]. Using 2 mm diameter mask, 100 nm thick Au contacts were evaporated on the g/FTO/n-CdS/n-CdTe/p-CdTe layer at a pressure of 10⁻⁵ Nm⁻² prior to current-voltage (I-V) measurements.

2.2 EXPERIMENTAL TECHNIQUES USED

With major emphasis on the characteristic properties of CdS as it is affected by its thickness, the experimental techniques are focussed on both the as-deposited and CdCl₂ treated g/FTO/CdS layers. The optical properties such as the absorbance and transmittance were measured using Cary 50Scan UV-Visible spectrophotometer at

room temperature. Prior to optical measurements, the system was calibrated using a thoroughly cleaned blank g/FTO as a baseline to eliminate the effect of the underlying substrate from the obtained results. The morphological properties were obtained using FEI Nova 200 NanoSEM equipment at a magnification of $\times 60,000$. The structural properties such as crystallite size and phase were obtained using Philips PW 3710 X'pert diffractometer with both the X-ray generator tension and current set to 40 kV and 40 mA respectively. The XRD system was incorporated with Cu-K α monochromator of wavelength $\lambda=1.54 \text{ \AA}$. The CdS layers thicknesses were measured using UBM Microfocus optical depth profilometer (UBM, Messetechnik GmbH, Ettlingen, Germany) while the electrical properties such as the current-voltage properties of the fabricated solar cell were obtained using RR267MON calibrated Rera Solution I-V measurement system.

3 RESULTS AND DISCUSSIONS

3.1 OPTICAL PROPERTY

Figure 1 (a) and (b) shows the Tauc's plot of $ah\nu$ versus $h\nu$ [16] and percentage transmittance versus wavelength for CdCl₂ treated g/FTO/CdS layers, where α is absorption coefficient and $h\nu$ is the energy of the incident light. From Figure 1 (a), it was observed that the bandgap lies within $2.44\pm 0.02 \text{ eV}$ with the highest bandgap was observed at 50 nm. This observation might be due to either the early nucleation stage in which the underlying g/FTO substrate is not fully covered due to the columnar growth in electroplating as discussed in Section 1 and/or the comparatively low crystallite size and crystallinity [17] as shown in Table 1 for 50 nm thick CdS layer. Significantly, an increase in the steepness of the absorption edge and a shift of the absorption edge towards shorter wavelength were observed with increase in CdS thickness. This observation is documented in the literature [18], [19] with researchers such as Bosio et al, 2006 [7], Han et al, 2011 [20] suggesting superior semiconductor material quality with steeper absorption edge.

The transmission of all photon through gaps is equivalent to a wider bandgap. The reduction in bandgap observed with increase in thickness to 100 nm might be due to the full coverage of the underlying substrate. Consequently, reduction in transmittance from $\sim 90\%$ to $\sim 75\%$ was observed with increasing thickness from 50 nm to 200 nm as shown in Figure 1 (b). It is important to note that although thinner CdS layers give higher transmittance, hence higher photocurrent can be generated, although it can suffer from discontinuities and defects such as pinholes [10], [21]. Therefore it is pertinent that the optical property of the semiconductor layer must be considered to achieve optimum photocurrent.

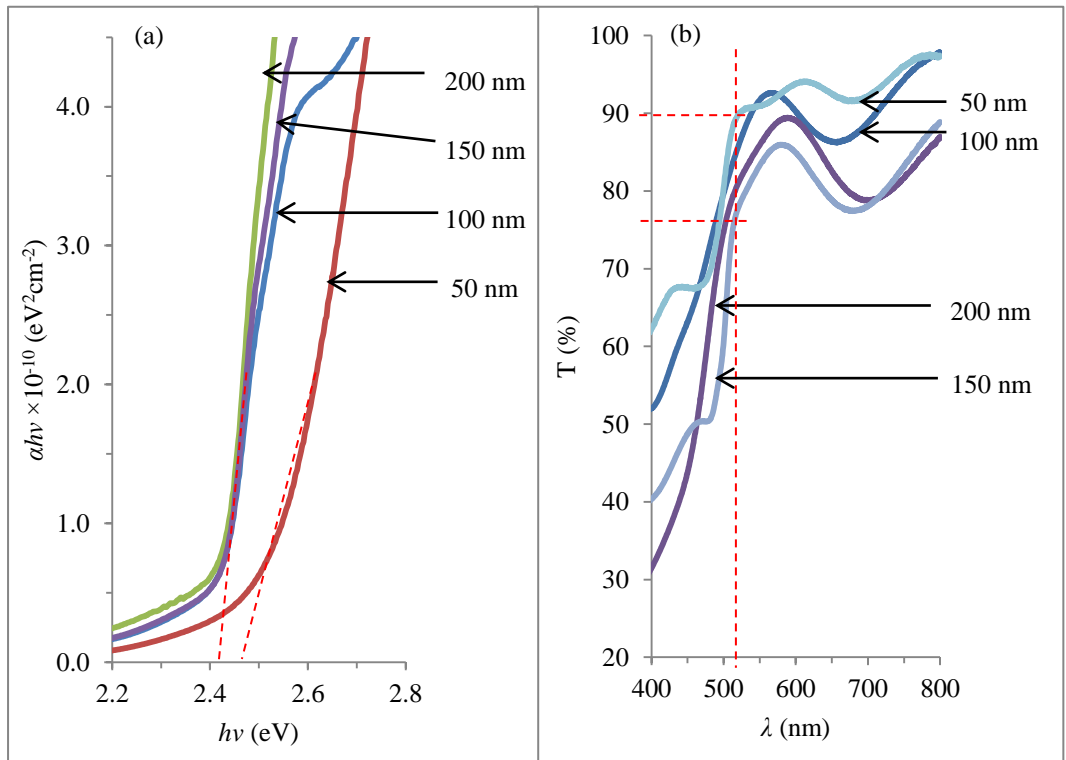


Figure 1: (a) Tauc's plot of $\alpha h\nu$ versus $h\nu$ and (b) transmission versus wavelengths for CdS layers with varying thickness.

3.2 MORPHOLOGICAL PROPERTY

The SEM micrographs of 50, 100, 150 and 200 nm thicknesses of CdCl₂ treated CdS layers grown on g/FTO are shown in *Figure 2* (a-d) respectively. Although the as-deposited layer, g/FTO/CdS is not presented in this paper due to its triviality, grain growth and the coalescence of grains were observed after CdCl₂ treatment. As observed in *Figure 2* (a), full coverage of the underlying g/FTO substrate has not been attained with the g/FTO grains still visible beneath the CdS layer due to significant gaps between grains. This observation might be as a result of the early stage of nucleation of CdS to the underlying conducting substrate and also the columnar growth mechanism in electroplated semiconductors. With an increase in thickness to 100 nm and above as shown in *Figure 2* (b-d), grains tend to be more closely packed with full coverage of the g/FTO underlying substrate. It should be noted that the fabrication of a solar cell using the 50 nm pinhole infected CdS layer will lower the performance of the solar cell due to low open-circuit voltage, fill factor and short-circuit current density as a result of shunting.

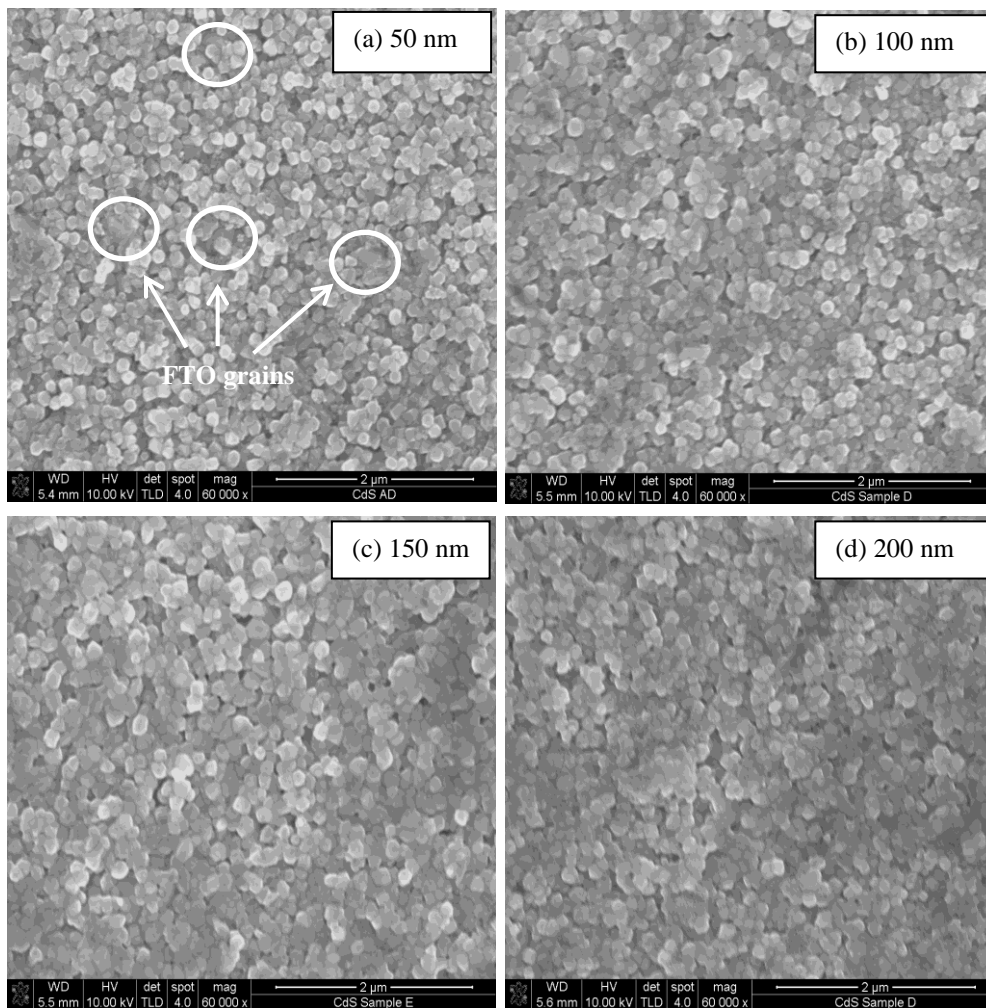


Figure 2: SEM micrographs for of CdCl₂ treated CdS layers with varying thicknesses; (a) 50 nm, (b) 100 nm, (c) 150 nm and (d) 200 nm.

3.3 STRUCTURAL PROPERTIES

For these experiments, only the results obtained from CdCl_2 treated CdS layer will be discussed due to the focus of this paper. *Figure 3* shows the XRD micrographs of g/FTO/CdS with variation in the CdS thickness between 50 nm and 200 nm. The figure shows the plot of XRD peak reflection against 2θ angle. It should be taken into account that the XRD fingerprints were stacked together for better peak comparison in *Figure 3*. From observations, all the layers are polycrystalline in nature with peaks associated with hexagonal (100), (002), (101) and (103) were observed at $2\theta=24.9^\circ$, $2\theta=26.7^\circ$, $2\theta=28.4^\circ$ and $2\theta=48.0^\circ$ respectively. It should be noted that as documented in the literature, CdS can be grown in hexagonal (wurtzite structure) and the cubic (zinc blende structure) crystallite structure with the hexagonal phase being more metastable [22]. Therefore only the hexagonal phase is retained after CdCl_2 treatment [10] as shown in this work. From observation, the peak H(002) at $2\theta=26.7^\circ$ overlaps with an FTO peak. With the effect of the FTO peak being unquantifiable, the second dominant peak along the H(101) plane was considered for detailed analysis. From observation of the 50 nm thick CdS layer, it is clear that the peak associated with H(101) is still at the emerging stage with no visible presence of peaks associated with H(100) and H(103). Increase in CdS thickness to 100 nm and above, peaks attributed to H(100) and H(103) planes were observed along with the H(101). An increase in reflection intensity with increasing thickness was also noticeable. Based on this observation, it can be said that the increase in the reflection intensity is directly associated with increasing thickness [10], [18]. The reflections observed in this work matches the JCPDS reference file No. 01-080-0006 for the hexagonal phase of CdS.

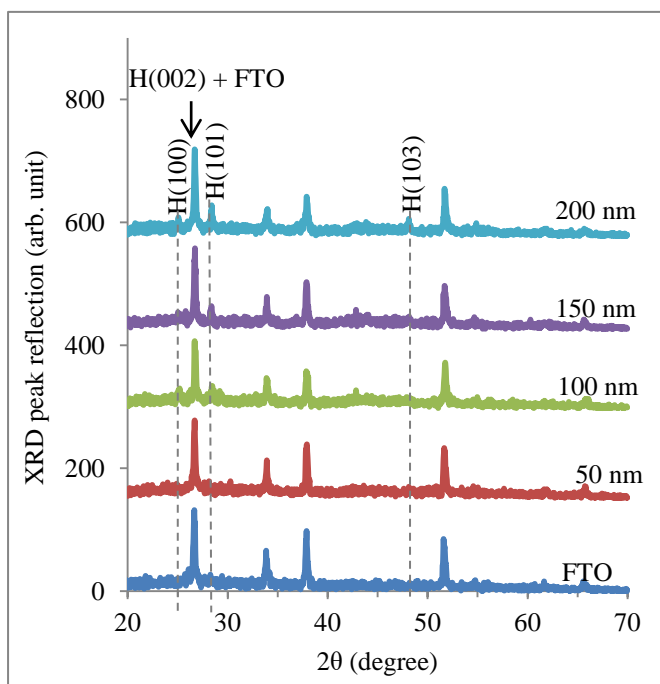


Figure 3: Typical XRD spectra observed for CdCl_2 treated CdS layers with varying thicknesses.

Other structural properties such as the peak position, full-width-at-half-maximum (FWHM), d-spacing and crystallite size are tabulated in *Table 1*. The crystallite sizes were calculated using Scherrer equation as shown in Eq. (1) where D is crystallite size, β is the FWHM of the diffraction peak in radian, θ is the Bragg angle and λ is the wavelength of the X-rays used (1.54 Å).

$$D = \frac{0.94\lambda}{\beta \cos\theta} \quad (1)$$

As observed in *Table 1*, the H(101) preferred orientation reflection of the of 50 nm thick CdS layer was indistinguishable by the Philips PW 3710 X'pert diffractometer for analysis due to its thinness or weak crystallinity. It should be noted that the electrodeposition of CdS commences with the deposition of sulphur before the deposition of cadmium is triggered [6], therefore, a sulphur rich CdS and weak CdS can be experienced at the initiation stages of nucleation of CdS. Furthermore, an increase in crystallite size was observed to be associated with the increasing thickness. Similar observation has also been documented in the literature by other independent researchers [10], [18].

Table 1: Summary of results from the XRD analysis for CdCl₂ treated CdS layers with increasing thicknesses.

Thickness (nm)	CdS(101)H reflection (arb. unit)	Peak position (°)	FWHM	d-spacing (nm)	Crystallite size D (nm)
~50	27	-	-	-	-
~100	35	28.45	0.390	0.313	22.0
~150	37	28.38	0.260	0.314	32.9
~200	50	28.42	0.195	0.317	43.9

3.4 THICKNESS MEASUREMENT

Figure 4 shows the both the as-deposited, CdCl₂ treated CdS layer and average growth current density against CdS thickness. The thickness of the as-deposited CdS layer was estimated using Faraday's law of electrolysis as shown in Eq. (2)

$$T = \frac{JtM}{nFp} \quad (2)$$

where T is the thickness of the film, J is the average deposition current density, t is the deposition time, M is the molar mass of CdTe (144.48 gmol⁻¹), n is the number of electrons transferred for deposition of 1 molecule of CdTe ($n = 2$ for CdS), $F=96485$ Cmol⁻¹ is the Faraday constant and p is the density of CdTe. While the thickness of the CdCl₂ treated CdS layers is measured using the UBM Microfocus optical depth profilometer. It should be

noted that the Faraday's law of electrolysis assumes that all the electronic charges flowing through the electrolytic bath contribute to the deposition of the CdS layers without considering the electronic charges involved in the dissociation of water into its constituent ions. Therefore, the CdS layer thickness estimated using Faraday's law of electrolysis is always higher than the measured thickness. It is clear that an increase in deposition time results into increase in the deposited layer thickness in a non-linear relationship between deposition thickness and deposition time. As observed in *Figure 4*, an increase in the deposition time results into the reduction of average deposition current density due to the reduction in the substrate conduction with increasing CdS thickness.

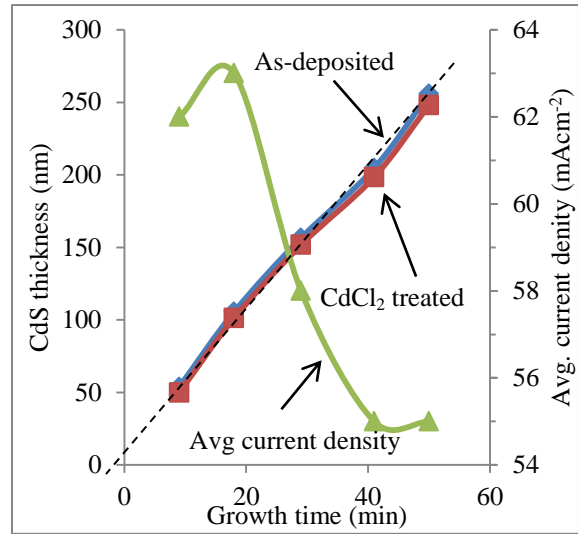


Figure 4: Typical graph of as-deposited CdS, CdCl₂ treated CdS and average deposition current density against growth time.

3.5 SOLAR CELL PERFORMANCE

Figure 5 (a) shows the band diagram of the $g/FTO/n-CdS/n-CdTe/p-CdTe/Au$ device and Figure 5 (b) shows the I-V curve of a cells incorporating 150 nm thick CdS layer at A.M1.5, while Figure 5 (c) and (d) shows the linear-linear and log-linear I-V curve of the of the $g/FTO/n-CdS/n-CdTe/p-CdTe/Au$ device incorporating 150 nm CdS layer.

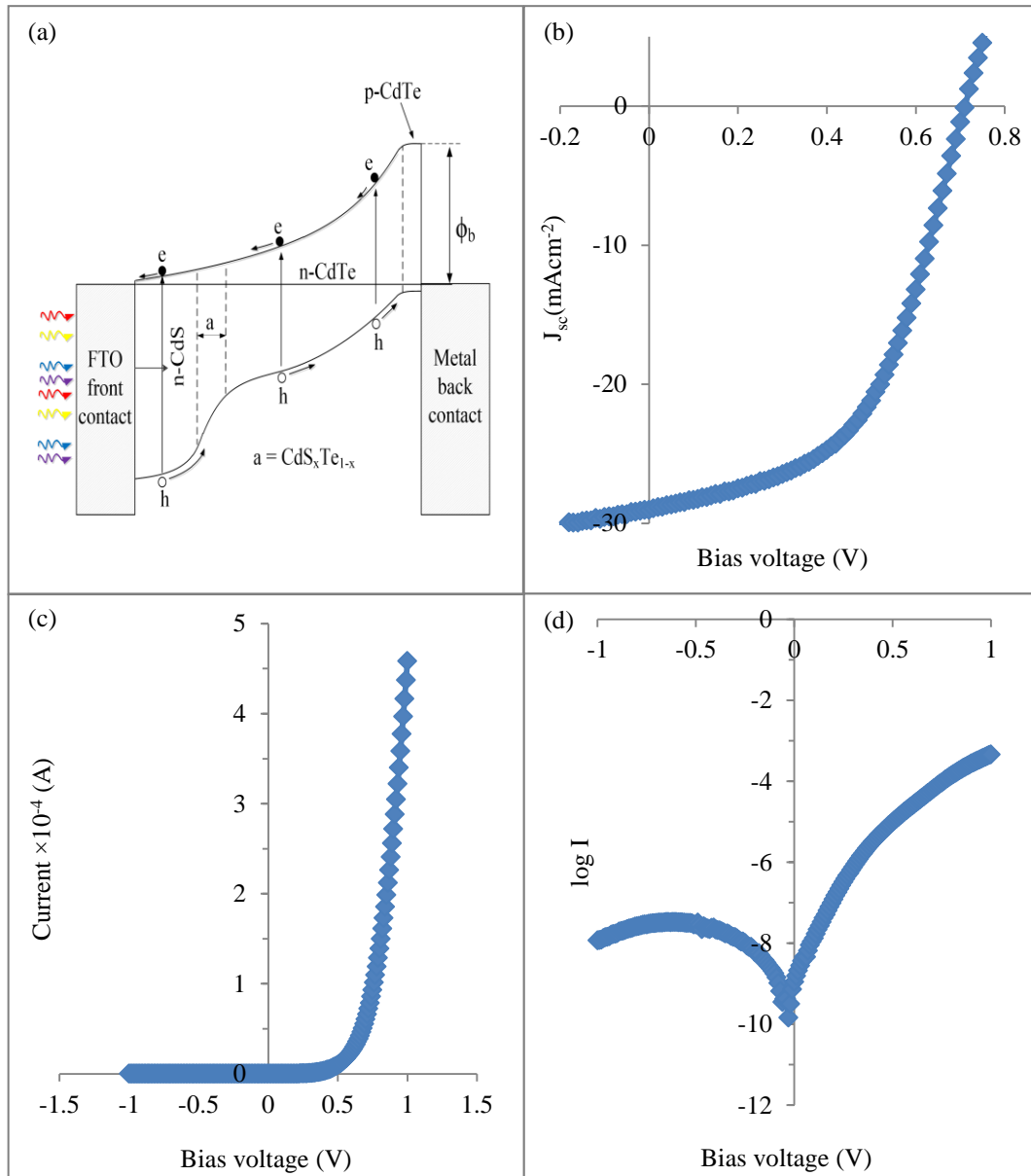


Figure 5: (a) The band diagram of the $g/FTO/n-CdS/n-CdTe/p-CdTe/Au$ thin film solar cell and (b) current-voltage curve of $g/FTO/n-CdS/n-CdTe/p-CdTe/Au$ champion cell incorporating 150 nm CdS, while (c) and (d) are its the linear-linear and log-linear I-V curve under condition.

The band diagram as depicted in *Figure 5 (a)* is a result of prior material investigation as reported in the literature by Salim et al [14] that the conductivity type of electrodeposited CdTe layer is retained after CdCl₂ treatment, although, a shift towards the opposite conductivity type was observed.

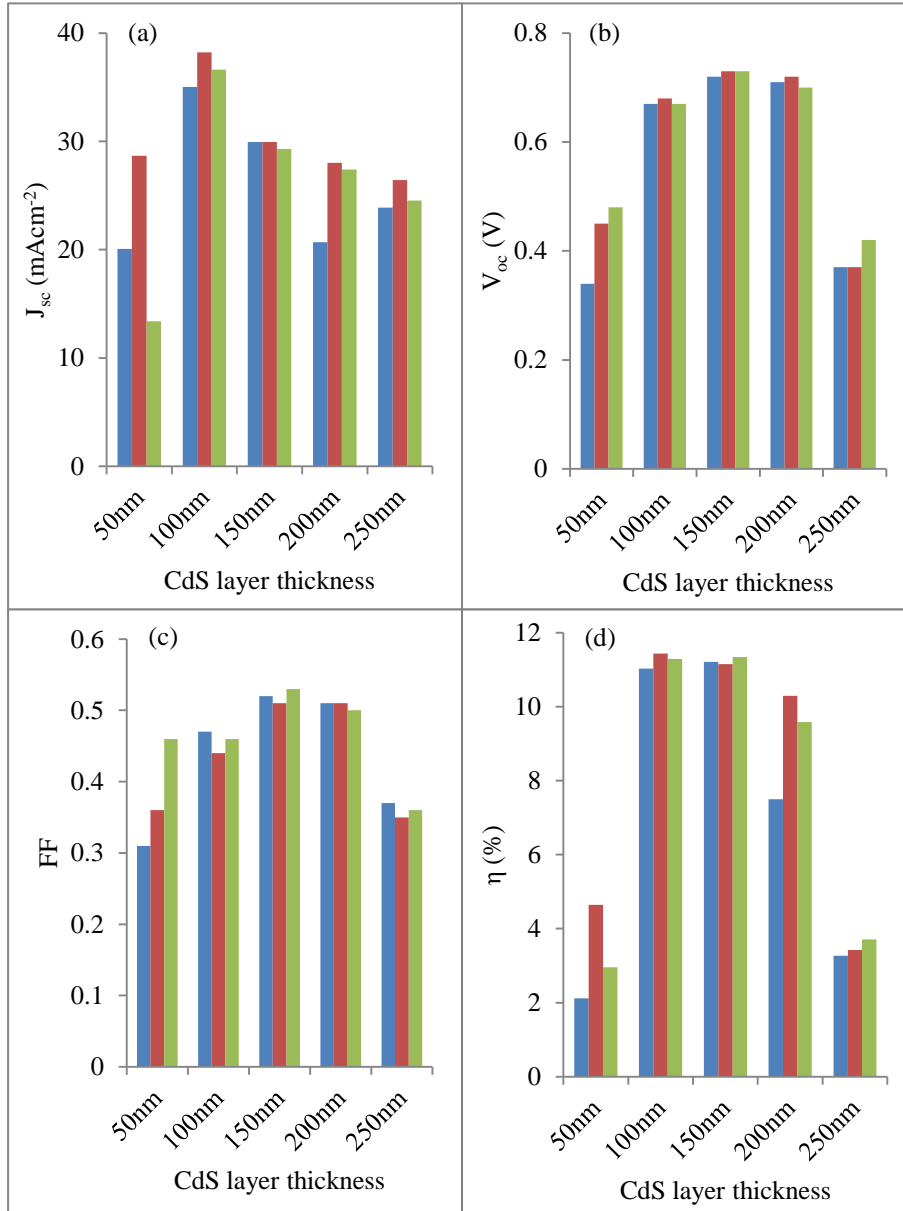


Figure 6: Histogram of three champion solar cells parameters from g/FTO/n-CdS/n-CdTe/p-CdTe/Au with different CdS thicknesses measured at A.M1.5 (a) J_{sc} against CdS thickness, (b) V_{oc} against CdS thickness, (c) FF against CdS thickness and (d) η against CdS thickness.

Figure 6 (a-d) shows the short-circuit current density (J_{sc}), open-circuit voltage (V_{oc}), fill factor (FF) and photon-to-electron conversion efficiency (η) measured at A.M1.5 against CdS layer thickness respectively, while *Table 2* summarises the tabulated I-V parameters of the three champion cells from the solar devices with varied CdS thickness. As shown in *Figure 6 (a)*, the comparatively low J_{sc} observed in the device incorporating

the 50 nm CdS layer was not expected due to the high transmittance in 50 nm thick CdS layer as discussed in Section 3.1, hence, high photocurrent is expected. But based on the incomplete coverage of the underlying g/FTO substrate, the gaps will serve as shunting paths and thereby reducing the photo-generated current due to increases recombination of the electron-hole pairs and poor quality diode.

The increase in the CdS thickness in the device configuration to 100 nm shows higher J_{sc} due to better CdS layer coverage over the g/FTO and high transmittance as discussed in Section 3.1. The devices incorporating CdS with thickness above 100 nm, shows a gradual reduction in J_{sc} . This might be as a result of the reduction in transmittance, photo-generated current and also increased parasitic absorption due to increased CdS thickness [3], [7]. Low CdS thickness (40 nm) was demonstrated by Ganata et al, 2000 [3] to achieve the highest photocurrent using high temperature (600°C) closed-space-sublimation growth technique due to the unique qualities of CdS. However, electrodeposition at low temperature (~85°C) on the other hand, requires increased thickness of CdS layer to suppress the effect of surface roughness and deposition/nucleation mechanism. It should be noted that the J_{sc} as observed in this work is higher than the Shockley–Queisser limit on single $p-n$ junction [23] due to the incorporation of the multilayer $n-n-p$ configuration [24]

Table 2: Tabulated device parameters of g/FTO/n-CdS/n-CdTe/p-CdTe/Au incorporating different CdS thicknesses.

CdS (nm)	J_{sc} (mAcm ⁻²)	V_{oc} (mV)	FF	Efficiency (%)
50	20.1	0.34	0.31	2.11
	28.7	0.45	0.36	4.64
	13.4	0.48	0.46	2.95
100	35.0	0.67	0.47	11.03
	38.2	0.68	0.44	11.43
	36.6	0.67	0.46	11.29
150	29.9	0.72	0.52	11.29
	29.9	0.73	0.51	11.15
	29.3	0.73	0.53	11.34
200	20.7	0.71	0.51	7.50
	28.0	0.72	0.51	10.29
	27.4	0.70	0.50	9.59
250	23.9	0.37	0.37	3.27
	26.4	0.37	0.35	3.42
	24.5	0.42	0.36	3.71

An increase in both V_{oc} and FF with increasing CdS thickness up to 200 nm as shown in *Figure 6* (b-c) is also observed. This observation can be associated with the reduction of shunt [4] and other defects relating to the early CdS nucleation stages. Ultimately, the efficiency of devices incorporating both the 100 nm and 150 nm

thick CdS layer appears to be the best devices with fairly similar efficiency values due to comparatively high J_{sc} observed in the 100 nm CdS and high V_{oc} plus FF in the device incorporating 150 nm thick CdS layer. It should be taken into account that shunt resistance is associated with semiconductor layer quality [25] which explains the low efficiency observed in the device incorporating the electrodeposited 50 nm thick CdS layer. While the gradual reduction in efficiency with increasing thickness is due to the low transmittance, reduced photocurrent as a result of increased parasitic absorption [4].

Table 3: Diode parameters extracted from dark I-V for champion cells of g/FTO/n-CdS/n-CdTe/p-CdTe/Au incorporating different CdS thicknesses in Table 2

CdS (nm)	R_{sh} (Ω)	R_s (Ω)	$\log(RF)$	I_o (A)	n	ϕ_b (eV)
50	51.1	23.3	0.3	2.81×10^{-3}	>2.00	>0.42
100	4.3×10^6	500.0	4.1	1.02×10^{-9}	1.86	>0.80
150	6.2×10^6	577.7	4.4	1.26×10^{-9}	1.71	>0.80
200	3.5×10^6	800.0	3.5	3.98×10^{-9}	1.95	>0.77

Table 3 shows the diode parameters such as shunt resistance R_{sh} , series resistance R_s , rectification factor RF , saturated current I_o , ideality factor n and barrier height ϕ_b as obtained from the champion cells of the g/FTO/n-CdS/n-CdTe/p-CdTe/Au devices incorporating different CdS thicknesses tabulated in *Table 2*. As observation in *Table 3*, the low R_{sh} observed for devices incorporating 50 nm thick CdS layer signifies the presence of shunt paths. The shunting might be due to the incomplete coverage of the g/FTO with CdS as discussed in Section 3.2. Thereby creating direct leakage path between the g/FTO substrate and the grown CdTe layers as further suggested by the comparatively high I_o value observed using the 50 nm thick CdS layer. From observation, the R_s under dark condition are high for layers incorporating CdS thickness of 100 nm and above. However, I-V measurements under illuminated condition shows a reduction in R_s value to (100 – 200) Ω ranged. This reduction is due to the photoconductivity of the material layer used. As iterated by Dharmadasa et al [1], high efficiency solar cells can only be achieved provided the RF value is $\geq 10^3$. The RF values as observed for devices incorporating CdS with thickness ≥ 100 nm shows the tendency of achieving high efficiency. Furthermore, the ideality factor n which depicts the charge carrier transportation mechanisms show that the g/FTO/n-CdS/n-CdTe/p-CdTe/Au devices incorporating CdS with thickness between 100 nm and 200 nm are governed by both recombination and generation (R&G) centres and thermionic emission. While the charge carrier transportation mechanism of devices incorporating the 50 nm CdS thickness is governed not only by R&G centres and thermionic emission but also due to tunnelling of high energy electrons through the barrier height [26] resulting into a reduction in the barrier height as observed in *Table 3*. The lowest ideality factors observed for 100 & 150

nm shows the presence of low defects reducing R&G process. Therefore the J_{sc} values can be large for such devices as we experimentally observed in this work.

3.5.1 PHOTOVOLTAIC (PV) DEVICE YIELD

Figure 7 shows the graph of the percentage yield of the active cells as against the CdS thickness incorporated in the g/FTO/n-CdS/n-CdTe/p-CdTe/Au structure. The number of cells in all the fabricated solar cell devices incorporating different CdS window layer thicknesses was 12. It was discovered that the percentage of PV active cell in the device incorporating 50 nm thick CdS was low. This observation can be related to the morphological analysis as discussed in Section 3.2.

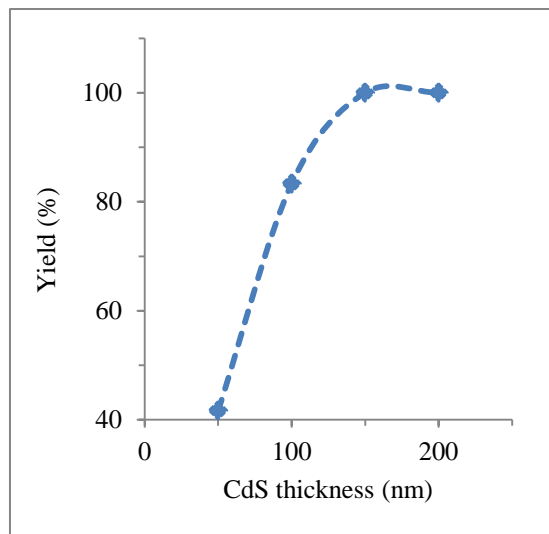


Figure 7: Graph of percentage yield against CdS thickness in a g/FTO/n-CdS/n-CdTe/p-CdTe/Au device structure.

There is a high tendency that the non-functional cells are g/FTO/n-CdTe/p-CdTe/Au due to the incomplete coverage of the underlying CdS layer. It should be noted that although the grown CdTe layer with a supposed depletion in-between the n-CdTe and p-CdTe but due to the characteristic large grains observed in CdTe after treatment, the increased grain growth of CdTe on a rough surface favours the inclusion of pores or pinholes in-between the grains after treatment. Which leaves Au with the tendency of contacting directly with g/FTO creating a shunting paths and electron-hole pair recombination centres. An increase in the CdS thickness above 50 nm improves the percentage yield close to 100% at 150 nm CdS thickness.

3.5.2 STANDARD DEVIATION

Figure 8 shows the normal distribution curve of both J_{sc} and η using standard deviation parameters as calculated in Table 4. As stated in Section 3.5.1 only three champion cells from each fabricated device incorporating 50

nm, 100 nm and 150 nm thick CdS was considered in this work due to high parasitic absorption observed with higher CdS thickness. Both the mean (\bar{x}) and the standard deviation (δ) were calculated as shown in Eq. (3) and Eq. (4) respectively, where n is the number of cells explored and x is the value to explored cells.

$$\bar{x} = \frac{1}{n} \sum_{i=1}^n x_i \quad (3)$$

$$\delta = \sqrt{\frac{\sum(x - \bar{x})^2}{n-1}} \quad (4)$$

It should be noted that the data utilised in the calculations shown in *Table 4* is an extract from *Table 2*. The standard deviation as depicted using the normal distribution curve is used to measure the dispersion in a set of explored data. The horizontal axis represents the dependent variable which for the sake of the work is J_{sc} and η in *Figure 8* (a) and (b) respectively while the vertical axis shows the probability that the value of the standard deviation will occur.

Table 4: Table of mean and standard deviation of three champion cells device parameter incorporating different CdS thickness in g/FTO/n-CdS/n-CdTe/p-CdTe/Au configuration.

	Mean $\bar{x} = \frac{1}{n} \sum_{i=1}^n x_i$				Standard deviation $\delta = \sqrt{\frac{\sum(x - \bar{x})^2}{n-1}}$			
CdS (nm)	J_{sc} (mAcm ⁻²)	V_{oc} (V)	Fill factor	Efficiency (%)	J_{sc} (mAcm ⁻²)	V_{oc} (V)	Fill factor	Efficiency (%)
50 nm	20.70	0.423	0.38	3.24	7.66	0.074	0.0764	1.2879
100 nm	36.62	0.673	0.46	11.25	1.59	0.006	0.0153	0.2039
150 nm	29.72	0.726	0.52	11.23	0.37	0.006	0.0100	0.0971
200 nm	25.37	0.710	0.51	9.12	4.06	0.010	0.0058	1.4537
250 nm	24.95	0.386	0.36	3.47	1.33	0.029	0.0100	0.2222

As shown in *Figure 8* (a), the highest J_{sc} was observed in the device incorporating the 100 nm thick CdS layer with a 50% probability of achieving 36.62 mAcm⁻² and ~30% probability of occurrence as compared to the devices incorporating 150 nm thick CdS layer with 50% probability of achieving a J_{sc} of 29.72 mAcm⁻² and ~80% probability of occurrence. In both the device incorporating 100 nm and 150 nm thick CdS interesting features such as high J_{sc} and high probability of occurrence can be explored by carefully optimising the CdS layer thickness to fall in-between 100 and 150 nm CdS thickness. It should be noted that one of the advantages related to an increase in the thickness of the CdS window layer is smoothening out the surface before absorber layers such as CdTe can be grown. Device incorporating the 50 nm thick CdS layers shows the largest dispersion of J_{sc} , lowest J_{sc} value range and less than 10% probability of achieving comparably high photocurrent based on the results obtained from this work. For example, based on the normal curve generated in

Figure 8 (a), less than 5% of the fabricated cell in a device can achieve J_{sc} of 30 mAcm^{-2} and above for cells incorporating 50 nm CdS thickness as compared to the devices with the 100 nm and 150 nm thick CdS with 100% and 50% probability for achieving 30 mAcm^{-2} short-circuit current density respectively. The effect of both pin-holes and parasitic absorption is clearly annotated for the low (50 nm) and high (150 nm) CdS thickness in this work.

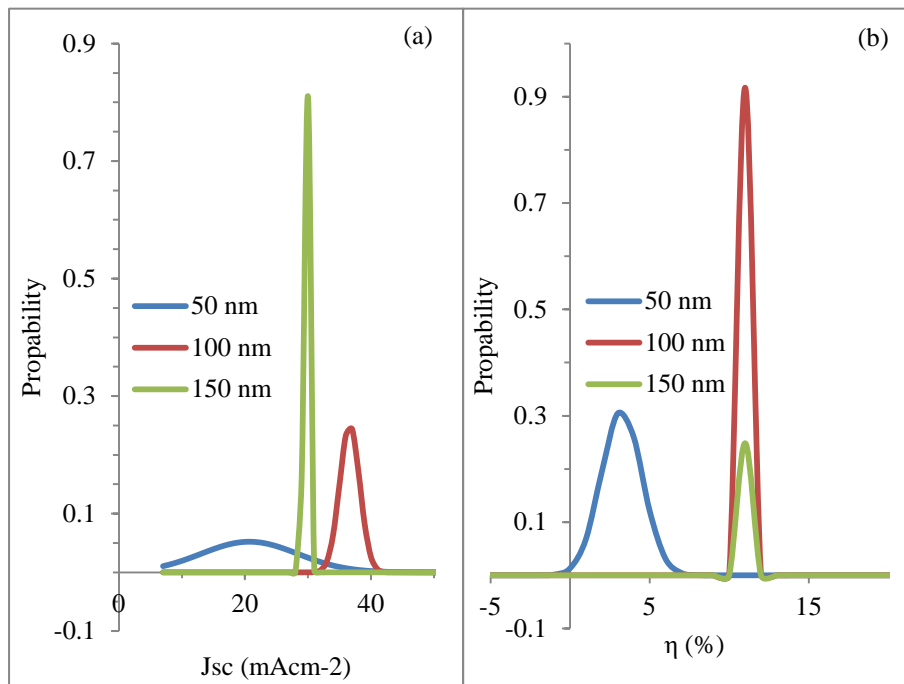


Figure 8: Normal curve of probability of occurrence against (a) J_{sc} and (b) η .

Furthermore, Figure 8 (b), shows that the highest η can be achieved with devices incorporating both 100 nm and 150 nm thick CdS with high occurrence probability of ~90% observed at 100 nm and ~30% occurrence probability for the 150 nm thick CdS. It should be noted that the η of the device incorporating the 50 nm thick CdS shows low η values range and low probability of occurrence.

4 CONCLUSIONS

In conclusion, this work supports work done by other researchers on the optimisation CdS thickness as related to CdS/CdTe cell but focuses on the iteration of the effect of deposition technique and nucleation mechanism of electroplated semiconductor materials. But contrarily, the proposed thin CdS window layer with thickness <50 nm by other authors cannot achieve comparatively high efficiency using electrodeposition technique without detrimental effect as demonstrated in this paper.

From the observed results, optical properties such as transmittance favour the 50 nm CdS thickness while crystallinity favours the highest CdS thickness with increase in both crystallite size and preferred orientation reflection intensity. But with a more critical observation on PV property and statistical analysis, the g/FTO/n-CdS/n-CdTe/p-CdTe/Au show better device property with the incorporation of 100 nm to 150 nm thick CdS layer relative to the optical, morphological, structural and electronic properties analyses of the incorporated CdS layer. Work is progressing in the optimisation of other layers and the improvement of the utilised configuration.

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