# Investigation of electronic quality of electrodeposited cadmium sulphide layers from thiourea precursor for use in large area electronics

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# Investigation of Electronic Quality of Electrodeposited Cadmium Sulphide Layers from Thiourea Precursor for use in Large Area Electronics

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## ABSTRACT

CdS layers used in thin film solar cells and other electronic devices are usually grown by wet chemical methods using $CdCl_2$ as the Cadmium source and either $Na_2S_2O_3$, $NH_4S_2O_3$ or $NH_2CSNH_2$ as Sulphur sources. Obviously, one of the sulphur precursors should produce more suitable CdS layers required to give the highest performing devices. This can only be achieved by comprehensive experimental work on growth and characterisation of CdS layers from the above mentioned sulphur sources. This paper presents the results observed on CdS layers grown by electrodepositing using two electrode configuration and thiourea as the sulphur precursor. X-ray diffraction (XRD), Raman spectroscopy, optical absorption, scanning electron microscopy (SEM), energy-dispersive X-ray analysis (EDX) and photoelectrochemical (PEC) cell methods have been used to characterise the material properties. In order to test and study the electronic device quality of the layers, ohmic and rectifying contacts were fabricated on the electroplated layers. Schottky barriers, formed on the layers were also compared with previously reported work on Chemical Bath Deposited CBD-CdS layers and bulk single crystals of CdS. Comparatively, Schottky diodes fabricated on electroplated CdS layers using two-electrode system and thiourea precursor exhibit excellent electronic properties suitable for electronic devices such as thin film solar panels and large area display devices.

Keywords: Semiconductor, Thin films, Electrical properties, Electrochemical technique.

## 1. INTRODUCTION

The study of the structural, optical, morphological and physical properties of binary compound semiconductors such as cadmium sulphide (CdS) thin films is a subject of current interest due to its applications in optoelectronic and large area electronic devices. In photovoltaics, polycrystalline CdS thin films are often used as a window layer in the CdS/CdTe solar cells configuration in order to achieve highest efficiency. CdS thin films have been grown using over 10 different techniques [1] as reported in the literature with electrodeposition edging other deposition based on its simplicity, low cost, scalability amongst other attributes [2]. The electrodeposition of CdS as reported in the literature is done mainly by using Sodium thiosulfate ($Na_2S_2O_3$) as the sulphur precursor. This precursor is associated with the formation of sulphur precipitate during growth and the accumulation of sodium, Na, in the electrolytic bath [3]. The incorporation of p-type dopant such as Na into CdS layer through absorption or chemical reaction will reduce the electrical conductivity of the grown layer and thus constituting a drawback in the electrical property of the CdS layer [3]. Therefore, in a view of depositing CdS from other sulphur precursors without the aforementioned drawbacks, other sulphur source needs to be explored. Sulphur source such as thiourea ($NH_2CSNH_2$) has been well established in the growth of CdS using chemical bath deposition (CBD) technique, but literature on the use of electrochemical technique for this precursor is scarce. Electrodeposition (ED) technique is comparatively advantageous with respect to deposition process continuity and Cd-containing waste reduction. Although, preliminary investigation of the electrodeposition of CdS from thiourea has been explored in 2001 by Yamaguchi et al [4], but this paper presents in full the comprehensive details of the growth and characterization of CdS from $NH_2CSNH_2$ precursor and further investigate the effect of $CdCl_2$ treatment, film thickness and heat treatment duration on the electronic quality of electrodeposited CdS layers.
This article goes beyond the growth and characterisation norm into the comparative analysis of the electronic properties of electrodeposited CdS using thiourea precursor to CBD-CdS and single crystal CdS previously reported in the literature.

## 2. EXPERIMENTAL DETAILS

### 2.1 Electrolytic Bath Preparations

CdS thin films were cathodically electrodeposited on glass/FTO substrates by potentiostatic technique in which the counter electrode was a high purity graphite rod. Cadmium chloride hydrate ($CdCl_2 \cdot xH_2O$) of 98% purity and Thiourea ($NH_2CSNH_2$) of 99% purity were used as cadmium and sulphur sources respectively. The electrolyte was prepared by dissolving 0.12M $CdCl_2 \cdot xH_2O$ and 0.18M $NH_2CSNH_2$ in 800 ml de-ionised (DI) water contained in a 1000 ml polypropylene beaker. The polypropylene beaker was placed inside a 1800 ml glass beaker containing DI water. The glass beaker serves as the outer bath and helps to maintain uniform heating of the electrolyte. The solution was stirred and electro-purified for ~50 hours to reduce the impurity level and to achieve homogeneity of the solution. Afterwards, a complete characterisation of the CdS grown at different voltages were undertaken to determine the optimum growth voltage ($V_g$). For these experiments, the bath temperature was maintained at 85˚C during the CdS growth to achieve higher crystallinity due to high deposition temperature [5]. However, the temperature increase is limited due to the use of aqueous solution. The pH value was adjusted to 2.50±0.02 at the start of deposition using diluted solutions of HCl and $NH_4OH$ for all the samples. It is important to maintain the pH of the electrolytic bath between 2.00 and 3.00 as an increase or decrease in pH outside this range results into the formation of white precipitates of cadmium hydroxide and rapid precipitation

of CdS [6]. Two-electrode configuration was used in this study with glass/FTO as the working electrode. The working electrodes of sheet resistance ~7 Ω/□ were cut into 2×4 $cm^2$ pieces and a high purity carbon rod was used as the anode. Computerized Gill AC potentiostat was utilised as the power supply source. The cyclic voltammogram of the resulting electrolyte(s) were recorded prior to the deposition of CdS layer to determine the possible deposition voltage range of CdS.
All the substrates and chemicals used in this study were procured from Sigma Aldrich Ltd, UK.

### 2.2 Substrate Preparation

Substrates were ultrasonically cleaned at the initial stage in soap solution for the duration of 20 minutes and rinsed in deionised (DI) water. The substrates were then cleaned thoroughly with methanol and acetone to remove any grease and rinsed in DI water. Finally, the FTO is submerged in a clean beaker of DI water and transferred directly into the electroplating bath. Prior to characterisation, electrodeposited CdS layers were rinsed, dried and divided into two halves. One half was left as-deposited and the other half was cut into several samples and heat treated in the presence of $CdCl_2$ at 400˚C in air for different time durations to enhance its properties.

### 2.3 Experimental Techniques

The level of crystallinity, crystalline structure and phase identification of the as-deposited and post-growth treated CdS layers were obtained using X-Ray diffraction (XRD) technique. This information were extracted using Philips PW 3,710 X'pert diffractometer with Cu-$K_\alpha$ monochromator of wavelength λ=1.54 Å. The X-ray generator tension and current were adjusted to 40 kV and 40 mA respectively for this set of experiments. Optical properties such as the absorbance and transmittance were studied at room temperature using Carry 50 Scan UV-Vis spectrophotometer between the wavelengths of 200 nm to 800 nm using a thoroughly cleaned TEC7 FTO as baseline. Raman spectroscopy studies were performed on samples using Renishaw InVia Raman spectrometer using a 514 nm argon ion laser excitation source to identify the phases, determine the phonon modes, and also to determine the nature of crystallinity of both the as-deposited and the $CdCl_2$ treated samples. The Raman spectroscopy objective and laser power were set to ×100 and 50% respectively. CdS layers thickness was measured using UBM Microfocous optical depth profilometer (UBM, Messetecknik GmbH, Ettlingen, Germany). While the surface morphology and the compositional analysis of both the as-deposited and $CdCl_2$ treated CdS layers were studied using FEI Nova 200 NanoSEM equipment. Using conventional Hall Effect measurements to determine the electrical properties of CdS deposited on FTO will not be possible due to the underlying conducting layer. Therefore, PEC cell measurement was conducted to determine the electrical conductivity type of the CdS layer. This was conducted by dipping the glass/FTO/CdS into an aqueous electrolyte containing 0.1M $Na_2S_2O_3$ to form a solid/liquid junction. The difference between the voltages measured under illuminated ($V_L$) and dark ($V_D$) conditions provides the PEC signal and determines the electrical conductivity type of the CdS layer.

## 3. RESULTS AND DISCUSSION

### 3.1 Cyclic Voltammetric Study

Cyclic voltammogram is a plot of current density as a function of the applied voltage across an electrolytic bath. Fig. 1 shows the cyclic voltammogram of aqueous solution of a mixture of 0.12M $CdCl_2 \cdot xH_2O$ and 0.18M $NH_2CSNH_2$ in 800 ml of DI water during the forward and reverse cycles between 100 and -1500 mV cathodic voltage at pH 2.50±0.02 and a fixed scan

rate of 3 $mVs^{-1}$. The stirring rate and temperature of the bath was kept constant at 300 rpm and 85˚C respectively. According to the redox potential value of cadmium and sulphur ions, sulphur deposits first (E˚ for sulphur is -0.43 V w.r.t. standard $H_2$ electrode), followed by cadmium (E˚ for cadmium is -0.40 V w.r.t. standard $H_2$ electrode). The complete electro-chemical equation for the formation of CdS at the cathode can be written as:

$$Cd^{2+} + S_2O_3^{2-} + 2e^- \rightarrow CdS + SO_3^{2-} \quad (1)$$

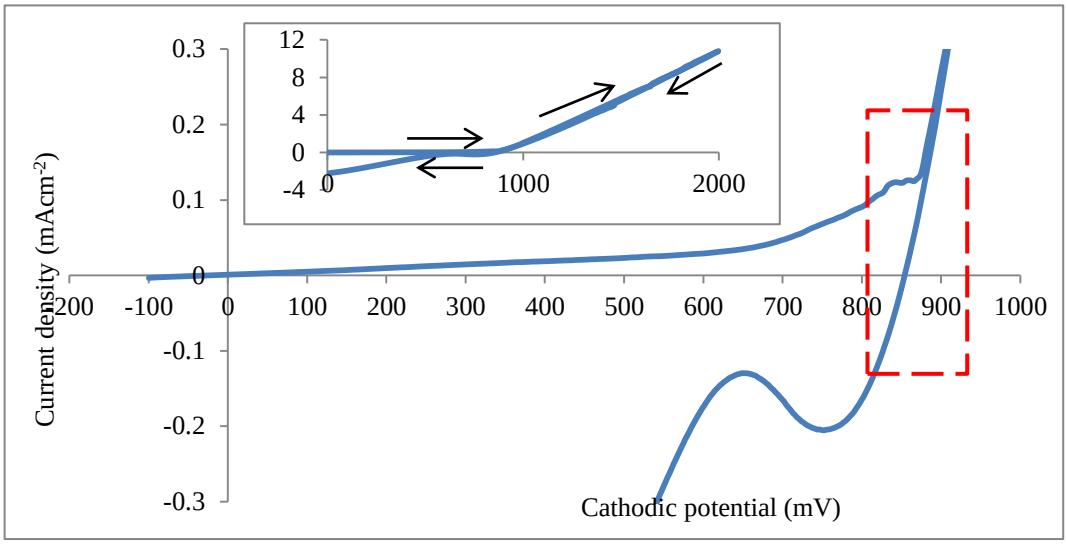


*Fig. 1: A typical cyclic voltammogram for deposition electrolyte containing the mixture of 0.12M $CdCl_2 \cdot xH_2O$ and 0.18M $NH_2CSNH_2$ at ~85˚C and pH=2.50±0.02.*

It was observed in the forward cycle that, between the cathodic voltage range 785 mV and 880 mV, the deposition current density appears to be fairly stable within the range of ~130 $\mu Acm^{-2}$. The growth voltage range (i.e. 785 mV to 880 mV) had been pre-characterized at cathodic voltage steps of 10 mV using XRD analysis (not presented in this paper). The highest XRD peak intensity was observed at 790 mV. Therefore, the surrounding cathodic voltage was scanned at steps of 1 mV to further investigate surrounding growth voltage values. The result of the characterised CdS layers grown between the cathodic voltages of (788–793) mV using PEC cell measurement, optical absorbance and transmittance measurement, XRD and SEM were used to determine the optimised growth conditions.

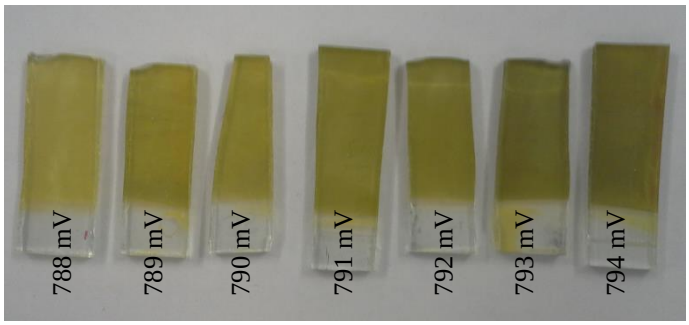


*Fig. 2: The physical appearances of as-deposited CdS grown at $V_g$ from 788 mV to 794 mV.*

It was also observed during the voltammetric cycle that the deposited film colour changes to transparent yellow at growth voltages ($V_g$) ≥780 mV which suggests a region of sulphur richness. The deposited film colour turns to transparent greenish-yellow at growth voltage

above 780 mV which suggest the presence of stoichiometric or near stoichiometric CdS thin films. As the growth voltage increases above 793 mV, the film colour changes to dark green as shown in Fig. 2. This can be attributed to Cd richness in CdS. Therefore, stoichiometric CdS thin film range can be qualitatively predicted by appearance during voltammetric cycle.
It should be noted that above 880 mV cathodic voltage, high current density is observed with detrimental effect on the ED-CdS layer quality. The sharp increase in current density might be due to the electrolysis of water and the deposition of Cd dendrites.
It was interesting to observe no sulphur precipitate was observed throughout this sets of experiments which is one of the problems associated with other sulphur sources.

### 3.2 Structural Analysis

#### 3.2.1 X-ray Diffraction Study

After preliminary growth and characterization, CdS layers were grown between (788–793) mV cathodic voltages at 1 mV step change so as to comb the cathodic voltages surrounding the predetermined 790 mV to identify the stoichiometric or near stoichiometrically grown CdS layer. For this work, each CdS sample was grown for the same time period and $CdCl_2$ treated under the same condition. The observed XRD peaks/crystallinity for both the as-deposited and $CdCl_2$ treated CdS layers within this cathodic voltage range were compared as shown in Fig. 3 (a-b), Fig. 4 and Fig. 5.
As observed in Fig. 3, all the as-deposited CdS layers were polycrystalline with a preferred peak orientation along the CdS (002)H plane which coincides with the FTO peak at angle 2θ=26.68˚. The as-deposited CdS layers were polycrystalline with peak orientations corresponding to CdS (100)H at 2θ=24.90˚, CdS (002)H at 2θ=26.68˚, CdS (101)H at 2θ=28.86˚, CdS (220)C at 2θ=46.98˚, CdS (103)H at 48.01˚, Cd (101)H at 2θ=38.89˚ and S (319)O at 2θ=42.63˚ present. This indicates the inclusion of elemental Cd and S, together with Cubic –CdS phase within the main phase of hexagonal-CdS. The preferred peak orientation along the CdS (002)H plane coincides with FTO peak at 2θ=26.68˚. Due to the effect of the FTO peak on the CdS (002)H peak intensity, CdS (101)H at 2θ=28.86˚ with the second predominant peak intensity was utilised as the preferred peak for analysis of the CdS layers. After $CdCl_2$ treatment, peaks identified as Cd (101)H at 2θ=38.89˚, S (319)O at 2θ=42.63˚ and CdS (220)C at 2θ=46.98˚ completely disappears as observed in Fig. 3(b) and Fig. 5. This can be attributed to the diffusion of excess sulphur, the formation CdS from the reaction between elemental Cd and S to form hexagonal-CdS and the instability of cubic phase CdS after heat treatment. Substantial increase in XRD peak intensity of CdS in hexagonal phases were also observed after $CdCl_2$ treatment except for CdS (103)H as shown in Fig. 5.
It is well documented in the literature that CdS can grow in two different crystalline structures, namely the hexagonal (wurtzite structure) and the cubic (zinc blend structure) with the hexagonal being the more metastable phase [7]. Hence, the hexagonal CdS phases were retained after $CdCl_2$ treatment at 400˚C for 20 minutes. The initial presence of CdS in both hexagonal and cubic phases in the as-deposited layers may be attributed to vigorous stirring during growth at low temperature as argued by Kaur et al [8]. All the hexagonal phases of CdS in the as-deposited layer showed a substantial increase in intensity after $CdCl_2$ treatment except for CdS (103)H as shown in Fig. 5. These alterations in the XRD peak intensity might be due to the reorientation of the crystal lattice during heat treatment in the presence of $CdCl_2$ [9].
A plot of CdS(101)H peak intensity against cathodic voltage for both as-deposited and $CdCl_2$ treated samples as depicted in Fig. 4 shows that the highest peak intensity was attained at 791 mV under the conditions used in this work. The extracted XRD data from these CdS

material work matches the JCPDS reference file No. 01-080-0006 and 00-001-0647 for both the hexagonal and cubic phases respectively. The crystallite size, D was calculated using the Scherrer's formula:

$$D = \frac{0.94\lambda}{\beta \cos\theta} \qquad (2)$$

Where λ is the wavelength of the X-rays used (1.542 Å), β is the full width at half maximum (FWHM) of the diffraction peak in radian and θ is the Bragg angle. The summary of XRD data and obtained structural parameters of CdS thin films grown at $V_g$=791 mV is shown in Table 1.

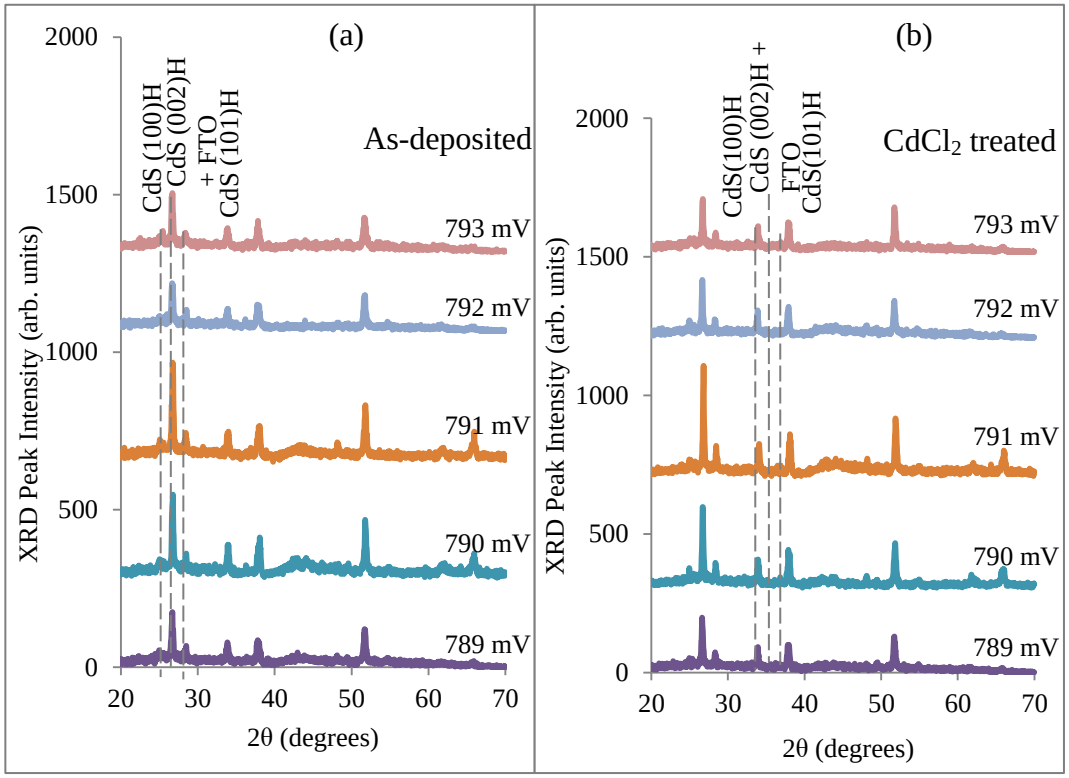


*Fig. 3: Typical XRD patterns of CdS layers grown between 789–793 mV deposition potential for (a) As-deposited CdS layers (b) $CdCl_2$ treated CdS layers at 400˚C for 20 minutes.*

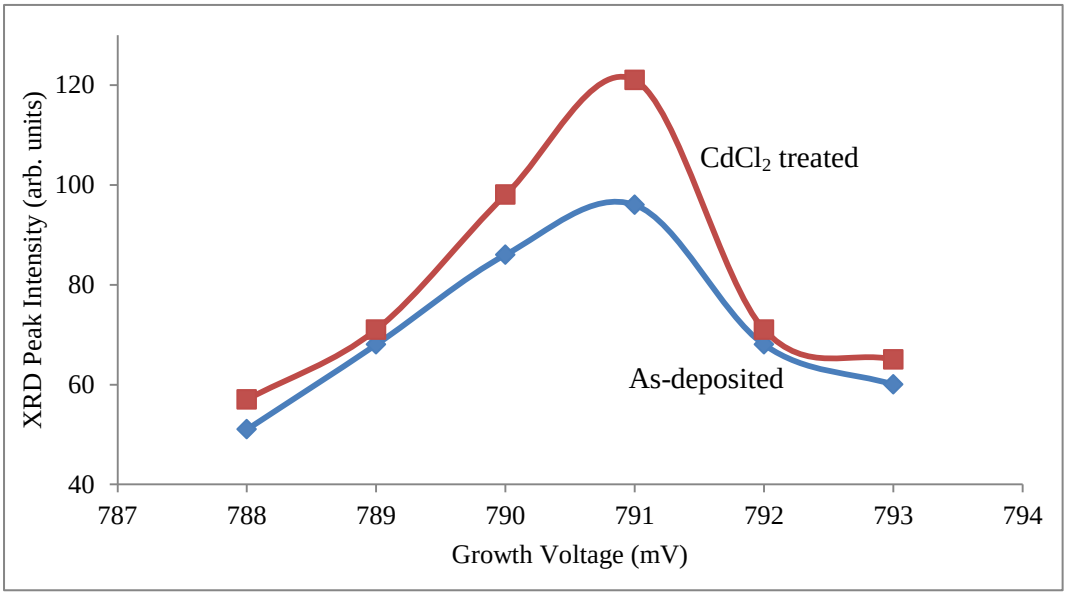


*Fig. 4: Comparative analysis CdS (101)H peak for as-deposited and $CdCl_2$ treated layer grown at different growth voltages grown at 791 mV.*

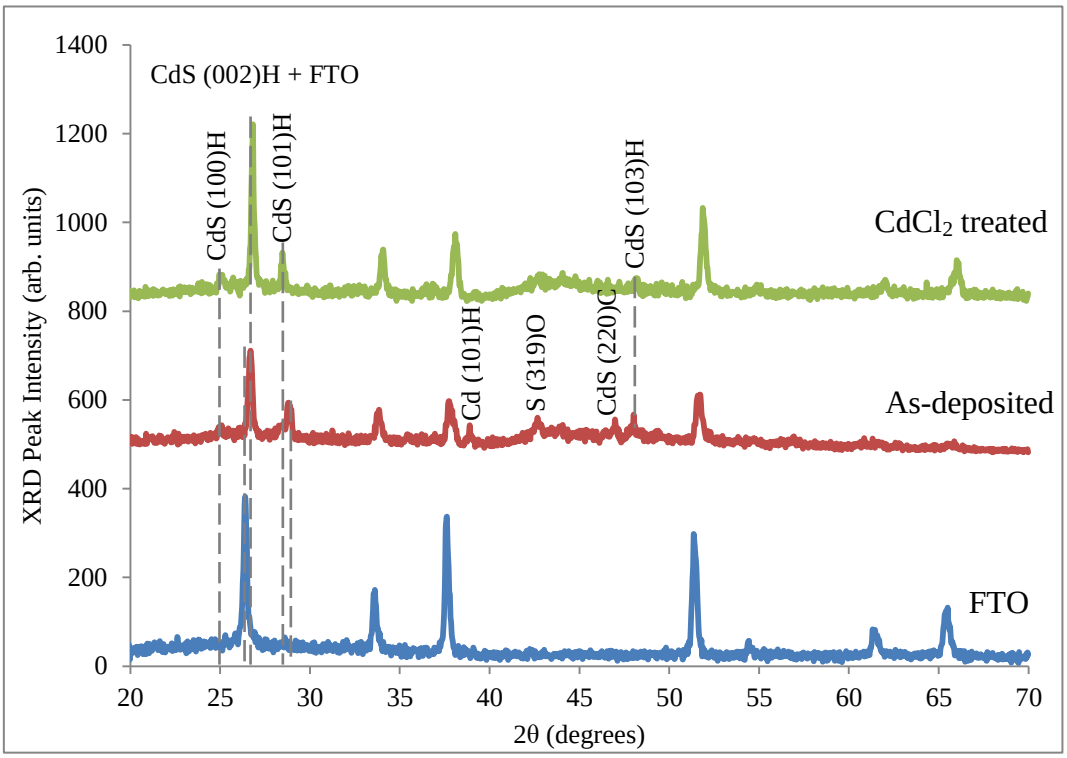


*Fig. 5: Comparative analysis of peaks from as-deposited and $CdCl_2$ treated CdS layers grown at 791 mV.*

*Table 1: The XRD analysis of CdS layers grown at cathodic potential of 791 mV for the as-deposited and the $CdCl_2$, heat-treated layers at 400˚C for 20 minutes in air.*

| Sample | 2θ (degrees) | Lattice Spacing (Å) | FWHM (Degrees) | Crystallite Size D (nm) | Plane of Orientation (hkl) | Assignments |
|---|---|---|---|---|---|---|
| As-Deposited | 24.90 | | | | (100) | Hex CdS |
| | 26.69 | 3.340 | 0.227 | 37.5 | (002) | Hex CdS/FTO |
| | 28.83 | 3.097 | 0.195 | 44.0 | (101) | Hex CdS |
| | 38.92 | 2.314 | 0.195 | 45.2 | (101) | Hex Cd |
| | 42.64 | 2.121 | 0.390 | 22.9 | (319) | Orth S |
| | 47.00 | 1.933 | 0.260 | 34.8 | (220) | Cubic CdS |
| | 48.02 | 1.895 | 0.195 | 46.7 | (103) | Hex CdS |
| $CdCl_2$ treated | 25.07 | 3.553 | 0.260 | 32.7 | (100) | Hex CdS |
| | 26.80 | 3.326 | 0.130 | 65.7 | (002) | Hex CdS/FTO |
| | 28.45 | 3.137 | 0.130 | 65.9 | (101) | Hex CdS |
| | 48.17 | 1.889 | 0.162 | 56.0 | (103) | Hex CdS |

### 3.2.2 Raman Study

Fig. 6 shows typical Raman spectra for ~500 nm thick layers of both as-deposited and the $CdCl_2$ treated samples of CdS. In this spectra, strong scattering due to the longitudinal optical (LO) vibration mode were observed for both the as-deposited and $CdCl_2$ treated layers. For the as-deposited CdS layer, the dominating 1LO peak was observed at ~303 $cm^{-1}$ while a broad 2LO peak was observed at ~604 $cm^{-1}$. The 1LO and 2LO peaks for the $CdCl_2$ treated samples were observed at ~300 $cm^{-1}$ and 602 $cm^{-1}$ respectively. The slight red shift observed in the 1LO and 2LO peak positions after heat treatment at 400˚C for 20 minutes in the presence of $CdCl_2$ in air is logged in Table 2. This shift can be attributed to internal dislocation and extrinsic defect in CdS layer [7]. Furthermore, the obtained FWHM from the Raman spectra shows a reduction in its value after $CdCl_2$ treatment which is an indication of an improvement in the crystallinity and increased grain size of the treated layer. This analytical trend is consistent with that observed from the XRD analysis.

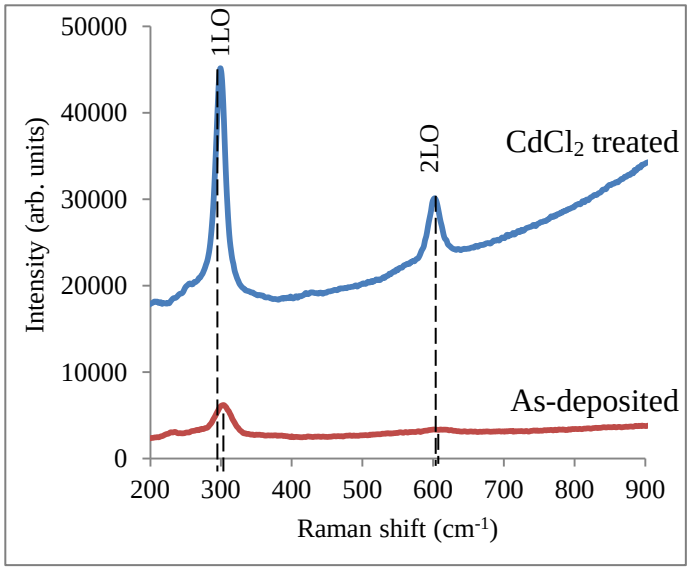


*Fig. 6: Raman spectra of as-deposited and $CdCl_2$ treated CdS thin films grown at 791 mV.*

*Table 2: Raman Analysis of As-deposited and $CdCl_2$ Treated CdS layers.*

| | As-deposited CdS | | $CdCl_2$ Treated CdS | |
|---|---|---|---|---|
| | 1LO | 2LO | 1LO | 2LO |
| Raman peak position ($cm^{-1}$) | 303.15 | 604.36 | 299.25 | 601.79 |
| Intensity (arb. units) | 3645.7 | 390.6 | 26017.0 | 7504.7 |
| FWHM | 28.73 | 51.44 | 16.28 | 20.71 |

### 3.3 Thickness measurements

The thickness measurement of layers grown between (787-793) mV was carried out both theoretically and experimentally. Theoretical measurement was estimated using Faraday's law of electrolysis as shown in equation *(3)*.

$$T = \frac{JtM}{nF\rho} \qquad (3)$$

Where $T$ is the film thickness, $J$ is the average deposition current density, $t$ is the deposition time, M is the molar mass of CdS, $F$=96485 C $mol^{-1}$ is the Faraday constant, $\rho$ is the density of CdS and $n$ is the number of electrons transferred for deposition of 1 molecule of CdS ($n$ = 2 for CdS). The experimental thickness measurement was carried out using UBM Microfocous optical depth profilometer (UBM, Messetecknik GmbH, Ettlingen, Germany). It was observed in Fig. 7(a) that the value of the measured thickness was lower than the calculated thickness using Faraday's law of electrolysis. This can be attributed to the assumptions made in Faraday's law of electrolysis that all the electronic charges contribute to the deposition of CdS without any consideration of the electronic charges involved in the decomposition of water into its constituent ions. It was also observed that the growth current density increases with an increase in growth voltage and therefore results into increased film thickness and also changes were observed in the coloration of the deposited film. It is worth noting that for these experiments, all the CdS layers were grown for the same time duration and heat treated under the same condition. As shown in Fig. 7(a), after heat treatment at 400˚C for 20 minutes in the presence of $CdCl_2$, the thickness of the samples grown at 787 and 788 mV show a slight reduction in thickness which might be a result of the loss of sulphur from the S-rich CdS layers. While the thickness of the samples grown between (789 and 792) mV remained virtually unchanged which might be attributed to stoichiometric or near-stoichiometric nature of the grown layer within this range. The layer grown above 791 mV shows a sharp reduction in thickness as a result of the sublimation of cadmium from the Cd-rich CdS layer.

This information shows that stoichiometric CdS can withstand the heat treatment but either S-rich CdS or Cd-rich CdS layers easily breakdown and sublime under the same conditions. Further experimentations were performed to determine the effect of heat treatment duration in the presence $CdCl_2$ as shown in Fig 7(b). A reduction in thickness due to sublimation of CdS layer was observed after 20 minutes and a sharp reduction after 25 minutes heat treatment duration. Based on this result, heat treatment of CdS in the presence of $CdCl_2$ above 20 minutes results into layer deterioration and sublimation of the CdS layer and might result into pin-hole formation.

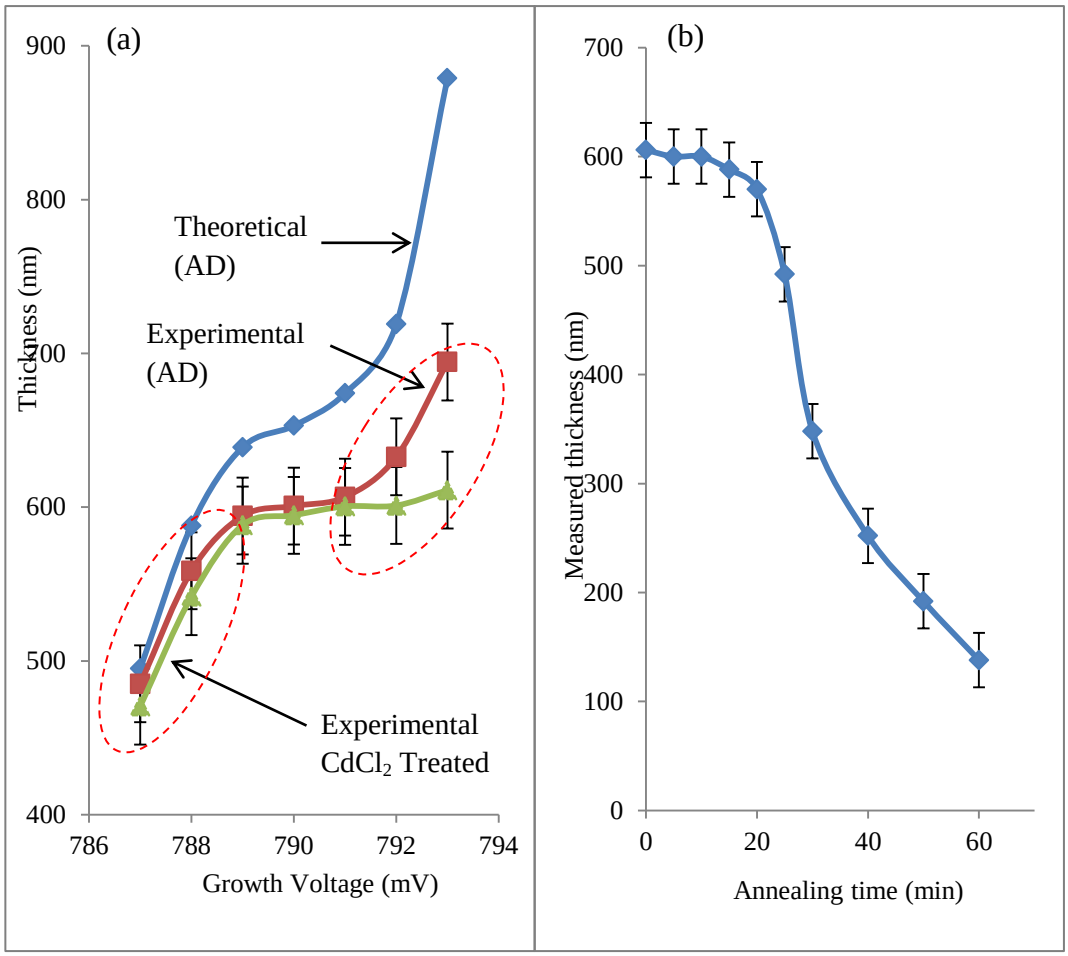


*Fig.7: (a) Graph of CdS layer thickness (theoretical and experimental) against growth voltages for both as-deposited and $CdCl_2$ treated CdS layers and (b) graph of measured CdS layer thickness against different annealing duration in air at 400˚C in the presence of $CdCl_2$.*

### 3.4 Optical Properties

The optical absorbance measurements were carried out on samples grown between (787 and 793) mV for both the as-deposited and the $CdCl_2$ treated samples so as to determine the energy bandgap of each CdS layer and its conformity with the energy bandgap of the bulk CdS. The spectra of optical absorbance for the CdS thin films grown at different voltages for as-deposited and $CdCl_2$ treated samples are shown in Fig. 8(a) and (b). The square of absorbance ($A^2$) was plotted against the energy of photons and the extrapolated straight-line section of the graph to the energy of photons axis (at $A^2=0$) gives an estimate of the bandgap energy. As observed, the as-deposited CdS layers grown within the explored growth voltage range shows bandgap ranging between 2.41±0.03 eV as shown in Fig. 8(a) and Table 3. While the $CdCl_2$ treated samples grown within the same growth voltage range shows a bandgap range between 2.41±0.01 eV. This slight reduction in the bandgap range after $CdCl_2$ treatment might be attributed to pin-hole removal, re-crystallization of the lattice structure and improvement in material composition. Notably, the growth voltages surrounding 791 mV shows comparatively sharp difference in bandgap. This might be due to the insulative property of sulphur due to its richness as observed at low $V_g$ and the metallic behaviour of cadmium due to its richness at high $V_g$. It was interesting to see that the layer grown at 791 mV shows 2.42 eV bandgap which is comparable with the standard bandgap for bulk CdS. Also in Table 3 it was observed that the growth voltages outside the predetermined/explored range show bandgap values which were not close to the bulk-CdS value of 2.42 eV. This

might be attributed to the richness of sulphur or cadmium in the grown CdS layers. Fig. 9 shows the transmittance of the explored growth voltage range after heat treatment at 400˚C for 20 minutes in the presence of $CdCl_2$. It is worth mentioning that all the samples show transmittance above 60% for wavelength larger than 512 nm.

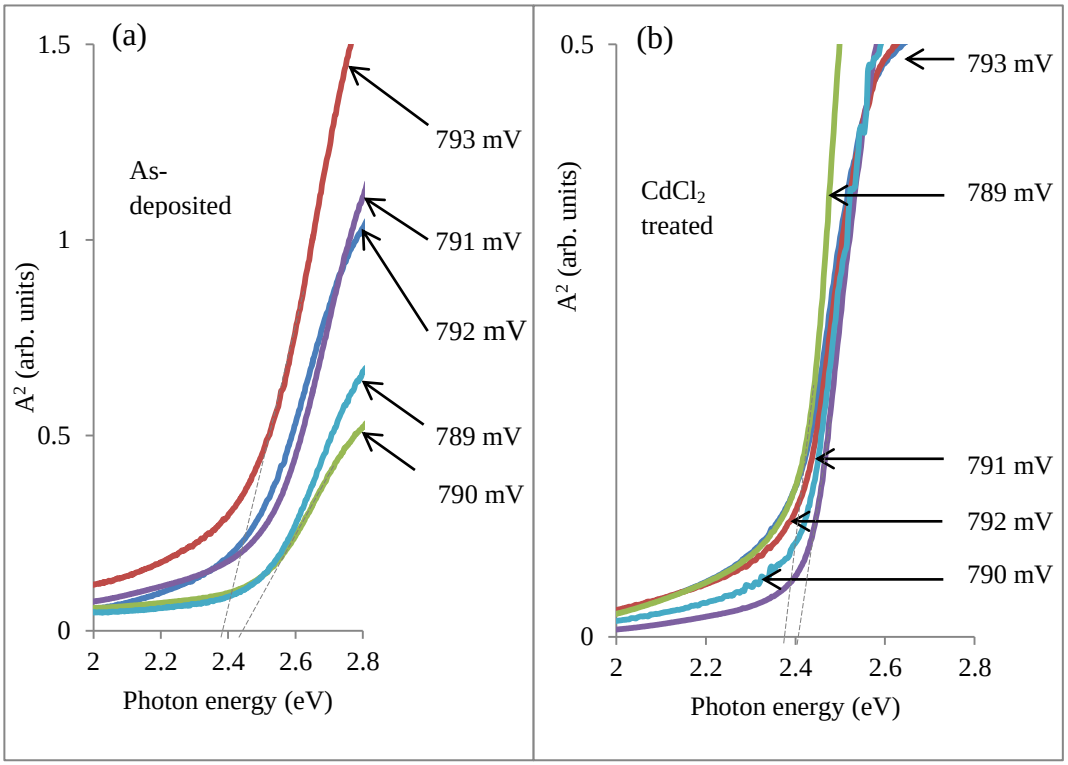


*Fig. 8: Optical absorption spectra for electrodeposited CdS thin-films between voltage range 789 to 793 mV for (a) as-deposited, and (b) $CdCl_2$ treated CdS at 400˚C for 20 minutes in air.*

*Table 3: The optical bandgap and transmittance of CdS layers grown at cathodic potentials between 789 mV and 793 mV for the as-deposited and the $CdCl_2$ treated layers at 400˚C for 20 minutes in air.*

| Growth voltage (mV) | 789 | 790 | 791 | 792 | 793 |
|---|---|---|---|---|---|
| Band gap for as-deposited CdS (eV) | 2.45 | 2.44 | 2.42 | 2.42 | 2.39 |
| Band gap $CdCl_2$ treated CdS (eV) | 2.41 | 2.41 | 2.42 | 2.41 | 2.40 |
| Transmittance for AD-CdS (%) | 58 | 57 | 47 | 47 | 43 |
| Transmittance for $CdCl_2$ treated CdS (%) | 79 | 76 | 76 | 63 | 61 |

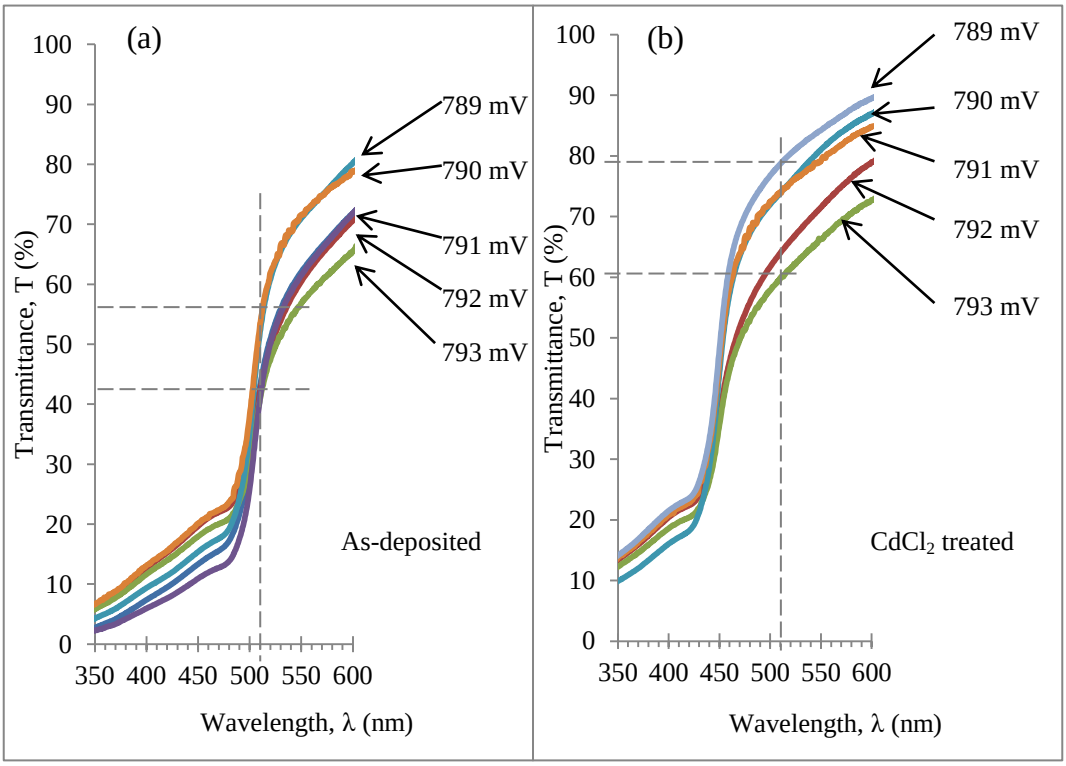


*Fig. 9: Optical transmittance spectra for electrodeposited CdS thin-films between voltage range 789 to 793 mV for (a) as-deposited, and (b) $CdCl_2$ treated at 400˚C for 20 minutes in air.*

Further experimentations on the effect of film thickness and the effect of heat treatment duration at 400˚C in the presence of $CdCl_2$ on the optical properties of CdS layers were explored in this work. The effect of film thickness on the absorbance and transmittance can be clearly seen in Fig. 10(a). It was observed that the increase in thickness of $CdCl_2$ treated layer above 380 nm resulted into a reduction in bandgap from 2.42 eV to 2.41 eV. Accordingly, reduction in the transmittance below 60% was also observed for samples with thicknesses above 330 nm. Therefore, CdS layer with thickness lower than 330 nm will be appropriate to justify one of the properties of window layer. It is important to note that thinner CdS layers can suffer from discontinuities and defects such as pinholes [8], therefore, an optimum thickness must be determined to avoid pin-holes and to achieve high optical transmittance. The observed high bandgap at thicknesses lower than 152 nm might be due to the porosity and/or pin-holes due to incomplete coverage while the low bandgap at thicknesses above 380 nm might be due the complete coverage of the underlying substrate. It might also be due to the acidic attack on cadmium from the electrolyte due to prolonged growth duration.

The experimentation on the effect of heat treatment duration on CdS at 400˚C in the presence of $CdCl_2$ in air as shown in Fig. 10(b) was performed on ~300 nm thick as-deposited CdS layers. A gradual increase in transmittance was observed with increasing $CdCl_2$ treatment duration. It should be noted that the change in transmittance between 15 minutes and 25

minutes treatment duration is comparatively minimal with a transmittance difference of ~65%±2% as compared to others. Correspondingly, a similar trend was observed with bandgap energy of the CdS layers as shown in Fig. 10(b). The initial increase in both transmittance and bandgap energy between (0 and 10) minutes can be attributed to the improvement in CdS properties either by sublimation of excess elements (Cd and/or S), increase in CdS crystallinity and grain growth. The CdS layers $CdCl_2$ treated between (15 and 25) minutes can be said to be highly crystalline CdS layer with full coverage of underlying FTO substrate. Evidence of these can be seen in the bandgap which equals the bulk CdS bandgap of 2.42 eV. These properties are required to produce high efficient solar cell devices. The increase in both the transmittance and bandgap energy observed for CdS layers $CdCl_2$ treated for durations above 25 minutes can be attributed to severe loss of CdS layers and the formation of pin-holes. This observation is in accord with the thickness measurement discussed in Section 3.3.

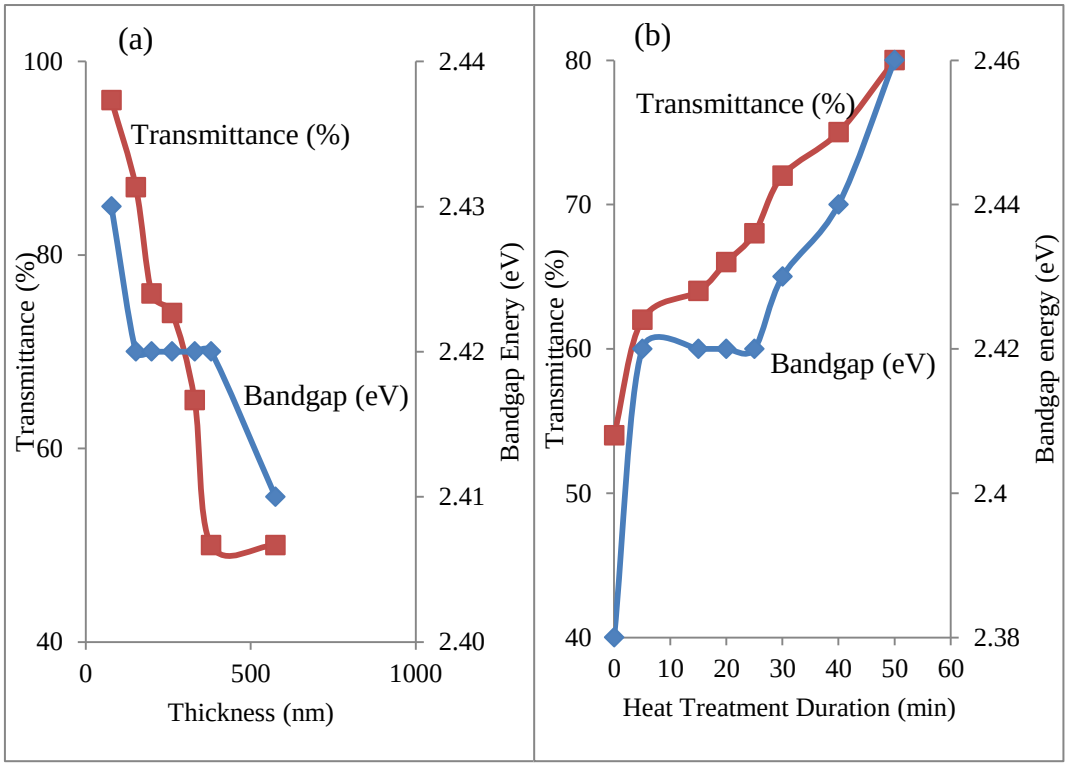


*Fig. 10: (a) The effect of CdS film thickness on optical bandgap and transmittance spectra for $CdCl_2$ treated CdS thin-films at 400˚C for 20 minutes in air, and (b) The effect of heat treatment duration on CdS thin-film grown at 791 mV and heat treated at different durations at 400˚C in the presence of $CdCl_2$.*

## 3.5 Morphological and Compositional Analysis

### 3.5.1 SEM Study

Fig. 11 shows the SEM micrograph images of (a) as-deposited and $CdCl_2$ treated CdS at 400˚C for the duration of (b) 10 minutes, (c) 20 minutes (d) 30 minutes (g) 40 minutes and

(h) 50 minutes respectively. Topologically, the surface of the FTO/CdS substrate shows full coverage with CdS nanoparticles for the as-deposited and heated samples for 10, 20 and 30 minute durations. It was also notable that the coalescence of grains and increase in grain sizes was slightly observable after 10 minutes heat treatment duration, (150-200) nm. A further increase in grain size to (300-550) nm was observed with an increase in the heat treatment duration. This microstructural change of the surface morphology as a result of heat treatment can be attributed to re-crystallisation and the partial transformation of the mixed cubic/hexagonal phases into single hexagonal phase after heat treatment [9] as observed from XRD. Gaps along the grain boundaries were observed for samples heat treated for 30 minutes and above which can be attributed to the sublimation of the CdS layer and due to a build-up of larger CdS nanoparticles from the coalescence/growth of CdS crystallites [10] in the vertical direction. These observations are in accord with the thickness measurement in Fig 7(b) and the optical absorption Fig 10(b).

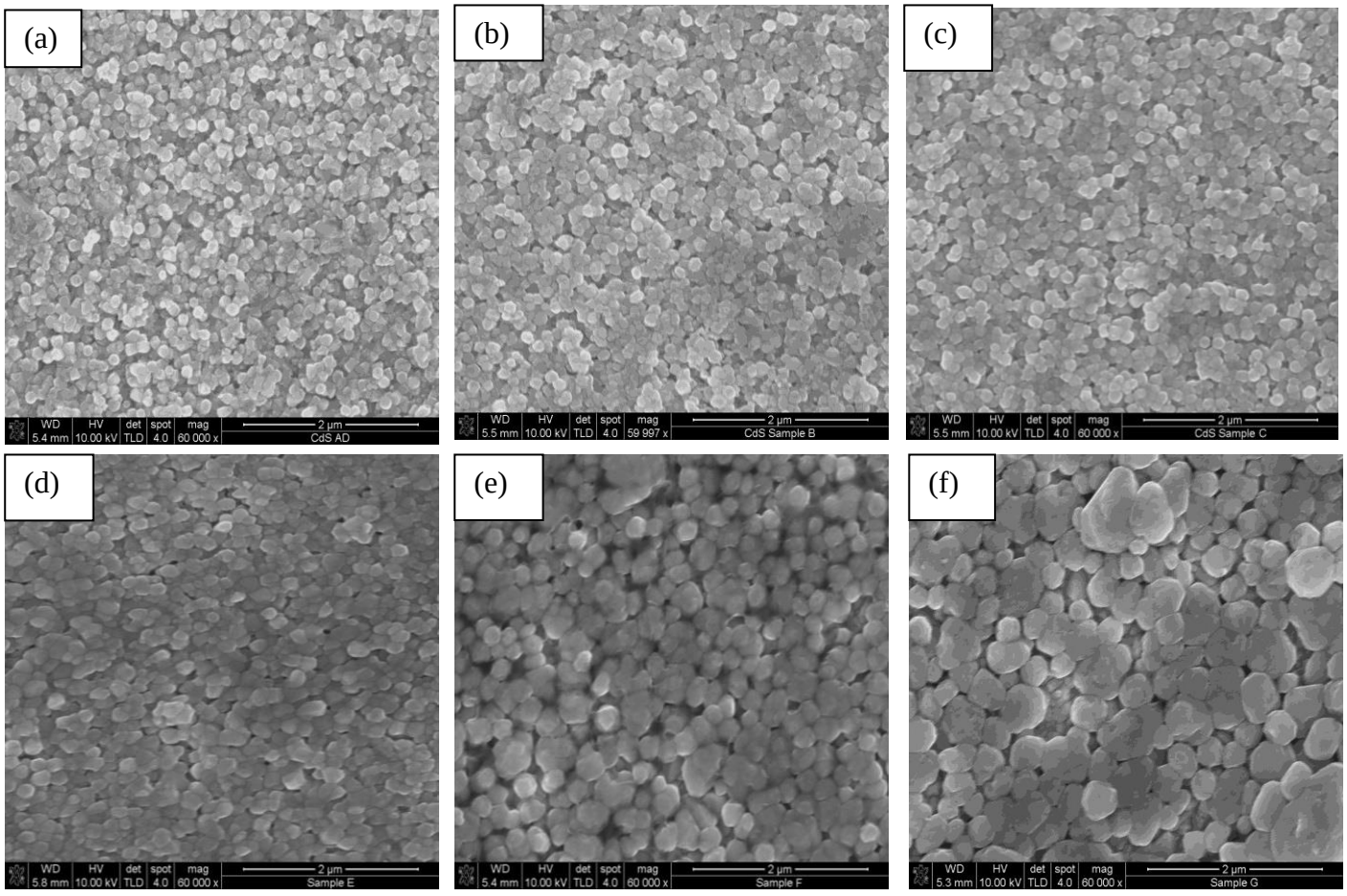


*Fig. 11: SEM micrograph images of (a) as-deposited and $CdCl_2$ treated CdS at 400˚C for the duration of (b) 10 (c) 20 (d) 30 (e) 40 and (f) 50 minutes respectively.*

### 3.5.2 Compositional Analysis

EDX measurements were performed to determine the atomic composition of Cd and S for both the as-deposited and $CdCl_2$ treated CdS films. Seven samples were grown at different cathodic voltages within the range of 788 to 794 mV at 1 mV step and used for the analysis. Fig 12 summarises the atomic ratio of Cd to S in CdS layers grown at different growth potentials as observed in EDX. The presence of other elements such as Sn and Cl were also observed. This is due to the underlying glass/FTO layer and the presence of chlorine in the CdS deposition bath and the $CdCl_2$ treatment as described in Section 2.1. As illustrated in Fig. 12, S-rich CdS was observed at 788 mV with an atomic ratio of Cd/S less than 1.0 which confirms the S-richness of CdS. A gradual increase in Cd content incorporated into CdS layer was observed with increasing growth voltage. Stoichiometric CdS was observed at 791 mV for both the as deposited and the $CdCl_2$ treated layers with the Cd/S atomic ratio equal to 1.01. It was interesting to observe that after $CdCl_2$ treatment, both the S-rich and the Cd-rich CdS tends toward stoichiometry. This observation further shows that $CdCl_2$ treatment improves CdS layer properties by reaction between unreacted Cd and S, and the sublimation of elemental Cd and S from the layer. The results obtained in this section is in agreement with the visual, structural and optical observations earlier discussed

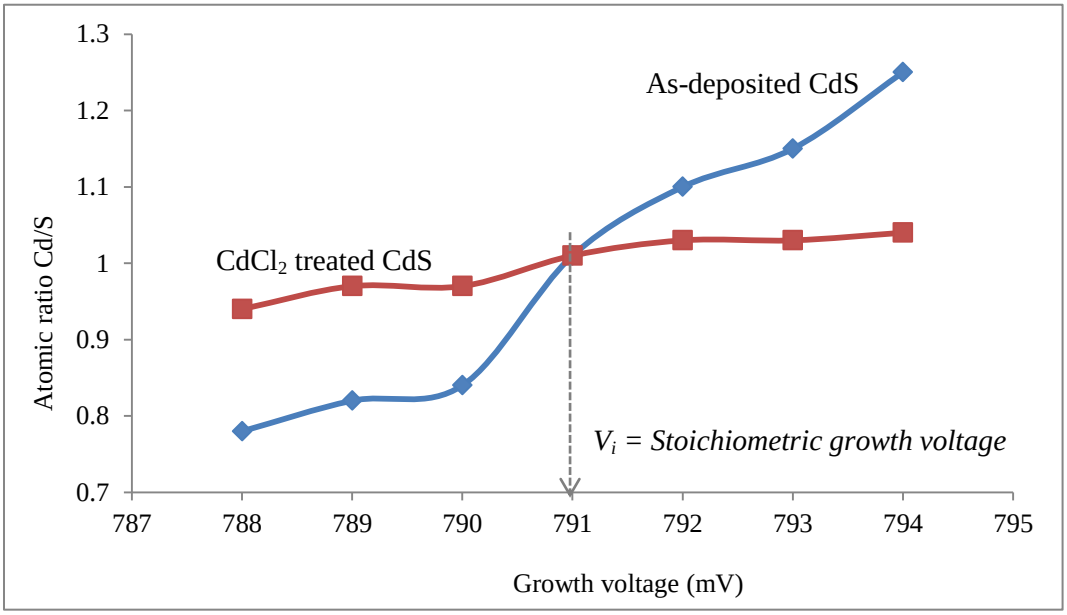


*Fig. 12: Graphical representation of percentage compositions ratio of Cd to S atoms in as-deposited and $CdCl_2$ treated CdS thin films at different deposition cathodic voltages.*

## 3.6 Electrical properties

### 3.6.1 Photoelectrochemical (PEC) Cell Measurement

As observed in Fig. 13, both the as-deposited and the $CdCl_2$ treated layers were all n-type in electrical conductivity type. The n-type conductivity nature of CdS layers is due to the presence of Cd interstitials and S vacancies in the crystal lattice of the deposited CdS layers. The Cd interstitials and S vacancies has been reported as an intrinsic donor defects in CdS layers [11], [12]. The magnitudes of the PEC signal in the $CdCl_2$ treated layers were higher than in the as-deposited layers. This might be as a result of the improvement of the depletion

layer at the CdS/electrolyte junction due to the enhancement of the electronic quality of the CdS layer.

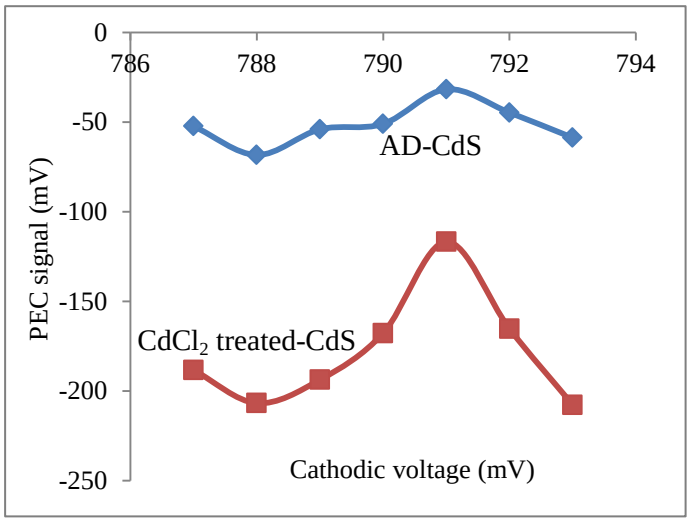


*Fig. 13: PEC signals for layers grown at different cathodic voltages, showing n-type electrical conductivity type for all samples investigated within explored conditions.*

### 3.6.2 Current – Voltage Characteristics with Ohmic contacts

The DC conductivity measurements were carried out on the electrodeposited CdS layers to determine the electrical conductivity (σ) and resistivity (ρ) of the layers. This experiment was performed to determine both the effect of film thickness and the heat treatment duration on the electrical properties of CdS layers. 2 mm diameter and 60 nm thick In contacts were evaporated onto CdS layers to give ohmic behaviour. The electrical resistance (R) of the glass/FTO/CdS/In structure was calculated from the ohmic I-V data under dark condition using Rera Solution PV simulation system. Using equation (4), which incorporates resistance R, contact area A and film thickness L, the resistivity (ρ) was calculated

$$\rho = \frac{RA}{L} \qquad (4)$$

The summary of the electrical resistivity and conductivity as a function of CdS layer thickness is tabulated in Table 4. To determine the effect of heat treatment duration on the electrical properties, 310 nm thick CdS was deposited on a (3×8) $cm^2$ FTO substrate and treated with $CdCl_2$ after growth. The substrate was cut into (3×1) $cm^2$ pieces before heat treating each substrate at 400°C for different time durations. As observed in Fig. 14(a), an initial stagnation of the resistivity of the CdS layer was observed for 5 and 10 minutes heat treatment duration which suggests that the latent heat required in melting grain boundaries, activate grain growth and forming crystalline mono-phased CdS have not been surpassed due to the gradual temperature increase of the substrate and treatment time duration. The increase in the conductivity of CdS for samples heat treated for 20 minutes can be attributed to growth in grain size, reduction of grain boundaries and increased crystallinity of the CdS layer. While the samples heat treated above 20 minutes duration shows a gradual decrease in conductivity which might be due to the deterioration of the CdS layer caused by sublimation of elements [3]. This decrease in electrical conductivity could also be due to compensation taking place by diffusion of p-dopant such as Na from glass substrate during prolonged heat treatment. This observation is in accordance with the structural, morphological, and optical properties discussed above. This shows that the optimum heat treatment at 400˚C is for ~20 minutes to achieve the highest electrical conductivity.

*Table 4: Summary of electrical properties of CdS layers after heat treatment durations at 400˚C in the presence of $CdCl_2$ in air.*

| Heat treatment duration at 400°C (min) | Measured Thickness (nm) | Avg. Resistance (Ω) | Avg. Resistivity $\times 10^4$ (Ω.cm) | Avg. Conductivity $x10^{-5}$ $(\Omega.cm)^{-1}$ |
|---|---|---|---|---|
| 5 | 302 | 28.4 | 2.97 | 3.39 |
| 10 | 300 | 28.3 | 2.97 | 3.39 |
| 20 | 285 | 20.2 | 2.23 | 4.51 |
| 25 | 246 | 22.8 | 2.91 | 3.48 |
| 30 | 174 | 24.8 | 4.47 | 2.32 |
| 40 | 126 | 20.6 | 5.13 | 2.09 |
| 50 | 96 | 20.4 | 6.67 | 1.57 |
| 60 | 69 | 20.8 | 9.46 | 1.09 |

*Table 5: The effect of layer thickness on the electrical conductivity of $CdCl_2$ treated CdS layers.*

| Thickness (nm) | Resistance (Ω) | Avg. Resistivity $\times 10^4$ (Ω.cm) | Avg. Conductivity $x\ 10^{-5}$ $(\Omega.cm)^{-1}$ |
|---|---|---|---|
| 79 | 15.4 | 6.11 | 1.73 |
| 159 | 15.4 | 3.94 | 2.56 |
| 223 | 25.5 | 3.58 | 2.79 |
| 292 | 18.7 | 2.01 | 5.23 |
| 397 | 23.5 | 1.86 | 5.42 |
| 528 | 30.0 | 1.79 | 5.73 |

Further experimentation on the effect of thickness on the electrical conductivity of CdS layers which had been post-growth treated with $CdCl_2$ at 400°C for 20 minutes shows that an increase in film thickness results into an increase in the conductivity as shown in Table 5 and Fig. 14(b). This can be attributed to the formation of large grains, reduction of voids/pin-holes, increase in S vacancy and/or Cd interstitials which serves as n-type intrinsic dopant of CdS [12].

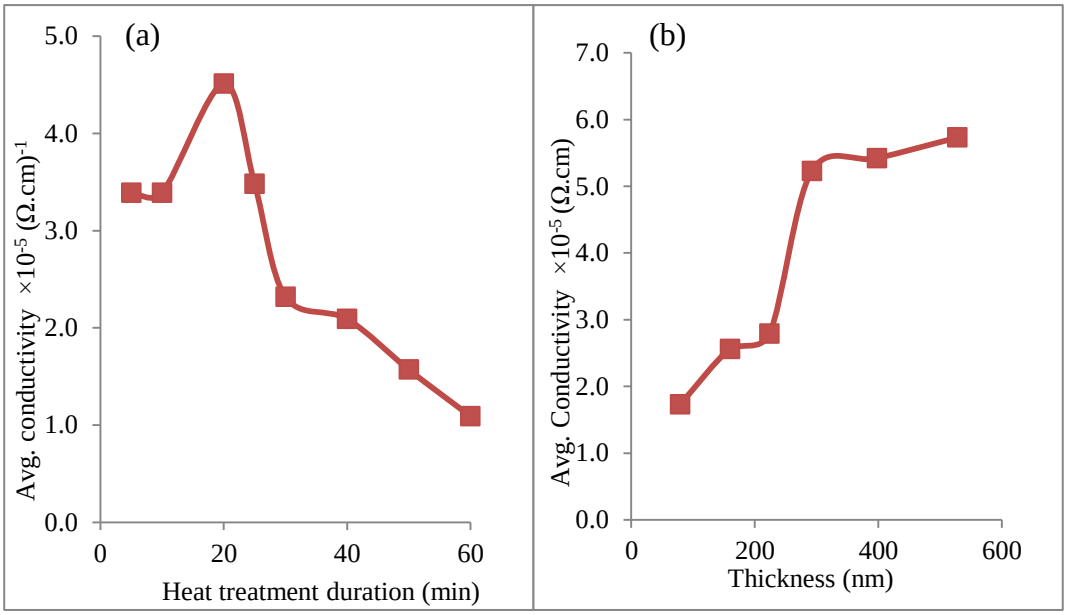


*Fig. 14: (a) The effect of heat treatment duration on CdS thin films grown at 791 mV and heat treated at different durations at 400˚C in the presence of $CdCl_2$. (b) The effect of CdS film thickness on electrical conductivity for $CdCl_2$ treated CdS thin-films at 400˚C for 20 minutes in air.*

### 3.6.3 Current – Voltage Characteristics with Rectifying contacts

The current–voltage (I–V) characteristics for rectifying contacts have been broadly used to study Schottky diodes and to determine some important device and material parameters. For these experiments, the thicknesses of CdS films were varied to determine the effect of thickness on the characteristic behaviour of glass/FTO/CdS/Au Schottky diodes. The I-V characteristics were measured in dark condition at a bias voltage range of (-1.00 to 1.00) V. The I-V characteristics of a Schottky diode under dark condition can be expressed using equation (5) [13].

$$I_D = SA^*T^2.\exp\left(\frac{-e\phi_b}{kT}\right)\left[\exp\left(\frac{eV}{nkT}\right)-1\right] \quad (5)$$

since $$I_0 = SA^*T^2.\exp\left(\frac{-e\phi_b}{kT}\right) \quad (6)$$

equation (5) can be rewritten as

$$I_D = I_0\left[\exp\left(\frac{eV}{nkT}\right)-1\right] \quad (7)$$

where $I_0$ is the saturation current, $S$ is the area of the contact, $A^*$ is the effective Richardson constant for thermionic emission, $T$ is the temperature, $e$ is the electronic charge, $\phi_b$ is the

potential barrier height, *k* is the Boltzmann constant and *n* is the ideality factor of the diode. As reported by Rhoderick and Williams 1982 [13], if the applied voltage across the diode exceeds 75 mV, then

$$\exp\left(\frac{eV}{nkT}\right) \rangle\rangle 1 \tag{8}$$

equation (7) can be rewritten as

$$I_D = I_0 . \exp\left(\frac{eV}{nkT}\right) \tag{9}$$

or

$$\log_{10}(I_D) = \left(\frac{e}{2.303nkT}\right) . V + \log_{10}(I_0) \tag{10}$$

Therefore, from the plot of $\log_{10}(I_D)$ versus voltage applied (*V*), the saturated current and the ideality factor can be obtained. The intercept on the current axis gives the saturation current $I_o$ while the slope in the forward bias gives the value through which the ideality factor *n* was calculated using equation (10). This was obtained with the consideration of largest gradient of the curve that gives the lowest value of *n* [13]. The rectification factor *RF* which helps in determining the quality of a rectifying diode can be calculated as the ratio of forward current to reverse current at a constant voltage as estimated from the $\log_{10}(I_D)$ versus voltage (*V*) plot. The barrier height $\phi_b$ was calculated using equation (6) and the effective Richardson constant for CdS layer was calculated to be 25.24 $Acm^{-2}K^{-2}$ using equation (11).

$$A^* = \frac{4\pi m_e^* k^2 q}{h^3} \tag{11}$$

where $m_e^* = 0.21 m_o$ is the effective electron mass of n-CdS, $m_o = 9.1 \times 10^{-31}$ kg is the free electron mass and $h = 6.626 \times 10^{-30}$ $cm^2kgs^{-1}$ is the Planck's constant. The series resistance $R_s$ and shunt resistance $R_{sh}$ were calculated from the slopes of linear-linear I-V curve in the forward and reverse bias respectively as shown in Table 6. Fig 12(b) shows the typical I-V curves of g/FTO/CdS/Au diodes observed with electroplated CdS layers. It was observed that across all thicknesses in this experiment, the cells show infinite (∞) $R_{sh}$ and $R_s \leq 0.1$ Ω which is close to that of an ideal diode with $R_{sh}$ and $R_s$ equals infinity (∞) and zero (0) respectively. The observed ideality factor was in the range of (1.69-1.81) with a gradual increase in value with an increase in thickness as shown in Table 6. This shows that the current transport mechanisms in the depletion region of the M-S (metal-semiconductor) structure consist of both thermionic emission and recombination and generation (R&G) processes. Other factors such as the increase in $R_s$ and tunnelling through the diode could have increased the ideality factor *n* [2] but in this experiment the $R_s$ was 0.1 Ω. Further observations on the effect of thickness on CdS layer shows that thickness has no significant influence on the barrier height $\phi_b$. The fabricated CdS diodes show an RF value of ~$10^4$ across all thicknesses. This indicates that the CdS layers are suitable for application in electronic devices. Additional experimentations on the effect of heat treatment duration on CdS layers as depicted in Fig. 15(c) shows an optimal value for both $\phi_b$ and *n* at 20 minutes heat treatment duration. This observation can be attributed to better material quality, high crystallinity, and minimisation of defect distribution. Material deterioration was observed at higher heat treatment duration as the *n* value tends towards 2.00, which show the presence of higher R&G centres.

*Table 6: The summary of observed parameters obtained from current-voltage (I-V) characteristics for CdS/Au Schottky diodes at different thicknesses.*

| Thickness (nm) | Series Resistance $R_s$ (Ω) | Shunt Resistance $R_{sh}$ (MΩ) | Rectification factor RF | Avg. Reverse saturation current $I_o \times 10^{-7}$ (A) | Range of Ideality factor n | Avg. Barrier Height $\Phi_b$ (eV) |
|---|---|---|---|---|---|---|
| 79.0 | 0.089 | 0.96 | $10^{4.2}$ | 3.46 | 1.68 -1.72 | > 0.67 |
| 159.6 | 0.075 | 1.10 | $10^{4.2}$ | 3.04 | 1.70 - 1.72 | > 0.67 |
| 223.7 | 0.075 | 1.13 | $10^{4.1}$ | 4.02 | 1.70 - 1.75 | > 0.67 |
| 292.4 | 0.075 | 1.18 | $10^{4.0}$ | 4.66 | 1.72 - 1.78 | > 0.66 |
| 397.5 | 0.084 | 1.25 | $10^{4.2}$ | 4.71 | 1.76 - 1.82 | > 0.66 |
| 528.0 | 0.094 | 1.27 | $10^{4.1}$ | 5.17 | 1.80 - 1.83 | > 0.66 |

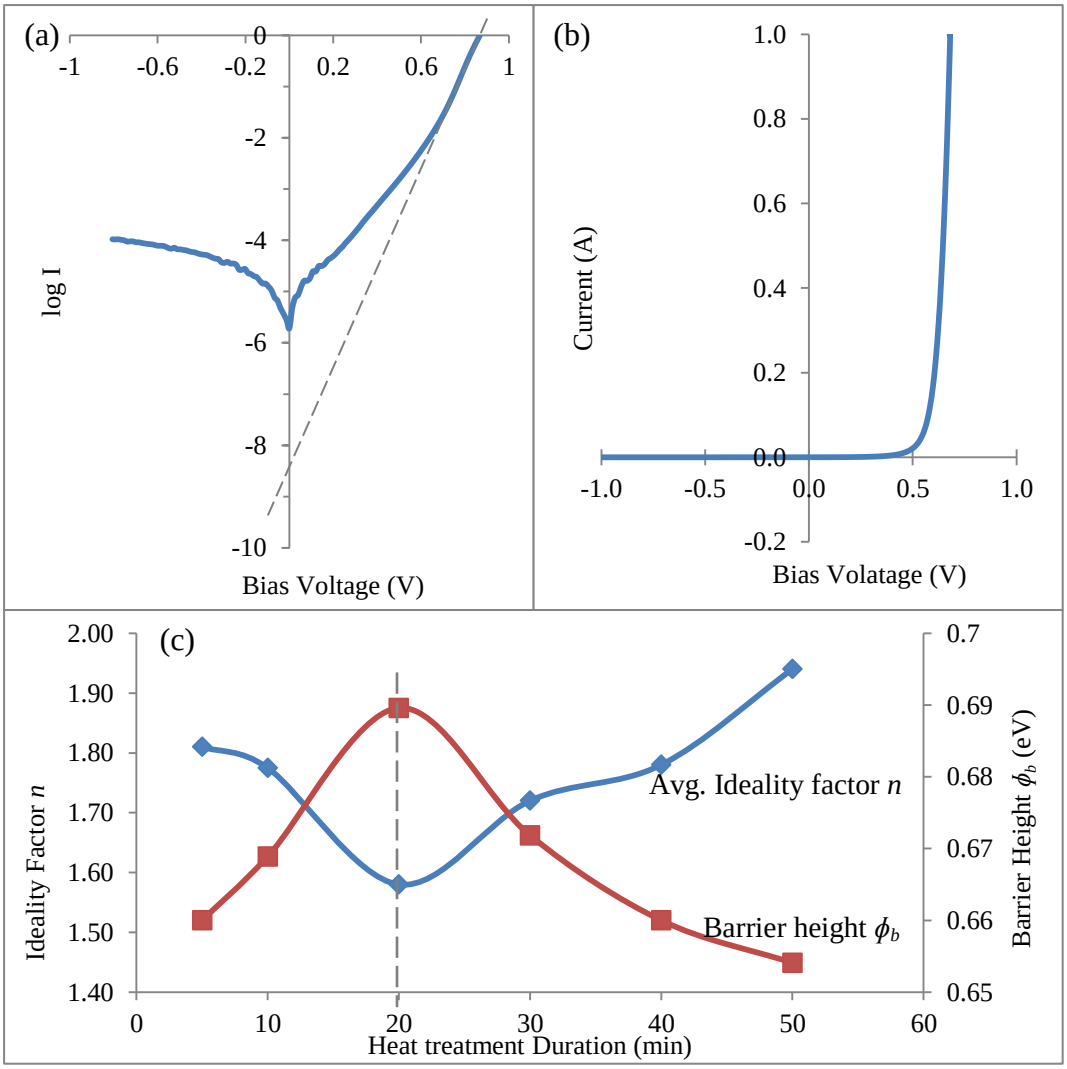


*Fig. 15: (a) A typical semi-logarithmic current vs. voltage curve measured under dark condition for Au Schottky contacts made on heat treated CdS (b) linear-linear I-V curve of Au Schottky contacts made on heat treated CdS layers and (c) The effect of heat treatment duration at 400˚C on ideality factor and potential barrier height for Au Schottky contacts under dark condition.*

### 3.6.4 Capacitance – Voltage characteristics of rectifying contacts

The capacitance-voltage (C-V) technique was performed to determine important device and material characteristics such as position of Fermi level ($E_F$), built-in potential ($V_{bi}$), doping concentration of the material ($N_D$-$N_A$), barrier height $\Phi_b$, charge carrier mobility ($\mu_\perp$) and depletion layer width at zero bias of glass/FTO/CdS/Au Schottky diodes fabricated on varied CdS layer thickness. Due to the underlying conducting substrate (FTO), Hall Effect measurement is unsuitable for the acquisition of electrical parameters required. Therefore, an indirect method of combining I-V and C-V measurements were used to estimate the materials parameters such as doping concentration and mobility. All the samples used in this experiment were $CdCl_2$ treated at 400°C for 20 minutes. The C-V measurements were performed in dark condition at a bias voltage range of (-1.00 to 1.00) V with 1 MHz AC signal at 300 K. The built-in potential ($V_{bi}$) and donor concentration ($N_D$-$N_A$) in this configuration can be determined using the Mott-Schottky plot as shown in Fig. 16 and equation (12) and (13).

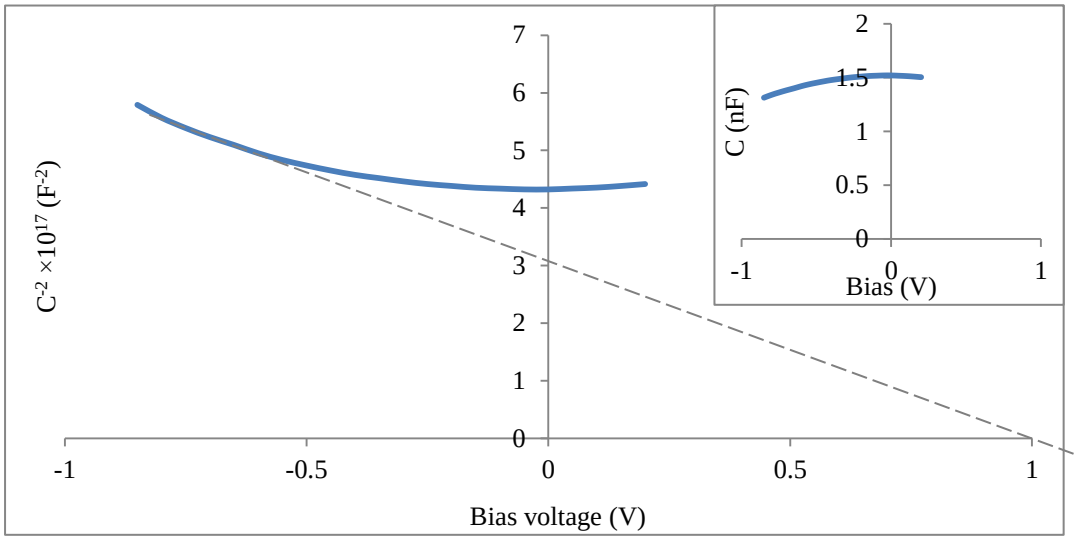


*Fig. 16: A typical Schottky–Mott plot for Schottky contacts made on electroplated CdS layer. Inset shows the variation of capacitance as a function of DC bias voltage.*

$$\frac{1}{C^2} = \frac{2}{\varepsilon_s e A^2 (N_D - N_A)}(V_R + V_{bi}) \quad (12)$$

$$N_d = \frac{2}{\varepsilon_r \varepsilon_0 e A^2 * slope} \quad (13)$$

$$Slope = C^{-2}(V_R - V_{bi})^{-1} = \frac{2}{\varepsilon_s e(N_D - N_A)} \quad (14)$$

where $C$ is the capacitance, $\varepsilon_s$ is the semiconductor permittivity, $\varepsilon_r$ is the relative dielectric constant, $\varepsilon_o$ is the permittivity of free space, $e$ is the electronic charge, $A$ is the area of the contact, ($N_D$-$N_A$) is the donor concentration, $V_R$ is the reverse bias voltage and $V_{bi}$ is the built-in potential. The slope of the $C^{-2}$ versus $V$ plot is given by equation (14) [13]. The $V_{bi}$ can be estimated as the tangential intersection on V-axis in $C^{-2}$ versus V plot. The effective density of state $N_c$ of CdS was calculated to be 2.42 ×$10^{18}$ $cm^{-3}$ using equation (15), where, $k$ is the Boltzmann's constant, $m_e^*$ is the effective electron mass, $T$ is the temperature, and $h$ is the Plank constant.

$$N_C = 2\left[\frac{2\Pi m_e^* kT}{h^2}\right]^{\frac{3}{2}} \quad (15)$$

The Fermi level $E_F$, charge carrier mobility $\mu_\perp$ and the barrier height $\Phi_b$ were calculated using equation (16), (17) and (18) respectively *(with all parameters predefined)*.

$$E_F = \frac{kT}{e}\ln\left[\frac{N_C}{N_D - N_A}\right] \quad (16)$$

$$\mu_\perp = \frac{\sigma}{ne} = \frac{\sigma}{(N_D - N_A)e} \quad (17)$$

It has been assumed that all excess donor atoms ($N_D$) are ionised at room temperature, therefore $n \approx (N_D - N_A)$ as shown in equation (17). The $\mu_\perp$ is the mobility of electrons in the direction perpendicular to FTO surface. It should be noted that $\mu_\perp$ is different from the reported mobility values measure by conventional Hall Effect method. These values are $\mu_{//}$, and it represents the mobility of electrons moving parallel to the FTO layer. Due to the presence of grain boundaries, $\mu_{//}$ will be much smaller than $\mu_\perp$ for nano-crystalline CdS layers.

$$\phi_b = V_{bi} + E_F + kT \quad (18)$$

It should be noted that the calculated $\Phi_b$ values using C–V measurements are affected by the effects of defects and interfacial resistive layers producing excess capacitance and inhomogeneity of the semiconductor layer in the diode [14]. The calculated $\Phi_b$ was mainly to show the trend in this work. As observed from Table 7 and Fig. 17(a), the increase in average conductivity with respect to increase in the thickness of CdS layer can be attributed to the resultant effects on $n$ and $\mu_\perp$ for electrons. The gradual increase in $n$ values indicates that R&G centres increases with increase in thickness.

*Table 7: The summary of observed parameters obtained from Schottky–Mott plots for CdS/Au Schottky diodes at different thicknesses.*

| CdS layer thickness (nm) | Range of Ideality factor $n$ | Avg. Conductivity σ $\times 10^{-5}$ $(\Omega cm)^{-1}$ | Avg. $(N_D\text{-}N_A)$ $\times 10^{17}$ $(cm^{-3})$ | $(E_C\text{-}E_F)$ (eV) | Barrier height $\Phi_b$ (eV) | Mobility $\mu_\perp$ $\times 10^{-4}$ $(cm^2V^{-1}s^{-1})$ |
|---|---|---|---|---|---|---|
| 79.0 | 1.68 -1.72 | 1.73 | 9.03 | 0.11 | > 0.84 | 1.19 |
| 159.6 | 1.70 - 1.72 | 2.56 | 8.13 | 0.12 | > 0.86 | 1.96 |
| 223.7 | 1.70 - 1.75 | 2.79 | 7.22 | 0.14 | > 0.89 | 2.41 |
| 292.4 | 1.72 - 1.78 | 5.23 | 4.92 | 0.15 | > 0.89 | 6.63 |
| 397.5 | 1.76 - 1.82 | 5.42 | 1.30 | 0.17 | > 0.91 | 26.00 |
| 528.0 | 1.80 - 1.83 | 5.73 | 1.22 | 0.19 | > 0.92 | 29.26 |

Mobility of charge carriers (free electrons) depends on scattering due to lattice vibration, ionised and neutral impurities, native defects and grain boundaries. Table 7 summarises the variation of parameters such as $n$, $\sigma$, $N_D$ and $\mu_\perp$ for CdS layers with increasing thickness. The diode behaviour observed in Fig. 16 is typical for moderately doped semiconductors with the doping range of $(10^{15} - 10^{17})$ $cm^{-3}$ [14]. Although, there are possibilities of obtaining varying doping concentrations under different growth conditions [14], but in the case of this experimental work all growth parameters were kept constant.

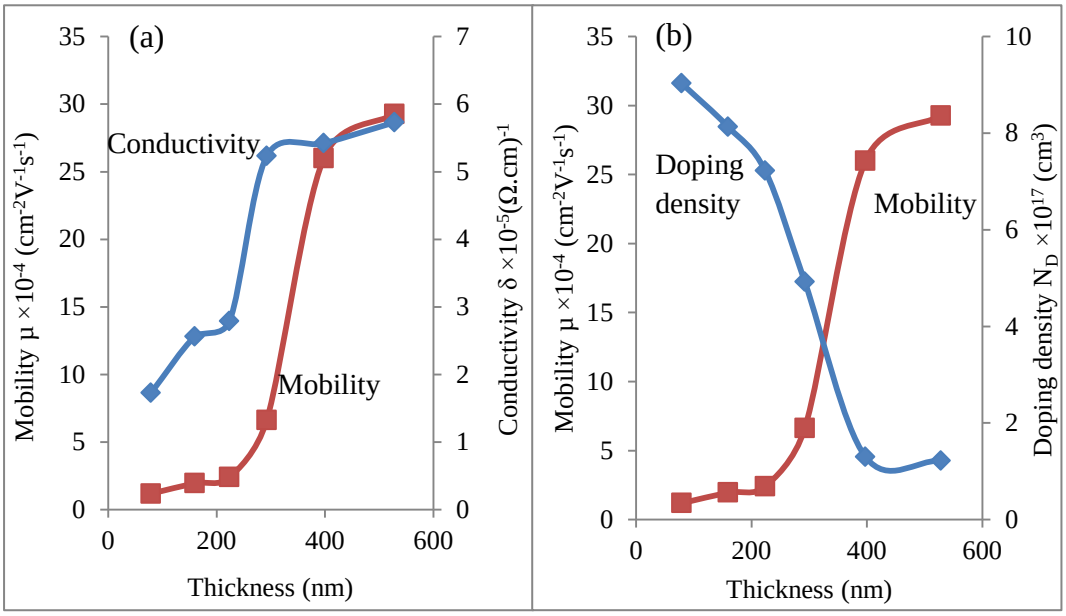


*Fig. 17: Graph of mobility and conductivity as a function of CdS layer thickness, (b) graph of mobility and doping density as a function CdS layer thickness.*

Additional experimentation was performed to determine the effect of heat treatment duration on 205 nm thick as-deposited CdS layer. The layers were subjected to post-deposition heat treatment at 400˚C at different heat treatment durations, after which glass/FTO/CdS/Au rectifying contacts were fabricated. As shown in Table 8 and Fig. 18, low carrier mobility was observed for samples heat treated for duration less than 10 minutes. This can be attributed to low CdS crystallinity and resulting high density of grain boundaries and defects as described in Section 3.6.2. While the mobility reduction for heat treatment duration above 20 minutes can also be attributed to material deterioration and increase in defects. The heat treatment at 400˚C for 20 minutes in air appears to be the optimum condition for post-deposition treatment. Under these conditions, doping concentration of ~$9.0\times10^{17}$ $cm^{-3}$, lowest $n$ ~1.65, highest barrier height of 1.01 eV and the highest mobility $\mu_{\perp}$ ~20.7 $cm^{-2}V^{-1}s^{-1}$ were achieved for these devices on CdS films.

*Table 8: The summary of observed parameters obtained from Schottky–Mott plots for CdS/Au Schottky diodes heat treated at 400˚C for different time duration.*

| HT Duration (min) | Avg. Conductivity σ $\times10^{-5}$ $(\Omega.cm)^{-1}$ | Range of Ideality factor n | Avg. ($N_D$-$N_A$) $\times10^{18}$ ($cm^{-3}$) | Fermi level $E_F$ (eV) | Barrier height $\Phi_b$ (eV) | Mobility μ $\times10^{-5}$ ($cm^2V^{-1}s^{-1}$) |
|---|---|---|---|---|---|---|
| 5 | 2.28 | 1.80 -1.82 | 5.53 | 0.15 | > 0.88 | 2.57 |
| 10 | 2.24 | 1.76 - 1.79 | 1.71 | 0.18 | > 0.91 | 8.18 |
| 20 | 2.99 | *1.62 – 1.67* | *0.90* | 0.20 | > 1.01 | 20.70 |
| 30 | 2.11 | 1.70 – 1.75 | 5.53 | 0.15 | > 0.88 | 2.38 |
| 40 | 1.79 | 1.75 – 1.81 | 9.03 | 0.14 | > 0.82 | 1.24 |
| 50 | 1.31 | 1.90 – 1.97 | 16.25 | 0.12 | > 0.75 | 0.50 |

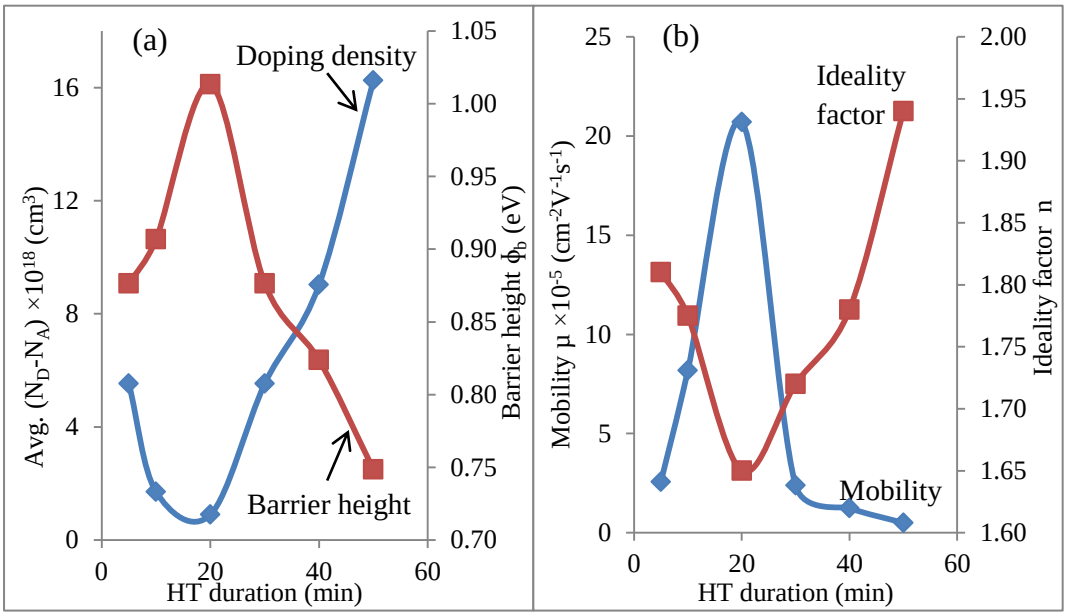


*Fig. 18: (a) Graph of Barrier height and doping density as a function of heat treatment duration and (b) graph of mobility and ideality factor as a function of heat treatment duration.*

In order to achieve better quality CdS layers required for highly efficient PV solar cell development, the doping density ($N_D$-$N_A$), electrical conductivity ($\sigma$) and charge carrier mobility ($\mu_\perp$) should be optimised with major consideration of layer thickness, heat treatment temperature and duration. Other factors to consider such as the reduction of defects due to inherent impurities and production of larger grains to reduce native defects and scattering will further improve the properties of the layers. The observation of minimum ideality factor (*n*) at 20 minutes heat treatment duration shows the presence of minimum R&G centres under the treatment conditions.

Comparison of results on electrodeposited ED-CdS layers presented in this work with previously reported Schottky barrier work on thin films of CdS grown by chemical bath deposition (CBD) and bulk CdS crystals grown by melt-grown techniques show great prospects for development of ED-CdS layers. Table 9 summarises the main parameters available for comparison. Schottky barriers formed on all the layers exhibit similar parameters for RF and potential barrier height. Low *n* values for diodes made on bulk crystal show the presence of less R&G centres as expected. However, the diode properties observed for poly-crystalline CdS show that the layers have good electronic quality for fabricating excellent PV devices. Although the ideality factor *n* of both ED-CdS and CBD-CdS shows that the charge carrier transportation mechanism is governed by both thermionic and R&G, it was interesting to observe that comparatively high rectification factor and low series resistance in the ED-CdS layer. The lower barrier height in Ed-CdS might be due to Fermi-level pinning at the defect states or due to the presence of impurities.

*Table 9: The summary of electrical property comparison between ED-CdS, CBD-CdS and bulk CdS crystal.*

| CdS Material Used | $\rho$ (Ωcm) | RF | *n* | $\phi_b$ (eV) | $R_s$ (Ω) | $R_{sh}$ (Ω) | $N_D$-$N_A$ ($cm^{-3}$) | μ ($cm^2V^{-1}s^{-1}$) |
|---|---|---|---|---|---|---|---|---|
| ED-CdS | $2.2\times10^4$ | $10^4$ | 1.65 | 1.01 | 0.1 | $10^6$ | $10^{17}$ | $2.1\times10^{-4}$ |
| CBD-CdS [14] | $10^5$ | $10^{3.3}$ | 1.50 | 1.02 | 20.0 | - | $10^{17}$ | $10^{-3}$ |
| Bulk- CdS [15], | - | $10^4$ | 1.08to | 1.04 (SXPS) | - | - | $10^{16}$ | - |

| | | | |
|---|---|---|---|
| [16] | | 1.30 | 0.8 (I-V) |

## 4. CONCLUSIONS

The work presented in this paper demonstrates the electrodeposition of CdS using 2-electrode configuration from an electrolytic aqueous bath containing cadmium chloride hydrate ($CdCl_2 \cdot xH_2O$) and thiourea ($NH_2CSNH_2$) as cadmium and sulphur precursors respectively. Based on the material characterisation techniques explored, 791 mV was identified as the best cathodic potential in which stoichiometric ED-CdS is achieved. XRD results show that the both cubic and hexagonal CdS were present in the as-deposited CdS layer, while, only the hexagonal CdS was retained after heat treatment at 400˚C for 20 minutes in air in the presence of $CdCl_2$ with preferred orientation along the (002) plane. Both the XRD and SEM results in this work indicate grain growth after $CdCl_2$ treatment and the formation of large clusters of CdS consisting of small crystallites size ranging from ~(23–47) nm as-deposited and ~(33–66) nm after $CdCl_2$ treatment and a cluster size ranging from 300 nm to 1µm. The optical absorption results showed a bandgap range of (2.40–2.42) eV after $CdCl_2$ treatment.
The effects of heat treatment temperature and heat treatment duration were also explored using thickness measurement, SEM, optical absorbance and transmittance. Further analysis on the electronic properties of ED-CdS using both I-V and C-V measurements were also explored. Excellent rectifying diodes with rectification factor exceeding ~$10^4$ were formed with FTO/CdS/Au structures. The observed ideality factor ranges between 1.50–2.00 and a barrier height above 1.01 V was achieved. The C-V and Mott Schottky plot of the effect of CdS layer thickness shows an increasing conductivity and hence mobility with increase in layer thickness. While an inverse relationship between doping density and mobility was also observed. Comparisons of Schottky device parameters show that ED-CdS layers have good electronic quality when compared to CBD-CdS layers and bulk CdS crystal. The lowest ideality factor was observed after heat treatment at 400°C for 20 minutes which indicates the lowest R&G centres under the condition. The incorporation of these layers into CdS/CdTe solar cell is in progress.

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