A tutorial on double pulse test of silicon and silicon carbide MOSFETs

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A Tutorial on Double Pulse Test of Silicon and Silicon Carbide MOSFETs

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***Abstract*— In the power electronics and machine drives area, recent advancements in power electronics devices are paving a more sustainable future. The importance of improved power devices is beneficial within the growing industry, for example, Electric Vehicles. New power devices are continuously researched to combat drawbacks like loss and switching time. The electrical engineering curriculum should be supported by market-oriented knowledge and industry skills based on the market leaders' vision and recruiting plans. Our ultimate objective is to modify the power electronics modules' curriculum and reskill our graduates to satisfy the industry's needs. This paper introduces one of the topics in power electronics which was identified as an industry requirement: the Double Pulse Test (DPT), to be highlighted in future curriculums. This test will be used as a comparison tool for two power electronic devices: Silicon MOSFET (Si-MOSFET) and Silicon Carbide MOSFET (SiC-MOSFET).**

Keywords—Double Pulse Test, Power electronics, Si-MOSFET, SiC-MOSFET, Switching Loss, Industry skills, electrical Engineering market.

I. INTRODUCTION

Nowadays, wide-bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have more attention due to their superior performance in automotive and industrial applications compared to Silicon switches [1] - [4]. The MOSFETs featured in this manuscript are the traditional Silicon (Si) MOSFET and the recent SiC-MOSFET from the enhancement mode type. The traditional n-type MOSFET is a quad-terminal device comprised of a Gate Body, Source, and Drain. The gate, a metal contact, is electrically insulated from the main body of the device with a thin oxidation layer < 100 nm of Silicon Dioxide or Silicon-Oxynitride. Applying a bias voltage to the gate controls the conducting channel width, formed below the oxidation layer and situated between the source and drain. Hence, the gate controls the flow of charge carriers from the source to the drain [5]. Wide band-gap devices such as SiC offer superior performance to their Si-based counterparts [6]-[9]. The construction process of the SiC-MOSFET is similar to Si-MOSFET. The fabrication process is advantageous as opposed to other wide band-gap materials like Gallium Nitride (GaN). More specifically, wafers of Silicon- Dioxide can be grown using thermal oxidation, a process already utilised in Silicon wafer construction [10], [11]. The proposed benefits of a Silicon-Carbide substrate over a pure Silicon substrate rely on the difference in band-gap between the materials. Pure silicon has a far smaller band-gap compared to that of Silicon-Carbide. The Si-MOSFET has an energy gap of 1.1-1.5 eV, while the SiC-MOSFET has 2 to 7 eV. Ultimately this allows Silicon-Carbide, to tolerate an electric field of approximately ten times that of pure silicon [11]. Therefore, traditional MOSFETs are restrained by the 'Silicon Limit', the optimal doping profile that provides the minimum series resistance for an Epitaxial Layer for a given breakdown voltage under set conditions. The Epitaxial Layer is the key voltage-sustaining region and is the greatest contributor to the on-state resistance of the MOSFET [12]. Accordingly, there is a need for switching devices to provide high efficiency, high switching frequency, small size, and low cost [1].

One of the major benefits of the SiC-MOSFET over the Si-MOSFET counterpart is that they can be built smaller and thinner for similarly rated performances. The higher critical electric field of the SiC substrate allows for higher injection doping levels, hence a greater packing density [13], [14]. Therefore, SiC offers low switching loss (lower turn-on and turn-off loss), increased thermal capabilities, and a high rating from the forward current and blocking voltage [1], [2], [6]. SiC MOSFETs have blocking voltage in the range of 1.2 kV up to 15 kV and have become an excellent contender to Si-IGBT while offering a higher switching frequency. Therefore, they become candidates for motor drive applications such as electric vehicles and switched-mode power supplies. A sample of SiC and Si-MOSFET is shown in Fig. 1.

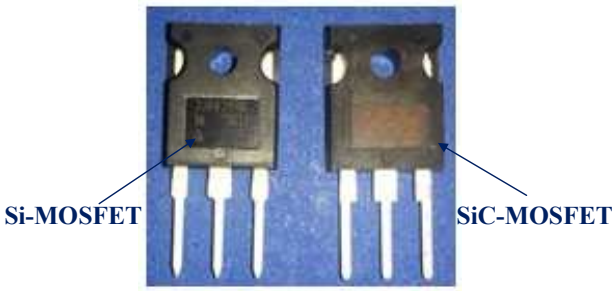


Fig. 1. Sample of Si and SiC MOSFETs

To this end, Section II presents the double pulse test for power switches. Analytical calculations for switching times and losses are detailed in section III. The hardware setup for the DPT is introduced in section IV, including simulation and practical results for the selected switches. The conclusion is added in section V.

II. DOUBLE PULSE TEST (DPT)

One of the gaps that fresh engineers have is limited knowledge about the most up-to-date technology in devices such as SiC MOSFET, including reliability, heat management, control, and losses, as they are rarely covered in the university curriculum. One of these topics is the switching loss for devices such as Si and SiC MOSFETs using DPT. A survey was conducted between 38 academics and 18 industry employers regarding the DPT to be embedded in the PEMD curriculum. Fig. 2 indicates the response to questions. The response shows that 69 % of the academics do not deliver anything about the topic, while 78 % of the industry employers want this knowledge.

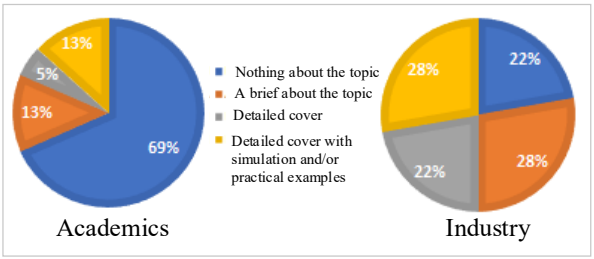


Fig.2. The academia and industry response.

The double pulse test determines the switching behaviour for a specific switch, such as IGBT and MOSFETs [1], [2], [15], [16]. The test enables the device under test (DUT) to be switched at different current levels by adjusting the double pulse timing using inductive load and DC-power supply [1], [15]-[17] while turning it on and off at that current. The circuit diagram of the DPT is shown in Fig. 3. It consists of a DC-power supply with smoothing and filtering capacitors, switch (SW), inductor, freewheeling diode, the DUT, voltage and current measurement, and Gate Drive Circuit (GDC) for generating the pulses applied to the gate-source terminals.

The pulses are generated as illustrated in Fig. 4. A PC-Host is used to build the code that generates the double pulse using Arduino or a microcontroller. In this manuscript, we used Arduino to create pulses with a level voltage of +5V. The output from the Arduino will trigger the GDC. The function of the GDC is to generate a pulse that matches the DUT gate and achieves short rise and fall switching times. The GDC generates the required voltage by the switch to be applied between Gate-Source for MOSFETs and Gate-Emitter if it is an IGBT device, as shown in Fig. 5 part (a). The timing of the pulses is denoted as T1, T2, and T3. The time T1 represents the time of pulse 1, T2 represents the off time between pulses 1 and 2, while T3 represents the time of pulse 2. To limit the *di/dt*, the switching pulse time are selected for not less than 10 µs with designed inductance to ensure that the device reaches the selected current [6], [18]. If the time T1 is selected T µs, the time T2 is selected to be shorter than T1 and can be taken as ½ to ⅔ T to keep the load current constant at on and off transitions. At that time, the diode acts as a freewheel. The time T3 is shorter than T1 but sufficiently long to take the measurement and can be taken as ½ T [4], [15], [19]. The maximum range of time T1 is 200 µs to avoid a slow *di/dt* and avoid voltage dip for the DC bias voltage of more than 5 % and limit the temperature increase to not affect the switch performance [15], [19].

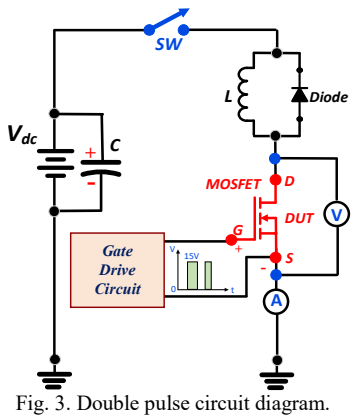


Fig. 3. Double pulse circuit diagram.

The typical switch voltage is depicted in Fig. 5 part (b), while a typical switch current is illustrated in Fig. 5 part (c). Fig. 6 shows the current flow at different pulses. During pulse 1 (Turn-On stage), the energy is transferred from the DC source to the inductor and establishes the designed current through the DPT, as indicated in Fig. 6a. The inductor is used to replicate circuit conditions in a converter design [2], considering clamped and unclamped cases. The inductor can be designed using (1) and (2). During pulse 1, dt = T1, and di = I (the desired current), and v is the DC-Bias voltage, V_{DC}.

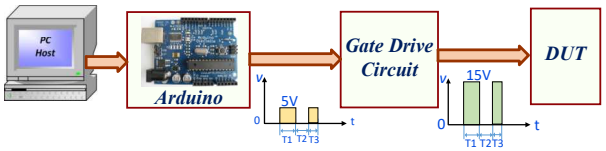


Fig. 4. Double pulse generation.

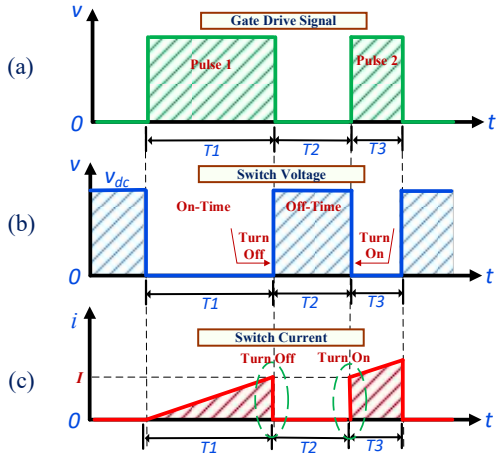


Fig. 5. Double pulse out from the GDC and switch voltage and switch current during Turn-On and Turn-Off instants (a) Double pulses, (b) Switch voltage, and (c) Switch current.

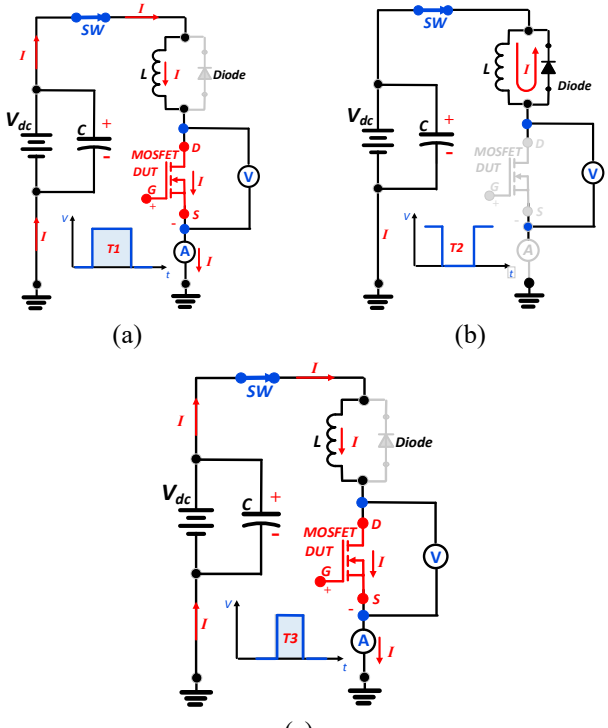


Fig. 6. Current flow at different pulses (a) At pulse T1, (b) at pulse T2, and (c) at pulse T3

$$v = L\frac{di}{dt} \quad (1)$$

$$L = \frac{V_{DC} * T1}{I} \quad (2)$$

The time T2 represents the Turn-Off stage, and current flows in the freewheeling diode, as shown in Fig. 6b while current flow at time T3 is indicated in Fig. 6c. The first Turn-On pulse will start making the MOSFET to conduct but the current is not yet established in the inductor. Therefore, calculating the losses at this moment will result in inaccurate assessment. So, we have to build up a current in the inductor then turn off then turn on to calculate the losses more accurately. The main target is the Turn-On and Turn-Off instants. Turn-Off and Turn-On timing measurements are captured at the first pulse's Turn-Off and the second pulse's Turn-On [1], [15] as those happened at the same current value as shown in Fig. 5 (c). At the Turn-On instant, the switch changes the voltage from the source voltage to the switch saturation voltage. The current reaches the designed value and vice-versa for the Turn-Off. The Turn-ON time determines the Turn-on parameters (Turn-On delay time, rise time, *dv/dt*, and *di/dt*). The Turn-Off time determines the Turn-Off parameters (Turn-Off delay time, fall time, Turn-Off time, *dv/dt*, and *di/dt*). The On and Off -energy (E_{on} and E_{off}) can be measured, determining the energy loss during On and Off times.

III. Switching Times and Losses Calculation

Assessing the switching losses is inevitable for power switches. The learners should know its measurement and how to be minimised as they affect the overall system efficiency. The non-ideal behaviours occur because of the switching times and the drain-source resistance during conduction R_{ds-on} and parasitic capacitors between the terminals, as shown in Fig. 7 [15]. For MOSFETs, there is an input capacitance between gate and source C_{GS}, gate and drain C_{GD}, output capacitance between gate and source, and drain and source C_{DS} [16]. Parasitic capacitances are the major contributor to switching losses and switching time delay during On and Off times. The parasitic capacitances on the gate slow down the device's switching speed, extending the Turn-On and Turn-Off times and limiting the switching frequency. Hence, there is a trade-off between keeping the switching losses at a minimum and increasing switching frequency.

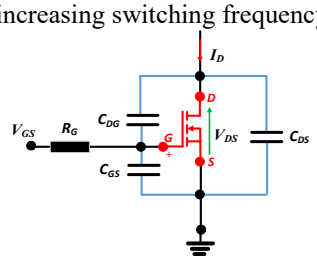


Fig. 7. MOSFET model with parasitic capacitance.

Fig. 8 illustrates the MOSFET behaviours during On and Off times. Fig.7a indicates the Turn-On and Turn-Off times versus gate-source voltage, while Fig. 5b illustrates the MOSFET behaviour (Drain current and Drain-Source voltage) during On and Off times. Prior to $t = 0$, the switch is in the Off state and the drive voltage, $V_{GS} = 0$. At t=0, the drive voltage is applied to the gate-source terminals. Gate current flows from the drive voltage through R_G (Fig. 7) into the MOSFET input capacitance (C_{DG}+C_{GS}). The voltage V_{GS} charges exponentially with a time constant τ=R_G(C_{DG}+C_{GS}) as in (3).

$$v_{GS}(t) = V_{GS}\left(1 - e^{-\left(\frac{t}{\tau}\right)}\right) \quad (3)$$

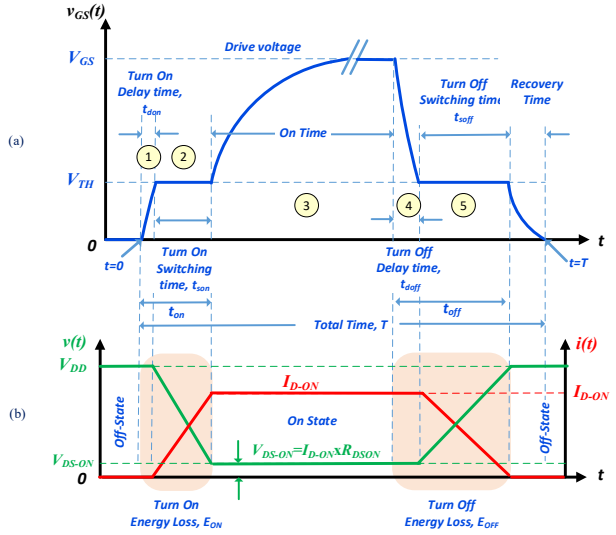


Fig. 8. Switching time versus drive voltage (a) Turn-On and Turn-Off time versus Gate-Source voltage (b) Switch voltage and current versus Turn On and Turn Off time.

At the time $t = t_{don}$, the voltage $v_{GS}(t_{don})$=V_{TH}, where V_{TH} is the switch threshold voltage. The interval t_{don}, (denoted by 1 in the yellow circle, Fig. 8a represents the delay between the rising edge of the drive signal, V_{GS}, and the Turn-On response of the MOSFET or the time between a rising edge of the drive voltage and the onset of switching in the MOSFET. Interval 2 represents the Turn-On switching interval t_{son}. The drain-source voltage, V_{DS}, falls from V_{DD} to V_{DS-ON}, and the drain current starts to increase from 0 to I_{D-ON}, (see Fig.8b). We assume that the drain voltage and drain current change linearly. Accordingly, the drain-gate voltage, V_{DG}, is changing, and (4) for capacitor C_{DG} current must hold

$$i_{DG} = C_{DG}\frac{dV_{DG}}{dt} \quad (4)$$

If the rate of change of V_{DG} is much higher than the rate of change of V_{GS}, with respect to the time as in (5), almost all gate current flows in the capacitor C_{DG} implies that the voltage V_{GS}, is almost constant.

$$\left|\frac{dV_{DG}}{dt}\right| > \left|\frac{dV_{GS}}{dt}\right| \quad (5)$$

Substituting for the current in (4) provides

$$\frac{V_{GS} - V_{TH}}{R_G} = C_{DG}\frac{V_{DC}}{t_{son}} \quad (6)$$

The energy dissipated during the Turn-On process is given by

$$E_{on} = \int_0^{t_{son}} P(t)dt \quad (7)$$

where P(t) is the instantaneous power, is

$$P(t) = v_{DS}(t)i_D(t) \quad (8)$$

From Fig. 8b, interval 2, the drain voltage and drain current are given by

$$v_{DS}(t) = -\frac{V_{DC}}{t_{son}}t + V_{DC} \quad (9)$$

$$i_D(t) = \frac{I_{D-ON}}{t_{son}}t \quad (10)$$

Using (9) and (10), substitute in (8)

$$E_{ON} = \frac{V_{DC}I_{D-ON}}{6}t_{son} \quad (11)$$

For interval 3, the MOSFET is now On, and the drive voltage continues to rise towards the V_{GS} (Fig. 8b). The MOSFET looks like a resistor with a value $R_{DSon,}$ and the drain-source voltage V_{DSON} is given by

$$V_{DS-ON} = I_{D-ON}R_{DS-on} \quad (12)$$

Intervals 4 and 5 represent the Turn-Off process (Fig. 8b). The turn-off process is essentially the reverse of the Turn-On process. At interval 4, the delay time t_{doff} is incurred between the falling edge of the V_{GS} and the exponential fall of drive voltage reaching V_{TH}.

$$v_{GS}(t) = V_{GS}e^{-\left(\frac{t}{\tau}\right)} \quad (13)$$

If the voltage $v_{GS(t)}= V_{TH}$, the time $t = t_{doff}$. The input capacitance must be discharged from V_{GS} to V_{TH}, before Turn-Off switching can occur. The current available to charge C_{DG} from approximately V_{DS-ON} to V_{DC} is different to the turn-on case. The Turn-Off switching time t_{soff} is caused by the limited availability of gate current to charge C_{DG} to the value V_{DC}.

$$I_G = \frac{0 - V_{TH}}{R_G} = C_{DG}\frac{V_{DC}}{t_{soff}} \quad (14)$$

$$t_{soff} = R_G C_{DG}\frac{V_{DC}}{V_{TH}} \quad (15)$$

The energy dissipated during the Turn-Off process is given by

$$E_{off} = \int_0^{t_{soff}} P(t)dt \quad (16)$$

From Fig. 8b, interval 5, the drain voltage and drain current are given by

$$v_{DS}(t) = \frac{V_{DC}}{t_{soff}}t \quad (17)$$

$$i_D(t) = -\frac{I_{D-ON}}{t_{soff}}t + I_{D-ON} \quad (18)$$

Substitute in (16)

$$E_{Off} = \frac{V_{DC}I_{D-ON}}{6}t_{soff} \quad (19)$$

Accordingly, DPT is a good tool to determine switching losses by calculating energy loss during Turn-On and Turn-Off times for a designed current and voltage, considering intervals 2 and 5 during the test. Three options can be used to calculate energy loss during ON and OFF time. Option 1, using (11) and (19) to give an estimate about the switch loss. Option 2, using the scope and math function, multiplies the voltage and current to have the instantaneous power, captures the power waveform for the selected time window, and integrates the power function with the aid of MATLAB to get the energy loss. Option 3, the lab can provide a scope with a math function to multiply current and voltage and then integrate for the selected time interval. Authors used option 2 to calculate the switch loss using DPT.

IV. Double Pulse Test Hardware Setup

The hardware setup of the DPT, as shown in Fig. 9, is built based on section IV. A DC power supply is used to supply the required DC voltage. In our undergraduate lab, the maximum DC voltage is 35 V. A 30 MHz voltage probe is used to capture the drain and source voltage V_{DS} while a current clamp is used at the MOSFET source terminal to measure the source current I_D. The design specifications and testing conditions are at ambient temperatures (24 °C), Drian current 1 to 1.2 A, pulse T1 is in the range of 30 µs, and pulse T3 is in the range of 10 µs.

From (2), the inductor size and rating can be calculated as 1 mH. Table I illustrates all the designed circuit components.

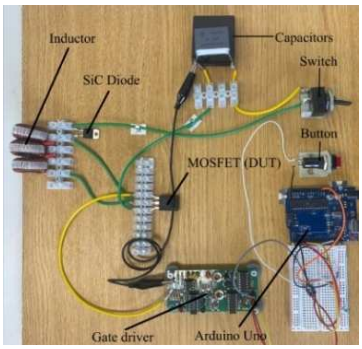


Fig. 9. The hardware setup of the DPT.

As aforementioned, the Gate Driver is an essential part of the testing circuit. The gate driver is responsible for supplying the MOSFET gate with a suitable voltage so that the MOSFET can reach saturation and Turn-On. It is crucial to ensure the gate driver can provide a proper square wave signal at +15V. To test the GDC, use a 5 V DC input from a voltage source, as shown in Fig. 10, and a square wave signal of 5 V is produced using a signal generator. This causes the output of the gate driver to produce a square wave signal from 0 to +15V. The Gate driver outputs the signal as the input signal frequency. This means the MOSFET switching characteristics can be tested at a large range of frequencies. Later, an Arduino will be used to produce the double pulse to be input for the Gate drive. The circuit shown in Fig. 9 can be used to test any switch within the designed current range.

Table I: DPT circuit components

Component	Value/rating	Reference
Inductor	Toroidal 3*330 µH (in series), 5.2 A	[20]
Capacitor	AC Filtering Metalized Polypropylene Film Capacitor, 10 µF, 250 V_{AC}	[21]
Diode	STPSC12065-Y, 650-V, power Schottky silicon carbide diode	[22]
Switches	Toggle and On-OFF switches 16 A, 250 V_{AC}	[23]

The objective is to compare the Si and SiC Power MOSFETs, using simulation and experimentation methods to determine the individual device characteristics. By testing Si and SiC

Power MOSFET devices from various manufacturers, the most effective MOSFETs can be ascertained based on price and desirable characteristics. Furthermore, the measured advantages of the SiC MOSFET can be compared with the Si-MOSFET, and the most suitable applications for each device can be suggested. Finally, comparisons can be made between the results of electrical circuit/device simulation software and real-world performance under laboratory testing conditions. The switches that were under test are tabulated in Table II.

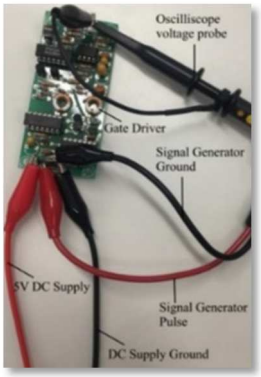
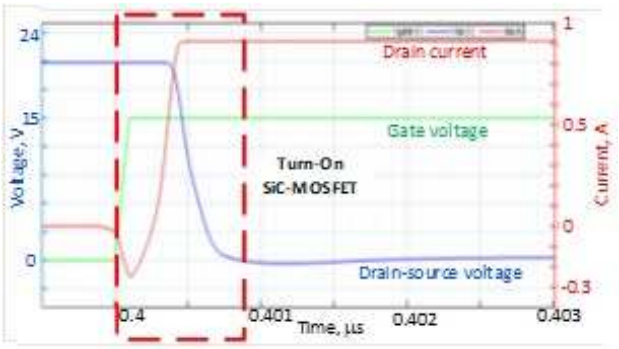


Fig. 10. Gate driver testing using a signal generator and DC voltage source.

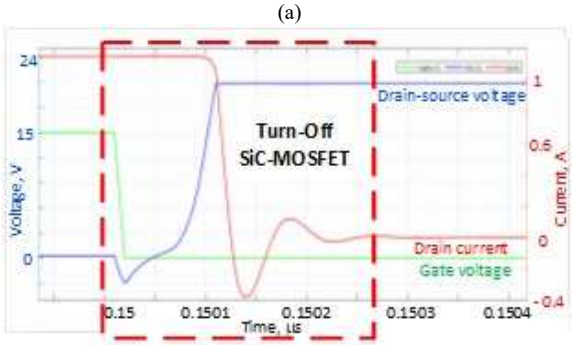
Table II: Switches under test

Switch	Model / Type	Reference
SiC	Cree, C2M0160120D Silicon Carbide Power MOSFET, 1200 V, 19 A	[24]
	SCT30N120, 1200 V, 45 A	[25]
Si	Vishay IRFPC60LC, SiHFPC60LC, 600 V, 16 A.	[26]
	Infineon SPW20N60S5, 600 V, 20A	[27]

The LTspice Software package is used to simulate the DPT. There are two types of Spice models for MOSFET characterisation. The ".MODEL" statement is the simplest complexity (SPICE Level 1), and the ".SUBCKT" statement provides a much higher complexity model (SPICE Level 2 or 3), as it includes many more parameters used in the model. Manufacturers use ".SUBCKT" to simulate the MOSFETs to a higher degree of accuracy but at a slower simulation time compromise. The MOSFETs simulated in this project will use the ".SUBCKT" statement. A sample of the DPT simulation results is shown in Fig. 11. Fig. 11a and c illustrate the Turn-On process for the SiC-C2M0280120D [24] and SPW20N6055S [27], respectively. While Fig 11b and d show the Turn-Off process. These Figs. have been presented in MATLAB, with data collected using SPICE simulation. By simulating MOSFETs before experimenting, the reliability and accuracy of the SPICE modelling package and manufacturer component models can be compared against the experimental values. Findings can be drawn as to whether this simulation package is suitable to rely upon. Switching energy (Energy Ton and Toff) have been found by using the LTspice integrator tool after finding the instantaneous and average power for both switches. By observing the energy consumed over the switching periods, it is obvious the energy loss difference between the power switches affirms the superiority of the SiC. The current waveform depicts higher oscillation while switching the Si MOSFET. The voltage also reaches steady-state quicker in the SiC case. This allows the SiC to switch at higher frequencies than the Si.



(a)



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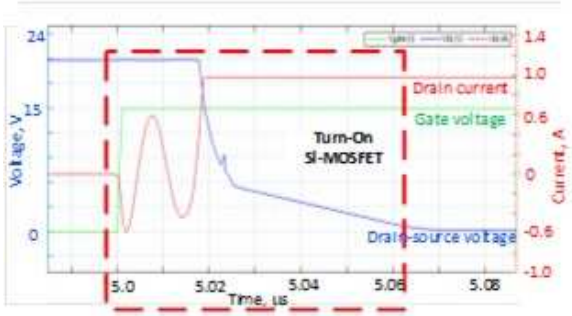
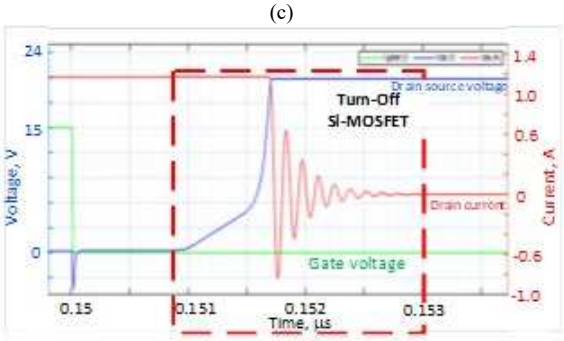


(c)



(d)

Fig. 11. Simulation of DPT for SiC-C2M0280120D and SPW20N6055S (a) and (b) Sic MOSFET, (c) and (d) Si MOSFET, (a) and (c) Turn-On time, and (b) and (d) Turn-Off time.

It is well known that simulation is never 100 % accurate compared to the real experimentation due to laboratory simulations inconsistencies and natural variance, small factors such as room temperature or component variance can affect the overall performance. A sample of the experimental results for SiC is shown in Fig. 12.

Fig. 12. DPT experimental results for SiC MOSFET.

V. Conclusion

The paper discussed embedding an activity which will achieve up-skilling and bring more awareness about recent power switches by conducting a Double Pulse Test (DPT) for the semiconductor devices such as Silicon MOSFET or Silicon Carbide MOSFET. The DPT is performed to guarantee the specification of power-device datasheets, confirm the actual value or deviation of the power devices or power modules, and measure the switching parameters with various current value conditions. We introduced a detailed structure of the DPT to be built either using simulation or in the lab. Now, it easily includes the DPT in the power electronics curriculum based on the industry employers' recommendations.

Acknowledgement

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