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Review

Electroplating of Semiconductor Materials for Applications in Large Area Electronics: A Review

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Abstract: The attributes of electroplating as a low-cost, simple, scalable, and manufacturable semiconductor deposition technique for the fabrication of large-area and nanotechnology-based device applications are discussed. These strengths of electrodeposition are buttressed experimentally using techniques such as X-ray diffraction, ultraviolet-visible spectroscopy, scanning electron microscopy, atomic force microscopy, energy-dispersive X-ray spectroscopy, and photoelectrochemical cell studies. Based on the results of structural, morphological, compositional, optical, and electronic properties evaluated, it is evident that electroplating possesses the capabilities of producing high-quality semiconductors usable for producing excellent devices. In this paper we will describe the progress of electroplating techniques mainly for the deposition of semiconductor thin film materials and their treatment processes, and fabrication of solar cells.

Keywords: electroplating; semiconductors; large-area electronics; characterisation; solar cells

1. Introduction

Electroplating has been well explored over the years especially for the purification, extraction, protection, and coating of semiconductors, metals, and metalloids in the industrial sector [1] to achieve diverse characteristic properties. The use of the electroplating technique in the deposition of semiconductor materials dates back to the 1970s [2–4], with the deposition of semiconductors from the II-VI group. The ascendance of the electrodeposition of semiconductor material led to the growth and fabrication of CdS/CdTe-based solar cell devices within a decade afterwards [5]. The fabrication of thin-film solar cells with photovoltaic conversion efficiency of ~10% was the stimulus for an intense global research into electrodeposited semiconductor compounds. The research also spanned into the electrodeposition of II-VI semiconductor materials such as ZnTe [6], ZnSe [6], ZnS [7], ZnO [8], etc., and spread into semiconductor material compounds in the binary (III-V, IV-VI), ternary (CuInSe₂) [9,10], and quaternary (Cu₂ZnSnS₄, CuInGaSe₂) groups [11]. The electroplating of elemental semiconductors and other wide bandgap nitrides has also been captured in the literature. This communication critically appraises the strengths, weaknesses, potentials, and the state-of-the-art electroplating technique in the fabrication of large-area electronics and other macro-electronic devices such as photovoltaic (PV) solar panels and display devices.

2. An Overview of Electrodeposition Technique

Electrodeposition is the process of depositing elemental or compound metals or semiconductors on a conducting substrate by passing an electric current through an ionic electrolyte in which metal or semiconductor ions are present [12]. The passage of current is required due to the inability of the chemical reaction resulting in the deposition of the solid material on the conducting substrate to proceed on its own as a result of positive free energy change ΔG of the reaction.

Electrodeposition can be categorised based on power supply source, working electrode, and electrode configuration (as shown in Figure 1), but the basic deposition mechanism and setup remains similar. The basic deposition mechanism entails the flow of electrons from the power supply to the cathode. The positively charged cations are attracted towards the cathode and negatively charged anions to the anode. The cations or anions are neutralised electrically by gaining electrons (through reduction process) or losing electrons (through oxidation process) and being deposited on the working electrode (WE), respectively [12].

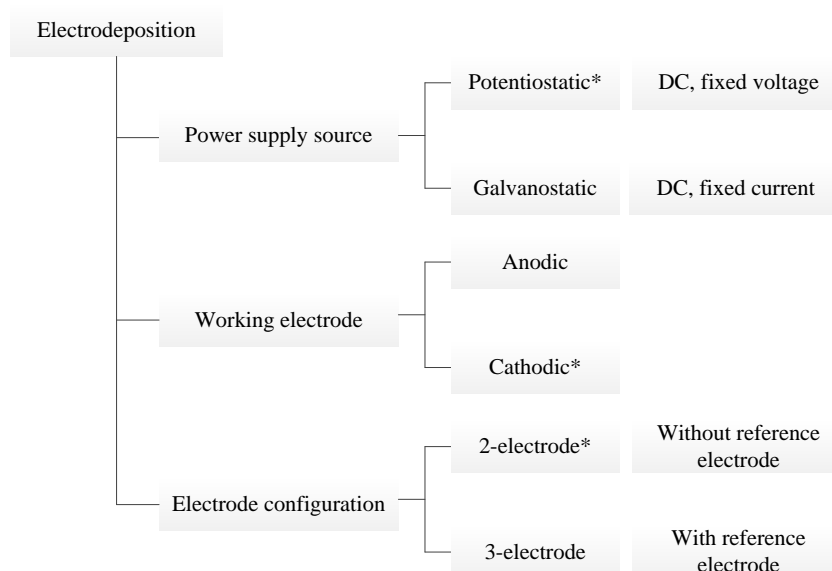


Figure 1. The main categories of electrodeposition technique.

The typical electrodeposition (ED) setup of a two-electrode (2E) configuration, as shown in Figure 2a, consists of a deposition container (beaker), deposition electrolyte, magnetic stirrer, hotplate, power supply, a working electrode, a counter electrode, and an optional reference electrode (RE) in the case of a three-electrode (3E) configuration (see Figure 2b). The use of a potentiostatic power source was due to the effect of deposition voltage on the atomic percentage composition of elements in the electrodeposited layer, which is one of the factors determining the conductivity type [13,14]. Cathodic deposition is mainly utilized due to its ability to produce stoichiometric thin-films with good adherence to the substrate as compared to anodic deposition [15]. Conversely, the galvanostatic electrodeposition is controlled and measured by maintaining constant current density through an electrolytic cell disregarding the changes in the resistance due to the deposited electroplated layer.

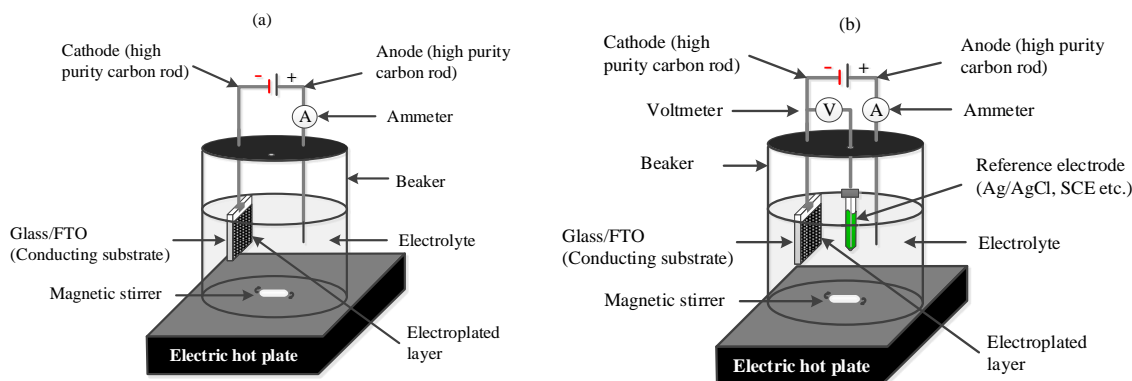


Figure 2. Typical (a) two-electrode and (b) three-electrode electrodeposition setups.

The 2E configuration, as shown in Figure 2a, was utilised due to its industrial applicability, process simplification, and also to eliminate possible Ag^+ - and K^+ -ion doping [16,17], which may emerge from the Ag/AgCl or saturated calomel electrode (SCE) reference electrodes (see Figure 2b). Taking the electrodeposition of n-CdS and n-CdTe layers which are respectively utilised as the main window and absorber layers in this work into perspective, both K^+ and Ag^+ from group I of the periodic table are considered as p-type dopants. Therefore, any leakage of K^+ and Ag^+ into the electrolytic bath may result in compensation leading to the growth of highly resistive material which has a detrimental effect on the efficiency of fabricated solar cells. This has been experimentally shown and reported in the literature [16].

The two-electrode electrodeposition configurations are not without challenges, with the main challenge being the fluctuation or drop in the potential measured across the cathode and the anode during deposition. This is due to the alteration in resistivity of the substrate with increasing semiconductor layer thickness and the change in the ionic concentration of the electrolyte. For the three-electrode configuration, the potential difference is measured across the working and the reference electrodes, while the measured current is between the working and the counter electrodes. In general, other factors such as the pH of the electrolyte [18], applied deposition potential [13,14], deposition temperature [19], stirring rate [20], deposition current density, duration of deposition and thickness [21], underlying substrate [22], and concentration of ions in the deposition electrolyte [18] affects the electrodeposition process and the properties of the deposited layers. Recent publications have demonstrated the similarities between electrodeposited semiconductors using three-electrode and two-electrode electroplating configurations [23,24]. The electrodeposition of both elements and compounds is governed by Faraday's laws of electrodeposition as mathematically depicted in Equation (1).

$$T = \left(\frac{1}{nF} \right) \left(\frac{itM}{\rho A} \right) = \left(\frac{JtM}{nF\rho} \right) \quad (1)$$

where T is the thickness (cm), J is current density (A cm^{-2}), t is the deposition time (s), M is the molecular mass (g mol^{-1}), n is the number of electrons transferred in the chemical reaction for the formation of 1 mole of substance in g cm^{-3} , F is Faraday's constant ($96,485 \text{ C mol}^{-1}$), and ρ is the density (g cm^{-3}). It should be noted that Faraday's law of electrolysis assumes that all electronic charges passing through the electrolyte contribute to the deposition of deposited material layer without any consideration of the resistance losses in the system and electronic charge contribution to the decomposition of solvent into its constituent ions [25].

3. Factors Influencing Electrodeposition

3.1. Solutes, Solvents, and Deposition Electrolytes

The effects of the incorporated solute and solvent utilised are of importance in electrodeposition. Taking the electrodeposition of CdS into consideration, sodium-(Na)-based precursor ($\text{Na}_2\text{S}_2\text{O}_3$) has been often utilised [26,27]. Although sodium (Na) ions are not electrodeposited at low cathodic voltages, the incorporation of Na in CdS films is achievable through adsorption, absorption or chemical reactions as a result of increased Na accumulation in the electrolytic bath. It should be noted that Na is a p-type dopant in CdS [28] resulting in increasing electrical resistivity of subsequent CdS layers due to Na accumulation. Further to this, the Na-based precursor ($\text{Na}_2\text{S}_2\text{O}_3$) is also associated with the precipitation of sulphur during the electroplating. Recent understanding has shown that the replacement of the well-established sulphur precursor with thiourea (NH_2CSNH_2) (which is more associated with chemical bath deposition (CBD) technique) results in the reduction/elimination of sulphur precipitate [29,30].

The choice of solvent to be utilised also possesses as an important factor in electroplating as demonstrated by the deposition of CdTe from ethylene glycol ($\text{C}_2\text{H}_6\text{O}_2$) electrolyte containing cadmium iodide (CdI_2) [31]. Using aqueous solution as solute, Cd-I complexes such as CdI^+ , CdI_2 ,

CdI_3^- , and CdI_4^{2-} are formed in aqueous solution [32,33] debarring the deposition of Cd and the co-deposition of CdTe. It is noteworthy that CdTe from other Cd precursors have been explored and reported in the literature [34,35]. Therefore, the choice of solute and solvent for electroplating purposes is a factor to reckon with in addition to a number of other factors inherent in the electrodeposition process to achieve superior qualities of electroplated semiconductor materials. This understanding has been accrued for over two decades of exploration, and careful examination of grown semiconductors at Solar Energy Group within Sheffield Hallam University (SHU), in addition to the literature. A large number of semiconductors explored in SHU and documented in the literature [9,29,36–47] is summarised in Table 1.

Table 1. Summary of explored electronic materials to date at authors' research group using electroplating from aqueous solutions.

Material Electroplated	E_g (eV)	Precursors Used for Electroplating	Comments	Ref.
CuInSe ₂	~1.00	CuSO ₄ for Cu ions, In ₂ (SO ₄) ₃ for In ions and H ₂ SeO ₃ for Se ions	Ability to grow both p- and n-type material	[9]
CdTe	1.45	CdSO ₄ or Cd(NO ₃) ₂ or CdCl ₂ for Cd ions and TeO ₂ for Te ions	Ability to grow both p- and n-type CdTe using Cd-sulphate, nitrate, and chloride precursors	[40,41]
CuInGaSe ₂	1.00–1.70	CuSO ₄ for Cu ions, In ₂ (SO ₄) ₃ for In ions, Ga ₂ (SO ₄) ₃ for Ga ions and H ₂ SeO ₃ for Se ions	Ability to grow both p- and n-type material	[42]
CdSe	1.90	CdCl ₂ for Cd ions and SeO ₂ for Se ions	–	[43]
InSe	1.90	InCl ₃ for In ions and SeO ₂ for Se ions	–	[44]
GaSe	2.00	Ga ₂ (SO ₄) ₂ for Ga ions and SeO ₂ for Se ions	–	–
ZnTe	1.90–2.60	ZnSO ₄ for Zn ions and TeO ₂ for Te ions	Ability to grow both p- and n-type material	[45]
CdS	2.42	CdCl ₂ for Cd ions and Na ₂ S ₂ O ₃ , NH ₄ S ₂ O ₃ or NH ₂ CSNH ₂ for S	Conductivity type is always n-type	[29,46,47]
CdMnTe	1.57–2.50	CdSO ₄ for Cd ions, MnSO ₄ for Mn ions and TeO ₂ for Te ions	–	–
ZnSe	2.70	ZnSO ₄ for Zn ions and SeO ₂ for Se ions	Ability to grow both p- and n-type material	[36]
ZnO	3.30	Zn(NO ₃) ₂ for Zn ions	–	[37]
ZnS	3.75	ZnSO ₄ for Zn and (NH ₄) ₂ S ₂ O ₃ for S ions	Ability to grow both p- and n-type material	[38]
Polyaniline (PAni)	–	C ₆ H ₅ NH ₂ and H ₂ SO ₄	To use as a pinhole plugging layer	[39]

3.2. Electrolytic Bath pH Value

The composition of an electrolytic bath naturally determines the pH of the bath. Basically, the acidity (pH < 7.00) of an electrolyte can be increased by the introduction of an acid. The hydrogen ions (H⁺) from the dissociated acid reacts with water in aqueous solution to form hydronium ions (H₃O⁺). On the other hand, the alkalinity of a solution increases (pH > 7.00) with the reduction in the H₃O⁺ concentration. This is caused by the reaction of dissociated hydroxide ions (OH[−]) from introduced alkaline with H⁺ ions from water dissociation to form water (H₂O) rather than hydronium ions. It is well documented that elemental and compound deposition responds to this chemical dynamic mainly in wet deposition techniques such as chemical bath deposition (CBD) [48] and electrodeposition techniques [49]. With emphasis on electrodeposition, the effect of pH on the bath and the deposited layers vary from selective deposition/etching of element [50], alteration of the characteristic properties of the deposited layers [51,52], elemental/compound precipitation [53],

and increase in the deposition current density [54]. Furthermore, the effect of pH on the dissociation of common solvent such as water is also well documented in the literature [55], with the notion that an increase in the acidity of an electroplating bath results in the increase in the concentration of dissociated ions in the aqueous solution [55]. Due to the increased ionic concentration, the deposition current density increases until it stabilises or continues to increase, depending on the composition of the solution.

3.3. Deposition Temperature

It is a known fact that an increase in the temperature of a matter increases the motion of the molecules inside it. As such, the electrolytic bath temperature increases solubility of the solvent, catalyses the reactions, energizes the ions, and increases the transport number, which results in an increase in the deposition current density and rate of deposition of constituent elements or compounds. Further to this, the work performed on electrodeposition depicted that an increase in the crystallinity of as-deposited semiconductor material is achievable at higher growth temperature [3,56]. For electroplated semiconductor materials from aqueous solution, there is a limitation on the growth temperature due to the boiling temperature of water at 100 °C under standard atmospheric pressure, while the electroplating from other electrolytic baths can go as high as 160 °C [31]. Deposition of materials at higher temperature provides energy required for ions/atoms to move around and deposit in a regular crystalline pattern.

3.4. Deposition Current Density

With regards to Faraday's law of electrodeposition, the deposition current density is directly related to the thickness of the deposited layer. Thus, the deposition current density is dependent on factors effecting the energizing of the inherent ions in the electrolyte such as stirring rate, bath temperature, concentration of constituent [57], and electrical conductivity of the substrate amongst other constraints. While a gradual alteration in the deposition current density is expected depending on the electrical conductivity of the electroplated layers.

With respect to semiconductor materials such as CdTe, the literature depicts the effect of current density on the morphological, compositional and the structural properties of the deposited layer [58,59]. Based on the deposition configuration, it can be inferred that the deposition current density of three-electrode configuration and two-electrode deposition configuration vary. CdTe with optimal characteristic properties deposited from a three-electrode deposition is known to lie between $\sim(0.3\text{--}0.6)$ mA cm⁻² [57,60]. While two-electrode electrodeposition has been documented to produce CdTe layers with an optimal characteristic property of $\sim(0.15\text{--}0.18)$ mA cm⁻² [61]. Under potentiostatic mode, Basol (1988) clarified that the deposition current density for CdTe electroplating depends on the tellurium concentration in the electrolyte [57]. The incorporation of excessive Te can alter the composition of the deposited CdTe, conduction type to *p*-CdTe due to Te-richness [62], and reduce adhesion on the underlying substrate. Reduction in the adhesion of CdTe may also occur due to the deficiency of Te concentration in the electrolytic bath. In either condition (excess or deficiency of Te concentration in the electrolyte), the crystallinity, morphology, and adhesion of the ensued CdTe layer suffer. In addition, current density during co-deposition of competing ions such as Ga³⁺ and Fe²⁺ in the electroplating of Fe–Ga alloys is a determinant of the Fe:Ga elemental composition ratio of the resultant alloy [63].

3.5. Duration of Deposition and Thickness

Electroplating of materials with main emphasis on semiconductor commences by the nucleation of the most electropositive element on the points on the conducting substrates with the highest electric field. Therefore, it can be categorically stated that the nucleation and nucleation modes of semiconductor material is conductive substrate dependent [1,22,64]. Consequential to the surface roughness of the underlying working electrode such as glass/fluorine-doped tin oxide (g/FTO),

the highest electric field is experienced at the peaks of the rough surfaces. The nucleation of the electroplated material spreads out through to the lowest valley from the initiation rough surface peaks resulting into columnar nature of the deposited layers [14]. The potency of this mechanism is highly influential at the initial stages of deposition due to unevenness of the deposited layer thickness characterised by pin-holes, voids, gaps, and high dislocation density within the semiconductor material [21]. This characteristic property is detrimental when a thin semiconductor layer with a thickness of <100 nm is required [21].

4. Strengths and Weaknesses of Electrodeposition

4.1. Strengths of Electrodeposition

4.1.1. Electrolytic Bath Life Longevity and Self -Purification

At the start of an electrolytic bath, electro-purification of the bath is highly essential to reduce and eliminate the impurity level, which is mostly incorporated in the precursors amongst other impurity sources. It should be noted that even with a high purity precursor with 99.999% purity, it can carry an impurity level of 10 ppm. Purification is essential due to the effect of impurities even in ppm levels [65] on the characteristic properties of electroplated semiconductor materials. It should be noted that electro-purification of a bath must be performed using similar deposition parameters (such as bath temperature, pH, stirring rate, etc.) to the semiconductor deposition. The electro-purification potential utilised should be lower than the deposition potential range of the required elements established using cyclic voltammetry. Based on this characteristic property of electroplating technique, the more layers deposited, the purer the electrolyte and the electroplated semiconductor gets due to the gradual reduction of background impurities and improved material property. This property not only increases the purity of the electrolyte and the deposited semiconductor, but also increases the longevity of the bath as compared to the batch process of chemical bath deposition (CBD) technique.

To further mitigate other sources of impurities, a fraction of researchers choose two-electrode over the three-electrode configuration to avoid possible impurities from the reference electrode. While the usage of Teflon-ware (polypropylene beaker) is necessitated to house the electrolyte due to possible leaching of elemental sodium and other dopants from glass-wares [66] into acidic electrolytes.

4.1.2. Ease of Doping Intrinsic and Extrinsic

With the effective purification of the electrolyte, intrinsic doping has been demonstrated in the literature for binary [38,67], ternary [68], and quaternary [69,70] semiconductor materials by changing the deposition voltage. Taking an example of a I–III–VI₂ semiconductor materials such as CuInGaSe₂, the stoichiometric semiconductor layer consists of 25% of the group I element, 25% of the group III elements, and 50% of group VI element. Due to the positive reduction potential of Cu ($E_o = 0.52$ V), at low deposition voltages, high elemental composition of Cu (group I) is incorporated in the semiconductor resulting into *p*-type conduction type. But an increase in the cathodic voltage increases the elemental composition resulting in an *n*-type semiconductor material, as in the case of CuInSe₂ (see Figure 3a). While at intermediate voltages, the material exhibits insulating or intrinsic properties. This electrical characteristic property, as demonstrated in the literature [68–70], signifies the ability of growth of *p*-, *i*-, and *n*-type materials from the same bath by cathodic voltage variation (see Figure 3). The incorporation of Ga in CuInGaSe₂ [42] increases the bandgap and also makes the material *p*-type. This must be due to the formation of acceptor-like defects in the material (see Figure 3b).

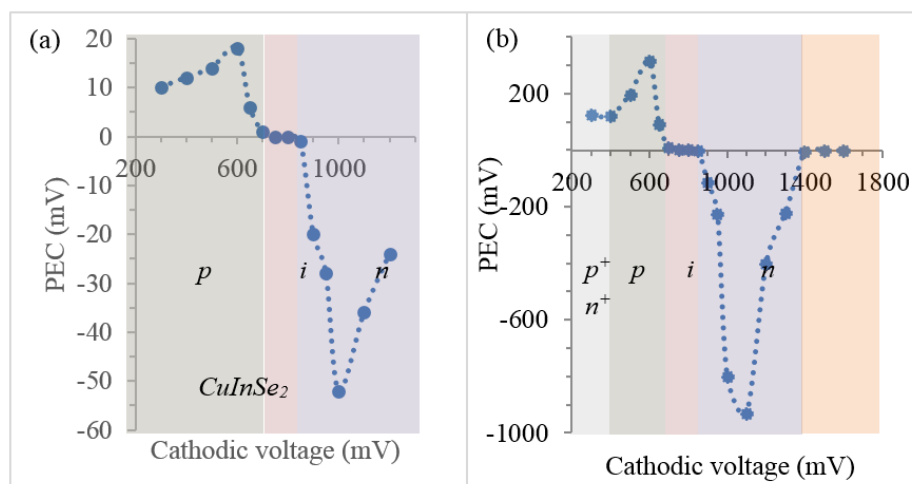


Figure 3. Photoelectrochemical (PEC) cell measurement signal for (a) CuInSe_2 and (b) CuInGaSe_2 with increasing cathodic voltages. Note the ability to grow p^+ , p , i , n , and n^+ materials from the same electrolyte, simply by varying the deposition voltage. Reproduced from [68,70] with permission; Copyright 2004 Sheffield Hallam University.

The effect of cathodic voltage on the elemental composition of binary semiconductors has also been demonstrated and documented in the literature [14,62]. The effect of alteration in the growth voltage on the elemental composition of electroplated materials even for as low as 1 mV step has been documented [29] (see Figure 4).

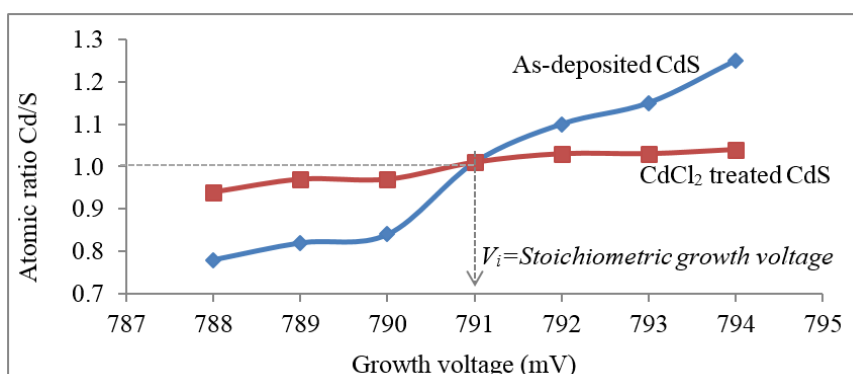


Figure 4. Atomic composition ratios of Cd to S in as-deposited and CdCl_2 treated CdS thin films at different deposition cathodic voltages.

The ease of intrinsic doping and the effect of extrinsic doping of electroplated semiconductor materials have been well established in the literature [65,71]. Due to the simplicity of ED, doping at the ppm level is made possible [65,71,72].

4.1.3. Bandgap Engineering Capability

The control or alteration of the bandgap of materials (with emphasis on semiconductor) is easily achievable in electrodeposition techniques. Typically, this can be achieved by controlling the atomic composition of the elemental component of the semiconductor material. Intrinsically, electrodeposition has the ability to change the composition of growing material by a simple alteration of the cathodic voltage [38,68–70]. An ensuing alteration in the bandgap of grown semiconductor material due to change in the growth cathodic voltage has been documented in the literature [42]. It is well known that an increase in the atomic concentration of Ga in CuInGaSe_2 by increasing the cathodic voltage increases

the bandgap of CuInGaSe_2 . While a reduction in the cathodic voltage of the CuInGaSe_2 results in the reduction of bandgap due to the richness of Cu [42] (see Figure 5). This ability provides the ease of bandgap engineering of semiconductor material such as CuInGaSe_2 between ~ 1.00 and 2.20 eV. Extrinsicly, this observation has also been documented for electroplated binary semiconductor materials such as CdTe doped with Ga [65] amongst others. The bandgap of the resulting doped semiconductor directly affected the incorporated dopant even at the parts per million level [65,71].

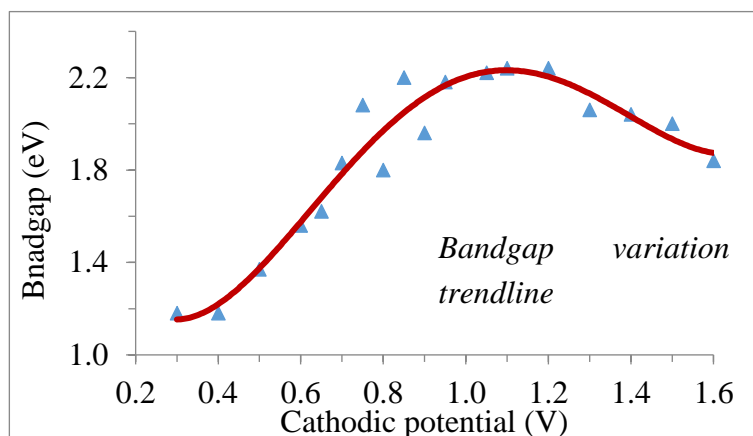


Figure 5. Energy bandgap variation for CuInGaSe_2 as a function of the cathodic voltage.

4.1.4. Low Cost and Simplicity

There are over 14 different and well-established techniques to grow thin-film semiconductor materials [73] which can be broadly categorised under physical or chemical deposition. Physical deposition refers to the technologies in which material is released from a source and deposited on a substrate using thermodynamic, electromechanical or mechanical processes [1,74]. Chemical deposition techniques are accomplished by the utilisation of precursors either in their liquid or gaseous state to produce a chemical reaction on the surface of a substrate, leaving behind chemically deposited thin-film coatings on the substrate. Electrodeposition falls under chemical deposition techniques which can be carried out in an uncontrolled environment and without a vacuum system. The setup for electroplating which is mainly constituted of a computerized potentiostat and hotplate/magnetic stirrer with a cost implication of less than £5000 as compared to other techniques such as the well-established metallorganic chemical vapour deposition (MOCVD) or close space sublimation (CSS) system with a high initial cost implication of about £1 million for a laboratory setup. In addition, these systems have limitations as concerning the materials that can be grown. Furthermore, the relatively low heat energy required during growth and post-growth treatment makes electroplating a more energy-economic deposition technique as compared to a large number of other techniques. More importantly, grown semiconductor layers using cost-effective electroplating techniques are comparable to semiconductor layers grown using highly expensive techniques [29,75], and they all require post-deposition treatments [76,77].

4.1.5. Scalability and Manufacturability

The scalability and manufacturability of electroplating has been demonstrated on an industrial scale by British Petroleum (BP) Solar in the 1980s and 1990s [78,79]. BP Solar manufactured CdTe-based solar cells with a solar panel area $\sim 1 \text{ m}^2$ with a conversion efficiency of $\sim 10\%$ [78,79]. As compared to the laboratory scale setup as shown in Figure 2, scaling up requires a larger tank to contain the electrolyte and multi-plate cathode attached to multiple conducting substrates. The use of larger tanks and multi-plate cathode increases the throughput of deposited layers and an added advantage of electroplating on intricate shapes and designs.

4.2. Weaknesses of Electrodeposition

One of the main disadvantages of electrodeposition includes comparatively low rates of deposition and the need for a conducting substrate as the working electrode in the electroplating setup. Due to this requirement, using conventional characterisation techniques such as the Hall effect to determine the electrical properties of the deposited layers on FTO, for example, will not be possible due to the underlying conducting layer.

4.2.1. Instability of Current Density during Deposition

The control of the electrodeposition process due to the alteration of current density with increasing deposition layer thickness is a challenge (under potentiostatic condition). The electroplating of materials with electrical conductivity levels lower than the primary substrate results in the reduction of current density with a direct relationship with the thickness of the deposited material [80]. This observation is common for both 2E and 3E electroplating configurations, but the applied voltage can vary slightly in 2E configuration.

4.2.2. Control and Regulation of Ions within the Electrolytic Bath

The chemical concentration of ionic species in an electrolytic bath is defined during bath creation, but the control, regulation and measurement of ionic concentration within the electrolytic bath during electroplating remains a challenge. This is as a result of the depletion in the ionic concentration and the inability to gauge/measure the concentration change during and after initial deposition, therefore replenishing the bath with the appropriate chemical concentration becomes difficult and thereby reducing reproducibility tendencies of electroplated layers.

4.2.3. Formation of Solution-Based Complexes

There is a possibility for the formation of complexes within the electrolyte which might be debarring the deposition of an element and/or the co-deposition of a compound [32,33]. This is the case for the deposition of CdTe from aqueous solution containing CdI_2 as the Cd-precursor. The literature shows that due to the formation of Cd-I complexes in aqueous solution, only p-CdTe layers due to Te-richness is possible [32,33]. Unnecessary precipitation removes chemicals from the electrolyte, changing the elemental concentration in the bath.

4.2.4. Extrinsic Doping of Electrolytic Bath by the Electrodes

Control of purity throughout the electrolytic bath lifespan if an electrolytic bath is essential. It is well known that the purity of an electrolytic bath increases with the deposition aging of the bath but there is a tendency of an influx of impurity which might be due to etching, corrosion or dissolution of the electrode. For electrodeposition setup using carbon electrode, there has been observation of increased carbon concentration in deposited semiconductor layers. The incorporation of carbon into the electrolytic bath is due to the deterioration of the anode utilised in the electrolytic cell setup.

4.2.5. Non-Uniformity of Electrodeposited Semiconductor Layers

Due to the unevenness of the underlying conducting substrate such as transparent conducting oxide (TCO), the highest electric field is experienced at the peaks of the rough conducting substrate surfaces. Nucleation starts at the peaks and spreads out through to the lowest valley resulting into layers with columnar nature [14].

4.2.6. Post-Growth Treatment

It is well documented that electrodeposited layers with an emphasis on semiconductors often require post-deposition treatment to further improve their structural, morphological, compositional, and optical properties [81–83]. It is, although, arguable that other semiconductor deposition techniques

such as [77], MOCVD [84], and CSS [85] also require such treatments, as it is evident in the performances of the applications utilised for References [81–83].

Asides semiconductors, other issues such as the influence of different process conditions on mechanical properties of electroplated materials and the control of the integrity of the electroplated layers as it relates to further processing have also been the raised [86,87], but not discussed in this communication.

5. All-Electroplated Photovoltaic Devices

The comparability of the structural, morphological, compositional, optical, and other material properties has been well documented in the literature [29,42,68,88]. Electrodeposited cadmium telluride (CdTe) and copper indium gallium selenide (CIGS) are amongst the commonly used absorber layers in all-electrodeposited photovoltaic applications [57,89]. The versatility of the technique in the growth of all-electrodeposited configurations has been well documented [13,90–92]. The band diagrams of possible n-p and n-n⁺ large Schottky barrier junctions are shown in Figure 6 fabricated using CdS/CdTe configuration. The full characterisation process of both the CdS and CdTe are documented in the literature [40,46]. The electronic properties of the fabricated photovoltaic cells obtained using current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) techniques are summarised in Table 2.

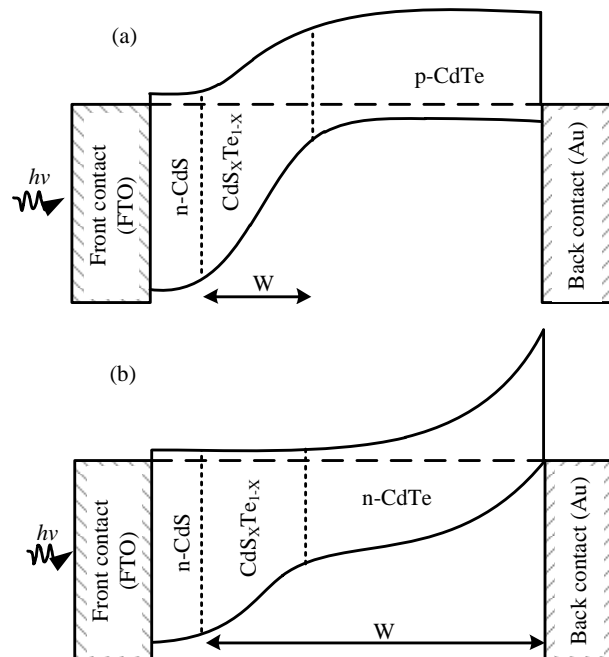


Figure 6. Energy band diagrams representing (a) glass/FTO/n-CdS/p-CdTe/Au and (b) glass/FTO/n-CdS/n-CdTe/Au device configurations.

Table 2. Summary of device parameters obtained from I - V (both under illuminated and dark conditions) and C - V (dark condition) for simple CdS/CdTe-based solar cells grown at different growth voltages in the vicinity of $V_i = 1370$ mV.

Parameters	Values				
CdTe Growth Voltage (mV)	1340	1360	1370	1380	1400
<i>I</i> - <i>V</i> under dark condition					
R_{sh} (Ω)	1016	$>10^5$	$>10^5$	$>10^5$	$>10^5$
R_s ($k\Omega$)	0.21	0.80	0.50	1.43	1.50
\log (RF)	0.4	3.5	3.9	3.3	3.0
I_o (A)	2.5×10^{-5}	3.9×10^{-9}	1.0×10^{-9}	3.2×10^{-9}	5.0×10^{-9}
n	>2.00	1.95	1.86	1.58	1.86
Φ_b (eV)	>0.52	>0.76	>0.81	>0.77	>0.77
<i>I</i> - <i>V</i> under AM1.5 illumination condition					
I_{sc} (mA)	0.53	0.62	0.65	0.82	0.57
J_{sc} ($mA\ cm^{-2}$)	16.88	19.75	20.70	26.11	18.15
V_{oc} (V)	0.23	0.49	0.72	0.60	0.57
Fill factor	0.31	0.46	0.50	0.45	0.48
Efficiency (%)	1.20	4.45	7.50	7.05	4.97
<i>C</i> - <i>V</i> under dark condition					
$\sigma \times 10^{-4}$ ($\Omega\ cm^{-1}$)	1.41		2.85		6.03
N_A or N_D (cm^{-3})	7.74×10^{16}		3.10×10^{14}		9.10×10^{14}
μ ($cm^2\ V^{-1}\ s^{-1}$)	0.01	—	5.74	—	4.14
C_o (pF)	1630		330		370
W (nm)	187.6		926.7		826.5

It is well known that intrinsic CdS is n-type and remains n-type due to the inherent defect as a result of the presence of S vacancies and Cd interstitials in the crystal lattice of the deposited CdS layers [93]. The devices are fabricated by incorporating CdTe deposited at the vicinity of the transition voltage (V_i) from p-type to n-type CdTe or vice versa. Electroplated CdTe can either be p-type (when Te rich) or n-type (when Cd rich) material under as-deposited condition. Retention or transition of electrical conduction type is possible after cadmium chloride treatment. It is noteworthy that the conversion of the electrical conduction type after post-growth treatment may be attributed to the doping effect as a result of the heat treatment temperature, duration of treatment, initial atomic composition of Cd and Te, the concentration of $CdCl_2$ utilised in treatment, defect structure present in the starting CdTe layer, and the material's initial conductivity type as documented in the literature [40,41,94]. Therefore depending on the final electrical conduction type, the possible device configurations are possible, and the analysis of device results must be performed with extreme care.

Table 2 summarises the results of CdS/CdTe solar cells made with CdTe layers grown in the vicinity of $V_i = 1370$ mV. Below the V_i , the CdTe layers are p-type and therefore the devices made are p-n junctions (see Figure 6a). Above the V_i , the CdTe layers are n-type and hence the device structures are n-n⁺ Schottky barrier (see Figure 6b). As shown in Table 2, the devices fabricated with n-CdTe performs better than those made with p-CdTe layers.

CdTe-based devices assuming p-CdTe in CdS/CdTe devices has been documented in the literature [27,95]. But based on recent observations, the incorporation of Cd-rich CdTe absorber layers produce high efficiencies. These effects have been independently observed and reported [96,97] and mainly attributed to the reduced defects in Cd-rich CdTe (the layers are deposited using physical deposition processes).

Using mainly n-CdTe absorber layers, few devices incorporating all-electrodeposited from the SHU group have been documented in the literature and summarised in Table 3.

Table 3. Summary of device parameters obtained from I - V (both under illuminated and dark conditions) and C - V (dark condition) for glass/FTO/ n -CdS/ n -CdTe/Au and glass/FTO/ n -ZnS/ n -CdS/ n -CdTe/Au solar cells.

Properties	Configuration			
	g/FTO/ n -CdS/ n -CdTe/Au (Two-Layer Device)	g/FTO/ n -CdS/ n -CdTe/ p -CdTe/ Au (Three-Layer Device)	g/FTO/ n -CdS/ n -CdTe/ p -CdTe/ Cu-Au (Three-Layer Device)	Glass/FTO/ n -ZnS/ n -CdS/ n -CdTe/Au (Three-Layer Device)
I - V under dark condition				
R_{sh} (Ω)	$>10^5$	$>7.2 \times 10^5$	10^6	$>10^5$
R_s ($k\Omega$)	0.50	0.50	0.92	0.47
\log (RF)	3.9	4.1	3.5	4.8
I_o (A)	1.0×10^{-9}	1.0×10^{-9}	3.16×10^{-9}	1.0×10^{-9}
n	1.86	1.86	1.68	1.60
Φ_b (eV)	>0.81	>0.80	>0.80	>0.82
I - V under 1.5 AM illumination condition				
I_{sc} (mA)	0.65	1.06	1.85	1.07
J_{sc} (mA cm^{-2})	20.70	33.80	58.9	34.08
V_{oc} (V)	0.72	0.73	0.64	0.73
Fill factor	0.50	0.62	0.50	0.57
Efficiency (%)	7.50	15.3	18.5	14.18
C - V under dark condition				
$\sigma \times 10^{-4}$ (Ω cm) $^{-1}$	2.85	—	—	8.82
N_D-N_A (cm^{-3})	3.10×10^{14}	6.67×10^{14}	1.82×10^{14}	7.79×10^{14}
μ ($cm^2 V^{-1} s^{-1}$)	5.74	—	—	7.07
C_o (pF)	330	395	160	280
W (nm)	926.7	—	—	1092.2

6. Conclusions

This work describes electroplating as a robust material deposition technique with wide applications ranging from surface protection to large-area electronics and nano-technology while focusing on semiconductor deposition. The manuscript also reviews the pros and cons of electroplating techniques. The effect of growth parameters such as temperature, pH, stirring rate, precursor, solvent and cathodic voltage, and post-growth heat treatments of the deposited were iterated. The capability of electroplated material to be comparable and possibly superior to semiconductor materials grown using other cash intensive techniques are also highlighted with experimental evidence. Electroplated materials can be applicable in large-area devices such as photovoltaic solar panels and large-area display panels in which intricate shapes are required. Bandgap grading, alteration of elemental composition, and different conductivity type are also possible intrinsically with a change in the cathodic voltage. Other advantages such as columnar growth of nanorods which are tightly packed and normal to the substrate could trigger many new applications in the nanotechnology area.

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