The influence of ZnS crystallinity on all-electroplated ZnS/CdS/CdTe graded bandgap device properties

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The Influence of ZnS Crystallinity on all-electroplated ZnS/CdS/CdTe Graded Bandgap Device Properties

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Abstract

Electrodeposition of zinc sulphide (ZnS) was achieved from electrolytic bath containing zinc sulphate monohydrate ($ZnSO_4 \cdot H_2O$) and ammonium thiosulphate ($(NH_4)_2S_2O_3$) in a two-electrode electroplating configuration. The cyclic voltammetric studies show that ZnS layers can be electroplated between (1350 and 1550) mV. The grown layers were characteristically explored for their structural, optical, morphological and electronic properties using X-ray diffraction (XRD) and Raman spectroscopy, UV–Visible spectrophotometry, scanning electron microscopy (SEM), photoelectrochemical (PEC) cell and DC conductivity measurements respectively. The structural analysis shows that crystalline ZnS can be deposited within a narrow cathodic deposition range between (1420 and 1430) mV. The UV–Visible spectrophotometry shows that the bandgap of both as-deposited and heat-treated ZnS films are in the range of ~(3.70 and 3.90) eV. The SEM shows small grains depicting the wetting property of ZnS. The PEC results show that the electroplated ZnS below 1425 mV is *p*-type and above 1425 mV is *n*-type under both as-deposited and heat treated condition. The DC conductivity shows that the highest resistivity is at the inversion growth voltage (V_i) for the ZnS layers. The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices were fabricated using crystalline-ZnS and amorphous-ZnS buffer layers. The devices were explored using current-voltage (I-V) and capacitance-voltage (C-V) techniques. As expected, devices fabricated with *c*-ZnS show improved device parameters (ideality factor n=1.60, depletion width W=1092 nm, open-circuit voltage V_{oc}=730 mV, short-circuit current density J_{sc}=34.1 mAcm^{-2}, fill factor FF=0.57, conversion efficiency η=14.2%) when compared to device parameters (n=1.85, W=900 nm, V_{oc}=720 mV, J_{sc}=29.9 mAcm^{-2}, FF=0.52, η=11.2%) of these devices fabricated with *a*-ZnS buffer layers.

Keywords: ZnS amorphisation; *n*-ZnS/*n*-CdS/*n*-CdTe, Multilayer graded bandgap, Post-growth treatment; Electroplating of semiconductors.

1 Introduction

Zinc Sulphide (ZnS) from the II-VI group has been well explored for its physical, chemical and electronic properties. The optoelectronic and photovoltaic properties of this material are continually drawing more attention based on its extensive applications in light emitting diodes (LED), sensors and as buffer/window layers in photovoltaic solar cells [1,2]. The use of cadmium sulphide (CdS) as a window layer in cadmium telluride (CdTe)-based solar cells has yielded high photovoltaic conversion efficiency [3,4]. The use of CdS is constrained due to the parasitic absorption of CdS below 520 nm photon wavelengths [5] as a result of its 2.42 eV bandgap. ZnS, on the other hand, possesses a wider bandgap of ~3.7 eV [6] and has been explored as a substitute for CdS [7] but factors such as high lattice mismatch between ZnS and CdTe, the comparatively high conduction band edge of ZnS as compared to CdTe and the high resistivity of ZnS has necessitated the retention of CdS in the ZnS/CdS/CdTe solar cell configuration. Therefore, the inclusion of ZnS provides good wetting property, bandgap grading and allows for the reduction of CdS thickness without an increasing shunt [8] and reducing the parasitic absorption of CdS [5]. The buffer layer, ZnS also provides a better substrate for growing high quality CdS layer.

Several techniques have been recorded in the literature for possible growth of ZnS [9]. However, electrodeposition technique edges others with attributes such as low-cost, simplicity, scalability and the manufacturability of large area solar panels [10]. Literature records that the electrodeposition of crystalline ZnS has been achieved mainly by the inclusion of complexing agents such as ammonia (NH_3) [9], hydrazine (N_2H_4) [11], trisodium citrate ($Na_3C_6H_5O_7$) in the electrolytic bath [12] and glycerol ($C_3H_8O_3$) [13]. The literature on the electrodeposition of ZnS without a complexing agent has been scarce and the reported ZnS layers were structurally amorphous [14,15]. With a view of cost reduction and process simplification, this paper presents in full, the electrodeposition process and characterisation of crystalline ZnS grown without the use of binding/complexing agent in a 2-electrode electrodeposition bath.

2 Experimental details

2.1 Electrolyte and Substrate Preparations

ZnS thin films were electrodeposited cathodically on glass/FTO substrates by potentiostatic technique in which the counter electrode was a high purity graphite rod. Zinc sulphate monohydrate ($ZnSO_4 \cdot H_2O$) of 99.9% purity and ammonium thiosulphate ($(NH_4)_2S_2O_3$) of

98% purity were used as zinc and sulphur precursors respectively. The electrolytic bath was prepared by dissolving 0.2 M $ZnSO_4 \cdot H_2O$ and 0.2 M $(NH_4)_2S_2O_3$ in 400 ml de-ionised (DI) water housed in a polypropylene beaker with a capacity of 500 ml. The polypropylene beaker was placed in an 800 ml glass beaker containing DI water. The DI water contained in the outer glass beaker helps to maintain uniform heating of the electrolyte. The solution was continuously stirred and electro-purified at 1000 mV for ~100 hours to reduce the level of impurity and also to achieve homogeneity of the solution. Afterwards, ZnS layers electrodeposited at different cathodic voltages were characterised. For these set of experiments, the bath temperature was maintained at 30˚C and the pH value of the bath was set to 4.00±0.02 using dilute H_2SO_4 and NH_4OH at the start of deposition. It should be noted that the pH of the electrolytic bath should be maintained within the range of 3.00 and 4.50 due to the formation of white precipitates of sulphur and rapid deposition of ZnS layer with low adhesion to the underlying glass/FTO layer observed.

In this study, two-electrode electrodeposition configuration was utilised for simplicity. Glass/FTO and high purity carbon electrode serve as the working (cathode) and counter electrodes (anode) respectively. The working electrode of sheet resistance ~7 Ω/sq (TEC7) was cut into 3×2 cm^2 and cleaned ultrasonically before deposition. The electrodeposition process was performed using Computerized Gill AC potentiostat. Prior to the deposition of ZnS layers, the cyclic voltammograms of the electrolyte was performed to determine the possible deposition voltage range of ZnS.

The substrates were ultrasonically cleaned for 20 minutes in an ultrasonic bath containing soap solution and rinsed in deionised (DI) water afterwards. The substrates were degreased using both methanol and acetone and rinsed in DI water. Finally, the glass/FTO layers were rinsed in DI water and immediately transferred into the electrolytic bath. Prior to characterisation, the electroplated ZnS layers were rinsed, dried and divided into two halves. One half was left as-deposited and the other half was heat treated at 300˚C for 10 minutes in the air to enhance both their material and electronic properties [15]. Both the as-deposited and the heat treated ZnS layers were characterised afterwards for both their material and electronic properties.

2.2 Material Characterisation

Data on the structural parameters of the ZnS samples such as the phase identification, preferred orientation and estimated crystallite size were acquired using Philips PW 3,710 X'pert diffractometer with Cu-Kα monochromator with a wavelength of 1.54 Å. The X-ray generator pressure and current were accordingly set to 40 kV and 40 mA. Other structural parameters such as the molecular vibration phases of the materials were extracted using Renishaw's Raman spectrometer with an argon laser and an excitation wavelength of 514 nm. The optical properties of the ZnS layers were studied at room temperature within the wavelength range of (200 to 1000) nm using Cary 50 Scan Ultraviolet-Visible (UV–Vis) spectrophotometer. Information on the surface morphology properties of the electroplated ZnS layers was obtained using FEI Nova 200 NanoSEM at a magnification of ×60,000. The conduction type of the grown ZnS layers was determined using photoelectrochemical (PEC) cell measurement. The PEC measurement was achieved by inserting the glass/FTO/ZnS layers into an aqueous solution comprising of 0.1 M sodium thiosulphate ($Na_2S_2O_3$) to form a solid/liquid junction. The PEC cell undergoes measurements under both illuminated and dark conditions for constant time duration. The magnitude of the difference between the measured voltages of the PEC cell under illuminated (V_L) and dark (V_D) shows the suitability of doping density of the semiconducting layer for fabricating electronic devices [16] and the mathematical sign indicates the electrical conduction type of the layer under investigation. The direct current (DC) conductivity measurement was performed to determine the electrical conductivity of the ZnS layers using fully automated Rera Solution I–V measurement system at room temperature.

2.3 Fabrication of all-electroplated ZnS/CdS/CdTe graded bandgap configuration

The effect of the crystalline property of the ZnS layers on glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au graded bandgap photovoltaic device as shown in Figure 1 was evaluated using both current-voltage (I-V) and capacitance-voltage (C-V) techniques. Two sets of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices were fabricated incorporating crystalline *n*-ZnS layers grown at 1425 mV in one and while the other includes amorphous *n*-ZnS layers grown at 1440 mV. Using the electroplating processes discussed in Section 2, ~50 nm thick ZnS was deposited on different glass/FTO layers at 1425 mV and 1440 mV respectively. The layers were heat-treated at 300°C for 10 minutes in air and allowed to air-cool prior to the deposition of CdS. It should be noted that the other processing steps asides the deposition of ZnS from different cathodic voltage are all similar.

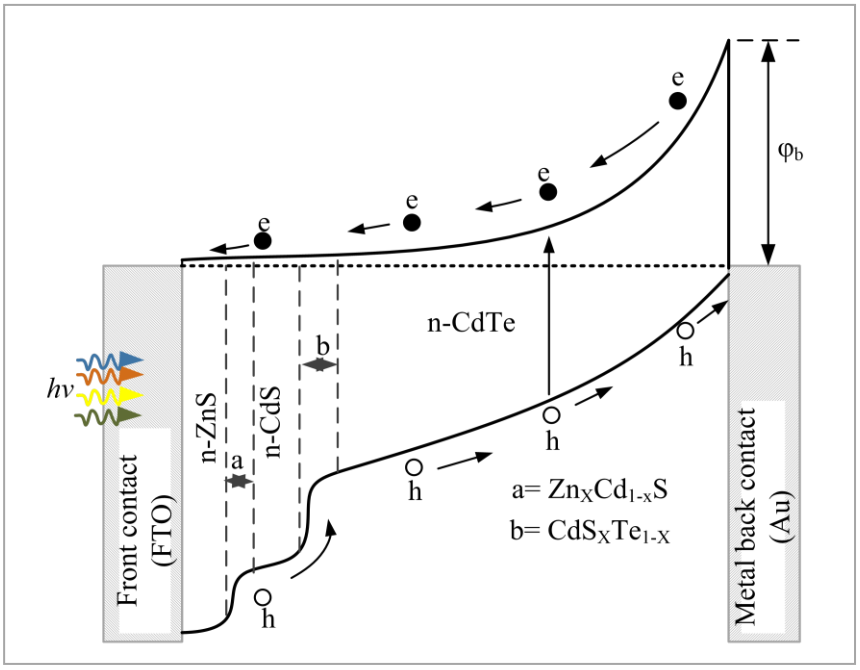

Figure 1: A typical graded bandgap diagram of glass/FTO/*n*-ZnS (~50 nm)/*n*-CdS(~65 nm)/*n*-CdTe (~1150 nm)/Au device configuration (not to scale).

Cadmium sulphide (CdS) layers with a thickness of ~65 nm were electroplated at 1200 mV on the glass/FTO/*n*-ZnS layer from an aqueous electrolyte. The CdS electrolytic bath contained 0.3M cadmium chloride hydrate ($CdCl_2 \cdot xH_2O$) with a purity of 99.99% and 0.03M ammonium thiosulphate ($(NH_4)_2S_2O_3$) with 98% purity in 400 ml of DI water. The bath conditions such as the temperature and the stirring rate were maintained at 85°C and ~300 rpm respectively, while the pH was set to 2.50±0.02. The resulting glass/FTO/*n*-ZnS/*n*-CdS layers were $CdCl_2$ treated and annealed at 400 °C for 20 minutes in the air. Afterwards, the layers were air-cooled and rinsed before the deposition of the *n*-CdTe layer.

The cadmium telluride electrolytic bath utilised for the deposition of ~1150 nm thick *n*-CdTe layers on the glass/FTO/*n*-ZnS/*n*-CdS contained 1.5M cadmium nitrate tetrahydrate ($Cd(NO_3)_2 \cdot 4H_2O$) of 99.0% purity and 0.0002 M tellurium dioxide (TeO_2) in 400 ml of DI water. The electrolytic bath temperature, pH and the stirring rate were maintained at 85°C, 2.00±0.02 and ~300 rpm. The cathodic voltage for the deposition of the *n*-CdTe layers was maintained at 1400 mV. The resulting glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were $CdCl_2$+$Ga_2(SO_4)_3$ treated and annealed at ~430 °C for 20 minutes in the air [17,18]. Afterwards, the layers were air-cooled, rinsed and dried in a stream of nitrogen gas. The full details of the growth and characterisation of both the CdS and CdTe layers are reported by authors' group in the literature [19,20].

Before the metallisation process, the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were etched using both acid and alkaline-based solutions in quick successions to improve the metal/semiconductor contact [21]. The acid etchant is an aqueous solution containing $K_2Cr_2O_7$ and diluted H_2SO_4, while the alkaline etchant is an aqueous solution containing NaOH and $Na_2S_2O_3$. The etching was performed by dipping the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers into the acid etchant for 2 seconds, rinse in deionised water and dipped into the alkaline etchant (maintained at 60 °C) for 120 seconds. The glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers were rinsed in deionised water afterwards, dried in a stream of nitrogen gas. The layers were transferred directly into a high vacuum metallisation system (Edward Auto 306) to deposit 100 nm thick Au contacts of 2 mm diameter on the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe layers.

3 Results and Discussions

3.1 Cyclic Voltammetry

Figure 2 shows a typical cyclic voltammogram of an aqueous solution of 0.2 M $ZnSO_4 \cdot H_2O$ and 0.2 M $(NH_4)_2S_2O_3$ in 400 ml of DI water during the forward and reverse cycle between the cathodic voltages 0 and 2000 mV. The scanning rate was fixed at 3 mVs^{-1} with the bath temperature, stirring rate and pH set to 30˚C, 300 rpm and 4.00±0.02 respectively.

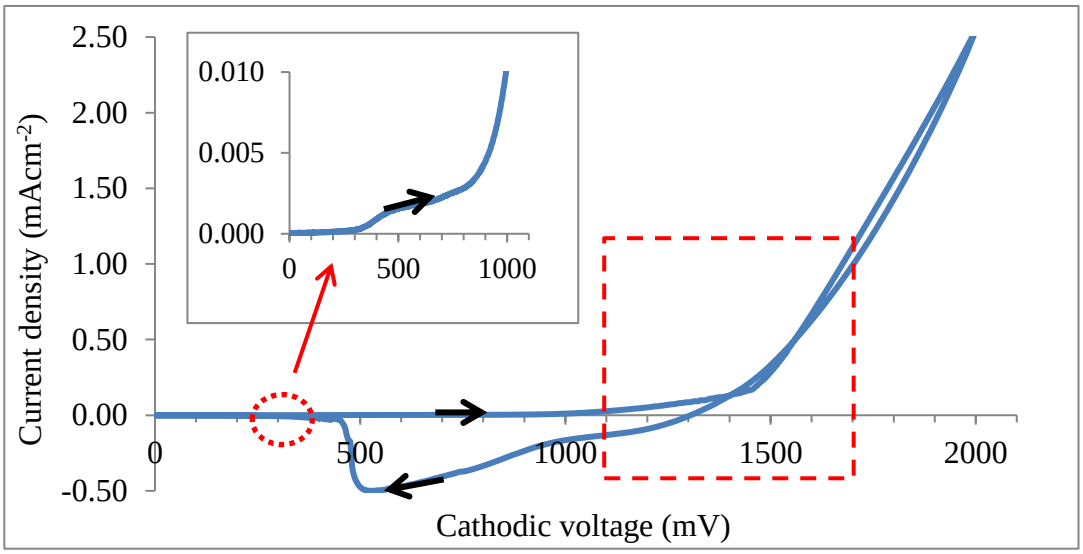

Figure 2: Cyclic voltammogram for the electrolyte containing 0.2 M $ZnSO_4 \cdot H_2O$ and 0.2 M $(NH_4)_2S_2O_3$ in 400 ml of DI water at ~30˚C and pH 4.00±0.02. The inset is the expanded forward cycle between (0 and 1100) mV.

The growth temperature was set to 30˚C to avoid vigorous sulphur precipitation which occurs at a higher temperatures and amorphous ZnS deposition which occurs at a lower temperature. Based on the standard reduction potential values of both Zn^{2+} and S^{2-} with E˚=-0.762 V and E˚=0.449 V respectively with respect to standard H_2 electrode, sulphur deposits first at ~300 mV, followed by the deposition of zinc at ~1100 mV in the forward cycle. On the reverse cycle, the dissolution of zinc starts at ~1300 mV, followed by sulphur at ~540 mV. It was deduced that between the cathodic voltage range of (1100 and 1700) mV, ZnS can be achieved as either S-rich, stoichiometric or Zn-rich ZnS. The fairly stable current density of ~1.50 $mAcm^{-2}$ is observable between (1320 and 1500) mV cathodic voltages. ZnS layers were grown within this range at the step of 50 mV and characterised to identify the approximate growth voltage in which stoichiometric/near stoichiometric ZnS can be achieved. On this initial experimentation using only XRD analysis, crystalline ZnS was observed only at 1420 mV. Therefore, surrounding cathodic potentials were explored at the steps of 10 mV to identify the optimum growth voltage. The final electrochemical equation for the formation of ZnS at the cathode can be written as equation (1).

$$Zn^{2+} + 2e^{-} + S \rightarrow ZnS \qquad (1)$$

3.2 Structural Analysis

A typical XRD analysis for both as-deposited and heat treated ZnS at 300˚C for 10 minutes is shown in Figure 3 (a) and Figure 3 (b) respectively. As observed in Figure 3 (a), ZnS layers grown at cathodic voltages outside the range of 1410 to 1430 mV show an amorphous behaviour which might be as a result of the growth technique, the cathodic voltage and the ensuing elemental composition [22], temperature of growth [23], and the absence of binding/complexing agent in the electrolytic bath [24]. For the ZnS layers grown at 1430 mV, peaks associable with ZnS(111)C, ZnS(110)H and ZnS(220)C were observed at 2θ=~29.2˚, ~47.5˚ and ~48.2˚ [25] respectively. Conversely, the ZnS layers grown at 1420 mV show peaks associable with ZnS(101)H, ZnS(002)H at 2θ=~30.8˚ and (002)H at 32.16˚ respectively. An inclusion of ZnO(101)H and unreacted Zn(101)H phase were also observed at 2θ=36.18˚ and 42.88˚ for most of the deposited layers across the explored cathodic voltage range. The presence of ZnO might be as a result of the aqueous solution utilised and/or the oxidisation of the ZnS surface in air.

With regards to the XRD spectra of heat treated ZnS layers shown in Figure 3 (b), amorphisation of all the crystalline ZnS layers grown at all the explored cathodic voltages

was observed. For the ZnS layers grown at 1430 mV, a retention of ZnS(111)C peak was obserced at 2θ=~29.0˚ with reduced of the peak intensity (see Figure 3 (b) and Figure 4).

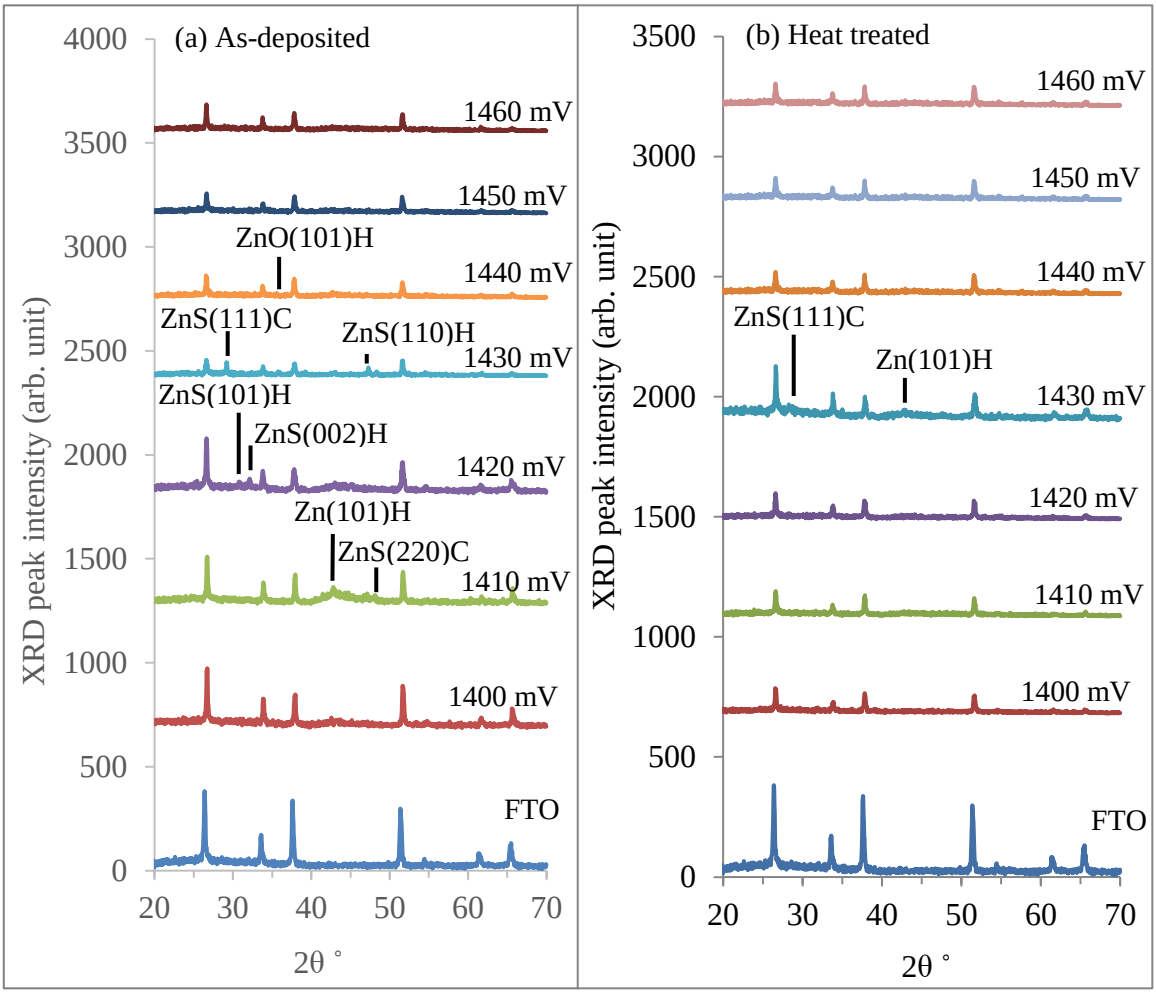

Figure 3: XRD patterns for ZnS layers grown between 1400 and 1460 mV cathodic voltages for (a) as-deposited and (b) heat treated at 300˚C for 10 minutes.

Figure 4 shows the XRD spectra plotted in log-scale in order to identify all peaks. The slight shift towards lower 2θ angle of the ZnS (111)C after heat treatment indicates compressive stress formation in the deposited film and also possible change in chemical composition [26,27].

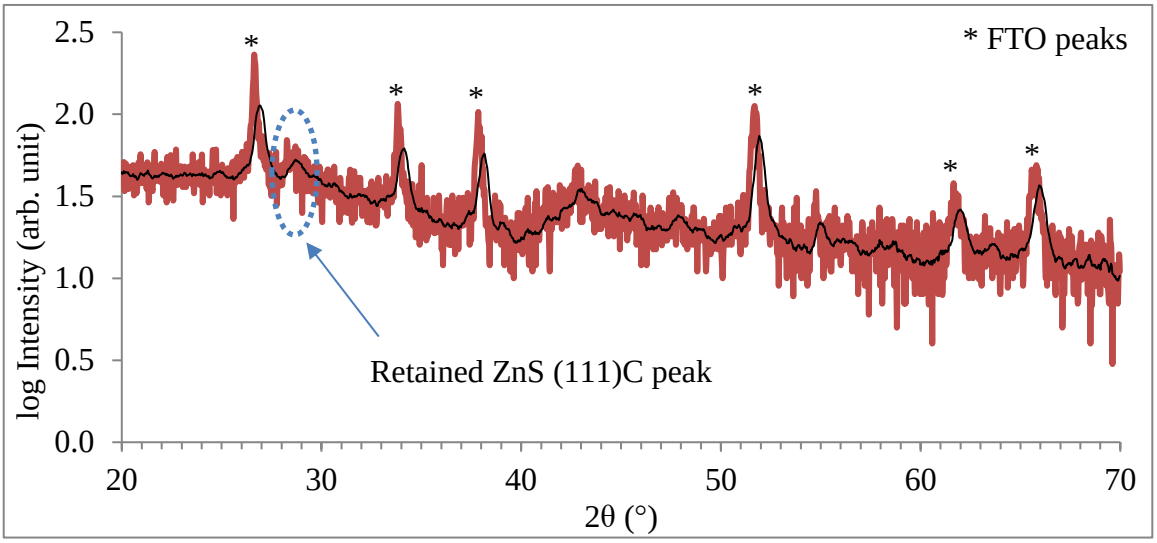

Figure 4: XRD patterns of heat treated ZnS layer grown at 1430 mV plotted in log-scale.

The amorphisation of the crystalline ZnS grown at 1430 mV might be due to high defect concentration [13], elemental composition, oxidation, and the sublimation of the layer leading to the degradation of the ZnS layer. The crystallite size was calculated using the Scherrer's formula (see equation (2)), where θ is the Bragg angle, β is the full-width-at-half-maximum (FWHM) of the diffraction intensity in radians and λ is the wavelength of the X-rays used (1.54 Å) and the XRD data is summarised in Table 1. The highest crystallite size of ~66 nm was observed for the ZnS layers grown at 1430 mV. After heat treatment, a reduction in the crystallite size along the same plane was observed for the ZnS layers grown at 1430 mV due to deterioration of the ZnS layer [13]. This observation can be attributed to the re-crystallisation of ZnS resulting in the competing phases of hexagonal and cubic ZnS. Another possibility is the oxidation of ZnS surface to give ZnO with competing crystalline phases resulting to collapse of the ZnS crystallinity. The extracted XRD data from this ZnS material work matches the Joint Committee on Powder Diffraction Standards (JCPDS) reference file number 00-05-566, 00-05-492 and 00-36-1450 for ZnS, 00-036-1451 for ZnO and 00-004-0831 for Zn. The presence of the narrow crystalline range of electrodeposited ED-ZnS and the amorphisation of the ED-ZnS layers is very different to the ZnS layers electroplated from the bath incorporating complexing agents [9,11,12] with improvement in the ZnS layer crystallinity with the increasing complexing agent concentration [24].

$$D = \frac{0.94\lambda}{\beta \cos\theta} \qquad (2)$$

Table 1: The XRD analysis of ZnS layers grown at cathodic voltages of 1420 mV and 1430 mV under both as-deposited and the heat treated conditions.

Sample	2θ (°)	d-spacing (Å)	FWHM (°)	Crystallite size (nm)	Plane (hkl)	Assignments
AD						
1420 mV	32.16	2.8	0.2598	33.3	(200)	ZnS cubic
1430 mV	29.22	3.05	0.1299	66.0	(111)	ZnS cubic
HT						
1430 mV	29.0	3.12	0.3031	28.3	(111)	ZnS cubic

Figure 5 (a) and Figure 5 (b) show the Raman spectra of ~600 nm thick ZnS layers grown on glass/FTO substrates at 1420 mV, 1430 mV and 1440 mV cathodic voltages under as-deposited and heat treated conditions respectively. Raman peaks associated with ZnS were observed at 147 cm^{-1} and 217 cm^{-1} which are identified as 2TA and 2LA optical mode phonons. With respect to the as-deposited ZnS layers (Figure 5 (a)), sharp Raman peaks were observed at 147 cm^{-1} and 217 cm^{-1} for the layers grown at 1420 mV and 1430 mV while broad peaks were observed for the ZnS layers grown at 1440 mV. It should be noted that the ZnS layers grown at 1440 mV is similar to all the other explored ZnS layers (1400 to 1460) mV with the exception of 1420 mV and 1430 mV grown layers. As documented in the literature, the broadness of the observed peaks under as-deposited condition suggests the amorphous nature of the most of the ZnS layers which are in accord with the submissions made in the XRD section (see Section 3.2a) for ZnS [28,29]. While the observed broadening of the peaks at 147 cm^{-1} and 217 cm^{-1} of the ZnS layers grown at 1420 mV and 1430 mV after heat treatment shows the amorphisation of the layers due to the randomisation of the crystal structure [30,31]. In addition, possible oxidation of the ZnS surface resulting into competing crystalline phases of ZnS and ZnO may occur and result to collapse of the crystalline structure.

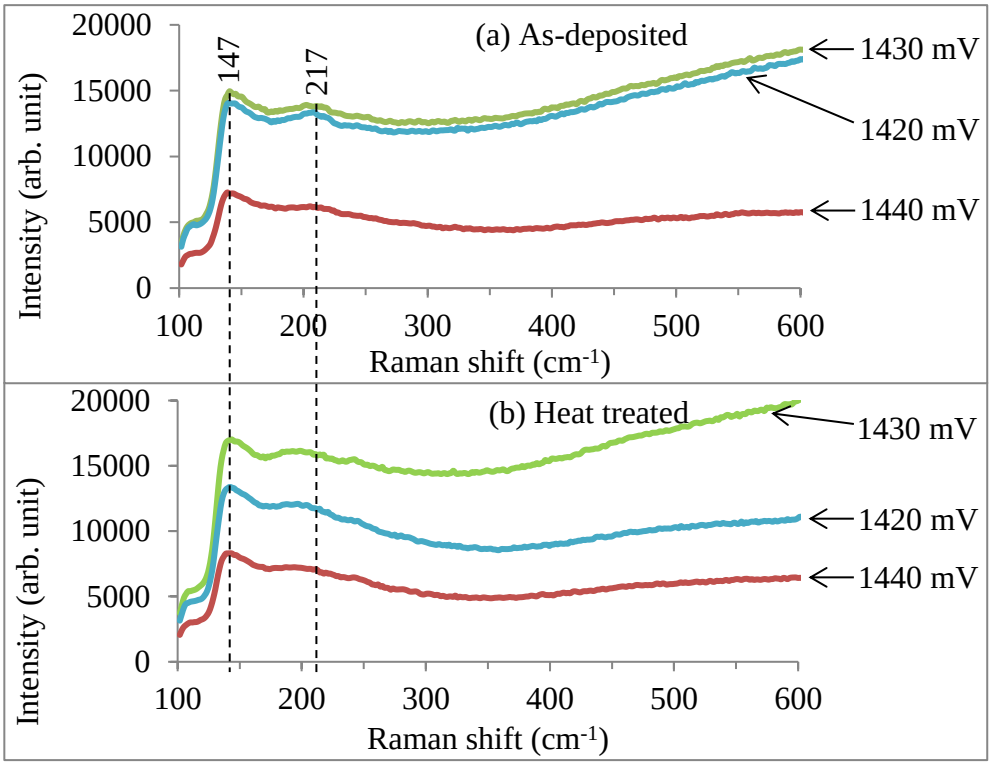

Figure 5: Raman spectra of (a) as-deposited and (b) heat treated ZnS thin-films grown between (1420 and 1440) mV.

3.3 Optical Analysis

Figure 6 (a) shows the optical absorbance measurement of ~200 nm thick ZnS layers grown between the (1410 and 1440) mV cathodic voltage under the as-deposited condition and Figure 6 (b) after heat treatment at 300°C for 10 minutes. The absorbance squared (A^2) was plotted against the energy of photons and the extrapolated straight-line section of the graph to the energy of photons axis (at $A^2=0$) gives an estimate of the bandgap energy. With respect to the as-deposited ZnS layers grown between (1410 and 1440) mV (Figure 6 (a)), the observed bandgap ranges between (3.70 and 3.85) eV. After heat treatment, an increase in the observed bandgap ≥3.84 eV and a reduction in the bandgap range between (3.84 and 3.94) eV were observed. The deviation of the observed bandgap energy from that of the bulk cubic-ZnS of ~3. 70 eV [6] might be due to the incorporation of hexagonal ZnS which is known to have a bandgap of ~3.90 eV [32–34] (see Section 3.2). The non-conformity of deposited ZnS with 3. 70 eV bandgap norm has also been observed for layer grown from other techniques such as chemical bath deposition (CBD) [35] and metal organic vapour phase epitaxy (MOVPE) [36] amongst others.

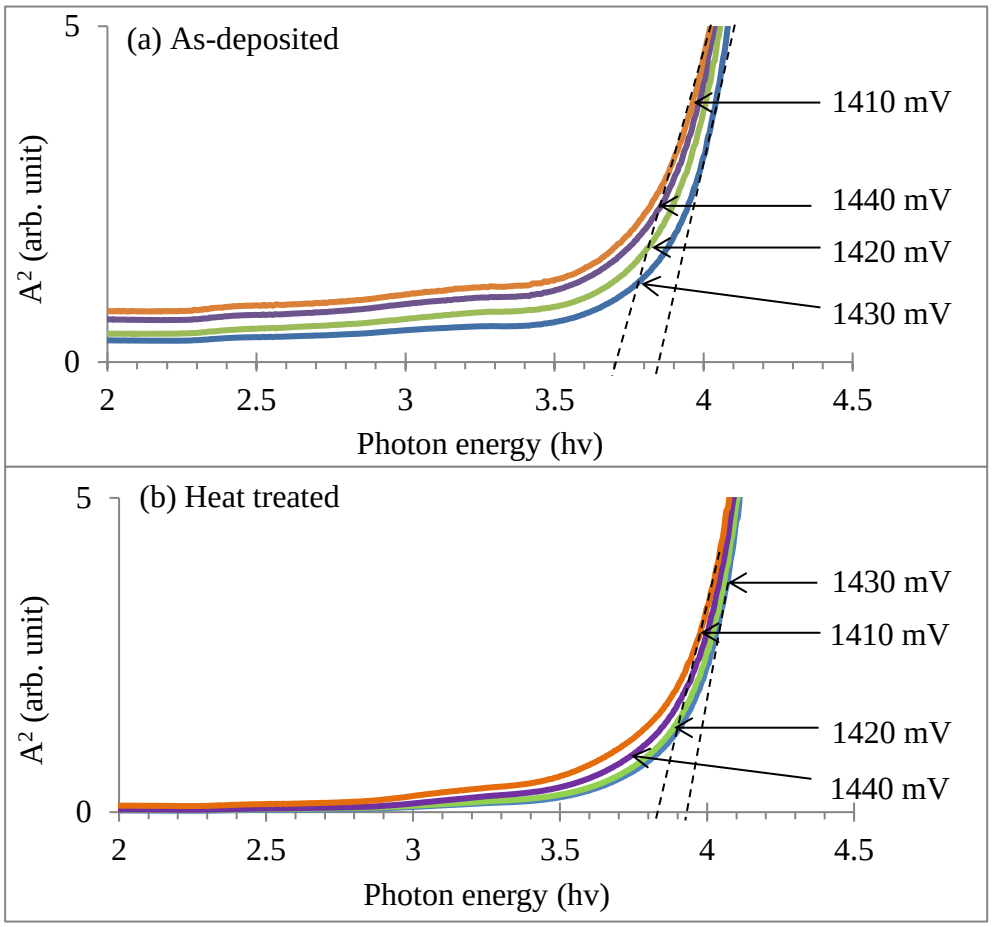

Figure 6: Optical absorption spectra for electrodeposited ZnS thin-films between voltage range 1410 to 1440 mV for (a) as-deposited, and (b) heat treated ZnS at 300˚C for 10 minutes in air.

Figure 7 (a) shows the transmittance of 150 nm thick ZnS layers grown between (1410 and 1440) mV under as-deposited and Figure 7 (b) after heat treatment at 300°C for 10 minutes. Comparatively, a slight increase in transmittance was observed for all the explored ZnS layers after heat treatment. It is noteworthy that all the samples show transmittance above 50% for wavelengths larger than 335 nm with the highest transmittance of ~80% observed for the layers grown at 1420 mV and 1430 mV. The ZnS layers grown at 1420 mV and 1430 mV shows high optical property suitable for a buffer layer in a photovoltaic device configuration with the negligible parasitic absorbance of incident photon to the cell.

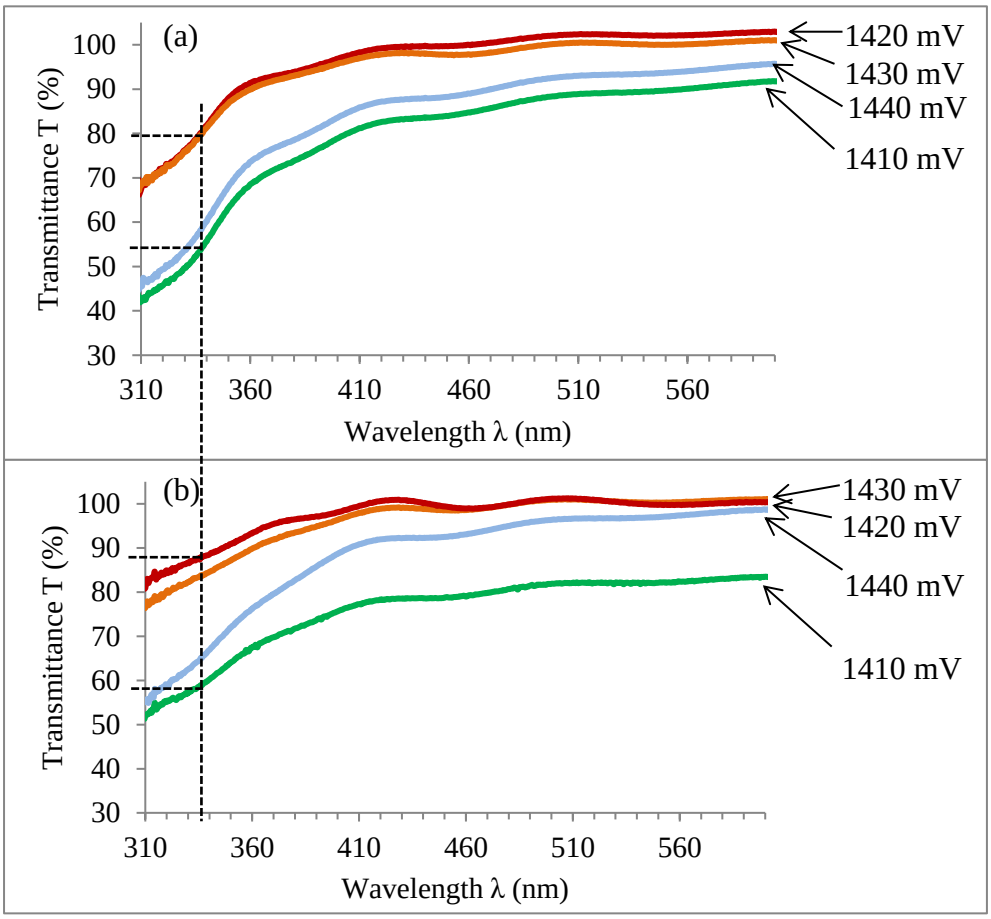

Figure 7: Optical transmittance spectra for electrodeposited ZnS thin-films between voltage range 1410 to 1440 mV for (a) as-deposited, and (b) heat treated ZnS at 300˚C for 10 minutes in air.

3.4 Morphological and Compositional Analysis

Figure 8 (a), Figure 8 (b) and Figure 8 (c) show the SEM micrographs of as-deposited ZnS layers grown at 1410 mV, 1430 mV and 1440 mV respectively, while Figure 8 (d), Figure 8 (e) and Figure 8 (f) show their respective heat treated micrographs. For this set of experiments, the ZnS layers utilised were ~200 nm thick grown on glass/FTO. For the explored cathodic voltages range between (1410 to 1440) mV under both the as-deposited and heat treated conditions, full coverage of the underlying glass/FTO substrate was observed. A slight increase in the grain sizes of the as-deposited ZnS layers ranging from ~(100 to 380) nm to ~(120 to 400) nm after heat treatment was observable. Further to this, it appears that grains of the ZnS layers grown at 1430 mV and 1440 mV coalesce after heat treatment.

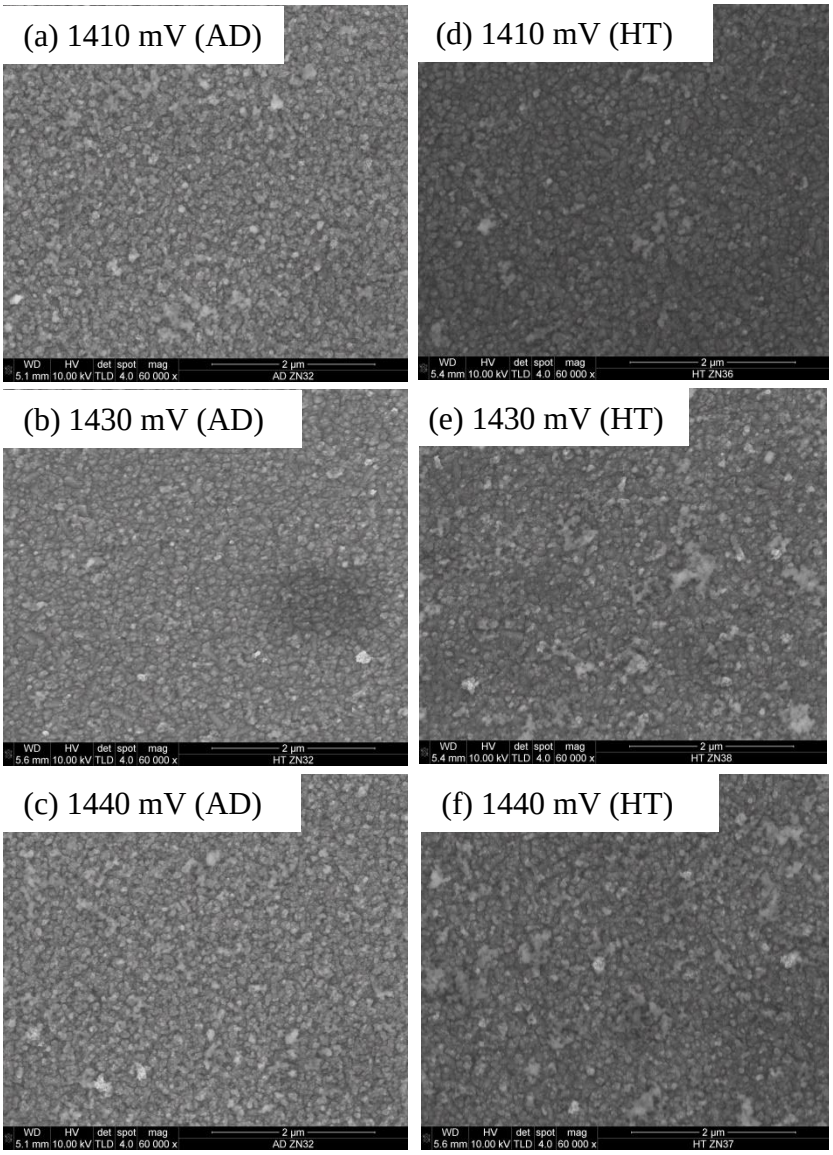

Figure 8: SEM micrographs of as-deposited (AD) and heat treated ZnS layers grown between (1420 and 1440) mV.

3.5 Electrical Property Analyses

The plot of the PEC signals against the cathodic voltage range of (1360 to 1480) mV from which the ZnS layers were grown is shown in Figure 9. It should be noted that prior to PEC measurement, a semiconductor with a known conduction type was measured to calibrate the PEC cell measurement system. From observation, both the as-deposited and the annealed ZnS layers show a similar trend with a transition from *p*-ZnS to *n*-ZnS between (1420 and 1430) mV. As documented in the literature, the richness of sulphur in ZnS results in the *p*-type conductivity of ZnS, while the *n*-type conduction of ZnS is associated with zinc-richness [15]. It should be taken into consideration that the transition cathodic voltage from *p*- to *n*-type conduction type is the voltage from which stoichiometric ZnS is obtainable with 1:1

atomic ratio of Zn to S in the layer. Based on the observations made on the PEC result, it can be inferred that the crystallinity ZnS layers can be grown close to the transition cathodic voltage as discussed in Section 3.2.

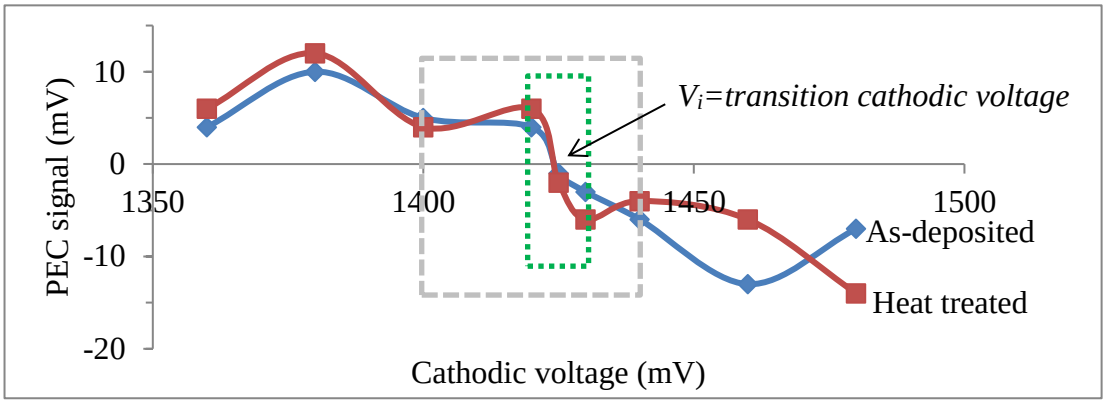

Figure 9: PEC signals for ZnS layers grown between 1360 mV and 1480 mV cathodic voltages under both as-deposited and heat treated conditions.

Consequently, there is a possible few millivolts (mV) shift in either direction from time to time due to bath replenishment with either Zn^{2+} or S^{2-} ions. It is however important that the transition (intrinsic) cathodic voltage (V_i) is known as it serves as a point of reference. Furthermore, the observed PEC signal magnitude is comparatively low as compared to the other electrodeposited semiconductors materials [37,38]. This observation could be attributed to the wide bandgap nature of ZnS resulting in the transmission of most of the visible light [15,39] with low absorption.

Prior to DC conductivity measurement, Ohmic contacts were formed on both the *p*-ZnS and *n*-ZnS layers by respectively depositing 100 nm gold (Au) or indium (In) on the ZnS layers to form glass/FTO/*p*-ZnS/Au or glass/FTO/*n*-ZnS/In. The ZnS layers utilised for the DC conductivity measured were ~1 µm thick each. The resistivity ρ was estimated using equation (3) where R is the resistance, A is the contact area, L is the film thickness and σ is the electrical conductivity. The electrical resistance (R) of the structure was calculated from the Ohmic I-V data obtained under dark condition.

$$\rho = \frac{RA}{L} = \frac{1}{\sigma} \qquad (3)$$

Figure 10 shows the graphical plot of conductivity against the growth voltage of ZnS layers after heat treatment. The large bandgap of ~(3.70-3.90) eV is an indication of the electrical property of ZnS tending towards insulation. A noticeable trend showing a gradual reduction

in electrical conductivity value from the ZnS layers grown at 1360 mV towards the ZnS layer grown at 1425 mV was observed in Figure 10. Conversely, a gradual increase in the electrical conductivity was observed with increasing cathodic voltage at which the ZnS layers were grown.

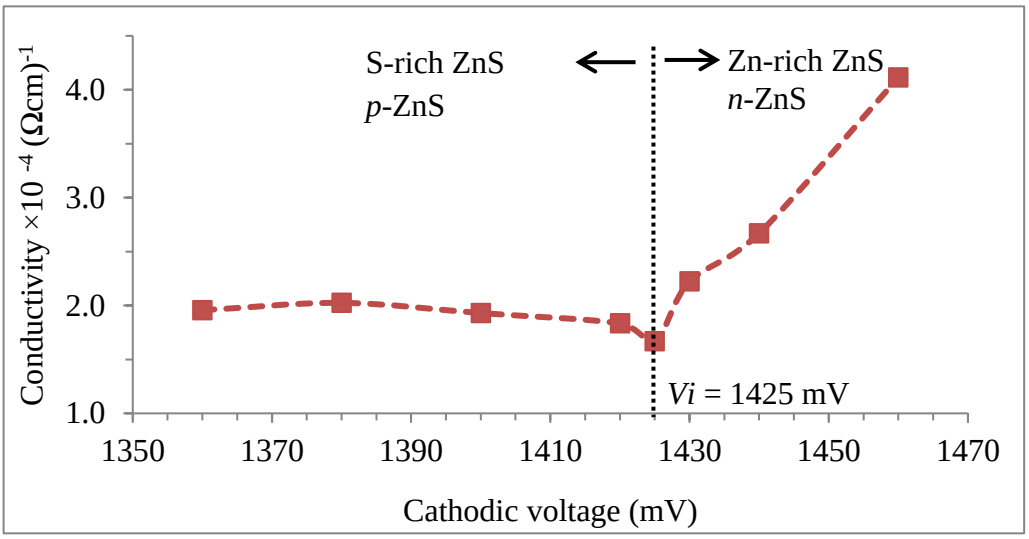

Figure 10: A typical graph of electrical conductivity against growth voltage of heat treated ZnS layers.

In relation to the cathodic voltage-dependent deposition sequence as discussed in Section 3.1, the observed trend in Figure 10 can be attributed to the deposition of S-rich ZnS layers at cathodic voltages lower than ~1425 mV and the increasing Zn-richness of the ZnS layers grown above 1425 mV. It is clear that the ZnS layers grown close to 1425 mV show relatively lowest conductivity due to the stoichiometric and the intrinsic nature of the ZnS layers grown since practically all valence electrons are engaged in bonding.

3.6 Solar cell device characterisation

The I-V measurements for the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices incorporating both *c*-ZnS and *a*-ZnS buffer layers were performed under both dark and AM1.5 illuminated condition. Under dark condition, parameters derived include shunt resistance (R_{sh}), series resistance R_s, rectification factor *RF*, reverse saturation current I_o, ideality factor *n*, and the potential barrier height ϕ_b. The effective Richardson constant (*A**) for CdTe was calculated to be 12 $Acm^{-2}K^{-2}$ using equation (4), where m^* is the effective electron mass and *h* is the Planck's constant (6.626×10^{-30} cm^2kgs^{-1}). Depending on the conductivity type of the semiconductor, the effective electron mass can be denoted as m_e^* or m_p^* for *n*-type and *p*-type semiconductor materials respectively.

$$A^* = \frac{4\pi m^* k^2 q}{h^3} \qquad (4)$$

From the I-V measurement under the illuminated AM1.5 condition for the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices, parameters such as short-circuit current density J_{sc}, open-circuit voltage V_{oc}, fill-factor *FF* and efficiency η were derived.

Figure 11 (a-b) show the I-V curves of glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device incorporating *c*-ZnS [18] or *a*-ZnS buffer layers under dark condition plotted in linear-linear and log-linear scales, while Figure 11 (c) shows the I-V curves plotted under illuminated AM1.5 condition. The obtained electronic parametric quantities of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au photovoltaic cells are summarised in Table 2.

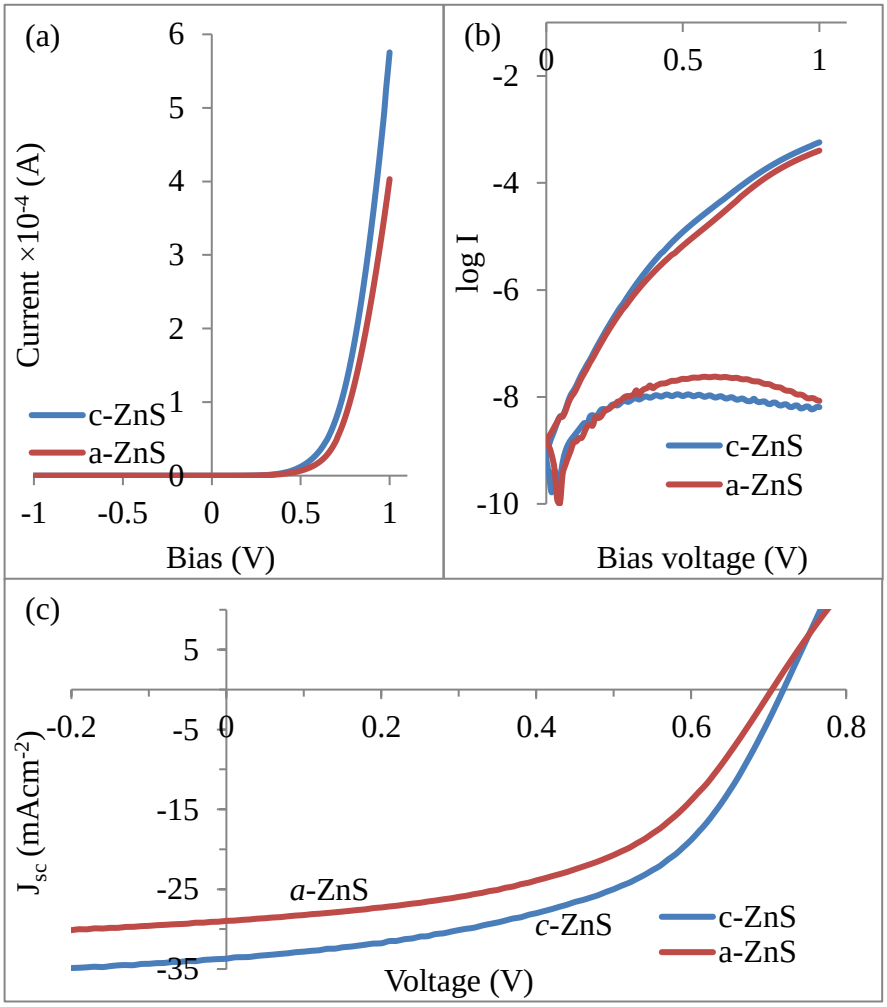

Figure 11: I–V characteristics of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au devices incorporating c-ZnS or a-ZnS buffer layers plotted under dark condition plotted in (a) Linear-linear scale (b) Log-linear scale and (c) I-V plotted under illuminated AM1.5

With respect to the observation in Figure 11 (a-b) and the dark I-V section in Table 2, the significantly high R_{sh} values recorded for the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices

indicate the absence of shunt paths which might be as a result of the ZnS buffer layer integrated into the device even with the thinning down of the CdS layer to 65 nm [8]. This indicates the provision of a good substrate for CdS and CdTe layers to grow with improved material qualities. High R_{sh} values in photovoltaic devices have also been associated with the quality of the deposited semiconductor layer with regards to the absence of gaps, voids and high dislocation density in the electroplated semiconductor material [40]. Both the R_{sh} values of the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au incorporating both *c*-ZnS and *a*-ZnS buffer layers are comparable. This indicates the provision of a good substrate for CdS and CdTe to grow with improved material qualities.

Considerably high R_s values of 470 Ω and 637 Ω for both devices respectively incorporating *c*-ZnS and *a*-ZnS buffer layers were observed which do have an adverse effect on all solar cell parameters. For both of the devices under consideration incorporating *c*-ZnS and *a*-ZnS buffer layers, outstanding Rectification Factor *RF* with values exceeding 10^4 was observed. As documented in the literature, RF values exceeding 10^3 is considered as one of the characteristic property of high-efficiency photovoltaic cell [10]. Additionally, the observed ideality factor *n* within the 1.00 and 2.00 range, signifies that both thermionic emission and recombination & generation (*R&G*) processes taking place in parallel are the dominating current transport mechanism of the devices [2,41,42]. For devices with n>2.00, the current transport mechanisms are associated with thermionic emission, *R&G* and tunnelling of electrons with high energy through the barrier height [43] resulting in the under estimation of the barrier height ϕ_b. High n>2.00 may also be dependent on the doping levels on both sides of the junction and on the interface charges of an hetero-junction device structure [44]. It should be taken into consideration that the estimated potential barrier height ϕ_b of >0.82 eV and >0.79 eV for respective devices incorporating *c*-ZnS and a-ZnS buffer layers may be lower than the actual value due to the influence of their respective high ideality factor values of 1.60 and 1.85. Based on the parameters obtained from the dark I-V data, it could be said that the dominance of *R&G* in the devices incorporating *a*-ZnS is comparatively high to that of the device incorporating *c*-ZnS layers. This indicates the high electronic properties of both the CdS and CdTe layers grown on crystalline ZnS buffer layer.

Table 2: Summary of device parameters obtained from I-V (both under illuminated and dark conditions) and C-V (dark condition) for crystalline ZnS (*c*-ZnS) and amorphous ZnS (*a*-ZnS) incorporated in glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au solar cell.

ZnS structure / Parameters	*c*-Zns	*a*-ZnS
I-V measurement under dark condition		
R_{sh} (Ω)	$>10^6$	$>10^6$
R_s (Ω)	470	637
log (R.F.)	4.8	4.2
I_o (A)	1.0×10^{-9}	1.2×10^{-9}
n	1.60	1.85
Φ_b (eV)	>0.82	>0.79
I-V measurement under AM1.5 illuminated condition		
I_{sc} (mA)	1.07	0.94
J_{sc} (mAcm^{-2})	34.08	29.94
V_{oc} (mV)	730	720
Fill-factor	0.57	0.52
Efficiency (%)	14.18	11.21
DC and C-V measurements under dark condition		
$\rho\times10^3$ (Ω.cm)	1.13	1.13
C_o (pF)	280	340
V_{bi} (eV)	1.10	1.07
(N_D-N_A) (cm^{-3})	7.79×10^{14}	9.52×10^{14}
(E_C-E_F) eV	~0.17	~0.21
W (nm)	1092.2	899.5
$\mu_\perp$ (cm^{2}V^{-1}s^{-1})	7.07	5.78

With respect to Figure 11 (c) and the AM1.5 illuminated condition section of Table 2, parameters derived include the short-circuit current density J_{sc}, open-circuit voltage V_{oc}, fill factor *FF*, and the conversion efficiency η. For the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices incorporating *c*-ZnS buffer layers, the derived parameters include the J_{sc}=34.08 mAcm^{-2}, V_{oc}=730 mV, *FF*=0.57 and the η=14.18%. While the derived parameters for the devices incorporating *a*-ZnS include J_{sc}=29.94 mAcm^{-2}, V_{oc}=720 mV, *FF*=0.52 and the η=11.21%. All four parameters have improved when *c*-ZnS buffer layer is used. For both devices, the observed J_{sc} values are higher than the Shockley–Queisser limit for single *p*-*n* junction [45]. The high J_{sc} observation is attributable to the multilayer graded bandgap configuration [46] utilised in this work. This observation have also been documented and backed by the literatures for inorganic [47,48] and hybrid [49] solar cell technologies. Theoretically, it has been proved that graded bandgap solar cell configurations are capable of

attaining a conversion efficiency of ~38% under AM1.5 [50,51] as compared to the 23% of single *p-n* junction solar cells [45]. Harvesting more photons, the contribution of "impurity PV effect" and "impact ionisation" observed in the graded bandgap devices as described in Ref [47,48] can be the explanation for this increase in J_{sc} values.

Figure 12 shows the Mott-Schottky plots of C^{-2} against V for the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices incorporating *c*-ZnS or *a*-ZnS layers measured under dark condition. The derived parameters from the C-V and C^{-2}-V plots include capacitance at zero bias C_o, Fermi level position (E_C-E_F), built-in potential V_{bi}, doping concentration of the material N_D-N_A, barrier height Φ_b, depletion layer width at zero bias W and charge carrier mobility $\mu_{\perp}$. Pertaining to Figure 12, a slightly stable and similar capacitance of ~280 pF and 340 pF for devices incorporating *c*-ZnS or *a*-ZnS layers were observed from the reverse bias region of -1 V, through the C_o up to ~0.5 V in the forward bias region. The constant capacitance signifies that the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au devices are fully depleted in which the depletion width W is larger or comparable to the device thickness of ~1.0 µm at reverse bias region up to ~0.5 V in the forward bias region.

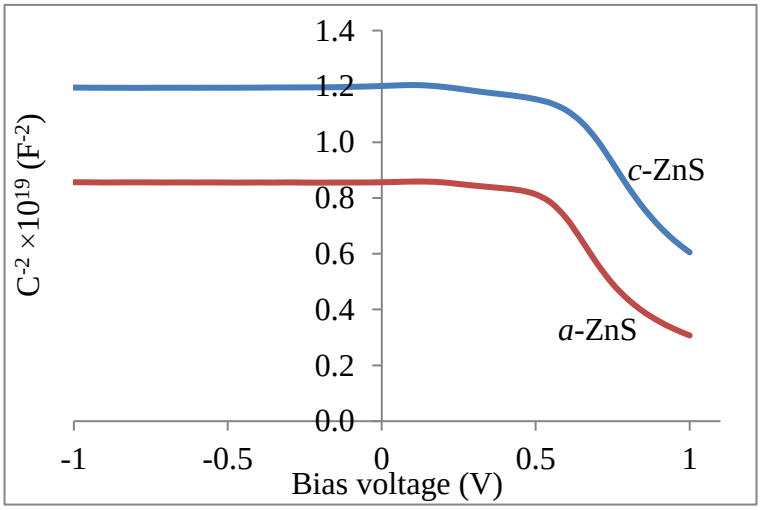

Figure 12: Mott-Schottky plot under dark conditions for glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au device cell incorporating *c*-ZnS and *a*-ZnS buffer layers.

With increasing forward bias voltage above 0.5 V, increase in the measured capacitance resulting in a gradual reduction of the depletion width was observed for both of the devices under consideration. The varying capacitance in the forward bias region was used to plot the Mott-Schottky graph and approximate values of the parameters for the material and the

device. Since the capacitance values depend on defects in the structure, the parameters obtained are not very accurate, but helpful in understanding the devices.

The depletion width of 1092 nm and 899.5 nm for the respective devices incorporating *c*-ZnS and *a*-ZnS at zero bias was calculated using equation (5). From observation, the calculated W for the two devices incorporating *c*-ZnS and *a*-ZnS shows a more similar width to the thickness of the device (~1150 nm). From the Mott-Schottky plot (see Figure 12) and equations (5)-(8), both the V_{bi} and (N_D-N_A) can be determined. In these equations, the capacitance is *C*, built-in potential is V_{bi}, *the* reverse bias voltage is V_R, the contact area is *A*, the electronic charge is *e*, the permittivity of free space is ε_o, semiconductor permittivity is ε_s and dielectric constant (or relative permittivity) is ε_r. based on the literature, ε_r is ~11 [52]. The gradient acquired from the intercept of the Mott-Schottky plot with the bias-axis (see Figure 12) was incorporated into equation (7).

$$C_0 = \frac{\varepsilon_r \varepsilon_0}{W} \tag{5}$$

$$C^{-2} = \frac{2}{\varepsilon_s e A^2 N_D}(V_R + V_{bi}) \tag{6}$$

$$slope = \frac{2}{\varepsilon_s e N_D A^2} \tag{7}$$

$$N_D = \frac{2}{\varepsilon_r \varepsilon_o e A^2 * slope} \tag{8}$$

The noticeable constant C^{-2} capacitance in the Mott-Schottky plot of both the devices indicates that both devices are fully depleted. Therefore, the doping concentration (N_D-N_A) can only be evaluated from the data in the forward bias voltage of ~0.5 V and beyond. The calculated doping densities of 7.79×10^{14} cm^{-3} and 9.52×10^{14} cm^{-3} for the devices respectively incorporating *c*-ZnS and *a*-ZnS buffer layers are primarily within the *n*-CdTe layers, which is the bulk of the device. The slight difference in the (N_D-N_A) associated with *n*-CdTe can be due to the substrate quality provided by the initial ZnS layers for the CdS and CdTe layers to grow with less defect. For both of the devices, the calculated values of the doping concentrations and the built-in potential are in line with the values of high-efficiency CdTe-based devices (~1.0×10^{14} to 5×10^{15}) cm^{-3} in the literature [3,53,54]. The effective density of states in the conduction band (N_c) was calculated to be ~7.92×10^{17} cm^{-3} using equation (9) where *h* is the Plank's constant, *T* is the temperature, *k* is the Boltzmann's constant and m_e^* is the effective electron mass. With the assumption that all donor atoms (N_D) are ionised ($n \approx N_D$)

at room temperature, the charge carrier mobilities $\mu_{\perp}$ were estimated using equation (10) to give (7.07 and 5.78) $cm^2V^{-1}s^{-1}$ for devices incorporating *c*-ZnS or *a*-ZnS layers respectively. It should be noted that the same electrical conductivity of 8.82×10^{-4} $(\Omega cm)^{-1}$ utilised was estimated from the dark I-V curves of glass/FTO/*n*-CdTe with Ohmic indium contacts.

$$N_c = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{\frac{3}{2}} \tag{9}$$

$$\mu_{\perp} = \frac{\sigma}{N_D e} \tag{10}$$

4 Conclusion

This work demonstrates the successful deposition of both *p*- and *n*-type ZnS thin-films from an aqueous solution containing 0.2 M $ZnSO_4{\cdot}H_2O$ and 0.2 M $(NH_4)_2S_2O_3$ using two-electrode electroplating configuration. Based on the selected material characterisation techniques explored, a narrow range of 1420 mV to 1430 mV was identified as the cathodic potential in which crystalline ED-ZnS is achievable. The XRD results show the amorphisation of the as-deposited crystalline ED-ZnS layer after 300°C heat treatment and the retention of crystallinity of the ED-ZnS layers grown at (~1425 to ~1430) mV. The SEM micrographs show small grain attesting to the wetting property of ZnS. The optical bandgap of the ED-ZnS layers is within the reported values for hexagonal ZnS layers (~3.90 eV). The fabricated devices using ZnS as the buffer layer in the glass/FTO/*n*-ZnS/*n*-CdS/*n*-CdTe/Au graded bandgap configuration show prospect of achieving even higher photovoltaic efficiency. The graded bandgap increases the possibility of harnessing more photons both from the blue-end and the red-end of the solar spectrum. The device parameters observed incorporating *c*-ZnS are much better (η=14.2%) than those devices fabricated with *a*-ZnS (11.2%). Work is on-going on the optimisation of other processing and device fabrication steps towards achieving higher efficiency.

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