Full-Custom Integrated Circuit Design for a Pulse Frequency Modulator

Uwe Schiller

A thesis is submitted in partial fulfilment of the requirements of Sheffield Hallam University for the degree of Doctor of Philosophy

September 1996

ACKNOWLEDGEMENT

A number of people supported me during the course of my research and without the help of whom I could have never completed this thesis. Both of my supervisors, Dr J. R. Travis and Dr Z. Ghassemlooy, were actively involved in all stages of my work and I wish to express my sincere gratitude and appreciation for their constant support, encouragement, valuable discussions and guidance throughout the duration of this project and for proof-reading the thesis.

I would also like to thank Dr J. M. Holding for many hours of useful discussions and support. Special thanks goes to all the technicians of the former School of EIT for their technical support, especially to Mr S. Spencer. The help of Jerome Grillot from GEII IUT 'A' Bordeaux I, France, and Michael J. Raabe from Fachhochschule Esslingen, Germany, who carried out project work at the School of EIT is greatly appreciated.

I also thank Ms O. Omar for her help in producing the scanning electron micrographs of the IC layout. I also thank all the members of the Electronics & Communications Engineering Research Group, especially my colleagues, and many of the lecturing staff of the former School of EIT who gave me lots of support and made my stay in England very enjoyable.

The financial help of Sheffield Hallam University is gratefully acknowledged.

Finally, the personal support given to me by my relatives and friends has been valuable indeed. I thank my parents for their encouragement and trust in me. Their Sunday telephone call never let me loose touch with home.

ABSTRACT

Pulse frequency modulation (PFM) is one of a number of pulse time modulation (PTM) techniques which is suitable for the transmission of video or TV signals through optical fibre. Although several PFM transmission systems have been reported over the past few years, those available commercially usually consist of several components. This thesis describes the design of a novel single chip PFM modulator implemented in 2.4 μm CMOS technology. Various design approaches are considered together with a review of circuit and silicon implementation techniques. The fabricated integrated circuit (IC) matches or exceeds the performance of PFM modulators built with commercially available components.

The performance of the design is strongly dependent upon its IC layout. A theoretical analysis of the relationship between the folding grade of a transistor and its parasitic capacitances has been undertaken. Novel equations are developed which enable to trade-off design shape against parasitic capacitance. The lowest drain/source capacitance is always achieved at a folding grade of two regardless of the transistor width to length ratio. The equations developed also show that even folding grades generally achieve a lower parasitic capacitance than odd folding grades.

Performance tests on prototype ICs have shown that the measurement equipment introduces significant capacitive loading. A novel approach of calculating this capacitive loading from transient measurement results is described.

The designed IC was extensively tested in a practical transmission system comprising modulator and demodulator and results of both quantitative and qualitative measurements are reported. At a carrier frequency of 32 MHz and a modulating input signal amplitude of 1 V, the circuit achieves a harmonic and non-linear distortions of -37.87 dB and -56 dB, respectively. These values compare favourably with published results of PFM systems. Further in system tests confirmed that the IC developed is well suited for the transmission of high quality still and moving pictures.

The IC was only compared with the VCO circuits available commercially (Plessey SP1658 and TI SN74S124) since VCOs are the main building block of a PFM modulator and single chip versions are not currently available. Results of the comparison show that the performance of PFM modulators, based on those VCOs, is inferior to the designed circuit whilst requiring a much higher power dissipation. The power dissipation of the designed circuit is 47.5 mW compared to 165 mW and 525 mW for the SP1658 and SN74S124, respectively. Due to the much reduced power dissipation, almost no heat is dissipated from the designed circuit. When operated at its maximum frequency (~ 40 MHz) the temperature of the IC was found to be only 3°C above room temperature.

DECLARATION

I hereby declare that this thesis is entirely my own work and has not been submitted in support of an application of another degree or qualification of this or any other university, institute of learning or industrial organisation.

Uwe Schiller

16 September 1996

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CHAPTER 1

INTRODUCTION

1 INTRODUCTION

Since the invention of the electric telegraph in the 1830s communication engineering has revolutionised the way our society is exchanging information. All the early telegraph systems relied on electrically conductive wire connections between information source and destination. Wireless (radio) communications were demonstrated in England towards the end of the last century. The invention of the vacuum diode and later the vacuum triode had a major impact on the development of wireless communications. The subsequent development of semiconductors in the form of initially the transistor and later the integrated circuit (IC) has further revolutionised communication systems.

The modern day requirements for large volumes of information transfer has lead to demands for increasingly greater bandwidth transmission channels. For wireless communications this is achieved by increasing the carrier frequencies into the Gigahertz range but this may not be practicable for certain applications due to the increased system cost. Optical fibre, however, provides also the necessary transmission medium for wide bandwidths. Nowadays, with optical fibres having an attenuation of less than 1 dB/km very large distances can be covered and transmission rates of more than 1 Gbits/sec can be achieved.

Early optical fibre communication systems used either purely analogue or digital modulation techniques. Analogue modulation techniques could not deliver the required signal-to-noise ratio (SNR) over long distances and were effected by non-linearity

associated with the optical transmission. Digital techniques could overcome these problems but required more hardware and were not bandwidth efficient. In addition, television (TV) signals required a very high data rate and resulted in high costs for fast digital transmission and switching circuitry. In the mid 1970s and early 1980s pulse time modulation (PTM), based on work published in 1947 [Cooke *et al.*, 1947] received a renewal of interest. PTM characteristics are intermediate between purely analogue or digital implementations. Since the form of the modulated carrier is similar to a binary pulse pattern the received signal is not effected by optical source and channel non-linearities and can be routed through logic circuitry. In addition, no analogue to digital conversion is necessary reducing the system's cost. It has been shown that this technique can deliver a better SNR than purely analogue modulation while maintaining a better spectrum efficiency than purely digital techniques [Wilson *et al.*, 1995].

Several PTM techniques have emerged over the years and been proven to be suitable for transmitting various kind of signals. Pulse position modulation (PPM) and pulse width modulation (PWM) have been proven by Holden [1975], Dibiase [1987] and Tanaka, Okamura [1991]. Other modulation techniques include pulse interval (PIM) and pulse interval and width modulation (PIWM) [Wilson *et al.*, 1992]. Pulse frequency modulation (PFM) and square wave frequency modulation (SWFM) have, in particular, been shown to be ideal for the transmission of TV and high definition TV (HDTV) signals over optical fibre [Heatley, 1982; Wilson *et al.*, 1991; Li *et al.*, 1992].

The development of ICs has contributed significantly to advances in communication systems. The evolution of ICs is almost unparalleled by any other engineering

discipline. The first integrated circuit was developed only 40 years ago and comprised a few transistors. Today, ICs containing 5 million transistors per chip are widely available. The development of IC design is characterised by ever increasing miniaturisation and functionality on one single chip. The physical size of modulation and demodulation circuits, for example, has shrunk with the increasing complexity of ICs.

This thesis investigates possible designs and the implementation of a CMOS single chip pulse frequency modulator. Design approaches are considered together with a review of circuit and silicon implementation techniques and novel solutions are determined and comparisons of simulated and practical performance given.

In Chapter 2 pulse time modulation techniques are introduced. General characteristics of each PTM scheme are given and modulation and demodulation techniques are presented. PWM, PPM, PFM and SWFM are compared with regard to non-linear distortion (NLD), harmonic distortion (HD) and signal-to-noise ratio performance. Reasons are given why PFM is a preferred modulation scheme for transmission of video or TV signals. The chapter concludes with more detailed theoretical aspects of PFM.

An overview of integrated circuit design is given in Chapter 3. Silicon IC technologies are compared and reasons are given for selecting CMOS as the preferred technology for implementing the PFM modulator. Furthermore, IC design methodologies are introduced and an overview of custom IC design is given. This is followed by a summary of the available IC technologies through EUROCHIP/EUROPRACTICE with

a performance evaluation of the Alcatel MIETEC 2.4 μm CMOS technology. This chapter concludes with a short introduction to the design environment employed.

Chapter 4 introduces full-custom IC layout with regard to CMOS technologies. The performance of folded MOS transistor layouts is theoretically analysed and the relationship between folding grade of the MOS transistor and important parasitic capacitances is investigated. Equations are given which allow the designer to trade-off design shape of the transistor and value of parasitic capacitances associated with the transistor and its IC layout. The importance of component matching in IC layouts is also discussed. Extraction of parasitic elements from the layout information is presented together with a brief evaluation of two different software extraction tools. During that investigation, it was found that one of the extraction tools, Mentor Graphic's IC Extract, had a faulty software routing calculating parallel resistivity.

The PFM modulator circuit design and description is given in Chapter 5 with subcircuit implementations, simulations and measurements presented in Chapter 6. Chapter 6 also investigates the accuracy of the SPICE transistor models provided. Furthermore, the capacitive loading of prototyping ICs by measurement equipment is investigated and a novel approach is described which allows the determination of this loading from transient measurement results.

Chapter 7 presents the final PFM modulator implementation. Results of measurements taken on the fabricated IC were used to determine its performance and suitability for transmission of video or TV signals. These measurements included time measurements

to determine pulse width and quality of transmitted signals, spectral measurements to determine spectral overlap, harmonic distortion and linearity and qualitative measurements to determine the system performance for video transmission. Differences between simulated and measured results are discussed. A comparison between the designed IC and commercially available PFM modulators is also carried out. This chapter concludes with the designed IC specification.

Conclusions resulting from the work undertaken are presented in Chapter 8 together with suggestions for future work.

CHAPTER 2

PULSE TIME MODULATION TECHNIQUES

2 PULSE TIME MODULATION TECHNIQUES

2.1 Communication Systems

In general terms, an information system consists of a source (transmitter) and a destination (receiver). In order for the information to be transferred between these two it is usually necessary to change its format to suit the transmission media. For example, information transfer between human beings may be converted into sound pressure waves for transmission through a gas (speech). Over longer distances the sound pressure waves may be converted directly into electrical potentials for transmission through copper cable or into light for transmission through optical fibre. The simple direct conversion process makes very inefficient use of the transmission media and often the characteristic of the information itself (such as wavelength or amplitude) makes it unsuitable for transmission.

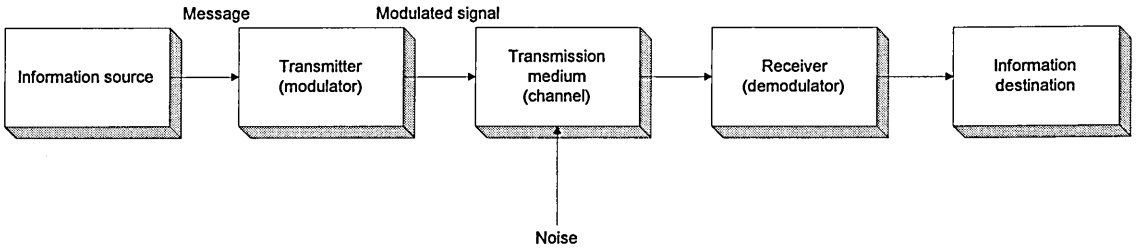

Figure 2.1: Block diagram of a communication system

The message is therefore usually modulated to enable efficient transmission through the selected media, as shown in Figure 2.1. Modulation also allows more than one message to be transmitted at a given time. Associated with the transmission media there will be attenuation and possibly contamination of the signal through noise and interference. If the transmission channel is very long the signal may need intermediate amplification

during its journey. At the receiving end the original signal must be recovered by demodulation. Recovering an exact copy of the waveform is almost impossible since the signal is always distorted to some degree by noise and non-linearity of the system. The quality of the transmission system is dependent upon how precisely the original message can be reproduced and this is normally measured in terms of the signal-to-noise ratio.

The first telegraphic system developed in the 1830s relied on a wired connection between source and destination. Wireless communication was first shown at the end of the last century. In today's communication technology, optical fibre cables are replacing copper cables because of the excellent features of optical fibres such as low transmission loss (< 1.0 dB/km), wide bandwidth, small physical size and immunity to electromagnetic interference [Ghassemlooy *et al.*, 1993]. To make full use of what is an almost ideal transmission channel and to produce a communication system which is cost effective as well as bandwidth efficient the choice of modulation format is of prime importance.

The various modulation schemes that exist can be grouped into three main categories, analogue, digital and pulse modulation. In analogue modulation the properties of a sinusoid carrier frequency, such as amplitude, frequency or phase are changed by the modulating signal. Examples are amplitude modulation (AM) where the amplitude of the carrier is proportional to the modulating signal, frequency modulation (FM) where the instantaneous frequency of the carrier is determined by the signal and phase

modulation (PM) where the instantaneous phase of the carrier is related to the input signal.

In digital modulation, the modulating signal is first converted into a digital form by sampling and quantizing the signal. This process will loose some information but this loss is minimised by selecting a quantization interval which is less than the sensitivity of the receiver. Quantization results in N preselected levels where each level covers a range of input signals. Numerical values will be assigned to these N levels which will then be converted into a binary format before being transmitted. Since the binary code consists only of logic 0s and 1s, the receiver has only to distinguish between these two states and this improves the overall performance of the system.

In pulse modulation, the carrier is, in most cases, a periodic sequence of constant amplitude pulses and the modulating signal is used to vary some properties of the pulse such as, width, position or repetition rate.

2.2 Comparison of Modulation Techniques

Since both, analogue and digital signals can be transmitted over fibre optics it is important to first compare advantages and disadvantages of analogue and digital modulation schemes.

In analogue modulation schemes the optical source is modulated in a continuous manner resulting in a variation of the intensity of the optical source. Known modulation

schemes (e.g. AM or FM) can be used to modulate the signal in the first instance followed by direct intensity modulation of the optical source. It is a very simple, bandwidth-efficient scheme. The disadvantage of this technique is that electro-optic converters are inherently non-linear and therefore introduce distortion. The non-linearity of a laser diode (LD), for example, gives rise to harmonics and intermodulation and it attenuates higher frequency components [Tucker *et al.*, 1983; Lin *et al.*, 1990]. The optical fibre introduces additional distortion [Royset *et al.*, 1994; Walker, 1994] and therefore, the achievable signal-to-noise ratio is often very low [Senior *et al.*, 1990].

Most of the problems associated with analogue transmission can be overcome by using digital modulation schemes such as pulse code modulation (PCM). This scheme is substantially immune to source non-linearity and has a better SNR performance than analogue schemes [Senior *et al.*, 1990]. However, digital systems require much more complex circuitry, resulting in an increased overall cost of the system. In addition, digital modulation requires a much larger bandwidth compared with analogue techniques. However, these latter problems can be overcome by employing code compression techniques but this is at the expense of further increase in complexity and cost [Wilson *et al.*, 1993; Rhomberg, 1981].

With the development of fibre transmission systems a third modulation technique, called pulse time modulation was reintroduced. First investigations into PTM techniques were carried out in the late 1940s [Cooke *et al.*, 1947] but it was not until the development of optical fibre systems in the late 1970s early 1980s that there was a revival of research interest and system development in that area [Rhomberg, 1981].

PTM can be used to overcome problems associated with purely analogue or digital methods. The characteristics of PTM techniques are intermediate between analogue and digital implementations. In PTM, the modulated carrier is a periodic sequence of pulses with a constant amplitude but variable pulse edge, width, position or repetition rate. Since the form of the generated signal is similar to a binary pulse pattern, the received signal is not affected by channel non-linearities and can also be routed through logic circuitry [Dibiase *et al.*, 1987].

PTM has the ability to trade-off performance with bandwidth which is particularly useful in fibre communication systems [Wilson *et al.*, 1993]. This unique feature can be exploited when designing systems having different SNR requirements. Thus, low speed optical sources such as light emitting diodes (LEDs) may be used for short distance applications while optical amplification and soliton techniques may be employed for long distance, terrestrial or undersea routes. (A soliton is an optical pulse in which the natural dispersion of the optical fibre is compensated exactly by its non-linearity; this allows an isolated soliton to propagate over a large distance without dispersion [Senior *et al.*, 1995]).

As PTM techniques employ a pulse format no consideration has to be given to LED or LD non-linearities as with direct intensity modulation schemes. Furthermore, some PTM schemes make use of very narrow pulses having a very high peak optical power with a low mean transmitted power, hence ensuring a good SNR performance whilst securing a long lifetime for the optical device.

Simple LEDs are often used for low cost, short distance applications whereas injection laser diodes (ILDs) are used for longer distances and high capacity systems [Wilson *et al.*, 1995]. ILDs are well suited for PTM schemes which vary the properties of a train of narrow pulses since these techniques exhibit a high optical peak power whilst having a low average power thus enhancing the lifetime of the ILDs.

2.3 Pulse Time Modulation Techniques

2.3.1 PTM schemes

By using PTM the information is conveyed in a time dependent feature of a constant amplitude carrier as summarised in Table 2.1.

Table 2.1: PTM methods [Wilson *et al.*, 1995]

PTM type	Variable
PPM	Position
PWM	Width (duration)
PIM	Interval (space)
PIWM	Interval and width
PFM, SWFM	Frequency (repetition rate)

One possible classification of PTM techniques, based on the sampling waveform's fundamental spectral component under modulation conditions, has been described by Wilson *et al.*, [1993] and is shown in Figure 2.2. This classification does not include some newly investigated digital pulse time modulation techniques [Wilson *et al.*, 1995; Ghassemlooy *et al.*, 1995].

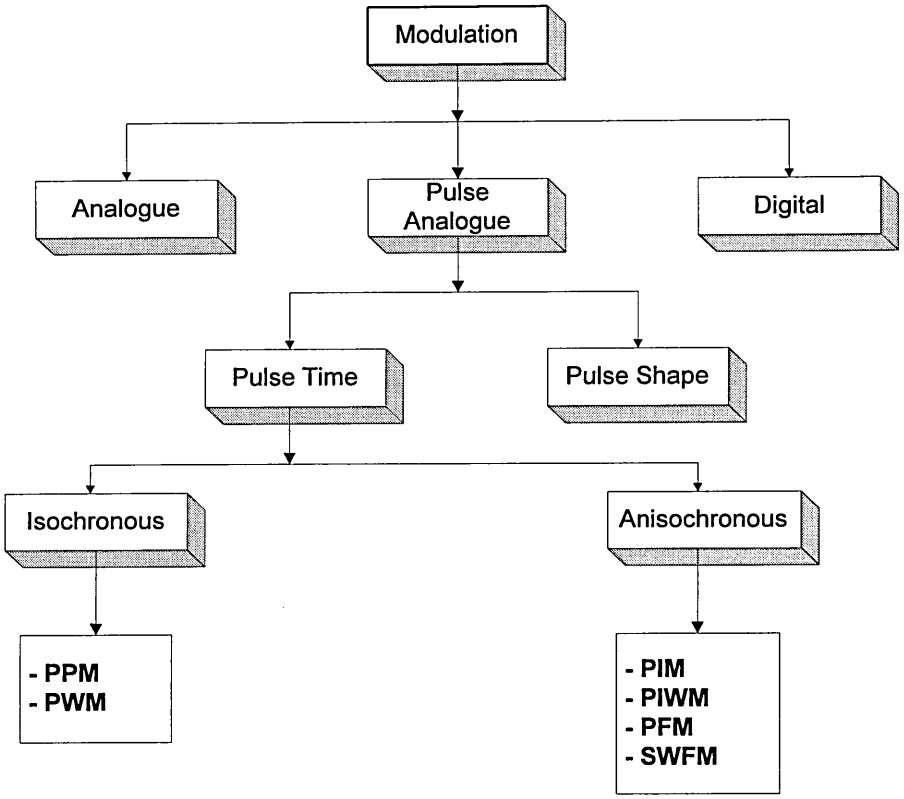

Figure 2.2: Modulation tree

In PWM, sometimes referred to as pulse duration modulation (PDM), the width (duration) of the carrier signal is changed without effecting the time frame, hence the duty cycle is changed dependent upon the sampled modulating input signal. PPM may be generated by detecting the modulated edge of the PWM waveform. Therefore, the information is conveyed in the variable position of a narrow pulse within a predetermined time frame. Both modulation techniques may be classified as isochronous since the sampling time and hence the time frame, is constant (Figure 2.3) [Wilson *et al.*, 1993].

In PIM the information is carried within the constantly changing intervals between narrow pulses, the interval being dependent upon the amplitude of the modulating

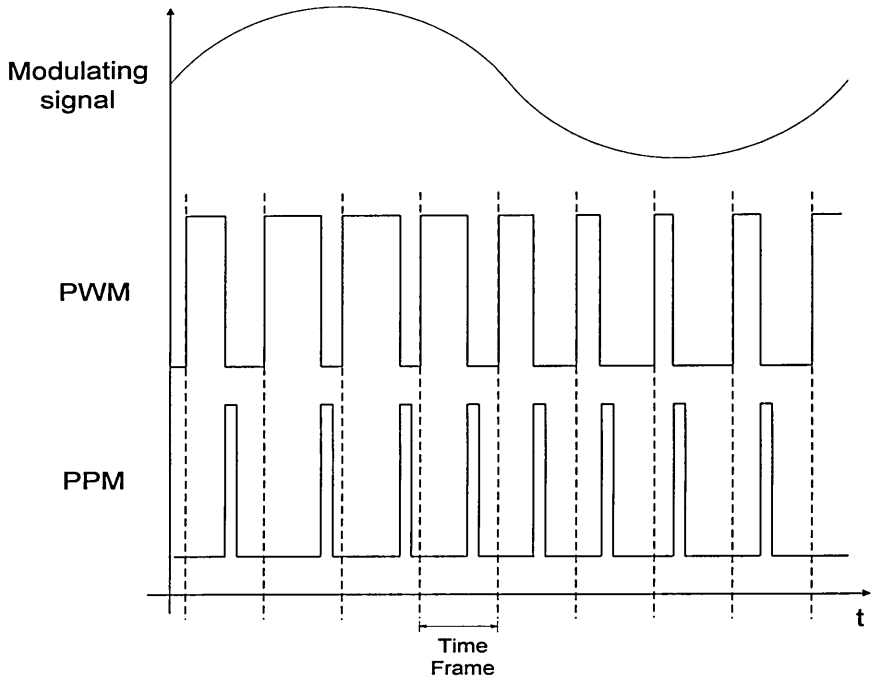

Figure 2.3: PWM and PPM techniques

signal. PIWM is derived from PIM to form a waveform where the information is conveyed in both marks and spaces. The difference between this and PWM or PPM is that in PIM/PIWM the next time frame commences immediately after the current time frame has finished and no fixed time frame for sampling is employed (Figure 2.4). These modulation schemes are therefore described as anisochronous [Wilson *et al.*, 1993].

In PFM, the repetition rate of a pulse train with fixed pulse width changes according to the amplitude of the modulating signal. SWFM is closely related to PFM and analogue FM. In SWFM a square wave is used as carrier compared to a sine wave as in FM. Again, these two modulation schemes may be categorised as anisochronous since there is no fixed time frame (Figure 2.5) [Wilson *et al.*, 1993].

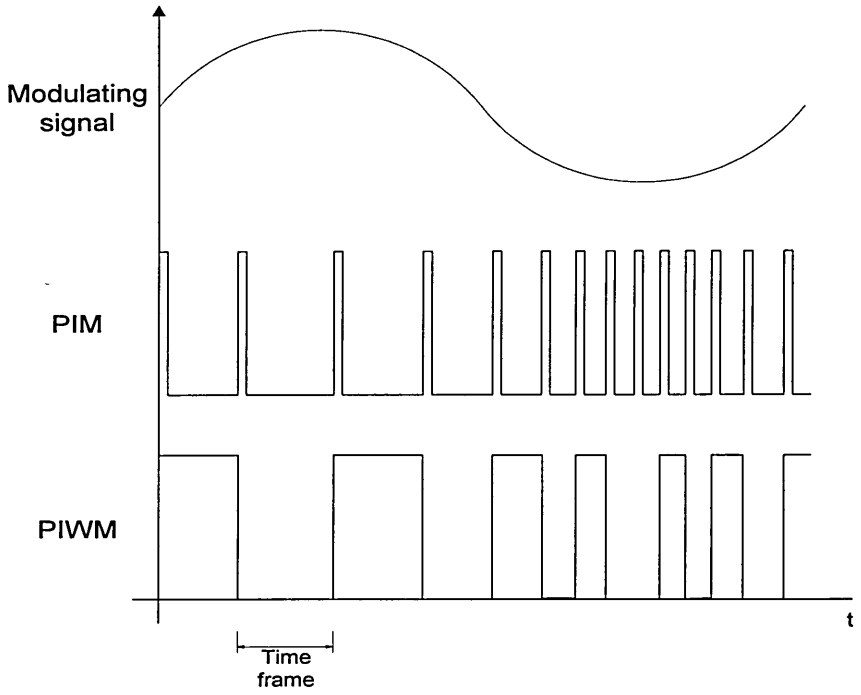

Figure 2.4: PIM and PIWM techniques

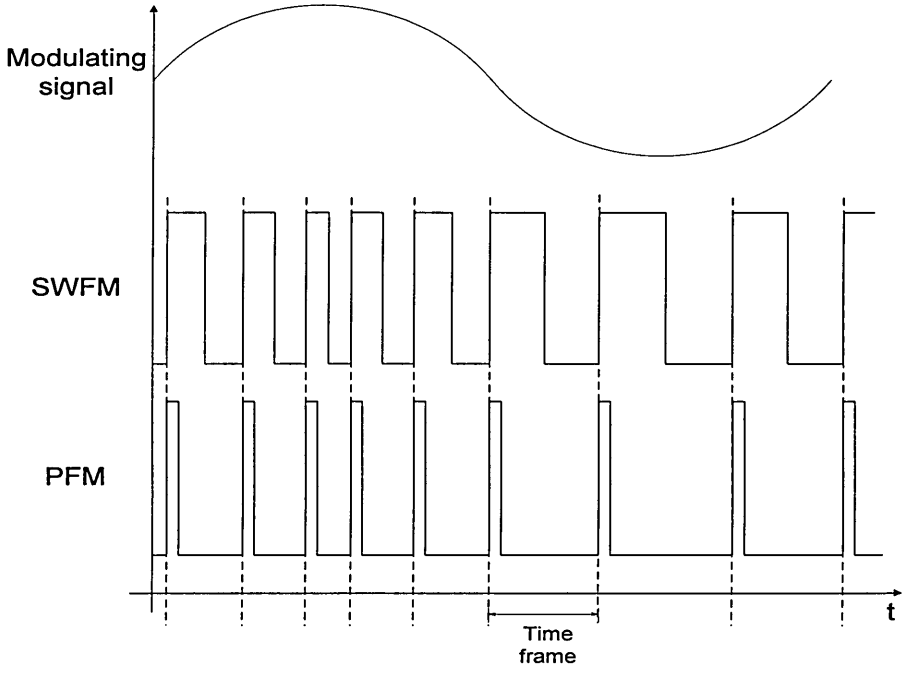

Figure 2.5: SWFM and PFM techniques

PWM and PPM are well know schemes and have been widely used in optical fibre applications [Holden, 1975; Dibiase, 1987; Providakes *et al.*, 1991; Wickramasinghe *et al.*, 1996]. They can easily be time multiplexed due to their fixed time frame and demultiplexing can be achieved with only moderate circuit complexity. Comparatively little work has been published on PIM and PIWM although these schemes offer certain benefits such as self-synchronising code for PIWM [Sato *et al.*, 1979; Wilson *et al.*, 1992]. PFM has been adopted for optical fibre transmission of video and broadcast quality TV signals as well as for CCTV systems. SWFM is being used for transmission of HDTV and other wideband instrumentation signals [Kanada *et al.*, 1982; Heatley *et al.*, 1984; Li *et al.*, 1992; Wickramasinghe *et al.*, 1995].

2.3.2 Modulation spectrum

All PTM techniques produce a modulation spectrum with some common features. Modulation will always produce a declining set of side tones centred around the carrier frequency and its harmonics. The side tones are separated by an amount equal to the modulating signal frequency. Some PTM techniques have the baseband components present in their modulation spectra as shown in Figure 2.6. This feature and the number and magnitude of the side tones present may be used to identify different PTM techniques.

Some PTM techniques require sampling of the signal prior to the modulation. The modulating signal can either be uniformly or naturally sampled. Naturally sampled modulators operate directly on the input signal whereas uniformly sampled modulators

may employ a sample and hold amplifier which samples the signal at predefined time intervals.

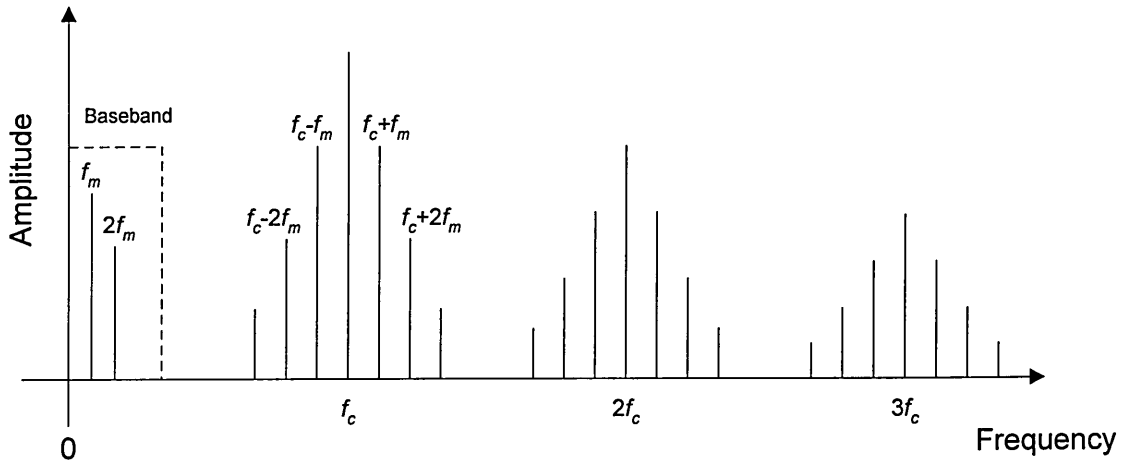

Figure 2.6: General PTM frequency spectrum

After converting the signal from optical to electrical, the PTM waveform is recovered by amplitude detection. Demodulation of PTM depends on the spectrum. If the spectrum contains the baseband component the signal is demodulated by employing a low pass filter. If no baseband component is present, then a conversion of this particular PTM signal into a PTM signal containing the baseband is required before low pass filtering it.

2.3.2.1 Pulse width modulation

In PWM the duty cycle of a constant pulse frequency carrier signal is changed by the sampled modulating signal. The PWM waveform may be generated by comparing the uniformly or naturally sampled input signal with a linear ramp signal. Figure 2.7 shows the principle difference in uniformly and naturally sampling. If a triangular waveform is

used instead of a ramp signal a double edge modulated PWM waveform will be generated.

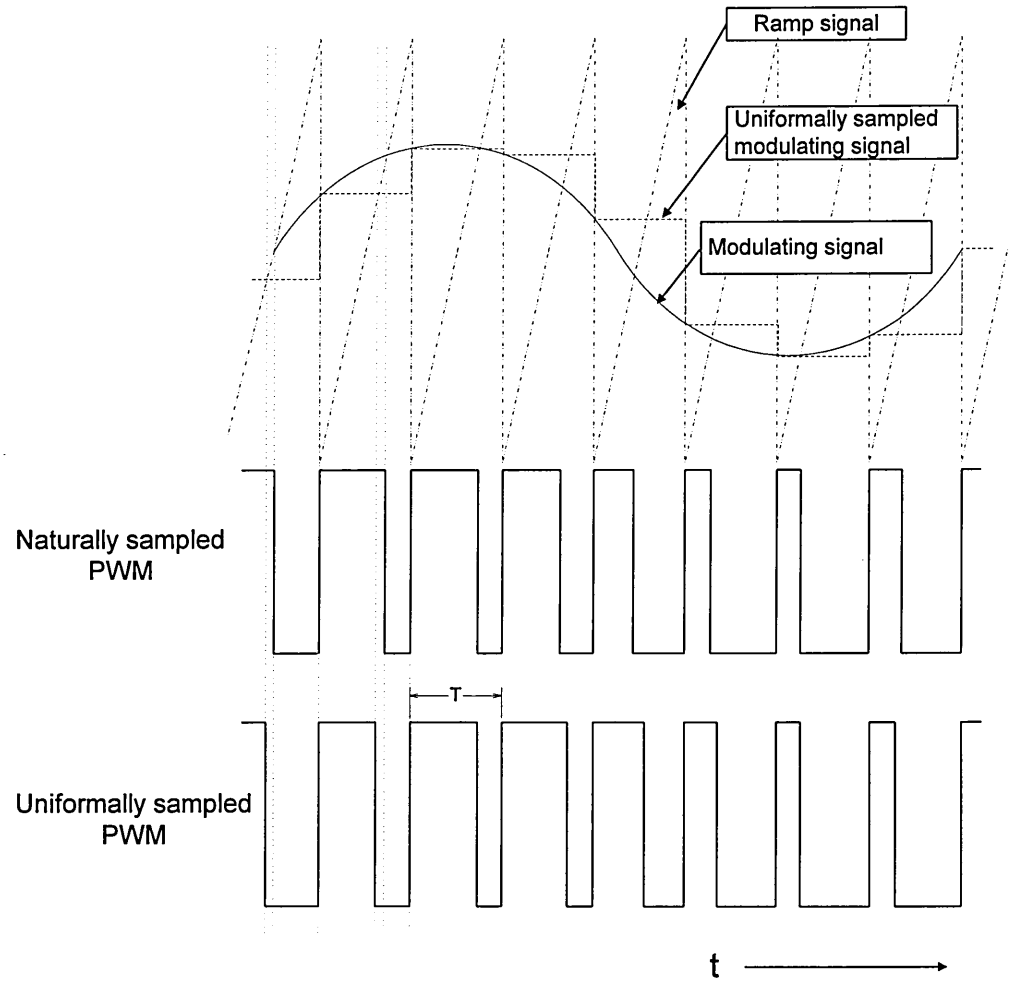

Figure 2.7: Trailing edge naturally and uniformly sampled PWM

The modulation index M ($0<M<1$) may be defined such that the maximum modulation occurs when the peak-to-peak modulating signal amplitude is equal to the ramp signal amplitude [Wilson *et al.*, 1995]. The modulation index may therefore be expressed as follows:

$$M = \frac{\tau}{T} \tag{2.1}$$

where τ is the pulse width deviation and $T = 1/f_c$ with f_c being the carrier frequency (Figure 2.8). The unmodulated pulse width is $T/2$ (i.e. a square wave).

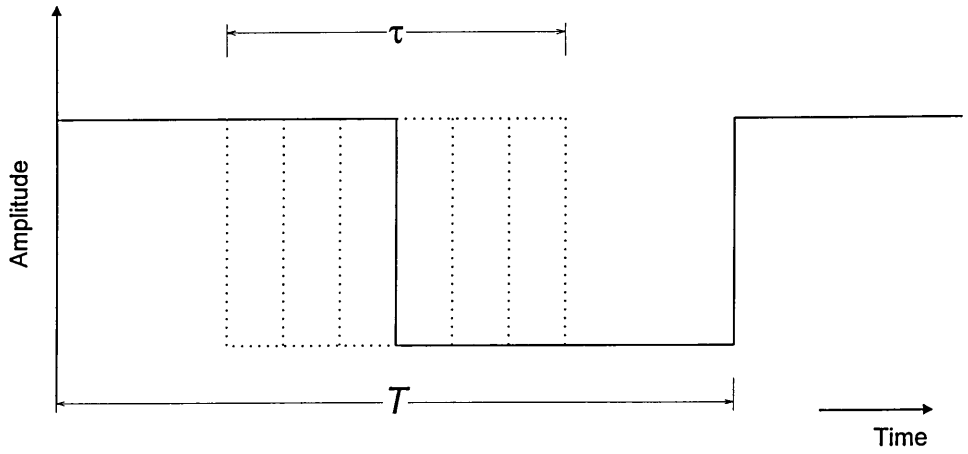

Figure 2.8: Modulated PWM waveform

The naturally sampled PWM modulation spectrum in which the trailing edge is modulated can be expressed as follows [Wilson *et al.*, 1993]:

$$v(t) = \frac{1}{2} - \frac{M}{2}\sin(\omega_m t) + \sum_{n=1}^{\infty}\frac{\sin(n\omega_c t)}{n\pi} - \sum_{n=1}^{\infty}\frac{J_0(n\pi M)}{n\pi}\sin(n\omega_c t - n\pi) - \sum_{n=1}^{\infty}\sum_{k=\pm 1}^{\pm\infty}\frac{J_k(n\pi M)}{n\pi}\sin\left[(n\omega_c + k\omega_m)t - n\pi\right] \quad (2.2)$$

Here ω_m and ω_c are the modulating signal and carrier frequencies, respectively and $J_k(x)$ is the Bessel function of the first kind, order k. Since the PWM signal clearly contains a baseband component (second term) it can be demodulated by employing a simple low-pass filter. Also, since neither the frequency nor the amplitude of the carrier signal is affected by the modulation index the technique may be classified as isochronous [Wilson *et al.*, 1995].

2.3.2.2 Pulse position modulation

Pulse position modulation may be generated by detecting the modulated edge of the PWM waveform. In this case, the information is conveyed by the variable position of a narrow pulse within a predetermined time frame. The naturally sampled PPM modulation spectrum may by given as [Wilson *et al.*, 1993]:

$$v(t) = \frac{A\omega_c\tau}{2\pi} + AM\cos(\omega_m t)\sin\left(\omega_m\frac{\tau}{2}\right) + \frac{2A}{\pi}\sum_{k=-\infty}^{\infty}\sum_{n=1}^{\infty}J_k(n\pi M)\frac{\sin\left[(n\omega_c + k\omega_m)\frac{\tau}{2}\right]}{k}\cos\left[(n\omega_c + k\omega_m)t\right] \quad (2.3)$$

Again, a baseband component (second term) is generated whose amplitude depends on pulse width and input frequency. But this is differentiated and, therefore, for demodulation it is essential to convert the signal into a PWM waveform before low pass filtering. The conversion process will require the clock signal which may be obtained by employing a phase locked loop [Wickramasinghe *et al.*, 1996].

2.3.2.3 Pulse interval modulation

In pulse interval modulation, the amplitude of the modulating signal is encoded as a variable interval between narrow pulses. The PIM waveform may be generated by comparing the modulating input signal with a ramp signal. When the amplitude of the ramp reaches the amplitude of the modulating signal, a narrow pulse is generated and the ramp signal is reset to its initial value. The main difference between this and PWM or PPM is that the next time frame commences immediately after the current one has finished. Thus, no fixed time frame for sampling is employed.

The PIM modulation spectrum may be presented as follows [Wilson *et al.*, 1995]:

$$v(t) = \left(\frac{\omega_0}{2\pi}\sum_{p=0}^{\infty} M^p \cos^p(\omega_m t)\right) \cdot$$
$$\left\{1 + 2\sum_{k=\pm 1}\sum_{n_1=-\infty}^{\infty}\sum_{n_2=-\infty}^{\infty} J_{n_1}(kB_1)J_{n_2}(kB_2)\cos\left[\left(kA_0\omega_0 + (n_1 + 2n_2)\omega_m\right)t\right]\right\} \qquad \textbf{(2.4)}$$

where

$$A_p = \sum_{r=0}^{\infty}\left(\frac{M}{2}\right)^{2r}\frac{(p+2r)!}{(p+r)!r!} \qquad (p = 0,1,2)$$

and

$$B_p = \frac{2\omega_0}{p\omega_m}\left(\frac{M}{2}\right)^p A_p \qquad (p = 1,2)$$

where ω_0 is the unmodulated pulse train and ω_m is the modulating signal frequency.

The last term of equation (2.4) indicates that the spectral profile around the carrier fundamental and all its harmonics is heavily dependent upon the modulation index. The first term indicates that, in addition to the baseband component itself, there is also a series of baseband harmonics present. The amplitude of the baseband component and its harmonics is a function of the modulation index ($0 < M < 1$) with the harmonics becoming negligible at lower modulation indices. In contrast to PPM, the amplitude of the baseband component is not influenced by the modulating frequency. Therefore, for low modulation indices (< 10%) demodulation may be achieved by low pass filtering. If the full modulating range is used, demodulation may be carried out by regenerating the original ramp signal employing the PIM pulse train to reset and initiate the ramp. This is followed by either low pass filtering for naturally sampled signals or passing the

signal through a sample-and-hold amplifier before low pass filtering if the modulating signal was uniformly sampled.

2.3.2.4 Pulse interval and width modulation

Pulse interval and width modulation is derived from PIM and the information is conveyed in both mark and space. The PIWM spectral profile may be represented by [Wilson *et al.*, 1995]:

$$v(t) = \frac{V}{2}\left\{1 + \sum_{k=1}^{\infty}\sum_{n_1=-\infty}^{\infty}\sum_{n_2=-\infty}^{\infty} \frac{\sin\left(k\frac{\pi}{2}\right)}{k\frac{\pi}{2}} J_{n_1}(kB_1)J_{n_2}(kB_2)\cdot \cos\left[\left(kA_0\omega_0 + (n_1 + 2n_2)\omega_m\right)t\right]\right\} \tag{2.5}$$

where $$A_p = \sum_{r=0}^{\infty}\left(\frac{M}{2}\right)^{2r}\frac{(p+2r)!}{(p+r)!r!} \qquad (p = 1,2)$$

and $$B_p = \frac{2\omega_0}{p\omega_m}\left(\frac{M}{2}\right)^{p} A_p$$

where V is the PIWM signal amplitude and A_0 is calculated from A_p, with $p = 0$.

The PIWM spectrum contains no baseband component and has a side tone pattern around the carrier fundamental and all its odd harmonics. The absence of the baseband component results in decreased transmission bandwidth requirements. Demodulation is carried out by first converting PIWM signals into PIM signals followed by a standard PIM demodulation technique.

2.3.2.5 Pulse frequency modulation

In pulse frequency modulation, the repetition rate of a pulse train of fixed pulse width changes according to the amplitude of the modulating signal. PFM waveforms can be generated by employing a voltage controlled oscillator (VCO) followed by pulse generating circuitry.

The PFM spectrum for a pulse train with pulse width τ, repetition rate ω_c and frequency deviation $\Delta\omega$ when modulated with a sine wave of frequency ω_m may be expressed as follows [Fitch, 1947]:

$$v(t) = \frac{A\omega_c\tau}{2\pi}\cdot\left\{1+\frac{2\beta}{\omega_c\tau}\sin\left(\omega_m\frac{\tau}{2}\right)\cos\left(\omega_m t-\omega_m\frac{\tau}{2}\right)\right.$$
$$\left.+2\sum_{n=1}^{\infty}\sum_{k=-\infty}^{\infty}J_k(n\beta)\frac{\sin\left[(n\omega_c+k\omega_m)\frac{\tau}{2}\right]}{n\omega_c\frac{\tau}{2}}\cos\left[(n\omega_c+k\omega_m)t-k\omega_m\frac{\tau}{2}\right]\right\} \quad (2.6)$$

where $\beta=(\Delta\omega/\omega_m)$ and A are modulation index and pulse amplitude, respectively. It can be seen that the unmodulated pulse carrier consists of the fundamental carrier frequency and its harmonics with amplitudes which follow a '*sinc* = *sin(x)/x*' envelope determined by the pulse width τ. Under modulation conditions, the spectrum contains the original baseband component (second term) as well as side tones around the carrier frequency (last term) and all its harmonics. The *sinc* function causes a slight asymmetry with the upper side tones being stronger than the lower. Due to the presence of baseband components, PFM signals can be demodulated after threshold detection and pulse regeneration by low-pass filtering.

2.3.2.6 Square wave frequency modulation

Square wave frequency modulation is closely related to PFM and analogue frequency modulation. In SWFM a square wave is used as carrier in a similar manner to a sine wave in normal FM. The modulation spectrum may be expressed as [Chao, 1990]:

$$v(t) = AD\sum_{n=-\infty}^{\infty}\mathrm{sinc}(n\pi D)\sum_{k=-\infty}^{\infty}J_k(n\beta)e^{[j(n\omega_c+k\omega_m)t]} \tag{2.7}$$

where D is the duty cycle. The modulation spectrum is similar to FM with a pattern of side tones around the carrier fundamental and all its odd harmonics. If the carrier waveform has a precise 50% duty cycle, no baseband component is present. Deviations from this duty cycle will cause a baseband component to be present as well as sidebands at even harmonics of the carrier frequency. The SWFM waveform may be generated by employing a voltage controlled multivibrator.

Demodulation can be achieved by converting the SWFM waveform into a PFM waveform followed by low-pass filtering. If double edge detection is employed (i.e. rising and falling edges) the resulting spectrum contains along with the baseband component sideband structures around all the even harmonics of the carrier frequency. The carrier frequency itself and all odd harmonics are not present. This allows the minimum carrier frequency to be lowered reducing the bandwidth requirements. In addition, detecting the rising and falling edges results in superior SNR performance compared to standard PFM [Heatley, 1985].

2.4 Comparison of PTM Schemes

A comparison of PTM techniques may be carried out with regard to distortion and SNR performance. Furthermore, for analogue signals the techniques may be evaluated by their ability to produce low distortion at low sampling ratios and high SNRs. The minimum carrier frequency can be estimated from spectral overlap between modulating signal and lower side tones of the carrier fundamental. Another consideration when evaluating different modulating techniques may be the modulator/demodulator circuit complexity influencing the overall transmission systems' cost [Wilson *et al.*, 1995].

Several PTM techniques have been implemented and they all result in different system complexity, bandwidth requirements and SNR performance. A trade-off has to be made for conflicting requirements leading to an optimised system. Some video transmission systems employing PIM or PIWM were reported in the late 1970s [Ueno *et al.*, 1978; Sato *et al.*, 1979; Okazaki, 1979]. But these two modulation techniques have not received much attention since they showed no performance advantages compared to PPM and required more circuit complexity compared to PFM and SWFM [Senior *et al.*, 1995]. For this reason, only PWM, PPM, PFM and SWFM will be considered further.

The performance of modulation schemes may be compared with respect to a certain application. The application will give the minimum requirements, such as SNR or NLD, the system has to fulfil for a successful recovery of the transmitted signal.

The circuit to be designed must be capable of modulating a standard PAL video signal. Figure 2.9 shows the frequency components of the standard United Kingdom TV signal which has a total bandwidth of 6.05 MHz [DTI, 1984].

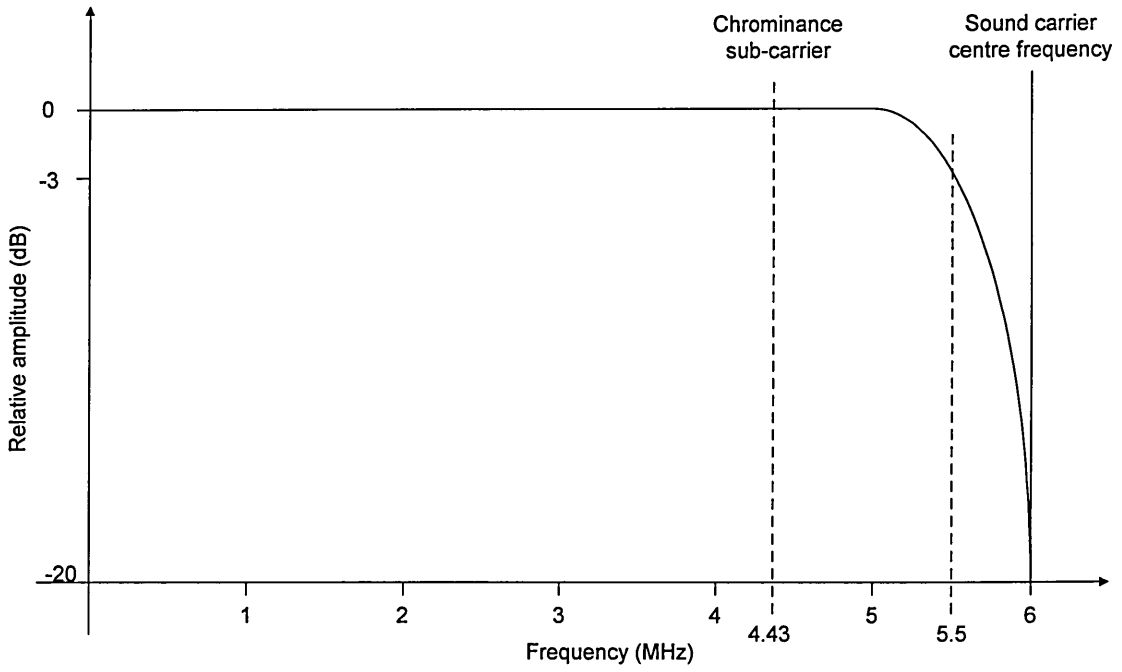

Figure 2.9: Video signal spectrum

Important frequency components are the chrominance or colour sub-carrier and the sound carrier centre frequencies. The frequency deviation of the sound carrier under modulation condition is 50 kHz. From here on the video signal will be represented by a 5.5 MHz sine wave indicating its highest frequency component and the audio carrier signal by a 6 MHz sine wave. This avoids the impossible task of carrying out a spectral analysis of the transmitted signal for a complicated multi-tone modulating signal.

Important criteria are the SNR performance and the overall linearity of the system. It has been shown that transmission systems achieving an unweighted SNR of at least 40 dB with a non-linearity of less than 1% (-40 dB) are sufficient for video and TV signals [Sato *et al.*, 1985; Gutierrez-Martinez, 1991; Ghassemlooy *et al.*, 1993].

2.4.1 Non-linear distortion

All PTM techniques produce a modulation spectrum with some common features. One of those features are the side tones around a modulated carrier frequency. Depending upon the ratio between carrier and modulating signal frequencies (sampling ratio), some of the lower carrier side tones will enter the baseband region causing non-linear distortion. These distortion levels can be estimated from the spectral profile. For PWM and narrow pulse PPM, the non-linear distortion level represents the ratio between side tone and recovered modulating signal amplitude and can be expressed as [Wilson *et al.*, 1995]:

$$NLD_{PWM/PPM} = 20\log\frac{2J_k(\pi M)}{\pi M} \tag{2.8}$$

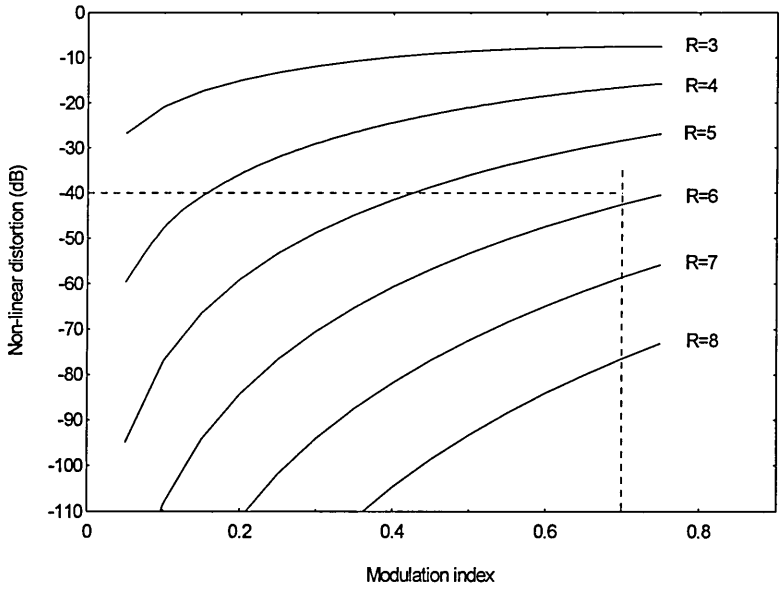

Figure 2.10: Distortion level of PWM and PPM

Figure 2.10 shows a the graphical representation of equation (2.8). A distortion level of -40 dB can be achieved at a sampling ratio of 4 and a modulation index of 0.16, increasing to 6 for a modulation index of 0.7.

A similar analysis for PFM and SWFM results in:

$$NLD_{PFM} = 20\log\frac{2J_k(M)\sin[\pi(f_c + kf_m)\tau]}{\pi f_m M\tau} \tag{2.9}$$

$$NLD_{SWFM} = 20\log\frac{J_k(2M)\sin[\pi(2f_c + kf_m)\tau]}{\pi f_m M\tau} \tag{2.10}$$

where f_m is the modulating frequency, f_c the carrier frequency and τ the pulse width. Figure 2.11 shows a comparison of equations (2.8) to (2.10). Each curve represents a non-linear distortion level of -40 dB and can be used to define modulation index and sampling ratio for the various modulation schemes. The best performance is clearly obtained using SWFM followed by PFM. Furthermore, it can be seen that PWM/PPM require a higher sampling ratio than SWFM or PFM resulting in higher bandwidth requirements.

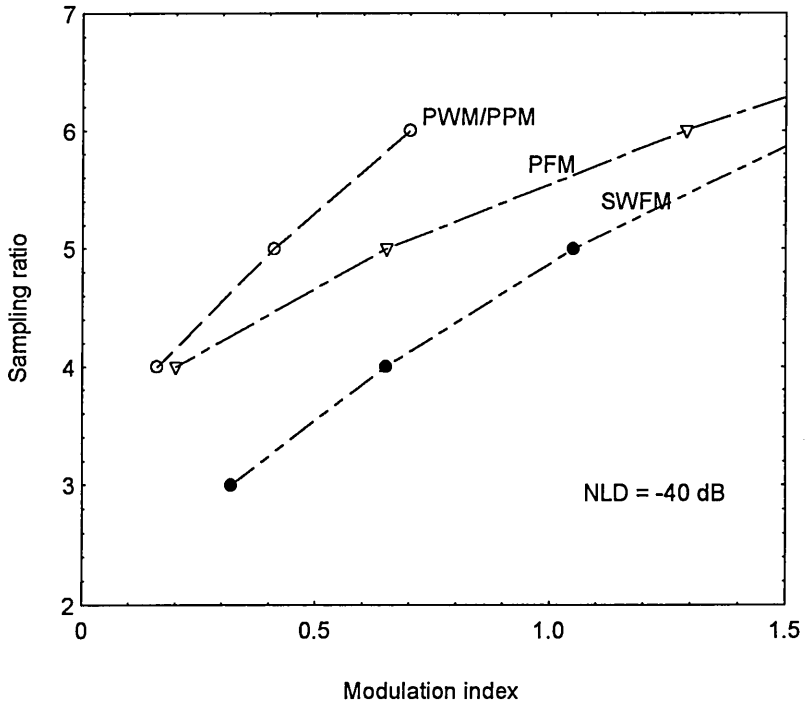

Figure 2.11: Sampling ratio versus modulation index for -40 dB distortion level

2.4.2 Signal-to-noise ratio performance

In addition to the non-linear distortion arising from spectral overlap the relationship between the output SNR and carrier-to-noise ratio (CNR) needs to be investigated. This relationship describes the interaction between SNR performance and the received pulse edge speed, as dictated by the channel bandwidth $B_t = 1/\tau$. An unweighted improvement factor *IF*, given by SNR minus CNR (in dBs), above threshold is proportional to the square of the ratio of transmission channel bandwidth to carrier frequency. The proportionality constant differs for each PTM technique [Chao, 1990; Wilson *et al.*, 1995] and can be expressed as follows:

$$PWM \qquad IF = \frac{\pi^2}{8}\left(\frac{MB_t}{f_c}\right)^2 \tag{2.11}$$

$$PPM \qquad IF = \frac{\pi^2}{4}\left(\frac{MB_t}{f_c}\right)^2 \tag{2.12}$$

$$PFM \qquad IF = \frac{3}{4}\left(\frac{MB_t}{f_c}\right)^2 \tag{2.13}$$

$$SWFM \qquad IF = \frac{3}{2}\left(\frac{MB_t}{f_c}\right)^2 \tag{2.14}$$

The minimum carrier frequency and bandwidth requirements for each modulation scheme is given in Table 2.2 with $f_m = 6$ MHz, $M = 0.7$ and $\tau = 7$ ns (f_g is the guardband) [Chao, 1990]. Except for PPM, all of the other schemes have a fairly similar bandwidth requirement and SWFM has the lowest carrier frequency due to a surpressed carrier fundamental.

Table 2.2: Bandwidth requirements for PTM schemes

PTM scheme	Channel bandwidth (B_t) (MHZ)	Carrier frequency (f_c) (MHz)
PWM	$f_m\pi M+3f_m+2f_g = 39$	21
PPM	$1/\tau = 143$	21
PFM	$3f_m+2Mf_m+2f_g = 38$	20
SWFM	$2f_m+2Mf_m+2f_g = 32$	14

Figure 2.12 shows the output SNR versus CNR for different PTM schemes applying equations (2.11) to (2.14) with values taken from Table 2.2. This is a valuable comparison since it takes into account the different sampling ratios and bandwidth requirements of each technique. Different values for pulse width or modulating frequency will result in slightly different curves.

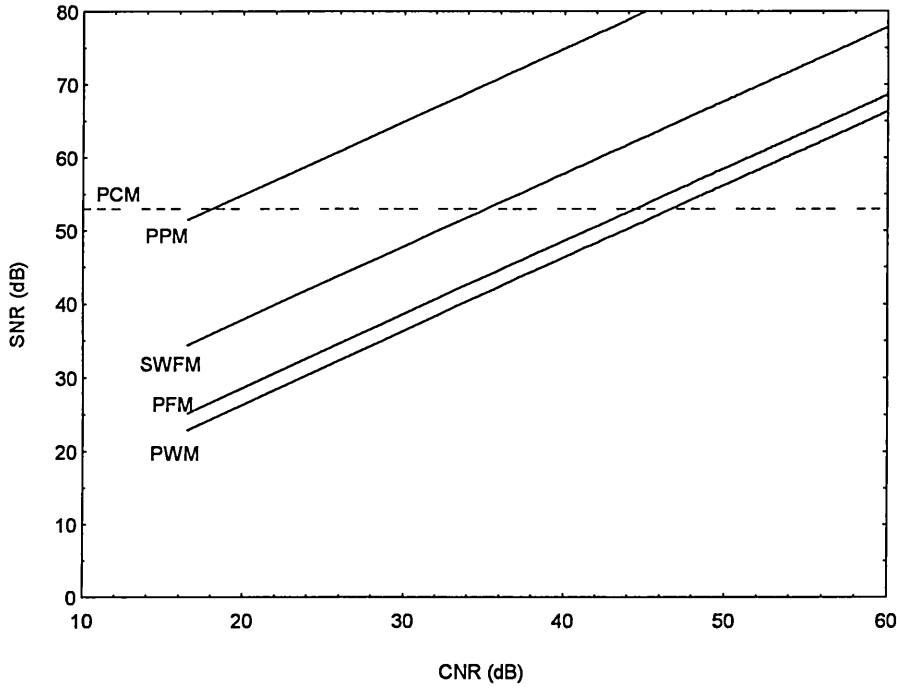

Figure 2.12: SNR versus CNR for various PTM schemes

It is clear that PCM offers improved SNR at lower CNRs than PTM. Above threshold detection, the SNR stays constant regardless of change in CNR values at the receiver [Chao, 1990]. But this is achieved at the expense of wider system bandwidth required for transmission. Another drawback is the increased circuit complexity requiring analogue to digital conversion at the modulator side and digital to analogue conversion at the demodulator side.

PPM has the best SNR performance of the PTM techniques considered but at the expense of wider transmission bandwidth and increased circuit complexity due to clock recovery at the demodulator. SWFM and PFM both offer good SNR performance, slightly better then PWM, while maintaining low sampling ratios and low cost.

These considerations make PFM and SWFM the preferred choice for transmitting TV signals through optical fibre cable. If a laser diode is used as an optical coupling device, PFM should be preferred due to its high peak and low average optical power ensuring a longer lifetime of the device.

2.5 Theoretical Aspects of PFM

2.5.1 PFM frequency spectrum and spectral overlap

In pulse frequency modulation the repetition frequency of a train of pulses is determined by the modulating signal voltage. The spectrum of a PFM pulse train when modulated with a sine wave has been given in equation (2.6). Figure 2.13 shows a typical frequency spectrum derived from this equation and it can be clearly seen that the lower

side tones of the carrier frequency especially distort the baseband component. The level of non-linear distortion will depend on the modulation index and sampling ratio. Figure 2.14 shows calculated distortion levels for a sine wave of 6 MHz and a carrier frequency of 22 MHz. The graph indicates that a smaller modulation index results in lower non-linear distortion levels.

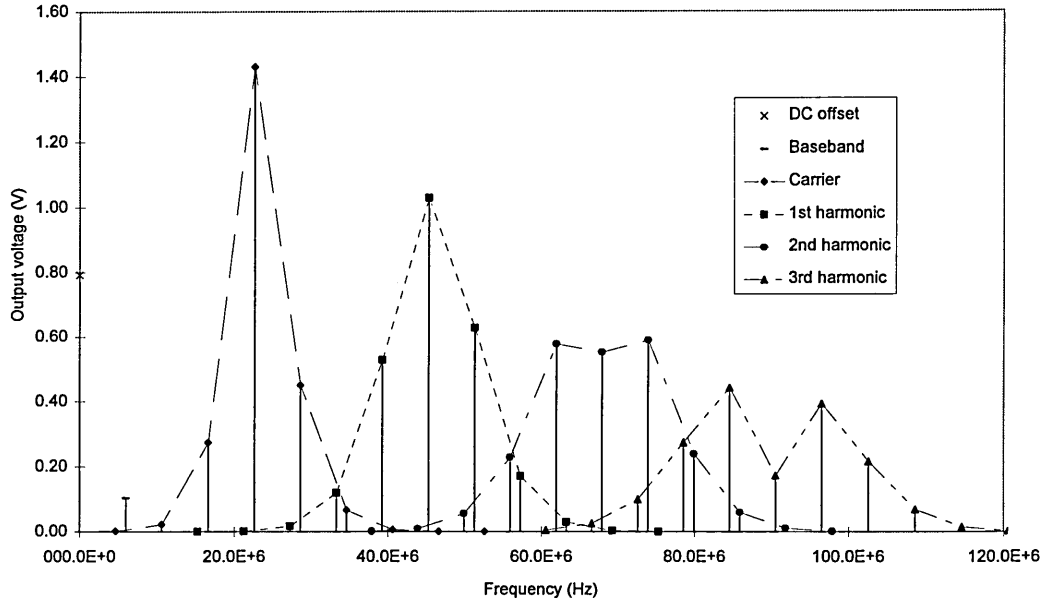

Figure 2.13: PFM frequency spectrum

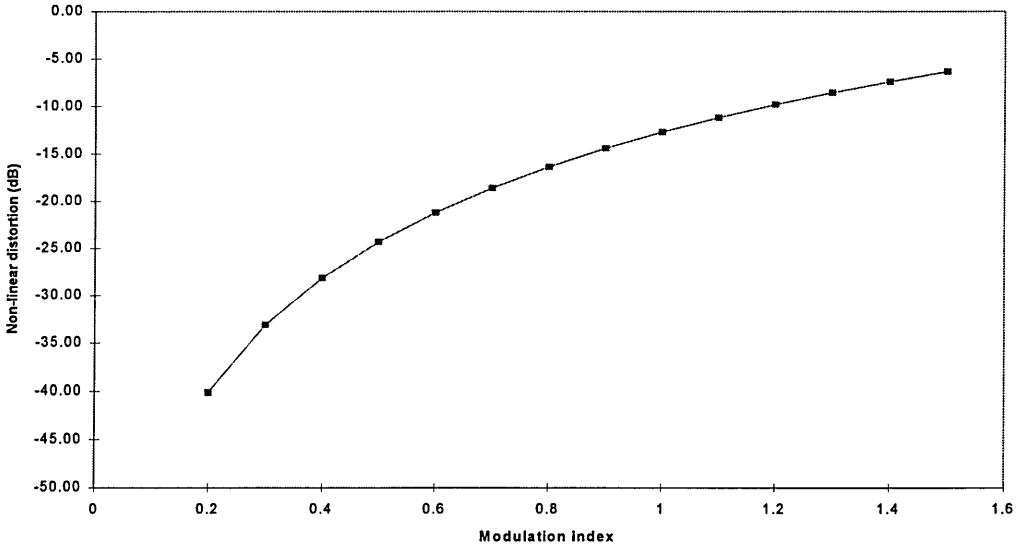

Figure 2.14: Non-linear distortion due to spectral overlap versus modulation index

2.5.2 Modulation and demodulation of PFM

PFM can be generated by employing a voltage controlled oscillator followed by pulse generating circuitry (Figure 2.15). If a VCO with sinusoidal output is used, threshold detection may be employed to change the output waveform into a square wave. If a 50% duty cycle can be achieved, this waveform would represent a SWFM signal. PFM is generated from the VCO output signal by using the pulse generating circuitry which detects rising, falling or both edges and generates a pulse of fixed width.

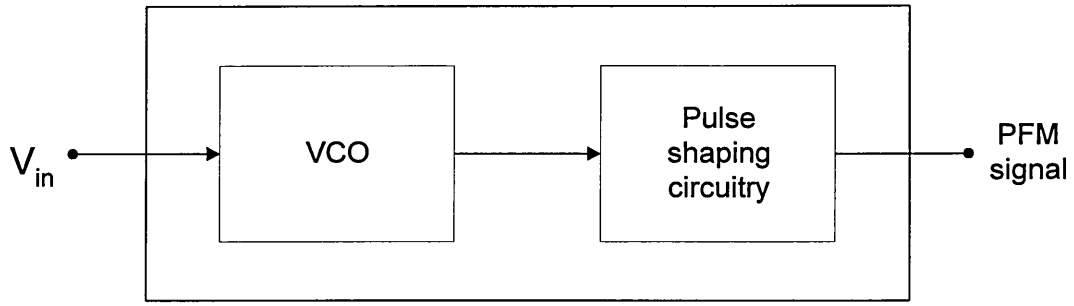

Figure 2.15: PFM modulator circuit

Since the PFM spectrum contains a baseband component, it can simply be demodulated using a low-pass filter. However, there is an alternative demodulation technique based on regeneration schemes where the received PFM pulse train is passed through a threshold detector, a constant width pulse generator and low pass filter.

By using the second method a greater SNR performance can be achieved as may be expected since the original transmitted signal is reconstructed before demodulation. The first scheme, on the other hand, provides a very simple and cost effective means of demodulation since only a low-pass filter is needed.

2.6 Summary

The development of optical fibre has renewed an interest in pulse time modulation techniques in the late 1970s and early 1980s. Since then, different modulation techniques have been investigated and some optical fibre communication systems are now being offered commercially [Optilas, 1995].

This chapter has reviewed the different PTM techniques and has given reasons why PFM is particularly favoured for the transmission of video signals through optical fibre [Heatley *et al.*, 1984; Heker *et al.*, 1988; Li *et al.*, 1992]. PFM has a lower SNR performance than PPM but it makes more efficient use of the available channel bandwidth. Demodulation is less complex than PPM requiring no clock regeneration.

Most PFM modulators consist of a VCO generating SWFM followed by some form of pulse generating circuitry. Thus several ICs are usually necessary to build up a PFM modulator. This thesis describes an investigation carried out to combine all the elements of a pulse frequency modulator on one chip thus making it easier to design PFM systems. The key advantages identified are reduced cost due to easier implementation and increased reliability due to fewer components needed to assemble such a system. Further advantages are greater system miniaturisation and better protection against reverse engineering.

CHAPTER 3

INTEGRATED CIRCUIT DESIGN

3 INTEGRATED CIRCUIT DESIGN

3.1 IC Design Overview

The history of integrated circuits so far has been very short but has been characterised by ever increasing performance and decreasing minimum dimensions. Since the first IC was produced by Kilby at Texas Instruments in 1958 [Kilby, 1976], the number of transistors per chip has increased dramatically to over 5 million in the latest processor chips. A procedure that more closely resembles today's ICs was reported by Robert Noyce of Fairchild at the beginning of 1959. Both scientists laid the foundation for what has become to be known VLSI design [Geiger *et al.*, 1990].

Silicon has replaced Germanium as the most widely used semiconductor material and, nowadays, other materials such as Gallium-Arsenide are used for special applications. Advances in technology such as improved materials or photolithography have made it possible to increase the number of functions implemented on one IC. These improvements have been matched by engineers, developing circuits which were not realisable on breadboards and having a much higher functionality. With the continuing increase in computing power, advanced computer aided design tools (CAD) have been evolved further speeding up the design cycle.

It was predicted by Moore, an electronics engineer, that the number of transistors per chip would grow exponentially [Moore, 1979]. This statement, which has come to be known as Moore's law, predicted the industrial trend towards higher integration remarkably well until the middle eighties. After this, due to the increasing complexity

and difficulties in testing of very large circuits, the transistor count per chip has not reached predicted values. However, the latest generation of microprocessor chips now contain more than 5 million transistors (Figure 3.1) [http1, 1996].

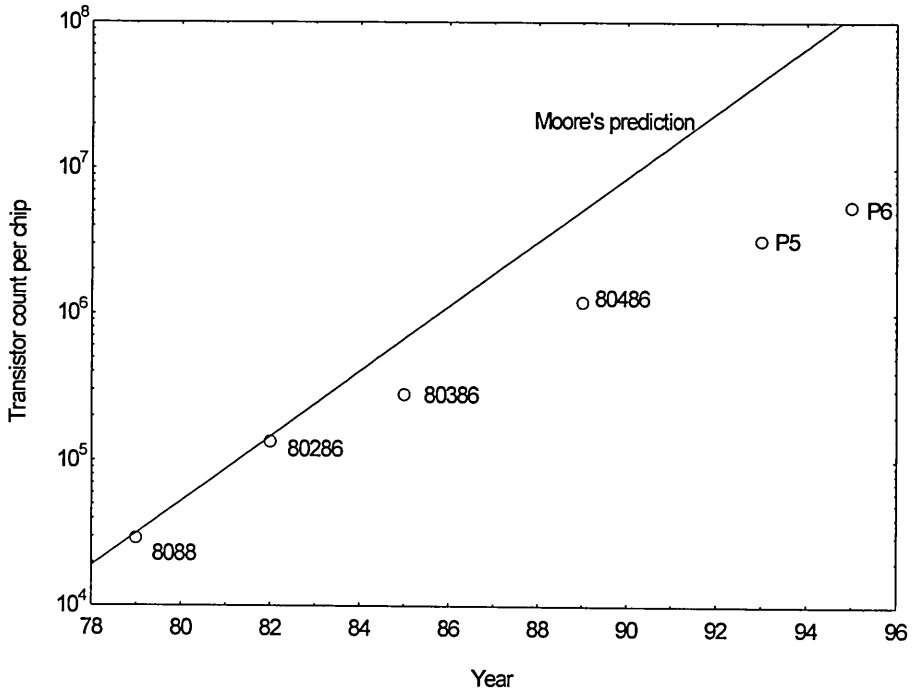

Figure 3.1: Transistor count per chip for the Intel x86 series

Although the individual feature size of transistors has been reduced significantly (with dimensions down to 0.28 μm in modern processes) the phenomenal increase in transistor count has resulted in an increase of die area per chip (Figure 3.2) [http2, 1996].

The capital cost required to produce these state of the art integrated circuits has also grown due to the much more sophisticated photolithographic equipment needed to create the designs and due to increased clean room costs to improve the yield of large wafers.

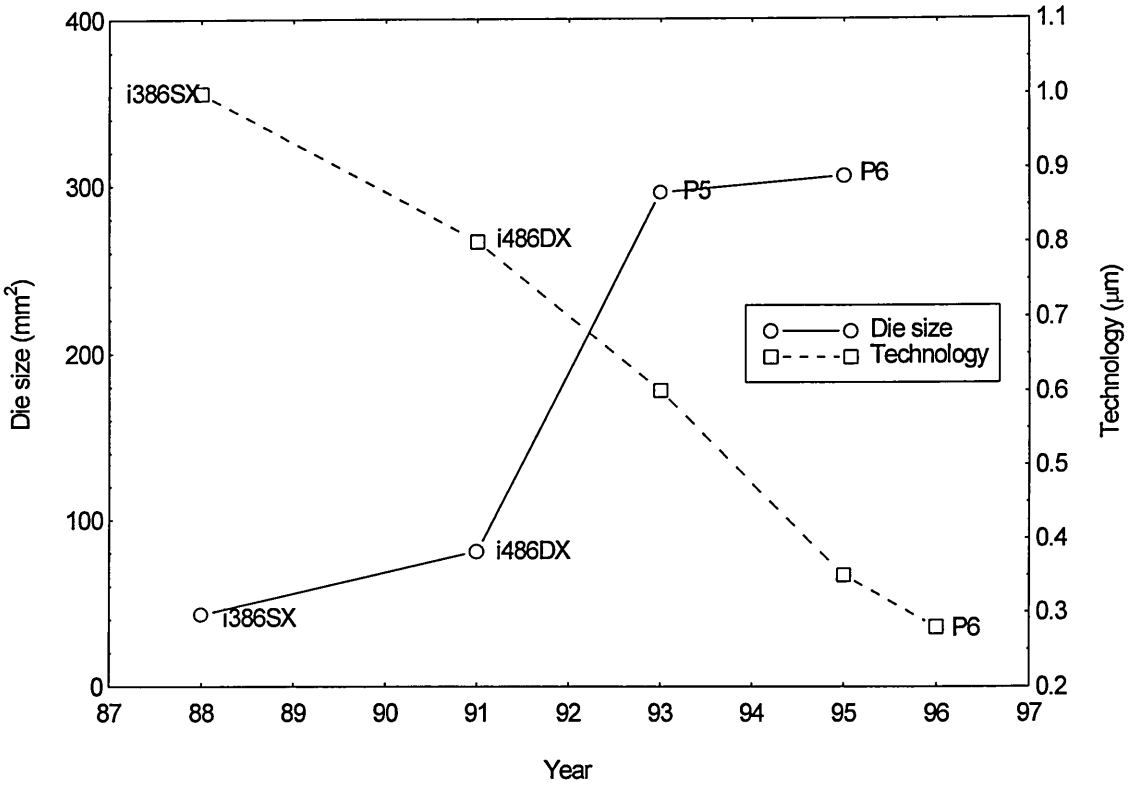

Figure 3.2: Technology advances for the Intel x86 series

3.2 Silicon Integrated Circuit Technologies

3.2.1 Technology overview

With silicon as semiconductor material, three different technologies can be categorised:

1. Bipolar
2. Complementary metal oxide semiconductor (CMOS)
3. BiCMOS (combination of the two above)

Table 3.1 lists general features of those three technologies. The choice of technology will depend on several issues related to the purpose of the product such as frequency range, operating speed, power consumption and cost.

Table 3.1: Advantages of silicon technologies

Bipolar	CMOS	BiCMOS
• Greater current drive per unit area • Better matching • Superior linear performance • Low sensitivity to process variations	• Smaller area • Higher yield • Lower parasitic capacitances • Lower power consumption • Near ideal switching device • Bi-directional • inherent memory capability	• Combines advantages of both worlds • Superior system-level performances • innovative structures (npn-PMOS merging • smart power applications **But 40% Cost Increase**

In general, the use of bipolar technology will result in higher speed and drive capabilities and better transconductance compared to CMOS technology but this is at the expense of higher power consumption and higher sensitivity to supply voltage changes. An advantage of CMOS is that its higher density allows a higher functionality per chip area. For analogue applications, bipolar offers a high gain per stage, higher bandwidth and output swing, better linearity and the implementation of precision passive components. Some of the disadvantages of CMOS for analogue purposes can be overcome by ingenious circuit designs such as cascading stages to increase the gain of amplifiers. Advantages of CMOS include a higher input impedance than bipolar and a near ideal switching characteristic making it well suited for digital designs. It also

provides a logic swing approaching the value of the supply voltage and has a superior noise voltage margin. However, bipolar devices can achieve a higher maximum switching speed [Hurst, 1992]. The difference in switching speed will reduce with the introduction of smaller geometry sizes since the speed of a CMOS transistor depends on the length of the channel, whereas the speed of a bipolar transistor depends on the width (thickness) of the base-emitter junction [Laker *et al.*, 1994].

BiCMOS combines the advantages of purely bipolar and CMOS technologies. It offers the designer the advantages of both technologies such as low noise and high switching speed of bipolar devices while maintaining active CMOS power dissipation levels. For example, an op-amp with high input impedance, large gain and high drive capability could use MOSFETs as input devices and bipolar transistors in the output stage. In addition, innovative structures such as npn-PMOS merged devices can be built allowing novel circuit designs. The disadvantage of employing BiCMOS is the increased cost since up to 18 masks are required in processing [Hurst, 1992].

The relatively lower cost of CMOS designs compared to bipolar and BiCMOS makes this technology the preferred choice even if the analogue performance is not superior. But this disadvantage can often be compensated by innovative circuit techniques. Furthermore, mixed signal circuits can benefit from the advantages that CMOS can offer for the digital part of the designs.

3.2.2 Theoretical aspects of bipolar and CMOS transistors

3.2.2.1 Bipolar transistor

A bipolar transistor is based on two pn junctions which share a common semiconductor layer. The behaviour of the bipolar transistor can be described by the *Ebers-Moll* model. Figure 3.3 shows *Ebers-Moll* circuit model of a npn bipolar transistor [Millman *et al.*, 1987].

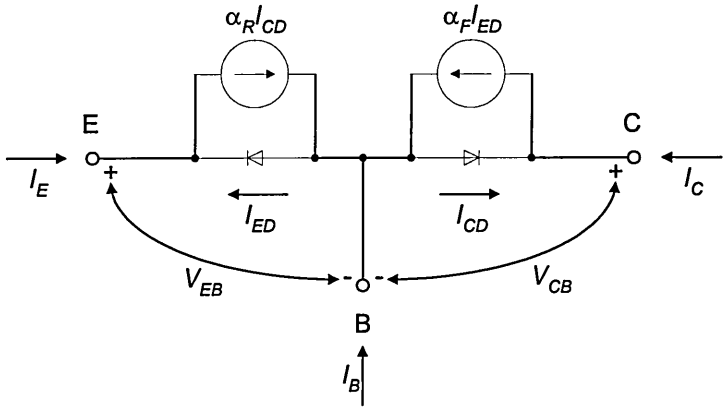

Figure 3.3: Ebers-Moll large signal representation of a npn transistor

The component $\alpha_R I_{CD}$ is that fraction of I_{CD} that is coupled through the base to the emitter. Likewise, $\alpha_F I_{ED}$ is the portion of I_{ED} coupled into the collector. The emitter (I_E) and collector (I_C) currents can now be determined from Figure 3.3 and represent the *Ebers-Moll equations* [Millman *et al.*, 1987]:

$$I_E = -I_{ES}\left(e^{-\frac{V_{EB}}{v_T}} - 1\right) + \alpha_R I_{CS}\left(e^{-\frac{V_{CB}}{v_T}} - 1\right) \qquad (3.1$$

$$I_C = \alpha_F I_{ES}\left(e^{-\frac{V_{EB}}{v_T}} - 1\right) - I_{CS}\left(e^{-\frac{V_{CB}}{v_T}} - 1\right) \qquad (3.2)$$

with $v_T = kT/q$ where k is the Boltzmann constant, T is the temperature and q is the charge of an electron. The four components I_{ES}, I_{CS}, α_F and α_R are functions of doping density and transistor geometry. Realising that the sum of the terminal currents must be zero, the base current may be written as:

$$I_B = -(I_E + I_C) \tag{3.3}$$

3.2.2.2 CMOS transistor

The metal oxide semiconductor field effect transistor (MOSFET) is the building block of the CMOS technology. Here, the conductivity of a channel is controlled by an electric field developed between an insulated 'gate' electrode and the conducting channel. The gate/oxide/channel combination forms a capacitance known as the gate capacitance. The voltage applied to the gate controls the conductivity of the channel. A current can flow through the channel provided a positive voltage is applied to one end of the channel and a negative to the other end.

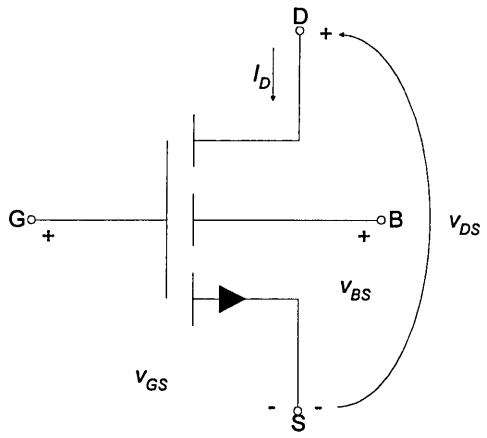

Figure 3.4: Variable and sign convention for an n-type MOS transistor

Depending upon the value of 'v_{GS} - V_T' (V_T is the threshold voltage of the transistor), various regions of operation of the MOS transistor can be determined.

Cut-off region (v_{GS} - $V_T \leq 0$):

$$I_D = 0 \tag{3.4}$$

Ohmic region ($0 < v_{DS} \leq v_{GS}$ - V_T):

$$I_D = k\frac{W}{L}\left[2(v_{GS} - V_T)v_{DS} - v^2{}_{DS}\right](1 + \lambda v_{DS}) \tag{3.5}$$

where W is the channel width, L the channel length, λ is the channel length modulation parameter and k the transconductance parameter. The transconductance parameter $k = \mu_n C_{ox}/2$, where μ_n is the electron mobility and C_{ox} is the gate capacitance. Both parameters are process dependent.

Saturation region ($0 < v_{GS}$ - $V_T \leq v_{DS}$):

$$I_D = k\frac{W}{L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}) \tag{3.6}$$

3.2.2.3 Comparison of bipolar and MOS transistor

By comparing the basic transistor equations for bipolar and CMOS devices some design principles can be concluded. The current flow through the bipolar device is controlled by a current whilst the current through a MOS transistor is controlled by a voltage. Furthermore, the characteristic of a MOS transistor is strongly dependent upon its geometry resulting in different circuit configurations for bipolar and CMOS technologies. In CMOS, for instance, the designer can change the performance of an operational amplifier by changing the transistor geometries. This is not easily achieved in bipolar [Sansen, 1994].

3.3 IC Design Methodologies

The increased functionality of ICs has made it necessary to develop design methodologies to simplify design problems and enable members of a design team to work together simultaneously. The design strategies can be divided into:

1. Bottom up design
2. Top down design
3. Combination of both

In the bottom up approach the designer starts at the bottom by specifying the technology and then developing the system from transistor or gate level. Using the second approach, the circuit is designed starting from a system level description derived from the specification. This approach is normally used in digital designs resulting in an increased productivity. The design is repeatedly split into groups of simpler sub-structures until the lowest level (simple gates) is reached. These may then be implemented in silicon using precompiled standard cells. This approach is also well suited for the application of hardware description languages (HDL). Efforts have been made to allow the use of the top down approach in analogue designs but the requirements for those circuits are too stringent and cannot, at present be met with this design methodology [Szepesi *et al.*, 1994].

The third methodology combines the features of the previous two. It may be used in designs where analogue and digital parts are included. It enables the designer to decompose the design into functional blocks which are already fully understood. The

bottom up approach is then applied to implement those functional blocks in silicon [Schwarz, 1993].

3.4 Custom Integrated Circuit Design

The circuit requirements for every electronic product will be very specific and unique to that product. A designer would traditionally use standard electronic components and sub-assemblies to generate the product. Using custom integrated circuits (circuits made for a specific product and containing all the functionality of that product) gives several advantages, such as fewer components, a smaller physical size, better reliability due to fewer connections between components. For some applications the reduced power and performance enhancements may also be of importance.

Different categories of custom ICs can be distinguished. In **full-custom** design the chip layout is developed and fully optimised for a particular application at mask level. **Standard cell** ICs rely on a precompiled library of standard circuit elements which can be automatically placed and wired by CAD tools. **Gate arrays** are prefabricated ICs with circuit elements already in place. Only the final interconnections between those cells have to be custom designed and made. The last two categories are also called semi-custom designs and mostly used for digital circuits [Davidse, 1994].

Full-custom designs are usually more expensive and time consuming than semi-custom designs and will only be economical for large volume production due to reduced silicon area. In semi-custom designs, gate arrays will be more cost efficient compared to

standard cells due to reduced cost involved for the mask layout but depending upon the production volume, the reduced die area for standard cell designs may make this approach more cost efficient.

Programmable logic devices (**PLDs**) are a special group of custom ICs. PLDs are able to realise any required logical function within the capacity of the device. Early PLDs were restricted to the implementation of Boolean functions which could be written in a sum-of-product form. Modern devices include flip-flops which may be used as memory elements. More recently field programmable gate arrays (**FPGAs**) have become widespread. These complex VLSI circuits consist of circuit cells and interconnecting segments which may be programmed to create any digital function required. They are ideally suited for the production of prototypes and also for cost effective chip design, especially for low volume applications [Kang *et al.*, 1996]. Currently PLDs and FPGAs are only generally available for digital custom ICs [Hurst, 1992].

Figure 3.5 shows the custom IC overview. It can be seen that the semi-custom ICs are mostly used for digital designs, although some research has gone in the application of transistor arrays for analogue applications [Declercq, 1994].

3.5 Computer Aided Design Tools

Increased computer performance has enabled significant advances in the computer aided design tools. The first IC designs were totally hand drawn using large drawing boards.

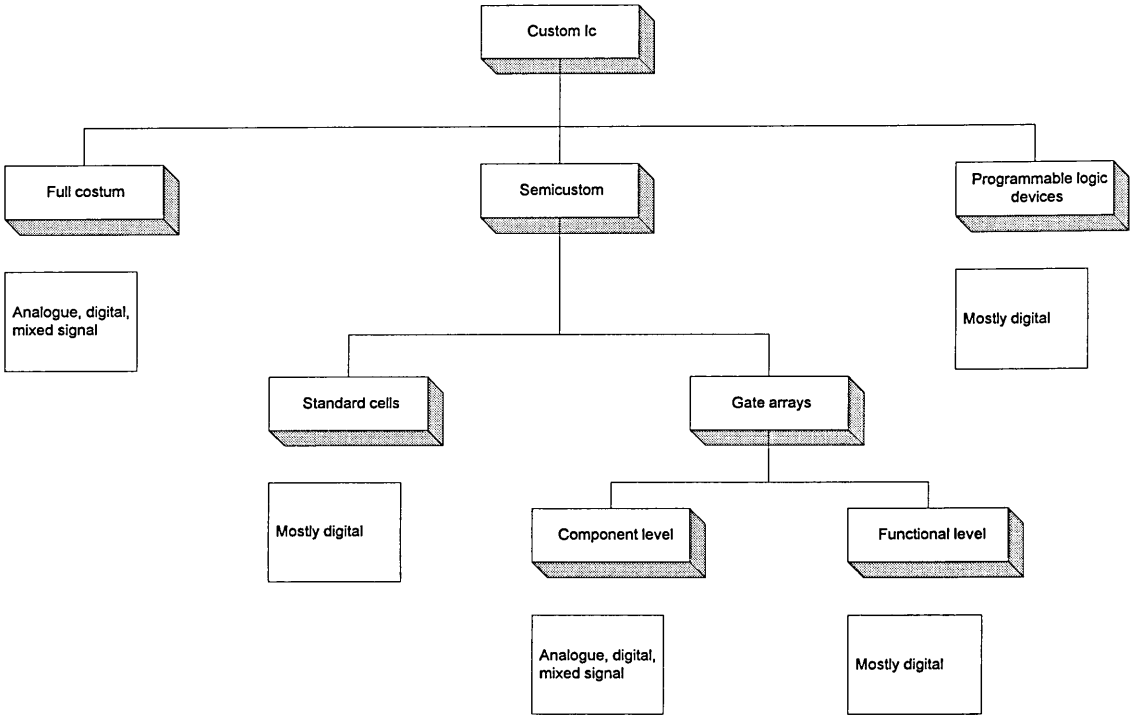

Figure 3.5: Custom integrated circuits overview

The mask layouts were again cut by hand using dimensionally stable plastic sheets. This procedure was very costly and ineffective due to many errors occurring in the layout.

With increases in computing power, the designer has seen a corresponding increase in support from CAD tools which have improved substantially over the years. Earlier problems such as verification and validation of IC designs could be automated and simulation times could be decreased.

Nowadays, CAD systems are truly hierarchical and all design phases access a common database. Thus, the computer helps the designer in all aspects of design management

integrating standard design tools in a common framework. Figure 3.6 shows the general design methodology adopted using CAD tools in a common framework.

3.6 EUROPRACTICE IC Technologies

3.6.1 EUROPRACTICE

The proposed IC has been fabricated through the EUROCHIP/EUROPRACTICE program. EUROCHIP was part of the ESPRIT VLSI DESIGN ACTION and provided its academic member institutions with a range of services including purchase and support of CAD software, access to chip fabrication, discounts on test equipment and training. The program terminated in September 1995 and was followed by EUROPRACTICE which aimed to stimulate wider exploitation of state-of-the-art technologies by European Industry. The IC Manufacturing Service (ICMS) co-ordinated by IMEC (Belgium), is the EUROPRACTICE service for low cost IC prototyping, volume and testing.

Taking into account cost and the considerations discussed in section 3.2, it was decided to investigate the usage of the Alcatel MIETEC 2.4 μm CMOS process for this work. Although the usage of the MIETEC 0.7 μm CMOS technology would have been more suitable the prototyping cost would have at least quadrupled. Also, the Mentor Graphics' analogue design kit was only made available in late 1995. General information about the MIETEC 2.4 μm CMOS technology can be found in Appendix A.

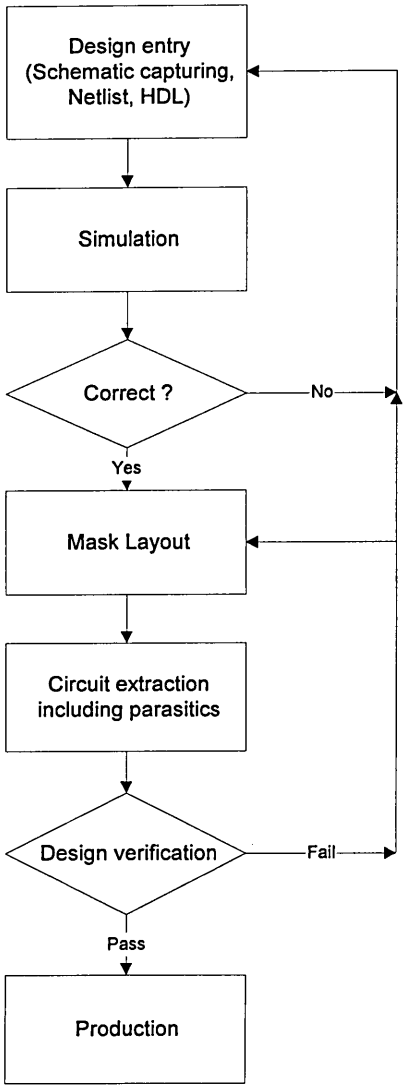

Figure 3.6: Design methodology using standard CAD tools in a common framework

ICMS offers access to CMOS, BiCMOS and GaAs processes from different foundries including technologies ranging from 2.4 μm digital/analogue CMOS and 0.5 μm digital CMOS to 0.8 μm BiCMOS. An ASIC bipolar array for fast turn-around analogue circuits is also offered together with GaAs processes. An up-to-date list can be found on IMEC's WWW page [http3, 1996].

3.6.2 Performance consideration for the MIETEC 2.4 μm technology

One of the prime criteria to satisfy is whether the chosen technology can deliver the speed required for modulating video signals. This requirement can be proven by analytical expression, simulation and practical measurement. This chapter presents results from analytical expressions and initial simulations; practical measurements are presented in Chapters 6 and 7.

Maximum frequency of operation

Laker and Sansen [1994] have shown that the maximum operating frequency f_{max} of a CMOS transistor may be written as:

$$f_{\max} = \frac{1}{2\pi} \frac{\mu}{L_{eff}^{\ 2}} (v_{GS} - V_T) \tag{3.7}$$

where μ is the channel mobility, L_{eff} is the effective channel length and v_{gs} and V_T are the gate-source and threshold voltage, respectively. The maximum frequency will be in the Gigahertz region for the chosen technology and should therefore be sufficiently high. But this is the maximum frequency of a single transistor where neither interconnections, parasitic elements nor subsequent stages are taken into account.

In order to prove the feasibility of this technology further, a digital circuit was simulated and its rise and fall times were measured. A Schmitt trigger was chosen as a test circuit [Filanovsky *et al.*, 1994]. With a capacitive load of 0.5 pF the rise and fall times were

24 ns and 11 ns, respectively, resulting in a possible operating frequency of 28 MHz which should be sufficient to meet the requirements as set in section 2.4 (Figure 3.7).

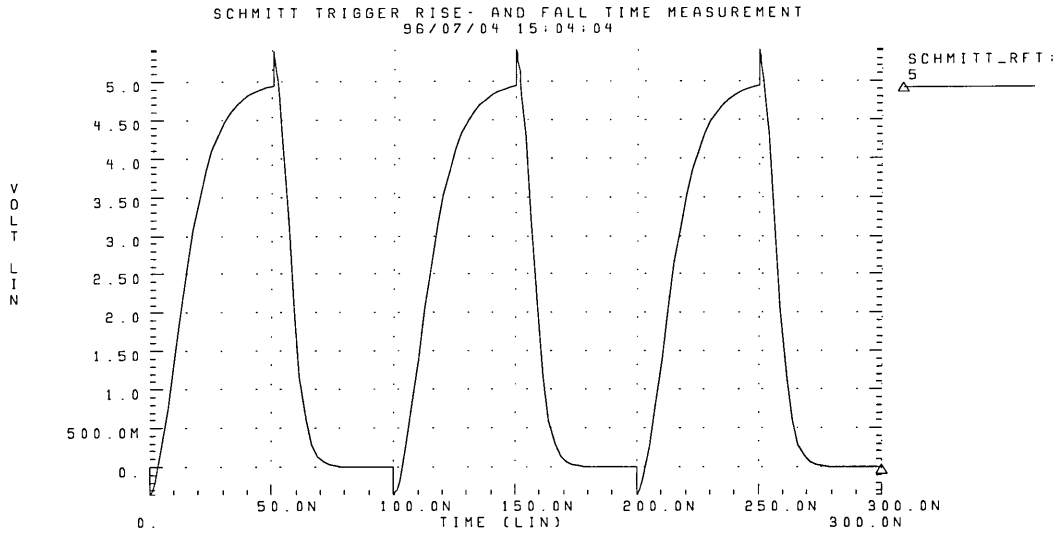

Figure 3.7: Simulated Schmitt trigger output waveform

3.7 Design Environment

All the IC design work was carried on a HP712/60 workstation running Mentor Graphics (MG) version A1F and META HSPICE version 95. Although an analogue simulator (ACCUSIM) is included in the MG framework this was not used due to the fact that it was based on an earlier version of SPICE (2G6) and frequently showed convergence problems for even simple circuits. HSPICE has built-in routines which avoid the problems encountered with ACCUSIM. In addition, HSPICE netlists are easily generated from IC Station (the IC mask layout editor of MG).

The design flow which has been adopted combines both the top down and bottom up approach. The PFM modulator is split into several functional blocks using the top down

method whereas each functional block is designed employing the bottom up method. Schematic capturing and mask layout is done using Design Architect (DA) and IC Station and simulations are carried out by generating a netlist and transferring it into HSPICE.

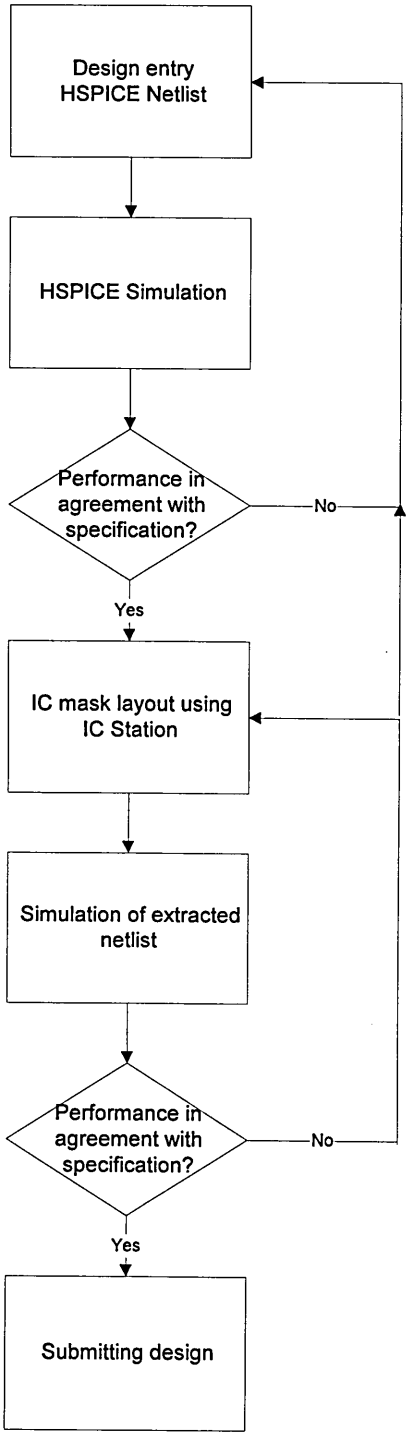

Figure 3.8: Adopted design flow

The adopted design flow for implementing the functional blocks is shown in Figure 3.8. The initial design idea is transformed into a SPICE netlist and simulated using HSPICE. This allows easy alterations to optimise the performance of the circuit. Once the circuit is finalised, the mask layout is created using IC Station. In order to ensure a correct mask layout, schematic capturing of the circuit using DA is needed. This allows a comparison of finalised mask layout and circuit schematics to be carried out.

After the layout has been finalised and passed the design rule check (DRC), a SPICE netlist is extracted which can include lumped parasitic capacitances. This circuit netlist is again simulated with HSPICE and if the performance is satisfactory, the layout can be prepared for design submission at IMEC. More detailed information about the implementation of the MIETEC technology into the IC layout design flow can be found in Appendix D.

3.8 Summary

This chapter has shown that advances in telecommunications have been matched by circuit designers trying to miniaturise parts needed for implementing these transmission systems. Examples are single chip FM and AM demodulators for radio receivers or even entire radios comprised on a single integrated circuit [http4, 1996].

This chapter has also considered the available silicon integrated circuit technologies for implementation of the design. Bipolar technologies would offer a higher operating speed than CMOS technologies but this would be at the expense of higher cost and

power consumption. Preliminary simulations have shown that the proposed Alcatel MIETEC 2.4 μm CMOS technology should be able to deliver the required operating speed and this technology was therefore chosen due to its low cost and ease of implementation within the existing CAD design environment.

CHAPTER 4

FULL-CUSTOM INTEGRATED CIRCUIT LAYOUT

4 FULL-CUSTOM INTEGRATED CIRCUIT LAYOUT

Full-custom layout can occupy a large proportion of the total design time and has a great impact upon the performance of the final product. Different applications usually demand different layout specifications. Analogue linear circuits, for instance, may require accurate component matching whereas digital circuits may be optimised for switching speed. In general, the IC layout must satisfy the electrical specifications within certain tolerances while optimising the silicon area used.

Full-custom designs can be interpreted as IC designs at silicon level with complete flexibility to design the individual transistor and the floorplan with no design restriction placed upon the designer [Hurst, 1992].

Electronic components such as transistors, diodes, resistors or capacitors and their interconnecting wires are assembled two-dimensionally on an integrated circuit. All devices are arranged on the surface of the silicon wafer, each one having a structure that either extends into the body or is attached to the surface of the wafer. IC layout design assigns to each component a certain area of silicon wafer usually extending to several layers. The manufacturing process may involve deposition or removal of materials in certain areas of the wafer. Areas which should not be effected by a particular processing step have to be protected. Therefore, for each wafer a set of masks is required which separates effective and non-effective areas and supports a specific manufacturing step (e.g. diffusion, metallisation). The actual IC is fabricated by using

this set of mask sequentially, with each mask comprised of geometric primitives such as rectangles and polygons.

IC layout design basically involves the mask layout of the actual IC. This is achieved with the use of either interactive or automatic layout generation tools. Interactive layout generation is usually employed for full-custom designs where as automatic tools are used in semi-custom designs. The graphical information for each mask is extracted from the finalised IC layout.

4.1 The CMOS Process

4.1.1 Structure of a MOSFET

The metal oxide semiconductor field effect transistor (MOSFET) is the basic active building block of the complementary metal oxide semiconductor (CMOS) technology. The conductivity of a field effect transistor is controlled by an electric field, in contrast to the bipolar transistor where the conductivity is controlled by a pn-junction. Figure 4.1 shows a general cross-section of a MOSFET with L the length and W the width of the channel. The thickness of the thermal oxide (t_{ox}) is approximately 100 nm or less [Geiger *et al.*, 1990]. L_{eff} represents the effective channel length which is smaller than L, and its value depends upon the process used. The lateral diffusion (X_{jl}) is important in order to determine the gate-drain and gate-source overlap capacitances. The metallurgical junction depth (X_j) is used to define the sidewall capacitances of drain and source junctions.

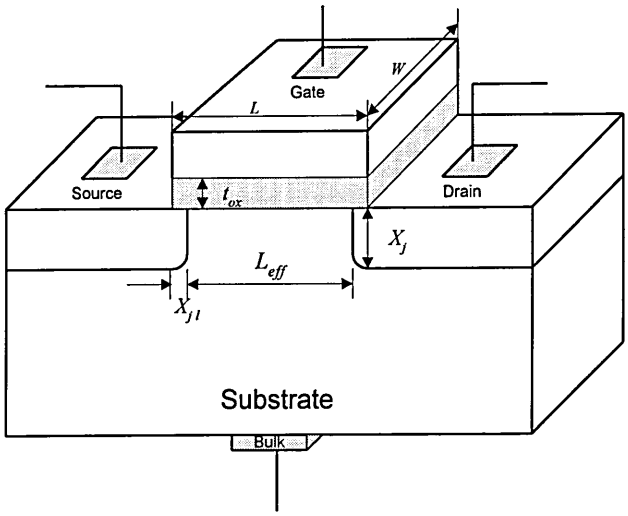

Figure 4.1: Cross-section of a MOSFET

Figure 4.1 shows clearly that the MOSFET is a symmetrical device, i.e. its properties are the same when drain and source terminals are exchanged. The conductivity of the channel is basically controlled by a voltage applied to the gate terminal. The gate is insulated from the channel by a very thin dielectric material, silicon dioxide (SiO_2). There is, therefore, almost no gate current and the transistor exhibits a very large input impedance. However, this thin dielectric causes a relatively high gate capacitance.

There are two different types of MOSFETs, p-type and n-type. P-type devices have a lightly doped n-type substrate with heavily doped p-type drain and source areas. The doping is reversed for n-type devices. Each type of transistor can also be either depletion or enhancement mode. For depletion mode transistors, a current flow from drain to source is possible even though there is no gate voltage present. A gate voltage is needed when using the enhancement mode transistor to allow a current flow from drain to source.

4.1.2 Complementary metal oxide semiconductor (CMOS)

The CMOS process combines n-type and p-type MOSFETs in one single technology. A principle cross-section of the MIETEC 2.4 μm CMOS technology is given in Figure 4.2. This is a n-well process with two metal layers for interconnections and two polysilicon layers to form on-chip capacitances. On-chip resistances can be made of n-well, active area or polysilicon.

The substrate is lightly p-doped. The n-MOST can therefore be implemented by diffusing a n+ implant. A lightly doped n-region, the so-called n-well, is needed to implement the p-MOST.

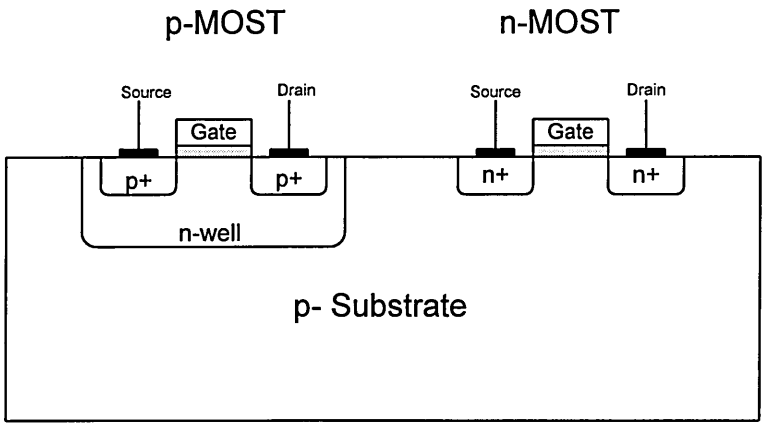

Figure 4.2: Principle cross-section of MIETEC 2.4 μm CMOS technology

4.2 IC Layout

IC layout is concerned with designing the masks needed for IC fabrication. This requires the three-dimensional concept of the circuit described above to be transformed in a two-dimensional top view of the device.

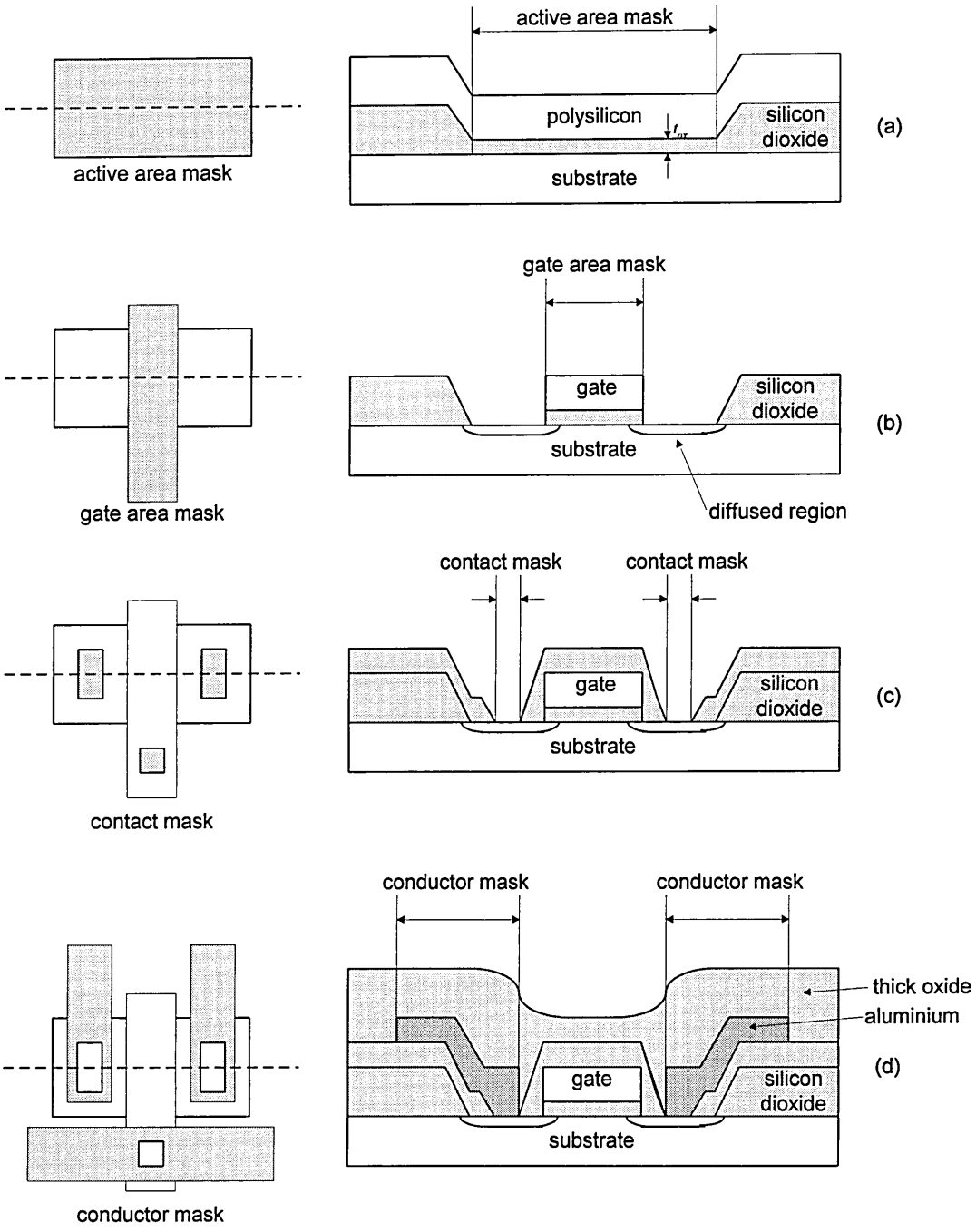

Figure 4.3: Simplified fabrication of a MOS transistor

Figure 4.3 shows a simplified example of how the mask layout information is used to fabricate a MOSFET. As a first step in the MOS production, a relatively thick layer of thermal oxide, about 1μm, is built up which is then fully removed from the regions where the transistor will be located, thus forming the active area. The next step involves

the build up of another layer of thermal oxide but much thinner than the previous one (about 100 nm or less (t_{ox})). In the next stage, the whole wafer will be covered with polysilicon as illustrated in Figure 4.3a. Polysilicon is a conductive layer and is used later as the gate area. In older processes this layer was made of aluminium and the process was therefore called Metal Oxide Semiconductor process (MOS).

The gate area mask, covering all the later gate regions, is then processed and all thin oxide areas (t_{ox}), not covered by the gate area mask, are totally removed by etching. In these regions, a high concentration of n- or p-type dopant is thermally diffused inside the substrate. The diffused regions have become the source and drain of the transistor as shown in Figure 4.3b. The distance between the two diffused regions underneath the gate polysilicon layer is known as the effective channel length (L_{eff}).

After covering the whole wafer again by thermal oxidation the contact mask is used to remove oxide from the regions where contacts will be made, Figure 4.3c. The conductor mask is used to apply metal interconnections and contacts to the diffusions and to the gate layer, Figure 4.3d. As a final step a passivation layer of thick insulating material (SiO_2) is used to prevent the chip from chemical contamination.

4.3 Optimisation of Folded MOS Transistor Layouts

MOS transistors used in analogue integrated circuit designs can have large width to length (W/L) ratios in order to provide high current drive capabilities and to increase high frequency performance. These large ratios results in geometries which are difficult

to incorporate in constraint IC layouts. To use costly silicon chip area efficiently, the individual modules must be designed to be as compact as possible. This may be achieved by splitting a single transistor into several smaller units and connecting them in parallel. This has the additional advantage that the values of parasitic capacitances associated with this transistor will become smaller. It is therefore necessary to analyse the relationship between the transistor's inherent parasitic capacitances and those of its interconnections to enable the designer to trade-off transistor design shape against magnitude of parasitic capacitance.

4.3.1 Parasitic elements in ICs

Parasitic elements are introduced by interconnecting wires, contacts and the MOS transistor itself. The dynamic response of MOS systems is highly dependent upon parasitic capacitances and resistances.

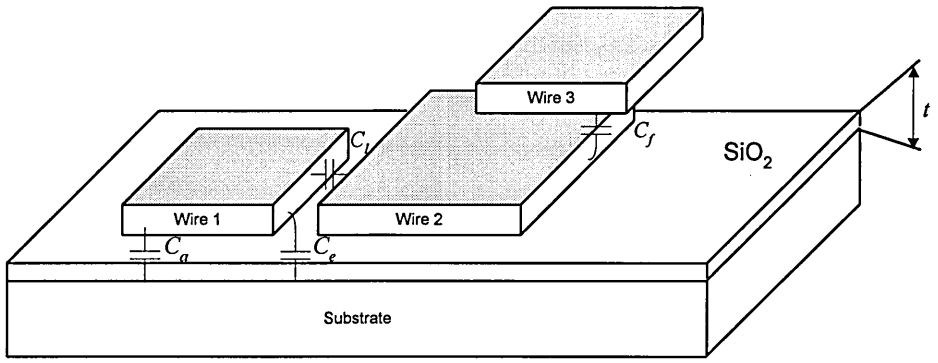

Figure 4.4: Parasitic capacitances of interconnection wires

Several parasitic elements can be identified in an IC. The sheet resistance is associated with conducting layers; contact resistances occur where two different conducting layers are interconnected. Layer and diffusion capacitances are associated with conducting

layers and transistors. As an example, Figure 4.4 shows parasitic capacitances between interconnecting wires. These are area (C_a), lateral (C_l), edge (C_e) and fringe (C_f) capacitances. These parasitic elements cannot be avoided but careful layout of transistors and interconnections can reduce their value and their influence upon the circuit performance.

4.3.2 Transistor layout methodologies

Three different MOS transistor layout styles, with the same *W/L* ratio, which are used in integrated circuit design are illustrated in Figure 4.5.

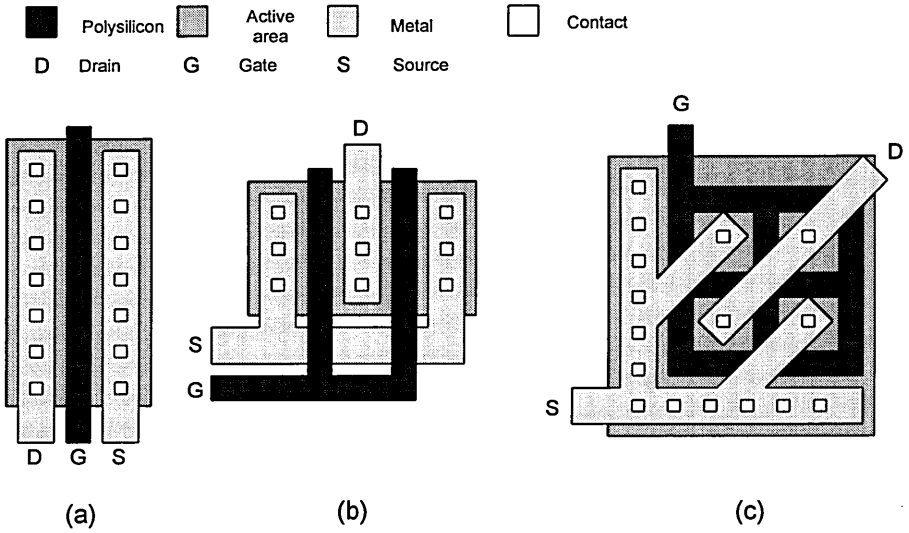

Figure 4.5: Different layout styles of MOS transistors (a) simple (b) folded (c) waffle

The simplest transistor is a straight forward design (Figure 4.5a) with one gate and a relatively large drain and source area and where minimum areas are defined by the design rules. A better transistor performance, with the same *W/L* ratio is achieved by 'folding' the simple transistor as shown in Figure 4.5b. This new design style is called a *interdigit design*, where the main improvement is a reduction in drain area and effective

perimeter by approximately 50%. Figure 4.5c shows another variation, the *waffle iron* design which offers the lowest junction capacitance of all three designs. However, the waffle design's noise performance is worse due to the large bulk resistance [Steyaert *et al.*, 1993] and has a higher gate capacitance than the interdigit design [Vemuru, 1992].

The drain- (source) bulk junction capacitance C_{db} consist of two parts, the bottomwall junction capacitance C_{dbj} related to the drain-bulk (source-bulk) area and the side-wall junction capacitance C_{dbjsw} related to the drain (source) periphery. C_{db} can be approximated for each layout type 'a', 'b' and 'c' in Figure 4.5 [Steyaert *et al.*, 1993]:

(a) Simple design: $$C_{db_a} \approx W \cdot L_{edge} \cdot C_{dbj} + (W + 2 \cdot L_{edge}) C_{dbjsw} \quad \textbf{(4.1)}$$

(b) Folded design: $$C_{db_b} \approx \frac{1}{2} W \cdot L_{edge} \cdot C_{dbj} + 2 L_{edge} \cdot C_{dbjsw} \quad \textbf{(4.2)}$$

(c) Waffle design: $$C_{db_c} \approx \frac{1}{4} W \cdot L_{edge} \cdot C_{dbj} \quad \textbf{(4.3)}$$

where L_{edge} is the drain (source) diffusion area length, W is the channel width (for designation see Figure 4.9). C_{dbj} and C_{dbjsw} are technology dependent parameters and normally provided by the foundry. Simplification of the above equations (usually $C_{dbjsw} << C_{dbj}$) results in [Steyaert *et al.*, 1993]:

$$C_{db_a} \approx 2 C_{db_b} \approx 4 C_{db_c} \quad \textbf{(4.4)}$$

From equation (4.4) it can be concluded that, with a simple design, the use of the interdigit design can double the switching speed of a circuit. The high frequency performance of the waffle structure layout can exceed that of the simple structure by a factor of four.

4.3.3 Folding of a simple MOS transistor layout

Folding a simple MOS transistor layout involves splitting the transistor into several smaller ones with the same reduced gate width and original gate length and connecting all the fragmented gates together in parallel. The more the transistor is folded the smaller the drain and source areas become, i.e. junction capacitances are reduced. However, the areas of conducting layers which connect common gates, drains and sources are increased (Figure 4.5a and b).

In Figure 4.6 a single n-channel transistor (NMOST) is shown with a *W/L* ratio of 150/3 and different degrees of folding. A simple transistor (n = 1) consists of a single gate, whereas a transistor folded once (n = 2) has two separate gates but note the width of each gate is reduced to half of the width of the unfolded transistor. The main advantage is realised when using one common drain area for two separated gates (Figure 4.5b) since this results in a decreased junction capacitance and a more compact design shape which is easier to incorporate into the whole chip design.

The aspect ratio of a complete IC layout is usually determined by the IC package used. Normally, a square layout is the preferred choice since the cavity of an IC package is square. With a large *W/L* ratio, a transistor exhibits a geometry which is very difficult to implement. Therefore, the design shape of single transistors should be as compact as possible making it easier to achieve the desired aspect ratio of the overall IC layout.

The number of gates of a folded transistor may be defined by its folding grade (n). It can be seen that for this specific W/L ratio of 150/3 and at a folding grade of four (transistor has got four parallel gates) the design shape is almost square.

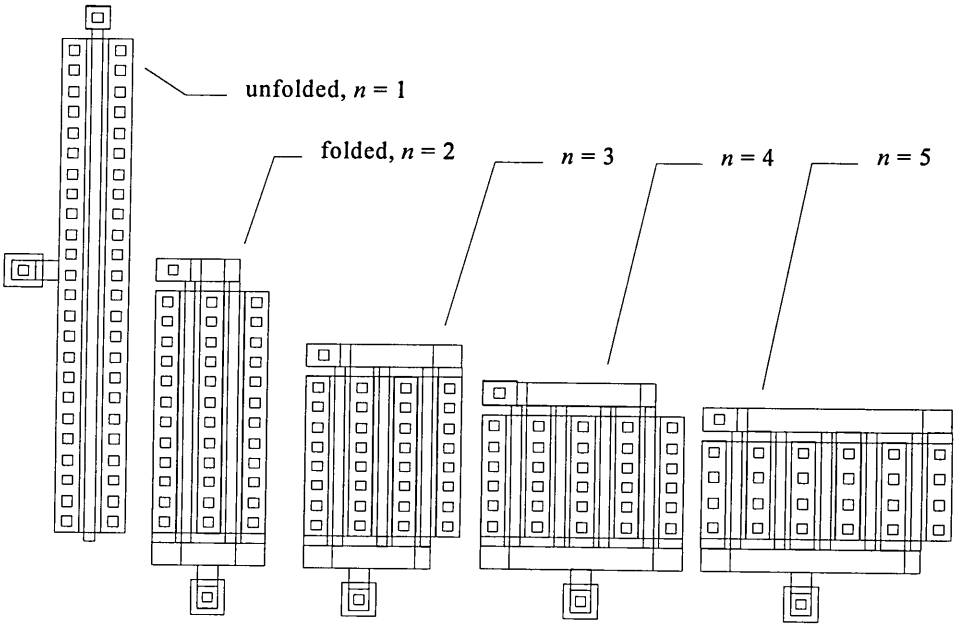

Figure 4.6: NMOST folding grade $n = 1..5$

A cross-section of a single gate transistor is shown in Figure 4.7. There are two major sources of parasitic capacitances which effect the switching performance of the transistor. These are the drain-bulk junction capacitance (C_{db}) made up of the bottomwall (C_{dbj}) and the sidewall (C_{dbjsw}) capacitances and the lumped parasitic capacitance caused by the interconnection layers (C_{in}) (this capacitance may be split into two contributions, one related to the area overlapping the free substrate and the other overlapping the drain region). Since the MOSFET is a symmetrical device, the capacitances related to the source are equal to those related to the drain and are therefore not illustrated in Figure 4.7. Capacitances connected to the gate (gate overlap capacitances) can be assumed constant for wide transistors [Steyaert *et al.*, 1993]. Since

folding is only employed for wide transistors, these capacitances will, therefore, not be dependent upon the folding grade and may be ignored.

The aim of folding is to find an optimum between compact layout and minimum interconnection and junction area (hence their capacitances) to achieve in this case the highest possible switching performance.

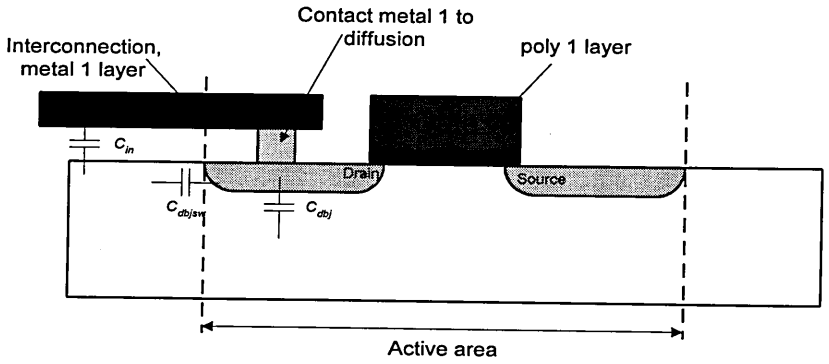

Figure 4.7: Cross-section with interconnection and junction capacitances

4.3.4 Calculation of parasitic capacitances of a folded MOS transistor layout

It can be deduced from Figure 4.7 that the parasitic capacitances are related to the drain and source junction areas and perimeters and the interconnection areas. These areas and perimeters have to be related to the folding grade to calculate the parasitic capacitances associated with the transistor layout.

The different layers of a folded transistor with $n = 3$ are shown in Figure 4.8. The area reduction of the interconnecting layers overlapping the drain and source regions matches the reduction in the drain and source areas, i.e. the same equations apply.

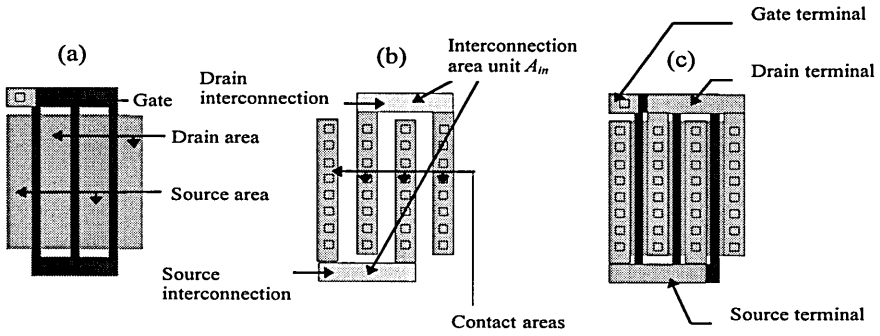

Figure 4.8: NMOST with folding grade $n = 3$

4.3.4.1 Areas of diffused regions

Equations describing the decrease in drain-bulk A_{db} and source-bulk A_{sb} areas as a result of folding differ according to whether the folding grade n is odd or even (Figure 4.6). If n is odd the reductions in A_{db} and A_{sb} are the same and both areas can be expressed as [Gatti *et al.*, 1994]:

$$A_{db,sb} \approx \frac{n+1}{2n} A_0 \tag{4.5}$$

where A_0 is the original drain-bulk or source-bulk area of the unfolded transistor as shown in Figure 4.9. For high folding grades, $A_{db,sb}$ converges to half its original value A_0.

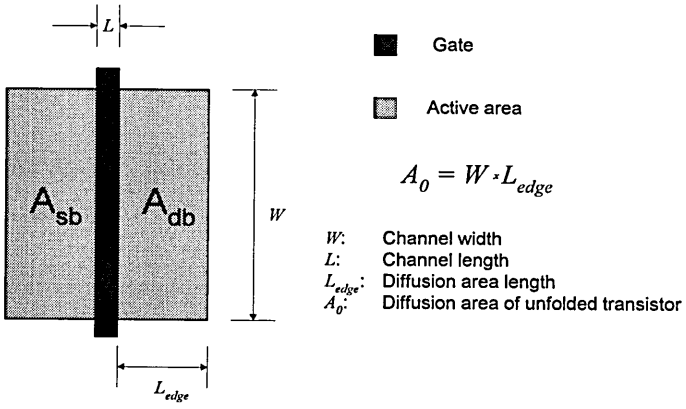

Figure 4.9: MOST area designation

If n is even the reduction in A_{db} is different from A_{sb}. Assuming that the smaller area is used as drain then A_{db} is constant in this case and its value is given by [Gatti *et al.*, 1994]:

$$A_{db} \approx \frac{1}{2} A_0 \tag{4.6}$$

Also, the source-bulk area is now given by [Gatti *et al.*, 1994]:

$$A_{sb} \approx \frac{n+2}{2n} A_0 \tag{4.7}$$

Thus for high values of n the drain-bulk area remains constant and the source-bulk area converges to half of its original area.

Figure 4.10 illustrates the area reduction for both, odd and even folding grades.

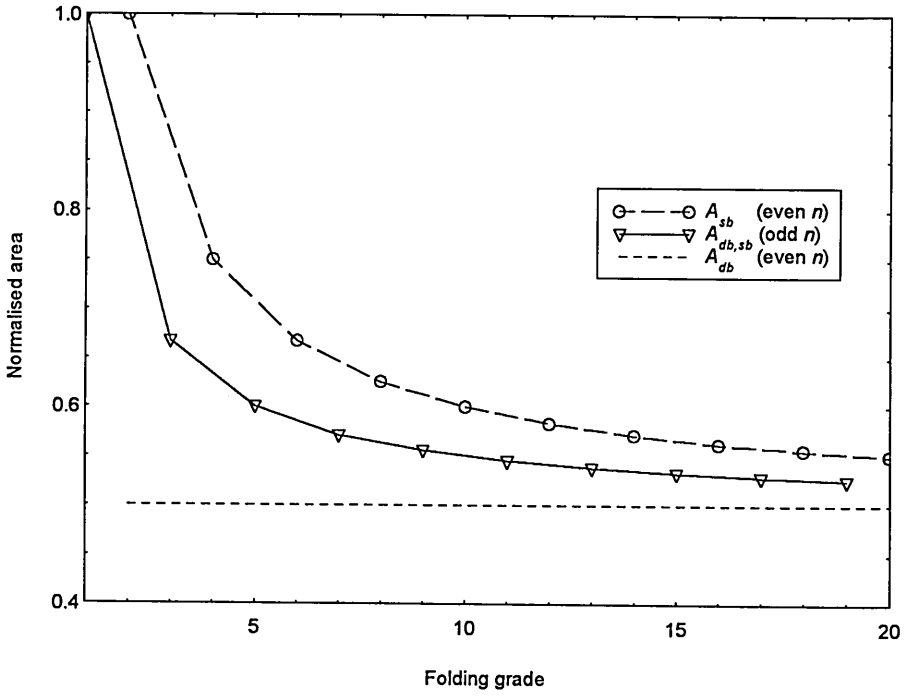

Figure 4.10: Drain-bulk and source-bulk area reduction

4.3.4.2 Perimeter of diffused regions

Junction capacitances are related to the sidewall regions, which can be calculated if the perimeters of drain and source regions are known. Algorithms defining the perimeter value which gives rise to sidewall junction capacitances differ from those implemented in HSPICE and those published in the literature [Tsividis, 1988, de Graaff *et al.*, 1990].

The algorithm implemented in HSPICE is known as ACM=2 (Area Calculation Method number two). This method was used within the transistor models for HSPICE simulations provided by the foundry. In these, the drain and source sidewall lengths contacting the channel are included whereas in published calculations only the drain and source sidewall lengths adjacent to the free substrate have been included. The following perimeter equations for both even and odd folding grades are based on the published calculations, i.e. sidewall lengths contacting the channel are excluded [Tsividis, 1988; de Graaff *et al.*, 1990].

For odd n the perimeter of drain P_{db} and source P_{sb} regions can be described as:

$$P_{sb,db} \approx \frac{W}{n} + 2 \cdot L_{edge} \frac{n+1}{2} \tag{4.8}$$

A graphical representation of equation (4.8) is shown in Figure 4.11. The top graph shows the perimeter as a function of folding grade with constant L_{edge} and W as parameter whereas for the bottom graph W is kept constant and L_{edge} is the parameter.

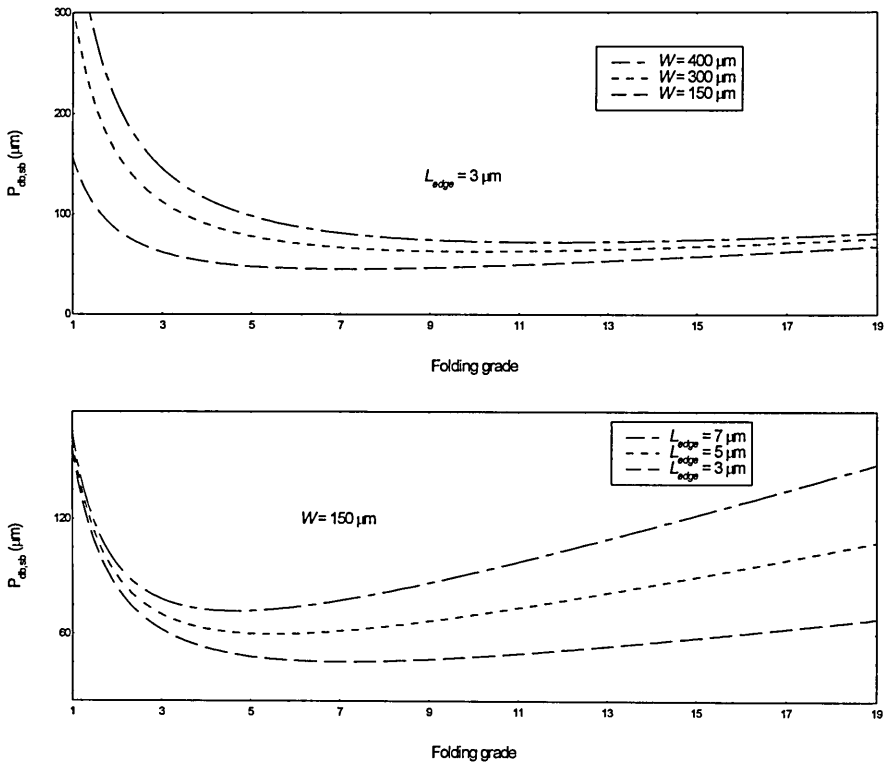

Figure 4.11: Perimeter of diffused regions for odd n

For even n the drain and source perimeter values differ. In this case the drain perimeter is only dependent upon L_{edge} and can be described by:

$$P_{db} \approx 2 \cdot L_{edge} \cdot \frac{n}{2} \tag{4.9}$$

This is also illustrated in Figure 4.12 with L_{edge} as parameter. The source region perimeter is dependent upon W and L_{edge} and its value is given by:

$$P_{sb} \approx 2 \cdot \frac{W}{n} + 2 \cdot L_{edge} \cdot \frac{n+2}{2} \tag{4.10}$$

Comparing equations (4.8) and (4.9), it can be deduced that the sidewall junction capacitance of the drain is much smaller than that of the source since it is not dependent upon the transistors width and $W >> L_{edge}$.

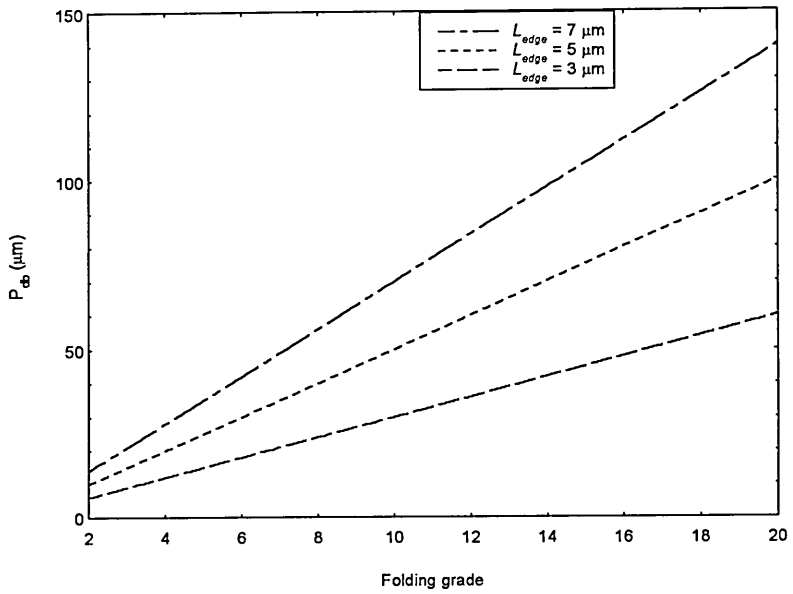

Figure 4.12: Drain perimeter for even n

Equation (4.10) is graphically illustrated in Figure 4.13. The top graph shows the source perimeter as a function of the folding grade with W as the parameter and for the bottom graph L_{edge} is the parameter.

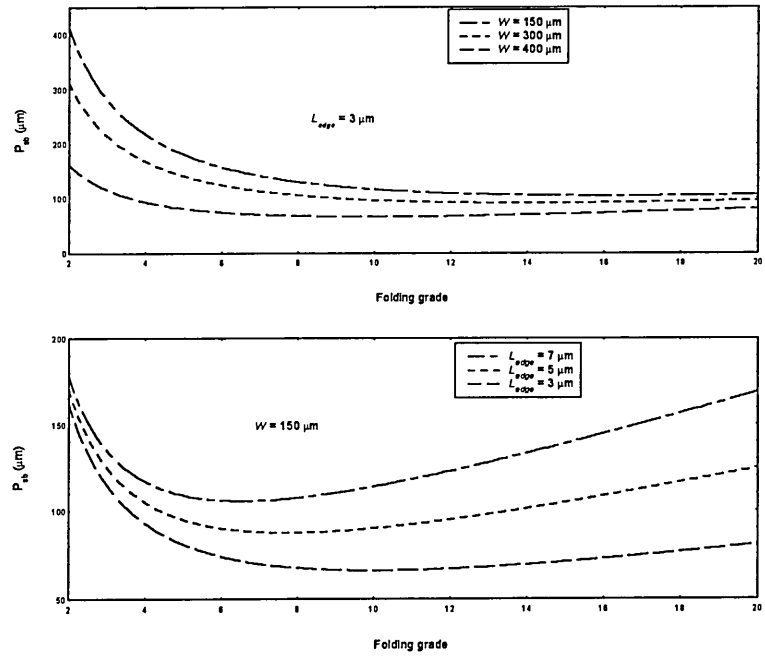

Figure 4.13: Source perimeter for even n

4.3.4.3 Areas of interconnections

Interconnections are used to connect common drains and sources (Figure 4.8b). Their areas may be defined as A_{dic} and A_{sic}, respectively. These areas, which overlap the free substrate, increase linearly with higher values of n and are given, for odd n, by:

$$A_{sic,dic} \approx \frac{n-1}{2} A_{in} \tag{4.11}$$

and for even n by:

$$A_{dic} \approx \left(\frac{n}{2} - 1\right) A_{in} \tag{4.12}$$

and

$$A_{sic} \approx \frac{n}{2} A_{in} \tag{4.13}$$

where A_{in} is the unit area of the interconnection between two drain or source areas of the folded transistor. Contact areas for metal layer to drain and source connections are determined from the equations (4.5)-(4.7) assuming that the metal area overlapping the active area is approximately the same as the drain and source areas.

4.3.4.4 Capacitance calculations from geometry equations

From the above described geometry calculations the reflected capacitances adjacent to drain and source regions, shown in Figure 4.7, can be calculated by multiplying the area and perimeter geometries presented in sections 4.3.4.1 to 4.3.4.3 with the value of the specific layer capacitance. The layer capacitance can differ substantially depending upon the technology used.

In the SPICE transistor model, the bottomwall junction capacitance is given as the model parameter CJ in units of Farads per unit area; the units for the sidewall junction capacitance (CJSW) are Farads per unit length. Both parameters are given for zero junction reverse bias voltage (V_{sb} and V_{db}). For a non-zero reverse bias voltage, new values for the junction capacitance C_J can be calculated using the following equation [de Graaff, 1990]:

$$C_J\left(V_{db,sb} \neq 0\right) = \frac{\mathrm{CJ}}{\left[1-\left(\frac{V_{db,sb}}{V_d}\right)\right]^p} \tag{4.14}$$

where V_d is the built-in junction potential (SPICE parameter PB) and p is a process dependent grading coefficient (described by SPICE parameters MJ and MJSW).

The drain and source junction capacitances of a folded transistor ($C_{db,sb}$), are the sum of the bottomwall and the sidewall capacitances and can be written as:

$$C_{db,sb} = C_{dbj,sbj} + C_{dbsw,sbsw} = A_{db,sb} \cdot \mathrm{CJ} + P_{db,sb} \cdot \mathrm{CJSW} \tag{4.15}$$

The second important capacitances that are connected to the drain and source areas are caused by metal interconnections and these are given by:

$$C_{in_{db,sb}} = \left(A_{db,sb} + A_{dic,sic}\right) \cdot C_{ic} \tag{4.16}$$

where C_{ic} is the metal layer capacitance per unit area and its value is also given by the foundry.

4.3.4.5 Specific calculations for the MIETEC 2.4 μm CMOS process

The following results presented are based on equations (4.6) to (4.16) and technology parameters provided by EUROCHIP for the Alcatel MIETEC 2.4μm CMOS technology (Appendix A). The following capacitance values of junction area, junction sidewall and metal interconnections were used [Das, C., 1994]:

$$CJ = 312\ \mu F/m^2$$

$$CJSW = 376\ pF/m$$

$$C_{ic} = 20\ \mu F/m^2$$

The calculated junction and interconnection capacitances over a wide range of folding grades for a NMOST with a *W/L* ratio of 150/3 for odd and even *n* are shown in Figure 4.14 and Figure 4.15, respectively. As can be seen, for odd folding grades the area capacitance decreases exponentially from the peak of 468 fF to around 245 fF whereas for even folding grades it stays constant at 234 fF over the entire range. The periphery and interconnection capacitances for odd *n* have their minimum at $n = 3$ and then increase approximately linearly with *n*. However, for even *n* the capacitances show no minimum and increase linearly with *n*.

In Figure 4.16 the sum of the junction capacitances of Figure 4.14 and Figure 4.15 is illustrated. For this specific *W/L* ratio of 150/3 the minimum drain connected capacitances can be found at a folding grade of two. The unfolded transistor has the highest drain connected capacitances and is approximately twice the possible minimum value. Even for higher values of the *W/L* ratio the minimum drain capacitance always occurs at a folding grade of two.

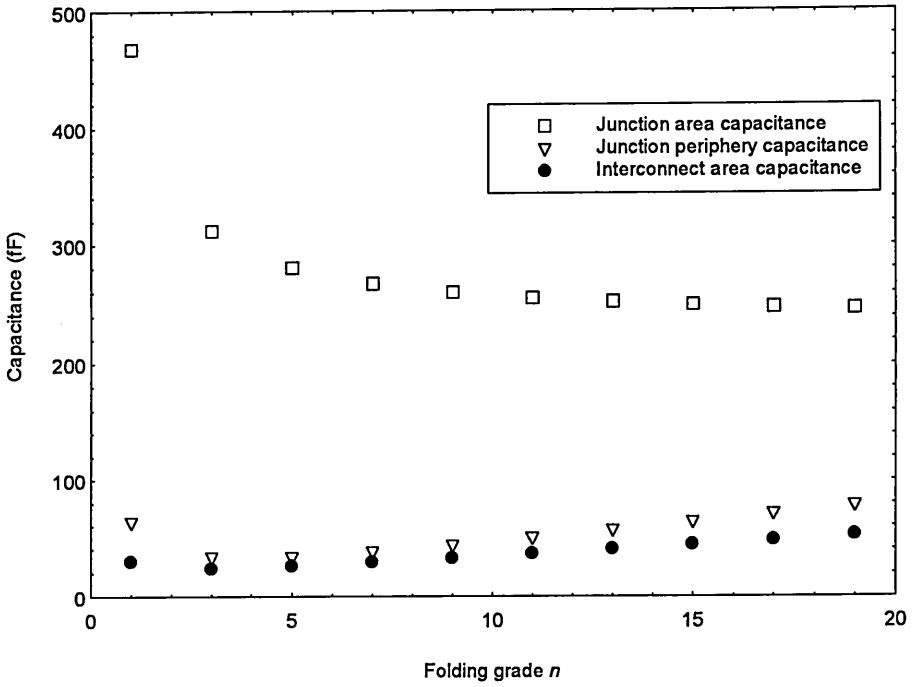

Figure 4.14: Drain capacitances for odd *n*

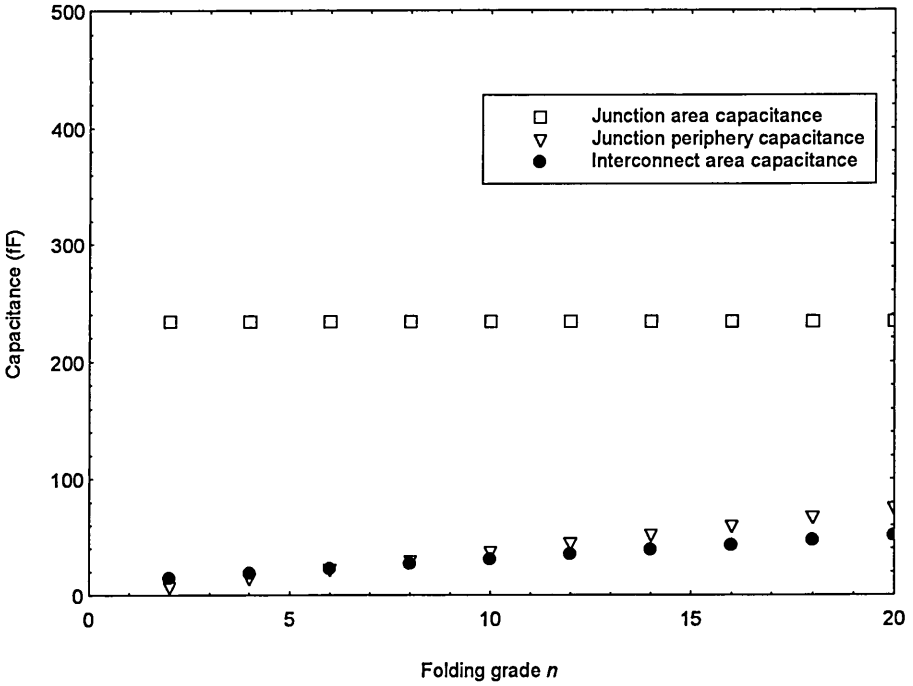

Figure 4.15: Drain capacitances for even *n*

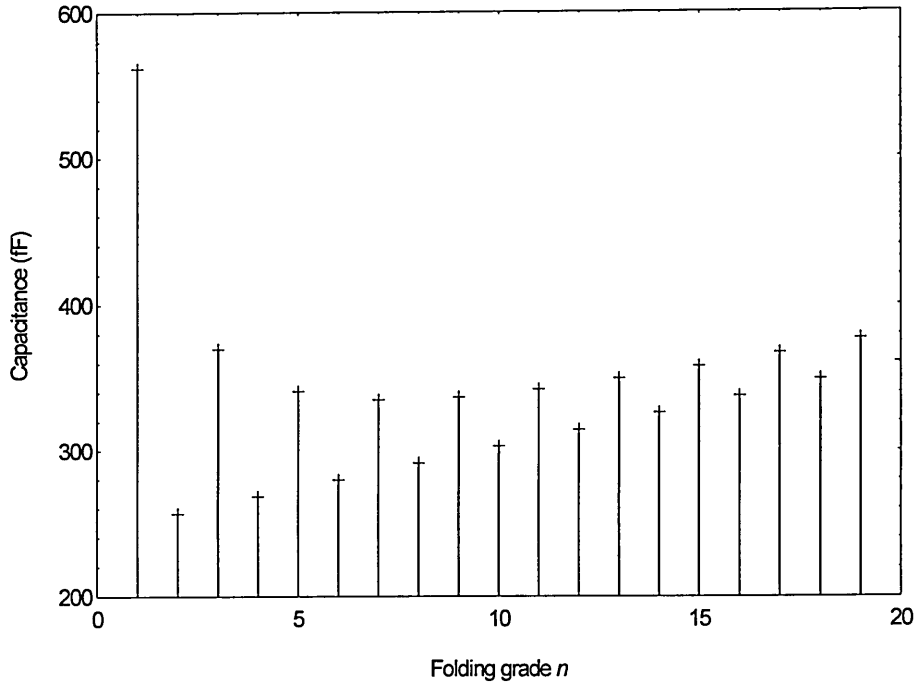

Figure 4.16: Total drain junction capacitances

4.3.5 Concluding remarks on layout optimisation of MOSFETs

For an NMOST with a *W/L* ratio of 150/3 and using the Alcatel MIETEC 2.4 μm CMOS technology, the major capacitances are the area capacitances of the diffused regions. The periphery and interconnection capacitances can be seen as minor contributors. In this case their value is ~10% of the area capacitances. They might, therefore, be neglected for transistors with a large width to length ratio.

Using a different technology with different parameters (e.g. larger conducting layer capacitances and/or smaller junction capacitance values) may cause the interconnecting capacitances to become predominant in relation to the junction capacitances. It is

important to note that the transistor layout optimisation is dependent upon the technology used. However, in general, lower drain junction capacitances can be achieved by using even folding grades because there are no junction sidewalls adjacent to the free substrate. The lowest possible parasitic junction capacitance is realised by implementing a folding grade of two. The designer has to trade-off lowest drain capacitance with a design shape appropriate for chip layout.

An analysis was carried out to determine the difference between the calculations used in this chapter and those applied in HSPICE (method ACM = 2). This was found to be between 15% and 20% of the total drain capacitance Cd_{tot}. In general, HSPICE simulations will predict larger values. Consequently, the simulation with ACM = 2 of the transistor switching performance will be somewhat slower compared with the real device.

4.4 Matching of Components in IC Layout

Matching of elements is very important in IC layout. Mismatch of components is always caused by parameter variations. These variations can be caused by device size, orientation, proximity and spacing [Carley, 1994]. For instance, many fundamental device parameters, such as oxide thickness or doping density have a low spatial variation. Thus by placing components far apart, matching will degrade. Another source of mismatch arises from other mask geometries in the vicinity of an edge. For example, in a folded transistor the length of the two outer transistors will be slightly smaller than the length of the inner transistors due to greater underetching. The normal

solution to such a problem is to place a dummy transistor at either ends of the folded transistor.

Sometimes, very accurate capacitor matching is required. This can be achieved, by splitting the capacitor into several smaller ones and connecting them in parallel. The smaller capacitors are distributed evenly over the die area ensuring that parameter variations will effect both capacitors equally. A similar principle can be applied if a N:1 ratio of capacitors is required. The most accurate matching can be achieved by laying out N+1 capacitors and wiring N of them in parallel [Carley, 1994].

In analogue design, a common problem is the matching of two transistors in a differential input stage. To ensure good matching, the transistors should be placed close together but this is difficult to achieve for wide transistors. One possible solution is to use an interdigitized arrangement. Here, the transistors are split into a parallel combination of several smaller transistors. These transistors are then placed in such a way, that both transistors are interdigitized as shown in Figure 4.17. Both transistors are thus spread out evenly over the area. Included in this layout are two dummy transistors to the right and left of the structure to ensure that the rightmost and leftmost transistors of the interdigitized differential pair do not suffer from underetching. The gates of the dummy transistors are connected to the VSS rail effectively making the channel highly resistive so that they do not influence the differential pair.

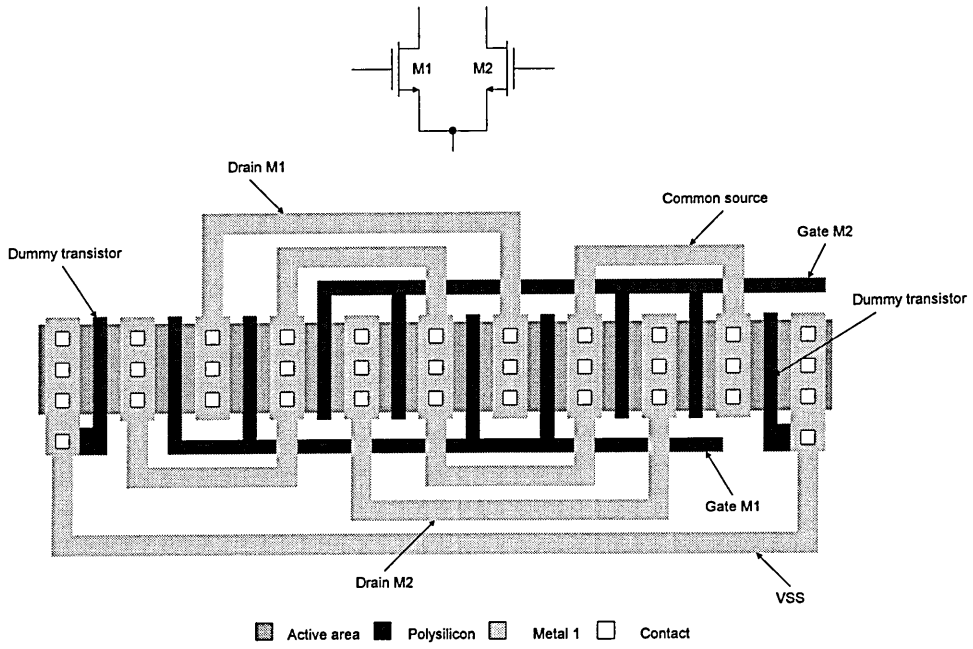

Figure 4.17: Interdigitized layout of a differential pair

4.5 Extraction of Parasitic Elements

4.5.1 Parasitic extraction using MG IC Extract

IC Extract is included in MG's IC Station and can be used to extract a HSPICE netlist from the mask-level layout designed in IC Station. This netlist may include parasitic elements. Two possible forms of parasitic extraction can be used, lumped and distributed parasitics. Lumped parasitics consist of only the net lumped capacitances which include all the net-to-ground (intrinsic) and net-to-net (coupling) capacitances. Distributed parasitics consist of distributed RC tree information. Each interconnect net is expanded and inserted with a RC network subcircuit. A data reduction option may be used to reduce the RC networks [Mentor Graphics, 1994].

4.5.2 Software problems within MG's IC Extract

The distributed method is the preferred choice for accurate simulations of parasitics. This method allows a better simulation of conducting layers because each layer can be represented much better by a RC network compared to only a lumped capacitance at each node. Unfortunately, due to a software problem within IC Extract, this method could not be employed. This became apparent during simulations carried out to evaluate the performance of different layout designs of single MOSFETs. After consultations with experts at IMEC, Belgium, a general problem associated with parallel resistive interconnect and performing extraction has been identified which makes the distributed parasitic extraction tool of IC Station unusable.

4.5.3 Parasitic extraction with SPACE

The SPACE program, developed by the University of Delft, The Netherlands, is an advanced layout to circuit extractor for analogue and digital integrated circuits. From a given mask-level layout, a circuit netlist of interconnected MOS transistors, bipolar and mixed BiCMOS devices is produced. Depending upon the desired level of detail, this netlist can also contain interconnect capacitances to substrate, interconnect coupling capacitances (both cross-over and lateral) and interconnect resistances. The extracted netlist can be simulated using HSPICE to verify the detailed behaviour of the implemented circuit [http5, 1996].

Space can easily be integrated into the IC design flow of Mentor Graphics as shown in Figure 4.18.

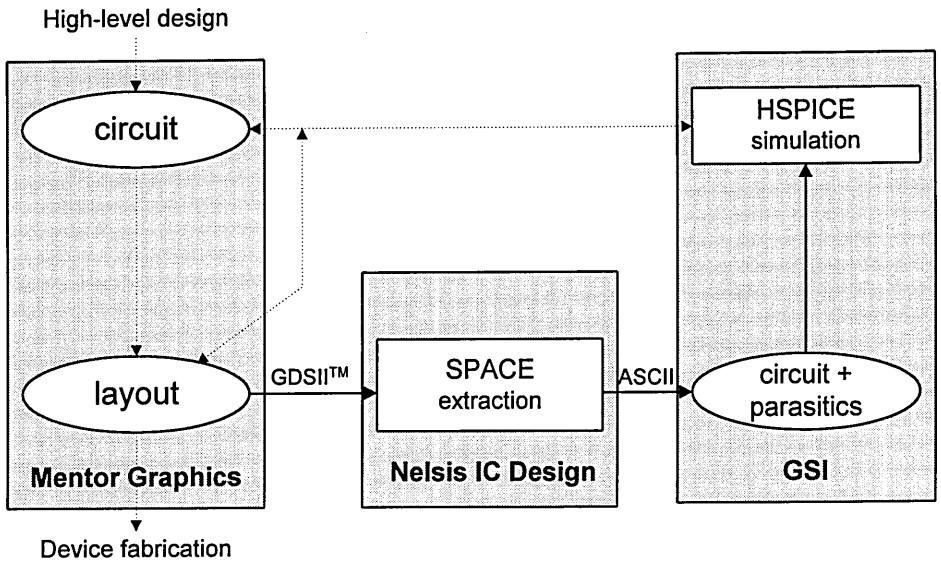

Figure 4.18: IC design flow using SPACE

The accuracy of the SPACE extraction and subsequent simulation depends on the accuracy and amount of available technology information since all the technology files have to be written by the designer. The information available for the MIETEC 2.4 μm CMOS process was insufficient to allow a justifiable comparison with lumped extraction of IC Station. However, an evaluation carried out by Raabe [1996] using the available technology information showed that all simulation results obtained laid within a region which was defined as follows:

Upper limit: Extraction carried out with IC Station and the netlist contains no parasitics.

Lower limit: Extraction carried out with IC Station and netlist contains lumped parasitics.

It is very difficult to make a quantitative judgement on the results since it was impossible to acquire more information on how MG's technology files were compiled. With more technology information available, SPACE should be the preferred choice for

parasitic extraction since it gives the designer many more options on how detailed the extraction should be.

4.6 Summary

Important considerations when laying out integrated circuits have been presented in this chapter. The physical structure of MOSFETs and the n-well CMOS technology have been discussed. The MOSFET is a symmetrical device and the conductivity of the channel can be controlled by a voltage applied to the gate terminal. Different types of MOSFETs can be classified depending upon their doping profile. The MIETEC 2.4 μm technology is based on a lightly p-doped substrate with the p-MOST implemented in a n-well.

IC layout is concerned with designing the masks needed for IC fabrication. All electronic components and their interconnecting wires are assembled two-dimensionally on an IC. Therefore, the IC layout has to assign an area on the surface of the wafer for each component and its interconnections. Components are assembled by placing different layers, indicating deposition or removal of material, onto the surface of a silicon wafer.

Several possibilities exist for MOSFET layouts and different layout techniques will effect the performance of the devices. Especially in analogue electronics, transistors with a large width to length ratio are sometimes required. This results in a difficult to implement aspect ratio of the transistor layout. Normally, these large transistors are

folded to achieve a more manageable aspect ratio. Folding of a MOSFET will have an effect upon its performance. The parameters affected by folding a transistor have been investigated and a theory presented which enables the designer to trade-off aspect ratio against performance based on junction and interconnect capacitance calculations. It was shown that folding increases the performance of a transistor significantly.

Every IC has also passive parasitic elements in form of capacitances and resistors. These will always degrade the performance of the circuit and must therefore be taken into account. Several software tools exist which enable the designer to extract these parasitics and simulate the behaviour of the circuit including the parasitics. It was discovered that part of IC Extract, the netlist extraction tool of MG's IC Station was not working properly. After further investigations, it was found that a software routine calculating the parallel resistivity was faulty. To overcome this problem, a different extraction program, SPACE, was implemented into the IC design flow but due to inefficient technology information a performance comparison with IC Extract was difficult to carry out. However, simulations of extracted netlists showed that with more information from the foundry, an accurate netlist can be extracted using SPACE allowing for better evaluation of the influence of parasitics upon the circuit performance.

CHAPTER 5

CIRCUIT DESIGN AND DESCRIPTION

5 CIRCUIT DESIGN AND DESCRIPTION

5.1 Overall Circuit Description

A pulse frequency modulator consists of a voltage controlled oscillator followed by a pulse shaping circuit, see Figure 5.1. The VCO can generate either sinusoidal or square wave output voltages. A sinusoidal waveform may be converted into a square wave by detecting the zero-crossings which can be implemented by employing a threshold detector. The pulse shaping circuitry generates a fixed width pulse of constant amplitude at the leading, trailing or both edges.

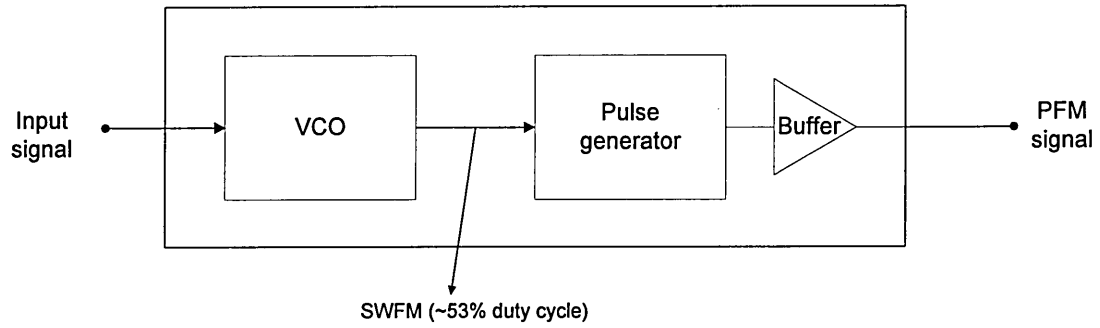

Figure 5.1: Overall circuit diagram of PFM modulator

A VCO is an oscillator circuit where the frequency of oscillation is controlled by an externally applied voltage. VCOs may be used in clock or timing recovery circuits or as modulators/demodulators in FM or PFM schemes. Depending upon the application, different performance criteria are important. For clock recovery circuits, low oscillation jitter is important whereas in modulation circuits a linear transfer characteristic is of prime importance, since non-linearity would cause harmonic and intermodulation distortion.

For a PFM modulator, the required frequency of the VCO depends on the highest frequency component of the input signal. It has been shown in Chapter 2 that spectral overlap can cause non-linear distortion of the baseband component. The sampling ratio, hence the frequency of oscillation has to be chosen in such a way that this distortion is keep below a predefined threshold level.

5.2 Voltage Controlled Oscillator Design

5.2.1 Types of VCOs

The voltage controlled oscillator is a fundamental building block for many communication systems. Oscillators are designed to give either a sinusoidal or a square wave output. Since the PFM signal is best generated by differentiating a square wave, therefore, only oscillators with a square wave output are considered here.

Various circuit implementations of square wave VCOs exist. One scheme employs an odd-numbered ring of inverting gain stages connected back to itself where the oscillating frequency is basically determined by the gate delay. To implement a VCO, this delay needs to be voltage controllable. Several methods have been reported such as inserting a MOSFET in series with every inverter stage as shown in Figure 5.2 [Enam *et al.*, 1990]. The transistor acts like a voltage controllable resistance and is used to vary the time delay of the *RC* network, where *R* is the MOSFET resistance and *C* the inverter input capacitance.

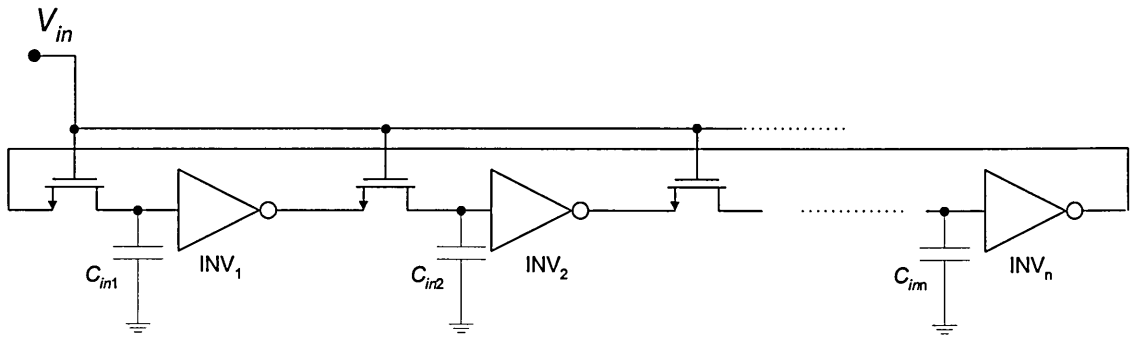

Figure 5.2: Ring based VCO with voltage controllable delay

Unfortunately, the additional delay introduced by the transistor reduces the highest achievable operating frequency since each MOSFET is basically doubling the delay per stage. On the other hand, reducing the number of inverting gain stages is impractical since it would lower the loop gain and may prevent oscillation altogether.

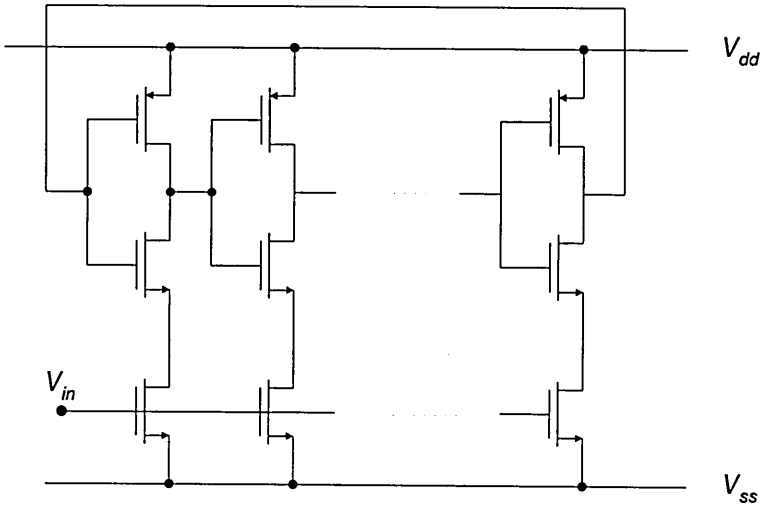

Figure 5.3: Ring based VCO with voltage controlled current biasing

Another scheme employs voltage controllable bias currents in each inverter of the chain resulting in voltage controlled rise and fall times, Figure 5.3 [Goto *et al.*, 1994]. Here, the additional transistor causes capacitive loading of the inverter limiting the operation at extremely high frequencies. Another circuit reported by Enam and Abidi [1990]

consists of a cascade of odd and even numbers of inverters, the outputs of which are mixed to constitute the feedback signal for the ring oscillator (Figure 5.4).

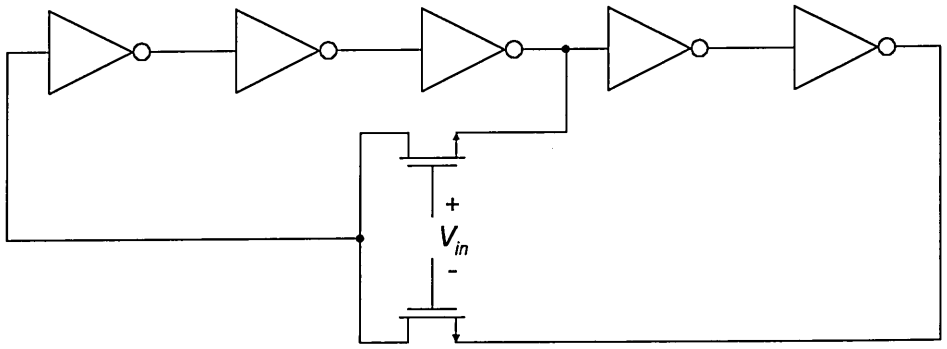

Figure 5.4: Ring based VCO with voltage controllable mixing in feedback path

The advantage of all these schemes is the wide tuning range and high oscillation frequency. Unfortunately, ring based VCOs tend to have a non-linear transfer characteristic (Figure 5.5) although some work has been reported on improving the linearity [McNeill, 1994]. This is caused by the use of MOSFETs as control devices which exhibit a non-linear characteristic. Ring oscillators are therefore more suited to clock recovery circuits where linearity may not be as important as a wide tuning range.

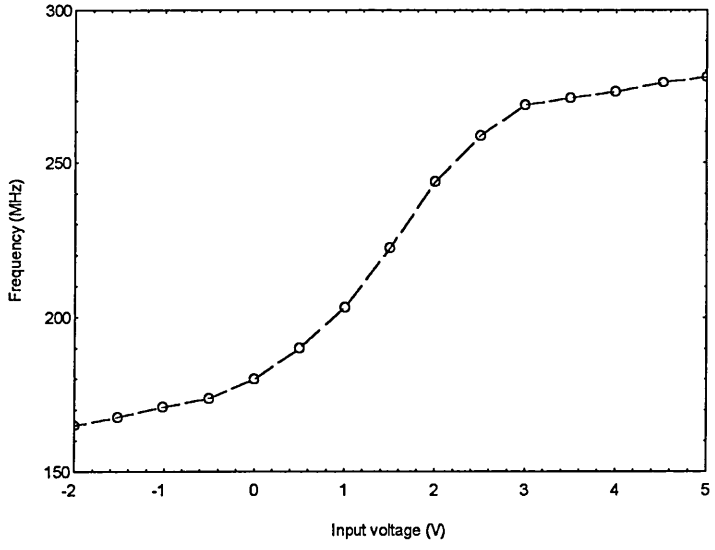

Figure 5.5: Transfer characteristic of ring VCO [Enam *et al.*, 1990]

There is also a VCO design, known as relaxation oscillator, which is based on charging and discharging of a capacitance to generate the oscillation. Here, a capacitor is alternately charged and discharged by a constant current thus generating a sawtooth waveform. This is then compared with a reference voltage level in order to provide the required square wave (Figure 5.6).

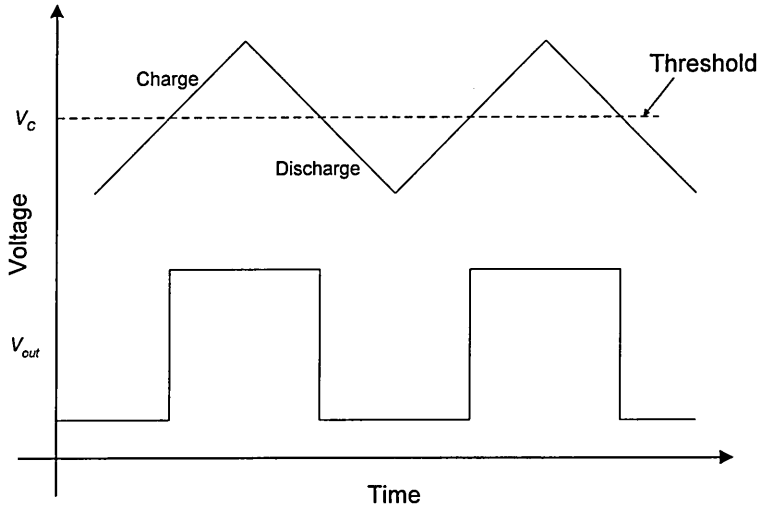

Figure 5.6: Principle of relaxation oscillator

Two major types of relaxation oscillators have been implemented. They employ either floating or grounded timing capacitors [Kukielka *et al.*, 1981]. The floating capacitor VCO is commonly implemented as an emitter-coupled multivibrator as shown in Figure 5.7.

*R*1, *R*2, Q3, Q4 and *C* form the emitter-coupled multivibrator which is fed by a voltage controlled emitter-coupled pair. A general waveform diagram for this type of VCO is shown in Figure 5.8. Assuming Q1 and Q4 are switched off and Q2 and Q3 are switched on, the capacitor is charged linearly with a constant current (*I*) through Q3. If the voltage across this capacitor is reaching V_{dd}, then Q2 and Q3 are switched off and

Q1 and Q4 are switched on and C is charged with alternating polarity. The output waveform will then be a square wave [Spencer *et al.*, 1990]. This type of VCO can also be implemented with CMOS devices [Razavi, 1996].

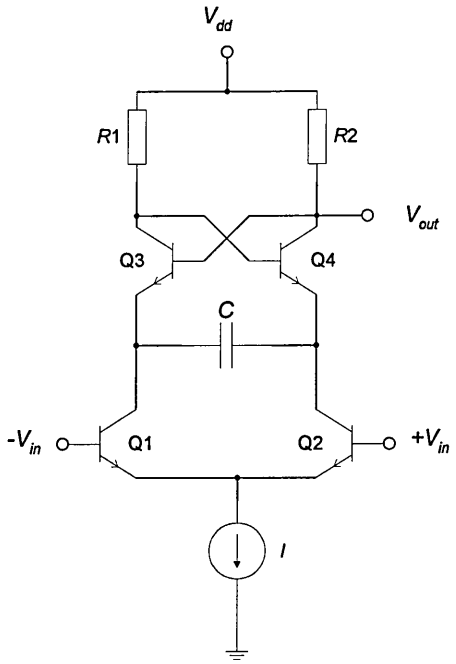

Figure 5.7: Emitter coupled multivibrator

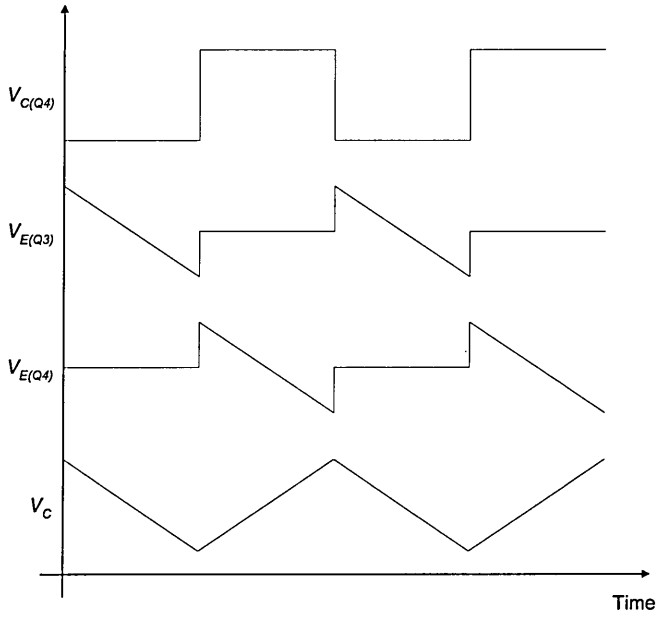

Figure 5.8: Waveform diagram of emitter coupled multivibrator

The parasitic capacitances associated with the emitter of Q3 and Q4 will influence the frequency characteristic of the circuit. At high frequencies they introduce voltage division and thus limit the performance [Kukielka *et al.*, 1981].

Employing a grounded capacitor based relaxation oscillator avoids some of the problems associated to parasitic capacitances. Here, the parasitic capacitance appears only in parallel to the timing capacitance, thus increasing its value.

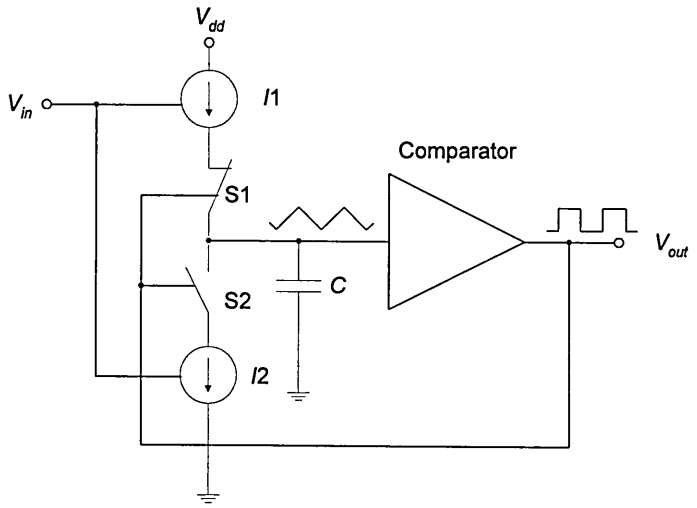

Figure 5.9: Circuit diagram of grounded capacitor based oscillator

Figure 5.9 shows the principle circuit diagram of such an oscillator and its operation is readily explained. With the switches positioned as shown, C is charged with a constant current, thus the voltage across C is rising linearly. The comparator has to drive the two switches S1 and S2. Therefore, the comparator must exhibit two threshold voltages, an upper (V_H) and a lower threshold (V_L) voltage. The output is switched from low to high when the comparator's upper threshold voltage is reached. This output change opens S1 and closes S2 resulting in a controlled discharging of C. When the lower threshold

voltage is reached, the output is now changed from high to low and the cycle starts again (Figure 5.10).

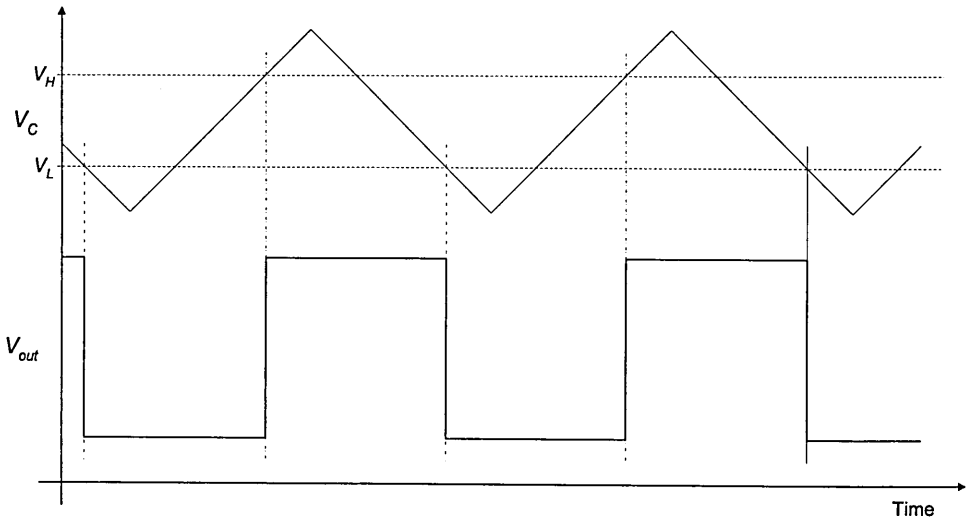

Figure 5.10: Waveforms for grounded capacitor based VCO

This oscillator, based on a grounded capacitor, is well suited for implementation in CMOS technology due to the availability of almost perfect switching devices in the form of MOSFETs. Kukielka and Meyer [1981] have suggested that this type of relaxation oscillator is superior to floating capacitor schemes for high frequency and temperature stable designs. This design has been proven to be appropriate by Banu [1988] and Flynn *et al.* [1992] and was therefore investigated further.

5.2.2 Grounded capacitor based VCO design

The oscillator consists of two distinctive blocks, the capacitor charging/discharging block, which will be described first and the comparator/feedback block.

5.2.2.1 Single capacitor oscillator

Figure 5.9 shows the principle circuit diagram of a VCO based on a single grounded capacitor. A Schmitt trigger circuit may be employed as comparator due to the availability of two threshold voltages [Soclof, 1991]. If V_H is upper and V_L the lower switching point of the Schmitt trigger hysteresis then the frequency of operation f_o can then be expressed as:

$$f_o = \frac{I}{2(V_H - V_L)C} \tag{5.1}$$

with I being the voltage controlled current ($I_1 = I_2$ in Figure 5.9). If the current I is a linear function of the input voltage then the frequency of oscillation is linearly dependent upon the input voltage.

Disadvantages of a single capacitor based design

This design suffers from several disadvantages. Wakayama and Abidi [1987] showed that random variations in the oscillator period (jitter) can be minimised by maximising the voltage across the timing capacitor. This could be achieved by increasing the supply voltages which is not desirable and in modern semiconductor processes may be impractical. The design requires the capacitor to be charged between two threshold voltages, each of which must be separated from the supply rail by at least one volt (one MOSFET threshold voltage), thus limiting the available capacitor voltage amplitude. A further problem arises from the fact that one current source is n-type while the other is a p-type source making it almost impossible to match them over a wide dynamic range.

The practical circuit will also suffer from delay times due to switching and comparison of capacitor (V_c) and reference (V_H) voltage. During that delay time, the capacitor will continue to charge resulting in overshoot (V_{o1}), Figure 5.11. Assuming charging and discharging currents to be equal, this overshoot will increase the discharging time by the same amount as the charging time resulting in an increased oscillation period of twice the delay time (t_d). At higher frequencies (f_1) the gradient of the capacitor voltage ramp, $V_c(f_{1,2})$, will be greater resulting in a greater overshoot (V_{o2}) for any given delay time. The increased overshoot may speed up the comparison due to an increased comparator overdrive [Flynn *et al.*, 1992]. This makes the delay time dependent upon the oscillating frequency, thus introducing some non-linearity in the operation.

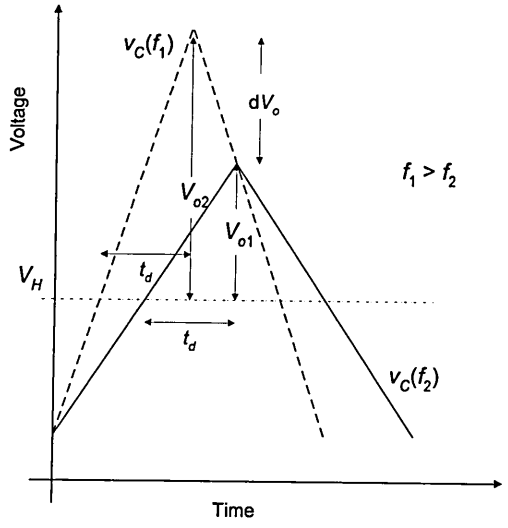

Figure 5.11: Effect of overshoot on capacitor voltage ramp

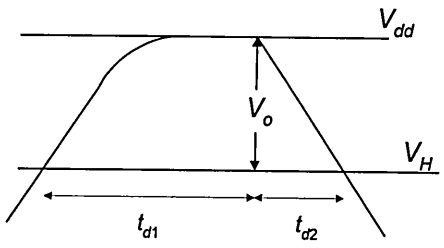

Figure 5.12: Effect of overshoot reaching supply rail

If the capacitor voltage ramp is maximised to decrease jitter, both threshold voltages will need to be placed close to the supply rails thus reducing the maximum possible overshoot. Under these conditions and at higher frequencies the overshoot will reach the supply rails causing saturation and resulting in different charge (t_{d1}) and discharge (t_{d2}) times (Figure 5.12). This will introduce further non-linearity.

5.2.2.2 Double capacitor oscillator

Most of the problems discussed above can be overcome by employing two grounded capacitors as shown in Figure 5.13 [Banu, 1988].

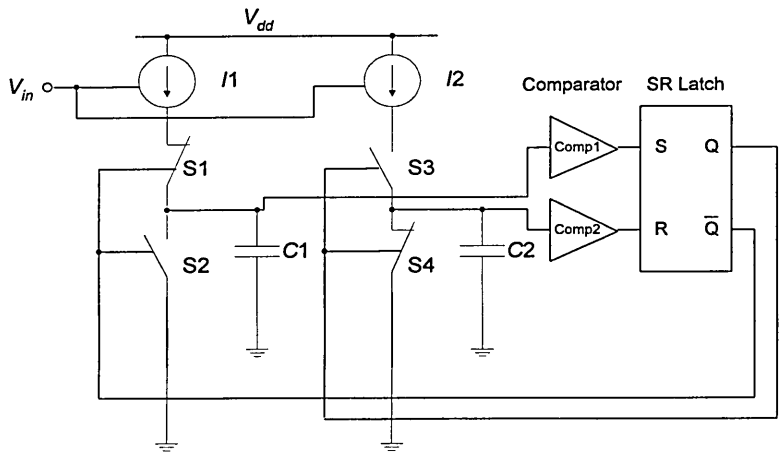

Figure 5.13: VCO design based on two grounded capacitors

Assuming S1-S4 positioned as shown in the diagram. $C1$ is charged until it reaches the threshold V_{T1} of Comp1. Upon reaching the threshold, the outputs of the SR latch changes and S1, S4 open and S2, S3 close. If the switches are designed in such a way that the discharging is carried out much faster than the charging, $C1$ is being discharged long before the voltage across $C2$ reaches Comp2's threshold voltage V_{T2}. The period of oscillation is now only dependent upon the charging time of the capacitor, Figure 5.14.

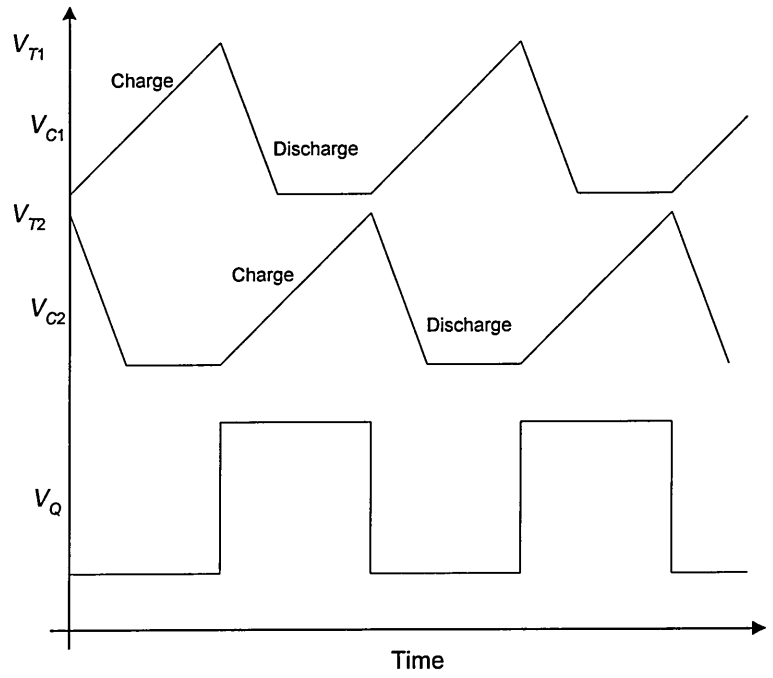

Figure 5.14: Principle of VCO based on two grounded capacitors

Advantages

This design offers several advantages compared to the single grounded capacitor design. Only one threshold voltage is necessary enabling an increased capacitor voltage ramp thus resulting in reduced oscillator jitter. Only one current source, (p-type in Figure 5.13) is employed, making the design easier. Switching occurs always at the same threshold voltage making it easier to achieve a 50% duty cycle if desired. Parasitic capacitances effect both timing capacitors equally and allowing for a symmetrical design which does not influence the duty cycle. The effect of overshoot upon oscillation period is greatly reduced since only the charging time determines this value. The VCO can be designed in such a way that the charging cycle always begins at the same predetermined voltage level.

Although many of the problems encountered with the single capacitor based design have been solved by employing two grounded capacitors, this design introduces a new problem. The oscillator period is determined by two symmetrical circuits. A good matching of these circuits must be achieved in order to compensate for circuit parameter variations. This is solved by inventive layout structures for timing capacitors, switches and comparison circuitry.

5.2.2.3 Switching and comparison

The speed of comparison will have a great impact on the highest possible oscillation frequency as well as the duty cycle. The speed can be improved by minimising the number of switching delays, thus minimising the number of transistors. The switches will therefore be implemented as single transistors. For the comparison and feedback block, Banu [1988] showed that the simplest circuit consists of a SR latch designed using NAND or NOR gates. However, there is a possibility of positive DC feedback with such a configuration, resulting in an unwanted stable state and thus preventing oscillation. This could happen, for example, if both inputs of the SR latch are driven into a high state since this is defined as the 'hold' operation, i.e. the output is not changing. The solution is to add a further SR latch in series [Banu, 1988].

5.2.2.4 Final VCO circuit diagram

Figure 5.15 shows the VCO design which has been evolved. If the width to length ratio of the NMOS transistors M2 and M4 is equal to that of M1 and M3, the current drive

capability of M2 and M4 will be about three times higher than that of M1 and M3 fulfilling the requirement of a much faster discharging than charging time. This is due to the inherent higher transconductance of the n-type MOST.

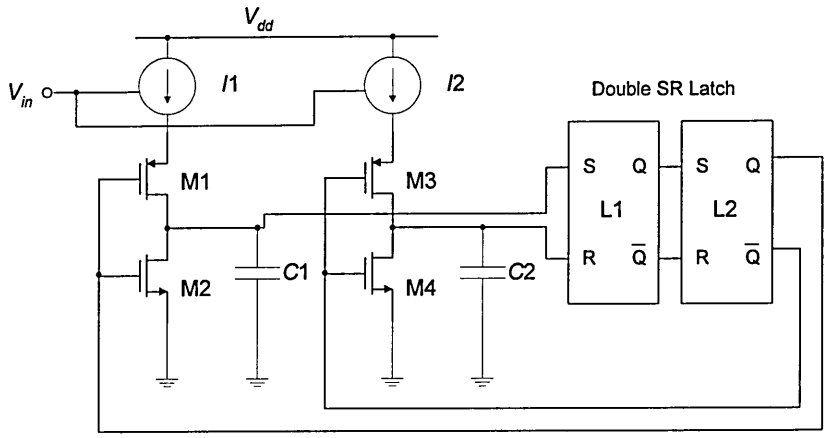

Figure 5.15: Adopted VCO design

*I*1 and *I*2 are voltage controlled current sources and L1 and L2 form a double SR latch implemented with NAND gates.

5.2.3 Voltage controlled current sources

Voltage controlled current sources are analogue circuits which convert an input voltage into a current. It is essential that they have a linear transfer characteristic over the required bandwidth. A basic voltage to current converter may be implemented by using a single MOSFET. If operated in the saturation region, the drain current I_D can be expressed as a function of the gate-source voltage v_{gs} as follows:

$$I_D = \frac{k'}{2}\frac{W}{L}\left(v_{gs} - V_T\right)^2 \qquad \textbf{(5.2)}$$

where k' is the transconductance parameter, W and L are the width and length of the channel, respectively and V_T is the threshold voltage. Equation (5.2) clearly shows that I_D is proportional to the square of v_{gs}. Therefore, a single MOSFET is unsuitable as a voltage to current converter since a linear transfer characteristic cannot be achieved.

Attempts have been made to develop circuits which behave like MOSFETs but have a linear characteristic [Bult *et al.*, 1991]. These circuits, so called 'super-transistor' were based on cascading stages, as shown in Figure 5.16, to enhance the DC gain of amplifiers [Hosticka, 1979; Säckinger *et al.*, 1990]. Due to the dynamic biasing of the cascaded stage, these circuits were not effected by channel length modulation and enhanced the performance of amplifiers when used as active devices in current mirrors. The disadvantage of the 'super-transistor' is that they need twice the threshold voltage of a simple transistor due to cascading. This might not be a problem with a 5 V power supply but reducing it to 3.3 V or less as in modern processes makes this circuit difficult to implement.

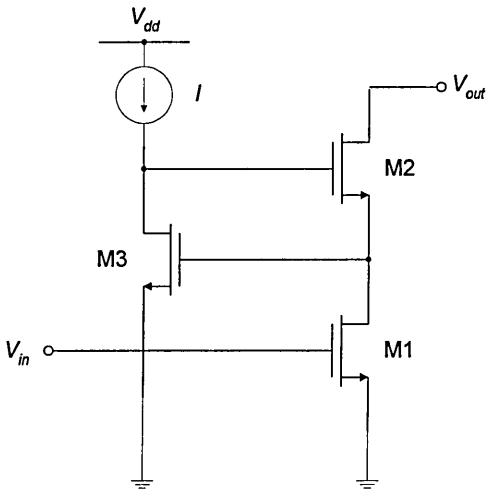

Figure 5.16: Cascaded gain stage with dynamic biasing

A voltage to current converter could be based on a floating resistance controlling the voltage to current transfer [Wilson *et al.*, 1993]. Kumuwachara *et al.* [1994] reported a differential voltage to current converter. Although, the transconductance of this circuit was linear and accurate over a wide dynamic range, the frequency response was not sufficient for the requirements of a PFM modulator. Furthermore, a single ended input and output is needed for the proposed VCO design.

Another interesting design is based upon a current conveyor circuit (Figure 5.17). A current conveyor circuit is a universal analogue building block in current mode designs. It can be seen as an alternative to the conventional operational amplifier. The second generation of current conveyors (CCII) was proposed by Sedra and Smith [1970] and has proven to be a very useful device in analogue signal processing.

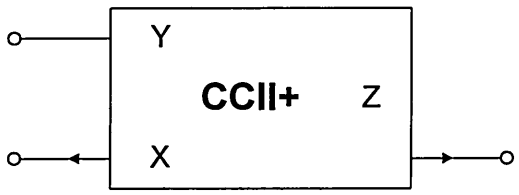

Figure 5.17: Current conveyor symbol

The operation of current conveyor can be described by [Toumazou *et al.*, 1990]:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad \textbf{(5.3)}$$

From this equation, it can be concluded that a CCII works like a voltage follower between Y-input and X-output ($V_X = V_Y$) and as a current follower between X-input and Z-output ($I_z = I_x$). The current conveyor is a very versatile building block and one

possible application is a voltage to current converter, as shown in Figure 5.18 [Toumazou *et al.*, 1990].

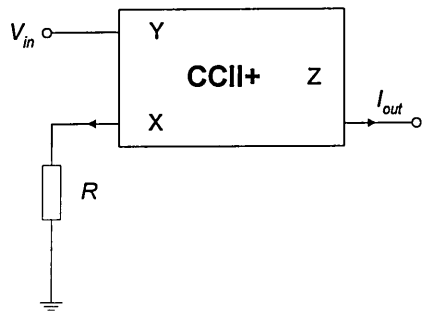

Figure 5.18: Voltage to current converter configuration

Applying equation (5.3) the transfer characteristic of this circuit can be expressed as follows:

$$I_{out} = \frac{V_{in}}{R} \tag{5.4}$$

A linear relationship between input voltage and output current can be observed. Furthermore, the output current offset can be determined for any given input voltage offset by R. How linear the characteristic of the voltage to current converter will be depends only on the characteristic of the current conveyor.

Current conveyor design

Although, many designs based on current conveyors have been reported only very few CMOS implementations were proposed over the last few years [Wilson, 1990]. Earlier designs relied on operational amplifiers with MOSFETs in the feedback path [Sedra *et al.*, 1990]. This had the disadvantage of rather complex designs and large supply voltage requirements [Cheng *et al.*, 1993].

A current conveyor configured as a voltage to current converter for use in a VCO design must maintain accurate voltage following between 'Y' and 'X' terminals while having a linear current transfer characteristic. A simple design fulfilling these requirements has been proposed by Palmisano and Palumbo [1995]. Figure 5.19 shows the circuit diagram of the current conveyor. Transistors M1 to M5 perform a unity gain amplification from node 'Y' to node 'X'. M6 and M7 form a common source amplifier; M5 and M7 are current sources with current biasing accomplished by M8, M9 and I_B.

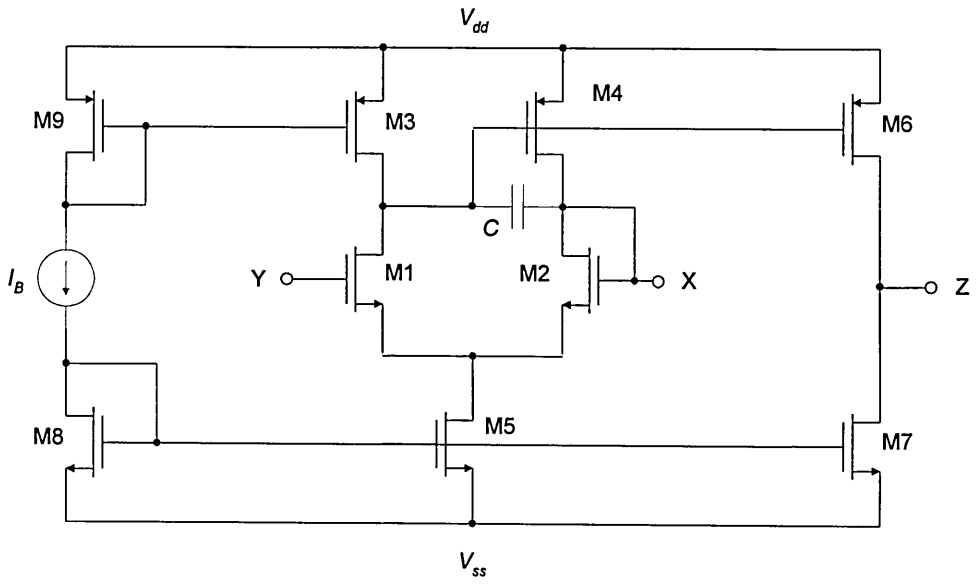

Figure 5.19: Current conveyor circuit diagram

Above the threshold voltage of M1, the circuit operation can be explained as follows:- The drain current of M9 will be mirrored into M3. M1 acts as a source follower, thus source voltage of M1 will be equal to its gate voltage reduced by the threshold voltage. M2 acts as a level shifter adding one threshold voltage from source to drain. Setting the drain current of M5 to twice the value of the drain current of M3 will make the gate-source voltages of M1 and M2 equal and fixed at their quiescent value. Due to the above described operation the voltage at the 'X' terminal will follow the voltage at the

'Y' terminal. Since the drain currents of M1-M3 are fixed at their quiescent values, the input current at the 'X' terminal is supplied by M4. This current is mirrored into M6 and therefore the current at terminal 'Z' is equal to current at terminal 'X'. Only basic current mirrors are used. Cascaded current mirrors would improve the current transfer characteristic but at the expense of reduced voltage swing at terminal 'Z', the output terminal.

Palmisano and Palumbo [1995] reported simulation results which confirm the expected operation of the circuit. The cut-off frequency of the voltage response is greater than 20 MHz and for the current response is 40 MHz. For signal amplitudes up to 1 V a total harmonic distortion of more than 55 dB was also reported by them. The described achievable performance is sufficient for our requirements as detailed in chapter 2. This design will therefore be adopted.

5.3 VCO Linearization Scheme

It has been shown in the previous section that the VCO voltage to frequency transfer characteristic may be non-linear causing harmonic and intermodulation distortions. This non-linearity may be minimised by inventive circuit techniques. Sometimes, this is not possible and therefore, a non-linear compensation network may be employed as shown in Figure 5.20. The network introduces a non-linearity of the same order but opposing that of the VCO. The effect is that the VCO non-linearity is cancelled out and the result is a linearity improvement and wider modulating range.

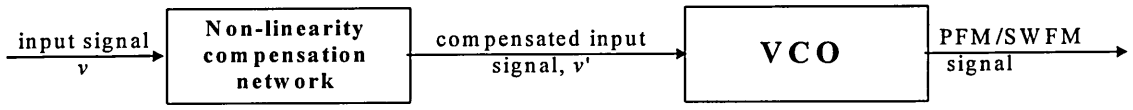

Figure 5.20: Proposed linearization scheme

The VCO transfer function may be represented by a third order polynomial. The non-linearity compensation network transfer function (or distortion function) must cancel out all terms of order higher than 1 in the VCO transfer characteristic, i.e.:

$$a_1 v + a_0 = a_3 v'^3 + a_2 v'^2 + a_1 v' + a_0 \tag{5.5}$$

where v is the original input voltage and v' is the modified input voltage (Figure 5.20). An analytical solution to equation (5.5) would be difficult if not impossible to implement in a simple analogue signal preprocessing circuit. The equation was therefore solved numerically and the solution fitted to a third order polynomial resulting in:

$$v' = c_3 v^3 - c_2 v^2 + v + c_0 \tag{5.6}$$

This equation can be implemented using analogue multipliers and operational amplifiers. Matlab simulations were used to confirm the theoretical analysis. An improvement of ~12 dB for second and ~15 dB for third harmonic distortion can be achieved, taking into account additional harmonic distortions caused by the employed multipliers and amplifiers [Schiller *et al.*, 1996].

5.4 Pulse Generator

The pulse generator is based on a standard circuit technique as shown in Figure 5.21. Note, a chain of transmission gates could be used in place of the inverter chain but this would not lead to significant savings in silicon area.

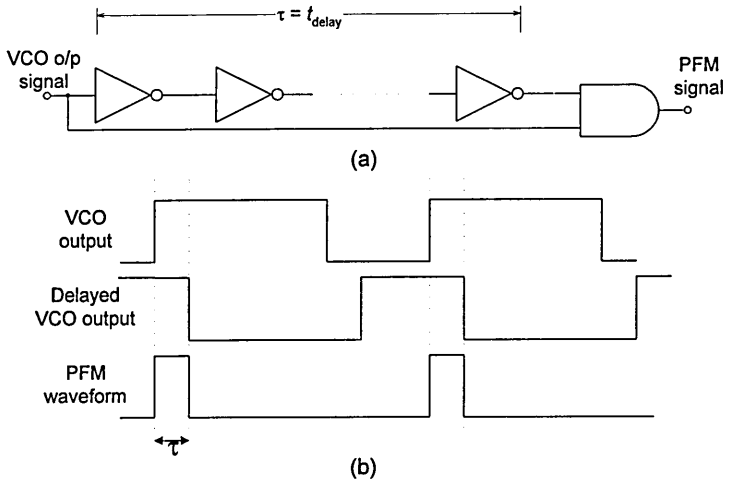

Figure 5.21: Pulse generator (a) circuit diagram (b) waveforms

5.5 Summary

Recognising the specifications laid out in the previous chapter, circuit specifications were developed for subsequent implementation. The PFM modulator circuit has then been developed using the top-down methodology by breaking the complex system into subsystems. For instance, the VCO design was divided into a current controlled oscillator design and the voltage to current converter design.

For each subsystem, critical performance parameters were given and different circuit implementations analysed. Detailed circuit description for the chosen implementation were given.

The PFM modulator will be based on a current controlled relaxation oscillator. This oscillator is based on charging and discharging two grounded capacitors. Applying two grounded capacitors instead of one as in conventional designs has several advantages. Less oscillation jitter is achieved due to an increased capacitor ramp amplitude. The influence of the capacitor voltage overshoot is reduced since the discharging time has no effect upon the frequency of oscillation.

The voltage to current converter is based on a current conveyor design. Current conveyors have proven to be very useful circuits in analogue signal processing and offer a better frequency characteristic than conventional circuits based on operational amplifiers. A circuit implementation of such a current converter has been presented. Palmisano and Palumbo [1995] have reported simulation results which showed that this circuit meets the performance criteria for the PFM modulator.

The pulse generating circuitry will be implemented using conventional digital circuit techniques such as an inverter chain to generate the necessary delay time. The PFM signal is generated from the VCO output signal by combining original and delayed signal using an AND gate. Initial simulation results presented in Chapter 3 showed that the chosen technology is capable of operating at the required speed.

CHAPTER 6

SUBCIRCUIT IMPLEMENTATION, SIMULATION AND MEASUREMENTS

6 SUBCIRCUIT IMPLEMENTATION, SIMULATION AND MEASUREMENTS

The previous chapter described the evolution of the chosen circuit design. This chapter introduces the subcircuit implementation of the PFM modulator. Simulation results indicating the predicted performance are also presented together with comparisons against practical measurements obtained from two fabricated ICs. The influence of capacitive loading of the measurement equipment is analysed in detail.

6.1 Initial Simulations and Tests

In order to test the accuracy of the available SPICE models for the Alcatel MIETEC 2.4 μm CMOS technology as provided by the foundry, a prototype circuit was designed and fabricated through EUROCHIP. A second objective was to test the design flow, the design tools and the routine necessary for design submission. The implementation also enabled an investigation into the effect of capacitive loading caused by measuring equipment and chip connections on prototyping ICs to be carried out.

This first fabricated design included single active and passive components as well as small subcircuits such as a Schmitt trigger and a CMOS switch. Figure 6.1 shows the circuit layout of this design. Two single MOSFETs can be identified in the top left-hand corner. Two resistors and two capacitors are laid out in the bottom right-hand corner. The Schmitt trigger circuit can be found in the top right-hand corner with an analogue buffer to its left.

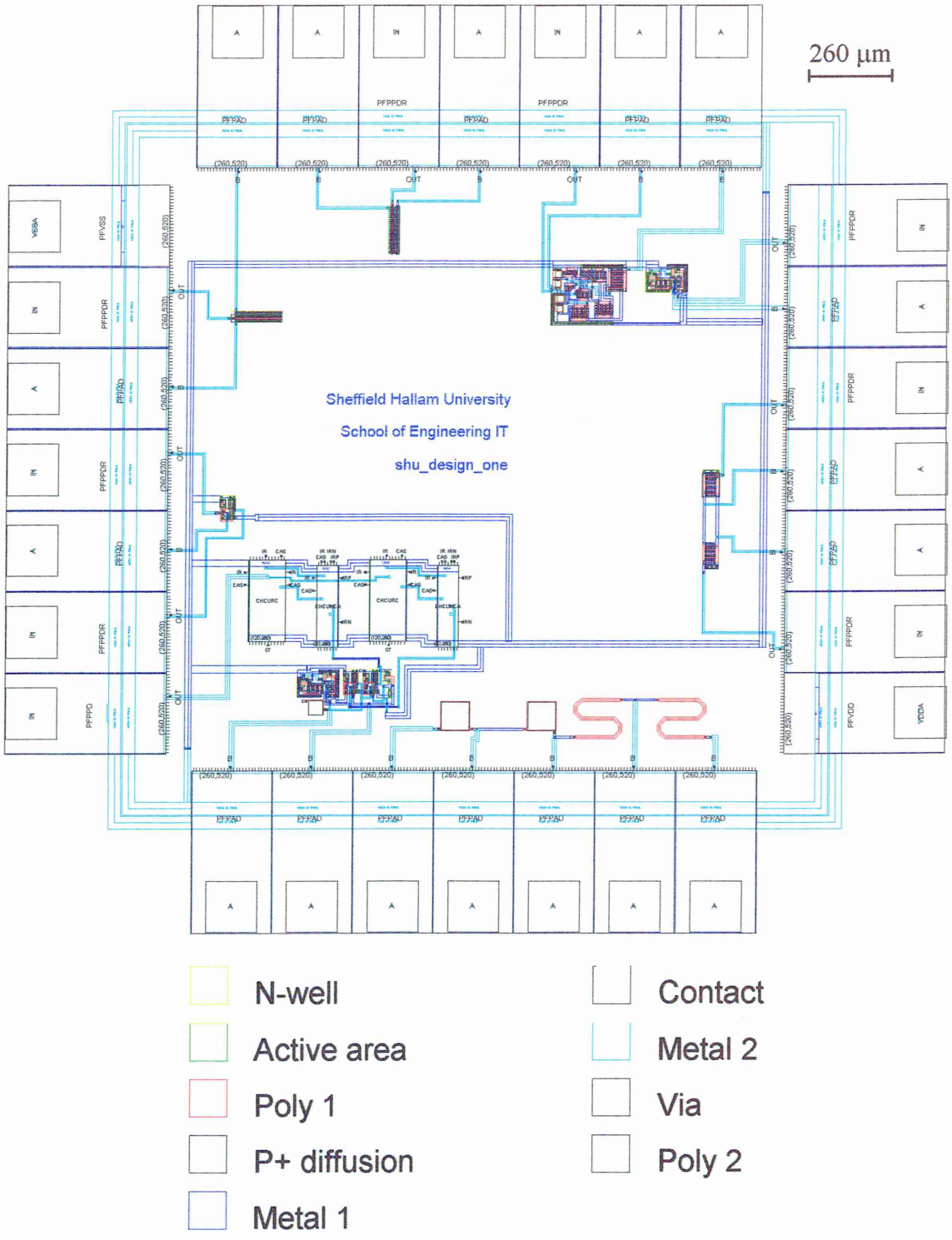

Figure 6.1: IC layout of first fabricated chip

6.1.1 Single transistor DC simulations and measurements

For DC measurements, parasitic capacitances do not influence the results and can be neglected. These measurements are used purely to confirm the large signal measured model parameters provided by the foundry (obtained as a mean from eleven runs) [Das, 1993]. MOSFETs simulations were performed using SPICE level 3 parameters. Boundary model parameters were calculated using average values (μ) and standard deviation (δ) with upper and lower limits defined as μ-δ and μ+δ, respectively. A small number of model parameters (threshold voltage, transconductance parameter and effective channel length) were also available for the actual run in which the chip was fabricated but these were not used since they are not normally available at the design stage. The difference between these and typical model parameters was less than 10 percent.

Practical DC measurements were carried out using a PL310QMT Thurlby & Thander dual voltage source and a HP3478A multimeter. Drain-source currents for various values of gate-source and drain-source voltages were obtained. Figure 6.2 shows the NMOST test circuit.

In total, nine circuits were measured from which the average and standard deviation values were calculated. The *t*-distribution has been used to determine the confidence interval for the mean μ of the small sample size of nine circuits. The percentage of confidence for the previously defined interval [μ-δ; μ+δ] has been calculated resulting

in a 98.5% confidence, indicating that more than 98 percent of all fabricated circuits should operate within that region [Rees, 1989].

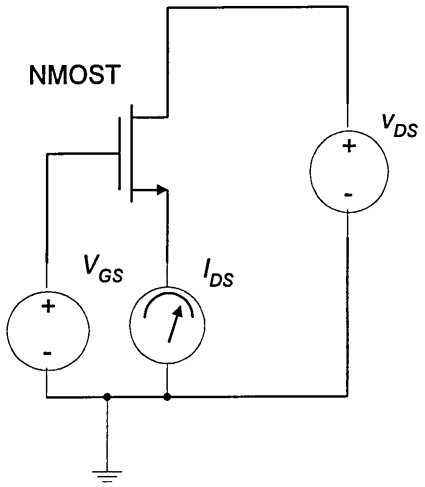

Figure 6.2: DC simulation and measurement setup

The simulation results obtained for a given set of foundry SPICE level 3 MOSFET model parameters and practical measurements are illustrated in Figure 6.3 and Figure 6.4 (for $v_{GS,SG} = 4$ V).

It can be observed that the measured results of the NMOS transistor are well within the simulated boundaries, whereas the PMOS transistor results are slightly shifted towards the upper limit. This is due to process variations resulting in a transconductance parameter which was above the defined upper limit for this particular run. The circuit operation can be considered predictable as long as the measured results lay within the simulated boundaries which is the case with these measurements.

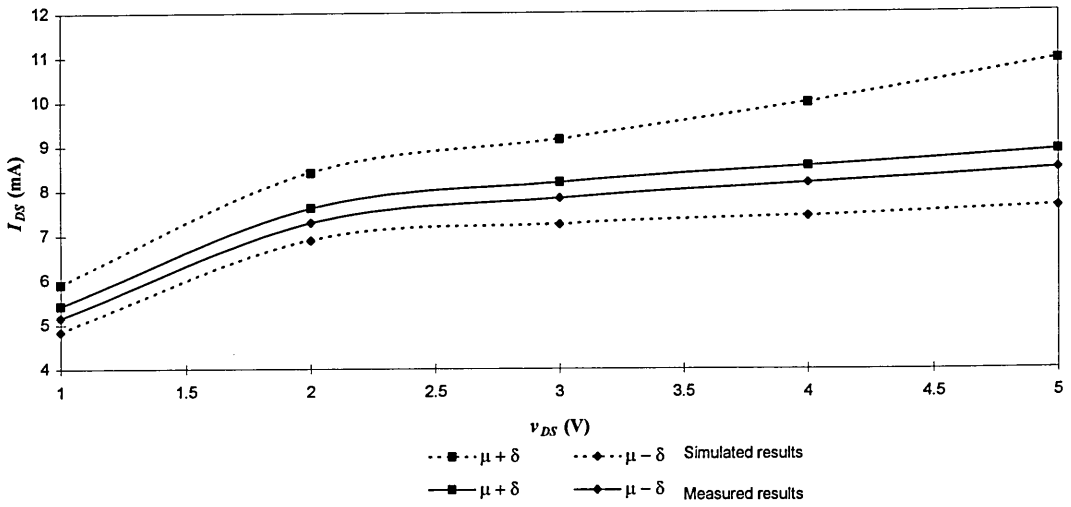

Figure 6.3: Comparison of measured and simulated NMOST DC characteristics

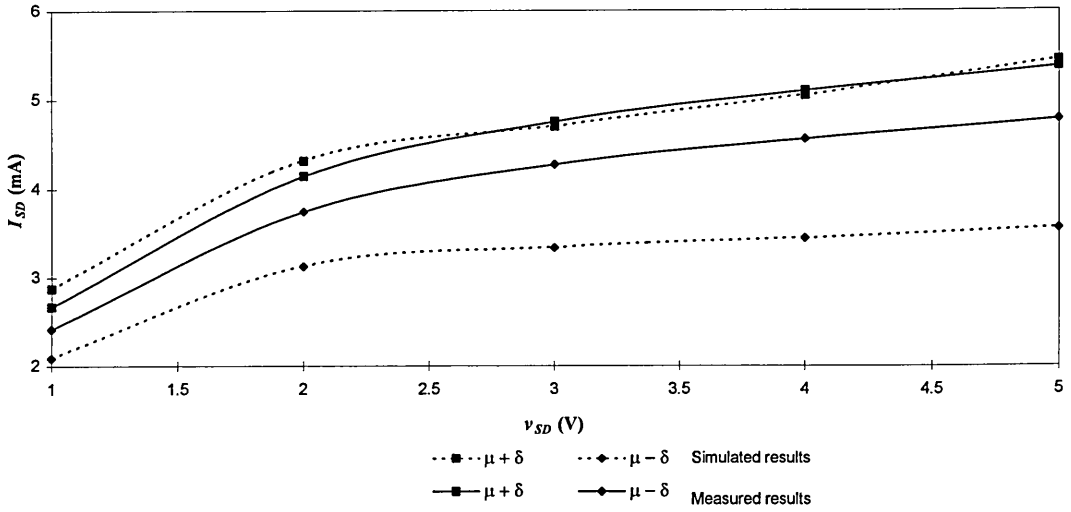

Figure 6.4: Comparison of measured and simulated PMOST DC characteristics

6.1.2 Transient simulations and practical measurement - capacitive loading of measuring equipment

The transient measurements will be influenced by all parasitic capacitances present. Therefore, the capacitive loading caused by the measuring equipment and chip

connections must be determined. Parasitic capacitances of the equipment contribute significantly to a degradation in performance.

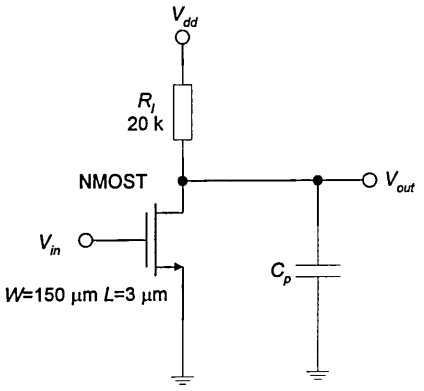

Figure 6.5: Transient simulation and measurement setup

Figure 6.5 shows the NMOST transient test circuit used for measurements. C_p represents the lumped off-chip parasitic capacitance. The load resistor (R_l) was chosen in such a way that it did not influence the switching characteristic of the MOSFET. R_l will always be in parallel with the on/off resistance of the transistor. The on-resistance is very small (a few hundred ohms) and is therefore not effected by the load resistance. On the other hand, with a large off resistance (a few Megohms) the charging of the lumped parasitic capacitance is governed solely by the value of R_l.

The parasitic capacitances are the most important factors limiting the switching speed. This was underlined by the fact that initial comparisons between simulated and practical results differed by over 200%. On analysis, the three major off-chip parasitic contributions were found to be the parasitic capacitance associated with the chip external connections and packaging (C_{p1}), the parasitic capacitance of the prototype PCB board (C_{p2}) and the capacitance loading of the measurement equipment (C_{p3}), i.e.

oscilloscope probe tip. Tests were conducted to determine the values of theses parasitics as attributable to the measurement setup which comprised printed circuit board, a HP54520A oscilloscope with a HP1144A active probe and a HP8116A function generator.

A unipolar square wave test signal of 5V amplitude at 500 kHz was applied to the gates of the MOSFET (Figure 6.5). The parasitic loading is assumed to be a load capacitance ($C_p = C_{p1}+C_{p2}+C_{p3}$) connected to the output of the test circuit, the charging of which is being described by the equation:

$$v = V_A\left(1 - e^{-\frac{t}{R_l C_p}}\right) \tag{6.1}$$

where V_A is the voltage amplitude of the test signal. With a known value for R_l and with rise time values (10%-90%) (t_r) as measured, C_p for the NMOST (C_{pNMOS}) is given by:

$$C_{pNMOS} = \frac{1}{R_l} \cdot \frac{t_r}{\ln 9} \tag{6.2}$$

Similarly, C_p of the PMOST (C_{pPMOS}) can be calculated from fall time (t_f) measurements, resulting in:

$$C_{pPMOS} = \frac{1}{R_l} \cdot \frac{t_f}{\ln 9} \tag{6.3}$$

Simulation results from HSPICE provided rise and fall times equivalent to zero added off-chip parasitics and, from the difference between these and the measured values (Table 6.1) an estimate of the off-chip parasitic loading can be made, i.e.:

$$C_l = \frac{1}{R_l} \cdot \frac{t_1 - t_2}{\ln 9} \tag{6.4}$$

Table 6.1: Simulation and practical rise and fall time measurements

	Practical measurements t_1	Simulation measurements t_2
NMOST rise times (ns)	336.67	11.27
PMOST fall times (ns)	372.89	15.96

This results in values of 7.4 pF and 8.12 pF for NMOST and PMOST, respectively. The ~10% difference may be caused by the input circuitry of the oscilloscope having a slightly different behaviour for rising and falling edges or slight inaccuracies in the values used in the SPICE transistor model.

Backannotating the off-chip parasitics into the simulation circuit should result in a very good agreement between practical and simulated rise and fall time measurements.

Table 6.2: Comparison of measured and simulated results

	NMOS transistor			***PMOS transistor***		
	Measured (ns)	*Simulated* (ns)	*Error* (%)	*Measured* (ns)	*Simulated* (ns)	*Error* (%)
Rise time	336.67	344.97	2.47	6.07	6.59	8.57
Fall Time	3.42	3.29	3.80	372.89	384.04	2.99

Results as shown in Table 6.2 indicate that almost all simulated rise and fall times are a little higher than the measured values. However, the errors are all less than 9% which could easily attributed to process variations between different runs and the nature of the

errors will provide a small safety margin between design parameters and those obtained in the practical circuit.

6.1.3 Concluding remarks on initial simulations and tests

The initial fabrication run confirmed the feasibility of the chosen IC design flow. The selected technology was incorporated into the design tools and the functionality has been proven. The design submission was successful and preliminary measurements on the fabricated circuit were carried out.

In addition, some problems associated with measuring the performance of the fabricated ICs could be identified. The significance of determining the capacitive loading caused by measurement equipment and chip connections has been demonstrated by the necessity to back annotate practical setup conditions into the simulated circuit in order to obtain good agreement between simulated and practical results.

The results obtained indicate that the set of foundry SPICE parameters used were sufficiently accurate since all practical results lay within the extremes of the simulated results and within the bounds of measurement tolerance.

6.2 Determination of Design and Layout Parameters

6.2.1 Voltage controlled oscillator

The circuit design of the VCO has been described in the previous chapter. The transfer characteristic of the VCO should linearly relate the input voltage to the output

frequency. Since the VCO design is comprised of a current controlled oscillator and current conveyor, the output frequency will be related to the current in the first instance.

Figure 6.6 shows an outline circuit diagram of the VCO. Assuming a constant current $I1 = I2 = I$, capacitors values $C1 = C2 = C$ and no switching delays, the charging of the capacitor from ground potential to the threshold voltage (V_{th}) of the comparator can be described as follows:

$$\frac{V_{th}}{\Delta t} = \frac{I}{C} \tag{6.5}$$

where Δt is the time needed to charge the capacitor from 0 V to V_{th}. For discharge, the capacitor is connected directly to ground and will therefore follow an exponential curve. Discharging, providing it is sufficiently rapid, will not effect the frequency of oscillation.

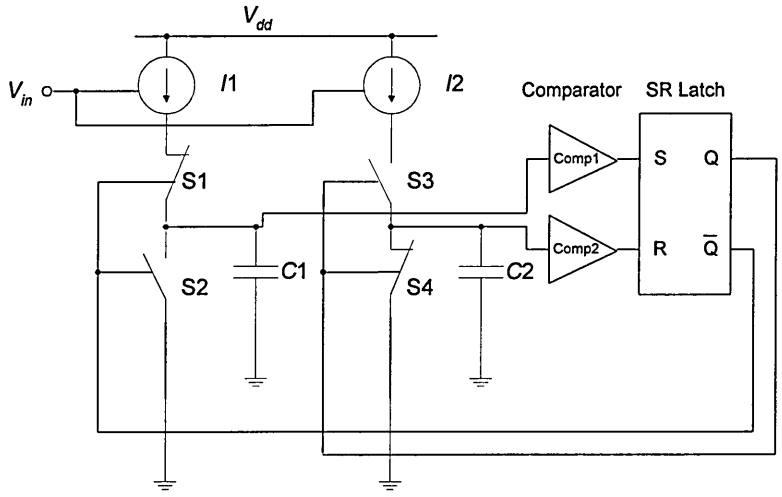

Figure 6.6: VCO circuit diagram

Each capacitor charging cycle is responsible for half the oscillating period (T), thus the frequency of oscillation (f_o) can be derived from equation (6.5) resulting in:

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{1}{2}\frac{I}{V_{th}C} \tag{6.6}$$

Equation (6.6) shows that the frequency depends upon three variables, current (I), comparator threshold voltage (V_{th}) and capacitance (C). This allows the designer two degrees of freedom (i.e. any two parameters may be chosen). Capacitor values should be kept small since they must be easily integrated on-chip and smaller capacitors will result in smaller area requirements making the IC cheaper. A capacitor value of 0.5 pF was initially chosen resulting in an area requirement of 1000 μm^2 (typical capacitance of a poly1-poly2 thin oxide layer is 0.5 $fF/\mu m^2$).

Different considerations have to be taken into account when deciding upon the threshold voltage. Figure 6.6 shows that the capacitor is charged via the voltage to current converter and the switch each of which requires a certain voltage level to operate. In order to decrease jitter, the voltage across the capacitor should be high but this is at the expense of reducing the remaining voltage level for operating the current sources and switches. The threshold voltage was, therefore, initially set to half the supply voltage, i.e. 2.5 V. An additional advantage of setting the threshold voltage to $V_{dd}/2$ is that logic gates from the MIETEC standard cell library may be used.

It was shown in Chapter 2 that a sampling ratio of at least 4 is required to minimise non-linear distortions, due to spectral overlap, to at least -40 dB. This requires the VCO to achieve a centre frequency of 24 MHz. Setting the capacitor value to 0.5 pF and the threshold voltage to 2.5 V, equation (6.6) can be solved for I resulting in:

$$I = 2 f_o V_{th} C = 2 \cdot 24 \cdot 10^6 \cdot 2.5 \cdot 0.5 \cdot 10^{-12} = 60\,\mu A \tag{6.7}$$

Equation (6.7) shows that a current of 60 μA is needed to achieve the required frequency. These calculations may be confirmed by simulation. It is likely that the frequency of oscillation will be significantly lower than predicted by calculations since no parasitic capacitances are taken into account. Since both of the timing capacitors are grounded at one side, the parasitics are effectively in parallel thus increasing the value of the capacitors. This may be compensated by decreasing the capacitor values or increasing the current.

To give a very low channel resistance for S2 and S4 and thus a rapid discharge of the timing capacitors the dimensions of the n-type switches are given the same dimensions as the p-type charging transistors S1 and S3. Therefore, only the dimensions of the p-type devices have to be determined.

It is difficult to determine accurately the geometries of the p-type transistor, since the rising voltage across the capacitors will drive the transistor from the saturated into the ohmic region. The worst case will be when the capacitor voltage is at its maximum, i.e. the drain-source voltage of the p-type switch is at its minimum. This case and the necessary voltages to determine the dimensions of the PMOST are shown in Figure 6.7. The voltages indicate that the PMOS transistor will be in the ohmic region and its *W/L* ratio can, therefore, be determined from the standard MOSFET equation.

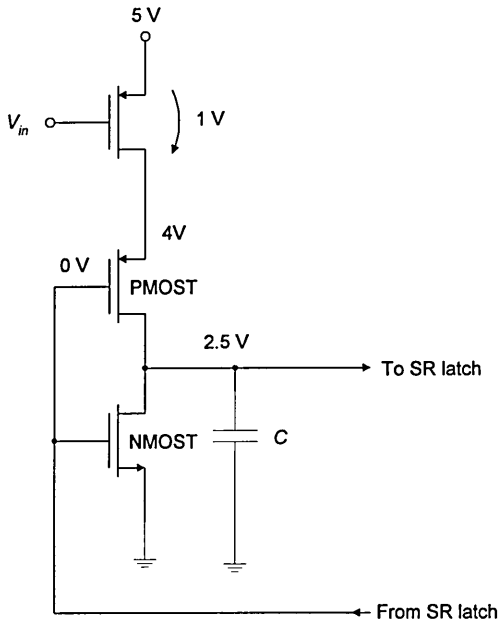

Figure 6.7: Circuit diagram of switches with maximum capacitor voltage amplitude

Preliminary simulations and analysis of the results indicated that a channel width of 50 μm and a length of 10 μm would be satisfactory.

It was shown in Chapter 5 that the switching delay will cause a non-linearity in the transfer characteristic. Flynn and Lidholm [1992] showed that the actual frequency (f_a) can be related to the ideal frequency (f_i) by the following equation:

$$f_a = \frac{f_i}{1 + T_d f_i} \tag{6.8}$$

where T_d is the switching delay. This non-linearity will cause harmonic and intermodulation distortion.

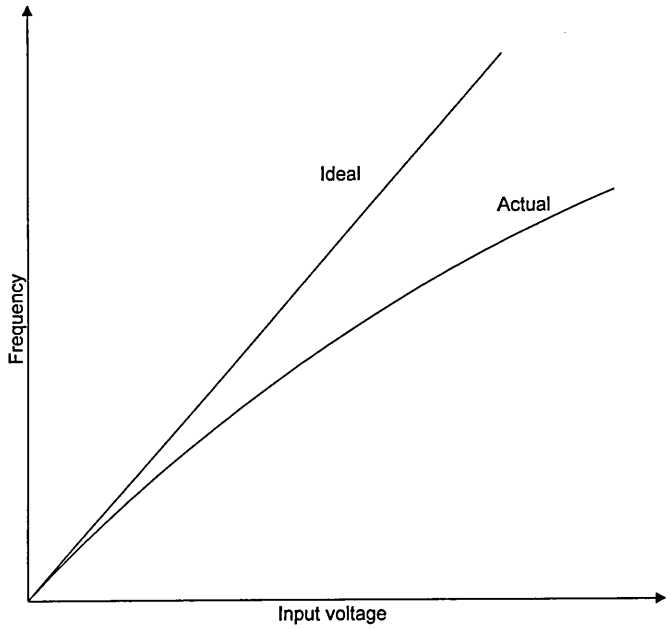

Figure 6.8: Deviation from ideal frequency caused by switching delay

The harmonic distortion can be calculated by expanding equation (6.8) into a series:

$$\frac{f_i}{1+T_d f_i} = T_d^2 f_i^3 - T_d f_i^2 + f_i + E \tag{6.9}$$

where E is the error introduced by calculating the series for only three terms. This error can be calculated from equation (6.9) and was found to be 0.49% for $T_d = 7$ ns and $f_i = 24$ MHz and is, therefore, negligible.

A sinusoidal input voltage results in:

$$\begin{aligned} f_i(t) &= \sin(\omega t) \\ f_i(t)^2 &= \sin(\omega t)^2 = \frac{1}{2} - \frac{1}{2}\cos(2\omega t) \\ f_i(t)^3 &= \sin(\omega t)^3 = \frac{3}{4}\sin(\omega t) - \frac{1}{4}\sin(3\omega t) \end{aligned} \tag{6.10}$$

with $\omega = 2\pi f_i$. Substituting equation (6.10) into equation (6.9) results in:

$$-\frac{T_d^2}{4}\sin(3\omega t)+\frac{T_d}{2}\cos(2\omega t)+\left(1+\frac{3}{4}T_d^2\right)\sin(\omega t)-\frac{T_d}{2} \tag{6.11}$$

Second and third harmonic distortion can now be determined:

$$HD_2 = 20\log\left(\frac{2T_d}{4+3T_d^2}\right) \tag{6.12}$$

$$HD_3 = 20\log\left(\frac{T_d^2}{4+3T_d^2}\right) \tag{6.13}$$

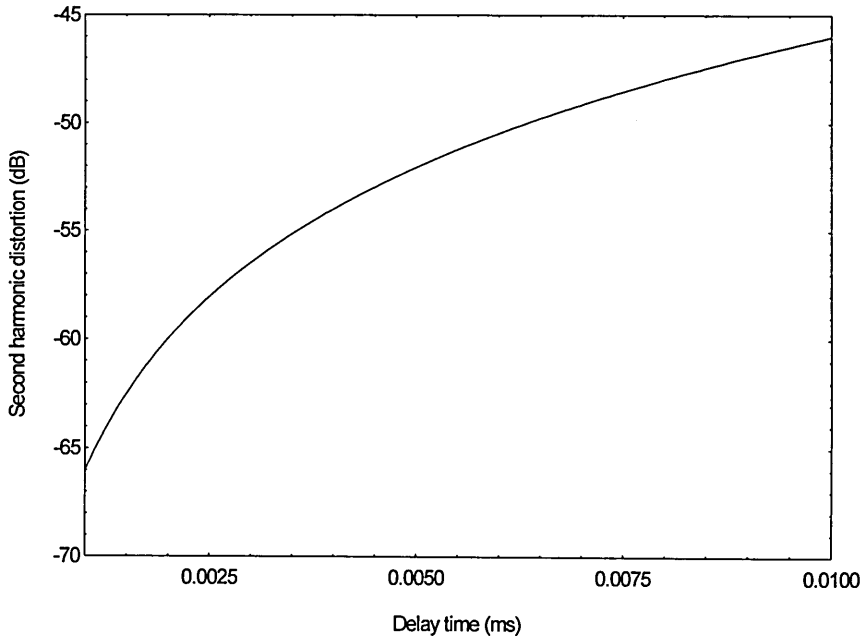

Figure 6.9: Predicted second harmonic distortion

Figure 6.9 shows the graphical representation of equation (6.12). Note that for a delay time of less than 10 ns, a theoretical second harmonic distortion level of less than -45 dB is predicted.

HSPICE simulations of the VCO circuit (Figure 6.10) indicated that the output frequency was much lower than predicted. A current of 60 μA resulted in a simulated frequency of 12.9 MHz. This difference to the theoretically predicted frequency of 24 MHz is attributable to two factors, switching delay and parasitic capacitances. The influence of the switching delay upon the frequency was shown in equation (6.8) and results in a deviation from the ideal frequency. The second factor influencing the frequency performance is due to parasitic capacitances associated with the switches and the input transistors of the SR latch.

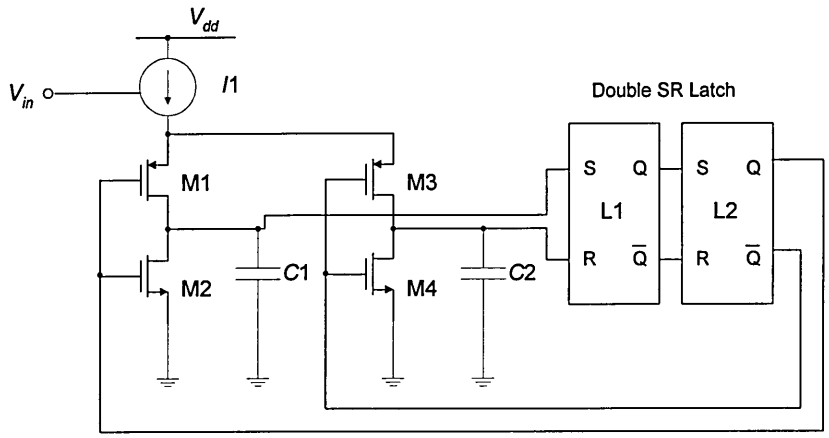

Figure 6.10: Simulated VCO circuit diagram

The simulation results were also used to confirm the harmonic distortion analysis. Necessary for this analysis was a knowledge of the delay time. Using simulation results, the propagation delay of the SR latch was found to be 4.87 ns. This would relate to a harmonic distortion of -52.27 dB which is well below the required -40 dB level. The input current $I1$ was varied from 15 μA to 105 μA in steps of 10 μA corresponding with ±45 μA on a DC offset of 60 μA. Since the earlier analysis assumed a sinusoidal input with no DC offset this offset was removed.

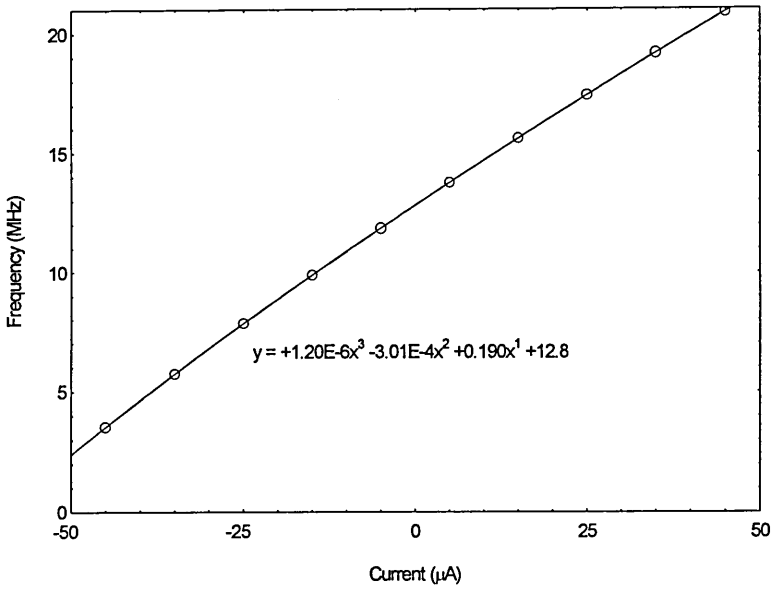

Figure 6.11: Transfer curve of CCO simulation

Figure 6.11 shows the simulation results without the DC offset. A third order polynomial curve fit was applied to this graph and, from this, the harmonic distortion was calculated as follows:

The polynomial curve fit resulted in the following transfer function:

$$h(t) = 1.2 \cdot 10^{-6} x^3(t) - 3.01 \cdot 10^{-4} x^2(t) + 0.19 x(t) + 12.8 \qquad \textbf{(6.14)}$$

Substituting a sinusoidal input current into equation (6.14) results in:

$$h(t) = -\frac{1.2 \cdot 10^{-6}}{4} \sin(3\omega \cdot t) + \frac{3.01 \cdot 10^{-4}}{2} \sin(2\omega \cdot t) + \left(0.19 + \frac{3}{4} 1.2 \cdot 10^{-6}\right) \sin(\omega \cdot t) + 12.8 - \frac{3.01 \cdot 10^{-4}}{2} \qquad \textbf{(6.15)}$$

Using a similar approach as in equation (6.12) the second harmonic distortion level is -62.02 dB, i.e. better than predicted by ~10 dB. This may be due to additional

unaccounted non-linearities which oppose the known non-linearity caused by switching delays.

The total switching delay can be estimated from the simulation transfer function, Figure 6.12. A first order curve fit, representing a linear transfer function, results in:

$$f_i = 0.221 \cdot I + 0.213 \tag{6.16}$$

Substituting this into the equation developed by Flynn and Lidholm [1992] gives:

$$f_a = \frac{0.221 \cdot I + 0.213}{1 + T_d(0.221 \cdot I + 0.213)} \tag{6.17}$$

Another curve fit using equation (6.17) with the time delay T_d as the unknown variable was then applied to the simulation results.

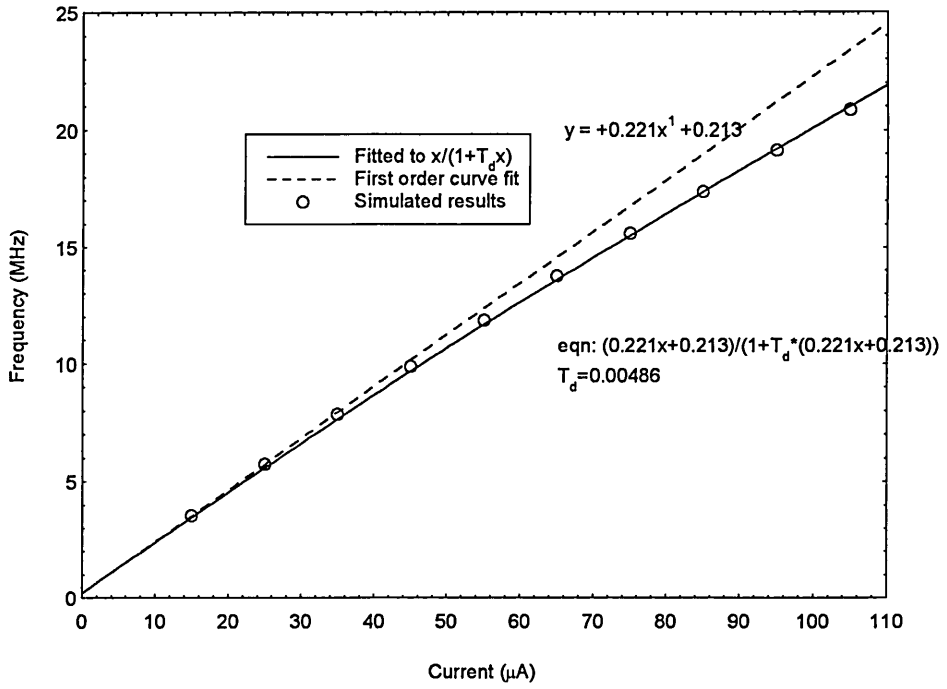

Figure 6.12: Estimation of switching delays

From this a predicted value for T_d of 4.86 ns was obtained which is in close agreement with the simulated propagation delay of the double SR latch of 4.87 ns.

The analysis of the initial simulation results indicated that some circuit parameters need to be adjusted to compensate for parasitics lowering the output signal frequency. This is achieved by decreasing the timing capacitor value to 0.35 pF and by increasing the current until the required oscillation frequency is achieved.

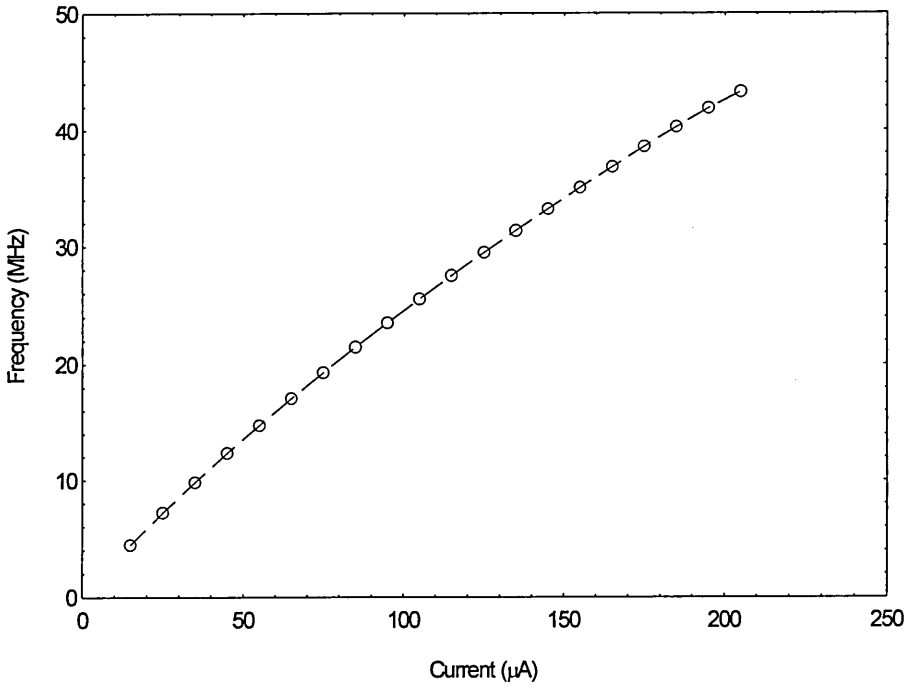

Figure 6.13: Current controlled oscillator simulation

Figure 6.13 shows the result of this simulation. It can be seen that an oscillation frequency exceeding 40 MHz is achievable (40 MHz ≡185 μA).

6.2.2 Pulse generation circuitry

The pulse generation circuitry consists of an inverter chain/AND gate combination as shown in Figure 5.21. The delay time of the inverter chain is equal to the pulse width (τ) of the resulting PFM pulse train. Suitable logic gates were available from the MIETEC standard cell library and these were, therefore, employed for this part of the circuit. Trial simulations indicated that nine inverters would provide a delay time of 5-6 ns.

Wickramasinghe *et al.* [1995] showed that in a PFM system, an adequate signal performance can be delivered by limiting the transmission bandwidth to $1/\tau$ when the duty ratio (D) of the PFM pulse train is kept below 25%. The duty ratio can be defined as:

$$D = \frac{\tau}{T} \tag{6.18}$$

where T is the oscillation period. The maximum oscillation period T_{max} of the modulated PFM pulse train may be expressed as:

$$T_{\max} = \frac{1}{f_c + \frac{\Delta f_{\max}}{2}} \tag{6.19}$$

where f_c is the centre frequency and Δf_{max} is the maximum frequency deviation. The maximum frequency deviation at a modulation index of 1 is 6 MHz. Assuming a sampling ratio of 4 (f_c = 24 MHz), the duty ratio can be calculated employing equations (6.18) and (6.19) resulting in 16.2% and increasing to 21% for a sampling ratio of 5 (f_c = 32 MHz). Both values are below the required duty ratio of 25% and it can be

concluded that a pulse width of 6 ns is sufficient for the requirements. Even a pulse width of 7 ns at a sampling ratio of 5 would still result in a duty ratio of the PFM pulse train which is below 25%.

6.2.3 Second design submission

In order to test the feasibility of the proposed design, an initial chip layout of the PFM modulator was designed and submitted to EUROCHIP for production (Figure 6.14). This chip contained the oscillator part and the pulse generator. The voltage to current converter was implemented using p-type MOSFETs.

Unfortunately, due to problems with the design implementation the pulse generator did not function correctly. Only the oscillator part could, therefore, be tested. This was possible since additional connections were designed originally to access the timing capacitances externally.

Figure 6.15 shows the waveforms across the timing capacitances as measured with a Tektronix TDS684A digital oscilloscope and P6245 active probes. It is clear that the capacitances are (a) charged linearly and (b) discharged well in advance of the next charging period.

The oscillation frequency is well below the simulated results due to external capacitive loading of the oscillator circuit by the measurement equipment.

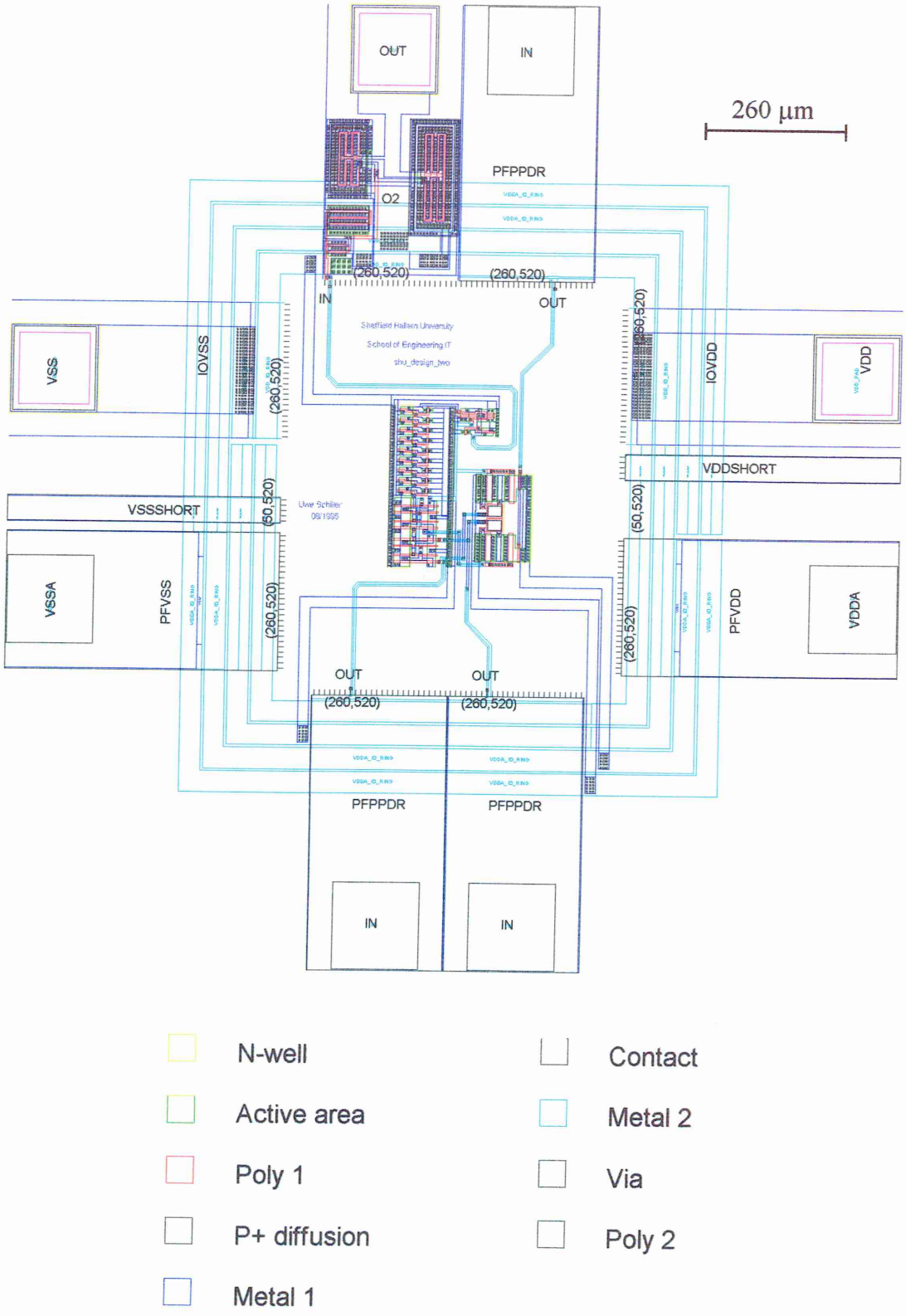

Figure 6.14: IC layout of second fabricated chip

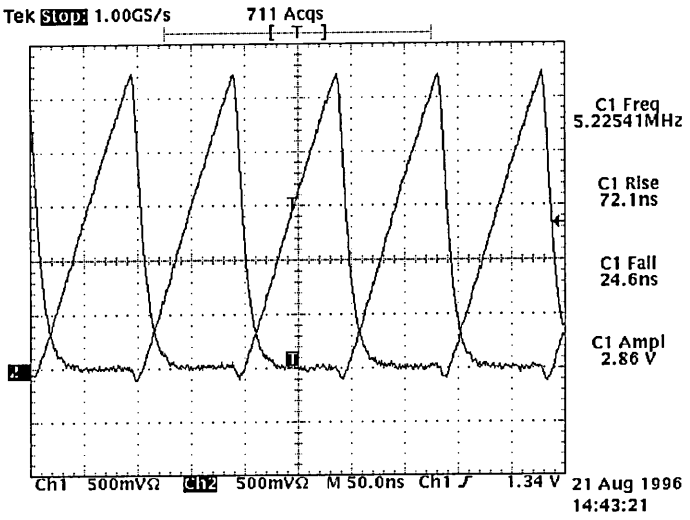

Figure 6.15: Voltages across the timing capacitors (V_{in} = 1.35 V)

An analysis of the effect is described in Appendix B from which it was concluded that a parasitic loading of 5 pF was caused by interconnections and measurement equipment. By backannotating this value into the HSPICE simulation a comparison between measured and simulated results could be carried out and a close agreement was found to exist (Figure 6.16).

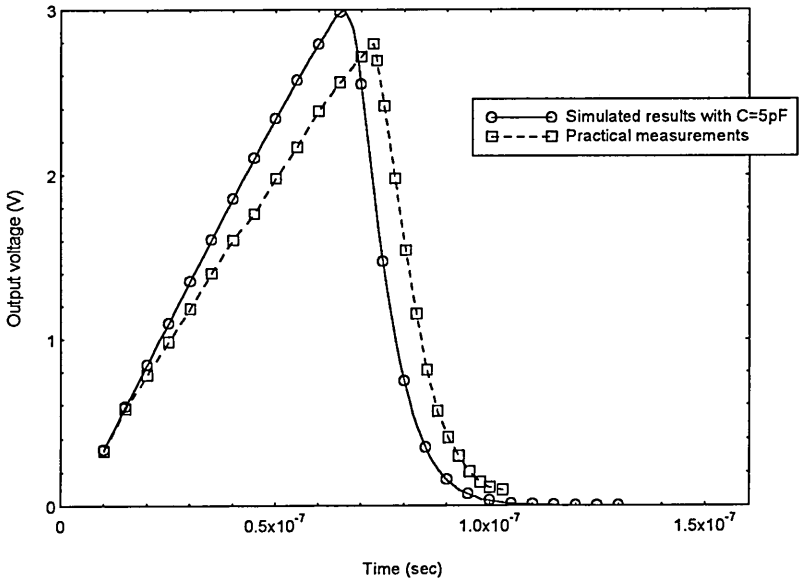

Figure 6.16: Comparison of simulated and practical measurements

The results obtained indicated that the proposed design was feasible and the simulations were reliable. The variations observed are within the limits of process variations and measurement tolerances.

6.2.4 Voltage to current converter

The voltage to current converter is based on a current conveyor circuit as shown in Figure 5.18 (p. 98). The transfer characteristic is given as:

$$R = \frac{V_{in}}{I} \tag{6.20}$$

From Figure 6.13 it can be determined that a current of about 100 μA is necessary to achieve the required carrier frequency of 24 MHz. The DC offset voltage is set to 3 V resulting in a resistor value of 30 kΩ. For proper operation of the current conveyor, the input voltage should be larger than the threshold voltage of the input transistor. Therefore, the effective voltage swing is limited to the region of 1 V to 5 V. The DC offset is set to the middle of that region.

The current conveyor circuit, as shown in Figure 6.17 was introduced in Chapter 5. The circuit parameters are calculated below:

The bias current I_B is set to 20 μA. Transistor M8 is in saturation and its drain current (I_{dM8}) can, therefore, be described as follows:

$$I_{dM8} = \frac{k'_n}{2}\frac{W}{L}(v_{GS} - V_T)^2 \tag{6.21}$$

where v_{GS} and V_T are the gate-source and threshold voltage, respectively, k'_n is the NMOST transconductance parameter and W and L are the width and length of the channel, respectively.

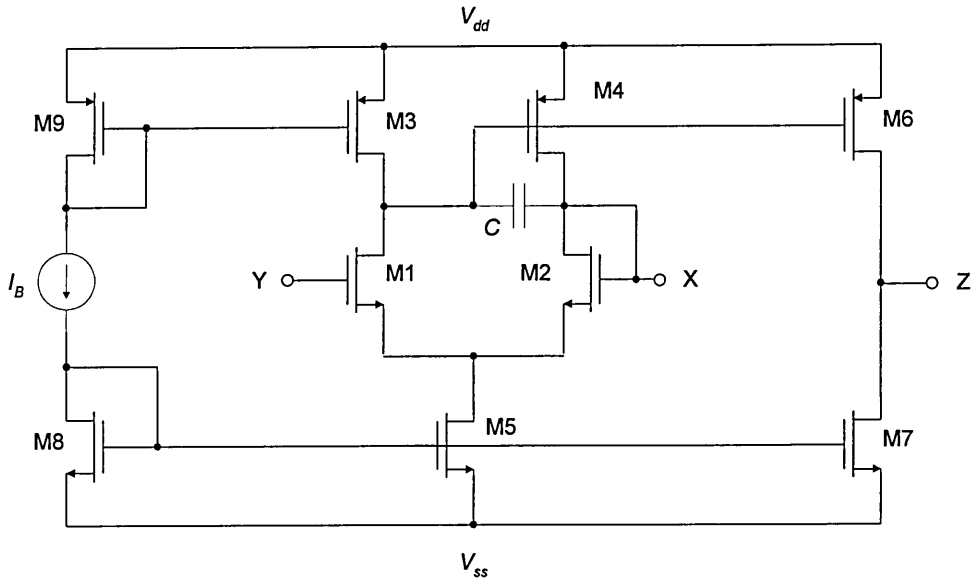

Figure 6.17: Current conveyor circuit diagram

The voltage difference 'v_{GS} - V_T' is set to 0.15 V to achieve a minimum voltage drop across M8. With I_{dM8} being equal to I_B and 'v_{GS} - V_T' set to 0.15 V the channel geometry of M8 can be determined to be 105/3. Since drain current of M8 is equal to drain current of M9 the channel geometry for M9 can be determined as follows:

$$\frac{(W/L)_{M9}}{(W/L)_{M8}} = \frac{k'_n}{k'_p} \tag{6.22}$$

resulting in 290/3 (k'_p is the PMOST transconductance parameter). M9 and M3 form a current mirror and making their geometries equal results in equal drain currents. M1 acts a voltage follower, hence every input voltage change is reflected by an equal change in source voltage. Setting $I_{dM5} = 2I_{dM3}$ makes the drain current of M2 equal to

that of M1 assuming that both transistors are matched. This will force the gate-source voltages of M2 and M1 to be equal and thus the voltage at the 'X' terminal will follow the voltage at the 'Y' terminal. Since M1 to M3 are fixed at their quiescent values, the input current at the 'X' terminal must be supplied by M4.

Assuming M4 and M6 are matched, their drain currents will be equal since they both have the same gate-source voltage. The current in M4 is the sum of the input current at the 'X' terminal (I_x) and the current of M2, hence it can be written as:

$$I_{dM4} = I_{dM6} = I_{dM2} + I_x \tag{6.23}$$

The output current at terminal 'Y' (I_y) is the difference of the drain currents of M6 and M7 and can therefore be written as follows:

$$I_y = I_{dM6} - I_{dM7} \tag{6.24}$$

Comparing equations (6.23) and (6.24) it is clear that in order to fulfil the requirement of a unity gain current transfer, the drain currents of M2 and M7 must be equal. This can be achieved by making $(W/L)_{M7}$ half the size of $(W/L)_{M5}$.

$$I_y = I_x = I_{dM6} - I_{dM2} \tag{6.25}$$

The bias current I_B is generated using the circuit shown in Figure 6.18. M11 and M12 are providing a bias voltage for transistor M10. The dimensions of M10 are set to W/L=20/5. The biasing conditions, calculated using equation (6.21), result in the source voltage of M10 being 1 V. The channel geometry for M10 can now be calculated using the following equation:

$$V_{gM10} = \frac{2I_B}{k'_n (W/L)_{M10}} + V_T + 1 \tag{6.26}$$

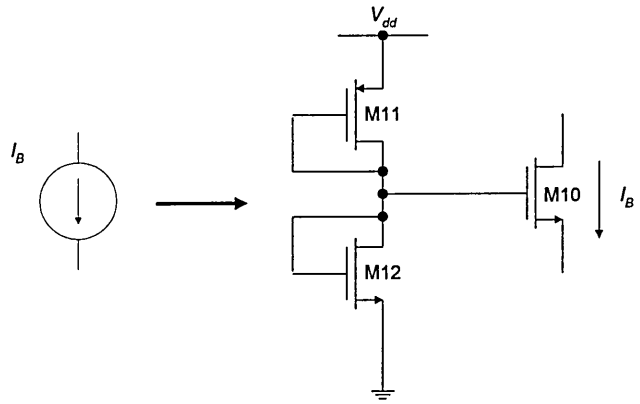

Figure 6.18: Circuit used to provide bias current

M11 and M12 are in saturation and their drain currents are equal. Setting either $(W/L)_{M11}$ or $(W/L)_{M12}$ to 1, the other ratio can then be calculated from the following equation:

$$\frac{k'_p (W/L)_{M11}}{2}\left(V_{DD} - V_{gM10} - V_T\right)^2 = \frac{k'_n (W/L)_{M11}}{2}\left(V_{gM10} - V_T\right)^2 \tag{6.27}$$

Simulations were carried out to confirm the operation of the current conveyor. These simulations were also used to fine-tune the parameters of the circuit to the specific requirements of the VCO. The values of the channel geometries are given in Table 6.3.

Table 6.3: Channel geometries of current conveyor circuit

Transistor	*W/L* ratio
M1, M2, M7, M8	120/3
M5	240/3
M3, M4, M6, M9	315/3
M10	20/5
M11	8/7
M12	4/6

The current conveyor was tested with one resistor (R_{in}) of 30 kΩ connected to the 'X' terminal and another resistor (R_{out}) of the same value connected to its 'Z' terminal as shown in Figure 6.19. If V_x follows V_{in} and I_z follows I_x accurately, then V_{out} should be equal to V_{in}.

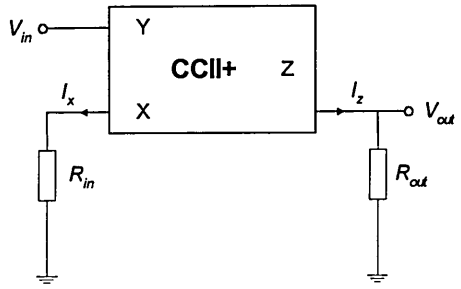

Figure 6.19: Simulation test configuration of current conveyor

Several simulations where carried out to confirm the performance of the current conveyor.

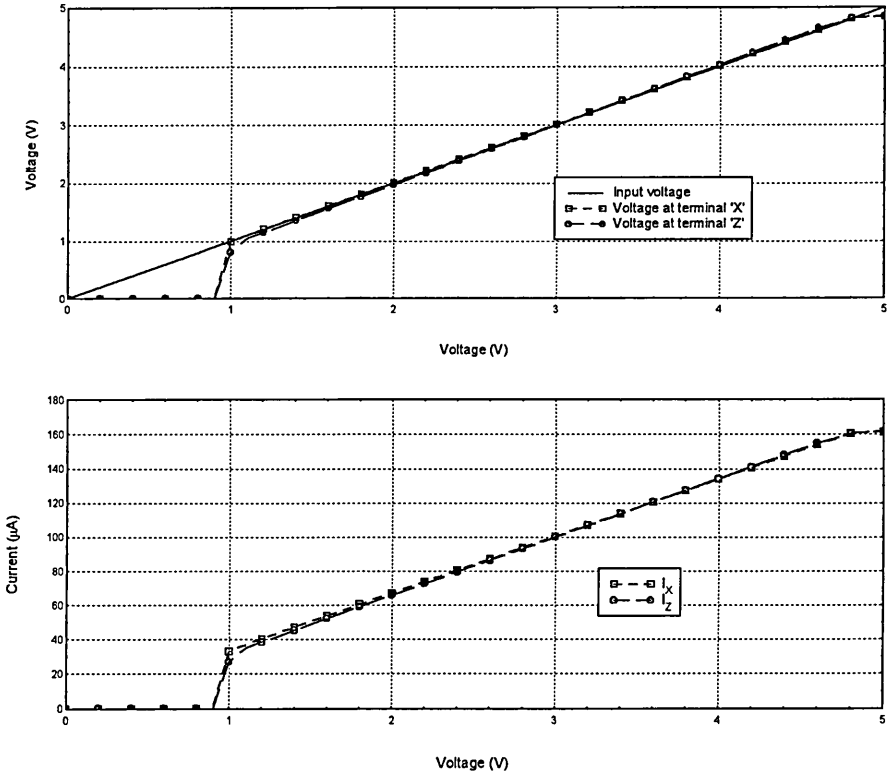

Figure 6.20: Results of DC simulations

The DC results are shown in Figure 6.20. The top graph indicates that the voltage at the 'X' terminal follows closely the voltage at the 'Y' terminal. Furthermore, the voltage across R_{out} caused by the current I_z is almost identical to the voltage across R_{in} indicating that a very good current transfer characteristic has been achieved. This is also underlined by the bottom graph of Figure 6.20, which shows that the currents through R_{in} and R_{out} are almost identical. The bottom graph also indicates that at a input voltage of 3 V a current of 100 μA is achieved as necessary for a oscillation frequency of 24 MHz as shown in Figure 6.11.

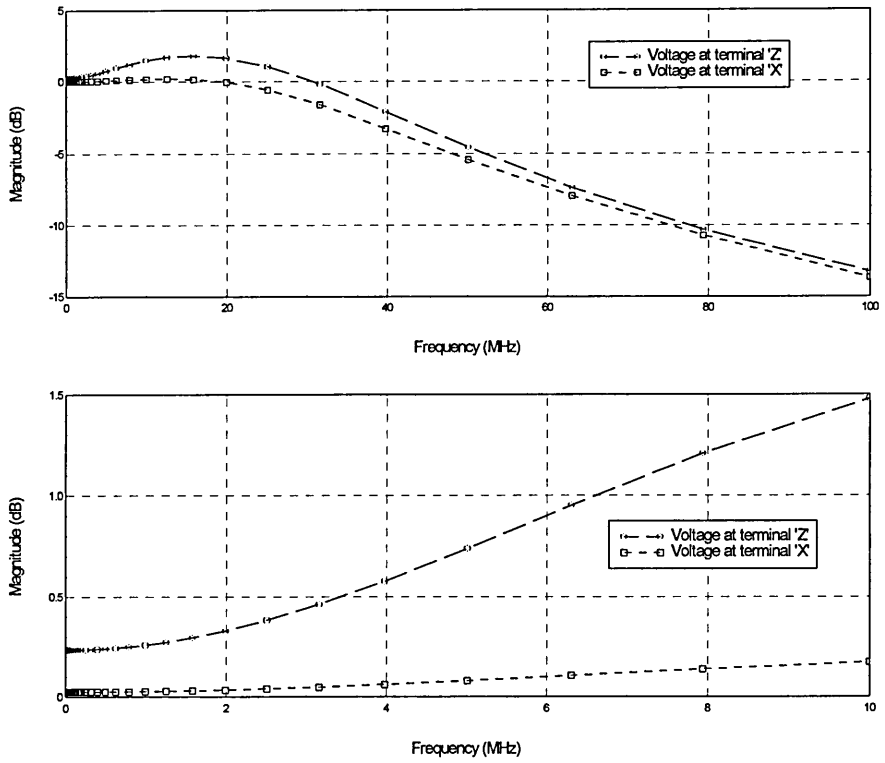

Figure 6.21: Results of AC simulations

Figure 6.21 shows the results of the AC simulations. The bottom graph shows only that region of the top graph which is of interest for the PFM modulator. This indicates that the voltage transfer from 'Y' to 'X' is almost constant over the frequency range from

1 kHz to 6 MHz reaching 0.2 dB at 10 MHz. The voltage across R_{out} (voltage at terminal 'Z') is overshooting, reaching 0.9 dB at 6 MHz. This would relate to a voltage error of 10% at that frequency. Simulations confirmed that this error is marginal and does not effect the overall performance of the PFM modulator.

6.3 Summary

This chapter has analysed the different subcircuits which were evolved in Chapter 5 and has presented initial simulation and measurement results. The results indicated that the proposed circuit can fulfil the requirements of the PFM modulator laid out in Chapter 2. Furthermore, it has been shown that the chosen technology is able to operate over the required frequency range.

Whilst analysing the subcircuits, problems influencing the performance have been indicated and the effect has been analysed. The switching delay, for instance is causing non-linearity of the VCO transfer characteristic. It has been shown that this non-linearity is well below the required -40 dB level and therefore be negligible.

Measurements carried out on initial designs fabricated through EUROCHIP showed that the measurement equipment is causing a parasitic loading which can effect the circuit performance considerably. Measurements have been carried out which allowed the capacitive loading of this equipment to be determined. The results obtained indicate that a capacitive loading of 5-8 pF, depending upon the measurement setup, must be taken into account for the final design of the PFM modulator.

CHAPTER 7

RESULTS AND DISCUSSIONS

7 RESULTS AND DISCUSSIONS

This chapter describes the final circuit implementation and presents simulation and measurement results of the final design. In order carry out a PFM system test an entire transmission system consisting of modulator and demodulator was implemented. A comparison between measured and simulated results is given and a performance evaluation of the system with regard to the transmission of TV signals is also presented. Finally, the modulator is compared with two commercially available PFM modulators.

7.1 Final PFM Modulator Implementation

7.1.1 Complete circuit diagram

The PFM modulator circuit was described in Chapter 5 with subcircuit implementations, preliminary simulation results and measurements presented in Chapter 6. The complete PFM modulator circuit is shown in Figure 7.1. Three blocks can be identified, the current conveyor configured as voltage to current converter, the current controlled oscillator and the pulse generator. The final output buffer is necessary to ensure external loads do not degrade the output signal of the pulse generation circuit.

7.1.2 IC layout of PFM modulator

The performance of the PFM modulator is critically dependent upon its silicon layout. Matching of the components is very important for the differential pair in the current conveyor, for the switching transistors and for the timing capacitors. Any mismatch will result in a performance degradation. The differential pair is implemented as a

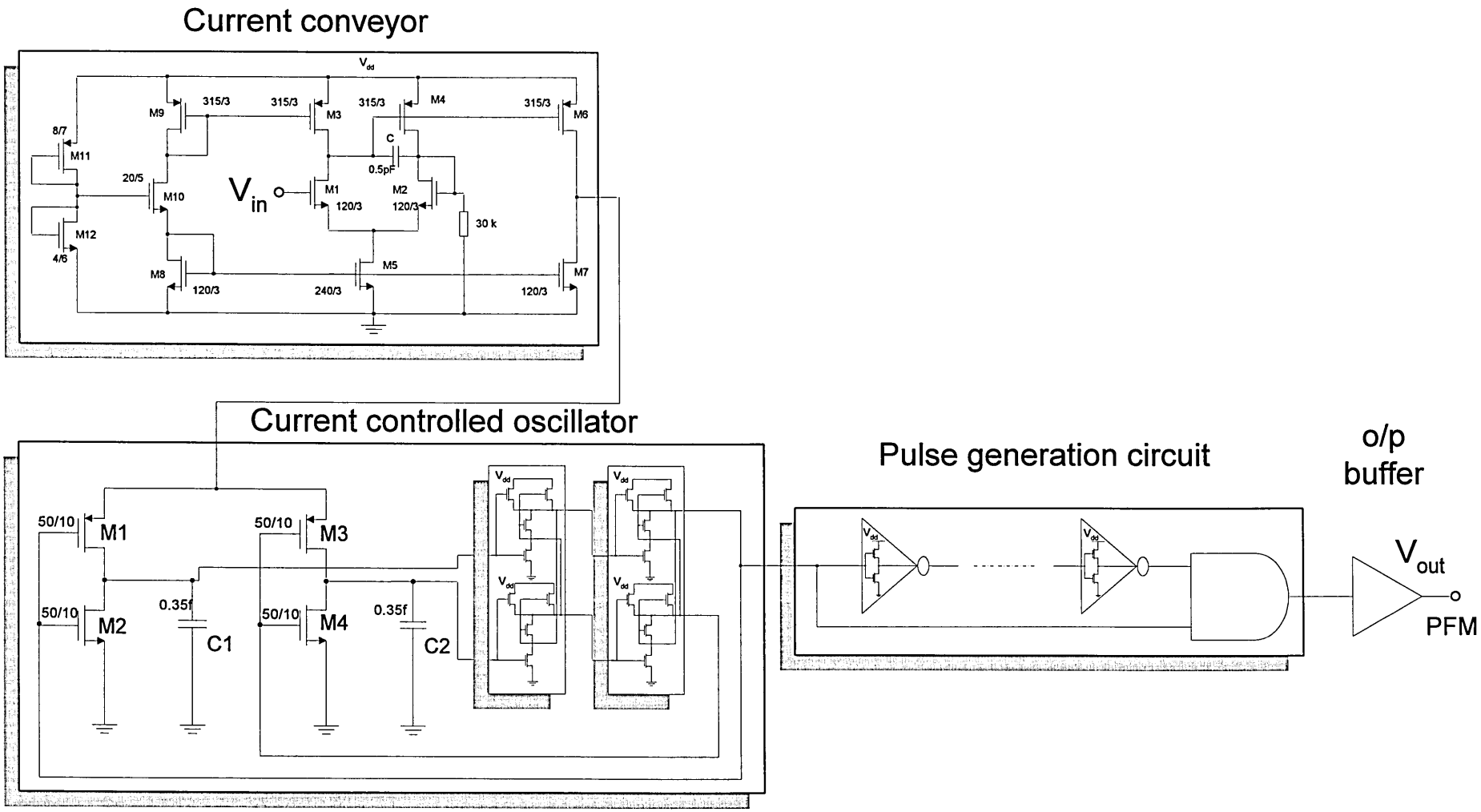

Figure 7.1: Complete circuit diagram of PFM modulator

interdigitized layout with dummy transistors at either ends of the structure. The two switching transistors and their associated timing capacitors are laid out as symmetrically as possible to ensure equal charging times. The output buffer is implemented using the MIETEC standard cell library.

The PFM waveform consist of very narrow pulses which will result in relatively high peak currents. The power supply lines must, therefore, be sufficiently wide to ensure they exhibit a very low sheet resistance. The same conditions apply for power connections from metal 1 to metal 2 lines where the maximum possible area should be used to ensure a low overall contact resistance. The power supply of the current conveyor is separated from the rest of the circuit in order to prevent switching pulses effecting the performance of the voltage to current converter. Two separate power supply lines are, therefore, employed, one for the analogue and one for the digital part of the circuit.

The finalised IC layout of the PFM modulator is shown in Figure 7.2. The power rings for analogue (PFVDD, PFVSS) and digital (IOVDD, IOVSS) supplies run around the periphery with spur feeders to the PFM circuit elements. The double SR latch and pulse generating circuitry are at the top of the layout diagram. The switching transistors are symmetrically placed on each side of the timing capacitors to ensure a good matching of the VCO timing elements (mid left hand side). The current conveyor is placed to the left and bottom of the switching transistors. The output buffer is included in the Mietec output cell (O2). The input cell (PFPPDR) contains a voltage protection circuit consisting of two diodes and a polysilicon resistance.

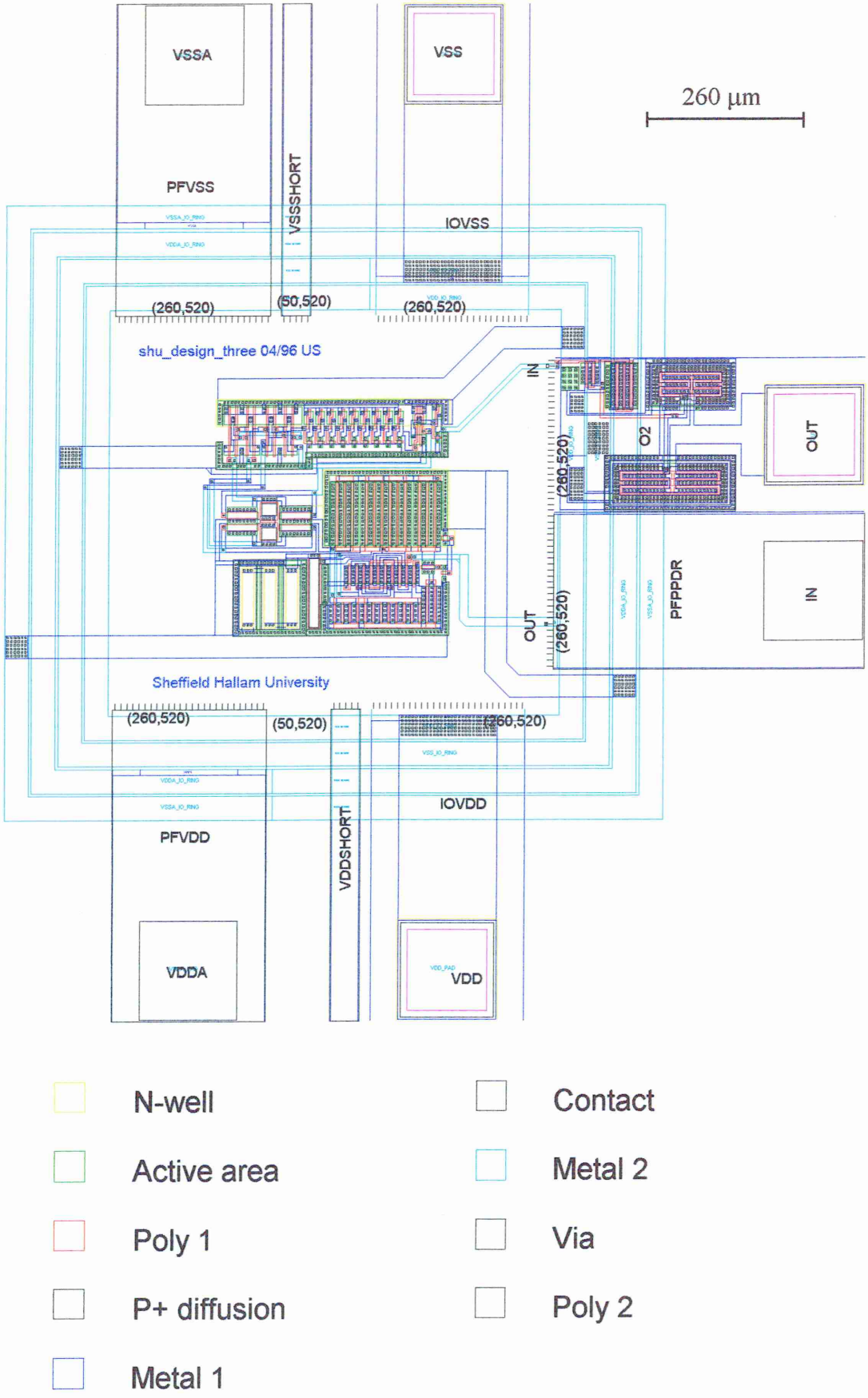

Figure 7.2: IC layout of PFM modulator

7.1.3 Simulation results

A SPICE netlist was extracted from the IC layout using MG's IC Extract software. This netlist was simulated using SPICE level 3 transistor parameters. The output buffer is included as a subcircuit from the model files provided by the foundry. A 5 pF capacitance is connected to the output of the buffer simulating the loading effect of external circuitry or measurement equipment. A complete HSPICE netlist is shown in Appendix C.

Several simulations were carried out to determine the performance of the PFM modulator initially in terms of the achievable pulse width and frequency transfer characteristic. With a constant DC input voltage a transient analysis was carried out. Figure 7.3 shows the resulting pulse train for a DC input voltage of 2.5 V. The pulse width is measured as 5.62 ns.

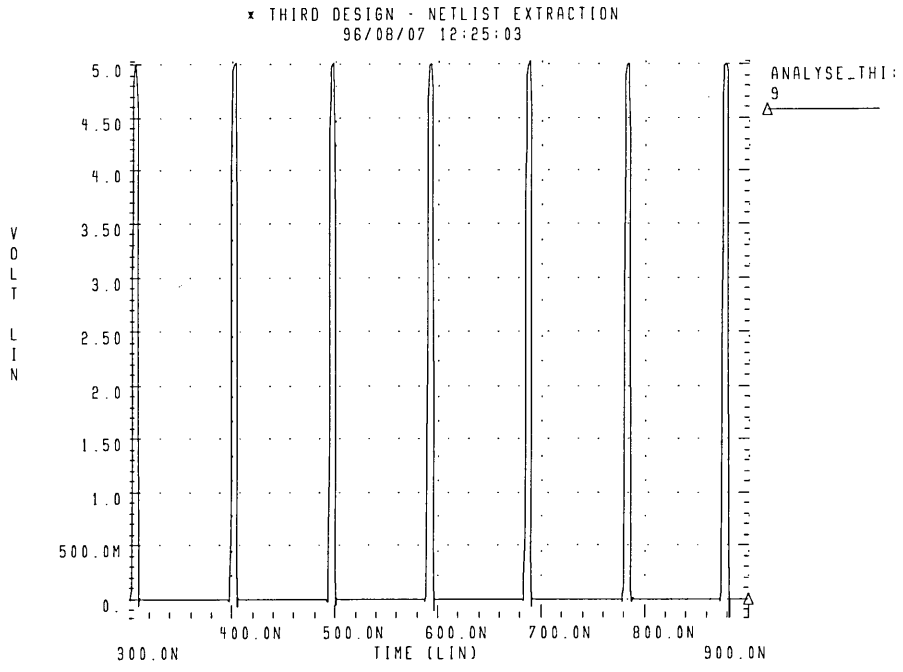

Figure 7.3: PFM pulse train for a constant DC input voltage

The transient analysis was repeated for different values of input voltage. A fast Fourier transformation (FFT) (using MATLAB) was carried out on the simulation results to determine the frequency spectrum of the resulting pulse train (Figure 7.4) and from this the frequency of oscillation. The total simulation time was 9 hours and 40 minutes on a HP712/60 workstation.

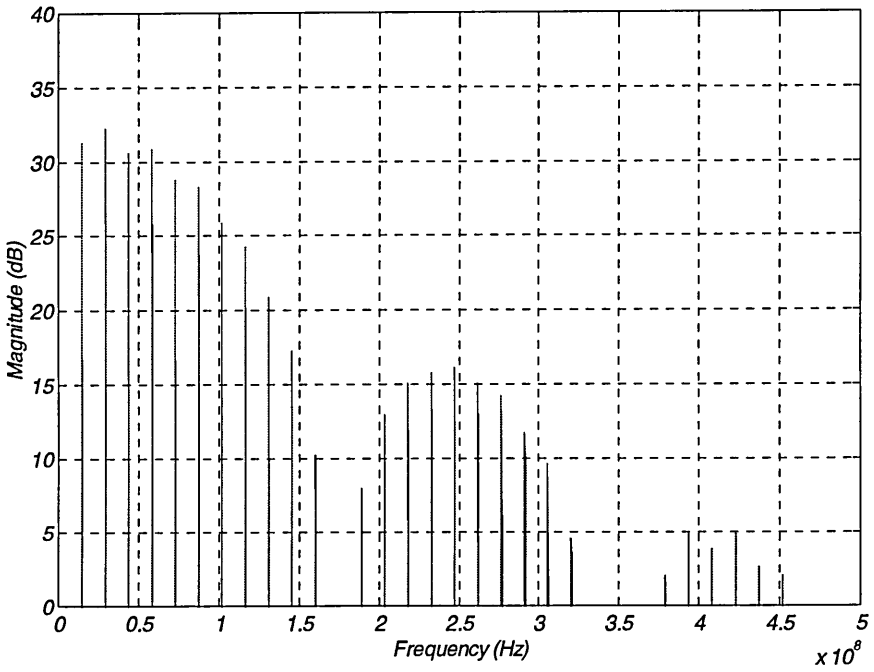

Figure 7.4: Frequency spectrum of unmodulated PFM pulse train (V_{in} = 2 V)

The results of this simulation were taken to generate the voltage to frequency transfer characteristic of the PFM modulator as displayed in Figure 7.5 with the dashed line indicating a linear voltage to frequency relationship for comparison. There is a usable operating range from about 2 V to 4.7 V. Assuming a 1 V modulating signal amplitude, this range can be divided into two regions, one centred around a DC offset voltage of 3 V and a second centred around 4 V corresponding to centre frequencies of 22.27 MHz

and 29.61 MHz, respectively (Figure 7.6). These regions are well suited for video transmission where low sampling ratio is a requirement for bandlimited systems.

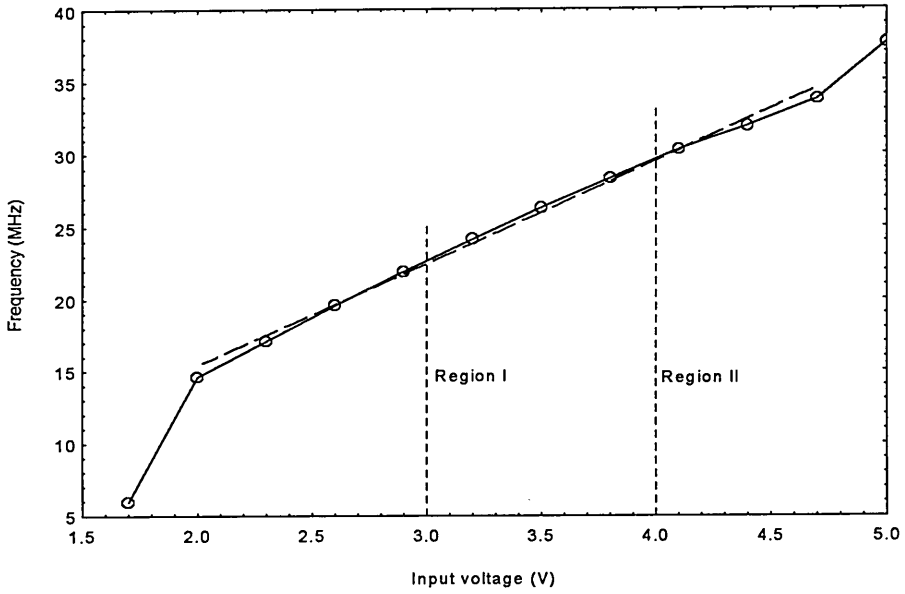

Figure 7.5: Simulated PFM modulator linearity test

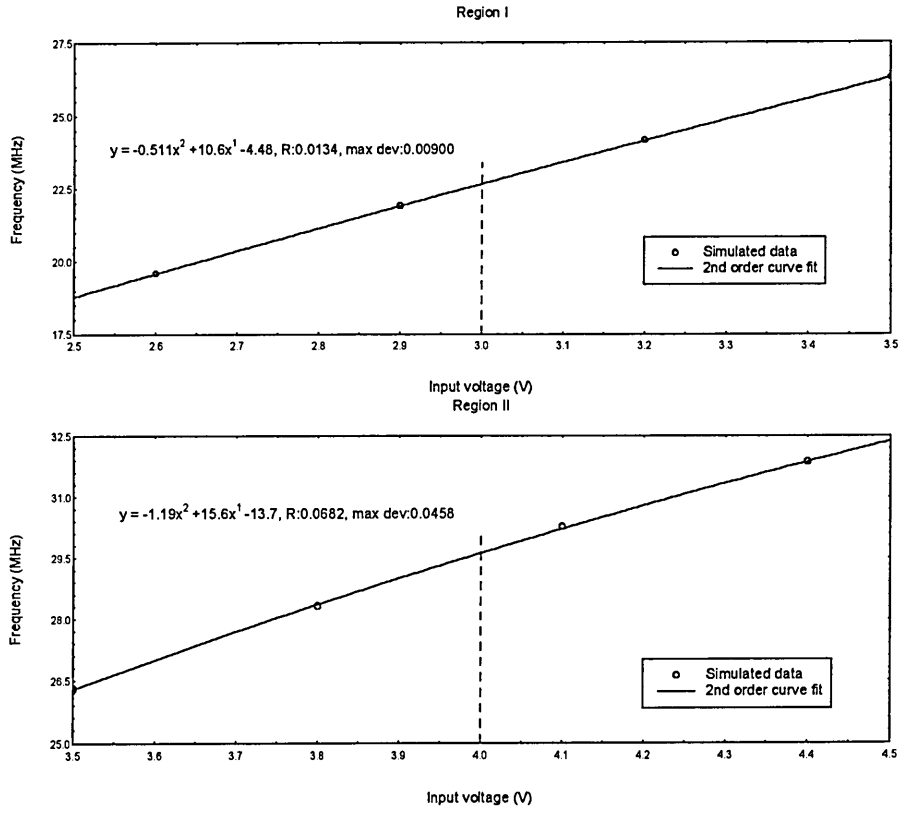

Figure 7.6: Expanded regions of operation

A polynomial curve fit has been carried out for both regions to determine the 2nd harmonic distortion levels. The simulation data for both regions were analysed further to obtain frequency deviation, resulting modulation index and sampling ratio. The results are listed in Table 7.1.

Table 7.1: Performance parameters for the two selected regions

Performance parameter	**Region I**	**Region II**
Carrier frequency (MHz)	22.67	29.61
Frequency deviation for a signal amplitude of 1 V (MHz)	7.5	6.18
Modulation index for a input signal amplitude of 1 V and a bandwidth of 6 MHz (TV)	1.25	1.03
2nd harmonic distortion (dB)	-34.57	-32.51
Sampling ratio (for a TV signal of 6 MHz)	~4	~5

Region one has a slightly better harmonic distortion level and a greater modulation index but at the expense of a lower carrier frequency which would result in a sampling ratio of ~4. Both regions have a 2nd harmonic distortion level which is greater than -40 dB but this may be reduced by reducing the modulating signal amplitude. As indicated in Figure 7.7, at signal amplitudes of less than 0.5 V, the 2nd harmonic distortion level drops below -40 dB.

Neither non-linear (Section 2.4.1) nor harmonic (Section 6.2.1) predicted distortion levels could be confirmed by simulation results because the resulting noise level from the FFT calculations was to high to make any quantitative measurements. In general,

the noise level was between 25 dB to 30 dB below the baseband information making it impossible to measure either 2nd harmonic or non-linear distortion levels.

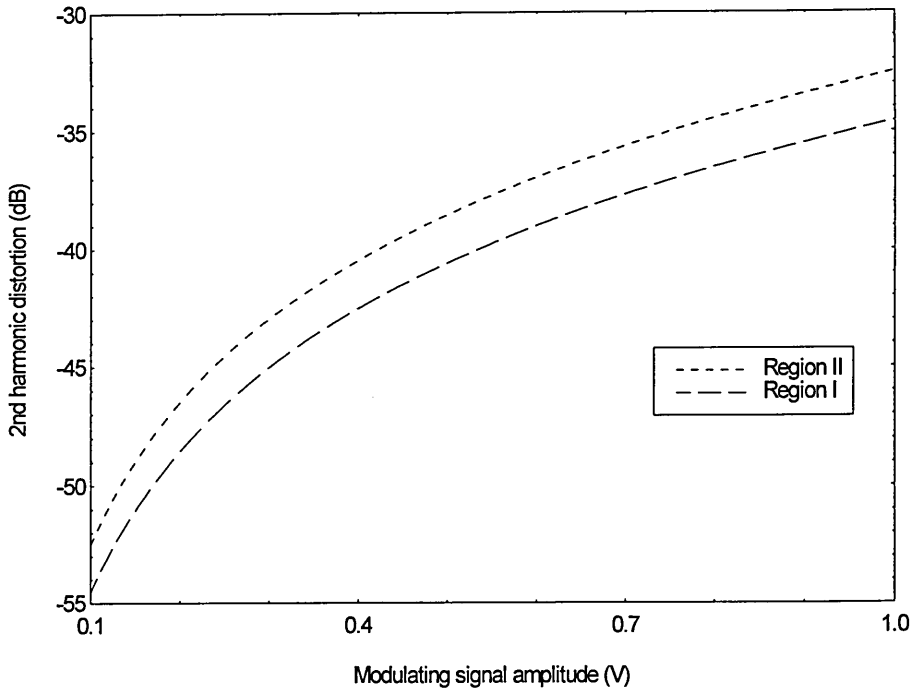

Figure 7.7: Predicted 2nd harmonic distortion levels as a function of signal amplitude

7.2 The Fabricated PFM Modulator Chip

The IC layout was submitted to EUROPRACTICE for fabrication and the packaged ICs were received 3 months later (Figure 7.8). In order to visualise the fabricated layout, scanning electron micrographs of the fabricated IC were taken. The PFM modulator chip layout is shown in Figure 7.9. Figure 7.10 shows part the PFM chip layout, the interdigitized differential pair. This photograph also shows the gate-source connected dummy transistors at either ends of the layout structure.

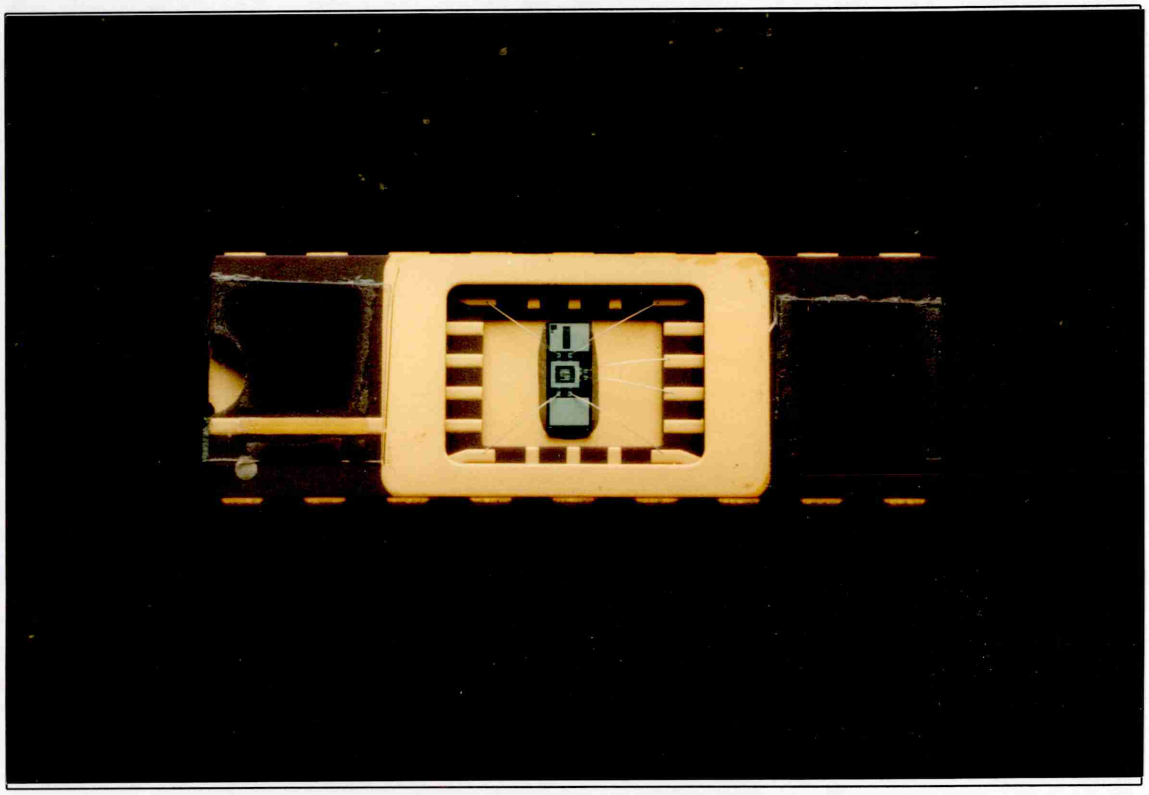

Figure 7.8: Photograph showing the bonding of the IC

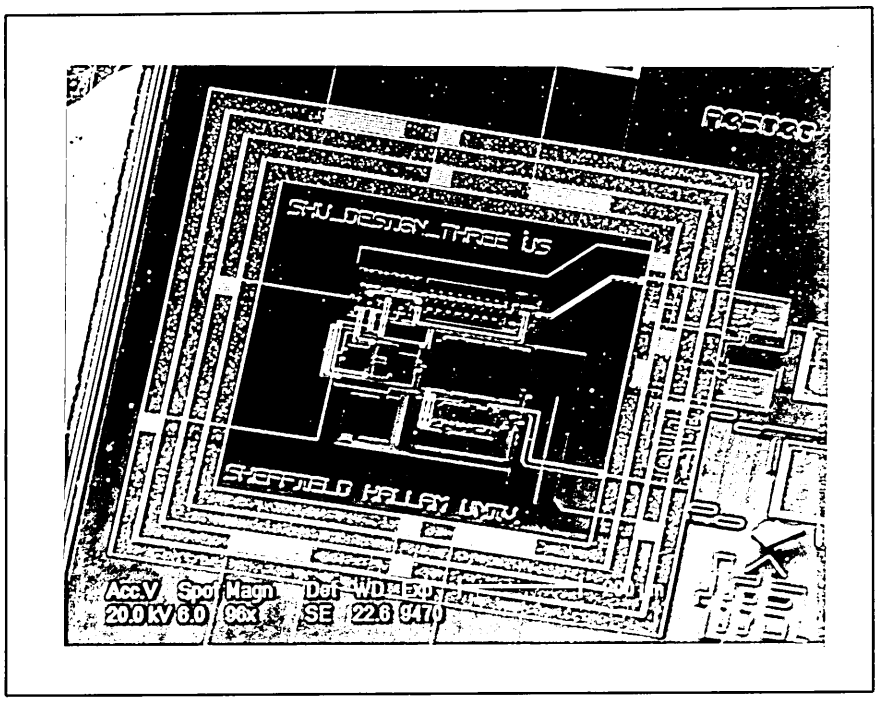

Figure 7.9: SEM photograph of PFM chip layout

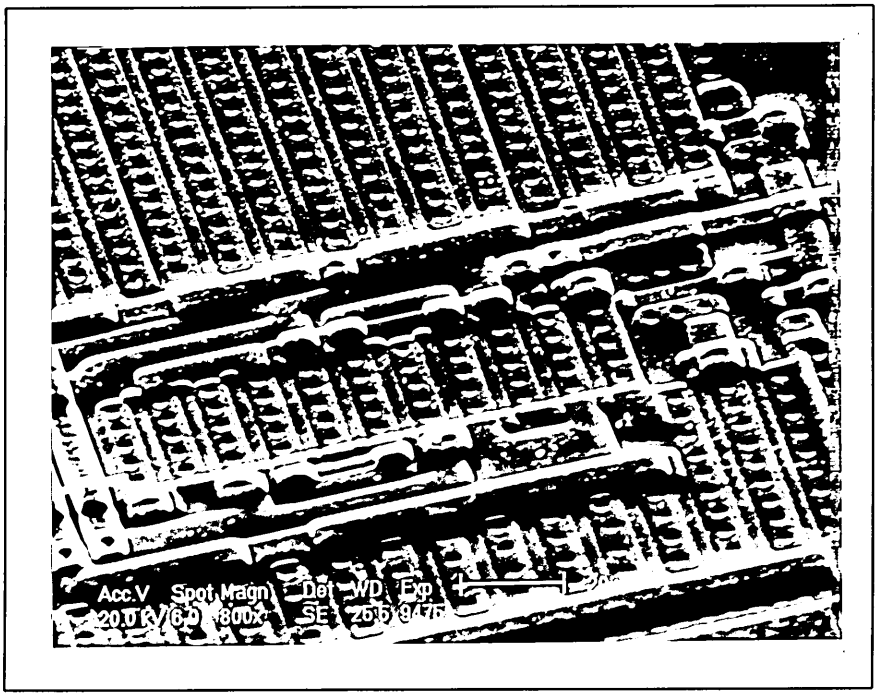

Figure 7.10: SEM photograph of interdigitized layout of differential pair

7.3 Measurements

Various measurements were carried out to determine the functionality and performance of the IC. These included time measurements to determine pulse width and quality of transmitted signal, spectral measurements to determine spectral overlap, harmonic distortion and linearity and qualitative measurements to determine the system performance for video transmission.

7.3.1 Measurement setup

In order to carry out system measurements the output signal of the PFM modulator was fed into a demodulator circuit consisting of a 7th order low pass Butterworth filter with a cut-off frequency of 5.5 MHz and a video amplifier. The input circuitry of the modulator consists of a coupling capacitance and a DC level shifter (Figure 7.11). The analogue and digital power supplies are separately decoupled.

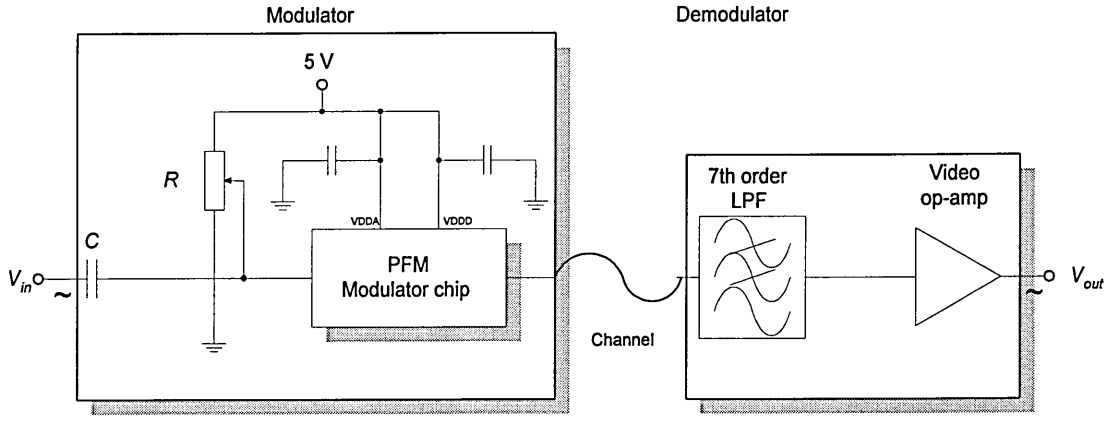

Figure 7.11: Measurement test circuit

The measurement setup is shown in Figure 7.12. Various configurations of measurement equipment were necessary to complete the required measurements.

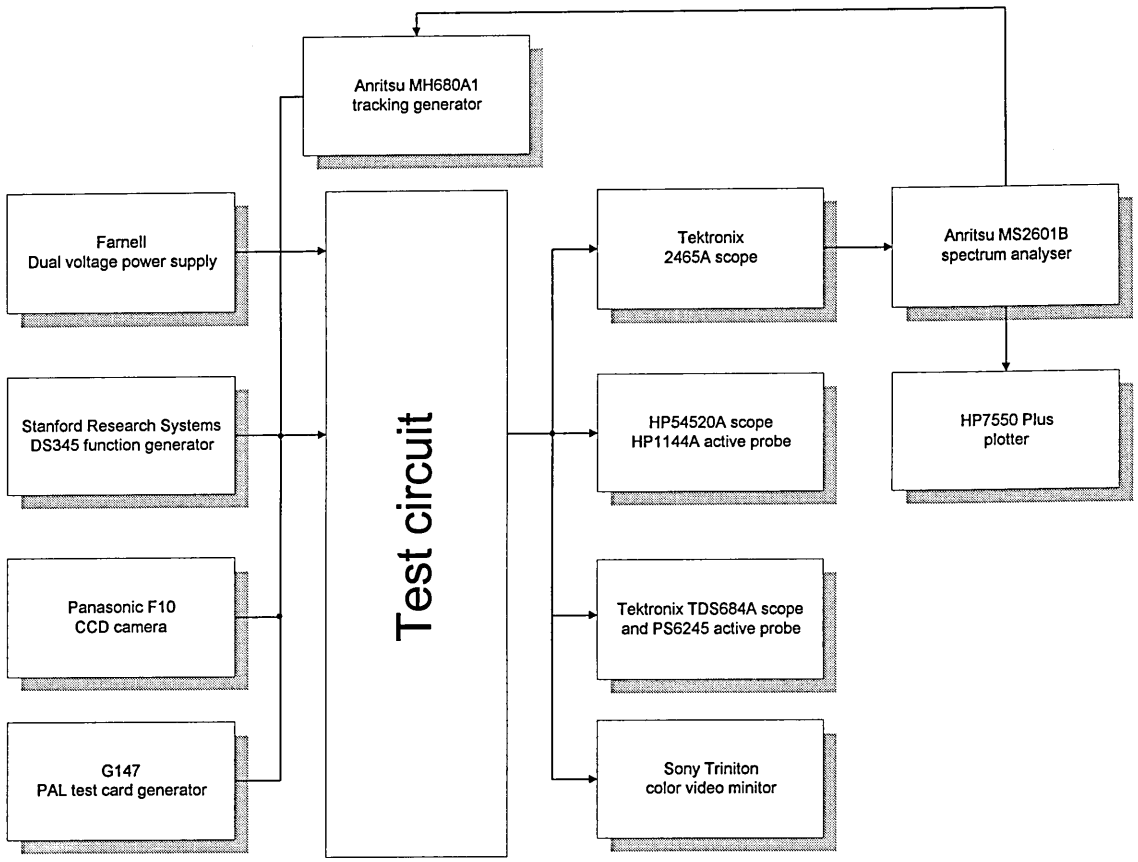

Figure 7.12: Measurement setup for PFM chip

7.3.2 Measurement of pulse width and linearity

Figure 7.13 shows the PFM pulse train of 24 MHz for an input voltage of 3 V. The pulse width was measured to be 5.72 ns which was in close agreement with the simulated value of 5.62 ns. The rise and fall times were measured to be 2.6 ns and 2.3 ns, respectively. The frequency spectrum of the unmodulated PFM pulse train is displayed in Figure 7.14. The pulse width was measured to be constant to within 80 ps over the entire modulating range.

An explanation of the abbreviations used for this and the following spectrum plots is given in Table 7.2.

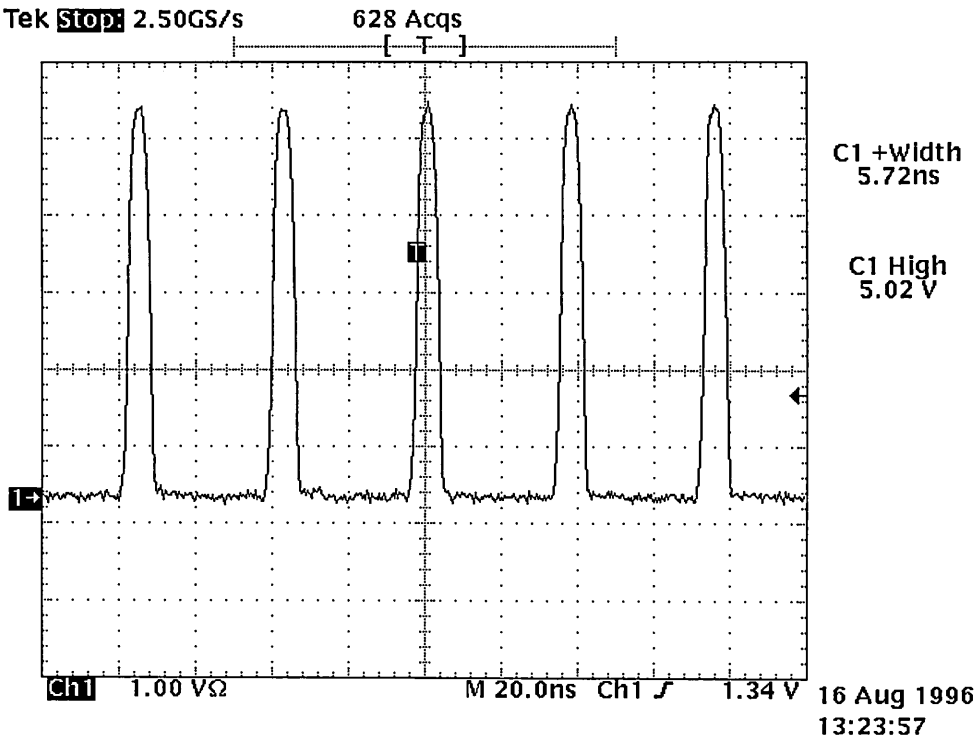

Figure 7.13: Oscilloscope picture of PFM signal

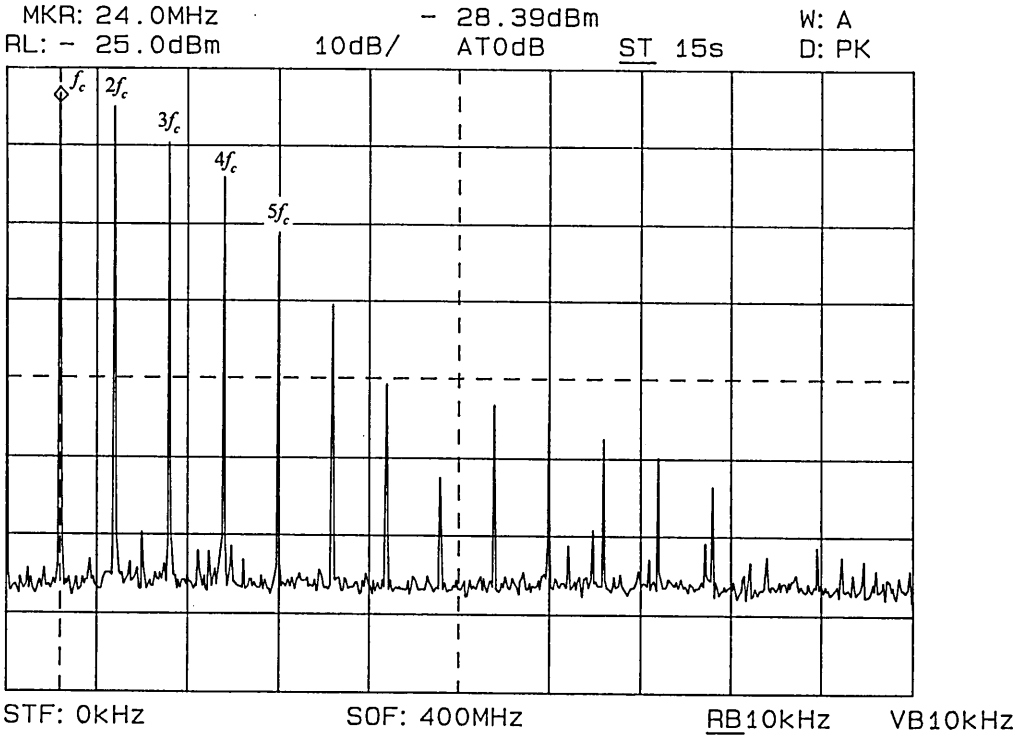

Figure 7.14: Unmodulated PFM spectrum (V_{in} = 3 V)

Table 7.2: Index to frequency spectrum plots

Abbreviation	Meaning
MKR	Marker
RL	Reference level
AT	Attenuation
ST	Sweep time
CNF	Centre frequency
SPF	Frequency span
STF	Start frequency
SOF	Stop frequency
RB	Resolution bandwidth
VB	Video bandwidth

The linearity was measured by varying the input voltage and measuring the frequency of oscillation (Figure 7.14). The minimum input voltage required to start reliable oscillation was 2.25 V. The result of the linearity test is shown in Figure 7.15. The dashed line represents a linear transfer characteristic for comparison. Assuming a modulating input signal with an amplitude of 1 V the two regions of operation as predicted from simulation results can be identified, one with a DC offset of 3 V and a second with a DC offset of 4 V (Figure 7.16). A DC offset of 3 V results in a carrier frequency of 24 MHz, thus fulfilling the requirement of a sampling ratio of at least 4 for a TV input signal of 6 MHz bandwidth. A DC offset of 4 V results in a carrier frequency of 32 MHz.

A polynomial curve fit was carried out for both regions to predict the 2nd harmonic distortion levels. Table 7.3 lists the achievable performance parameters determined from the linearity measurements.

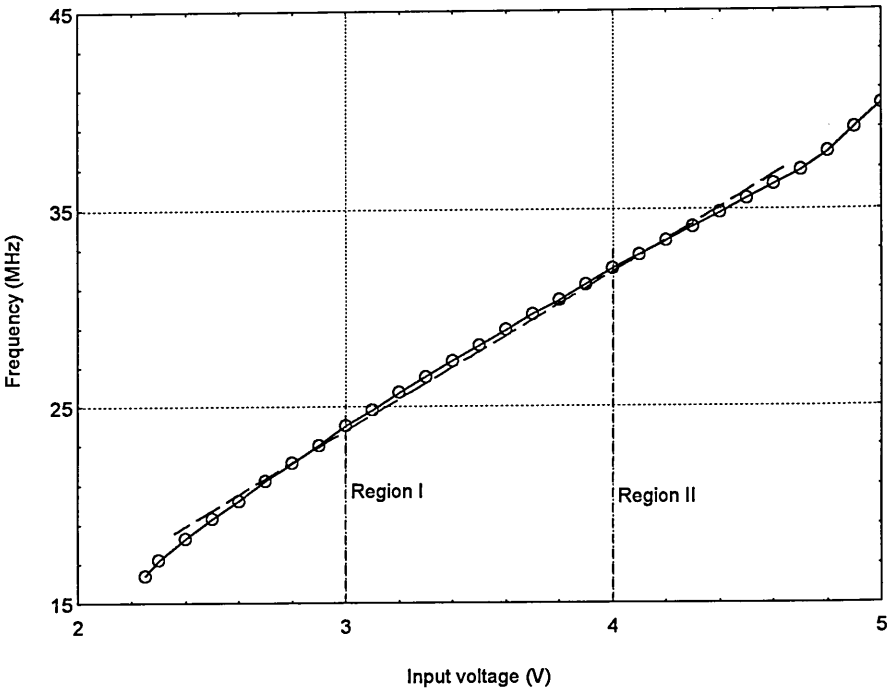

Figure 7.15: Linearity test of PFM modulator

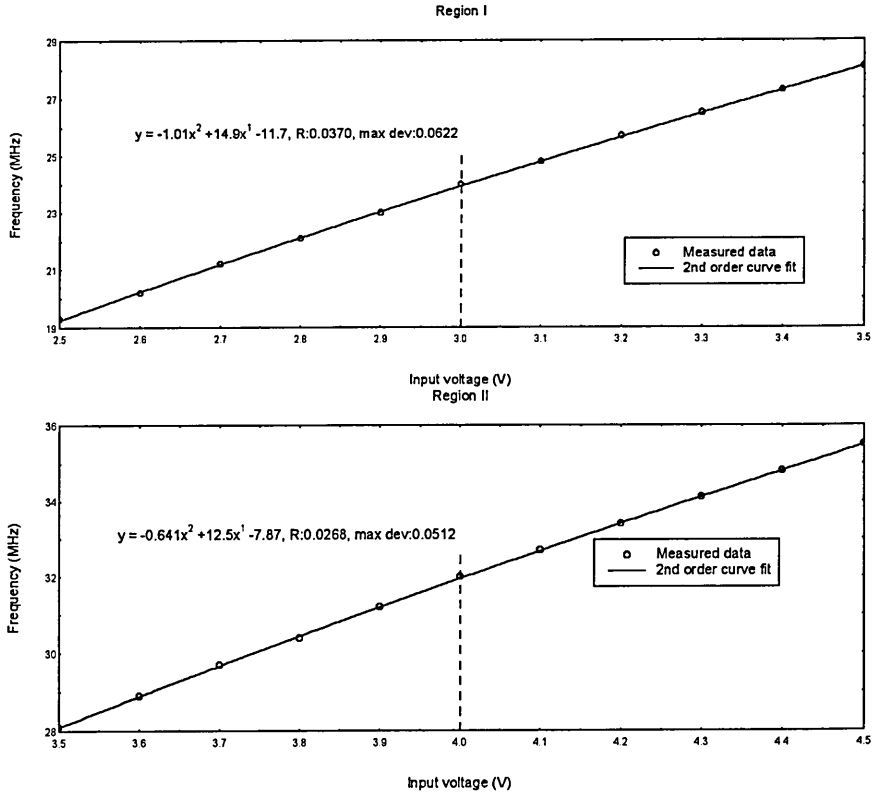

Figure 7.16: Regions of operation

Table 7.3: Performance parameters for the two selected regions

Performance parameter	**Region I**	**Region II**
Carrier frequency (MHz)	24	32
Frequency deviation for a signal amplitude of 1 V (MHz)	8.8	7.4
Modulation index for a input signal amplitude of 1 V and a bandwidth of 6 MHz (TV)	1.47	1.23
2nd harmonic distortion (dB)	-32.36	-34.81
Sampling ratio	4	5

The modulation index of 1.47 and 1.23 is adequate since most PFM systems are operated with a modulation index of about 1 [Wickramasinghe *et al.*, 1995]. The second harmonic distortion level for region II is slightly better than that for region I but it is higher than the required -40 dB. Lowering the input signal amplitude will result in a decrease of harmonic distortion (Figure 7.21).

Heatley [1982; 1984] reported optical video transmission systems based on PFM where the modulator operated at a carrier frequency of 30 MHz with a peak deviation of 7 MHz. These conditions are similar to the region II operating conditions.

Further measurements were carried out to determine the effect of supply voltage change upon the transfer characteristic. Figure 7.17 indicates that at a lower supply voltage, the frequency is shifted upwards and at a higher supply voltage, the frequency is shifted downwards. A 4% change in supply voltage results in a 5% - 6% change in frequency.

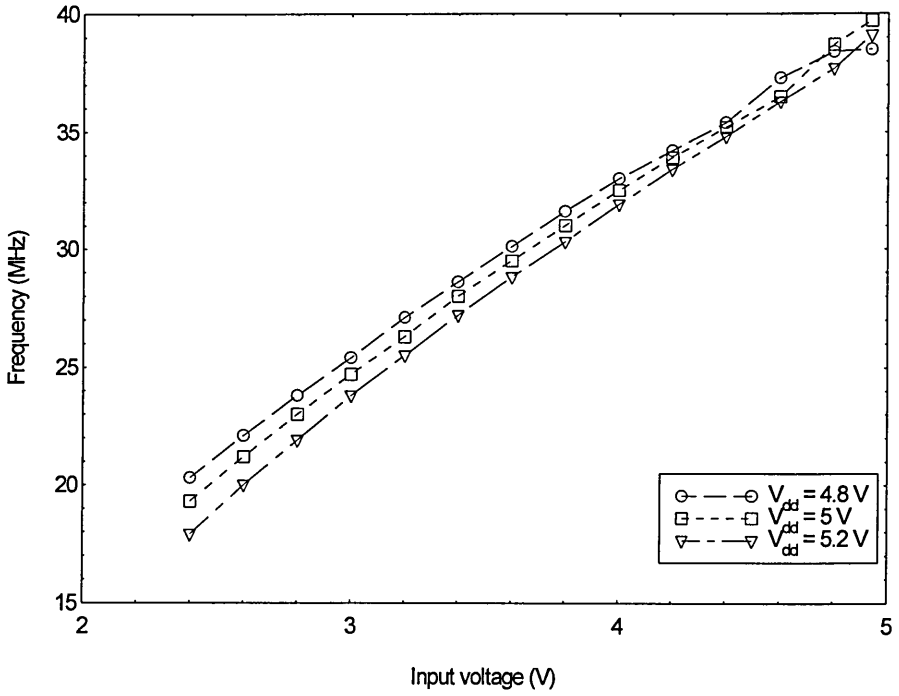

Figure 7.17: Effect of supply voltage change upon transfer characteristic

This change of oscillation frequency is due to the switching threshold being set by the threshold voltage (V_{th}) of a SR latch. The oscillation frequency (f) can be given as:

$$f = \frac{V_{in}}{2\,R\,C\,V_{th}} \tag{7.1}$$

where R the resistor of the current conveyor converting the input voltage V_{in} into a current and C the timing capacitance. Since a SR latch based on NAND gates is employed, the threshold voltage equation for NAND gates may be applied. V_{th} can, therefore, be related to the supply voltage (V_{DD}) as follows [Kang *et al.*, 1996]:

$$V_{th} = \frac{V_{T,n} + 2\sqrt{\frac{k_p}{k_n}}\left(V_{DD} - |V_{T,p}|\right)}{1 + 2\sqrt{\frac{k_p}{k_n}}} \tag{7.2}$$

where $V_{T,n}$ and $V_{T,p}$ are the NMOST and PMOST threshold voltages, respectively and $k_{p,n} = (W/L)k'_{n,p}$ with $k'_{n,p}$ the NMOST and PMOST transconductance parameter. Equation (7.2) shows that V_{th} is dependent upon V_{DD}. It is therefore possible to calculate the change of oscillation with regard to the threshold and supply voltages as follows:

$$\frac{f_1(V_{DD1} = 5.0\,\mathrm{V})}{f_2(V_{DD2} = 4.8\,\mathrm{V})} = \frac{V_{th2}(V_{DD2} = 4.8\,\mathrm{V})}{V_{th1}(V_{DD1} = 5.0\,\mathrm{V})} \tag{7.3}$$

Substituting equation (7.2) into (7.3) results in:

$$\frac{f_1(V_{DD1} = 5.0\,\mathrm{V})}{f_2(V_{DD2} = 4.8\,\mathrm{V})} = \frac{V_{T,n} + 2\sqrt{\frac{k_p}{k_n}}\left(V_{DD2} - |V_{T,p}|\right)}{V_{T,n} + 2\sqrt{\frac{k_p}{k_n}}\left(V_{DD1} - |V_{T,p}|\right)} \tag{7.4}$$

Equation (7.4) allows now to calculate the frequency change due to supply voltage change. It should be noted that the change in threshold voltage can be seen as the major contributor to the frequency change but not the only one. The change in supply voltage will effect other parts of the circuit, too.

Employing equation (7.4) a change in frequency of 4.28% can be calculated resulting from a change in supply voltage of 4%. This is in close agreement with the observed 5%-6% change as illustrated in Figure 7.17.

A change in operating temperature will effect the frequency performance of the VCO. (Initial tests showed that the IC itself increases its temperature by ~3°C when operated at its highest oscillation frequency.) It is expected that the frequency will decrease with

increasing temperature since the mobility of electrons and holes are temperature dependent and decreases with increasing temperature [Laker *et al.*, 1994]. The mobility is contained in the MOSFET transconductance parameter (k') and its temperature dependence is modelled in SPICE as follows:

$$k'(T) = k'\left(\frac{T}{T_{nom}}\right)^{a} \tag{7.5}$$

where T is the temperature, T_{nom} is the nominal temperature at which the SPICE models were measured (SPICE parameter TNOM) and a is the field mobility temperature exponent (SPICE parameter BEX) and its value is usually -1.5 [Meta, 1992]. Equation (7.5) clearly indicates that with increasing temperature the value of the transconductance parameter is decreasing resulting in a lower transistor drain current. The reduction in drain current will result in decreased oscillation frequency. A temperature change will not only effect the transconductance parameter but also the transistor capacitances and resistors associated with the drain and source junctions. The timing capacitances are also effected by temperature change.

To determine the effect of temperature change upon the oscillation frequency, the transfer characteristic was measured at various temperatures. Figure 7.18 shows that the frequency decreases with increasing temperature. The bottom graph of Figure 7.18 indicates that this decrease is non-linear.

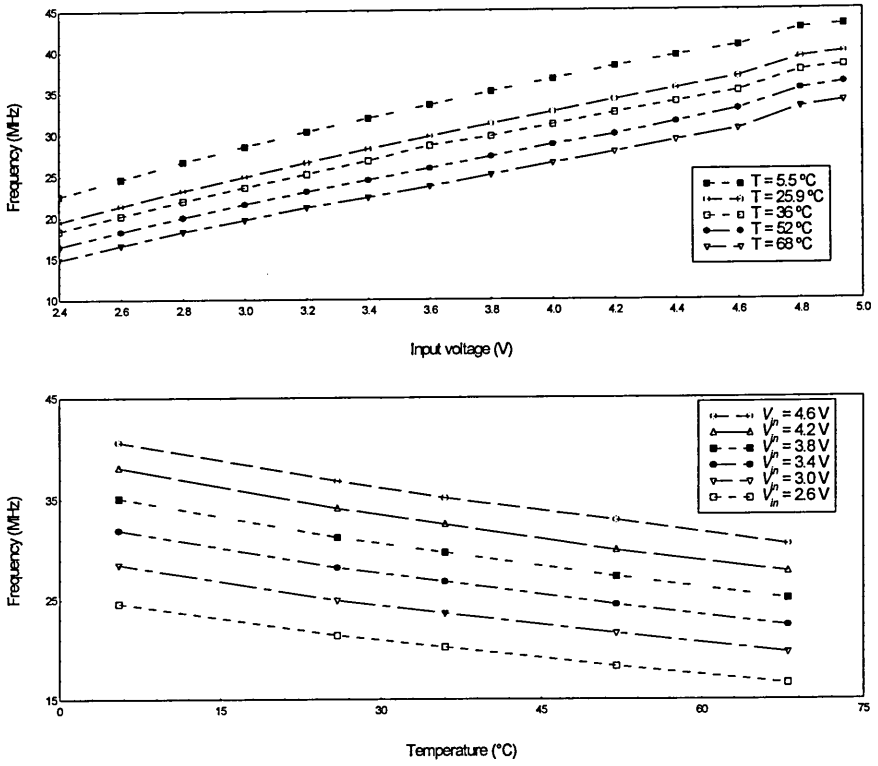

Figure 7.18: Results of temperature measurements

7.3.3 Harmonic and non-linear distortion measurements

Non-linear distortion will generate harmonics and increase the sidebands in the baseband region. The main source of this distortion will come from the non-linear frequency versus voltage performance of the VCO.

Harmonic distortion was measured by using an input signal of 1 MHz whose amplitude was changed from 1 V to 0.3 V in steps of -0.1 V. The resulting PFM pulse train was analysed using a spectrum analyser (Figure 7.19 and Figure 7.20). Figure 7.19 shows the spectrum of the modulated PFM pulse train. The carrier frequency (f_c), the second harmonic of the carrier frequency ($2f_c$) and their sidebands are indicated together with the baseband component (f_m) and its 2nd harmonic ($2f_m$).

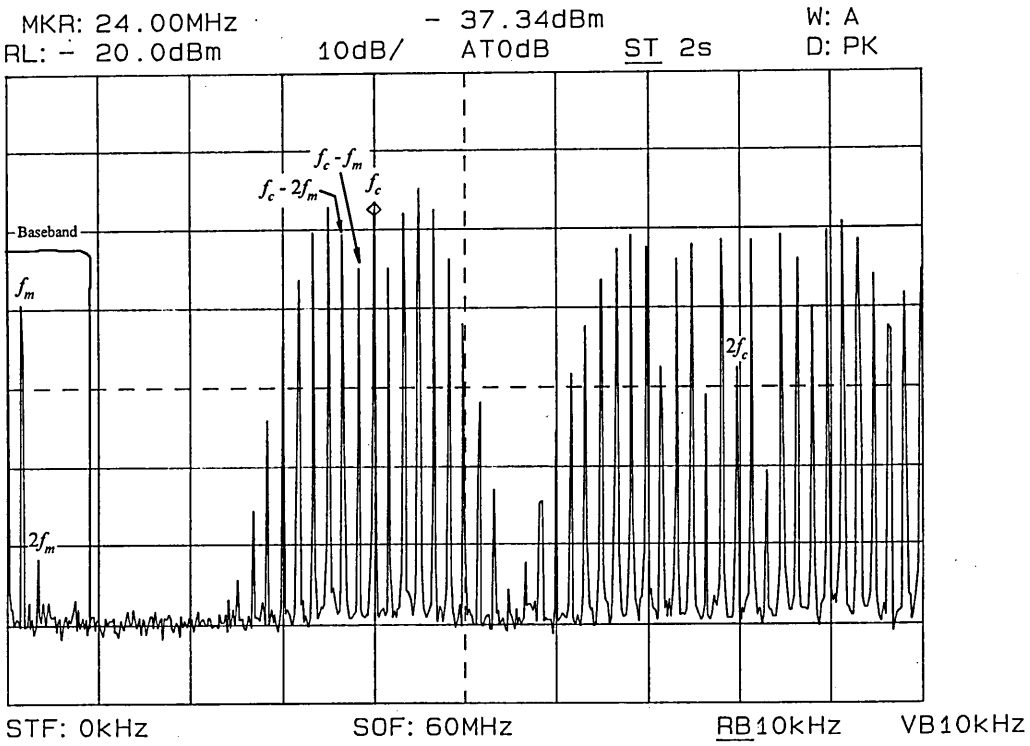

Figure 7.19: Modulated PFM spectrum (f_{in} = 1 MHz)

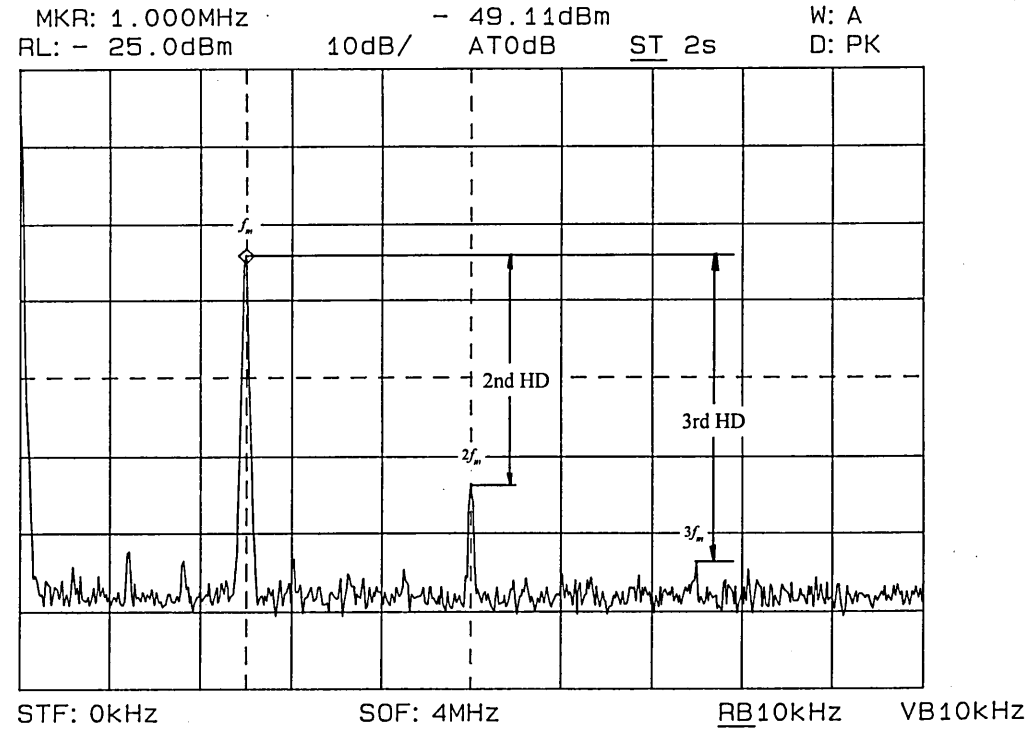

Figure 7.20: Typical frequency spectrum for harmonic distortion measurements

(f_{in} = 1 MHz)

Two sets of measurements for each region were taken. One set is from observations of harmonic distortion levels at the output of the PFM modulator while the other is from the entire system including the demodulator circuit. The results are shown in Figure 7.21 together with the predicted distortion levels as calculated from the measured transfer characteristic (Figure 7.16 and Table 7.3). For region I the measured 2nd harmonic distortion level at the output of the PFM modulator is much higher than the predicted level as calculated from the measured transfer characteristic. This may indicate that the transfer characteristic is not well represented by a polynomial curve fit. The system distortion level, measured at the demodulator output, is slightly lower than the modulator distortion alone (maximum difference is ~3.5 dB). This suggests that non-linearities in the demodulator may counteracting non-linearities in the modulator, thus increasing the overall system linearity.

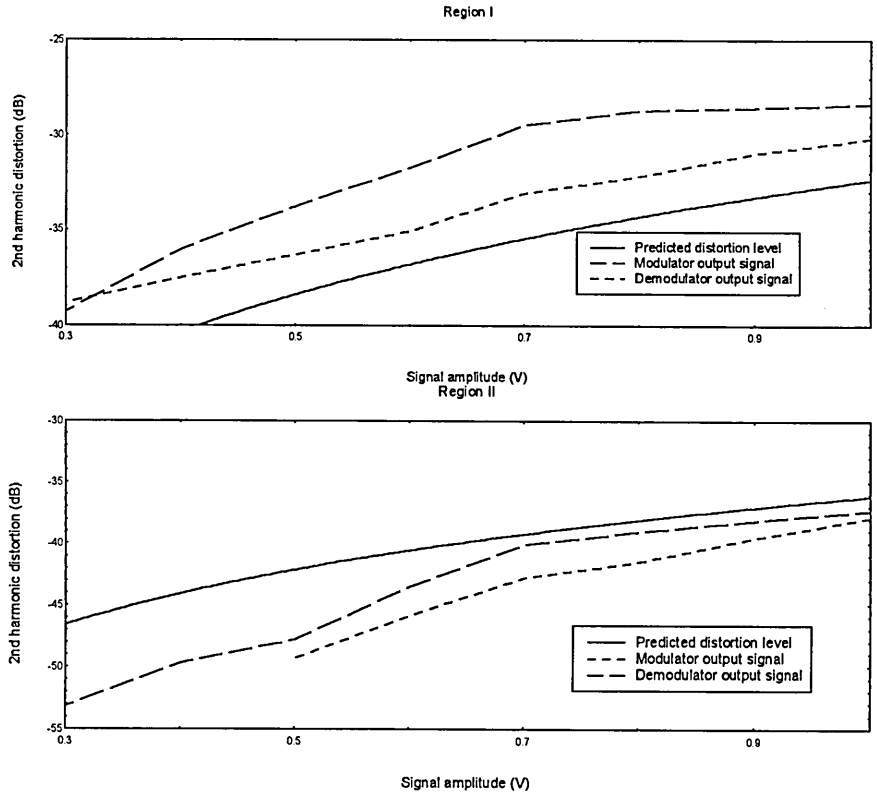

Figure 7.21: Measured 2nd harmonic distortion levels

In region II, PFM modulator output and system distortion levels were measured to within 2.5 dB. In this case the predicted distortion level as calculated from the measured transfer characteristic is in agreement with the measured values. Comparing regions I and II, it can be concluded that region II offers a much lower harmonic distortion and is therefore the preferred operating region.

The measured harmonic distortion level of -37.87 dB for region II is in close agreement with the value reported by Wilson *et al.* [1995] of at least -40 dB for a SWFM system where the centre frequency was set to 27 MHz.

Non-linear distortion results due to spectral overlap of the lower sidetones of the carrier fundamental with the baseband region (Figure 7.22).

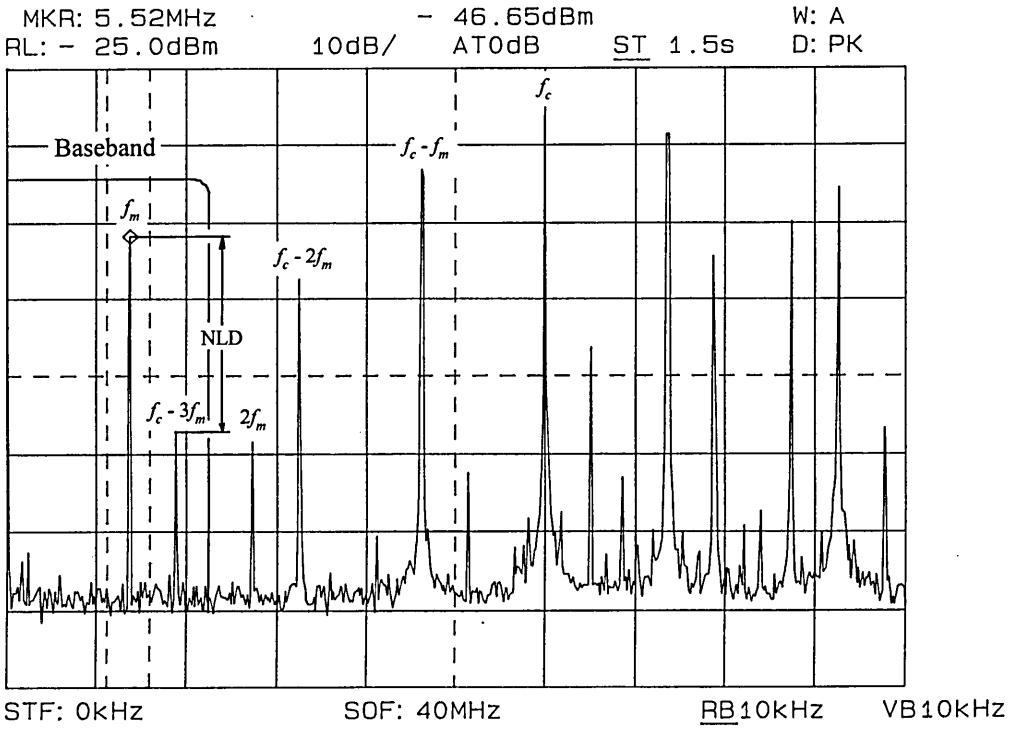

Figure 7.22: Frequency spectrum indicating NLD (f_{in} = 5.5 MHz)

This distortion may be measured with respect to sampling ratio and modulation index. In this case, the modulation index is linked to the modulating signal amplitude. A modulating signal frequency of 6 MHz whose amplitude was changed from 1 V to 0.4 V in steps of -0.1 V was applied to the input of the PFM modulator. By changing the DC offset, the carrier frequency was first set to 30.1 MHz (sampling ratio of 5). At this frequency the 4th side tone of the carrier fundamental overlaps with the baseband region. For a 1 V modulating signal amplitude, the NLD due to spectral overlap was measured to be -56 dB. Reducing the amplitude to 0.9 V resulted in an undetectable 4th sideband. The carrier frequency was therefore changed to 23.9 MHz (sampling ratio of 4) resulting in the values as shown in Figure 7.23 where, for example, a NLD of -40 dB can be achieved at a signal amplitude of 0.6 V.

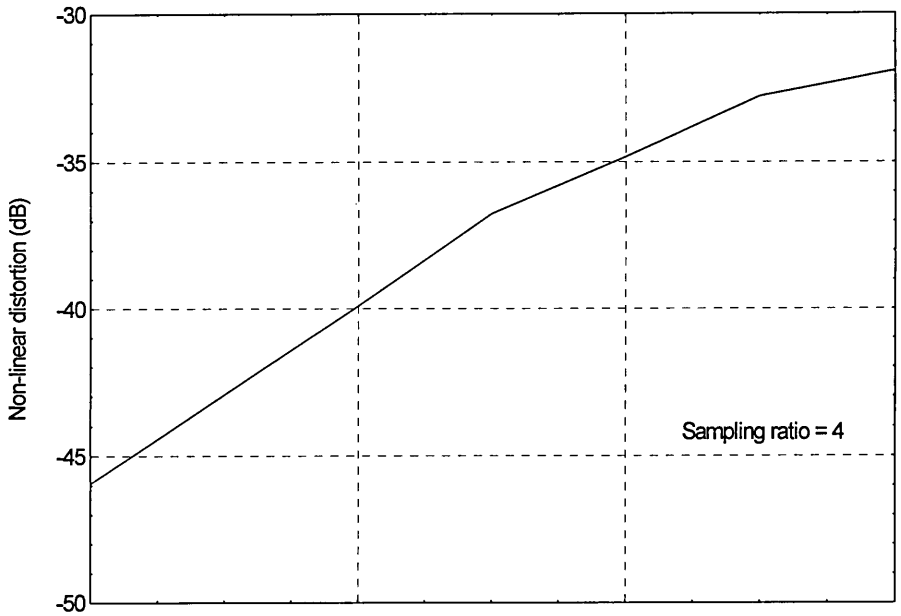

Figure 7.23: Non-linear distortion versus modulating signal amplitude

7.3.4 Qualitative and quantitative measurements of linearity

These measurement were carried out to obtain a qualitative impression of the linearity for the entire system including modulator and demodulator circuit. For this purpose, a triangular waveform with a frequency of 10 kHz was applied to the input of the modulator. This signal was compared with the output signal of the demodulator. The captured waveforms from the oscilloscope screen are shown in Figure 7.24. The upper waveform represents the input signal with the output signal shown in the lower half. It can be seen that the triangular waveform is fully recovered by the modulator indicating excellent linearity.

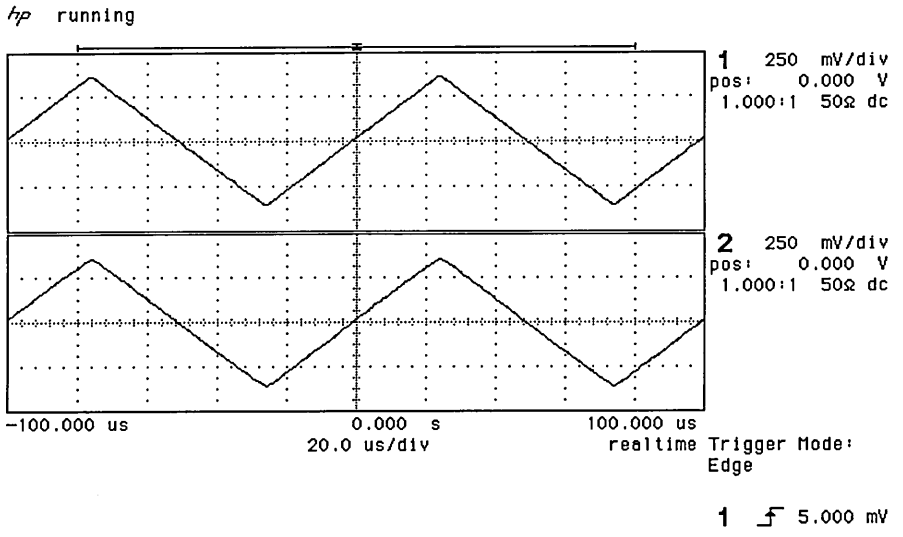

Figure 7.24: Oscilloscope screen capture of triangular waveform test

This test was repeated but this time with a square wave of 10 kHz as input signal. The captured waveforms from the oscilloscope screen are shown in Figure 7.25. Again, the upper waveform represents the input signal and the output signal is shown in the lower half. The figure shows that good signal recovery is achieved.

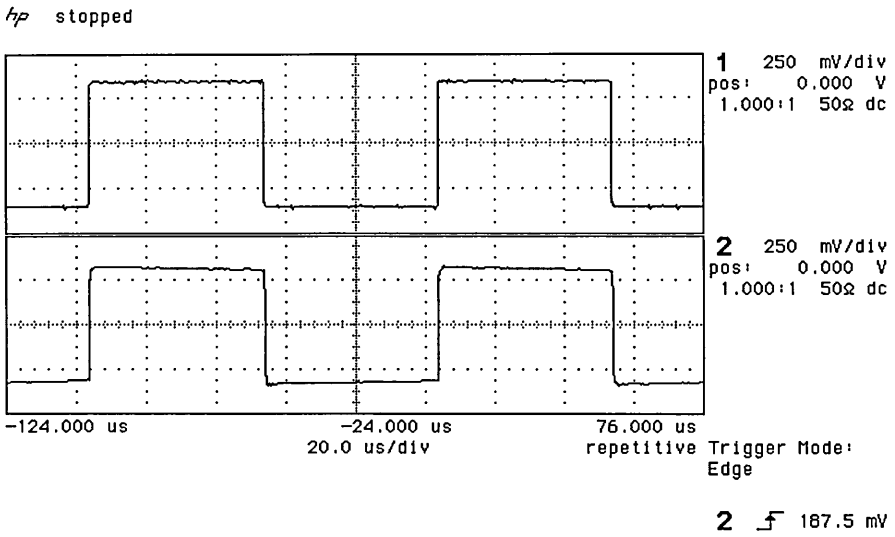

Figure 7.25: Oscilloscope screen capture of square wave test

A further set of measurements looked at a quantitative indication of non-linearity. A sine wave signal was applied to the input of the modulator and its amplitude varied. The output signal amplitude was then measured. The ratio of output to input amplitude was plotted against the input amplitude as shown in Figure 7.26. The maximum deviation between input and output signal amplitude was measured to be 2.61% and 1.67% for signal frequencies of 500 Hz and 100 kHz, respectively.

Another test was conducted to look at the frequency response of the entire system. For this purpose a tracking generator was connected to the input of the modulator and this supplied an input signal over the frequency range 0 to 15 MHz. The output response was captured with the spectrum analyser and is shown in Figure 7.27. The frequency response of the system was as expected with an almost flat response up to the cut-off frequency (-3 dB) of 5.5 MHz.

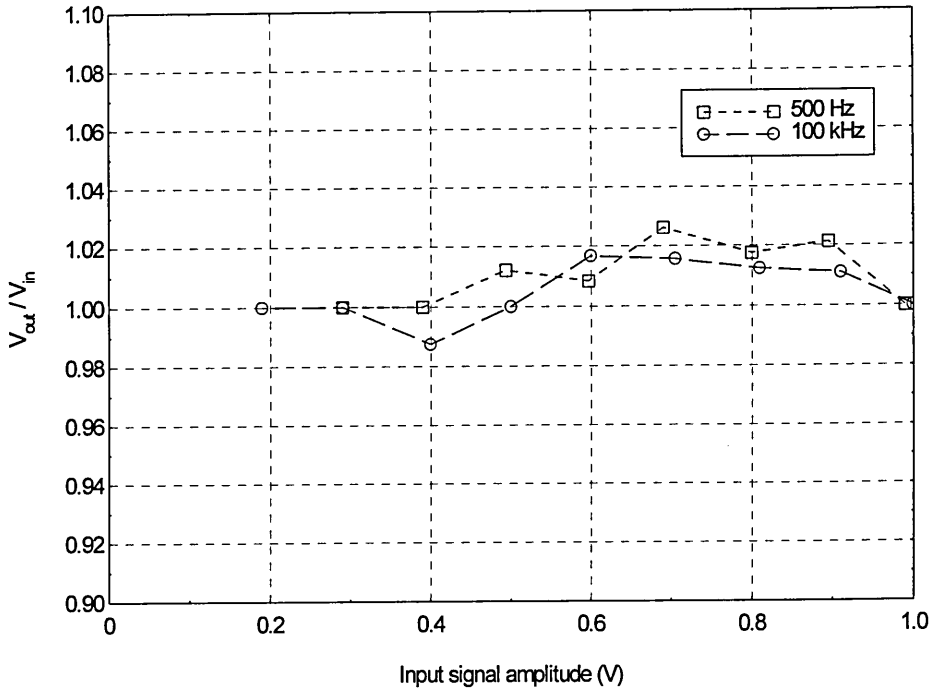

Figure 7.26: Ratio of output to input amplitude versus input amplitude

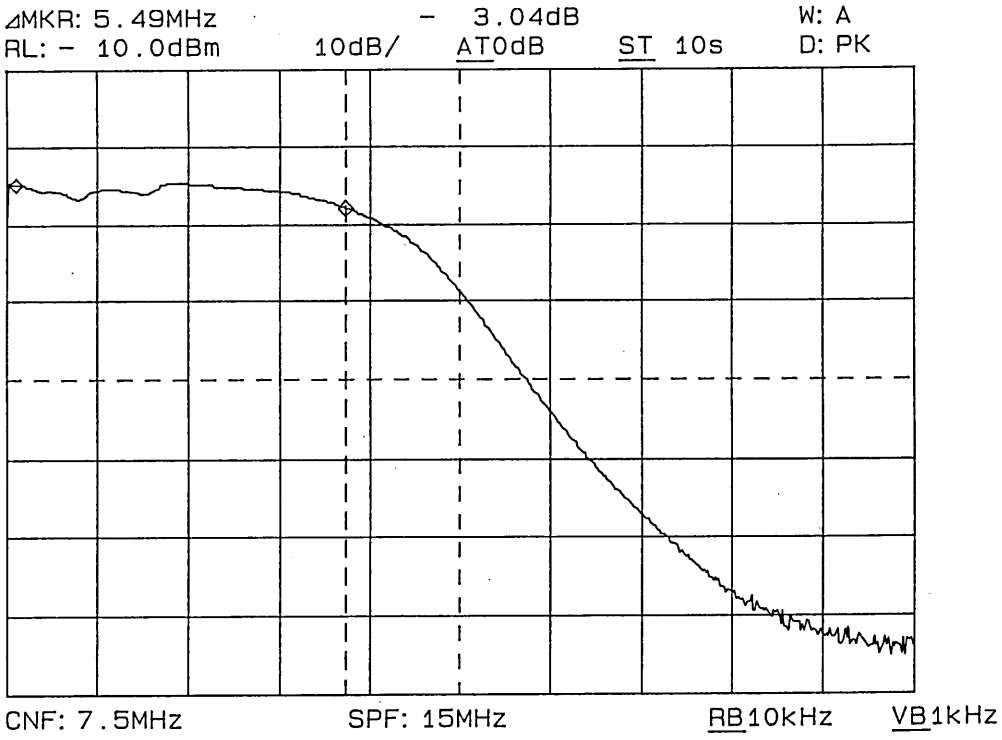

Figure 7.27: PFM system frequency response

7.3.5 Video transmission tests

The PFM modulator is designed for transmission of video signals. Tests were carried out by applying a video signal generated by a PAL test card generator to the input of the modulator. A single line of a received colour bar test card is shown in Figure 7.28. The colour burst and the typical colour bar steps can be identified. The distortion of the synchronisation pulse is attributable to the video amplifier of the demodulator since lowering the gain of this amplifier resulted in reduced distortion.

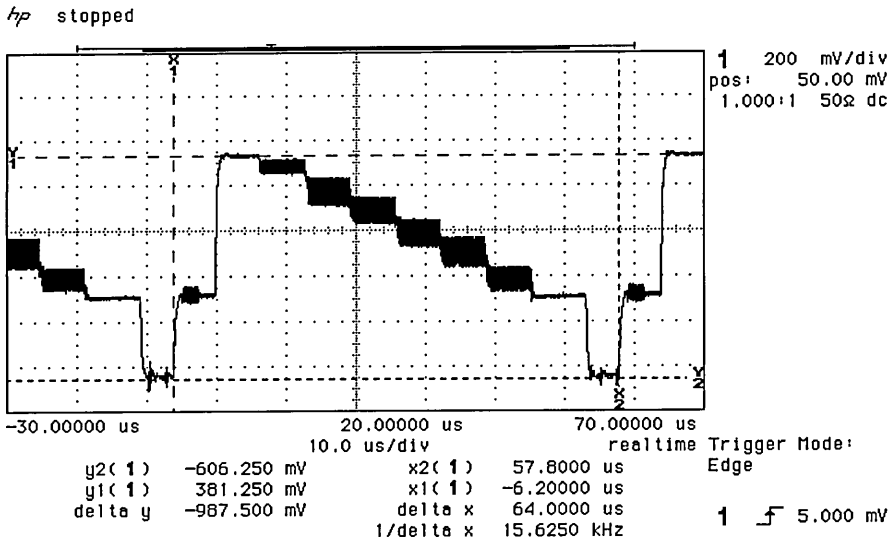

Figure 7.28: One line of a colour bar test card

Different test cards are shown in the following figures. Figure 7.29 shows the transmitted colour video test card generated with the PAL test card generator. This card is used as comparison for Figure 7.30 which shows the same card after modulation and demodulation. The distortions (shadowing) recognisable are attributable to the demodulator as indicated above. Figure 7.31 shows another test card as received indicating the performance of the entire video transmission system. These test cards indicate that the information is faithfully recovered by the demodulator.

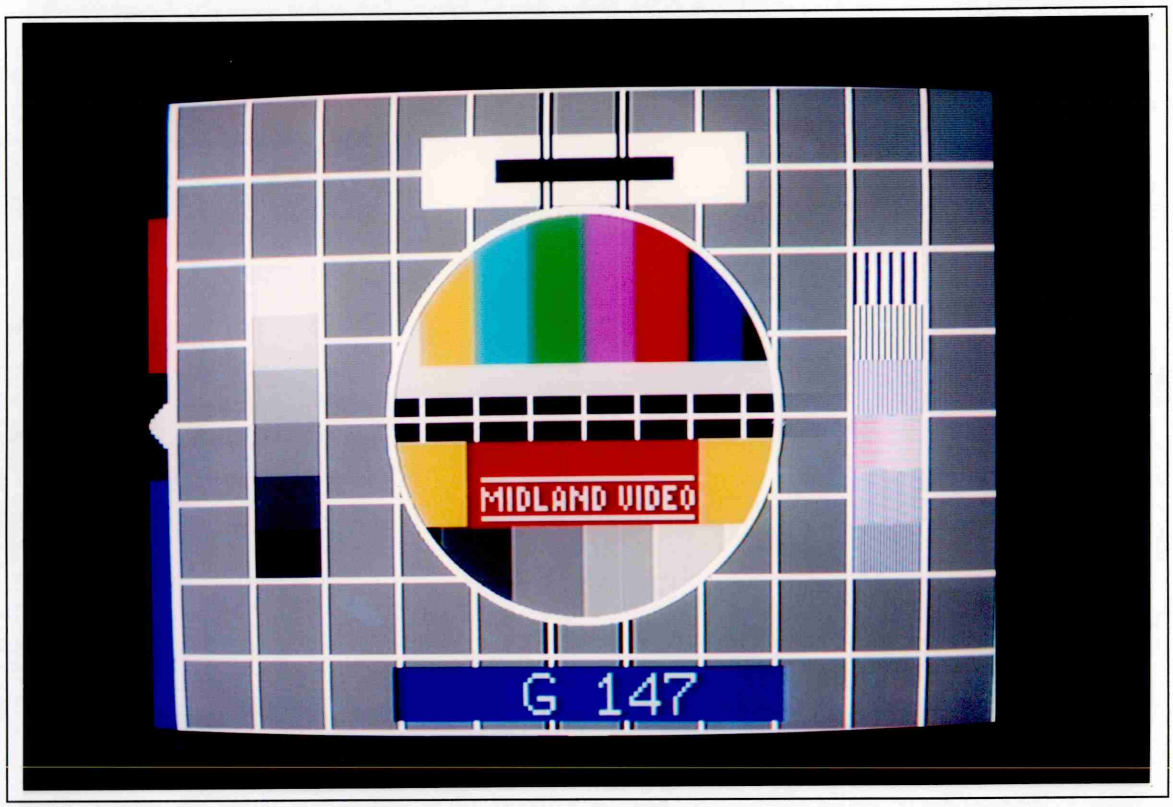

Figure 7.29: Transmitted video test card

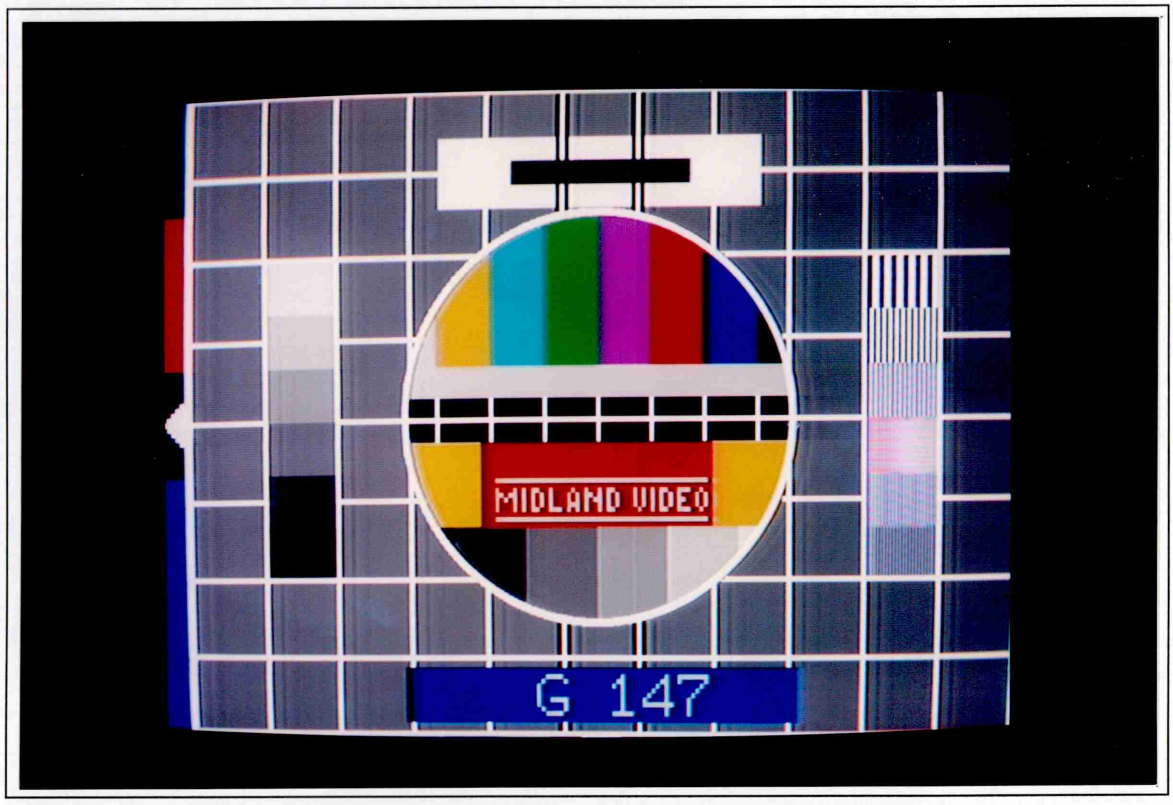

Figure 7.30: Received video test card

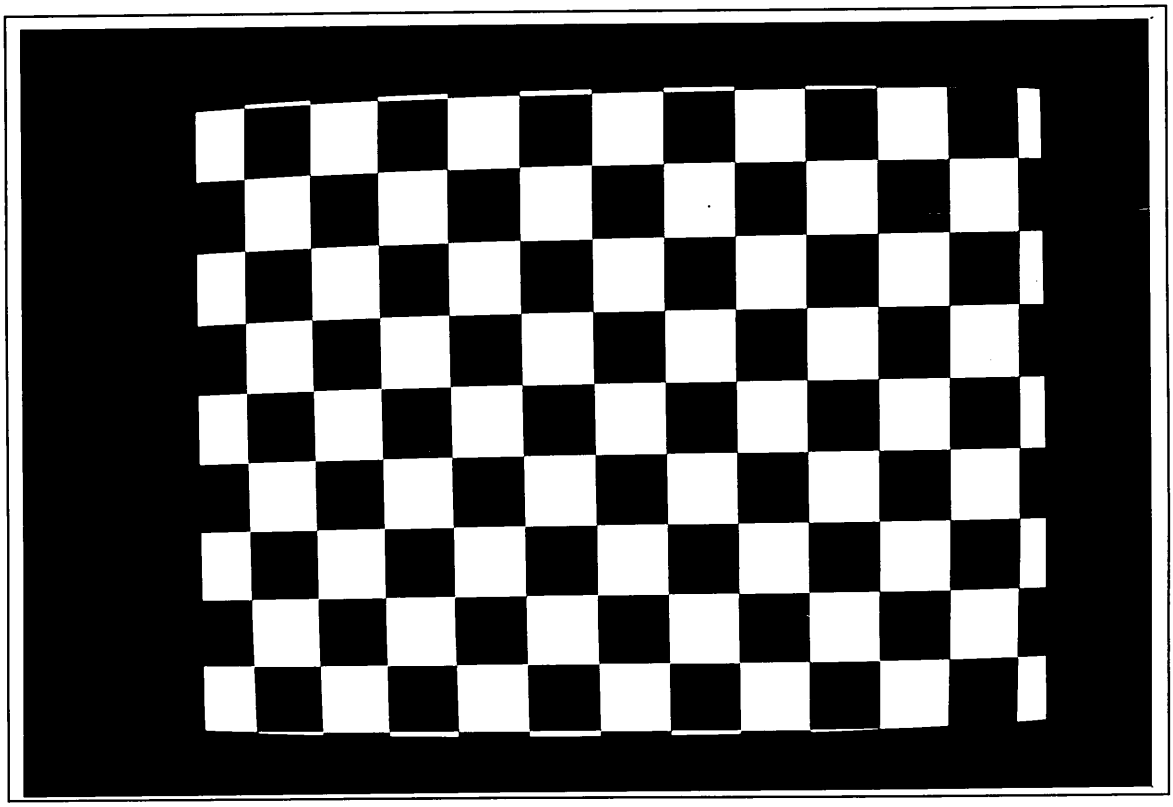

Figure 7.31: Received chequered test card

Since the PAL test card generator only allowed the testing of still picture transmission, it was replaced by a CCD camera in order to judge the quality of moving picture transmission. No problems could be observed with the picture quality. Picture synchronisation and reproduction was similar to the still picture transmission.

7.4 Comparison of Simulation and Measurement Results

The comparison between simulated and measured results is limited to the results obtained from HSPICE simulation since many more measurements were made than simulations. Figure 7.32 shows the comparison of transfer characteristics. In general, a good agreement can be found with the measured performance exceeding the simulated one. Furthermore, simulated results indicated that oscillation would start at around 1.5 V. This was proven to be wrong by the measurements which showed that oscillation did not start until an input voltage of 2.25 V was reached. The measurements also showed that the PFM modulator performs slightly better than expected at higher input voltages.

Performance parameters resulting from the linearity measurements were presented in Table 7.1 and Table 7.3 for simulation and measurements, respectively. Comparing the values in both tables it can be concluded that the fabricated PFM modulator slightly exceeds the performance as predicted by simulation results. The harmonic distortion as given by simulation results can also be compared to practical measurements. Since no entire PFM modulator/demodulator system simulation was carried out, only the

measured harmonic distortion levels at the output of the PFM modulator are compared with the predicted values as calculated from the simulated transfer characteristic (Figure 7.33).

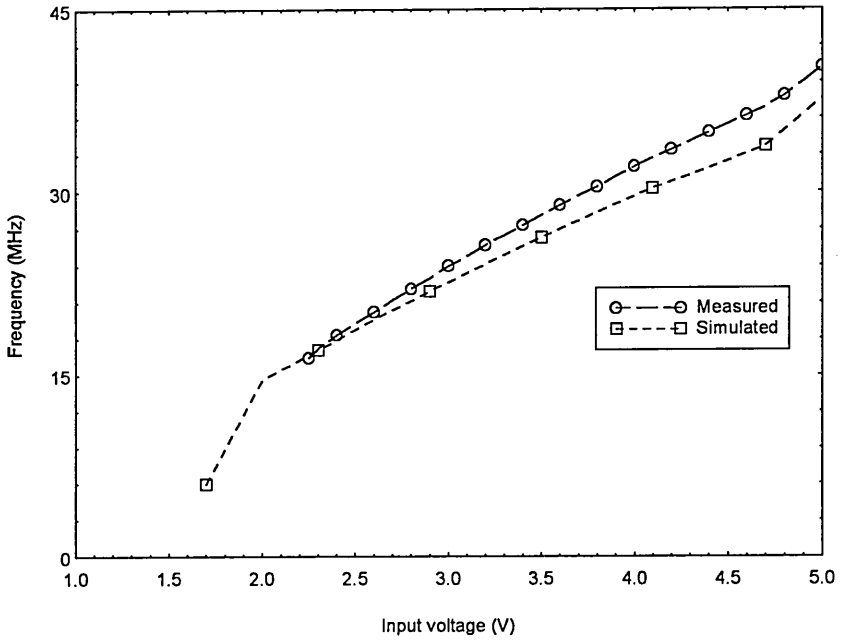

Figure 7.32: Linearity comparison

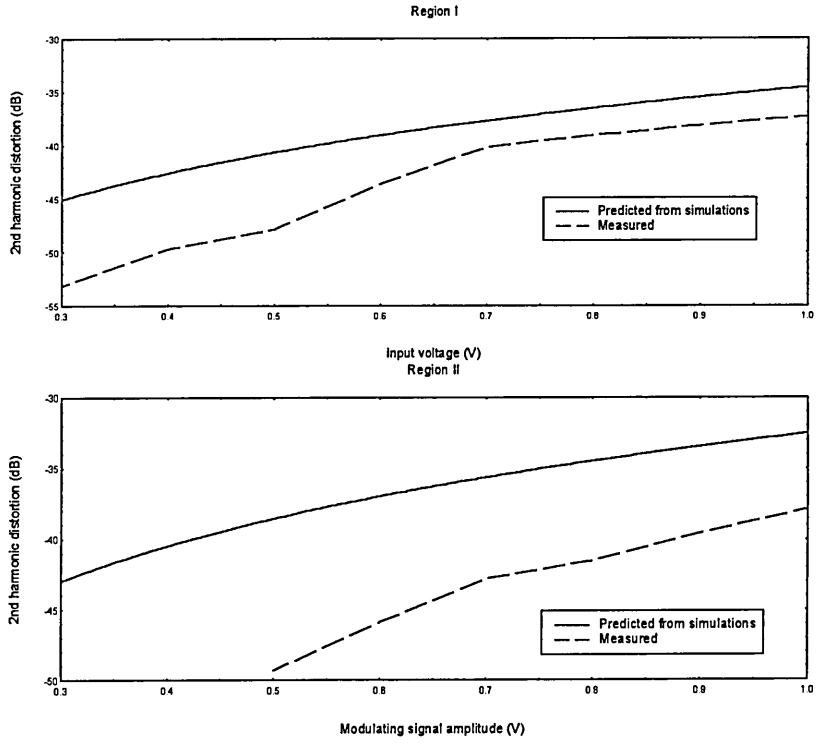

Figure 7.33: Comparison of predicted and measured harmonic distortion

In region I, a good agreement is found while in region II the predicted values deviated from the measured values. This indicates, that the simulation does not accurately model the behaviour of the PFM modulator at higher frequencies. This was also underlined by comparing simulated and measured transfer characteristics (Figure 7.32) and could be explained by process variations or slightly inaccurate SPICE models. The PMOST transconductance parameter value for narrow channel devices for instance, was 13% higher than the value used for simulations (NMOST 4% higher). This would result in an increased drain current for PMOST devices which could explain the difference in simulated and measured values. In addition, process variations could cause the thin oxide poly1-poly2 capacitance value per unit area to differ slightly from the modelled one resulting in a slightly changed frequency of oscillation.

All the differences between simulated and measured values are small (10% - 15% or less) taking into account process variations and measurement tolerances. Furthermore, comparisons between simulations and measurements indicated that the SPICE model parameters are conservative and in general the performance of the fabricated circuit exceeds that predicted by simulation.

7.5 Advantages of the Designed PFM Modulator

To the best knowledge of the author, this circuit represents the first fully integrated PFM modulator. Conventional PFM modulators are implemented using a commercially available VCO followed by digital circuitry to form the required pulse width. Several VCO ICs are commercially available such as the SN74S124 (TTL family) of Texas

Instruments or the SP1658 (ECL family) of Plessey Semiconductors. Both VCOs need external components to set the carrier frequency. Linearity measurements of the SP1658 were available for comparison with the designed PFM modulator. Figure 7.34 shows part of the transfer characteristic together with a polynomial curve fit to determine the 2nd harmonic distortion level. This part of the transfer curve was chosen in such a way that the centre frequency is equal to the region II centre frequency of the modulator. It can be seen that the modulating range is greater than the one of the designed circuit. In order to allow for a good comparison, the input voltage range of the SP1658 will be limited, so that a frequency deviation equal to that of region II, in Table 7.3, can be achieved.

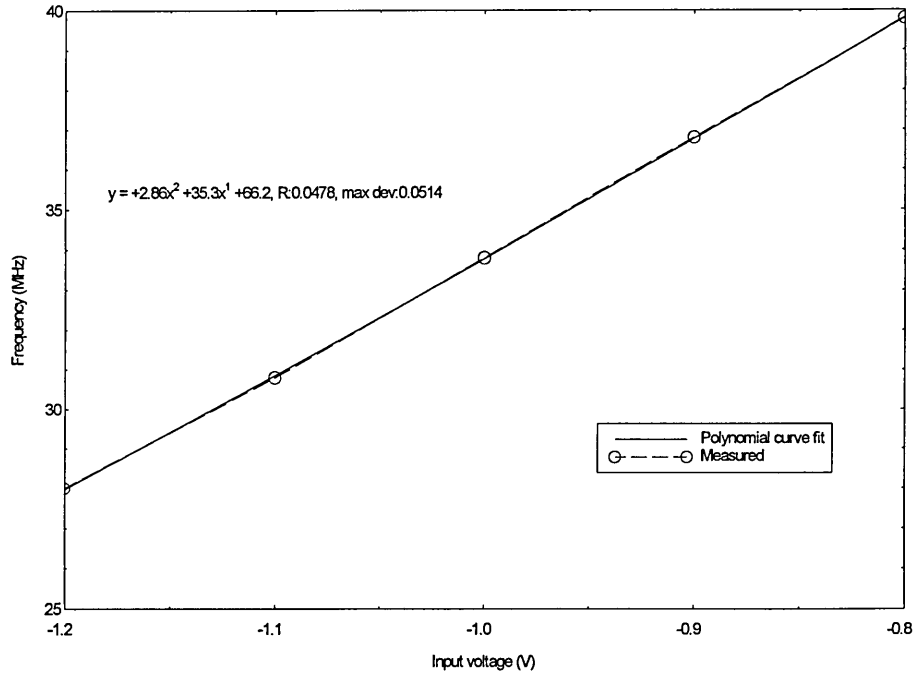

Figure 7.34: Linearity test of SP1658

A performance comparison between the designed PFM modulator and the SP1658 is summarised in Table 7.4. The difference in input voltage range (ΔV_{in}) was necessary in

order to obtain the same frequency deviation. This table shows that the designed circuit has a similar performance to commercially available devices. It should be noted that the comparison is between the entire PFM modulator and a voltage controlled oscillator alone, which is only part of the modulator design.

Table 7.4: Performance comparison

Performance parameter	**Designed circuit**	**SP1658**
Carrier frequency (MHz)	32	33.8
Frequency deviation (MHz)	7.4 (at $\Delta V_{in} = 1$ V)	7.4 (at $\Delta V_{in} = 0.24$ V)
2nd harmonic distortion (dB)	-37.87 (at $V_A = 1$ V)	-41.56 (at $V_A = 0.24$ V)

A further comparison has been carried out with regard to power consumption. It is expected that the designed circuit requires much less power to operate since it is a CMOS design while the SN74S124 and the SP1658 are both bipolar designs. Table 7.5 shows a comparison between the three ICs. As expected, the CMOS design required considerably less power than either of the other two ICs. In addition, because of the high power dissipation the SN74S124 even requires a heatsink.

Table 7.5: Power consumption comparison

	Designed IC (at $f = 40$ MHz)	SP1658	SN74S124
Voltage (V)	**5**	-5.2	5
Current (mA)	**~9.5**	~32	~105
Power (mW)	**~47.5**	~165	~525

A further advantage of the CMOS PFM modulator is its simplicity of use since only a coupling capacitance and a potentiometer are required externally. The use of this device would also increase the reliability of a modulator system due to fewer components and interconnections.

7.6 PFM Modulator Specifications

- Single chip PFM modulator for video or TV signals
- No external components necessary to set operating carrier frequency
- Separate analogue and digital voltage supply
- Low power consumption (~ 48 mW)
- Frequency range from 17 MHz to 40 MHz

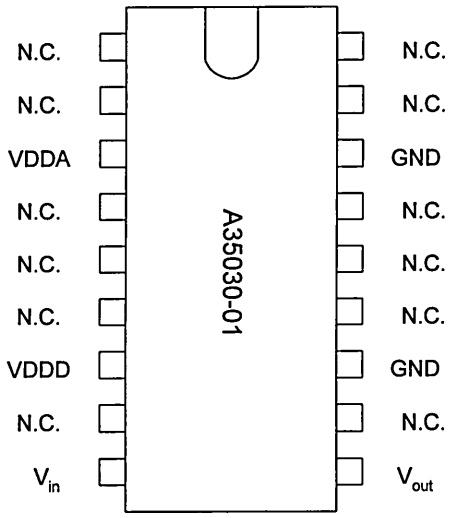

Figure 7.35: Pin diagram of modulator

Table 7.6: Recommended operating conditions

Supply voltage (V)	5
Supply current (mA)	9.5
Input voltage range (V)	2.25 - 5
Frequency range (MHz)	17 - 40
Carrier frequency (MHz)	24 (±560 kHz) *at* $V_{off} = 3\ V$
	32 (±1.04 MHz) *at* $V_{off} = 4\ V$

Table 7.7: Electrical output characteristics [Das, 1990]

Sink capability (mA)	3.2 at 0.4 V
Source capability (mA)	1.6 at 4.6 V
Short circuit current:	
o/p shorted to V_{dd} (mA)	70 (typ.)
o/p shorted to GND (mA)	40 (typ.)

Table 7.8: Output waveform description

Pulse width (ns)	5.72 (max. 6.43)
Rise time (ns)	2.6
Fall time (ns)	2.3
Duty cycle (%)	14 (at 24 MHz), 18 (at 32 MHz)
High output voltage (V)	5 (typ.)
Low output voltage (V)	0 (typ.)

7.7 Summary

This chapter described the final circuit implementation of the PFM modulator. Simulation results have been presented and analysed predicting the performance of the circuit with regard to transmission of video or TV signals and indicating that the circuit should fulfil the requirements of a quality video transmission system.

The fabricated circuit was included as modulator in an entire transmission system consisting of modulator and demodulator. From performance observations, it can be concluded that all initial requirements such as linearity and resulting harmonic and non-linear distortion levels could be fulfilled. Furthermore, extensive quantitative and qualitative measurements confirmed that the PFM modulator fulfilled all the requirements for quality still and moving picture transmission.

Finally, the PFM IC is compared with conventional PFM modulators from which it was concluded that a similar performance can be achieved at a much lower power consumption with the CMOS design. Further advantages include better reliability and ease of use due to lower component counts.

CHAPTER 8

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

8 CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

8.1 Conclusions

This thesis describes the design of a single chip PFM modulator implemented in a 2.4 μm CMOS technology. Various design approaches were considered in conjunction with a study of PTM schemes and circuit and silicon implementation techniques. Novel solutions were determined and the performance of the fabricated IC was compared with simulation results and with commercially available PFM modulators. The design was found to have a performance comparable with commercially available modulators but at a much reduced power consumption and circuit complexity.

The performance of different pulse time modulation techniques was compared with regard to transmission of video or TV signals. The advantages of using the PFM technique for these signals include better SNR performance than PWM while maintaining lower sampling ratios and cheaper system costs than PPM. PIM or PIWM in general offer no advantages compared with PFM or SWFM (the latter being closely related to PFM).

Silicon integrated circuit techniques have been discussed and reasons for choosing the CMOS technology include lower power consumption, near ideal switching characteristic and cheaper costs. The Alcatel MIETEC 2.4 μm CMOS technology was

chosen for the implementation of the PFM modulator because of its low cost and availability of a suitable CAD design environment.

An extensive analysis of DC and transient simulation and measurement results was carried out to determine the validity of the simulation results with the SPICE models employed. The effect of external loading by measurement equipment upon the circuit performance of the fabricated IC was investigated in detail. A novel approach of calculating this capacitive loading from transient measurements has been developed and this could be applied to other circuit designs.

Folding of MOS transistors with large width to length ratios is common in IC design. Folding will not only achieve a better aspect ratio of the transistor layout but increase the performance of the transistor due to reduction in active area and associated capacitances. A theoretical analysis of this effect was undertaken and novel equations developed which allow a designer to trade-off design shape against magnitude of parasitic capacitance. It was found that the minimum parasitic capacitance can be achieved at a folding grade of two and even values of folding grade generally achieve lower capacitances than odd values.

During simulations to confirm the theoretical predictions, a software problem in the netlist extraction tool of Mentor Graphics was discovered. This made this tool unusable for distributed parasitic extraction. The use of a different extraction tool, SPACE developed by the University of Delft, was investigated and incorporated into the existing IC design flow. Although, its applicability was proven it could not be used to

confirm the theoretical predictions due to insufficient technology information being available.

The voltage controlled oscillator is the main part of the PFM modulator. Advantages and disadvantages of different square wave voltage controlled oscillator circuits were reviewed. The selected method, a VCO design based on grounded capacitors, was critically reviewed and important criteria effecting the performance with regard to the circuit design and implementation were determined. HSPICE simulations were used to confirm the operation and achievable performance of this circuit.

Extensive quantitative and qualitative measurements of the final fabricated IC were subsequently performed to determine its performance in applications for transmission of video or TV signals. All the requirements for high quality transmission, such as maximum levels of harmonic and non-linear distortions, were achieved. At a carrier frequency of 32 MHz and a modulating input signal amplitude of 1 V, the circuit realises a harmonic distortion of -37.87 dB and a non-linear distortion of less than -56 dB. Live test carried out on actual video transmission confirmed that the modulator was capable of transmitting high quality still and moving picture information. Comparisons with PFM modulators, built with commercially available components, indicated that the design achieves a similar performance with much lower power consumption (~70% less) and a lower circuit complexity.

To the best knowledge of the author, the design represents the only single chip PFM modulator available at this time and is therefore in its entirety novel. This has been

achieved by close integration of circuit design considerations and layout implementations to procure a unique design.

8.2 Suggestions for Further Work

Although the performance meets the design specifications, certain criteria of the PFM modulator IC may be improved and its applicability extended.

Further analysis should enable the input voltage range to be extended to below 2.25 V resulting in an increased modulation range. Furthermore, the linearity of the system could be improved by adding a feedback loop to the design.

The suitability of the design for transmission of HDTV signals should be determined. This will include an increase in carrier frequency and modulation range which may be achieved by implementing the design in a different technology (such as the MIETEC 0.7 μm CMOS technology).

The effect of temperature upon the circuit performance should be analysed further. It should be determined whether the circuit can be altered so that its performance is less likely to be dependent upon the operating temperature. This may be achieved by making the temperature coefficient of the voltage to current converter opposite to that of the current controlled oscillator. Temperature compensation may also be achieved by implementing a feedback scheme [Kukielka *et al.*, 1981]

A further investigation might include the implementation of the electro-optic coupling devices such as LEDs or ILDs on-chip or within a hybrid device. This would increase the functionality of the design even further. This may also allow further improvements in the linearity by converting the optical signals back into electrical signals and using this information in a feedback loop. This might include implementing the design in a completely different IC technology.

This thesis has also presented a theory linking the layout of a folded transistor to its parasitic capacitances. This analysis could be confirmed by simulations using SPACE given the appropriate technology information. The theory could also be confirmed by practical measurements on fabricated layouts.

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APPENDICES

Appendix A: Alcatel MIETEC 2.4 μm CMOS technology

Foundry: Alcatel-MIETEC

Technology: 2 μm CMOS

Application: Digital, Analog and Mixed Analog-digital ASIC design for 12V applications

TECHNOLOGY DESCRIPTION

The 2 μm CMOS technology is a mixed analog/digital process with two layers of metal and two layers of low ohmic poly to form poly/poly capacitors.

General characteristics:

- EPI start material for high latch-up immunity
- N-well CMOS
- Optimised LOCOS for device isolation
- n+doped polysilicon gate
- Aluminium alloy based metallisation for low interconnect resistivity
- Nitride based passivation

Layout rules:

Both Full Digital and Mixed A/D design use identical layout rules.

Minimum electrical gate length: 2.4 μm for both PMOS and NMOS

Polysilicon pitch: 4.8 μm

Metal 1 pitch: 5.6 μm

Metal 2 pitch: 7.2 μm

Design is done in 3 μm design rules. Design is optically shrunk during mask making to 2.4 μm by a factor of 0.8. Fabricated area is 0.64 times the designed area.

Thin Oxide Poly/Poly Capacitor

Double poly capacitor

High value : 500 pF/mm^2 (80 nm oxide)

High linearity : 30 ppm/Volt typ.

STANDARD CELL LIBRARIES

Digital library MTC-2010

63 core cells (gates, latches, flip-flops,...)

33 I/O cells (CMOS & TTL levels, Bi-directional, level shifter, ...)

Compiled cells on request through EUROPRACTICE (RAM, ROM, PLA)

Characterised supply range : 3 ... 7 volt

For supply voltage < 3 V, most of digital cells are still working (until 1.5 V), but consult EUROPRACTICE.

Temp. range : -55 ... + 125°C ambient

Typical delay for loaded 2 input NAND : 2.5 nsec (8 standard loads)

Typical delay for unloaded 2 input NAND : 1.4 nsec

System speed up to 25 MHz (commercial temperature)

Power : 2 μW/gate/MHz at 5 V

Analog library MTC-2010

49 analog cells (bandgaps, opamps, oscillators, ...)

Block cells (A/D&D/A converters, special opamps)

Supply range: 3 ... 7 volt (low voltage range)

3 ... 12 volt (full voltage range)

7 ... 12 volt (high voltage range)

Temp. range: -55 ... + 125°C

DOCUMENTATION

Layout rules

Electrical rules

Spice parameters

Cell library documentation

CAD SUPPORT - DESIGN KITS

Cadence DFW-II

Front-end (schematic entry, Verilog simulation)

Back-end (Cell ensemble P&R)

Technology files for full custom design

Extraction and Spice netlist generation for full custom design

DIVA check

Synopsys

Schematic Entry, Simulation, Synthesis and Optimisation

Netlist transfer to Cadence and Mentor

Mentor V8

Front-end (schematic entry, Quicksim simulation)

AUTOLOGIC

Back-end (P&R)

IC rules check, IC Extract (extraction and Spice netlist generation)

Technology files

GDT technology files

DRACULA (DRC, ERC)

Appendix B: Measurement and calculations of capacitive loading

The second design was fabricated with external connections to the timing capacitors. These connections and the measurement equipment itself causes capacitive loading making a comparison between simulated and practical measurements (without knowledge of the parasitic loading) very difficult. An approach is given, which allows the determination of the capacitive loading.

The following derivations are made with the assumption that charging follows a linear and discharging follows an exponential function. Therefore, charging can be described by:

$$\Delta v_c = \frac{I_Q}{C} \cdot \Delta t \qquad \textbf{(B.1)}$$

and discharging by

$$v_c(t) = V_A \cdot e^{-\frac{t}{RC}} \qquad \textbf{(B.2)}$$

where v_c is the capacitor voltage, I_Q is the constant current charging the capacitor, V_A is the initial voltage amplitude and the other variables have their usual meaning. For each phase, two sets of measurements were taken, one with the on-chip capacitance plus total parasitic capacitance (C_p) and a second with an additional capacitance (C_a) of 3.3 pF added. This enables the calculation of the total capacitance (on-chip plus total parasitic). The method developed requires a curve fit of the experimental data (Figure B.1).

The capacitor charging follows a linear characteristic and is therefore fitted to:

$$y = ax \tag{B.3}$$

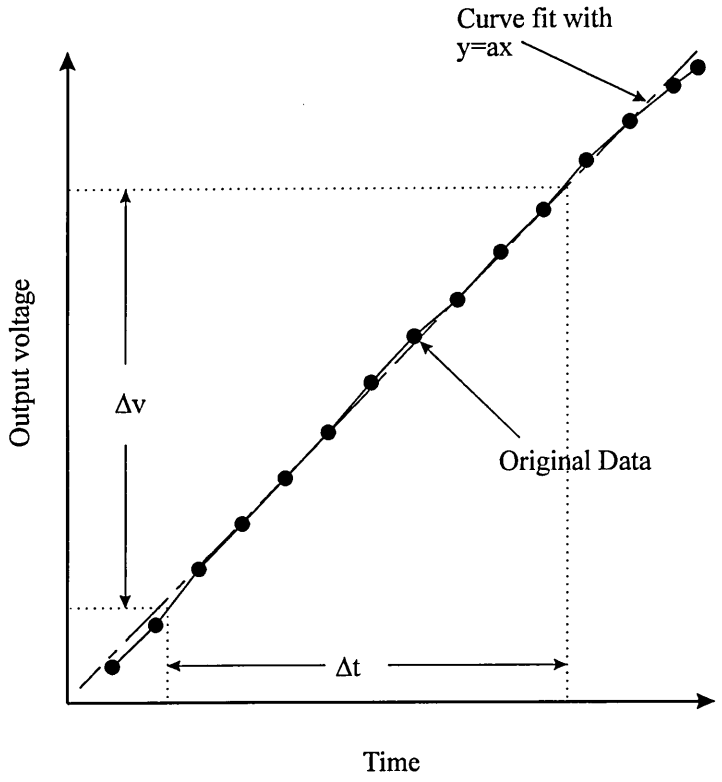

Figure B.1: Linear curve fit of charging phase

Two measurements resulting in two different values of a (a_1 and a_2) were taken. Comparing equation (B.1) with (B.3), one can see that $a = I_Q/C$. This can be mathematically described as follows:

$$\frac{a_1}{a_2} = \frac{\frac{I_Q}{C_p}}{\frac{I_Q}{C_p + C_a}} = \frac{C_p + C_a}{C_p} \tag{B.4}$$

This equation can be solved for C_p.

The capacitor charging follows an exponential characteristic and is, therefore, fitted to (Figure B.2):

$$y = V_A \cdot e^{-\frac{t}{b}} \tag{B.5}$$

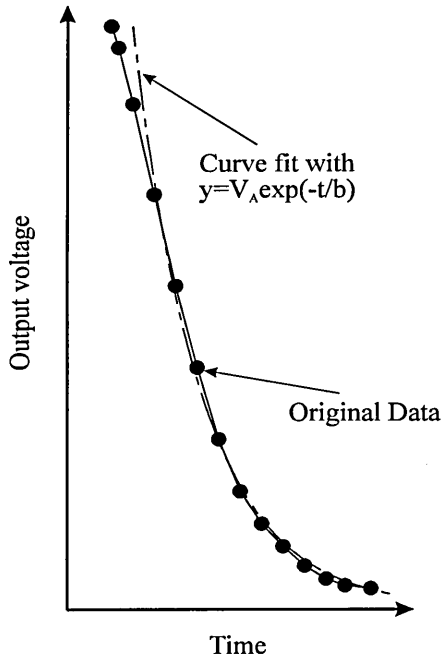

Figure B.2: Exponential curve fit

Again, two measurements were taken resulting in two different values of b (b_1 and b_2) with $b = RC$:

$$\frac{b_1}{b_2} = \frac{RC_p}{R\left(C_p + C_a\right)} = \frac{C_p}{C_p + C_a} \tag{B.6}$$

This equation can also be solved for C_p.

Measurements have been taken using a HP5420A oscilloscope with a HP1144A active probe. A double sided PCB board has been designed with the top side of solid copper as ground plane.

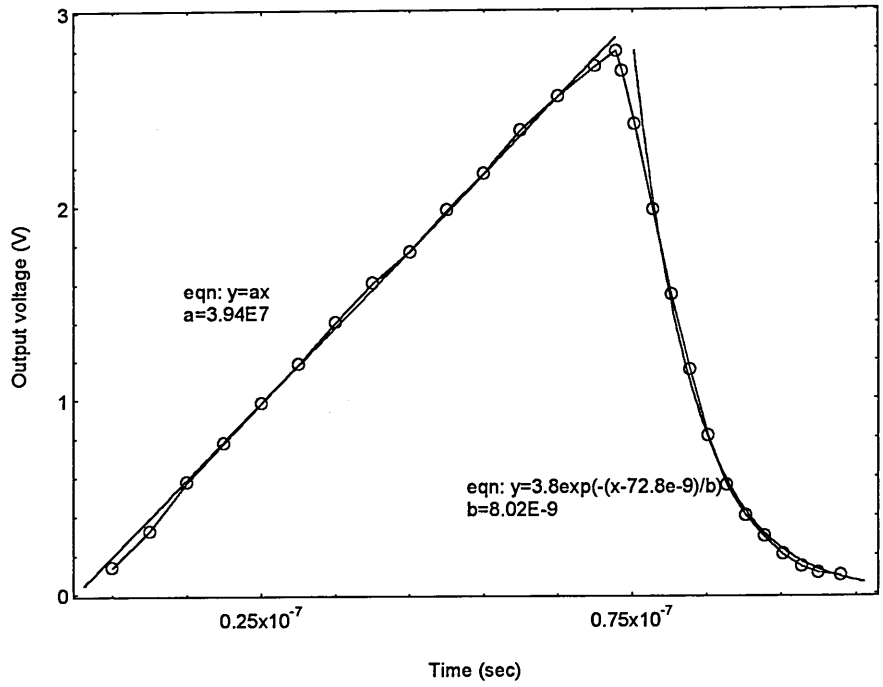

Figure B.3: VCO rise and fall time measurements (without C_a)

Figure B.3 shows the rise and fall time measurements taken with no additional capacitance present.

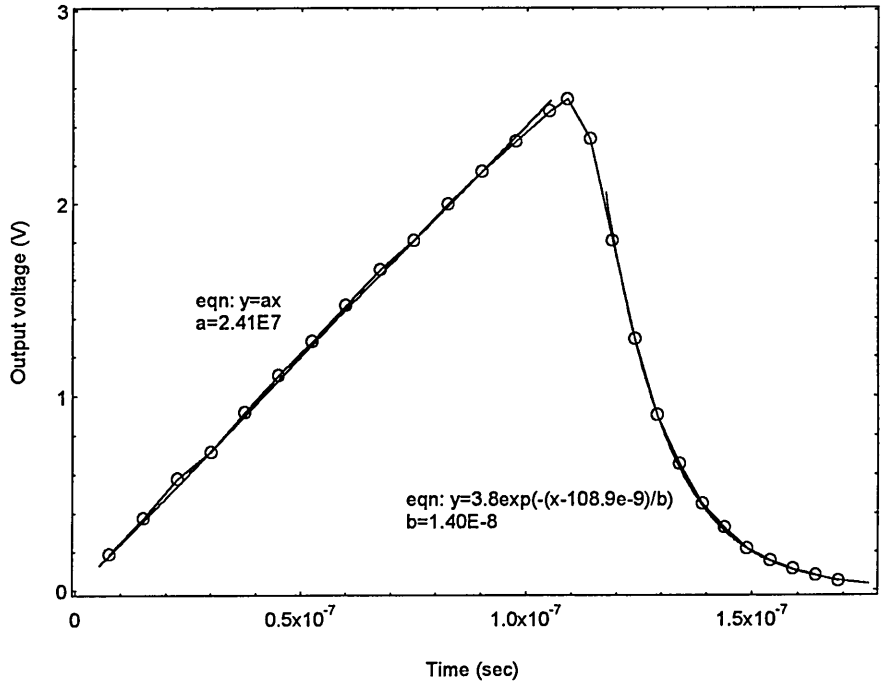

Figure B.4: VCO rise and fall time measurements (with C_a)

Figure B.4 shows the same measurements but with the additional capacitance present. Using equations (B.5) and values from Figure B.3 and Figure B.4, C_p was calculated to be 5.16 pF. Using equation (B.6) and the values from the same figures, C_p was calculated to be 4.43 pF. The difference of 16.5% may be caused by inaccurate curve fitting and different input capacitances of the oscilloscope and probe for rising and falling edges.

Appendix C: Extracted HSPICE netlist of PFM modulator chip layout

```
* Third design - netlist extraction
*
.include /users/research/eitus/h95.ini/hspice_cmos24_l3gsi.include
*.prot
*.option brief
*
VDDA 100 0 DC 5V
VDDD 101 0 DC 5V
Vin 1 0 DC 2.5V
*
X1 100 101 1 5 0 0 analyse_2
X2 5 9 O2
Cl 9 0 5pF
*
.tran 1e-9 1000e-9 -UIC
*
.print v(9)
*
* File: /users/research/eitus/mentor/third_design/analyse_2.sp.  Creation time: Wed Mar
27 14:21:05 1996
.subckt analyse_2 VDDA VDDD Vin Vout VSSA VSSD
* devices:
m0 31 6 5 VSSD nmos l=3u w=16.5u
m1 VSSD 8 31 VSSD nmos l=3u w=16.5u
m2 32 5 VSSD VSSD nmos l=3u w=16.5u
m3 8 7 32 VSSD nmos l=3u w=16.5u
m4 VSSD 3 7 VSSD nmos l=10u w=50u
m5 6 4 VSSD VSSD nmos l=10u w=50u
m6 33 8 3 VSSD nmos l=3u w=16.5u
m7 VSSD 4 33 VSSD nmos l=3u w=16.5u
m8 34 3 VSSD VSSD nmos l=3u w=16.5u
m9 4 5 34 VSSD nmos l=3u w=16.5u
m10 13 4 VSSD VSSD nmos l=3u w=7u
m11 14 13 VSSD VSSD nmos l=3u w=7u
m12 17 14 VSSD VSSD nmos l=3u w=7u
m13 11 28 VSSD VSSD nmos l=3u w=30u
m14 VSSD 28 11 VSSD nmos l=3u w=30u
m15 18 17 VSSD VSSD nmos l=3u w=7u
m16 19 VSSD VSSD VSSD nmos l=3u w=30u
m17 11 28 VSSD VSSD nmos l=3u w=30u
m18 20 18 VSSD VSSD nmos l=3u w=7u
m19 12 12 19 VSSD nmos l=3u w=30u
m20 VSSD 28 11 VSSD nmos l=3u w=30u
```

```
m21 19 12 12 VSSD nmos l=3u w=30u
m22 19 28 VSSD VSSD nmos l=3u w=30u
m23 21 20 VSSD VSSD nmos l=3u w=7u
m24 15 Vin 19 VSSD nmos l=3u w=30u
m25 VSSD 28 19 VSSD nmos l=3u w=30u
m26 22 21 VSSD VSSD nmos l=3u w=7u
m27 19 Vin 15 VSSD nmos l=3u w=30u
m28 19 28 VSSD VSSD nmos l=3u w=30u
m29 12 12 19 VSSD nmos l=3u w=30u
m30 23 22 VSSD VSSD nmos l=3u w=7u
m31 VSSD 28 19 VSSD nmos l=3u w=30u
m32 19 12 12 VSSD nmos l=3u w=30u
m33 19 28 VSSD VSSD nmos l=3u w=30u
m34 15 Vin 19 VSSD nmos l=3u w=30u
m35 24 23 VSSD VSSD nmos l=3u w=7u
m36 VSSD 28 19 VSSD nmos l=3u w=30u
m37 19 Vin 15 VSSD nmos l=3u w=30u
m38 19 28 VSSD VSSD nmos l=3u w=30u
m39 VSSD VSSD 19 VSSD nmos l=3u w=30u
m40 35 24 26 VSSD nmos l=3u w=16.5u
m41 VSSD 28 19 VSSD nmos l=3u w=30u
m42 VSSD 4 35 VSSD nmos l=3u w=16.5u
m43 28 28 VSSD VSSD nmos l=3u w=60u
m44 27 30 28 VSSD nmos l=5u w=20u
m45 VSSD 28 28 VSSD nmos l=3u w=60u
m46 Vout 26 VSSD VSSD nmos l=3u w=7u
m47 30 30 VSSD VSSD nmos l=6u w=4u
m48 5 6 VDDD VDDD pmos l=3u w=29.5u
m49 VDDD 8 5 VDDD pmos l=3u w=29.5u
m50 8 5 VDDD VDDD pmos l=3u w=29.5u
m51 VDDD 7 8 VDDD pmos l=3u w=29.5u
m52 3 8 VDDD VDDD pmos l=3u w=29.5u
m53 VDDD 4 3 VDDD pmos l=3u w=29.5u
m54 4 3 VDDD VDDD pmos l=3u w=29.5u
m55 VDDD 5 4 VDDD pmos l=3u w=29.5u
m56 13 4 VDDD VDDD pmos l=3u w=22u
m57 11 3 7 VDDA pmos l=10u w=50u
m58 6 4 11 VDDA pmos l=10u w=50u
m59 14 13 VDDD VDDD pmos l=3u w=22u
m60 17 14 VDDD VDDD pmos l=3u w=22u
m61 VDDA 15 11 VDDA pmos l=3u w=105u
m62 18 17 VDDD VDDD pmos l=3u w=22u
m63 11 15 VDDA VDDA pmos l=3u w=105u
m64 VDDA 15 11 VDDA pmos l=3u w=105u
m65 20 18 VDDD VDDD pmos l=3u w=22u
m66 21 20 VDDD VDDD pmos l=3u w=22u
m67 VDDA 15 12 VDDA pmos l=3u w=105u
m68 12 15 VDDA VDDA pmos l=3u w=105u
```

```
m69 22 21 VDDD VDDD pmos l=3u w=22u
m70 VDDA 15 12 VDDA pmos l=3u w=105u
m71 23 22 VDDD VDDD pmos l=3u w=22u
m72 15 27 VDDA VDDA pmos l=3u w=105u
m73 VDDA 27 15 VDDA pmos l=3u w=105u
m74 24 23 VDDD VDDD pmos l=3u w=22u
m75 15 27 VDDA VDDA pmos l=3u w=105u
m76 26 24 VDDD VDDD pmos l=3u w=29.5u
m77 27 27 VDDA VDDA pmos l=3u w=105u
m78 VDDD 4 26 VDDD pmos l=3u w=29.5u
m79 VDDA 27 27 VDDA pmos l=3u w=105u
m80 27 27 VDDA VDDA pmos l=3u w=105u
m81 Vout 26 VDDD VDDD pmos l=3u w=22u
m82 VDDA 30 30 VDDA pmos l=7u w=8u
c83 7 VSSD 330f
c84 6 VSSD 330f
c85 15 12 0.5p
r86 VSSD 9 10.2k
r87 10 9 10.2k
r88 10 12 10.2k
.ends analyse_2
*
.SUBCKT O2 3 4
*       Part:           o2
*       Pin:            IN      Node:  3
*       Pin:            OUT     Node:  4
*       Supply:         VDD     Node:  2
VDD 2 0 DC 5
*       Supply:         VSS     Node:  0
M_INS2 4 5 2 2 p_32 W=0.00067362 L=3.2e-06 AD=4.04172e-09
+ AS=4.04172e-09 PD=0.00135924 PS=0.00135924 NRD=0.00534426
+ NRS=0.00534426
M_INS4 4 5 0 0 n_31 W=0.00043085 L=3.1e-06
+ AD=2.5851e-09 AS=2.5851e-09 PD=0.0008737 PS=0.0008737 NRD=0.00835558
+ NRS=0.00835558
M_INS8 5 3 2 2 p_30 W=0.000222 L=3e-06 AD=1.332e-09
+ AS=1.332e-09 PD=0.000456 PS=0.000456 NRD=0.0162162 NRS=0.0162162
M_INS10 5 3 0 0 n_30 W=7e-05 L=3e-06 AD=4.2e-10
+ AS=4.2e-10 PD=0.000152 PS=0.000152 NRD=0.0514286 NRS=0.0514286
.model n_30 nmos level=2 vto=.9 kp=5.7e-05 gamma=.3 phi=.7 lambda=0.05
+ cgso=1.8e-10 cgdo=1.8e-10 cj=7e-05 mj=.5 cjsw=3.9e-10 mjsw=.33
+ js=0.001 tox=4.25e-08 nfs=1e+11 ld=2.2e-07 ucrit=10000 rsh=25
+ af=1 kf=2.3e-27
.model p_30 pmos level=2 vto=-.9 kp=1.7e-05 gamma=.5 phi=.69
+ lambda=0.04 cgso=2.8e-10 cgdo=2.8e-10 cj=0.00033 mj=.5 cjsw=4.4e-10
+ mjsw=.33 js=0.001 tox=4.25e-08 nfs=1e+11 ld=3.5e-07 ucrit=10000
+ rsh=45 af=1 kf=7.2e-29
.model n_31 nmos level=2 vto=.9 kp=5.7e-05 gamma=.3 phi=.7
```

```
+ lambda=0.0483871 cgso=1.8e-10 cgdo=1.8e-10 cj=7e-05 mj=.5
+ cjsw=3.9e-10 mjsw=.33 js=0.001 tox=4.25e-08 nfs=1e+11 ld=2.2e-07
+ ucrit=10000 rsh=25 af=1 kf=2.3e-27
.model p_32 pmos level=2 vto=-.9 kp=1.7e-05 gamma=.5 phi=.69
+ lambda=0.0375 cgso=2.8e-10 cgdo=2.8e-10 cj=0.00033 mj=.5 cjsw=4.4e-10
+ mjsw=.33 js=0.001 tox=4.25e-08 nfs=1e+11 ld=3.5e-07 ucrit=10000
+ rsh=45 af=1 kf=7.2e-29
.ENDS O2
*
.END
```

Appendix D: Full-custom IC design flow using Mentor Graphics IC Station

Full-custom design involves the generation of an IC mask layout by creating and editing each polygon manually. It generally gives the most compact design shape.

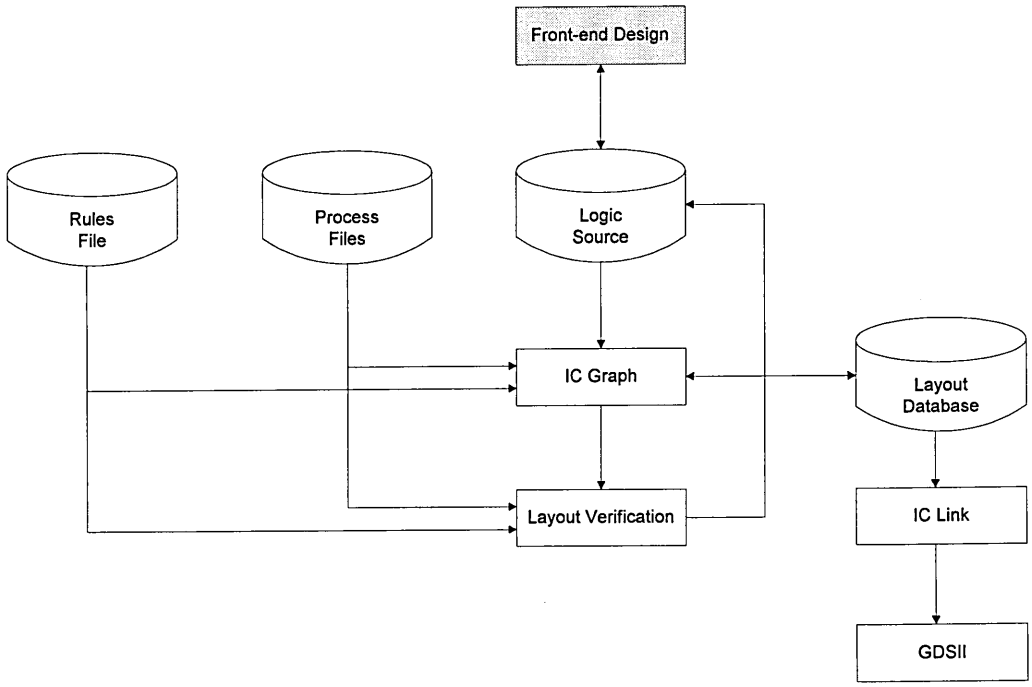

Figure D.1: IC Station full-custom IC design flow

IC Station provides the IC environment in that all IC tools operate. Figure D.1 shows the design flow and tools employed for implementing a full-custom IC [Mentor Graphics, 1993]. Rules and process files are dependent upon the IC technology used and are provided by the foundry or service centre. The logic source can be a design viewpoint created with the Design Viewpoint Editor (DVE). IC Graph is the layout editor used to manually create and edit polygons. The layout database contains all files necessary for the IC design. IC Link is the IC Station layout translator allowing the

finalised design to be translated into a standard format (e.g. GDSII) and then electronically transmitted for design submission.

Implementation of rules and process files

Rules and process files are normally provided by the foundry together with installation notes. Some of the design environment variables found in the location map have to be added. These will point towards the location of all necessary files. In case of the Mietec 2.4 μm CMOS technology, some environmental variables pointing to the Mietec userware have to be included into the shell startup file. This userware is adding some additional menus to the MG design tools, especially to the Design Architect (DA) and the DVE.

Mietec design environment

The Mietec design environment is shown in Figure D.2 [Das, 1993].

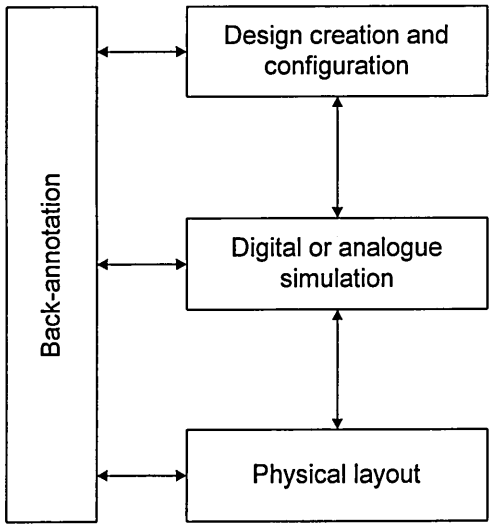

Figure D.2: Mietec design environment

With the installed design kit and the necessary configurations made, the design kit lets you create and configure designs with DA and DVE. DVE information provide the link between schematic information created in DA and simulation and layout tools. Back-annotation between the different tools may be used to confirm performance specifications. More detailed information for digital or analogue simulation or physical layout can be found in the Mietec design kit user's guide [Das, 1993].

Detailed information about the adopted IC design flow using the Mietec 2.4 μm CMOS technology, necessary files and information and how these are incorporated into the design software are given in Figure D.3. Information on how to use DA, DVE and IC Station can be found on the Inform CD-ROM accessible via the Bold Browser together with tutorials explaining in detail the different tools (Table D.1) available to the designer [Mentor Graphics, 1993]:

Table D.1: Explanation of tools used for the full-custom IC design

Tool	**Description**
DA	Used to create circuit schematics
DVE	Prepares project schematics for use with a specific MG tool by creating a logic source
IC Graph: IC Rules IC Trace IC Extract	IC design tools interface • Set of functions that together with a rules file allow to perform design and geometry rules checking • Set of functions that allow to perform layout versus schematic verification • Set of functions that together with process files allow to extract a SPICE netlist from the IC layout
IC Link	Program that converts IC layout information into the GDSII format

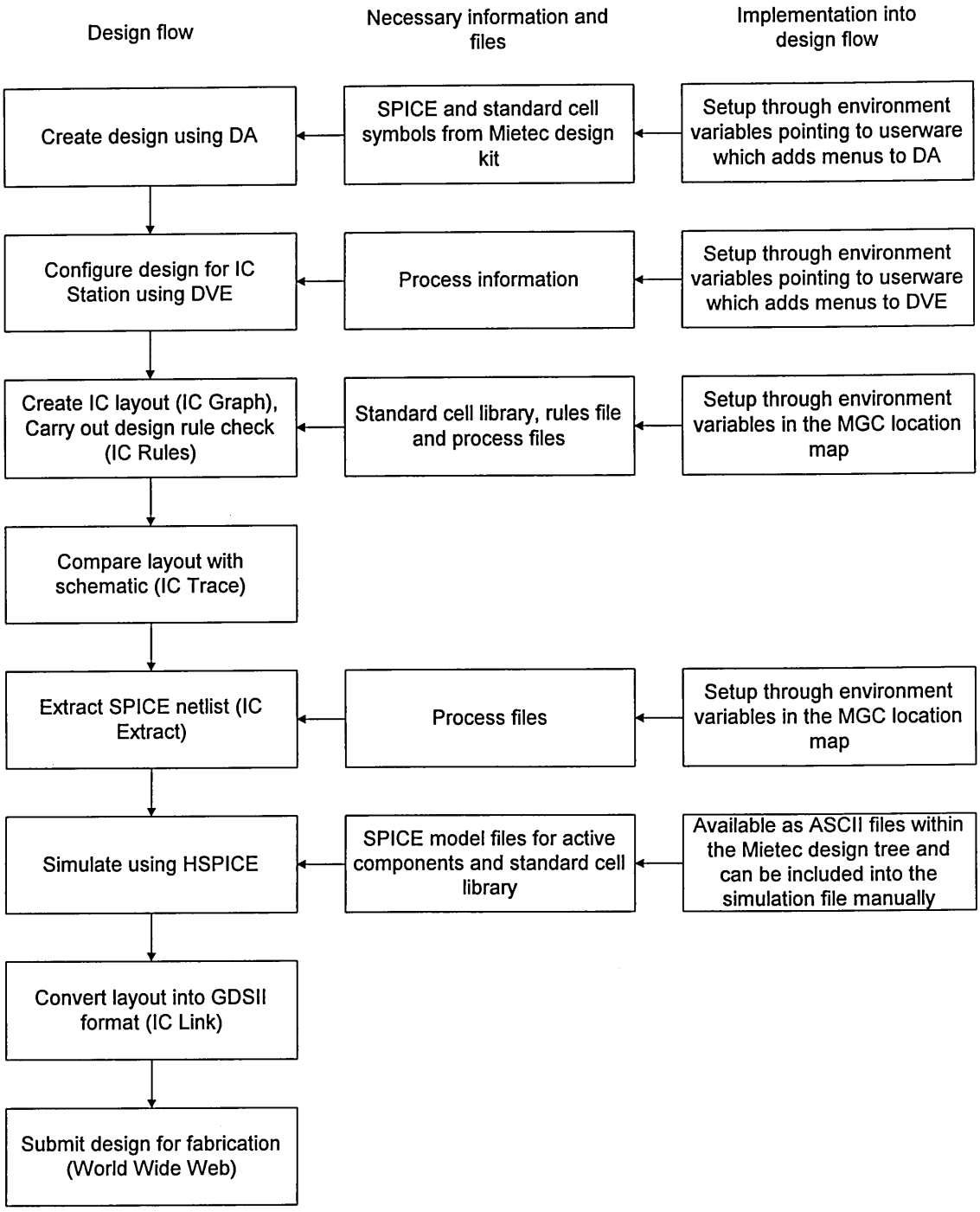

Figure D.3: Detailed information of adopted design flow using the Mietec technology

Directory structure and necessary files for setting up the design environment

In general, three software packages, Mentor Graphics, Mietec design kit and HSPICE must be linked together to carry out all the necessary design work. All of these packages should be installed by the system administrator and the user has only to access the software. In order to do that, several directories and files have to be created to set up the design environment for the user.

Figure D.4 shows the user home directory structure and files necessary to setup the design environment. The Mietec design kit is incorporated by a combination of settings in the '*.cshrc*' file and the '*mgc_location_map*' which is located under the directory '/ecad/mentor/etc'. HSPICE is setup by the '*hspice.ini*' file and settings in the '*.cshrc*'. Mentor Graphics is setup and customised by a combination of entries in the '*mgc_location_map*' and the '*.cshrc*' files as well as through all files under the 'mgc' directory (Figure D.4). All necessary files are listed underneath.

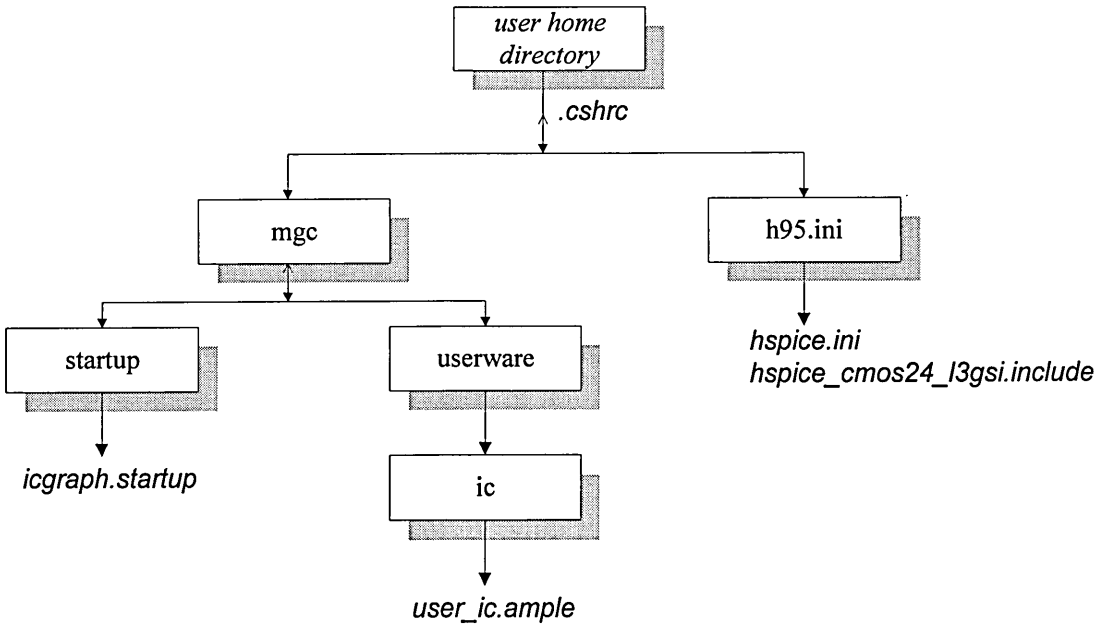

Figure D.4: User home directory structure

icgraph.startup

```
$load_userware("/users/research/eitus/mgc/userware/ic/user_ic.ample", "user_ic", @ample);
$setup_new_windows(@on, 0.5, 0.5, 1, 5, 0, 0, 5);
$set_undo_level(50);
$set_crosshair_style(@full90);
$show_layer_palette(@replace, ["1", "2", "4", "5", "7-12", "13", "109", "112"]);
```

user_ic.ample

```
function $print_object(
        printer : string{ default = $get_printer_name() },
        site : label string{ default = $get_site_name() },
        copies : label integer [ 1, 99 ]{ default = $get_num_copies() },
        config : label string{ default = $get_job_config() },
        orientation : switch name [bestfit, landscape, portrait] {default = $get_orientation()},
        priority : label name [ low, normal, high ] { default = $get_priority() },
        alarm_type : switch name [ noalarm, alarm ] { default = $get_alarm() },
        scale : label number{ default = $get_scale() },
        panel : label string{ default = $get_object_view() },
        save_options : switch name [ nokeep, keep ] { default = @nokeep },
        sw_arg_scale : optional string{ default = $get_sw_arg_scale() }
        )
{
// redefine $print_object to call $print_cell
// this is used for export graphics
        $print_cell(
        printer,
        $get_print_layers(),
        $get_print_levels(),
        $get_print_peeked_only(),
        $get_print_array_style(),
        copies,
        config,
        orientation,
        priority,
        alarm_type,
        scale,
        $get_print_grid(),
        $get_print_cull(),
        panel,
        @nokeep
        );
}
```

hspice.ini

```
* READING FILE:  /users/research/eitus/h95.ini/hspice.ini
.prot
.option
+ search=/ecad/meta/95/parts/ad
+ search=/ecad/meta/95/parts/behave
+ search=/ecad/meta/95/parts/bjt
+ search=/ecad/meta/95/parts/burr_brn
```

```
+ search=/ecad/meta/95/parts/comlinear
+ search=/ecad/meta/95/parts/dio
+ search=/ecad/meta/95/parts/fet
+ search=/ecad/meta/95/parts/lin_tech
+ search=/ecad/meta/95/parts/pci
+ search=/ecad/meta/95/parts/signet
+ search=/ecad/meta/95/parts/ti
+ search=/ecad/meta/95/parts/tline
+ search=/ecad/meta/95/parts/xilinx
**** add any user options, parameters, model includes,
***  subcircuit includes or libraries here
.unprot
.OPTION ICSWEEP=1
.OPTION ParHier=Local
.SAVE  TYPE=NODESET LEVEL=ALL
```

hspice_cmos24_l3gsi.include

```
* include file for MIETEC CMOS 2.4um process HSPICE files
.prot
.temp=27
.option post acct opts
.graph
.options scale=0.8 scalm=1
.options ingold=2
.include /ecad/eurochip/mietec_lib/analog/cmos24/mietec_cmos24_l3_modelcards.cir
.include /ecad/eurochip/mietec_lib/analog/cmos24/mietec_cmos24_subcircuits.cir
.unprot
```

Additions to 'mgc_location_map'

```
# MGC SYS-1076 std v8.2_1.9
$MGC_SYS1076_STD
<path_to_mgc_home>/pkgs/sys_1076_std/std

# MGC SYS-1076 mgc_portable v8.2_1.9
$MGC_SYS1076_PORTABLE
<path_to_mgc_home>/pkgs/sys_1076_std/mgc_portable

# MGC SYS-1076 ieee v8.2_1.9
$MGC_SYS1076_IEEE
<path_to_mgc_home>/pkgs/sys_1076_std/ieee

# MGC SYS-1076 src v8.2_1.9
$MGC_SYS1076_SRC
<path_to_mgc_home>/pkgs/sys_1076_std/src

# MGC gen_lib V8.2_1
$MGC_GENLIB
<your_path>/gen_lib

# Synthesis library
$MGC_SYNLIB
<your_path>/software/mentor82/syn_lib
```

```
# EUROCHIP mietec_lib for Mentor v8.2
$MIETEC_LIB
<your_path>/mietec_lib

$MIETEC_CMOS24_IC_PROC
<your_path>/mietec_lib/layout/cmos24/process/mietec_cmos24

$MIETEC_CMOS24_IC_RUL
<your_path>/mietec_lib/layout/cmos24/process/mietec_cmos24_rules

$MIETEC_CMOS24_IC_LIB
<your_path>/mietec_lib/layout/cmos24/library/mietec_cmos24

$MIETEC_CMOS24_ACCUSIM_MODFILE
<your_path>/mietec_lib/analog/cmos24/mietec_cmos24_subcircuits.cir

$MIETEC_CMOS24_ACCUSIM_MODCARDS
<your_path>/mietec_lib/analog/cmos24/mietec_cmos24_l3_modelcards.cir

$MIETEC_QCHECK_ERC
<your_path>/mietec_lib/qcheck/config_data/erc_rules.bin

$MIETEC_QCHECK_NC
<your_path>/mietec_lib/qcheck/config_data/nc_rules.bin

# This one is a work-around for AutoLogic
$DEV_LIB
<your_path>/mietec_lib

# Spice primitives library
$SPICE_LIB
<your_path>/spice_lib
```

Necessary additions to the '.cshrc' file

```
# Set up environment for Mentor:
        set path= PATH /ecad/mentor/bin)
        setenv MGC_HOME /ecad/mentor
        setenv MGLS_LICENSE_FILE /ecad/flexlm/licenses/license.dat
        setenv MGC_LOCATION_MAP /ecad/mentor/etc/mgc_map
                setenv ICSPOOLPATH /users/research/eitus/mentor/icplots
# End of Mentor additions

# Mietec design kit additions
        setenv AMPLE_PATH /ecad/eurochip/mietec_lib:/ecad/eurochip/spice_lib
# End of Mietec additions

# HSPICE Additions on Wed May 31 10:48:46 BST 1995
        setenv METAHOME /ecad/meta/95
        setenv installdir $METAHOME
        if ( $?PATH ) then
                setenv PATH $METAHOME/bin:$PATH
        else
                setenv PATH $METAHOME/bin:/bin:/usr/bin
        endif
```

```
        if ( $?MANPATH ) then
                setenv MANPATH $METAHOME/docs:$MANPATH
        else
                setenv MANPATH $METAHOME/docs:/usr/man:/etc/man
        endif
# End of HSPICE Additions
```