FABRICATION AND CHARACTERISATION OF POROUS SILICON

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Declaration

I certify that this thesis submitted for the degree of Ph.D. is the result of my own research, except where otherwise acknowledged, and that this thesis has not been submitted for a higher degree to any other university or institution.

Signed:.....

MOHAMMED FADHIL MABROOK

Date:..../..../....

Dedication

This thesis is dedicated to my beloved *parents*, *brothers*, *sisters*, my *wife* and my coming *child*.

ABSTRACT

A systematic study has been made of the electrical conduction processes through electrically etched porous silicon (PS) films sandwiched between two metal electrodes. The PS layers were formed by anodisation of p-type silicon wafers in a hydrofluoric (HF) acid solution. The effect of fabrication conditions on the structural and electrical properties of PS have been investigated. The thickness of PS layers was found to depend on the anodisation time, whereas porosity was regarded to be controlled by the current density and HF acid concentration.

The dark current-voltage I(V) characteristics at fixed temperature and the variation of current as a function of temperature have been established. The characteristics for all devices, regardless the metal contact, show a rectifying behaviour with ideality factor close to unity. It was found that PS films fabricated from p-type silicon substrates behave like n-type silicon due to the depletion of electronic holes. The results suggest that a pn heterojunction between PS and p-Si is responsible for the rectifying behaviour. A value of 0.7 eV was obtained for the barrier height at the interface between PS and p-Si at room temperature. The barrier height was found to increase with rising temperature. Recombination conduction process was found to be dominant at low temperatures as the activation energy did not exceed 0.22 eV. At high temperatures, thermionic emission diffusion process was found to be responsible for the current transport in the PS structures. A band model was proposed for metal/PS/p-Si/metal structures in order to explain the observed characteristics. A.c. dark current measurements revealed that the a.c. conductivity varies as ω^s where ω is the angular frequency and s is an index which depends on temperature and having a value less than unity. A.c. activation energy was interpreted in terms of hopping conduction at low temperatures (less than 200 K) and diffusion transport of charge carriers through PS layers at higher temperatures. Measurements of capacitance as a function of frequency and temperature showed a decrease with increasing frequency and increase with increasing temperature. The photoconduction behaviour of PS was characterised by high dark resistivity, a clear photosensitivity for visible light, and a bias voltage dependence of the spectral response.

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CHAPTER ONE

INTRODUCTION AND AIMS OF THE WORK

Silicon is a material which accounts for over 98% of sales in the global semiconductor market. There are many reasons why silicon devices dominate the microelectronics market, but the main factor is their stability and low manufacturing cost. Millions of devices with identical properties can be fabricated across increasingly larger silicon wafers, reducing the cost per device. The fabrication processes and the performance of the devices relay mainly on a number of inherent properties of silicon. Insulating materials made from silicon substrates (like silicon dioxide and silicon nitride) have allowed silicon to dominate over the other materials such as gallium arsenate (gas) and III-V semiconductor compounds. Moreover, it is more expensive to fabricate devices from III-V materials than from silicon because different processing techniques must be used and these have not yet reached the remarkable yields of silicon chips [Paul 2000].

However, there are a number of areas where silicon devices cannot compete with other semiconductor devices. The band structure of silicon has an indirect band gap of 1.1 eV, which means there is no optical recombination of excited states in bulk silicon in the visible region. As a consequence, optoelectronic devices, such as light emitting diodes, have to be made with other substrates. GaAs proved to be leading in this kind of devices as the electrons in the conduction band can combine with the holes in the valence band much more easily in GaAs than in silicon. In recent years, it is found that light emission out of silicon becomes achievable by using nanocrystalline silicon

structure. The way of obtaining this type of structure is by the formation of porous silicon (PS) [Richter et al 1992].

The principle feature of PS is a fine structure consist of pores separated by very small size columns of silicon. It may be fabricated by electrochemical desolution of silicon in a concentrated hydrofluoric (HF) acid solution. The pore size and hence the porosity of PS can vary over wide range depending upon the type and resistivity of the silicon substrate, the current density during anodisation, and the concentration of HF acid [Bomchil and Halimaoui 1988, Herino et al 1992, Badoz et al 1993]. Under the right conditions, more than 85% of the silicon is etched off leaving very thin silicon rods separated by large pores. The thickness of the PS layer can be controlled by the anodisation time, which usually does not exceed 30 minutes [Halimaoui et al 1992, Filippove et al 1994].

PS with high porosity can produce photoluminescence and electroluminescence in the visible range [Canham 1990, Koshida and Koyama 1992]. PS shows an increase in the band gap shifting the absorption edge to higher energies. The band gap energy and the peak of the luminescence spectrum are mainly depending on the fabrication conditions of the PS layer. However, the electrical properties of PS have recently attracted considerable attention owing to its potential applications in optoelectronic devices and sensor systems. Furthermore, the significant increase in the surface to volume ratio made from PS a promising layer for chemical sensing technology. This phenomenon has stimulated investigations into potential applications of PS in the field of gas sensing. Adsorbed species, such as alcohol, benzene, and other gases have profound effects on the PS film electronic properties [Angelucci et al 2000, Bilenko et al 2000, Bogue 1997, Thust et al 1999].

Al, Au, and ITO electrodes have been found to behave as injecting contacts to PS, where ohmic and rectifying behaviours have been observed. Sandwich thin film structures of PS were investigated with reasonable thicknesses of PS layers. The conduction mechanism of PS is somewhat complex and numbers of theories have been developed based on various experimental data. Two junctions could be responsible for the conduction in PS sandwich structures. Schottky junction between the metal and the PS layer was firstly reported as the main blocking contact responsible for the rectifying behaviour of the structure [Kosida and Koyama 1992, Dimitrov 1995, Simons et al 1995]. In the last few years it was reported that a pn heterojunction between the PS layer and the silicon substrate is behind the rectifying behaviour of PS [Pulsford et al 1994, Ray et al 1998].

Under a.c. fields, the conductivity of PS is higher by several orders of magnitude than that under d.c. conditions [Cruze et al 1998]. In general, the conductivity decreases with increasing frequency in the case of band conduction process, while it increases with increasing frequency in the case of hopping conduction process. Ben-Chorin et al (1993) reported that band conduction occurs at high temperatures and hopping transport become dominant at low temperatures in the PS devices made from n-type silicon substrates.

Our knowledge of the electrical and photoelectrical properties of PS is generally rather limited. The aim of this work is to investigate the fabrication and the electrical characterisation of PS. It is hoped that the results obtained should also be of assistance in any future work made on similar structures. To achieve this, a variety of experimental techniques have been utilised to study PS thin film for material

characterisation. These techniques include electrical and photoelectrical studies of metal/PS/p-Si/Al sandwich structure and the microstructure study of PS thin film using SEM technique. The major part of the experimental work can be summarised as fellows:

I. The first stage of the study was to design and build a PS fabrication set-up and prepare suitable homogenous and reproducible samples. Different samples with different fabrication conditions were produced for electrical and photoelectrical studies.

II. D. c. current-voltage characteristics within the temperature range 152 - 300 K were measured in order to determine the activation energy, barrier height, and the type of conduction mechanism in PS.

III. A.c measurements in the frequency range 20 Hz to 1 MHz and the temperature range of 152 - 300 K have also been carried out to gain further information on the conduction mechanisms in PS.

IV. Spectral responses of PS samples in different thicknesses were measured in the UV, visible, and IR regions. The photocurrent effect was also investigated for the same samples.

The thesis is presented in eight chapters. A general review of PS and its properties, in particular electrical properties, is given in chapter two. Details of the methods of fabrication, deposition, and measurement techniques are discussed in chapter three. Chapter four reports the structural properties and the electrochemistry

of pore formation of PS. Theoretical aspects concerning conduction mechanisms in semiconductors are introduced at the first parts of chapters five, six, and seven. The other parts of these chapters are devoted to a detailed account of the results obtained, data analysis, and discussion of the results. Finally, in chapter eight general conclusions concerning the results obtained and suggestions for further work are presented.

CHAPTER TWO

GENERAL REVIEW OF POROUS SILICON

2.1 Introduction

This chapter is a general review of the formation and the structural, electrical and luminescence properties of porous silicon (PS). Special attention will be given to the formation and the electrical properties of PS, and in particular the mechanisms responsible for the current transport through PS structures. The remainder of the chapter is concerned with the electrical and industrial application of PS.

2.2 Band structure of semiconductors

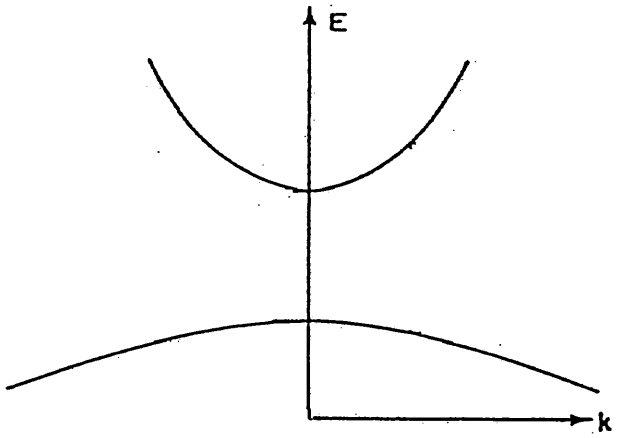
The basic property of a semiconductor is that it has an energy gap which separates the filled valence band from the empty conduction band. Conventionally, the band structure of a semiconductor is represented by a dispersion relation $E(k)$ where E is the energy of an electron (or hole) at the band edge and k is the wave vector. Figure 2.1 shows the E versus k diagram for Si and GaAs. It could be noticed that the valence band structure for most semiconductors is similar especially at $k = 0$. According to the band structure, semiconductors can be divided into two classes. The first class is called direct bandgap semiconductors in which the valence band maximum and the conduction band minimum occur at the same value of the wave vector. The other class of the semiconductors are those in which the conduction band minimum and the valence band maximum are separated in k space and known as indirect band gap

semiconductors. Figure 2.1(a) demonstrates the GaAs as a direct band gap semiconductor, with its conduction band minimum directly above the valence band maximum at the point where $k = 0$. In Fig. 2.1(b) the lowest minimum in the conduction band displaced from the point $k = 0$ resulting on indirect band gap in silicon. In the indirect band gap semiconductors, the electron moving from valence to conduction band must undergo a change in wave vector. The disadvantage of the indirect band gap semiconductors is that the optical absorption is allowed only with absorption of a phonon to conserve crystal momentum and it is much weaker process than in direct band gap materials [Chelikowsky and Cohen 1976, Ioffe 1960, Moss 1961, Perkowitz 1993, Rice 1977, Voos et al 1980]. An electron can be elevated from the valence to the conduction band if it absorbs a photon whose energy is at least equal to the band gap value. The reverse process, since momentum must be conserved, would result in photoluminescence process near the band gap which strongly affected by whether the material has a direct or indirect bandgap [Iyer and Xie 1995, Pankove 1971].

2.3 Nanostructured silicon (porous silicon)

Although bulk silicon is intrinsically inefficient at radiative recombination process, silicon can however be produced in nanostructured forms which produce efficient photoluminescence (PL) in the visible range. During the studies of electropolishing of silicon (electrolytic smoothing of solid surfaces) Uhlir at Bell Labs, US, in 1956 discovered the first PS film (under certain conditions an unwanted black film appeared on the wafer surface). There was only little interest in this black film until Yoshio Watanabe and co-workers at NTT Japan realised, during the early

1970's, that these films were highly porous (and called porous silicon) and likely to be readily oxidised and of potential use in silicon-on insulator (SOI) technology. The formation mechanisms of this new material have been studied widely by a large number of scientists [Beale et al 1985, Bomchil et al 1989, Gee 1960, Memming and Schwartz 1966, Parkhutik et al 1983, Turner 1958, Unagami 1980]. In 1981, Kazou Imai at NTT, demonstrated that full isolation of silicon devices could be achieved by using PS (so called FIPOS technology). Ten years ago, Canham from the Defence Research Agency, UK, described the process of making porous layers on the surface of silicon wafers as a technique of fabricating silicon quantum wires of subnanometer size as shown in Fig.2.2 [Canham 1990]. It was found that the optical properties of PS are different from the those of bulk silicon. Moreover, PS exhibits PL at an energy that is large compared to the band gap of crystalline silicon [Canham 1990, Cullis and Canham 1991, Foll 1991, Herino et al 1992, Kalkhoran et al 1992, Koshida and Koyama 1991, Koshida and Koyama 1992, Lee and Peng 1993, Lehmann et al 1992, Maruyama and Ohtani 1994, Motohiro et al 1995, Read 1992, Rees 1991, Sanders and chang 1992, ünal and Bayliss 1996]. The absorption edge of PS was found to be shifted to higher energies of about 1.5 eV compared to bulk crystalline silicon which has an absorption edge in the infrared region. The increase in the band gap and the emission energy suggested to be due to the quantum confinement effect, i.e. if the porosity of PS increases (leading to thinner wires) the band gap becomes greater and the PL emission will be at higher energy [Canham 1990]. Other possible mechanisms could be responsible for the light emitting in PS is the existence of luminescent molecules such as siloxene on the surface of the pores. The data on PS obtained so far support the quantum confinement mechanism suggested by Canham (1990).



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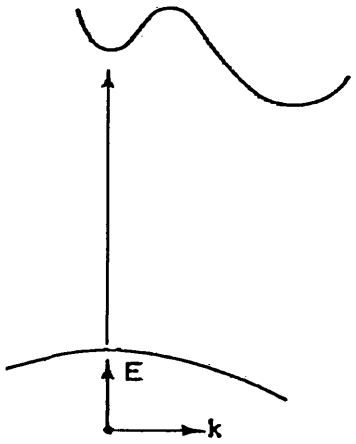

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Figure 2.1 The energy bands for direct (a) and indirect (b) bandgap materials [After Voos etal 1980].

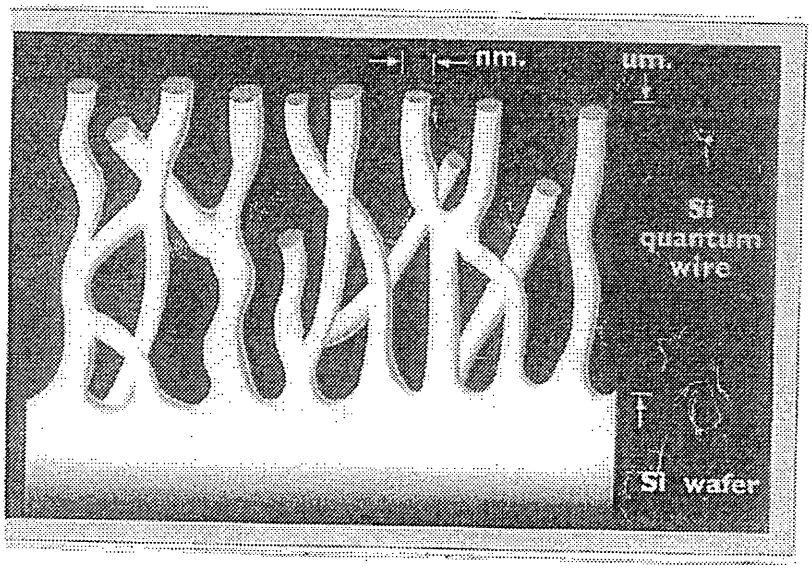


Figure 2.2 Schematic diagram of porous silicon layer [After Canham 1990].

The increased band gap decreases the concentration of the mobile charges within the remaining silicon structure and create a depletion layer [Smith and Collins 1992]. These results were reproduced by workers in many laboratories around the world and intense investigations into this phenomenon resulted [Koshida and Gelloz 1999, Pulsfurd 1994]. Electroluminescence (EL) in the visible range has been also observed from Schottky diodes formed on PS [Halimaoui 1991, Koshida and Koyama 1992].

2.4 Formation of porous silicon

Porous silicon is fabricated by an anodic dissolution process in hydrofluoric acid (HF) based electrolyte. Although the microscopic details of pore formation are complex and not completely understood, a complex grid of interconnected silicon skeleton is created. The microstructure of PS depends on the composition of the electrolyte, the type and resistivity of the starting silicon substrate, the current density during anodisation, and the anodisation time [Halimauoi et al 1991, Brandet et al 1992, Herino et al 1992]. Under the right conditions, a large pore structure created, in which as much as 85% of the silicon is etched off leaving silicon wires as thin as a few nanometers [Herino et al 1992, Zhang et al 1992].

The principal feature of PS is a very fine structure either wires or dots and the structural analysis of this material is quite difficult. In contrast, the formation of PS appears to be a self-adjusting process in which the quantum confinement effect governs the formation process. Using p-type substrates, the PS structure gets smaller until full depletion of the holes occurs on the surface of the PS layer. The electrochemical etching process stops at this stage if no extra holes are supplied to the surface by the

light. In n-type silicon substrates, there are no holes present and a depletion layer forms around the pores forcing the etching process to stop. To continue the etching until the production of nanoporous film, it is important to illuminate the samples during the fabrication to generate more holes on the surface [Steiner et al 1993]. In general, PS layers are fragile and by nature exhibit very high surface area. The resulting structure luminescence from red to blue when an UV radiation is applied to its surface.

The thickness of the PS layer can be controlled by the anodisation time only [Halimaoui et al 1991, Filippove et al 1994]. Depending on the type and resistivity of the silicon substrate, the diameter of electrochemically etched pores cover most of the PS layer. According to the pore size of PS layers, the material can be designated into three types [Cullis et al 1992]:

1. Microporous silicon, with pore diameter of less then 2 nm.
2. Mesoporous silicon, with pore diameter between 2 and 50 nm.
3. Macroporous silicon, with pore size of more than 50 nm.

The material with greatest interest is microporous silicon because of its luminescent properties. Although microporous silicon is found in all samples independently of the level of doping, only on moderately doped p-type substrate can pure microporous silicon be found. On p^+ and n^+ type substrates the PS structure is a mixture of microporous silicon and mesoporous silicon, while for low doped n-type substrates the microporous silicon is found to cover the wall of macropores [Gösele and Lehmann 1995, Lockwood et al 1992]. The inhomogeneous doping of the silicon substrate would make the structure even more complicated. Table 2.1 summarises the

fabrication conditions which lead to the creation of a layer of PS on top of the silicon substrate.

Substrate resistivity	0.01 - 250 Ω/cm
Current density	1 - 250 mAmp./cm^2
HF acid concentration	10 -50 %

Table 2.1 Fabrication conditions of PS

The formation of microporous silicon can be understood in term of hole depletion in the porous structure due to its quantum size dimensions [Lehmann and Gösele 1991]. According to this model, using higher formation current density (Higher than 100 mAmp./cm^2) leads to a smaller and mechanically less stable skeleton of microporous silicon. A microporous silicon layer of high porosity cracks during drying and the pieces shrink in size. This is could be due to the collapse of the pores under the attractive forces between the hydrogen atoms expected on the wall of the silicon wires. Microporous silicon layers formed at current densities below 100 mAmp./cm^2 were found to dry without cracking for a layer thickness of about 10 μm which attributed to the more stable silicon skeleton formed at low current densities [Filippove et al 1994, Lockwood et al 1992].

The relationship between the band gap widening and the size of the silicon wires in PS has been studied by many researchers. According to different experimental studies the photon energy of the PL from PS is about 1.6-2.2 eV, and thus the band

gap widening must be larger than this. The typical size range of the silicon wires in this type of PS layers is between a few nm and 10 nm [Bayliss et al 1994, Muller et al 1993]. Sanders and Chang (1992) give the wire thickness of about 1.5-3 nm for the fundamental bandgap of 1.5-2.7 eV. Other calculations by Buda et al (1992) estimated the thickness of the silicon wires to be between 0.83-1.45 nm, whereas 2.5-4.5 nm thicknesses were reported by Proot et al (1992) and Delerue et al (1995). From the study of Steigmeier et al (1992), it was found that the nanopartical diameters of PS reach more than 10 nm for energy bandgap range of 1.7-2.8 nm.

2.5 Porosity and pore size

Although there is some divergence of the calculated values of the porosity and the pore size depending on the methods and researchers, its clear that the calculated values for silicon nanowires are too small to be consistent. It is not easy to measure the pore size or the silicon nanowires since the pore dimensions are usually below the resolution limit of the scanning electron microscopy (SEM) as will be clearly studied in chapter four. For clear images of the surface of the PS layer it is important to use transmission electron microscopy (TEM) which required removing the PS layer from it's substrate. The pore size increased with the formation current density and the formation time. It was also found that the pore size correlates with the HF concentration with non-linear increase with decreasing HF concentration [Herino et al 1987].

The other important parameter in PS characteristics is the porosity of the sample. Porosity (P) can be estimated if the sample is weighed, before anodic reaction (m_1), after anodic reaction (m_2), and after the removal of the PS layer from the

substrate (m_3). The porosity then can be calculated with an accuracy of about 2% according to [Herino et al 1987]:

$$P = \frac{m_2 - m_3}{m_1 - m_3} \tag{2.1}$$

Matsuda et al (1990) used the optical properties of PS to estimate the porosity. According to their method, the porosity can be calculated using:

$$1 - \frac{P}{100} = \frac{n_c^2 - 1}{n^2 - 1} \tag{2.2}$$

Where n is the refractive index of the bulk silicon and n_c is the refractive index of the porous silicon. However, porosity can be estimated from the cross section SEM study of the PS layer profile (more details in chapter 4).

Bomechil and Halimaoui (1988) have investigated the relationship between the porosity and the fabrication conditions. For a given HF concentration, the average film porosity increases with the formation current density. For a heavily doped substrate in 25% HF concentration, the porosity increases regularly from about 25% to 70% when the formation current density rises from 10 mA/cm^2 to 250 mA/cm^2. The current density was estimated from I/a, where I is the measured current and a is the surface area of the anode. At higher current densities, the porosity becomes very high and the material losses its mechanical cohesion and becomes like a powder. However, it is possible to create a PS layer with porosity of more than 70% by reducing the HF acid concentration and increasing the current density. If the current density further

increased, direct electropolishing of the anodised layer will take place and then no film formation [Bomchil and Halimaoui 1988].

For all kind of substrates, an increase in the HF acid concentration, keeping a constant current density, results in decreasing porosity of the PS layer. If the porosity reaches values more than 70%, again the layer losses its mechanical properties and behaves like a powder. It is possible to form PS layers with the same porosity and pore size using a different combination of fabrication conditions [Herino et al 1987].

2.6 Porous silicon for optical measurements

The study of PS is usually carried out with the PS layer attached to the silicon substrate. However, for the optoelectronic characterisation of PS it is necessary to evaluate the intrinsic nature of PS without the effect of the silicon substrate. Moreover, it is not possible to study the optical properties of PS without detaching the layer from it's substrate. Self-supporting PS layers can be prepared by electrochemical separation of the anodised PS layer. This is achieved by rapidly increasing the anodisation current density up to the values in the electropolishing region (> 400 mA/cm^2) after the completion of the PS formation [Koshida and Koyama 1992b]. Badoz et al (1993) produced a self supported PS layer by reducing the HF acid concentration to a very low concentration (below 10%) and increasing the current density to a value of about 250 mA/cm2. The outcome from the electrochemical separation process is a very thin layer of PS (few micrometers) which proved to be very difficult to handle. In order to make an electronic contact to the self supported PS layer, Hlinomaz et al (1994) proposed a mechanical contact holder (Fig. 2.3) which could be used for electrical, photoelectrical and optical measurements of the self supporting PS layer. The sample

placed between two glass microscopic slides coated on the inner side by indium tin oxide (ITO) or Cr and mechanically gently pressed together. The advantage of this holder is that there is no risk of short circuit that may be caused by evaporating a metal to make the electrical contacts [Badoz et al 1993, Hlinomaz et al 1994].

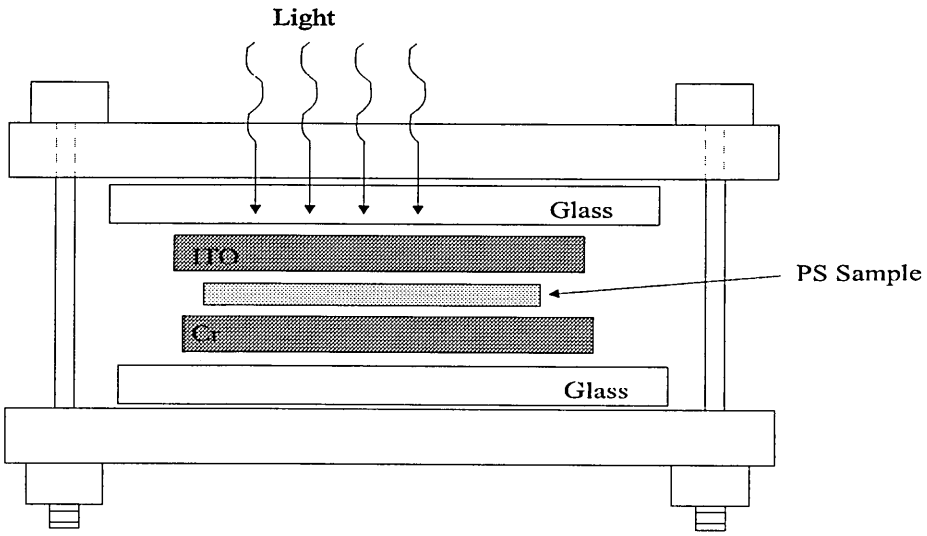


Figure 2.3 Mechanical contact holder [After Hlinomaz et al 1994].

2.7 Photoluminescence in porous silicon

Radiative recombination in semiconductors has been the subject of an enormous number of experimental and theoretical investigations that have proven very fruitful for the development of semiconductor physics. These fundamental studies have given rise to interesting applications in light emitting diodes and semiconductor lasers.

The simplest case of radiative recombination is when electrons in the conduction band recombine with the holes in the valence band giving up energy, which approximately corresponds to the energy bandgap, as electronic radiation which may be emitted from the semiconductor [Ellis 1973, Street 1991].

In the electronic excitations of a semiconductor which result in a nonequilibrium state of the semiconductor, radiative recombination represents one of the processes that can achieve a relaxation to the semiconductor ground state and regain the equilibrium state. Typically, excitation may be by photon absorption (photoluminescence) or current injection (Electroluminescence) [Voos et al 1980].

Photoluminescence (PL) is defined as the optical radiation emitted at different wavelengths by a physical system resulting from excitation to a nonequilibrium state by irradiation with light [Barry Bebb and Williams 1972]. PL emission is characteristic of material and involves radiative transitions between electronic energy levels in the material. The transition originates on some excited electronic levels, and after the emission of a photon a lower electronic level is occupied [Bar-Lev 1984]. The mechanism of PL can be divided into three stages, the first stage is the excitation of electron-hole pair. This occurs by photon absorption with energies close to the band gap energy. In the second stage, the excited carriers thermalise rapidly down to the band edge by emitting phonons until they are captured into localised states. The final stage is where the carriers can recombine either radiatively to give PL or non-radiatively [Bar-Lev 1984].

In bulk silicon, because of its indirect band gap, the emission of light is not possible due to the need of a change in the crystal momentum. Therefore the PL of bulk silicon is weak as nonradiative recombination becomes more efficient. But since

the discovery of the strong visible PL in PS by Canham (1990) many experimental and theoretical investigations have tried to identify the origin of this PL. However, the mechanism of the strong visible PL from PS still unclear. The main difficulty of this problem arises mainly from the large surface to volume ratio in nanostructures. Two main mechanisms have been invoked to explain PL in PS. The first one assumed that the visible light emission from PS layer is not an intrinsic property of crystalline silicon but depends on specific chemical reactions of silicon with hydrogen and oxygen [Brandt et al 1992, Fuchs et al 1992, Koch 1993, Stutzmann et al 1993]. The second mechanism proposed that PL in PS is intrinsic due to quantum confinement effects in small size silicon wires in the PS layer [Amato et al 1994, Canham 1990, Cullis and Canham 1990, Fauchet 1998, Filippov et al 1994, Gelloz 1997, Gole et al 1999, Korol and Kikkarin 2000, Koyama et al 1996, Lahmann and Gösele 1991, McGinnis et al 2000, Muller et al 1993, Rajaraman et al 1997, Skryshevsky 2000, Tsu et al 1992, Uosaki et al 1996, Wang 1995, Zhang 1995]. The second explanation is now more favoured as most works agree that the quantum size effect in the spongelike PS skeleton might play a key role in its optical properties as suggested originally by Canham (1990).

The most convincing results which support the quantum size effect is the blue shift of the PL peak with increasing the porosity of the PS layer which represents the average size of the PS nanostructures [Voos et al 1995]. The results is in qualitative agreement with the quantum size effect and indicates that the increase in the porosity results in a decrease in the size of the silicon wires in PS making the carrier confinement energy increase.

2.8 Electroluminescence in porous silicon

Electroluminescence (EL) occurs when electrons in materials such as semiconductors, are excited by the application of an electric field to the material, resulting in an electric current passing through it. The electrons recombine with holes to emit light as a function of applied voltage. Most practical solid state devices for visible injection EL used III-V compounds such as GaAs and GaP. This is because this series of materials produces high efficiency LEDs due to their direct energy band gap.

Since the discovery of visible PL from PS by Canham (1990), the production of efficient visible EL from PS has become a goal of extreme practical importance, motivated by the potential application in optoelectronic devices [Araki et al 1996, Bsiesy and Vial 1996, Bsiesy et al 1995, Fauchet 1996, Goryachev et al 1997, Halimaoui et al 1991, Koshida and Koyama 1992, Koshida et al 1995, Lalic and Linnros 1996, Nishimura et al 1998, Riess et al 1994, Steiner 1995, Takasoka and Kamei 1994]. EL has been observed with either dry contacts obtained by metallisation of the sample surface [Koshida and Koyama 1992, Koyama et al 1993, Lopez and Fauchet 1999, Nyrup et al 2000, Ogasawara et al 1995, Riley et al 1996, Tsybeskov 1995] or wet contacts resulting from immersion of PS in an electrolyte [Gelloz et al 1998, Goryachev et al 2000, Halimaoui et al 1991, Kooij et al 1994, Peter and Wielgosz 1996, Sakai et al 1994]. EL has been induced by injection of a sufficient number of electrons into the porous silicon layer (where the radiative recombination occurs).

Just like PL, EL can be analysed in the framework of the quantum confinement model [Bsiesy et al 1996, Muller et al 1993, Kozlowski and Lang 1992]. Short lived

EL has been observed during anodic oxidation of PS fabricated from p-type silicon substrate [Halimaoui et al 1991]. Efficient EL has also been observed from PS layers fabricated from n-type silicon substrates [Astrove et al 1995, Canham et al 1992, Gelloz et al 1998, Goryachev et al 2000, Lopez and Fauchet 1999, Riley et al 1996].

EL has been obtained from PS by making Schottky diodes between PS and Au or ITO electrodes. Diodes made by evaporation of Au, however, have showed a very low efficiency because the evaporated contact does not penetrate into the nanoporous layer and involves high applied bias voltages [Bsiesy et al 1996, Koshida and Koyama 1992]. Using indium tin oxide (ITO), generally, as the top electrode in LEDs provide better contacts and less light absorption.

2.9 Electrical properties of porous silicon

The discovery of electroluminescence behaviour in PS has stimulated many researchers to make further d.c. and a.c. electrical measurements on the material over a wide range of temperature and frequency. Wide range of theoretical and experimental studies have been carried out in an attempt to understand the electronic conduction mechanism of this material. The electrical conductivity is affected by the fabrication conditions of PS, especially the formation time as it controls the thickness of the PS layer and then the resistivity of the PS layer. Disagreements reported between the experimental and theoretical results obtained by different workers from measurements on PS are mainly due to this effect. Other factors like the humidity of the device and residual HF acid inside the PS pores reported to have important influence on the electrical properties of PS.

2.9.1 D.C. conductivity in porous silicon

The first experimental evidence for rectifying behaviour in luminescent PS was reported in 1992 during EL study of the PS structure [Koshida and Koyama 1992, Namavar et al 1992]. Later, many researchers studied the electrical properties of metal/PS/Si/metal structures at room temperature [Lazarouk et al 1996, Maruska et al 1993, Namavar et al 1992, Simons et al 1995] and as a function of temperature [Dittrich et al 1996, Mares et al 1993, Mathur 1998]. In semiconductor device technology the electrode material is of great importance in determining the type of conductivity observed. Therefore, the electrical properties of PS devices in terms of current-voltage response have been studied using different types of contact. In general, Al [Ben-Chorin et al 1994, Deresmes et al 1995, Lazarouk et al 1996, Ray et al 1998], Au [Ozaki et al 1994, Ke et al 1998] and ITO [Namavar et al 1992, Pacebutas et al 1995] electrodes were used in most of the studies. The results indicate rectifying behaviour in all structures, except in some studies were they found that the behaviour of the device depends on the top electrode work function [Simons et al 1995, Oguro et al 1996].

Molnar et al (1999) have also investigated the current-voltage behaviour of ITO/PS/Si/Al structures for n-type and p-type substrates. They found ohmic behaviour for the n-type PS samples at low voltages (V>5V) and then the current increasing exponentially at higher voltages. In the p-type PS structures, however, the space charge region is confined to a much lower voltage (V<1V). At the same time, light emission from the p-type PS structures was found to take place under forward conditions, while in the n-type PS structures the luminescence appears in the reverse bias only.

There are two different opinions on the reason for the rectification effects in PS devices. In the majority of the work, the rectification in current-voltage characteristics is believed to be due to the existence of a Schottky barrier between the metal and PS interface. However, the interpretation of rectifying characteristics due to the junction between the PS and its silicon substrate is also reported. Ke et al (1998) have studied the contact barrier at Au/p-PS interface using ballistic electron emission microscopy (BEEM). This technique is more accurate than the conventional techniques, such as current-voltage and capacitance-voltage, in measuring the barrier height at metal/semiconductor interface. As the PS surface consists of wires and pores with dimensions of few nanometers, the contact barriers are expected to vary in a similar scale [Lavine et al 1993]. Therefore, extremely high resolution BEEM technique should be applied to gain reasonable information on this type of surface. The barrier heights measured from the current-voltage characteristics at different points of the PS surface were reported to be between 0.89-1.1 eV. In fact most of the barrier heights reported in the literature are much larger than that for the Au/p-Si interface (0.34 eV, Sze (1981)). However, there are some conflicting values for the barrier heights in the range of 0.8 eV, reported for a similar structure [Tung 1991]. These values are very close to that of Au/n-Si indicating that these contacts are likely to occure at the centre of wires in the PS layer. Ke et al (1996) concluded that PS could behave like n-type silicon at some points of the surface.

Deresmes et al (1995) have characterised Al/PS/p-Si/Al structures using electrical measurements. They conclude that the Schottky junction between Al and PS is responsible for the rectifying behaviour with a barrier height ranged between 0.1-0.3 eV. Schottky diode behaviours with anideality factor of 1.8 and barrier height of 0.75

eV were also reported for Au/PS/n-Si/Al structures [Dittrich et al 1996]. Similar results with even higher ideality factors were also observed for PS structures with different top electrodes [Bogue 1997, Koshida and Gelloz 1999, Koshida and Koyama 1992, Lazarouk et al 1996, Namavar et al 1992, Tsai et al 1993, Yu and Wie 1992, Zheng et al 1992]. Simons et al 1995 have proved that PS is n-type in nature by comparing the current-voltage characteristics of different metal/PS/n-Si/Al structures. They noticed that if Al were used as the top electrode, the structure would show ohmic behaviour. However, using Au as a top electrode results in a rectifying Schottky barrier of height 0.74 eV. Moreover, they observed similar behaviours for metal/PS/Al structures. Hence, they conclude that there is no effect of the silicon substrate on the device behaviour. Same conclusions were reported by Mares et al (1993) as they observed a linear current-voltage behaviour from Au/PS/p-Si/Al structure. The exponential increase in dark conductivity with temperature of the structure was ascribed to the tunnelling between thermally vibrating sites placed on the surface of PS. PS layers consist of several sublayers with different structural characteristics were reported by Pacebutas et al (1995). 1-3 μm thick nanostructured top layer was observed on top of a microstructured layer connected to the silicon substrate. Improved electrical and photoelectrical diode performances were observed for the samples with the top layer being removed [Krotkus and Pasiskevicus 1992, Maruska et al 1993]. All the above reported evidence indicates that the interface between metal and PS plays a major role in the conduction mechanism in PS.

On the other hand, many workers have observed n-type material behaviour in PS. A study by Simons et al (1995) showed that PS fabricated from n-type substrates is n-type in nature. Furthermore, the electrical properties of PS films fabricated from p-type substrates have shown the same results [Mabrook et al 1995, Ozaki et al 1994].

This behaviour was ascribed to the depletion of holes in PS films and the fact that the depletion width is at least two orders of magnitude longer than the thickness of the silicon rods in PS film [Amisola et al 1992]. Also Pulseford et al (1993) have made a systematic study of the effect of various electrodes and the thickness of PS layers on the electrical properties of PS. They rolled out the effect of the metal/PS interface on the electrical properties of the material as they found that the device turn on is similar for all electrodes. Moreover, they reported that photoexcitation at the interface between the metal and the PS and across the PS layer produces no response. However, a sharp increase in the photocurrent is found to occur when the region just inside the silicon substrate is illuminated. This area of the device represents the interface between the PS layer and the silicon substrate, where the silicon is not completely etched.

Estimated values of the PS band gap were calculated from the luminescence and optical properties of the material. The photolominescence spectra of various devices show a peak at 650-700 nm at room temperature. This indicates that the band gap of the device is about 1.7-1.8 eV [Lang et al 1993, Pavesi et al 1997, Roy et al 1992, Vial et al 1992]. Furthermore, the peak of the photoluminescence spectra mainly depends on the thickness of the PS layer. Hence, the band gap of a PS layer depends essentially on the fabrication time. Cullis et al (1994) have observed a 1.5-1.7 eV band gap for PS layers depend on the postanodisation treatments. Optical studies of PS also shows an energy band gap of about 1.6-1.8 eV [Balagurov et al 2000, Buda et al 1992, Palsule et al 1997, Proot et al 1992]. Photoelectronic properties of PS show that PS layers have much wider band gap than silicon [Stievenard and Deresmes 1995]. Therefore, a heterojunction is expected to build up between PS and the silicon substrate resulting in the rectifying behaviour of the device [Pulsford et al 1994, Zimin 2000, Vikulov et al 2000]. The junction is either isotype heterojunction when n-type

silicon substrate is used, or anisotype heterojunction in case of using p-type silicon substrate.

Values of the barrier height reported heretofore range from 0-7-0.8 eV [Simons et al 1995, Dittrich et al 1996, Ray et al 1998]. These values of barrier heights are reported for PS samples made from both p-type and n-type substrates. However, higher values of barrier heights were reported for Au/PS/n-Si/Au structures [Laiho and Pavlov 1995]. Lower values of barrier heights were also observed for Al/PS/p-Si/Al structures at room temperature [Deresmes et al 1995, Pulsford et al 1994].

A very wide range of ideality factors were reported for different PS structures. Namavar et al (1992) have observed diode ideality factors of about 10 for a ITO/PS/p-Si/Al structure. Ideality factors of about 3-5 were also reported for Au/PS/n-Si/Al structures [Simons et al 1995, Pacebutas et al 1995]. However values of less than 2 were also reported for different PS structures [Dittrich et al 1996, Ray et al 1998].

The age of the PS samples were reported to have a considerable influence on their semiconducting properties. Ciurea et al (1998) have reported a stabilisation in the electrical properties of stored PS films compared to fresh samples. They observed a stronger rectifying behaviour for the PS films stored for 18 months in ambient conditions. In addition, the activation energy of the stored samples was estimated to be 0.6 eV at low temperatures and 1.8 eV at higher temperatures in contrast to the value of 0.55 eV calculated for fresh samples at all temperatures. This variation in conduction behaviour was ascribed to oxidation of the surface of the PS layer. These results are supported by the fact that PL properties (the shape of the spectral response and the position of the maximum) are changed with the age of the PS film [Ciurea et al 1996].

The thickness of the PS layer also plays a vital role in the electrical properties of the film. The value of the serial resistance of the device depends on the thickness of the PS layer. Values of few KΩ to a few tens of MΩ are reported for different PS samples [Yeh et al 1993, Mares et al 1993]. Ohmic behaviour was observed for thick PS samples, whereas rectifying conduction was found for thin layers. PS layers with thicknesses greater than 28 μm were found to show linear current-voltage characteristics in the range of -100 V to 100 V. However, thinner samples appear to show rectifying behaviour at threshold voltages dependent on the PS layer thickness [Balagurov et al 2000]. At the same time they found the activation energy for all samples to be 0.55 eV at room temperature. The significant increase of resistivity was attributed the existence of hydrogen on the surface of the PS wires which passivate the dopant atoms. Mathur et al (1998) have observed symmetrical current-voltage characteristics only in the samples with thickness greater than 2 μm. Similar results were reported by Ben-Chorin et al (1994) for PS layers of 10 μm thickness.

It is well known that the electrical properties of a semiconductor could change drastically when adsorbing pollutant gas. PS is found to behave like a semiconductor in response to gases, humidity and oxygen [Bilenko et al 200, Koshida and Gelloz 1999]. Furthermore, various ambients have an influence on PS surfaces, and therefore, PS films have potential for the coming generation of gas sensing devices [Bilenko et al 2000, Kelly and Bocarsly 1998]. For the PS fabricated from p-type substrates, the conductivity was found to increase many orders of magnitude in response to vapour pressure change from 0 to 100% [Schechter et al 1995]. More about the PS response to the ambient environment is are reported in section 2.10.

2.9.2 A.c. conductivity and capacitance

The d.c. electrical properties of PS have been widely studied, however much less data on the a.c. electrical properties is known. The a.c. conductivity of PS studied up to date has generally shown a power law dependence on angular frequency ω of the form ω^s. The index s was found to be variable, increasing with increasing frequency and decreasing with increasing temperature. This type of dependence represents a universal law [Mott and Davis 1971]. Such behaviour was observed over a frequency range of up to 10^6 Hz and a temperature range of 77-360 K. Ben-Chorin et al (1993) investigated the a.c. conductivity of a 10 μm thick PS layer at a wide range of frequencies and at different temperatures. The band gap energy of the sample was estimated to be around 1.7 eV. They observed power law conduction properties with an exponent $s = 0.95$ at frequencies below 10 kHz. At higher frequencies they reported higher values of s and they found no temperature dependence of the a.c. conductivity. Popkirov and Ottow (1997) have made a.c. measurements on Au/PS/n-Si/Al structure at room temperature and over a frequency range of 10-10^6 Hz. They claimed that the a.c. conductivity was almost constant at low frequencies whilst it was frequency dependent with $s = 0.85$ at higher frequencies. They concluded that this conduction was mainly due to the diffusion of charge carriers through the PS layers at low frequencies, whereas at high frequencies it is due to hoping of charge carriers. Higher values of s were also observed in different PS structures. Values of more than unity are observed for the exponent s by many researchers [Dimova-Malinovska et al 1997, Geloz and Bslesy 1998, Lysenko et al 1999, Yeh et al 1998].

The a.c. conductivity of Al/PS/p-Si/Al structures were studied by Parkhutik (1996) in the ranges 0.2-10^5 HZ and -100 to 200 ^{0}C. He observed a wide range of

activation energies (from 0.08 to 0.3 eV) directly influenced by the state of the surface layer at the pores walls (heated, wet or dry, etc.). Therefore, he claimed that it is very important to control all factors of PS formation and post-anodisation treatments to insure the necessary electrical and optical properties of PS. Parkhutik et al (1996) have also studied the electrical properties of PS at different post-anodisation treatments. They observed a linear growth of conductivity with increasing frequency for dry samples, whereas the as anodised samples are characterised by a power low with s changes between 0.2 to 1. They conclude that the frequency dependencies of the a.c. electrical conductivity of PS are sensitive to the presence of the residuals of electrolyte inside the pores.

Measurements of capacitance and loss tangent (tan δ) as a function of temperature and frequency are also of interest. Generally, it has been observed that the capacitance decreases with increasing frequency, and increases with increasing temperature. This behaviour was observed in Ag/PS/p-Si/Al [Lebedev et al 1995] and Al/PS/p-Si/Al [Arita and Kuranari 1997] structures. Linearly decreased capacitance with log(f) was also observed over a wide range of frequencies [Averkiev et al 1996]. They reported a low frequency dispersion of the electrical capacitance at room temperature, and no frequency dependence at low temperatures. Such data may be interpreted using existing theory, for the case of a thermally activated process when using ohmic contact [Gaswami and Gaswami 1973].

The loss tangent, which relates the conductance and the capacitance, is also influenced by both frequency and temperature. A decrease in tan δ with increasing frequency has been observed in Al/PS/p-Si/Al structures [Arita and Kuranari 1997]. However, this parameter has received very little attention in PS studies.

2.9.3 Photoconduction properties of PS

The dark d.c. electrical properties of PS have been widely studied, however much less data on the photoelectric properties are available. The photoconduction in PS layers studied to date has generally shown a clear widening in the energy band gap compared to crystalline silicon. Under negative bias, normalised photoconduction spectra at room temperature of a Au/PS/p-Si/Al structure shows that the peak wavelength shifts toward the lower energy side with increasing bias voltage. In contrast, the peak wavelength was found independent of the applied voltage for positive bias (Positive or negative bias voltage was applied to the Al contact with respect to the Au electrode) [Ozaki et al 1994]. Photoresponse spectra with a peak wavelength at 750 nm was observed by Pacebutas et al (1995). They also showed that the peak wavelength was independent on the resistivity of the silicon substrate. Similar results were also reported by Dinova-Malinovska et al (1997) for Zno/PS/p-Si/Al structure. Dafinei and Dafinei (1999) have also studied the electrical conductivity in PS under light at room temperature. They reported a red shift of the spectral response as the reverse bias increases. This behaviour was interpreted as a result of the increase of the band gap of PS and the existence of a heterojunction structure between PS and the silicon substrate. Also, Palsule et al (1997) found that the value of the peak of the photocurrent spectra depends mainly on the thickness of the PS layer, and the peak was observed at about 850 nm. On the other hand, Wang et al (1997) have reported a red shift in the photocurrent spectra as the anodisation current of the PS decreases. Peaks at 500nm were also reported for the photoconduction spectra of Au/PS/p-Si/Au structures.

Photocurrent-voltage characteristics have been studied by different researchers. For all PS structures it was found that the short circuit current (I_{sc}) and the open circuit voltage (V_{oc}) increases with increasing illumination intensity. Under the optimum preparation conditions, Lee et al (1999) have found a short circuit current of about 4 μA, and an open circuit voltage of about 0.52 V under tungsten lamp illumination of 24.4 mW/cm^2. Similar values of I_{sc} and V_{oc} were also reported for different PS structures [Parkhutik 1999].

2.10 Practical applications of porous silicon

The stability and high resistivity of PS indicates its potential usefulness as an insulator. However, since the initial exploration of the PL and EL properties of PS at room temperature, there have been continuous interest in the technical development of the material in the field of optoelectronic devices [Balagurov et al 2000, Ciurea et al 1998, Gaburro et al 2000, Herino et al 1992, Koshida and Gelloz 1999, Martin-Palma et al 2000, Mikrajuddin et al 2000, Molnar et al 1999]. To date, PS in general is not utilised commercially as a light emitting device due to technical difficulties involved in the fabrication of the device. Lack of reproducibility, very short life time and low efficiency of the luminescence properties of PS are the difficulties faced by most of the groups engaged in the study of PL and EL properties of the material [Koshida and Koyama 1992].

However, the electrical and optical properties of PS were found to be changed by the presence of many gases such as methanol, ethanol, propanol, acetone, benzene, CO, and NO_2 [Angelucci et al 2000, Bilenko et al 2000, Boarino et al 200, Bogue

1997, Luth et al 2000, Schechter et al 1995, Thust et al 1999]. This phenomenon has been exploited to develop gas sensors for such gases. Schechter et al (1995) have used the PS conduction properties for organic vapour sensing (methanol and benzene vapours) and they found that the forward current amplitude rose with increasing vapour concentration for various thicknesses of PS layers. The increase in current was ascribed to the reduction of the PS layer resistance with increase of vapour concentration. Anderson et al (1990) and Schwarz et al (1995) have argued that the change in the electrical properties of PS is due to liquid condensation inside the microcapillaries of the PS. This leads to an extra current flowing through the liquid enhancing of conductivity. The activation energy was found to decrease due to the introduction of an organic vapour to the sample, but the conductivity pre-factor (σ_o) is not affected [Schechter et al 1995]. Under vacuum condition, a constant activation energy of (0.49 eV) was found over the temperature range of (200-300 K) indicating that the Fermi level is pinned at a fixed point with respect to the band edge. The exposure of the sample to organic vapours injects extra carriers into the PS and shifts the Fermi level to a new position closer to the band edge. Other researchers used the electronic properties of meso-PS samples for gas sensing [Ben-chorin et al 1994, Mares et al 1995]. The silicon structure in these samples are larger (mesoporous silicon) and therefore quantum size effects are negligable and allow the use of PS as a usual semiconductor [Goudeau et al 1989, Lehmann and Gösele 1991]. The main difference between mesoporous silicon and a crystalline silicon is the large surface area of the PS (more details will be discussed in chapter 4). Ben-chorin et al (1994) reported that the current-voltage profile of all PS samples is approximately symmetrical with respect to zero voltage for a vacuum or nitrogen atmosphere. For low benzene or methanol concentrations the behaviour remains ohmic with an increase

in current amplitude. Exposure of a PS device to a high concentration of an organic vapor makes the current-voltage characteristic tend to a rectifying behaviour. The change of the behaviour from ohmic to rectifying one was imputed to the electrical structure of the device which is described as a serial combination of a resistor (PS layer) with a pn junction (between PS and the silicon substrate). At low vapor concentrations, the PS resistance remains very high that it limits the current flow, resulting in ohmic current-voltage behaviour. At higher concentrations, the PS resistance is much reduced and the current in the reverse bias is limited by the pn junction, giving rise to rectifying current-voltage response. However, under forward bias, the limiting element is the PS resistance, and thus, the sensing characteristics should be measured with a forward bias.

Gas sensors for water vapour using PS have been also investigated [Anderson et al 1990, Foucaran et al 2000, Mares et al 1995, Motohashi et al 1995]. In all humidity sensors, the capacitance of the sensors was measured against humidity and found to increase with increasing humidity. This variation of capacitance with increasing humidity was related to the modification of the dielectric constant of the PS sample in the presence of water (as the dielectric constant of water is 80).

CHAPTER THREE

EXPERIMENTAL APPARATUS AND MEASUREMENTS TECHNIQUES

3.1 Introduction

This chapter describes all the experimental work involved in this project. The first part of the chapter deals with the formation process of porous silicon (PS) including the fabrication setup for use in a clean room environment and the evaporation process used to deposit metal contacts on the PS layers and on the back side of the silicon substrates. Finally, the electrical and photoelectrical characterisation system is discussed briefly.

3.2 Porous silicon formation

3.2.1 Design the fabrication setup

PS is made by anodic etching of silicon in hydrofluoric acid (HF). As silicon is not normally attacked by HF acid, it is necessary to apply an electrical voltage to achieve electrochemical desolution on the silicon surface. An electrochemical cell has been designed (by the author) for this purpose to accumulate silicon samples in the range up to 2 inch diameter. The cell is made from Teflon (PTFE) to be chemically resistant to the HF acid. The size of the cell is (85 mm (L) x 85 mm (W) x 70 mm (H)) which is attached from the upper edges to PTFE shoulders to provide support to the cell to be mounted inside an ultrasonic oscillator. The cell contains two electrodes (anode and cathode) each immersed in the HF acid and connected to an external current supply to

provide the current density required for the anodisation. Coiled platinum wire 200 mm in length and 0.5 mm in diameter is used as a cathode whilst the silicon wafer acts as an anode. The area of the platinum coil was chosen to be larger than the silicon wafer area (more than double) in order to give enough ionic exchange during the anodisation. A baffle plate (porous PTFE sheet) is fitted in the middle of the cell in order to control the speed of the ionic exchange between the electrodes which increases the electrochemical etching efficiency. This porous plate is usually used for etching with high current density and /or low HF acid concentration [Jung et al 1992, Richter et al 1992, Sugiyama and Nittono 1989, Takasha and Seki 1978,]. Figure 3.1 shows the schematic diagram of the fabrication setup designed and operated in the clean room.

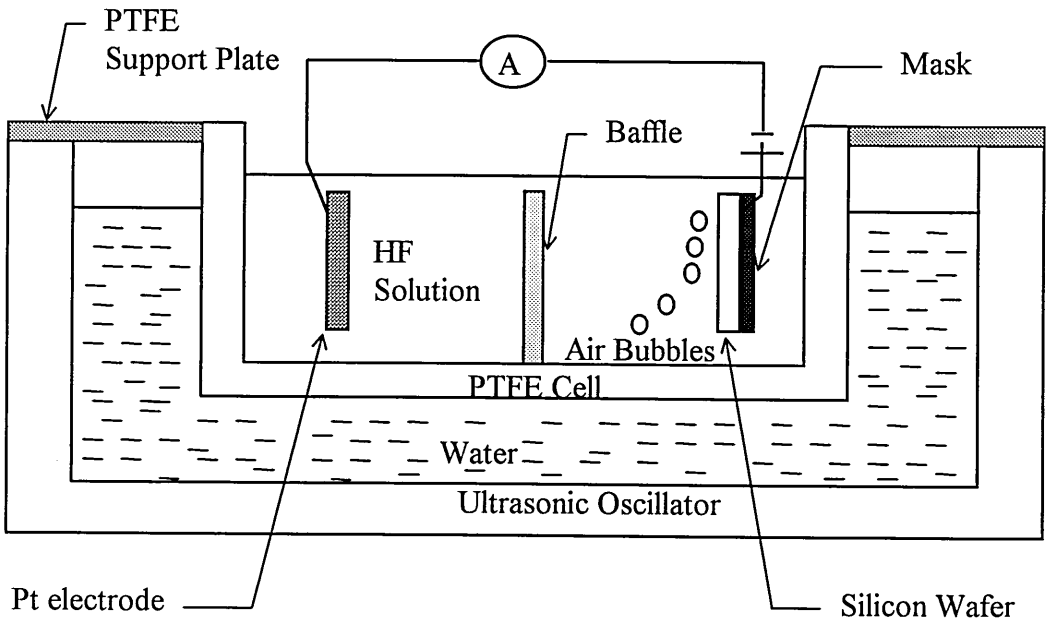


Figure 3.1 Schematic diagram of PS fabrication setup

3.2.2 Porous silicon formation process

The silicon substrates used for the fabrication of PS were 3 inch (100) p-type silicon wafers with 8-12 Ω.cm resistivity and 500 μm thickness. Very high resistivity (350 Ω.cm) silicon wafers were also used for some samples. The 3 inch silicon wafers were cut into small pieces (average of 0.5 cm^2) to produce as many as 20 pieces of substrates ready to be used at any time.

Prior to the first stage of the fabrication process it is important to clean the silicon substrates from any grease, dust, organic layers and naturally occurring oxide layer on the surface. The initial cleaning procedures were as follows:

(I) Fifteen minute ultrasonic wash in deionised water (or Isopropyl alcohol to remove any organics or grease on the surface of the wafers).

(II) The substrates were then taken for two minutes contact etching using very weak HF acid solution (10:1) to remove the naturally occurred oxide layer.

(III)The silicon substrates were then thoroughly washed with flowing water for at least 5 minutes and dried by exposing them to a nitrogen gas flow.

(IV)The silicon substrates were wrapped in a clean fiber-free tissue and stored in separate containers until required.

In order to provide a uniform current distribution during the anodisation, thin aluminium (Al) films were deposited on the backside of the substrates wafers and annealed at 350 °C for 30 minutes to form ohmic contacts. The evaporation process for depositing the Al films involves boiling and then evaporating a small amount of Al from a heating element. The process is performed under high vacuum (10^{-6} Torr) and the Al is evaporated very slowly. The deposition system and techniques will be explained in more

detail later in this chapter. The thickness of the Al films were in the range of (250-350 nm) for all the samples.

To protect the Al layers from HF acid attack, the backside of the wafers and the area not to be anodised were covered with an acid proof wax (black apiezon wax was used for most of the samples) or with insulating adhesive tape like PTFE tape. Usually, when using PTFE tape the HF acid penetrated through the PTFE tape edge and etched an area of the silicon substrate which are not desired for etching and, some time, reached the backside of the substrate etching away the Al layer on the backside. In order to avoid this problem, the edge of the desired silicon window (in other words, the edge of the PTFE tape) was covered with acid proof wax, as shown in Fig. 3.2. After waxing the silicon window was cleaned again from any wax particles using a wet clean fiber-free tissue.

HF acid in different concentrations (10%-30%) were used as the anodisation electrolyte either mixed with water or with ethanol with a view to reduce the size of the generated bubbles. The different concentrations of HF acid were tried in order to study the effect of the concentration on the PS layer. Low concentration HF acid (less than 10%) was used for some samples to study the structural difference when using low concentration HF acid (see chapter four). One of the problems associated with the fabrication of PS is the formation of large bubbles due to the desolution process. To avoid this problem, ethanol was mixed with the HF acid to reduce the size of the bubbles and an ultrasonic oscillator were used to sweep the bubbles away from the silicon wafer surface [Venkateswara et al 1991, Vial et al 1992, Koshida and Koyama 1993, Ben-Chorin et al 1994, Gesele et al 1997, Mathur et al 1998].

An external current supply provided the required constant current density during the anodisation process which was in the range of 10-50 mA/cm^2. Usually, the anodisation current density was adjusted to be below that used for electropolishing. An external variable resistor was used to control the current flow during the anodisation. The anodisation process was performed in the dark to control the number of electronic holes available on the silicon surface. Different anodisation times were used to produce PS layers with different thicknesses. For most of the samples, the anodisation time was between 5-30 minutes in order to minimise extra silicon desolution by chemical attack of the already formed PS layers.

After fabrication, the samples were detached from the PTFE tape and cleaned carefully from the wax (using acetone)and then thoroughly washed with flowing high purity water for at least 10 minutes and dried by exposing them to a nitrogen gas flow.

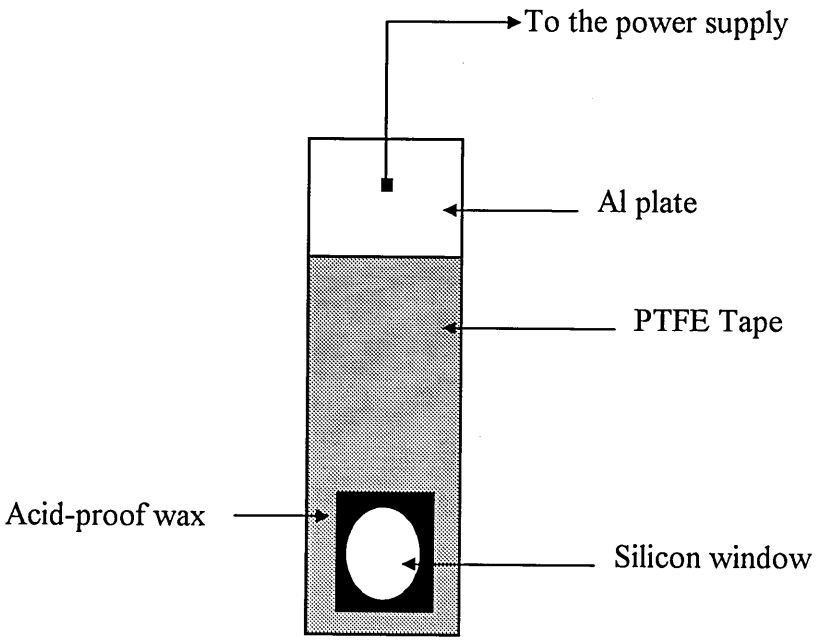


Figure 3.2 Schematic diagram of the anode used in PS formation process.

Some of the samples were stored in the dark for several months and the others were directly transferred to a vacuum chamber to deposit a metal contact on top of the PS layer.

The fabrication process described above involves a highly concentrated HF acid which is a very dangerous chemical to handle without extra training and appropriate protection. For this purpose, all the chemical procedures involved using HF acid were performed in a fume cupboard and operators were advised to wear appropriate protective clothing (coat, gloves, and protective glasses). Training in handling the chemicals and a full risk analysis was conducted to ensure that risks were minimised.

3.3 Electrical contacts

In order to measure the electrical and photoelectrical properties of the PS film, it is necessary to apply metal electrodes to the film surface. Evaporation techniques were used to deposit metals on top of the PS layers. It is important to choose the appropriate metal electrode for the required structure characterisations of all materials. Knowledge of the work function of the metal electrode is required to establish the type of contact to be made to the PS layers. As the PS device structure is not fully understood, aluminium or gold electrodes were used for all the PS samples. Different thicknesses of metal films were fabricated for comparison. The thickness of the top electrode varying between 50-150 nm depending on the type of the measurements. For photoelectric measurements, 50-60 nm thick gold electrodes were used to make a semitransparent layer on top of the PS layers. A masking system was used for all contacts to determine the electrode configuration and dimensions in order to give an accurate device action area. The final device active areas were on average 0.2-0.5 cm^2.

Thin copper wires were attached to the device electrodes using a silver conducting paste to provide the electrical connection between the measuring equipment and the devices. A diagram of the device structure used for identification of the electrical and photoelectrical properties of PS is shown in Fig. 3.3.

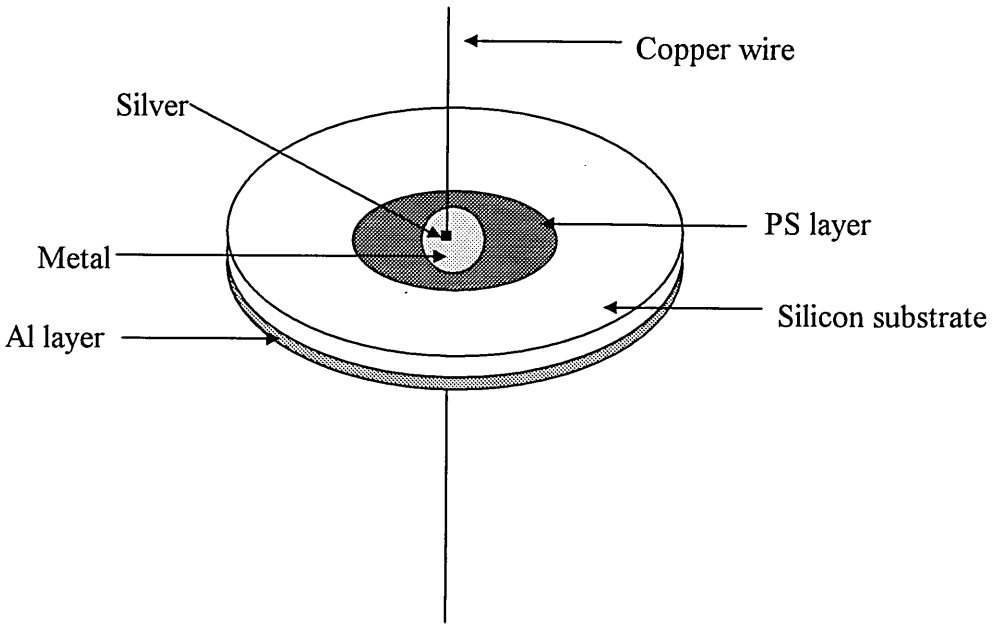


Figure 3.3 Device structure for the electrical properties measurements of PS

3.3.1 The evaporation system

Thin aluminium and gold films for all electrical and photoelectrical investigations were constructed using (the previously discribed) thermal vacuum evaporation technique. An Edwards Bir-Vac coating unit was used for the deposition of Al on the backside of the silicon substrate (before the anodisation) and for the subsequent

deposition of metal on the top of the PS layer (after anodisation). The coating unit consists of a vacuum system, coating chamber and external current supply to provide the required current for heating the evaporation source, as shown in Fig. 3.4. Vacuum gauges were connected to the coating unit in order to measure the backing pressure, Pirani gauge, and the pressure inside the vacuum chamber, Penning gauge. The vacuum system is a combination of a rotary pump and a diffusion pump working together to produce an ultimate vacuum of about 10^{-5} torr. The rotary pump was initially used to create a vacuum of 10^{-1}-10^{-2} torr to produce a backing to the diffusion pump as well as roughing the coating chamber to a vacuum level of about 10^{-1} torr. The diffusion pump contained a heating element in the base to boil the silicon oil which then condenses on water cooled metal plates. Usually the diffusion pump pulls the vacuum in the chamber to about 10^{-6} torr via the high vacuum valve.

A quartz crystal monitor system was connected to the coating system in order to monitor the evaporation rate and the evaporated electrode thickness. This system depends on measuring the change in the resonance frequency of the quartz crystal oscillator which is proportional to the mass of the material deposited on the crystal. The quartz crystal monitor (No.13 in Fig 3.4) was placed very close to the sample substrate so that the material deposited onto both of them at the same rate in order to produce high accuracy measurements. The thickness of the deposited electrode can be calculated from the frequency comparison between the monitor crystal and a reference crystal. The acoustic impedance (in g cm^{-1} sec^{-1}) and the density of the evaporated material (in g cm^{-3}) were input to the thickness monitoring system in order to enable the system to calculate and display the evaporated electrode thickness in Angstroms(10^{-10} m).

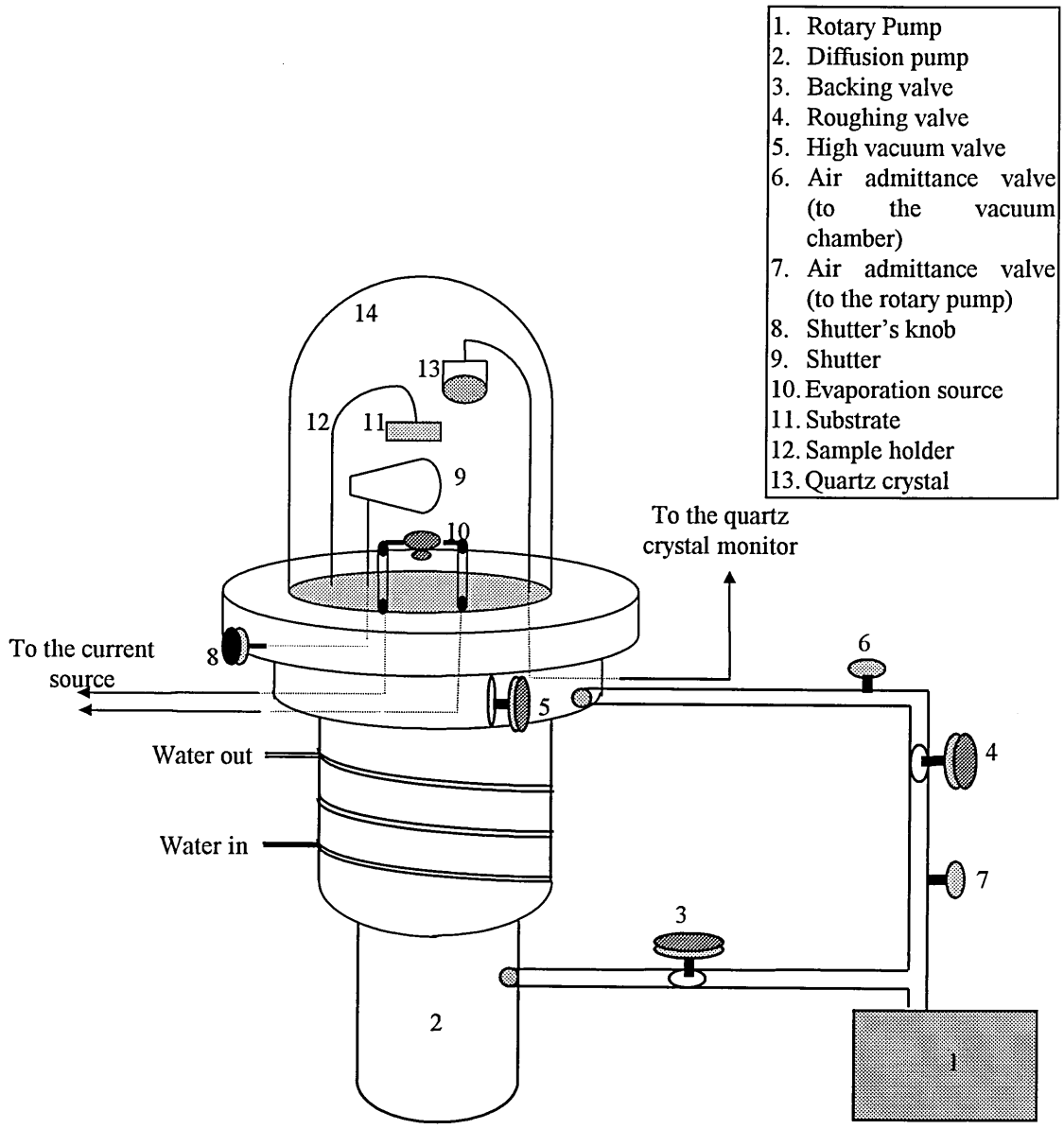


Figure 3.4 Schematic diagram of the coating system

In order to avoid any low boiling impurities and contamination of the evaporated layer, a mechanical shutter was used to separate the sample substrate from the heating source. An external current supply was connected to the coating unit in order to supply the required current for heating the evaporation source. This current supply is automatically switched on when the pressure in the vacuum chamber is of about 10^{-5} torr.

3.3.2 The evaporation procedure

Deposition of Al and Au contacts on the PS layers (or the back side of the silicon substrate) were performed using the evaporation system described above. Before the evaporation process the interior of the deposition chamber (all the parts inside the vacuum chamber) were cleaned to prevent any risk of contamination of the evaporated films.

Aluminium or gold wires (depend on the device structure and the purpose of the measurement) were evaporated onto the PS layer through the mask using the evaporation heating source. The evaporation sources used for depositing Al and Au are shown in Fig. 3.5. A tungsten filament was used as the evaporation source for depositing Al electrodes, while a molybdenum boat was used for Au electrodes .

The electrode size and pattern were achieved using a mask placed directly in front of the freshly made PS sample. The mask was made from a very thin metal plate with holes of different shapes and sizes. The PS sample was then placed inside the vacuum chamber close to the quartz crystal monitor and the pumping sequence was then initiated. When the vacuum chamber reached about 10^{-5} torr the current supply was then

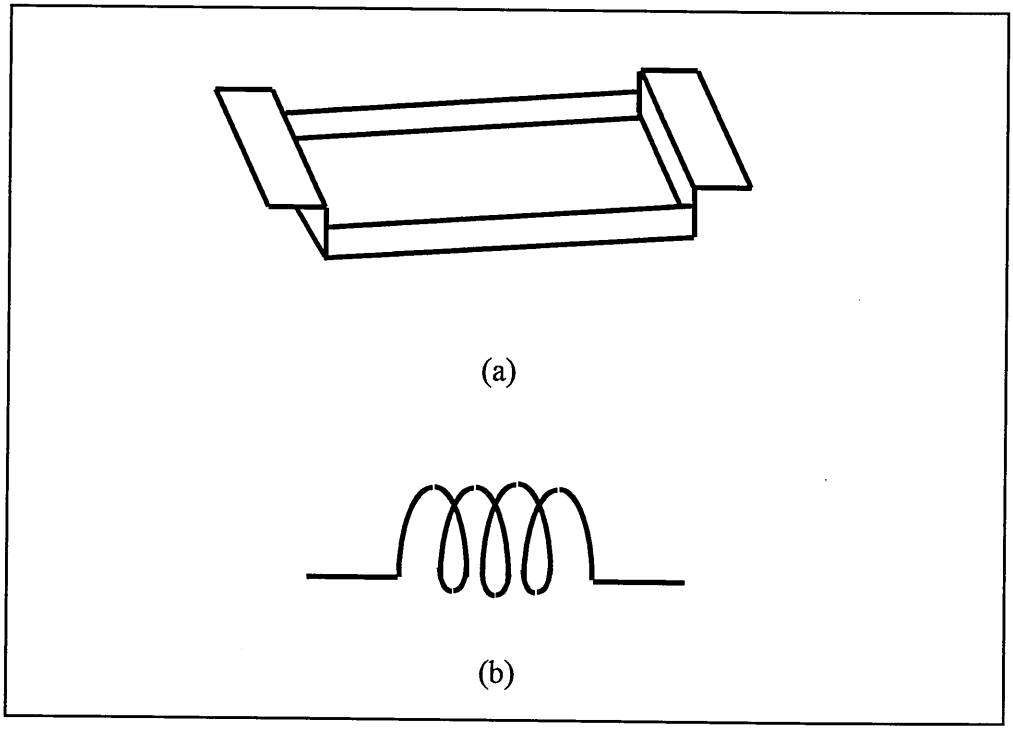


Figure 3.5 Evaporation sources to evaporate (a) Au and (b) Al

automatically switched on and the current to the evaporation source slowly increased until the evaporation rate reached about 10 nm/Sec..

The shutter was then removed and the evaporation process took place at a carefully controlled slow rate. The rate of the evaporation was sustained at about 1 nm $sec.^{-1}$ for all electrodes. When the evaporated electrode reachs the required thickness the shutter was closed to prevent further deposition on the electrode. Directly afterward, the evaporation process terminated by switching off the external current supply. The system then cooled down for at least 15 minutes and then the high vacuum valve closed before opening the air admittance valve to the vacuum chamber. The sample is now ready to be taken off for more treatments or for measurements.

3.4 The measurement systems

Most of the work required in this project focused on the elucidation of the mechanisms responsible for the current transport through PS-based structured. This involved the measurement of electrical and photoelectrical properties of these structures at different temperatures. The electrical characterisations were performed on different PS samples throughout these studies implied DC and AC characterisations for the temperature range between 77 and 300 K (room temperature).

For the convenience of the measurements, a Farnell SW1B IEEE-488 switching unit was used to allow a suitable connection for the measuring equipment to an IBM-PC. A National Instrument IEEE GPIB interface card was installed in the IBM-PC to control all the measuring equipment with the exception of the temperature controller. DC characteristics were performed between -3V to 3V with a 0.05V step size. Using a computer controlled system, the a.c. conductance, capacitance and the dielectric constant of PS were measured at semi-logarithmic preset steps in the frequency range of 20 Hz - 1 MHz. The software is designed to address the measuring instruments to perform the characterisations at any selected temperature between 77 K and 300 K or sweep the temperatures between 77 K - 152 K in 5 K steps, and from 152 K to 292 K in 10 K steps.

The PS-based devices were mounted in an Oxford Instruments liquid nitrogen cryostat (Fig. 3.6). The cryostat was connected to an ITC4 Intelligent temperature

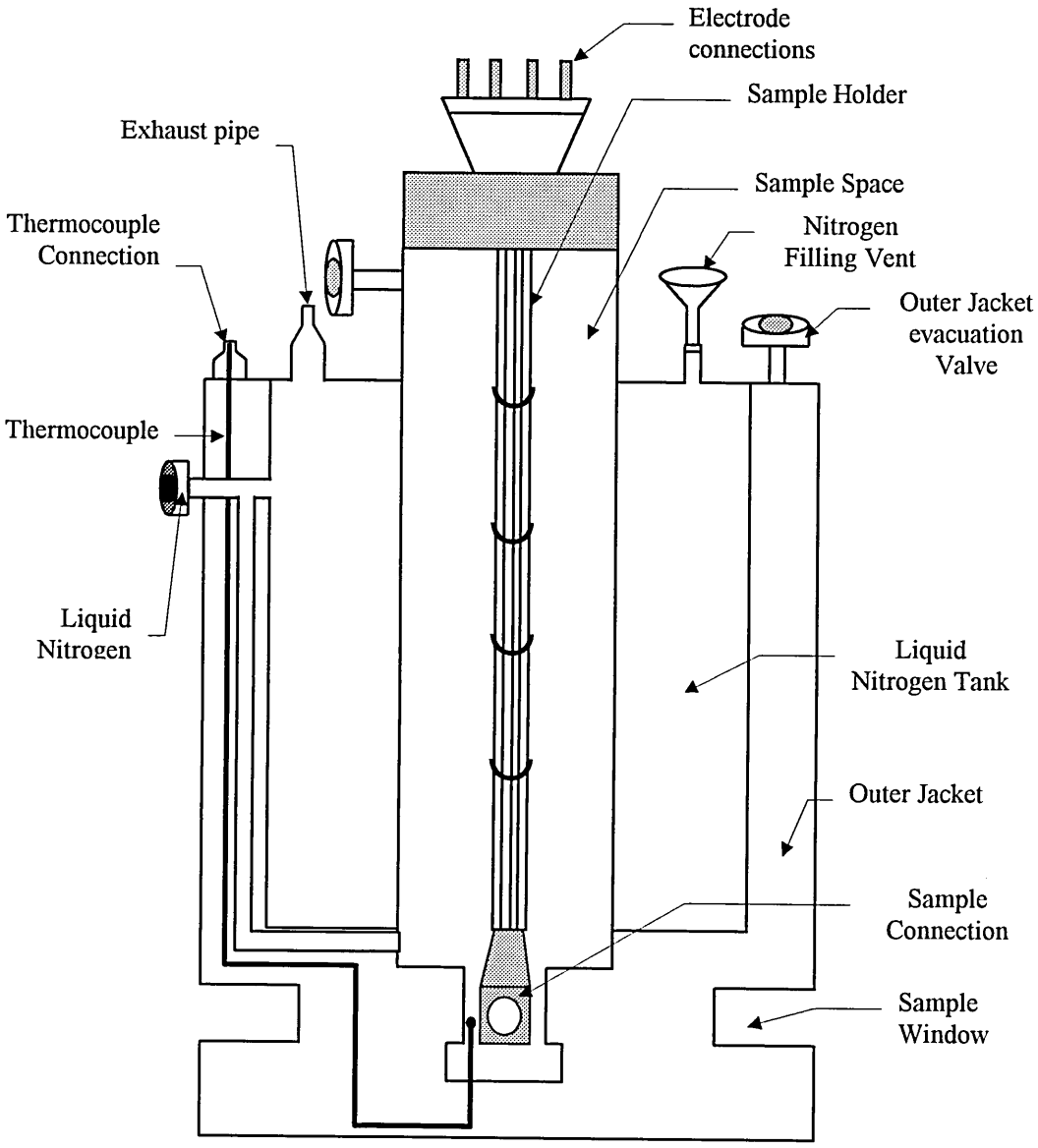


Figure 3.6 Cross sectional view of the liquid nitrogen cryostat

controller to allow the measurements to be taken at different temperatures. A thermocouple is located in the sample heat exchange area supplied with the cryostat as a temperature probe and connected directly to the temperature controller. The temperature controller was driven by the IBM-PC computer through its serial communication port. The cryostat was designed with a sample window for optical and photoelectrical measurements. However, the cryostat was also used to keep the sample in a clean and dry environment to prevent any humidity effects on the device.

3.4.1 Electrical measurements

The DC current - voltage $I(V)$ measurements were performed by applying a voltage across the PS-based sandwich structure and measuring the current passing through the structure. All the measurements were taken in the dark as the samples were mounted in the cryostat and the sample window closed to prevent any affect of the light on the measured current. A Keithley 617 digital electrometer was used as an ammeter with built-in voltage source to record the current (I) as a function of the applied voltage (V). The electrometer is capable of measuring currents in the range of 1 pA (10^{-12} A) to 2 mA, and supplied with a voltage source capable of supplying a d.c. voltage of -100 V to 100 V with minimum steps of 0.05 V.

For the AC measurements, the samples were connected to the sample holder mounted in the cryostat as for the DC measurements. The capacitance, a.c. conductance and the loss tangent were measured as a function of frequency using Hewlett Packard 4284A LCR meter over the frequency range 20 Hz - 1 MHz. The peak-to-peak voltage of the applied signal did not exceed 100 mV (the instrument is capable of applying a peak-to-peak signal as high as 20 V).

Experimental data over a wide range of temperatures were analysed in order to extract more information about the carrier transport mechanisms and the dielectric properties of the material. Therefore, all the above electrical measurements were performed at different temperatures between 77 K and 292 K (room temperature). Liquid nitrogen was introduced into the cryostat system to reduce the temperature of the sample to as low as 77 K. The temperature of the samples was controlled and recorded by the ITC4 temperature controller. A time delay (usually 10 seconds) was introduced between the recording of data at a particular temperature to reduce the effect of the polarisation of the sample and give the current enough time to stabilise. Another 10 minutes delay time was introduced between each temperature measurement to make sure that the temperature of the sample was stabilised. A schematic diagram of the electrical measurement system is shown in Fig. 3.7.

3.4.2 Photoelectrical measurements

For photoelectrical measurements a monochromatic system is used to illuminate the sample with light at a desired wavelength. The sample was connected firmly to the sample holder of the cryostat to control the environment (temperature, and level of illumination) of the samples and the light shone through the sample window of the cryostat. The measurement system consists of a radiation source, spectrometer, and wavelength minidrive, in conjunction with the electrical measurement system shown in Fig. 3.8.

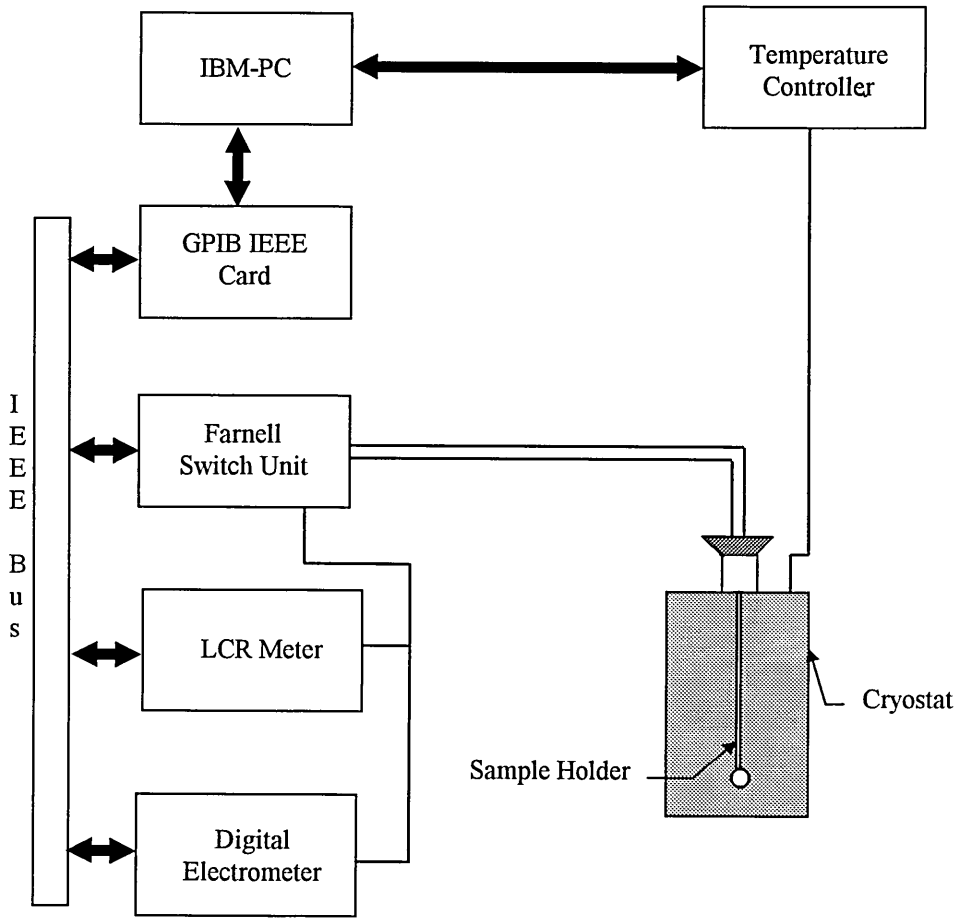


Figure 3.7 Schematic diagram of the electrical characterisation System.

An SPEX 1682 broad band radiation source was used as the illumination source over a wide range of wavelengths. The radiation source contains an incandescent lamp (1683L tungsten/halogen type) which supplies illumination between 300 and 3000 nm covering the wavelength range of interest of these studies (300-1100 nm). Stable intensity of light was ensured by sampling the lamp intensity through a fiber optics cable and feeding it back to an optical feedback circuit that controls the current applied to the lamp by the 1683p power supply. A SPEX 1681 spectrometer was used in conjunction with 1673 minidrive to provide and control the desired wavelength respectively.

The Keithley 617 digital electrometer was used to measure the dark current and the current under illumination. The photocurrent is the different between the two currents as:

$$I_{ph} = I_{ill} - I \tag{3.1}$$

where I_{ph} is the photocurrent, I_{ill} is the current under illumination and I is the dark current.

All the photoelectrical measurements were performed under a wide range of temperatures. Like the electrical measurements liquid nitrogen was used for low temperature experiments.

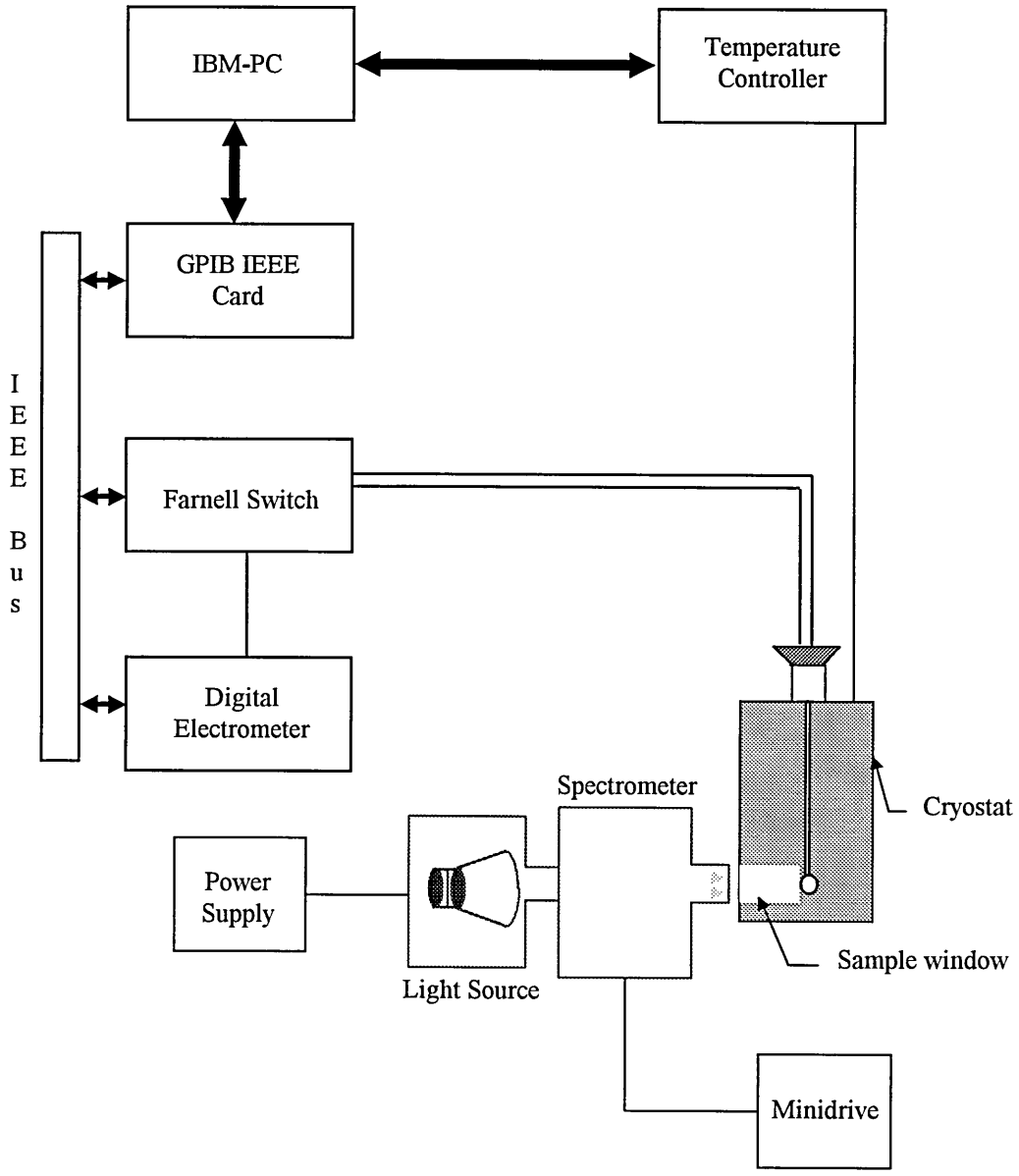


Figure 3.8 Schematic representation of the photoelectrical characterisation system

CHAPTER FOUR

MICROSTRUCTURE AND FORMATION MECHANISM OF POROUS SILICON

4.1 Introduction

Before studying the electronic properties of porous silicon (PS), it is very important to understand the electrochemistry of pore formation and the structural properties of the material. This chapter reports some of the models for the formation of PS. The effect of the silicon substrate resistivity, current density, and hydrofluoric (HF) acid concentration and the anodisation time is discussed in detail. Scanning electron microscopy (SEM) of PS layer surfaces and micrographic pictures of the cross section of PS/Si interface are also presented in this chapter.

4.2 The principles of anodic oxidation

Anodic oxidation (anodisation) is a process traditionally used for producing protective films on aluminium sheets. This process basically depends on the production of an oxide layer on the aluminium sheet by passing sufficient current through a suitable electrolyte in which the aluminium is the anode and a suitable material (like lead or platinum) acts as the cathode [Brace 1968]. This procedure required:

1. A direct current source.
2. Acid solution to provide oxygen ions. Different acids could be used with different concentrations.

When the current is applied to the electrochemical cell , with the anode connected to the positive terminal of the direct current source and the cathode connected to the negative terminal of the current source, the acid solution will start to decompose. Hydrogen will be produced at the cathode and oxygen ions (negatively charged) will be attracted to the anode. Most of liberated oxygen ions combine with the aluminium to form the oxide layer on top of the aluminium surface as shown in Fig. 4.1. The general equation describing the oxidation process of aluminium can be written as:

$$2Al + 3O^{2-} + 6h^{+} \rightarrow Al_2O_3 \qquad (4.1)$$

The thickness of the oxide layer is directly proportional to the current density and the anodisation time. However, the progress of the formation of oxide layer depends on the chemical composition and the concentration of the acid solution used during the anodisation [Henley 1982]. Some of the anodising solutions have no solvent action on the oxide layer and as a result the anodisation process will be automatically terminated in a very short time. For thick oxide layers, acid solutions with some solvent action should be used (like hydrofluoric acid and sulphuric acid) to produce porous oxide layers.

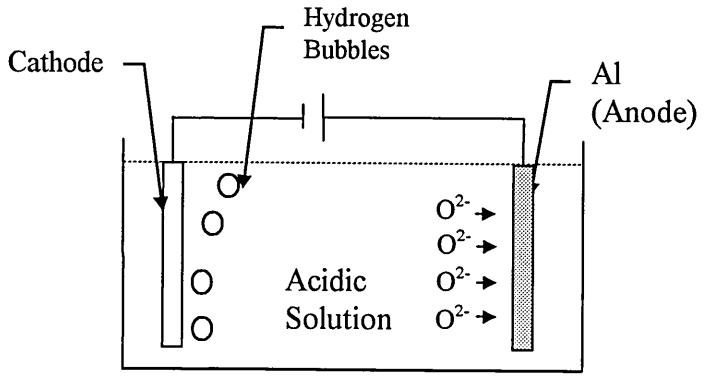


Figure 4.1 Aluminium oxidation cell

At the beginning of the oxidation process a thin oxide layer is built up on the anode and the electrolyte starts dissolving this layer, at millions of points per square centimetre, quickly resulting in producing very small holes (pores) in the oxide layer. These will continue to exist unless there is some major change in the anodisation conditions. If a constant voltage is applied, the anodising current will fluctuate and present problems in achieving the desired thickness. Therefore, to prevent this problem, a constant current density is usually used to produce the desired thickness of oxide layer.

The porous silicon formation process is essentially similar to the porous alumina (aluminium oxide) formation process described above [Parkhotik et al 1983]. In PS formation the etching process takes place on the silicon substrate (the anode) instead of building up an oxide layer.

4.3 Porous silicon formation mechanism

The silicon surface is known to be very inert against attack of hydrofluoric acid at any concentration. With no aid, the rate of the HF acid etching of a silicon surface is about few nanometer per hour [Rees 1991]. But this process can be accelerated and the silicon substrate can be quickly chemically dissolved in HF if anodic bias is applied to the silicon substrate to provide electronic holes. In a similar fashion to the formation of aluminium oxide, the process starts with building a very thin silicon oxide layer on the surface whose thickness is proportional to the applied voltage. Once this limiting thickness is approached the HF acid starts etching this layer at some points. The number of pores is directly proportional to the doping level for a fixed HF acid concentration and current density [Bomchil et al 1983, Beale et al 1985, Herino et al 1987]. Accordingly, It is generally assumed that the initial pore formation starts due to the

inhomogeneities in the interface between the silicon substrate and the HF acid solution [Zhang 1991, Barret et al 1992, Teschke 1994]. However, it was found that the density of PS increases with increasing the current density and decreasing the HF acid concentration [Bomchil et al 1988]. However increasing the current density is limited by the critical value of the electropolishing current which depends on the HF acid concentration.

Although different theories have been proposed for the formation mechanism of PS, a number of points are still not clearly understood. One of the remarkable features of PS layers is the resistance of the silicon wires (the walls between the pores) against further chemical etching of the electrolyte, if the formation took place in the dark for p-type silicon substrates. The principles of the formation and the surface dissolution mechanism of PS will be presented in this section.

The surface of silicon is usually positively charged due to the presence of surface states on the silicon surface. Therefore, the surface is expected to be depleted of electronic holes. If electronic holes are introduced to the silicon surface through heavily doping for the p-type substrate or illumination for the n-type samples, the anodic oxidation will start to build up a very thin silicon dioxide layer. At this point, the fluoride ions start to attack the oxide layer (expected to be at the places of the surface where there are electronic holes only) etching very small holes (pores). Hence, the top of the new surface structure (porous structure) becomes depleted of electronic holes and is consequently passivated. If there are no more electronic holes introduced to the surface, the structure is virtually inert against further attack of fluoride ions. However, electronic holes are available at the pore tips, causing the current to flow down through the electrolyte into the pores producing anodically oxidised layer at the pore bottoms [Unagami and Seki 1978]. The fluoride ions attack the new oxide layer making the pore

size bigger and the bulk silicon wire thinner as shown in Fig. 4.2. This process is a self adjusting process as it will be terminated when the walls between the pores (silicon wires) are completely depleted of electronic holes. The condition for this complete depletion of electronic holes is that the thickness of the silicon wires should be smaller than two times the depletion region. The anodic etching will continue at the same progress rate as long as there is no change in the fabrication conditions.

The above model is supported by the fact that PS layers formed from heavily doped silicon substrates have different microstructure from the ones formed from lightly doped substrates [Teschke 1994, Beale et al 1985]. The pore size is found to increase with decreasing the doping level, while the number of pores increases with increasing doping level. The carrier tunnelling process (through the barrier between the silicon substrate and the electrolyte) is found to be responsible for the current flow during the anodisation of heavily doped substrates. The maximum current flow occurs at the pores tip as the depletion width is at a minimum at that points [Beale et al 1985]. For lightly doped substrates, the current flow during the anodisation was ascribed to the thermionic emission of the carriers over the barrier between the substrate and the electrolyte. The rectifying behaviour of the current-voltage characteristics of metal/PS/P-Si/Al structures is found to be due to the pn junction between the silicon substrate and the PS layer (see chapter 5 for more details). These results also indicate that there is a depletion of holes in the PS region because the PS acts as n-type material. The electronic hole depletion mechanism responsible for microporous silicon formation was also studied according to the energy band gap structure of this material.

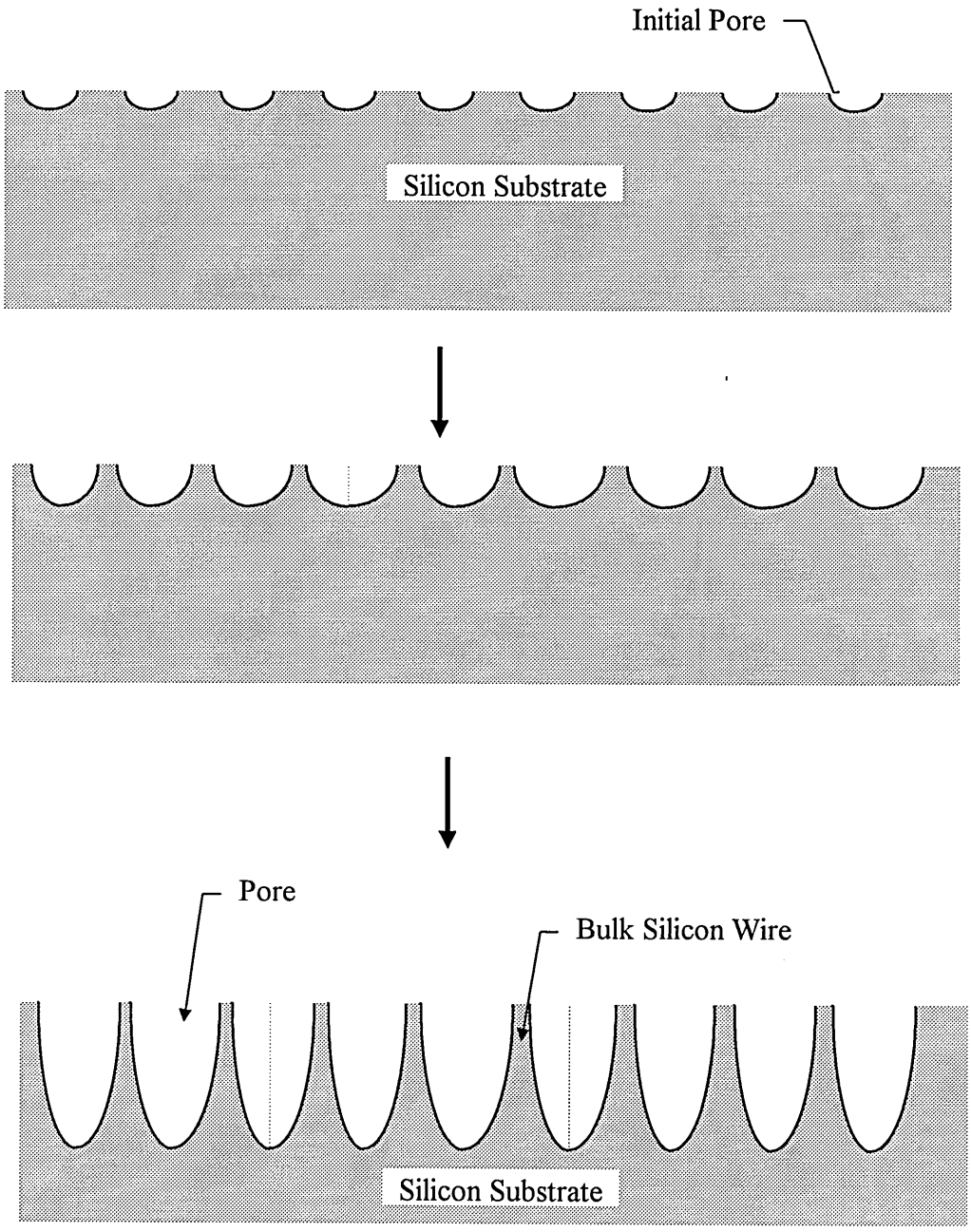


Figure 4.2 Schematic diagram of the formation steps of porous silicon

The light emission of microporous silicon in the visible range [Canham 1990] indicates that the band gap of this material is increased by about 0.5 eV above the accepted value of 1.2 eV for a crystalline silicon [Lehmann and Gösele 1991]. Lehmann et al (1992) proposed the existence of a hetrojunction between the PS layer and the silicon substrate. Figure 4.3 shows the band diagram of the PS-bulk silicon interface according to this model. The electronic holes in the bulk silicon region require an extra energy (E) to move into a wall between two pores in the PS region, whereas there is no additional energy necessary to penetrate the electronic holes into the pore tip. At the beginning of the formation, the silicon wires are large in size and imply a low energy barrier for holes. This allows more holes to penetrate into the wall and initiate further electrochemical dissolution of the silicon wires. This process will continue thinning the silicon wires until the band gab of the PS layer reachs a value at which electronic holes cannot, any more, enter the silicon wires from the bulk silicon. At this stage of the formation, the silicon wires become completely depleted of electronic holes and the HF acid etching of the walls will be terminated. At the same time the electrochemical dissolution continues at the pore tips which leads to an increase in the thickness of the PS layer as the electrochemical process continues. Thinner silicon wires can be produced by increasing the anodic current which consequently increases the energy of the electronic holes. This will increase the number of electronic holes which take part in the electrochemical dissolution of the silicon wires and increases the band gap of the PS layer. This theory is supported by the fact that the photoluminescence spectra shift from red towards the blue with increasing current density (with all the other fabrication conditions held constant) [Koshida and Koyama 1991, Lehmann et al 1992, and Voos et al 1992]. The blue shift of the emitted light can be due to an increase in the energy band gap of the PS layer.

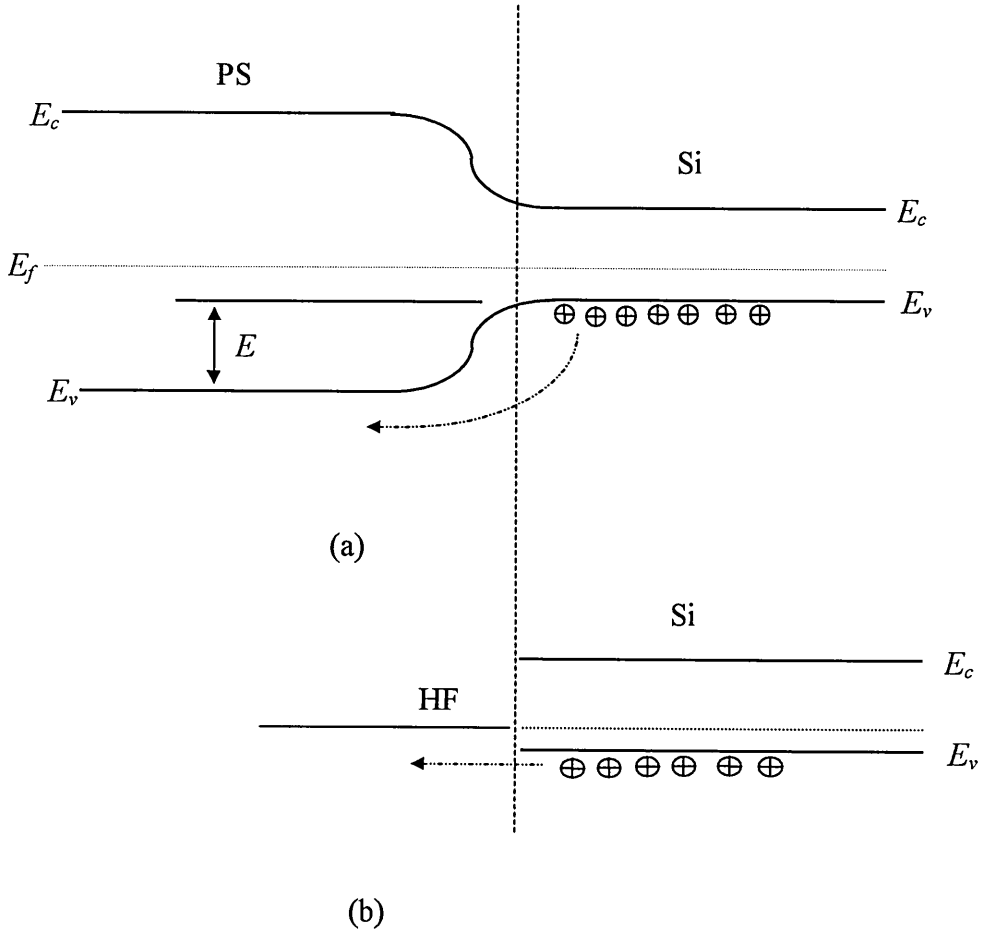


Figure 4.3 The band diagram of the interface between the silicon substrate and the PS layer at (a) silicon wire and (b) pore tip area.

4.4 Silicon surface dissolution chemistry

It is generally accepted that electronic holes are required in the initial oxidation step and subsequent dissolution process of silicon in HF acid, as in the case of electropolishing or porous silicon formation. The final and stable product for silicon in HF acid appears to be H_2SiF_6, regardless of whether electropolishing or pore formation occurs. However, the exact nature of the reactions responsible for the transition of silicon from a divalent to tetravalent are still under investigation [Turner 1962, Memming and Schwartz 1966, Unagami 1980, Zhang et al 1989, Belyakov et al 1993].

During the PS formation process there are two main chemical stages which appear to take place. The first stage is a purely electrochemical stage and related directly to the transfer of charge across the interface between the electrolyte and the semiconductor (HF-Si interface) [Belyakov et al 1993].

$$Si + 2HF + 2h^+ \rightarrow SiF_2 + 2H^+ \tag{4.2}$$

The second stage of the formation process is a chemical reaction that change the unstable silicon difluoride into a stable tetravalent form. There are two possible reactions which could be responsible for this stage, and these are:

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \uparrow (Bubbles) \tag{4.3}$$

and then a rapid reaction to produce H_2SiF_6:

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \tag{4.4}$$

or

$$SiF_2 + 2H_2O \rightarrow SiO_2 + 2HF + H_2\uparrow (Hydrogen\ Bubbles) \quad (4.5)$$

followed by a rapid reaction as:

$$SiO_2 + 4HF \rightarrow H_2SiF_6 + 2H_2O \quad (4.6)$$

It should be noticed that hydrogen is produced in both cases. This has been observed experimentally as large bubbles. The size of these bubbles can be reduced by increasing the ethanol concentration in the electrolyte as explained in chapter three. The above chemical reactions (equations 4.2 to 4.6) do not present the electrochemical dissolution in detail rather they focus on the first step of the reaction. Assuming that the silicon surface is covered with fluorine atoms, when a voltage is applied across the interface, electronic holes will move toward the surface (for p-type silicon substrate). One of the electronic holes trapped at the surface is the result of breaking a silicon-silicon bond as shown in Fig. 4.4 in step (a). The SiF_2 group swing away from the silicon atom which trapped the electronic hole (step (b)). With the presence of sufficient HF acid molecules, an HF molecule reacts immediately to form a bond with the corresponding silicon atom as demonstrated in step (c) in Fig. 4.4. Due to the instability of the SiF_2, the breaking up of the second Si-Si bond is a rather fast process. For this last reaction step another electronic hole is used up to split the SiF_2 group away from the silicon atom [Memming and Schwandt 1966]. As the applied voltage increases the more electronic holes are available at the silicon surface. This results in more dissolved silicon atoms and accordingly increases the number of pores on the silicon surface.

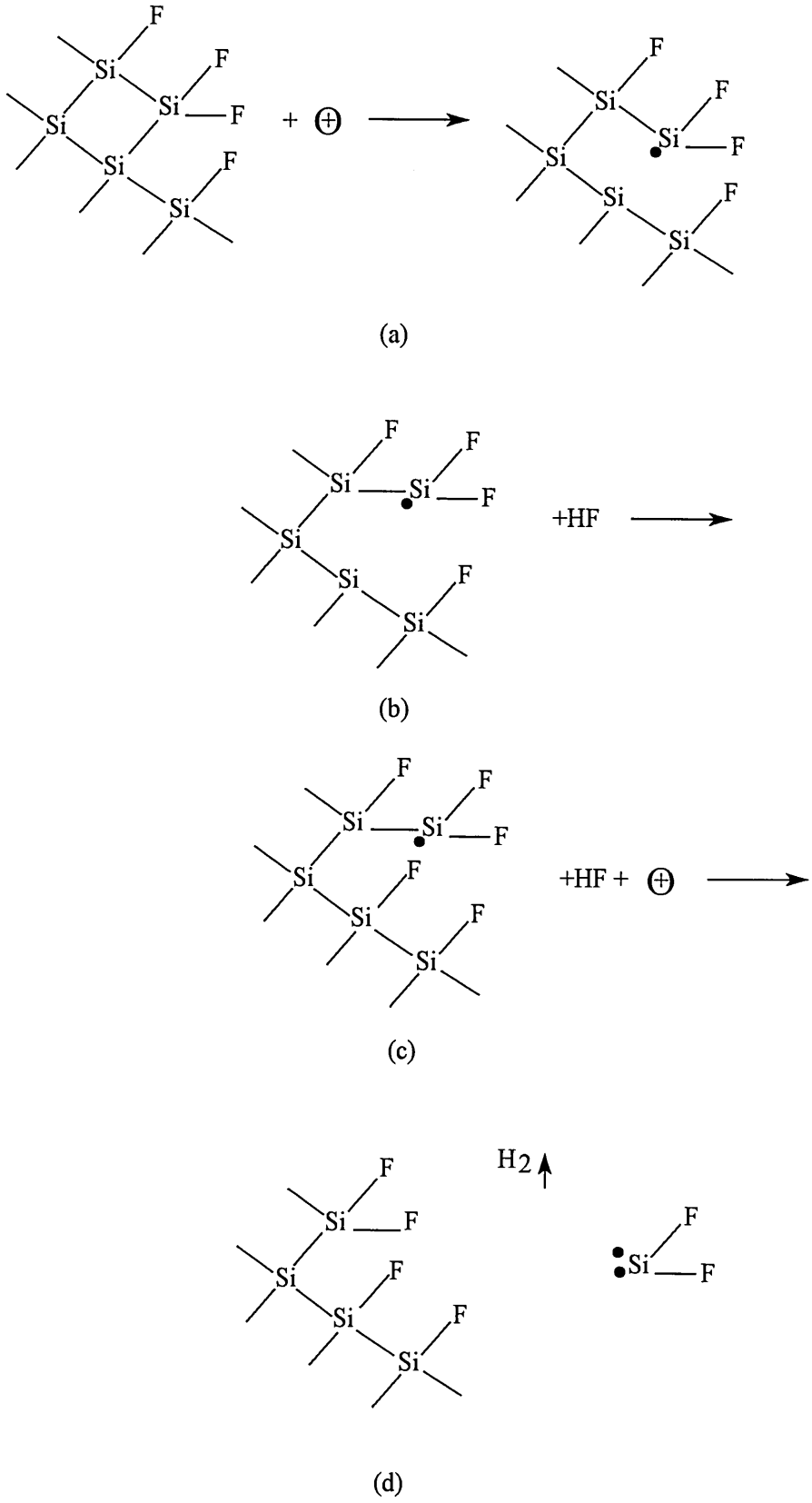


Figure 4.4 Dissolution mechanism of silicon in hydrofluoric acid solution (After Memming and Schwandt 1966).

Lehmann and Gösele (1991) proposed the existence of hydrogen on the surface of the silicon substrate. An essential proposition of the their silicon dissolution model is that silicon hydride bonds on the silicon surface would prevent any attack of fluoride ions unless electronic holes are available. If an electric field is applied across the silicon-hydrofluoric acid interface, electronic holes move towards the surface and fluoride ions attack the Si-H bonds to establish Si-F bonds on the silicon surface as shown in Fig. 4.5. As SiF_2 is unstable, the Si-Si backbonds will now be attacked by HF in a way that silicon atoms remain bonded with hydrogen. If the walls between the pores are totally depleted of electronic holes there will be no further dissolution. Therefore, the Si-H bonds are more likely to exist in an intermediates stage during the dissolution process and are not directly responsible for the pore wall passivation. In an early porous silicon formation mechanism, Turner (1964) proposed the formation of an amorphous silicon layer on the silicon surface as shown in equation (4.7).

$$2SiF_2 + 2HF \rightarrow Si_{\ amorphous} + H_2SiF_6 \qquad (4.7)$$

It has been also reported that resulting from equation (4.7) the thick high resistance amorphous silicon layer is responsible for the passivation of the pore walls [Smith and Collind 1992]. This resistance layer undergoes a slow electrochemical dissolution process which prevents the pore walls from rapid reactions. At the same time, the tips of the pores are free of the layer and are exposed to a rapid reaction. The reaction in equation (4.7) can be split into two consecutive reactions, the first reaction is:

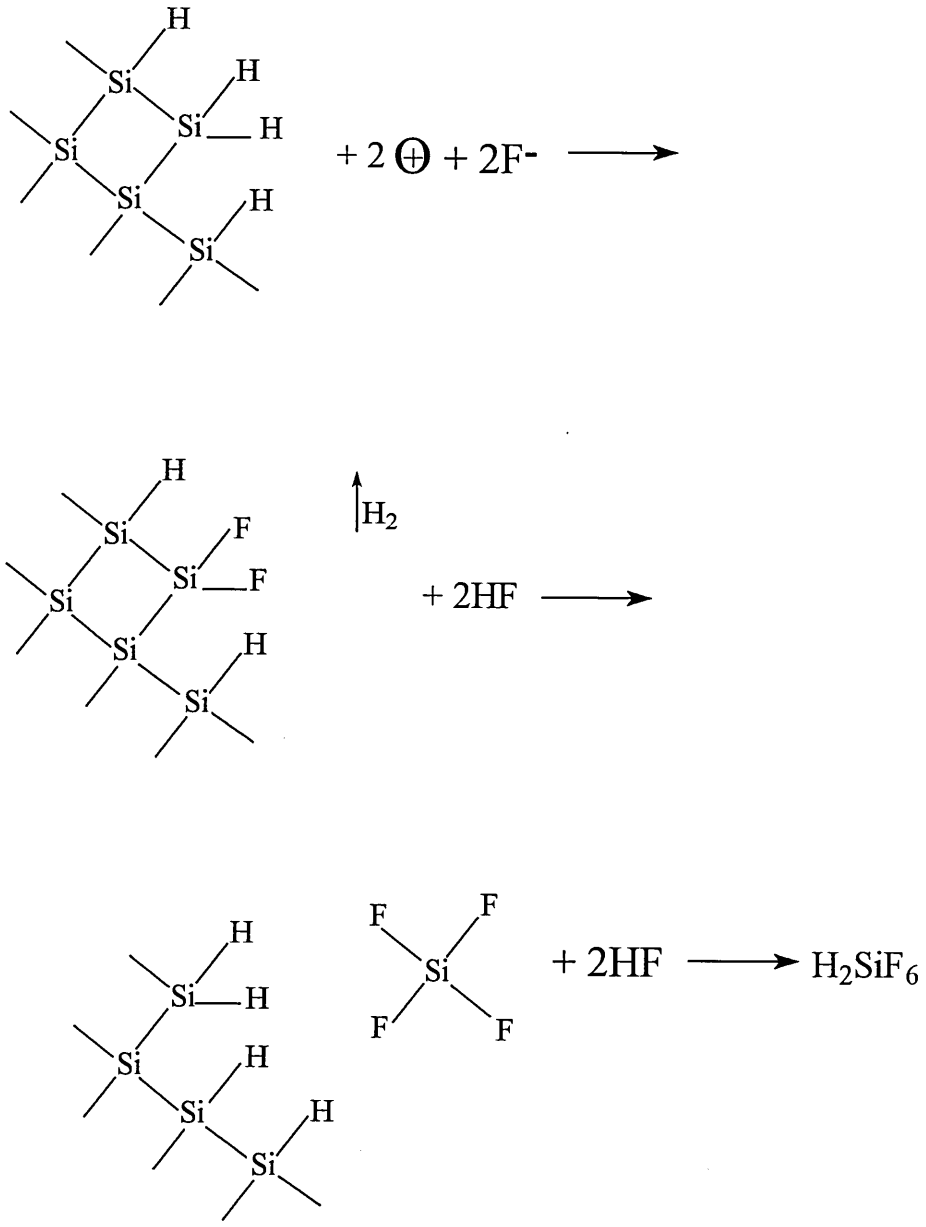


Figure 4.5 Mechanism of the anodic dissolution of silicon in concentrated hydrofluoric acid solution (After Lehmann and Gösele 1991).

$$2SiF_2 \rightarrow Si_{amorphous} + SiF_4 \quad (4.8)$$

and the second reaction can be split into two parallel reactions as in equation (4.9).

$$Si_{amorphous} + 2H_2O \overset{Slow}{\rightarrow} SiO_2 + 2H_2 \quad (4.9A)$$

$$SiF_4 + 2HF \overset{Rapid}{\rightarrow} H_2SiF_6 \quad (4.9B)$$

If the anodisation process takes more than an hour, the silicon dioxide layer in equation (4.9A) will undergo a further reaction to change it into a stable tetravalent form.

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (4.10)$$

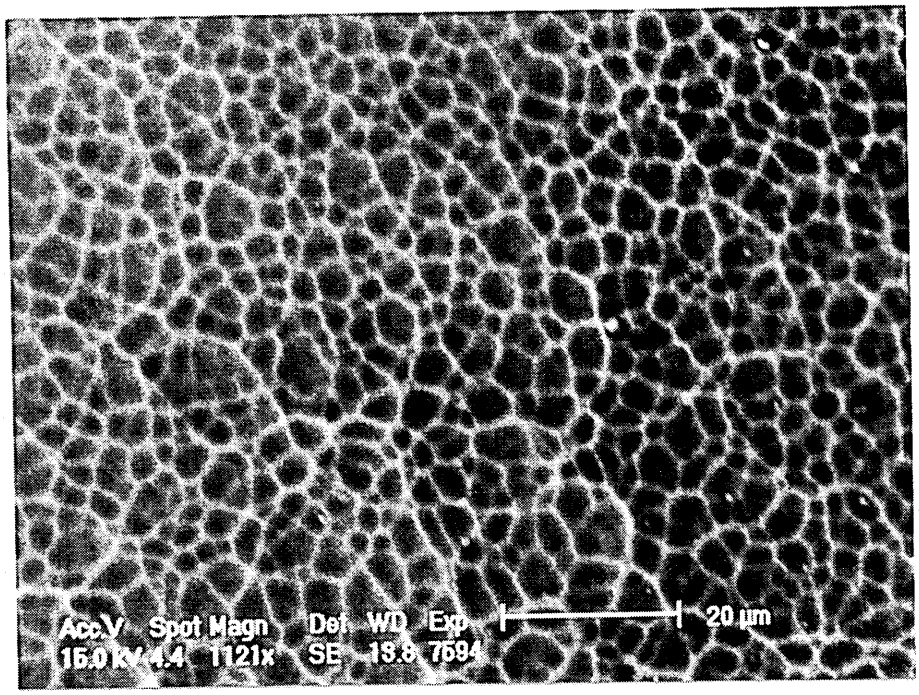
These reactions are very similar to the reactions (4.3)-(4.6) with the only different by the production of the thick resistance amorphous silicon layer. To summarise the porous silicon formation chemistries presented in this section, it is clear that the succession of the reactions (4.2)-(4.6), or some modification of them, is the main chemical processes behind the formation of porous silicon.

4.5 Structure study of porous silicon surface

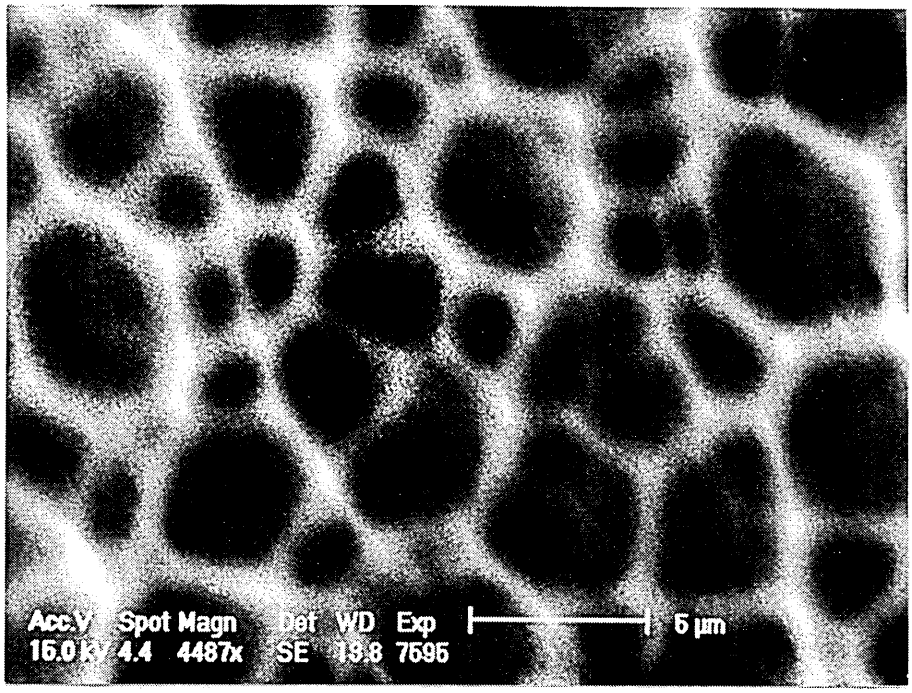
A scanning electron microscopy (SEM) has been used to study the structure of the PS surface. PS layers developed under different fabrication conditions have been examined using this technique to determine the optimum fabrication conditions for visible light emission devices. SEM studies were also used to investigate the PS layer homogeneousity and to estimate the sample thickness. The samples used for this

purpose were investigated in cross section and were therefore cut using a diamond saw. The samples used for SEM investigation were coated in a conductive material, such as gold or carbon, to improve the conduction between the sample surface and the electron detector.

Figure 4.6 shows the SEM image of a PS layer made from a 8-12 Ω.cm silicon substrate at an anodisation current of 30 mA/cm^2 in 20% diluted HF acid. The structure shows a fine uniform mesh of clear and dark regions in which the dark areas are silicon rich and the clear areas are pores (voids). As shown in Fig. 4.6, the pore size is in the 0.4-0.6 μm range which gives a non-luminescent macroporous silicon layer. It could be noticed that the pores are disorderly located and have various shapes. Figure 4.7 shows the SEM micrographic study of PS layer fabricated from high resistivity (300-400 Ω.cm) silicon substrate at 30 mA/cm^2 in 20% diluted HF solution for 10 minutes (the same fabrication conditions as in the sample used in Fig. 4.6 except for the substrate's resitivity). The sample shows again a fine mesh of clear and dark areas with pore size of about 2 μm. It is clear that the sample has a macroporous structure but the pores size is much larger than the sample in Fig 4.6. It has been found that all the PS samples fabricated from high resistivity silicon substrates give no luminescence and have very large pore size. In general, the PS layers fabricated from heavily doped silicon substrates have greater porosity with smaller pore size than samples made from lightly doped silicon substrates. These results support the proposal that the number of pores in a PS layer is directly proportional to the doping level of the silicon substrate.



(a)



(b)

Figure 4.6 SEM micrographic image of a PS layer formed in 8-12 Ω.cm silicon substrate at an anodisation current of 30 mA/cm^2 in 20% diluted HF acid. (a) With magnification of 1121. (b) At x5 higher magnification.

Luminescent PS layers with high level of porosity and nano-pores size have been fabricated using 8-12 Ω.cm silicon substrates in a bath of 50:50 (by volume) solution of aqueous 49% HF and 95% ethanol. The current density and the anodisation time were between 20-60 mA/cm^2 and 10-15 minutes respectively. All the samples with high porosity PS layers exhibit photoluminescence in the visible range. As luminescent PS structures have pores sizes in the range of a few nanometers, SEM techniques are unable to provide sufficient information regarding the surface structure of such devices. Figure 4.8 shows the effect of using low concentration HF acid and using long anodisation time (over an hour). The anodisation process took place with a current density of 20 mA/cm^2 in less than 10% HF acid for 70 minutes. The porous part of the sample consists of several sub-layers with different structural characteristics. The topmost layer was made up with 5-7 μm pores and could be removed by washing in a potassium hydroxide (KOH) solution. The lower part of the PS layer, closest to the substrate, contained crystalline particles with sizes smaller than the size of the particles in the topmost layer. According to this result the HF acid had etched the already made PS layer as the anodisation process continues for long time.

SEM micrograph images for the cross section of PS layers were used to gain more information about the structure of the films. The cross section study of all PS samples shows that the PS layers are uniform from the surface to the interface between the PS layer and the silicon substrate as shown in Fig. 4.9. It can be said that the silicon was dissolved uniformly towards the substrate direction. The thickness of the PS layer in Fig. 4.9 appears to be about 5-6 μm. The dark area in the interface between the PS layer and the silicon substrate is the area where the silicon was not completely etched (not fully depleted of electronic holes). The cross section of the PS layer shows that the pores are

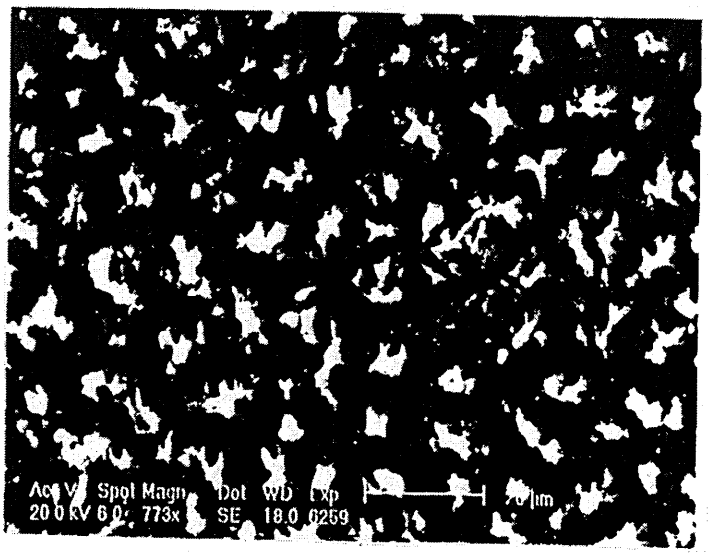


Figure 4.7 SEM image of the surface of a PS layer formed by the same fabrication conditions as in the sample used in Fig. 4.6 with high substrate resitivity (300-400 Ω.cm).

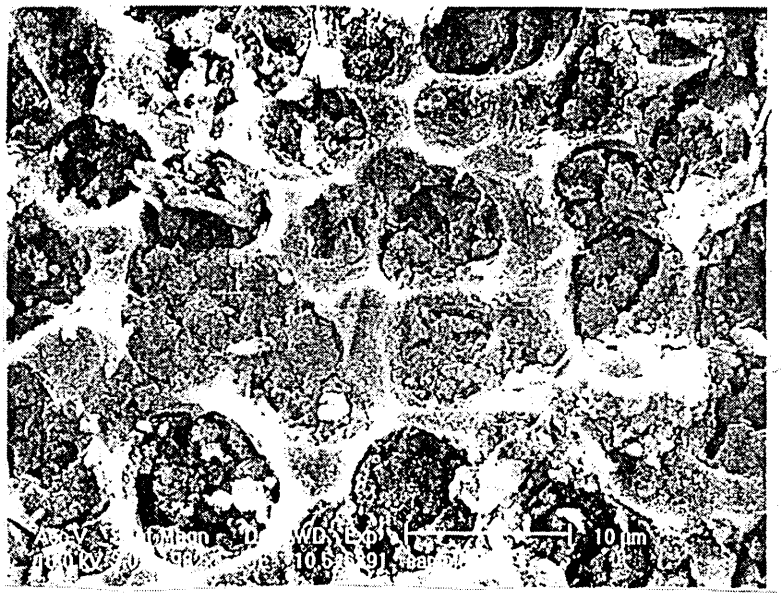
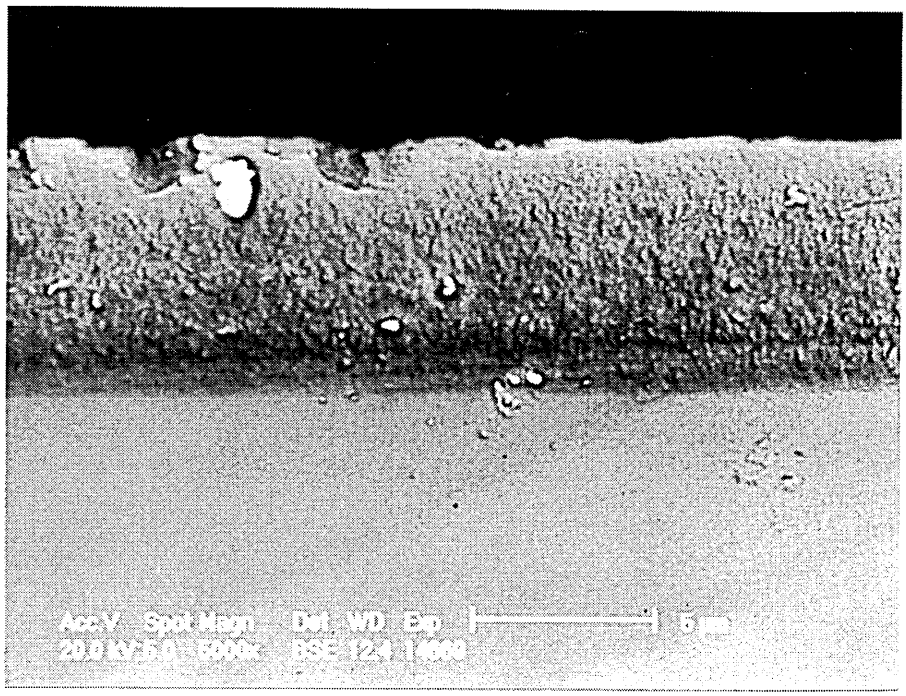
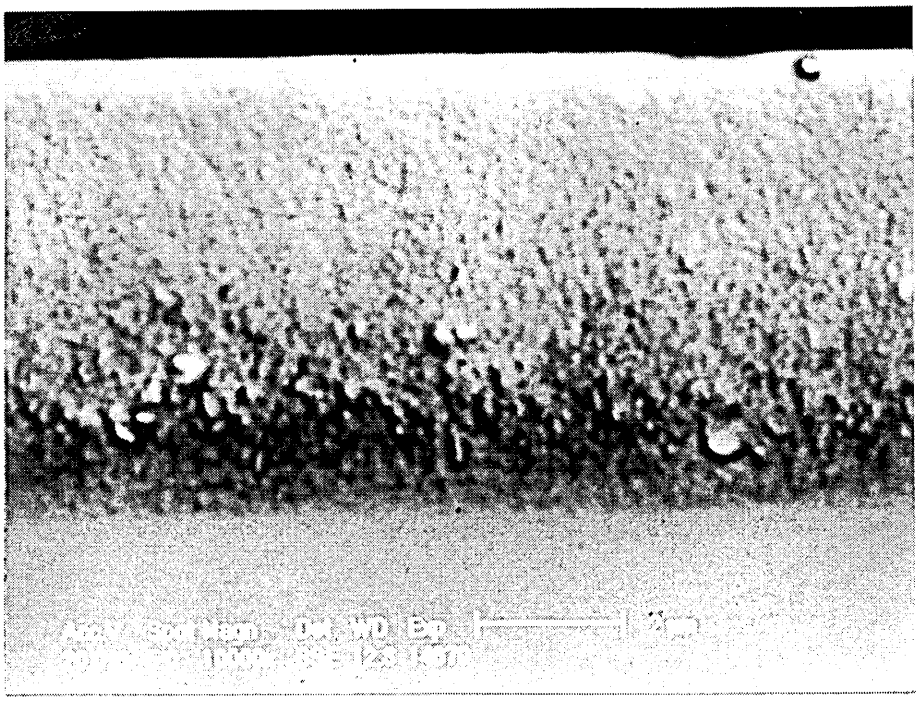


Figure 4.8 SEM micrograph of the surface of a PS layer formed in 8-12 Ω.cm silicon substrate with current density of 20 mA/cm^2 in less than 10% HF acid for 70 minutes.



(a)



(b)

Figure 4.9 Cross sectional SEM view of a PS layer formed under the same fabrication conditions as the sample in Fig. 4.6. (a) With magnification of 5000. (a) at x2 higher magnification.

not formed in a straight line from the surface to the interface with the substrate, it means that the pores are formed zig-zag in the thickness direction. Figure 4.10 shows a profile of the etching of the same PS sample as in Fig. 4.9. The curve in this figure shows the silicon concentration as a function of depth into the substrate. It is proposed that this curve can be used to estimate the porosity of the sample. The porosity of the PS layer shown in Fig 4.10 is estimated to be about 45-50 %. It can be seen that the PS layer is uniformly etched from the surface up to the interface between the PS layer and the silicon substrate where the curve starts to rise gradually.

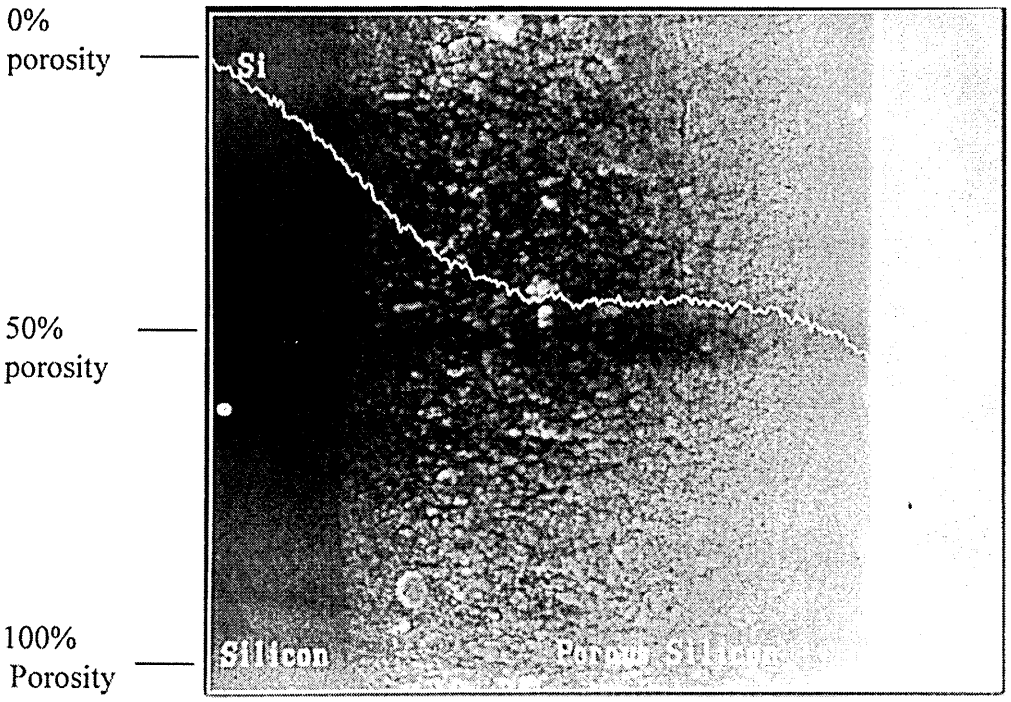


Figure 4.10 Cross sectional SEM image of the same PS layer as in Fig. 4.9 showing how the surface of the layer rich in silicon.

CHAPTER FIVE

DC ELECTRICAL PROPERTIES OF POROUS SILICON

5.1 Introduction

The dependence of current on the applied voltage and the temperature will provide important information on the current transport through a semiconductor. The barrier height, activation energy, ideality factor of the device, and the position of the Fermi level can be estimated from these measurements.

The measurements of electronic conduction through semiconducting materials will be briefly summarised in the first part of this chapter. Measurements of the d.c. conduction in porous silicon (PS) films at a wide range of temperatures will be discussed in details throughout the other part of the chapter. Different models to describe the conduction behaviour of PS will also be described in this chapter.

5.2 Theoretical Aspects

5.2.1 Electrical contacts (metal-semiconductor contacts)

The properties of junctions and electrical contacts form the basis of all semiconductor devices. The most common junctions in semiconductor device technology are the junctions between a p-type and an n-type semiconductors (p-n junction) and the metal-semiconductor (electrical contacts) contacts. Hence, it is important at this point to state the different types of junctions and discuss the importance of each of them.

The electrical contact is the area of the device in which charge carriers pass through to the device (or out of the device). Most applications of such contacts involve metal-semiconductor contacts which are usually formed by a thin film deposition process (see section 3.3) in which the metal acts as an electrode. This type of contact is dependent of the relative work functions of both the metal (ϕ_m) and the semiconductor (ϕ_s). The conductivity of the device can be altered by many orders of magnitude by the effect of the choice of the contact material. When the two materials (metal and semiconductor) come into contact, the Fermi levels on both sides align themselves as the most energetic electrons in the material with the smaller work function will tunnel into the other material searching for lower empty energy levels [Kasap 1997]. These electrons accumulate near the surface of the other material leaving an electron depleted region resulting in the positive space charge near the junction between the two materials. This initial flow of carriers across the junction leads to an electrical potential difference between the two materials which is equal in magnitude to the difference between their work functions.

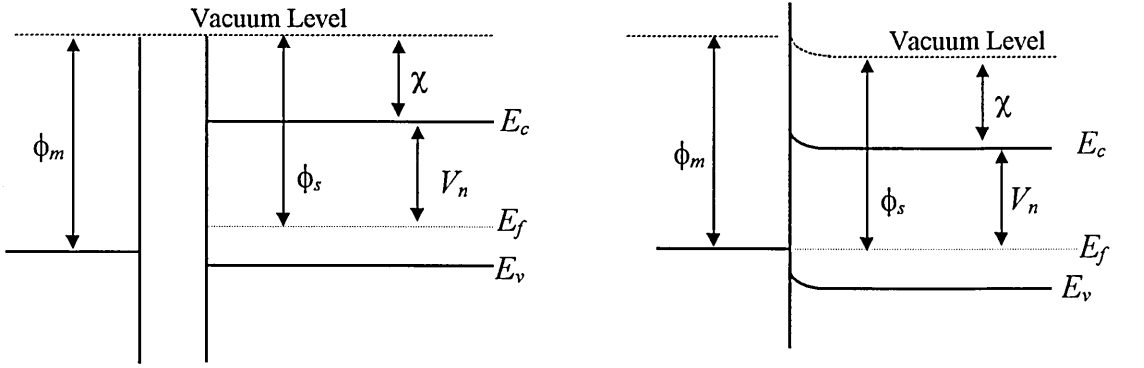
For the metal, the work function ϕ_m represents the minimum energy required to free an electron from the solid as there are electrons at the Fermi level of the metal. In a semiconductor, this is equivalent to ($\chi + V_n$), where χ is the energy required to remove an electron from the bottom of the conduction band (E_c) to the vacuum level (in other words, the width of the conduction band) and V_n is the energy difference between E_c and the Fermi level as shown in Fig. 5.1.

Depending on the metal work function and the type of the semiconductor (n- or p-type), there are initially two types of electrical contacts that can be formed on the

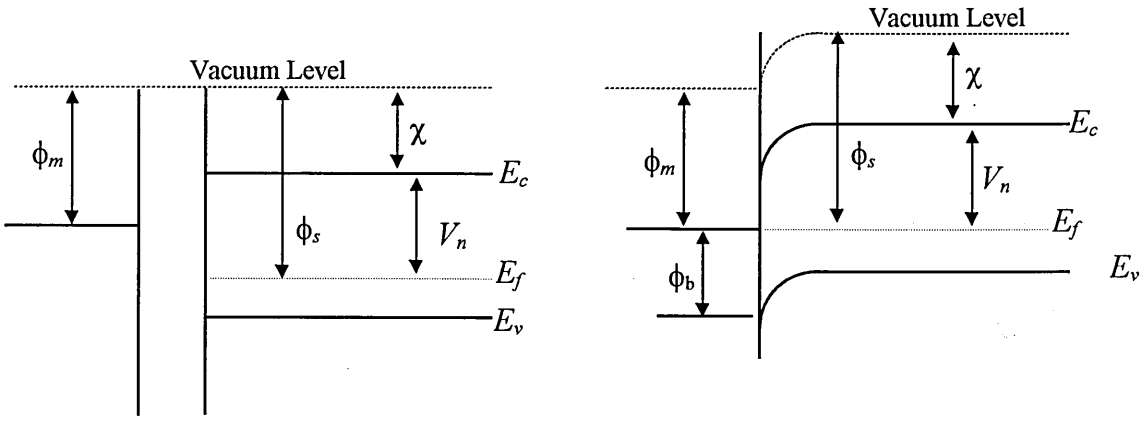
semiconductor, these are ohmic and blocking contacts. The properties of these contacts will be discussed in the following sections.

5.2.1.1 Ohmic contacts

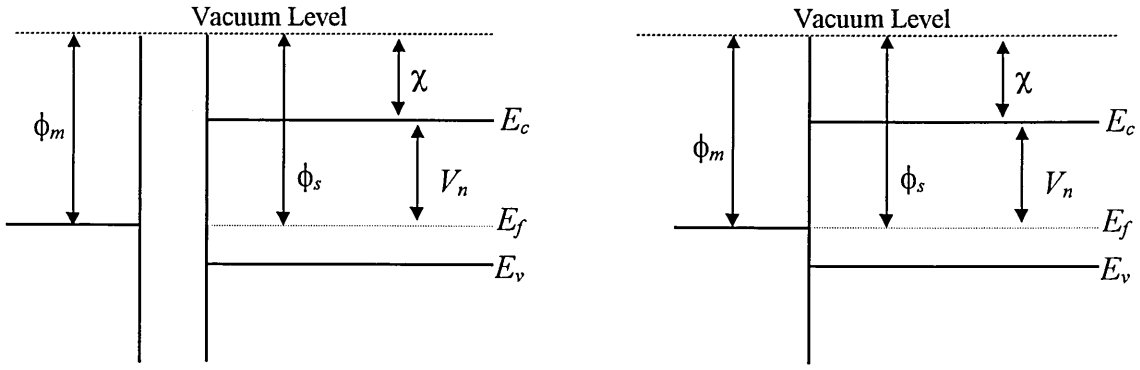
This form of metal-semiconductor contact is very common in semiconductor device technology. Ohmic contacts are needed in both p-type and n-type materials to connect the active region of the device with external circuitry. In this type of contact, the junction should have a very small resistance so that the current flow is essentially limited by the resistance of the semiconductor outside the contact area. In principle, in order to produce this type of contact it is important to choose a metal with a work function higher than that of a p-type semiconductor and smaller than that of an n-type semiconductor ($\phi_m > \phi_s$ for p-type semiconductor, and $\phi_m < \phi_s$ for n-type semiconductor). Figure 5.1.(a) shows the formation of an ohmic contact between a metal and p-type semiconductor, where the work function of the metal ϕ_m is higher than the work function of the semiconductor, ϕ_s. The Fermi levels are equalised by transferring holes from the metal to the semiconductor (or electrons from the semiconductor to the metal). There is thus no depletion at the junction and the equilibrium is reached when the accumulated holes in the valence band of the semiconductor prevent further holes tunnelling from the metal. There is then only a small barrier to further holes flow from the metal to the semiconductor can be easily overcome by an external bias.



(a) Ohmic Contact



(b) Blocking Contact



(c) Neutral Contact

Figure 5.1 Energy band diagram of a metal and a p-type semiconductor before (left) and after (right) contact.

Ohmic contacts can also be formed by introducing a heavily doped region close to the semiconductor region. There is then a thin potential barrier for the charge carriers to tunnel across into the main part of the metal or the semiconductor [Wood 1994]. In general, porous silicon has a very high resistivity so that the contact resistance is normally considered to be negligibly small.

5.2.1.2 Blocking contacts

This type of contact is frequently referred to as a Schottky junction (or rectifying contact). This type of metal-semiconductor contacts occurs when ($\phi_s > \phi_m$) for p-type semiconductors as shown in Fig. 5.1 (b). To restore the system to its equilibrium state (equalisation of the Fermi levels), the electrons flow from the metal to the semiconductor leaving positive charge on the metal surface. This transfer of electrons create a depletion region for holes near the surface of the semiconductor with a depletion width W from the contact into the semiconductor. As a result, a band bending will arise in the semiconductor band diagram with a potential barrier for holes moving from the metal to the semiconductor. This potential barrier has a barrier height ϕ_b which is given by (for p-type semiconductor)

$$\phi_b = E_g - \phi_m + \chi \tag{5.1}$$

where E_g is the semiconductor energy band gap. This type of contact is referred to as a hole blocking contact.

For an n-type semiconductor, the condition for a contact to be blocking is $\phi_m > \phi_s$ and the contact is referred to as an electron blocking contact [Tyagi 1985]. In this case the barrier height represents the difference between the metal work function and the electron affinity of the semiconductor.

$$\phi_b = \phi_m - \chi \tag{5.2}$$

Generally, for any given semiconductor and for any metal, the sum of the barrier heights on n-type and p-type substrates should be equal to the semiconductor band gap E_g.

The effect of the barrier height at a metal-semiconductor contact is to provide a rectifying contact so that it conducts current more easily in one direction than the other. Under forward bias charge carriers in the semiconductor can readily overcome the barrier height to enter the metal. Under reverse bias, however, the flow of carriers is limited by the carriers available over the Schottky barrier, in which case the carriers in the metal cannot easily overcome the barrier height.

Applying an external bias to a metal-semiconductor contact will alter the relative position of the Fermi levels, and hence the energy bands in the semiconductor. In this case, the major source of current flow across the metal-semiconductor interface is the thermionic emission of majority carriers over the potential barrier. The current flow through the semiconductor due to thermionic emission of majority carriers is given by the Richardson equation [Kasap 1997]:

$$I_{ther} = AST^2 \exp[-\frac{q\phi_b}{kT}] \tag{5.3}$$

where A is a constant called Richardson's constant (in Amp./cm^2/K^2), S is the device active area (in cm^2), q is the electron charge (in coulombs), k is Boltzmann's constant (in J/K), and T is the temperature (in Kelvin). If the barrier height is assumed to be independent of the applied voltage, this current saturates and represents the reverse bias current of metal-semiconductor junctions. According to Sze (1981), the current flowing from the semiconductor to the metal I_{sm} can be expressed as:

$$I_{sm}=AST^2\exp\left[-\frac{q\phi_b}{kT}\right]\exp\left[\frac{qV}{kT}\right] \tag{5.4}$$

where V is the applied voltage. As assumed before, if the barrier height for electrons from the metal into the semiconductor is independent of the applied voltage V, in equilibrium, the current from the metal to the semiconductor must be equal to the current from the semiconductor to the metal. Hence, the current from the metal to the semiconductor I_{ms} can be estimated using equation (5.4) at $V=0$

$$I_{ms}=AST^2\ \exp\left[-\frac{q\phi_b}{kT}\right] \tag{5.5}$$

Therefore the net current is:

$$I=I_{sm}-I_{ms}$$

or

$$I=I_s\left[\exp\left(\frac{qV}{kT}\right)-1\right] \tag{5.6}$$

where I_s is the reverse saturation current and given by:

$$I_s = AST^2 \exp[-\frac{q\phi_b}{kT}] \tag{5.7}$$

For high voltages ($V >> kT/q$), equation (5.6) can be written as

$$I = I_s \left[\exp\left(\frac{qV}{nkT} \right) \right] \tag{5.8}$$

The parameter n has been introduced in equation (5.8) in order to take into account the deviation of the diode response from its ideal behaviour and is called the ideality factor. The barrier height is an important characteristic of a Schottky contact (blocking contact), as it determines when the applied forward voltage V is large enough to cause significant conduction. From equation (5.7)

$$\ln(\frac{I_s}{T^2}) = \ln AS - \frac{q\phi_b}{kT} \tag{5.9}$$

where S is the device area. By plotting ln (I_s/T^2) vs $1/T$, the result should, in principle, give a straight line with the slope determining ϕ_b. But if the barrier height is assumed to be temperature dependent, the results should give a curve in which the tangent at any point (temperature) will give the value of the barrier height ϕ_b at that temperature.

At the end of this section it is worth mentioning that there is another type of contacts which can occur between metal and semiconductor, when the metal and the semiconductor work functions are equal ($\phi_s = \phi_m$), as shown in Fig. 5.1 (c). In this case there is no flow of charge carriers across the junction, no space charge formation or depletion region, and therefor there is no band bending in the semiconductor band diagram. This type of contact is called a neutral contact and operates as an ohmic contact at very low voltages.

5.2.2 The p-n junction

This is the most common and important junction in semiconductor device fabrication. This junction occurs when p-type and n-type materials of the same semiconductor meet together within the same lattice structure. This can be achieved by introducing dopants of opposite polarity into p- or n-type materials. Due to the hole concentration gradient from the p-side to the n-side, holes diffuse towards the n-side of the junction. The same thing happens to the electrons as they diffuse from the n-side into the p-side of the junction. The diffused electrons and holes meet and recombine around the junction region, which consequently becomes depleted of free carriers. An internal electric field is then set up in a direction so as to oppose any further carrier motion. This electric field will try to drift the holes back into the p-side and the electrons into the n-side of the junction. In other words, this field drives the holes and electrons in the opposite direction of their diffusion. As more holes diffuse toward the n-side and electrons diffuse toward the p-side of the junction, the internal field will increase until equilibrium is reached when the magnitude of these two currents are equal, and no more carrier movement across the junction occurs.

As with the metal-semiconductor Schottky (blocking) junction, at a p-n junction the Fermi levels equalise. To maintain a constant Fermi level throughout the whole device, the conduction and valence bands must bend in the junction area as shown in Fig. 5.2. Due to this bending, there will be a potential difference known as the built-in potential, V_{bi}, between the conduction bands of the p-type and the n-type materials. The built in potential will act as a barrier for further electron transport from the n-type region to the p-type region.

The application of an external bias to a pn junction will alter the relative position of the Fermi level, and hence the energy band diagram of the junction. This effect is similar to what happens in a Schottky junction with the difference that in a pn junction the major source of the current flow is dominated by the minority carriers. The current - voltage ($I(V)$) characteristics of a pn diode is similar to that of a Schottky diode and can therefore be expressed as:

$$I = I_s \left[\exp\left(\frac{qV}{nkT} \right) - 1 \right] \tag{5.10}$$

The ideality factor (n) and the reverse saturation current (I_s) can be determined from the slope and the intercept of a $\ln(I)$ against V plot respectively. The diode ideality factor can be used to indicate the current transport mechanisms in semiconductor junctions [Bube 1992]. An ideality factor close to unity indicates that the current in the junction is dominated by the carrier diffusion across the junction, while n values close to 2 are attributed to the dominance of carrier recombination in the depletion region as the main current transport mechanism. Higher values of n are ascribed to the recombination and tunnelling processes in the junction area.

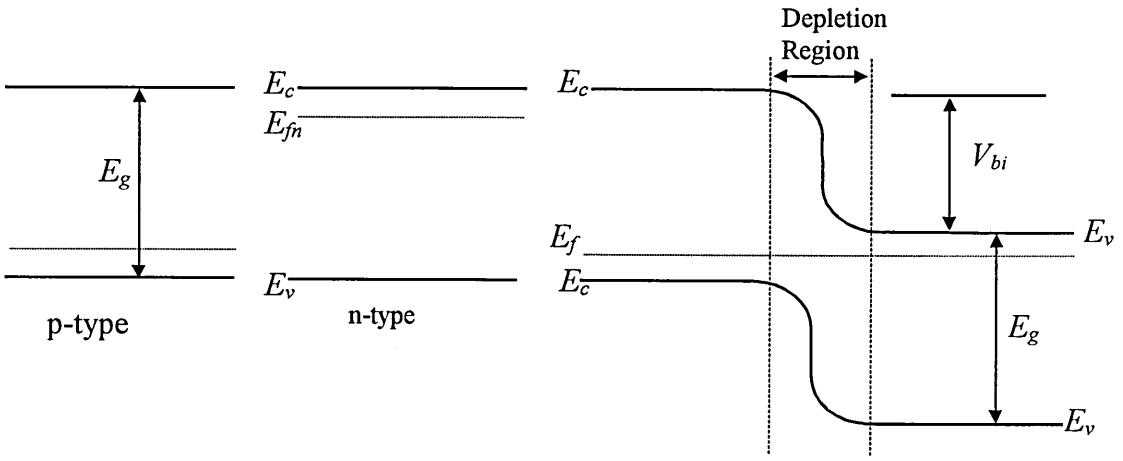


Figure 5.2 Band diagram of isolated p-type and n-type semiconductors (left) and a pn junction in equilibrium.

It has been suggested that the mechanisms responsible for making n exceed unity for the forward current must have some effect on the reverse current as well [Missous and Rhoderick 1986]. Therefore the second term of equation (5.10) ($-I_s$) should also contain n. For this purpose, Missous and Rhoderick (1986) have suggested that the current-voltage $I(V)$ characteristics of a diode can be written in the form:

$$I = I_s \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right] \qquad (5.11)$$

This equation is a generic one and can be applied to describe the conduction through a barrier at both pn junctions and metal-semiconductor Schottky contacts. Another reason of using equation (5.11) is that it could be used to describe $I(V)$ characteristics resulting from all transport mechanisms. It also has the practical advantage that a plot of ln[I/{1 -

$\exp(-qV/kT)\}]$ against V should be linear for all values of reverse voltages and forward voltages less than $3kT/q$. The value of n and I_s can be estimated from the slope of the liner portion of this graph and the intercept respectively.

The neutral area of the device (the depleted PS area, the rest of the silicon substrate and the ohmic contacts, in PS structures) offers a series resistance R_s and so a significant voltage drop occurs across that at large forward current [Chand and Kumar 1996]. This amounts to a reduction of the voltage across the barrier region from that actually applied to the electrodes of the device. Therefore, the voltage across the barrier region should be reduced from V to $V - IR_s$, and equation (5.11) becomes

$$I = I_s \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \qquad (5.12)$$

In this situation a plot of $\ln(I)$ versus V deviates from the straight line at high forward voltages.

Generally, the analysis of $I(V)$ characteristics of a pn junction usually reveals an unusual increase of the barrier height and decrease in the ideality factor with increasing temperature. These facts cannot be explained by incorporating interface states, tunneling, or generation-recombination effects. In fact, the decrease in barrier height at low temperatures leads to nonlinearity in the activation energy ($\ln(I_s/T^2)$ vs $1/T$) plot. The temperature dependence of the ideality factor is usually taken as: [Chand and Kumar 1996]

$$n = 1 + \frac{T_o}{T} \tag{5.13}$$

where T_o is a constant. It is common to plot nT versus T. According to equation 5.13 the plot should give a straight line with slop equal to 1. Experimental results, however, do not always follow such a dependence and show a deviation specially at low temperatures. Therefore, the ideality factor should be introduced to the exponential term of the saturation current in equation 5.7 in order to explain the increase of barrier height with increasing temperature. This means that as the ideality factor inccreasing with decreasing temperature, the barrier height reduced to ϕ_b/n. Hence, the plot of $\ln(I_s/T^2)$ vs $1/nT$ should remove the nonlinearity of the $\ln(I_s/T^2)$ vs $1/T$ plot and obtain a straight line corresponding to a single value of activation energy.

5.2.3 Heterojunctions

It has been approved in recent years that PS has a wider band gap than silicon. Therefore, the junction between PS and the silicon substrates could be regarded as a heterojunction. Heterojunction results when semiconductors of different band gaps and electron affinities are brought together to form a junction. It may be an isotype junction if the two semiconductors have the same doping, or anisotype junction if not. As PS behaves like n-type silicon, an isotype junction is expected to form between PS and the silicon substrate if PS is fabricated on n-type silicon substrates. In contrast, if p-type silicon substrate were used to fabricate the PS layer, anisotype junction would be expected to appear between PS and the silicon substrate. In this study, p-type silicon substrates were used to make PS samples and therefore the interest will be on anisotype heterojunctions.

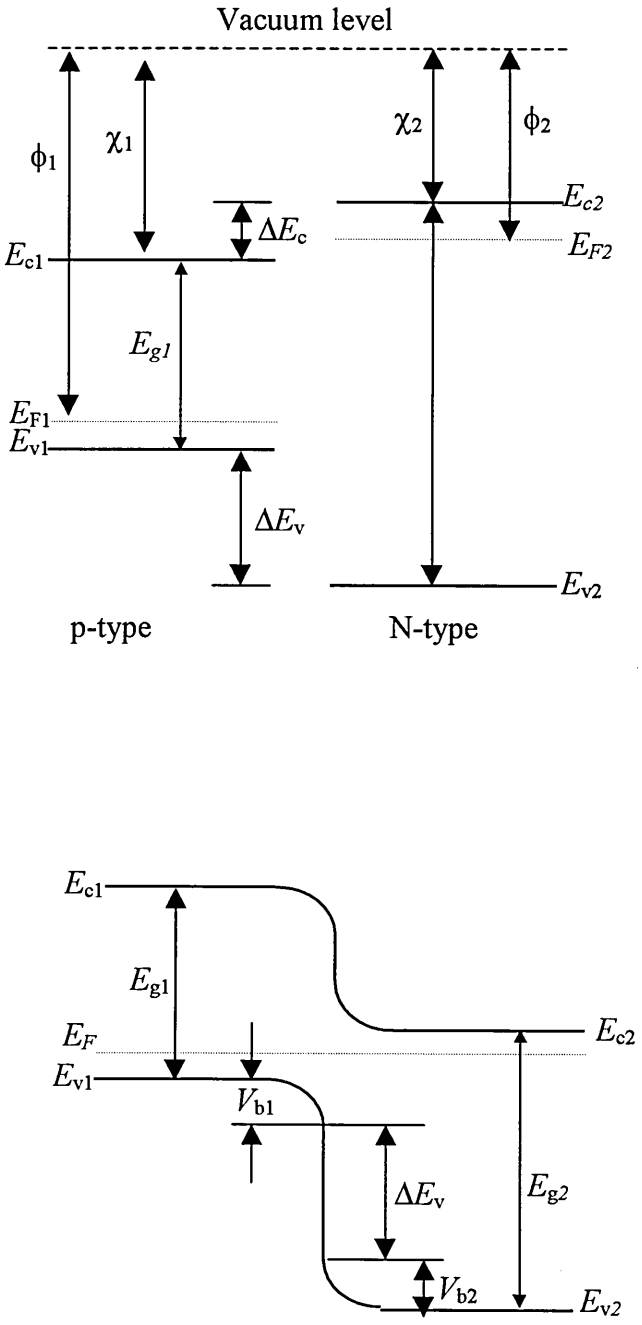


Figure 5.3 Energy band diagram for an ideal anisotype p-N heterojunction before (top) and after (bottom) contact has been made.

The energy band diagram of a heterojunction is more complicated than that of a homojunction. Figure 5.3 shows the energy band diagram of an ideal heterojunction. When a junction is formed, the Fermi levels E_{F1} and E_{F2} align themselves by charge movement that results in band bending on both sides of the interface (like in any junction formation). The built in potential V_b arises between the p-type and N-type neutral regions as required to align the Fermi levels at equilibrium. It can be calculated from the difference in the work functions of the two semiconductors (ϕ_1 - ϕ_2), which is equivalent to the sum of the voltages that appear across the two semiconductors (V_{b1} + V_{b2}) [Streetman 1995].

The main difference between a pn junction and a pn heterojunction is the formation of a discontinuity in the conduction band due to the difference in energies of the conduction band edges in the two semiconductors. The discontinuities in the conduction band ΔE_c and the valence band ΔE_v accommodate the difference in band gap between the two semiconductors ΔE_g. In an ideal pn heterojunction, ΔE_c may be calculated from the difference in electron affinities (χ_1 - χ_2) and ΔE_v would be found from ΔE_g - ΔE_c. The actual energy band profile for the heterojunction is dependent on the relative values of E_g, χ, and ϕ for the two semiconductors and therefore energy band profile for different heterojunctions differ.

The current transport mechanisms in pn heterojunction are similar to the mechanisms in pn homojunction. Therefore, heterojunctions exhibit current-voltage characteristics similar to the pn junctions and then equations 5.5 to 5.13 can be applied to the heterojunctions as well as pn junctions.

Measurement of the pn heterojunction capacitance as a function of voltage allows to observe if the junction is graded or abrupt junction, as well as the calculation of the built in voltage. The capacitance for an anisotype heterojunction can be obtained by solving Poisson's equation and may be expressed as [Sparkes 1987]:

$$C^2 = a^2 \frac{qN_D N_A \varepsilon_1 \varepsilon_2 \varepsilon_o}{2(\varepsilon_1 N_D + \varepsilon_2 N_A)} \times \frac{1}{V_b - V} \tag{5.14}$$

where N_D and ε_1 the donor concentration and permittivity respectively of the n-type semiconductor, N_A and ε_2 the acceptor concentration and permittivity respectively of the p-type semiconductor, a is the active device area, V_b is the build in potential, and V is the applied voltage. Taking the derivative of $(1/C^2)$ with respect to the applied voltage, the slop of the (C^{-2} Vs V) plot can be given by :

$$\frac{dC^{-2}}{dV} = 2 \frac{(\varepsilon_1 N_D + \varepsilon_2 N_A)}{a^2 q N_D N_A \varepsilon_1 \varepsilon_2 \varepsilon_o} \tag{5.15}$$

The linear relation ship between $(1/C^2)$ and V indicates that the junction formed between the two semiconductors is abrupt, otherwise it is graded.

5.2.4 Current transport models in semiconductors

The current transport in Schottky metal-semiconductor contacts is mainly dominated by the majority carriers, in contrast to pn junctions where the current is mainly due to the minority carriers. As discussed in chapter two, different models have

been proposed to describe the current transport in porous silicon (PS). The early model assumed that the rectification in the $I(V)$ characteristics of PS is due to the existence of a Schottky barrier between the metal and the PS interface [Koshida and Koyama 1992, Pacebutas et al 1995, Dimitrove 1995, and Maolong et al 1998]. However, an interpretation of rectifying characteristics due to the junction between the PS and its silicon substrate is also reported [Pulsford et al 1994, and Ray et al 1998]. In this section these two models as well as other possible transport mechanisms relating to the conduction in PS will be briefly discussed.

For the metal-PS junction model, the thermionic emission of majority carriers over the potential barrier is the major current transport mechanism. Some experimental data (including these presented in the present work) indicate that PS films fabricated from p-type substrates behave like n-type silicon due to the depletion of their majority carriers [Pulsford et al 1994, and Ray et al 1998]. Therefore, the pn junction is believed to be the main junction that is responsible for the current transport through PS structures. In this case, and as a normal pn junction, the diffusion of minority carriers is responsible for the current transport through the junction. Injected holes diffuse in the n-side and recombine with the electrons, which are abundant in this side. The electrons lost in the recombination process are easily replenished by the negative terminal of the power supply. The current due to hole diffusion can be maintained because more holes can be supplied by the p-side. This type of current transport is usually indicated by an ideality factor (n) close to unity. However some of the minority carriers recombine in the depletion region and the external current must supply the carriers lost in the recombination process in the space charge layer. The value of n in this process is usually close to 2.

5.2.5 Temperature dependence and activation energy

Most of the semiconductors possess a negative temperature coefficient of resistance due to the increase of the carrier concentration with increasing temperature [Kasap 1997]. The temperature dependence of current passing through a semiconductor can in general be expressed by:

$$I = I_o \exp\left[\frac{-E_a}{kT}\right] \tag{5.16}$$

where I_o is a constant which can be determined from the intercept of the plot of ln$I$ against $1/T$, and E_a is the activation energy. The above equation can be re-written as follows:

$$\ln(I) = \ln(I_o) - \frac{E_a}{kT} \tag{5.17}$$

and therefore a plot of ln$I$ against $1/T$ should yield a linear relationship with a slope of $-E_a/k$ from which the activation energy (E_a) can be calculated. However, the reverse saturation current I_s can be used to calculate the activation energy as explained in section (5.2.1.2). If the curve exhibits different linear regions then this indicates that each temperature region has different activation energy, and such behaviour can be ascribed to different excitation processes dominating each region. Generally speeking, small values of activation energy are believed to be associated with recombination current, while higher values correspond to diffusion current.

5.3 Experimental results and discussion

5.3.1 Current-voltage characteristics of porous silicon

The d.c. electrical measurements were made in the dark on a number of samples of metal/PS/p-Si/Al structures with PS typical thickness of 5-25 μm. The thickness of the metal (Al or Au) coated on top of the PS layer was about 50 nm. The active area of the devices were approximately 0.3 cm^2.

Figure 5.4 displays a typical $I(V)$ characteristic of a Al/PS/p-Si/Al structure, taken at room temperature (292 K) with PS layer thickness of about 5 μm. The thickness of the sample was estimated using the SEM study of a PS sample fabricated with the same fabrication conditions as explained in the last chapter. The characteristics are found to be reversible and reproducible, and show a rectifying behaviour with a rectification ratio (r) of 29. Measurements were also performed on structures fabricated under different conditions using various anodisation currents and post-anodisation treatments. The $I(V)$ characteristics exhibit similar rectifying features as shown in Fig. 5.5 for the same structure with PS layer thickness of about 10 μm. The use of gold as a top electrode produced no major effects on the measured $I(V)$ characteristics. This observation is in agreement with the results obtained by Pulsford et al (1994) for forward bias turn on current through similar structures obtained with calcium, magnesium and antimony as a top electrode material. It has been found that the current turns on at the same value irrespective of the metal used as a top electrode. On the other hand, these results are in contrast with the results found by Simons et al (1995) for metal/PS/n-Si/Al structure. They have observed that a rectifying Schottky barrier formed when Au was used as a top electrode material, while using Al as a top metal contact with PS leads to an ohmic behaviour. The present results, together with these

observed by Pulsford et al (1994), indicate that the interface between the metal and PS layer may not be responsible for the observed rectification behaviour.

In general, this type of non-linear dependence of the forward current I on the applied bias voltage V at a temperature T is given by equation (5.12). As was mentioned in section (5.2.2), this equation is a generic one and can be used to describe the conduction through a barrier at both pn junctions and metal-semiconductor Schottky contacts. Hence, it can be applied to the PS structure regardless of the structure models applied (metal-PS contact or pn junction between the PS and the silicon substrate). In order to achieve a better understanding of the transport mechanism across the PS/Si junction, the $I(V)$ characteristics were studied in the temperature range between 150 and 300 K (room temperature). Figure 5.6 shows a set of typical $I(V)$ characteristics at six different temperatures for the same sample as in Fig. 5.4. The reverse current does not appear to be saturating but shows voltage dependence. This may be indicative of carrier transport through a heterostructure.

The series resistance R_s and the ideality factor n are used in equation (5.12) as adjustable parameters in order to obtain a theoretical fit to the experimental curves. The factor $\left[1-\exp\left(-\frac{qV}{kT}\right)\right]$ is found to be the most effective within the reverse bias range and the forward voltage regime up to $\frac{3kT}{q}$ where the series resistance R_s becomes extremely small [Chand and Kumar 1995]. Then, equation (5.12) is reduced to the law governing diffusion current due to thermionic emission for $n=1$ and $R_s=0$.

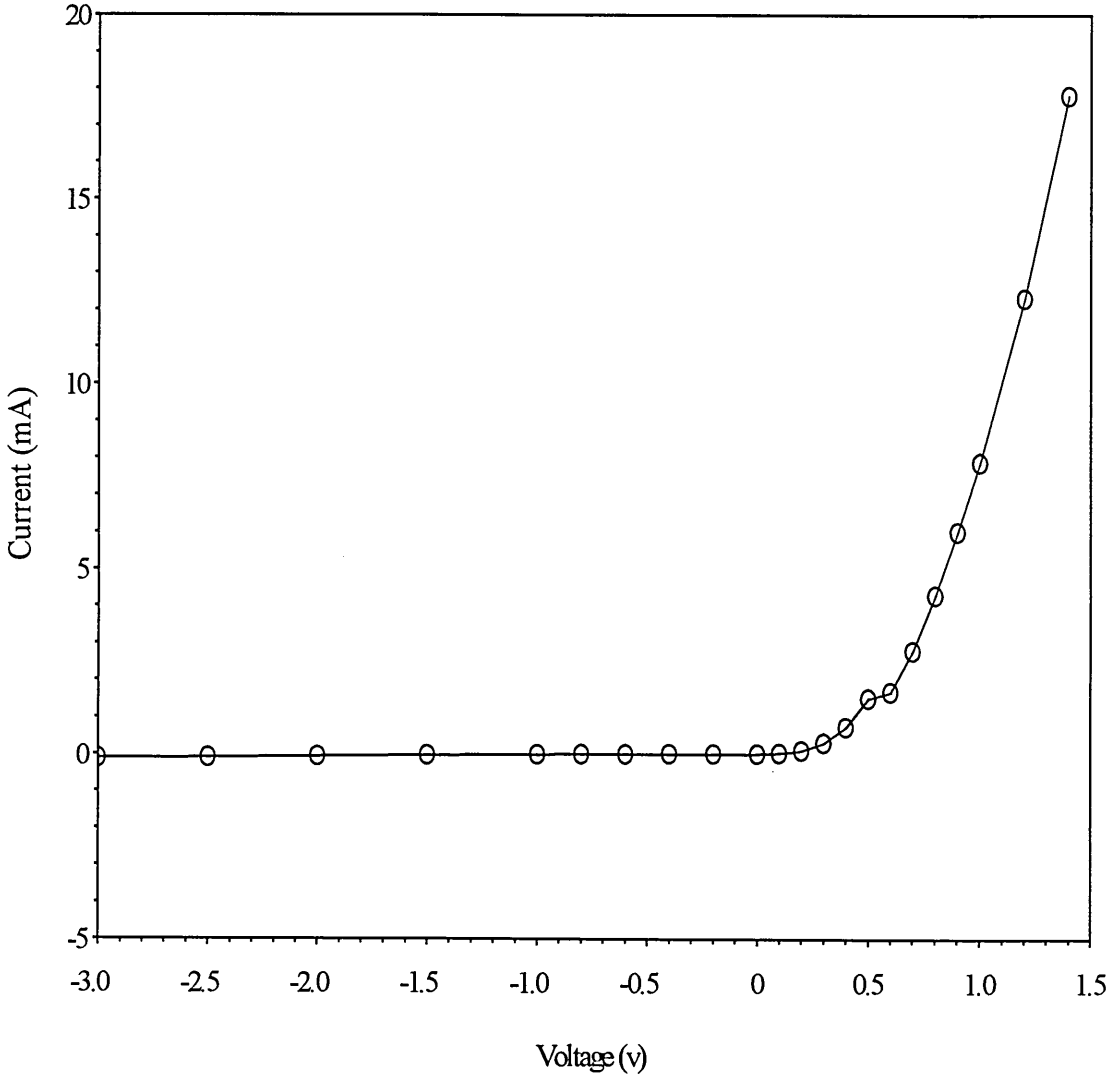


Figure 5.4 Dependence of the current (I) on the applied voltage (V) for Al/PS/p-Si/Al structure at room temperature. The thickness of the PS layer is about 5 μm.

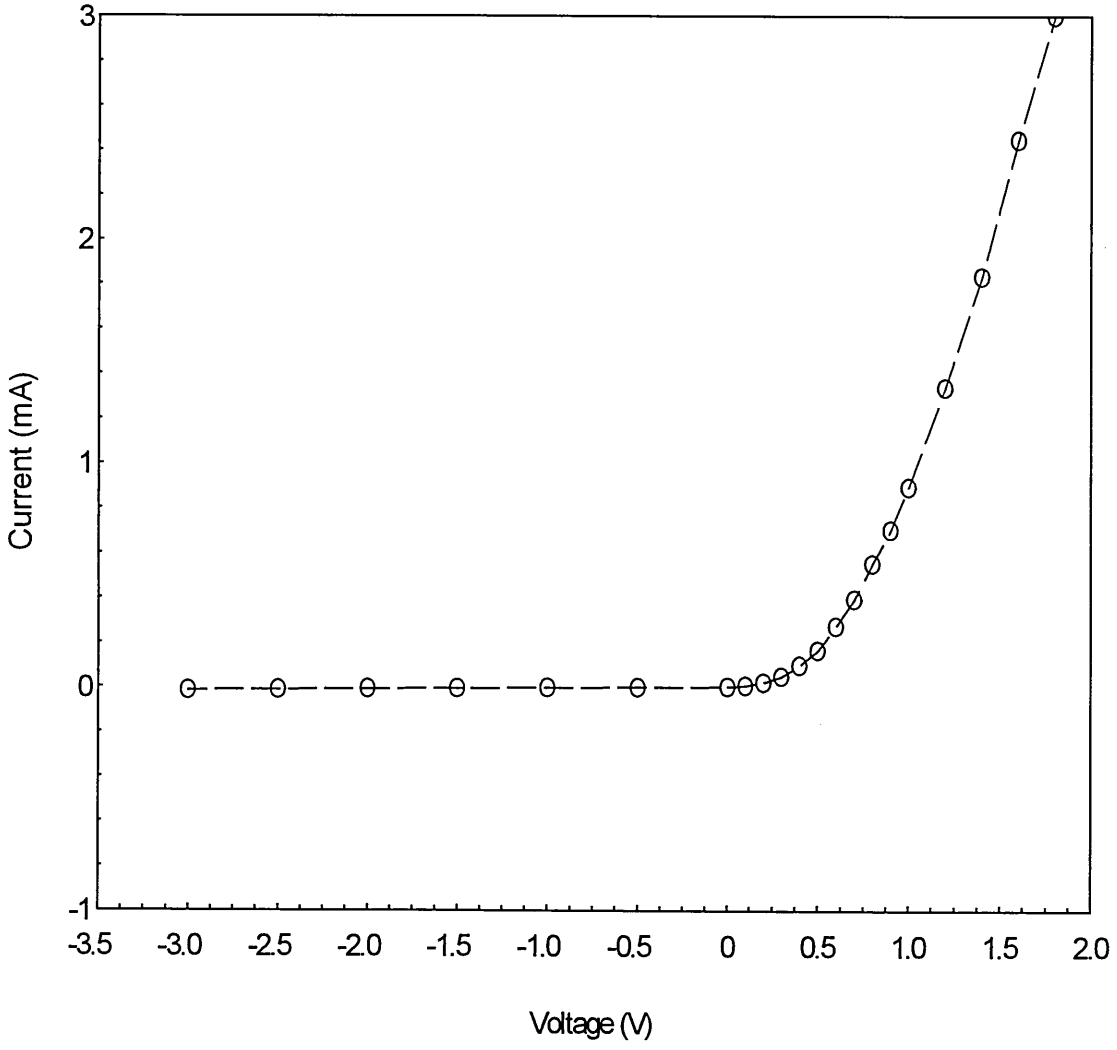


Figure 5.5 Dependence of the current (I) on the applied voltage (V) for Al/PS/p-Si/Al structure at room temperature. The thickness of the PS layer is about 10 μm.

Temperature	r at 0.2 V	n	I_s
152 K	6	1.13	0.72 pA
192 K	10.5	1.072	38 pA
212 K	12.8	1.05	200 pA
252 K	18.4	1.033	29 nA
272 K	25.3	1.023	140 nA
292 K	29	1.01	250 nA

Table 5.1 Electrical characteristics of Al/PS/p-Si/Al structure with PS layer thickness of about 15 μm.

Figure 5.7 shows a plot of $ln\left[I\Big/\left\{1-\exp\left(-\frac{qV}{kT}\right)\right\}\right]$ against V at room temperature. The resulting graph is linear within a voltage range of $-3.0V \le V \le 0.4V$ and the value of n is found from the slope of the linear portion of the graph. By substituting the values for n and I_s into Equation (5.12), an approximate value of R_s is obtained. A least squares fitting procedure is then set up with these starting values for the adjustable parameters in order to achieve a satisfactory convergence between experimental and theoretical data at different temperatures over a wide range of bias voltage (see Appendix A for the fitting program). Similar calculations were performed for the remaining temperatures and values of R_s and n are obtained with the standard error less than 5%. The estimated values of n and I_s is given in table (5.1).

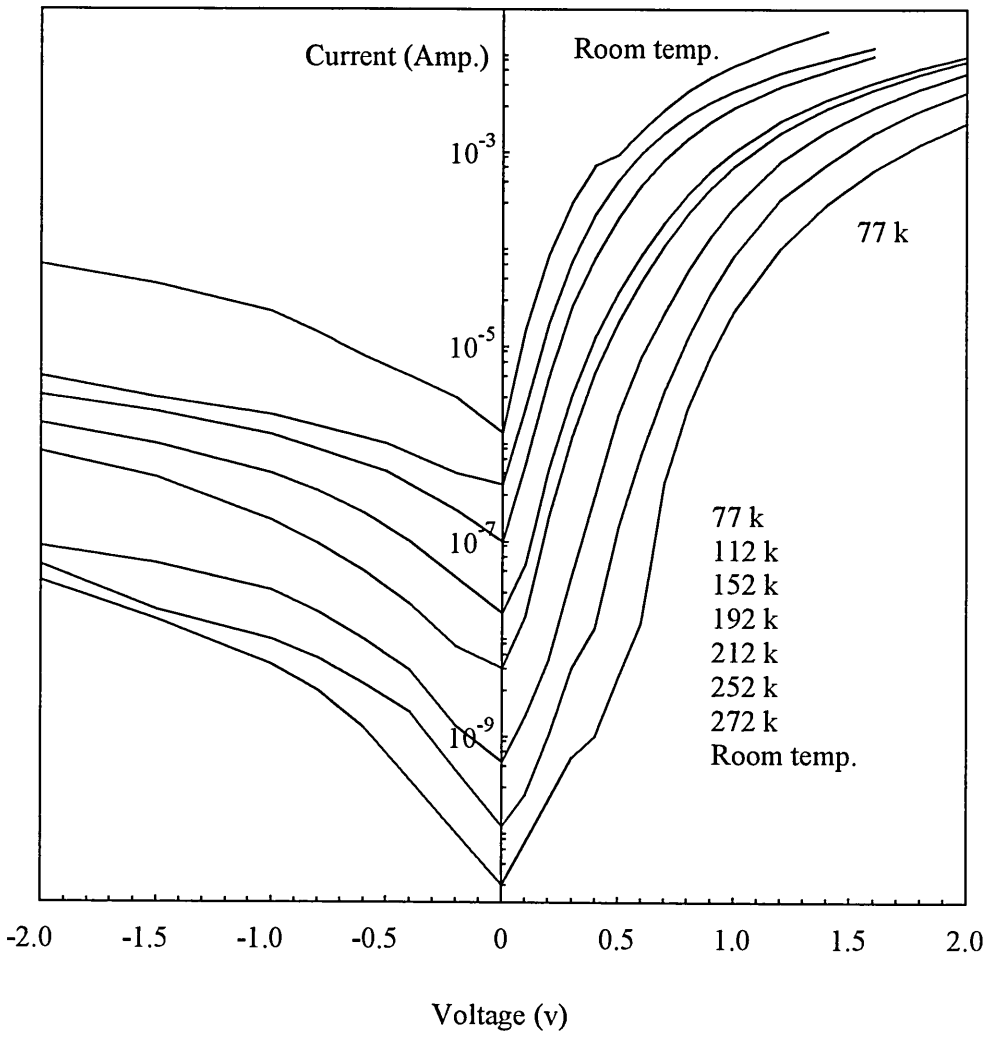


Figure 5.6 Current-voltage characteristics of Al/PS/p-Si/Al structure at different temperatures ranging from 150 K to 293 K using the same PS sample as in Fig. 5.4.

Figure 5.8 shows the dependence of the series resistance R_s and the ideality factor n on temperature T between 150K and 300K. R_s is believed to be decreasing with temperature T in an exponential manner of the type: $R_s = R_0 \exp\left(\Delta E_R / kT\right)$ with $R_0 = 0.28\Omega$ and $\Delta E_R = 0.19eV$. The sharp increase of R_s for temperatures below 200 K is believed to be due to the lack of charge carriers at low temperatures. It is found that $n = 1.13$ at $T = 150K$ while $n = 1.01$ at $T = 290K$. This indicates that the departure from ideality is not significantly large. Similar results were found for the same PS structure with PS layer thickness of 10 μm. Higher values of n were calculated using the standard diode equation (5.6) [Mabrook et al 1995]. Similar value of ideality factor was reported by Pacebutas et al (1995) for Al/PS/p-Si/Al structure using as-anodised PS layer, while lower values of n (n = 2) were calculated after removing the top nanoporous layer from the as-anodised samples. A value of 1.8 was reported by Dittrich et al (1996) as an ideality factor for PS devices fabricated from n-type silicon substrate. They concluded that the junction responsible for the rectifying behaviour of the device is that between the PS and the metal contact.

As shown in Fig. 5.8, the plot of n versus T^1 gives a linear relationship with slop of 0.897 instead of 1 as expected from equation (5.13). This suggest that for a practical pn junction, the unity in equation (5.13) should be replaced with a constant n_o which can be calculated from the slop of nT versus T plot. Hence, equation (5.13) should be written in the form:

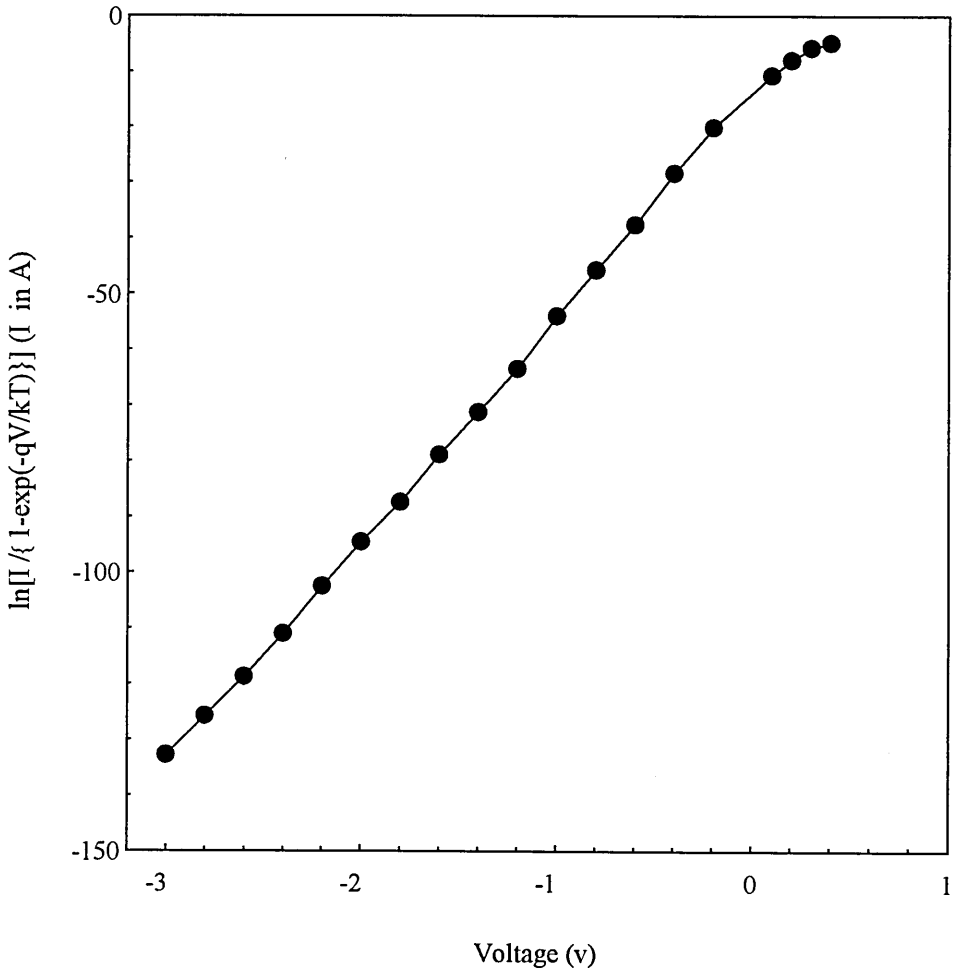
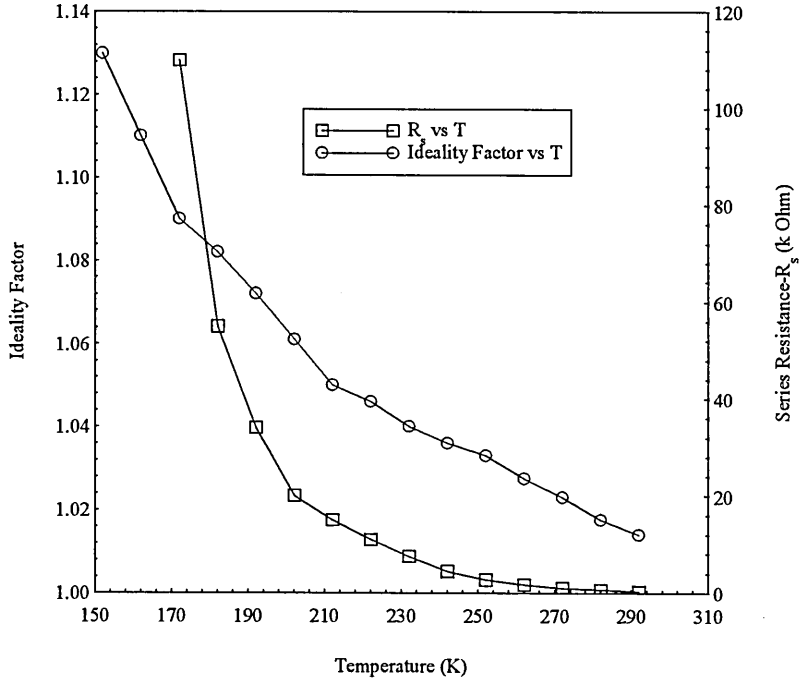
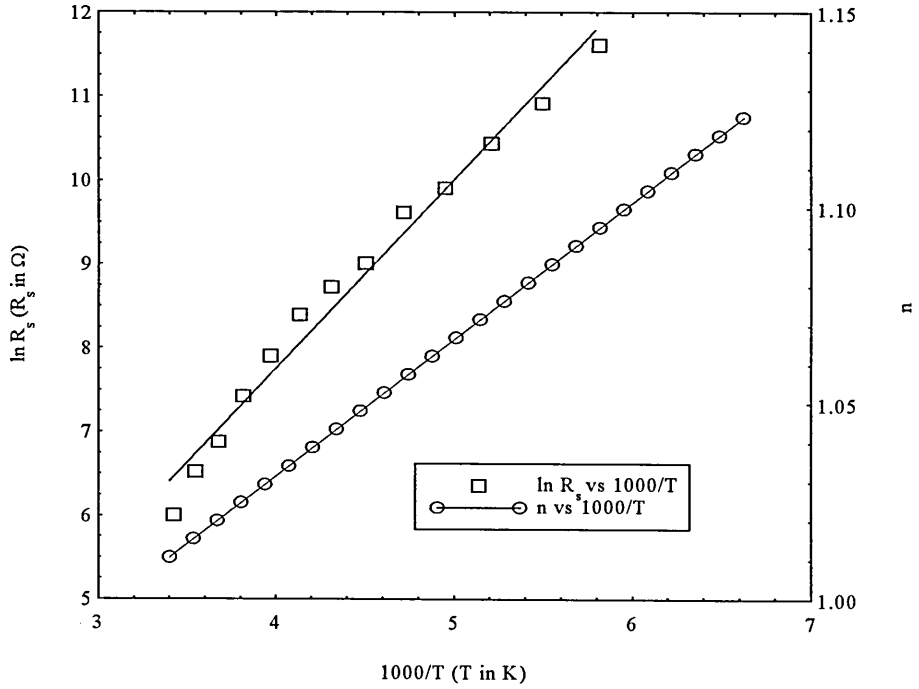


Figure 5.7 Logarithmic plot of I/[1-exp(-qV/kT)] for the same structure as in Fig. 5.4.



(a)



(b)

Figure 5.8 The variation of the ideality factor (n) and the series resistance (R_s) with respect to (a) Temperature (T) and (b) 1000/T, for the same structure as in Fig. 5.4.

$$n = n_o + \frac{T_o}{T} \tag{5.18}$$

Usually, the value of n_o should be very close to the average value of the ideality factor n over the whole temperature range. Figure 5.9 shows the plot of nT versus T for the same structure of Fig. 5.4, giving values of n_o and T_o as 0.897 and 34 K respectively. The same calculations were made for different PS samples with different fabrication conditions and different thicknesses giving values of n_o close to unity for all samples. Values of n_o of 1.05 and 0.95 were found for PS structures with PS layer thickness of 5 and 10 μm respectively.

Assuming that the zero bias reverse current I_s is primarily due to thermionic emission, the general behaviour of I_s can be written as in equation (5.7). Figure 5.10 (curve (a)) shows the plot of $\ln(I_s/T^2)$ against T^{-1} for the same sample as in Fig. 5.4. The relationship appears to be nonlinear which indicate that the barrier height is temperature dependent. This nonlinearity could be due to the increase of ideality factor with decreasing temperature as explained in section 5.2. Therefore, the ideality factor n is introduced in equation (5.7) and the saturation current I_s can be written in a modified form:

$$I_s = A\,S\,T^2\,exp\left[-\frac{q\phi_b}{k(n_0T + T_0)}\right] \tag{5.19}$$

Figure 5.10 (curve (b)) shows a plot of $ln(I_s/T^2)$ against the reciprocal of the product of ideality factor and temperature (nT). The resulting graph is found to be non-linear again, but it increases the linearity of the plot. Two dominant conduction

processes, however, are believed to exist, giving values of 0.70 eV and 0.22 eV for the activation energy corresponding to high and low temperature regimes, respectively. The transition between the two regimes is not abrupt but takes place gradually. There is a tendency for convergence between the two curves in Fig. 5.10 at high temperatures and therefore it appears that thermionic emission diffusion processes are predominating at high temperatures. This observation is in agreement with the fact that the ideality factor n approaches the value of unity at high temperatures (see Figure 5.8). The relatively small value of activation energy at low temperatures is believed to be associated with recombination currents. These values of activation energies are in agreement with the results obtained for the PS samples made from n-type silicon substrates [Simons et al 1995, Dittrich et al 1996].

For further analysis, the value of ϕ_b was calculated by applying the midpoint rule as a function of temperature in Fig. 5.10. The room temperature value of ϕ_b was found to be 0.7 eV. This is similar to the value found by Dittrich et al (1996) for Au/PS/n-Si/Al structure. The barrier height was found to increase monotonically with temperature as shown in Fig. 5.11. The least square linear approximation to the experimental data of ϕ_b versus T can be written as:

$$\phi_b = \phi_b(0) + \alpha T \tag{5.20}$$

where α is the temperature coefficient of the barrier height. The value of α according to this fitting is estimated to be $4.3\,\mathrm{meVK}^{-1}$.

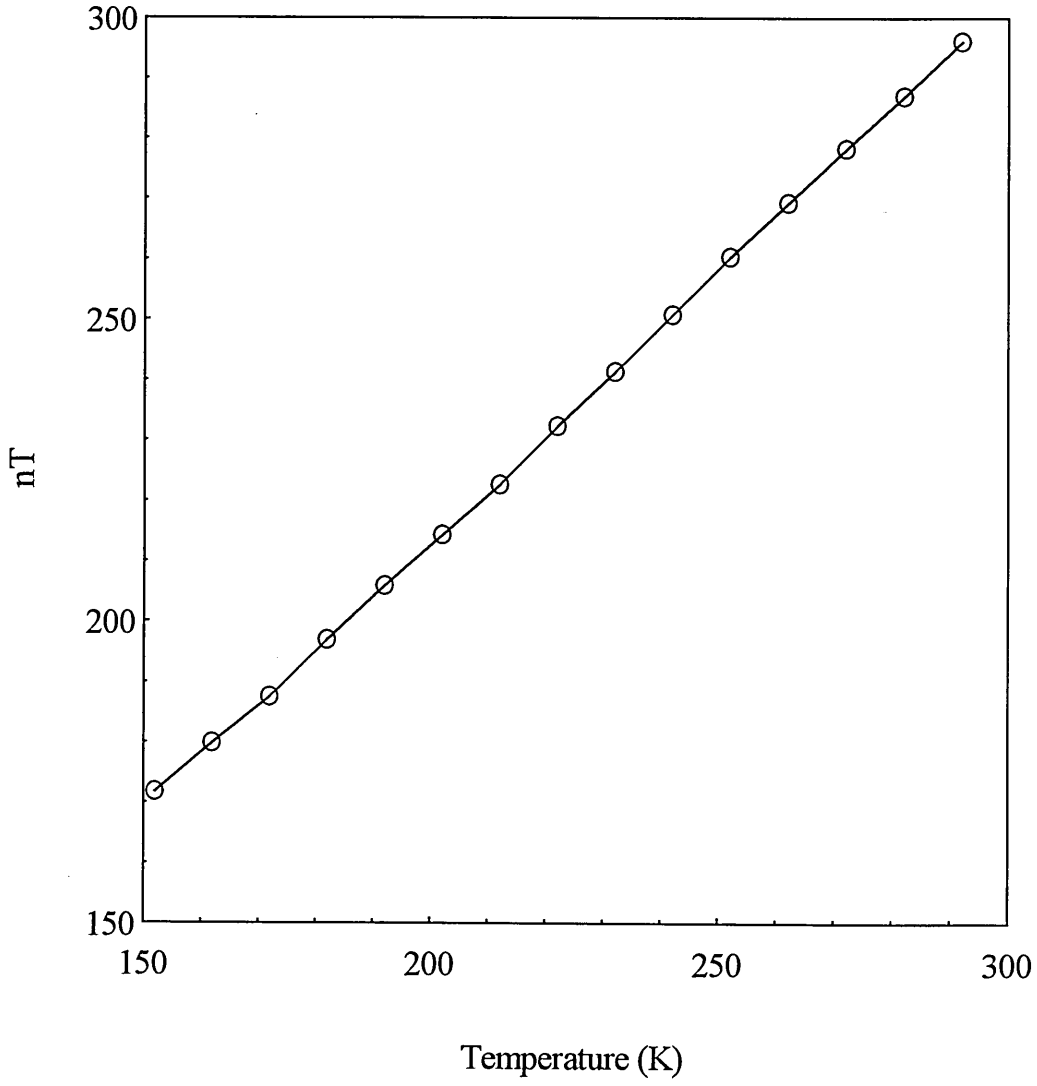


Figure 5.9 Plot of nT versus T for the same sample of Fig. 5.3.

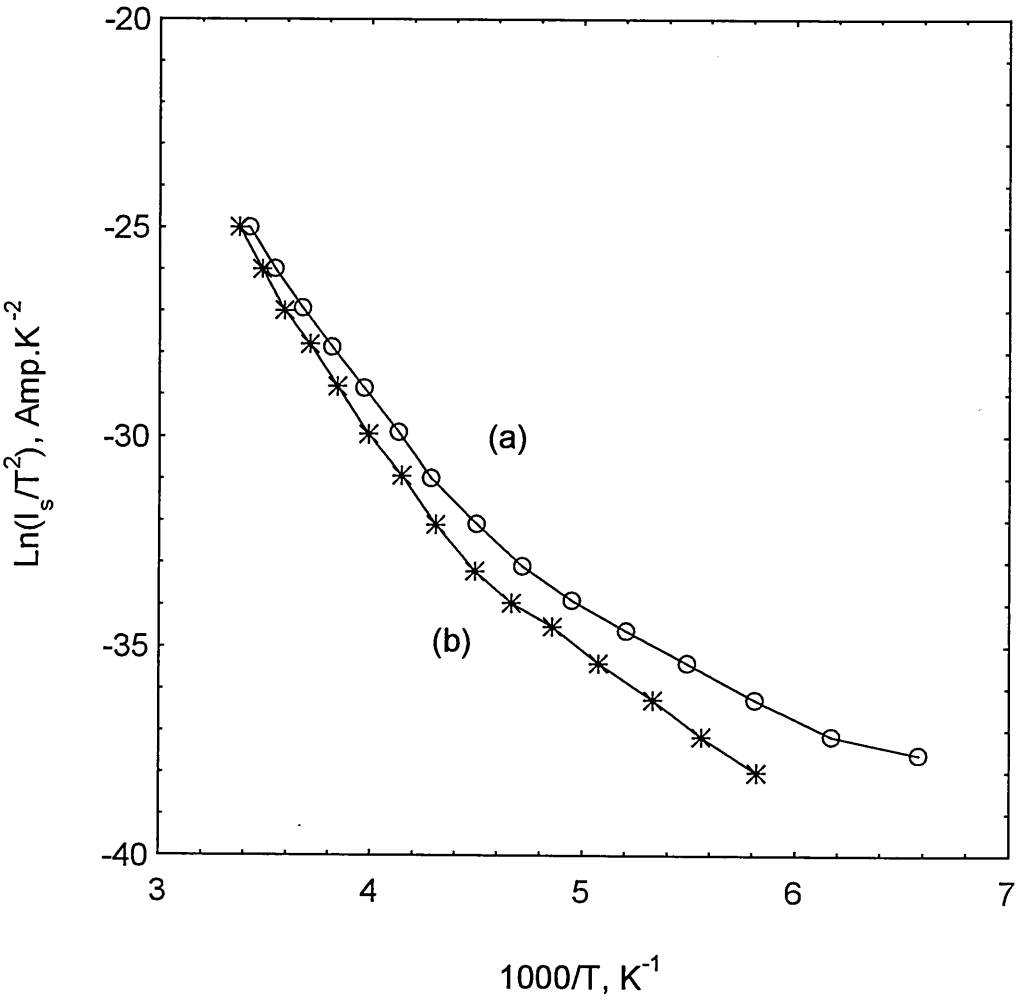


Figure 5.10 Plots of $\ln(I_s/T^2)$ against (a) the reciprocal of T and (b) the reciprocal of nT.

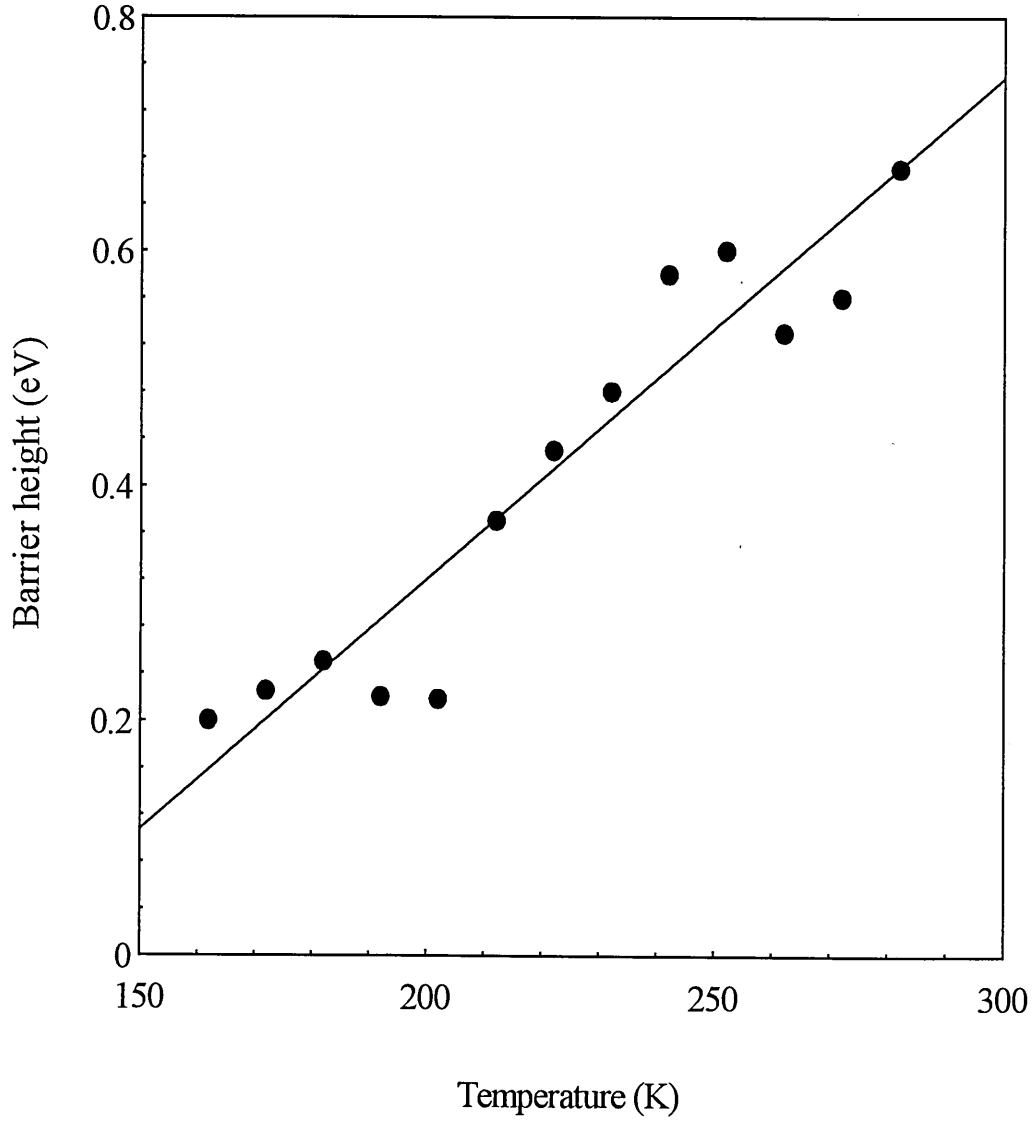


Figure 5.11 The temperature dependence of equilibrium barrier height ϕ_b for the same structure as in Fig. 5.3

The forward current characteristics for the same sample were fitted to the standard diode equation (equation 5.6) for the sake of comparison. The values of n and I_s were estimated from the slope and the intercept of the plot of ln$I$ against applied voltage V. Figure 5.12 shows an example of the plot at 272 K for the same sample used in Fig 5.4. Similar results were observed for different samples made with different fabrication conditions. The values of n obtained according to this method were found to be very high, with the best result of $n \approx 2.15$. Higher values of n were calculated for different samples and it could reach as much as 11.5 in some cases [Mabrook et al 1995]. These results are supported by the same observation found by different researchers. Koshida and Koyama (1992) found that the rectifying behaviour of the light emitting devices based on PS could be resulting from a combination of a Schottky junction between the metal and PS and a hetrojunction between PS and silicon substrate. They described the ideality factor of their devices as quite high (more than 10 for most of the devices). Lower values of ideality factor of about 3.2 were reported by Simons et al (1995) for Au/PS/Al structure which were found to be similar to those for Au/PS/n-Si/Al structure as the junction between Au and PS is responsible for the current limitation in the device. PS devices with ideality factor approaching the value of 10 were also reported by Namavar et al (1992), but they ascribed the rectifying behaviour of their devices to the pn hetrojunction between the metal (ITO) and the PS layer.

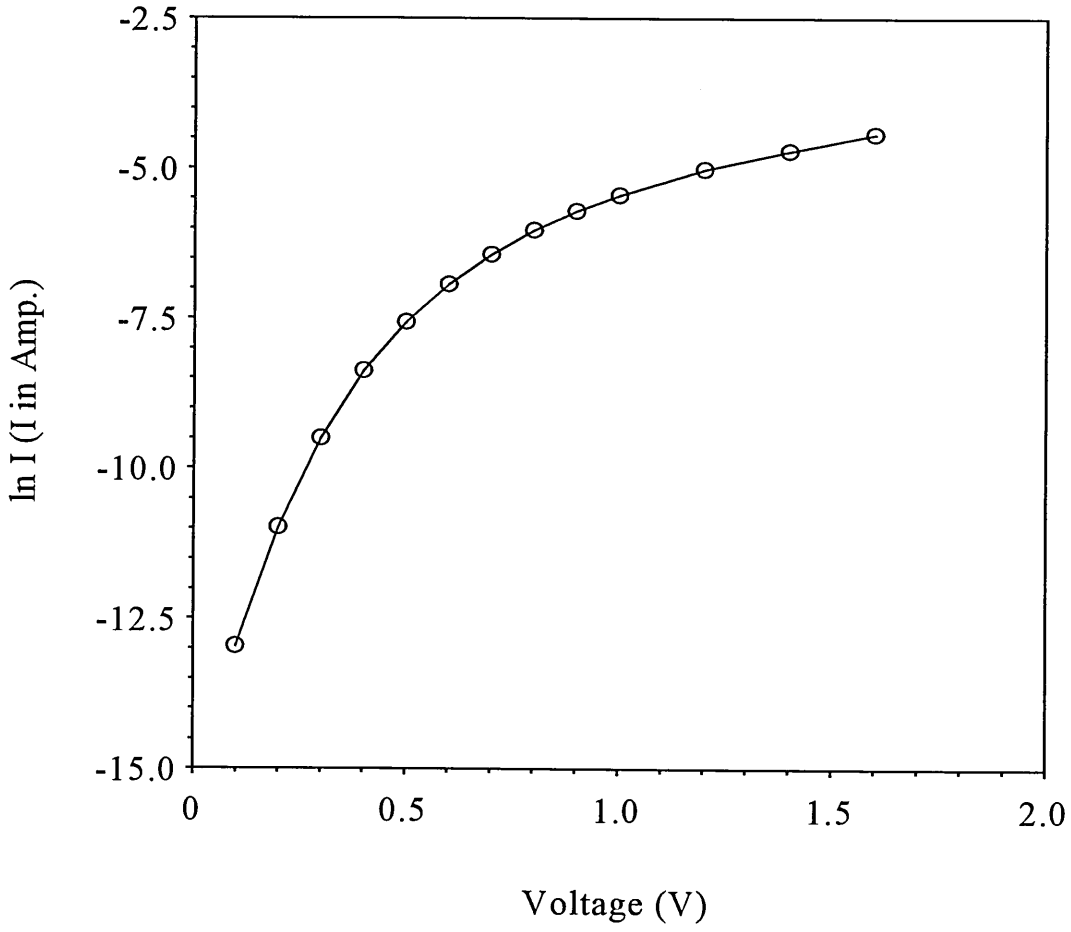


Figure 5.12 Plot of ln I against V for the same structure as in Fig. 5.3.

5.3.2 The band structure of porous silicon

The surface of silicon is usually positively charged due to the presence of surface states either on the silicon surface or in the native oxide. It is, therefore, expected that the surface is depleted of majority carriers which are holes. In p-type materials, the depth of the depletion region, which depends on carrier concentration and surface charge of silicon, extends over a distance of a few tenths of a micron into the silicon. Taking into account the fact that silicon rods in PS film have a thickness in the nanometer range, which is at least two order of magnitude less than the depletion width, it can be easily inferred that the bulk of PS is depleted of holes. Depleted PS forms an ohmic contact with the Al top electrode. It should be noted that the Au film as a top electrode, having much higher work function (ϕ_m = 5.2 eV) than Al (ϕ_m = 4.3 eV), does not make a significant difference in the $I(V)$ characteristics. The nature of porous silicon implies the very large effective surface area and consequently the large concentration of dangling bonds as shown in Fig 5.13. The dominance of a very high surface charge density in PS is expected to fix the Fermi level to a certain position near the conduction band edge.

According to the present results, a band model is presented in Fig. 5.14 in order to account for the conduction in Al/PS/p-Si/Al devices. The validity of this model can be justified in the light of reported results from the measurements of short-circuit photocurrent when a laser beam is scanned across the cleaved edge of the PS layer [Pulsford et al 1994]. The photo-excitation at the interface between the metal and PS layer and across the PS layer produces no response, but a sharp increase in photoinduced current is found to have occurred when the region just inside the silicon

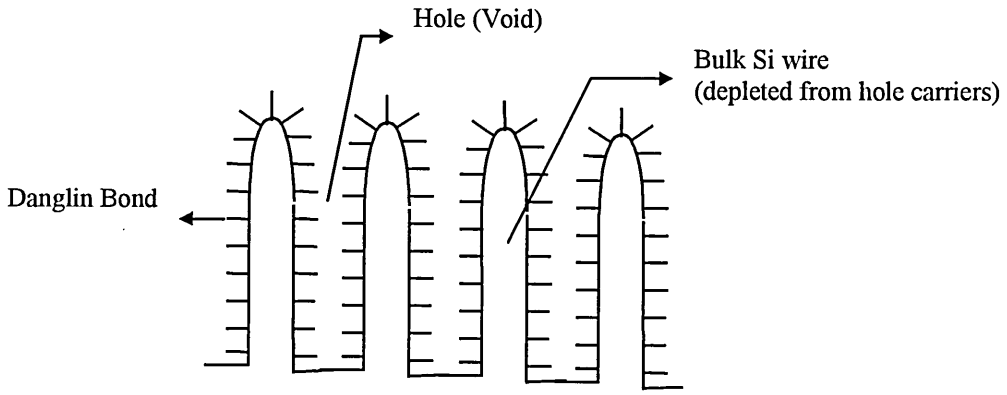


Figure 5.13 Schematic distribution of dangling bonds in porous silicon film surface

substrate is illuminated. This band structure has also some similarities with the heterojunction model proposed for photoelectronic properties of the PS layer in which the PS layer is assumed to have a much wider band gap than bulk silicon [Stievenard and Deresmes 1995]. Al layers form a Schottky contact with p-type silicon substrate giving a blocking contact for holes but ohmic for electrons. The electron current though the system is controlled by the barrier between p-Si and the depleted PS, which can cause an observed rectification. The barrier height ϕ_b of 0.70 eV obtained experimentally, therefore, corresponds to the barrier between the p-Si substrate and PS layer. The temperature coefficient α of the barrier height ϕ_b can be written as:

$$\alpha = \left[\frac{\partial E_{F(PS)}}{\partial T} - \frac{\partial E_{F(p-Si)}}{\partial T} \right] \tag{5.21}$$

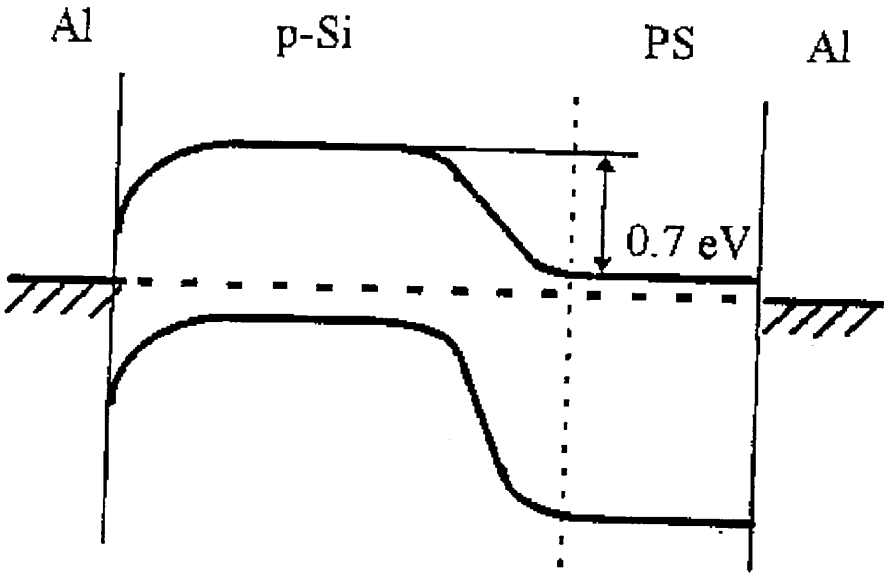


Figure 5.14 A band model for Al/PS/p-Si/Al structures.

where $E_{F(PS)}$ and $E_{F(p-Si)}$ represent the Fermi levels of PS layer and p-Si substrate. The value of the second term $\left(\frac{\partial E_{F(p-Si)}}{\partial T}\right)$ is estimated to be $0.7\,meVK^{-1}$. The value of $\left(\frac{\partial E_{F(PS)}}{\partial T}\right)$ is approximately equal to $5.0\,meVK^{-1}$. Because of the bandgap inhomogeniety, the Fermi level $E_{F(PS)}$ of porous silicon is, however, a spatially dependent quantity and it is, therefore, expected that there will be a distribution of values of $\left(\frac{\partial E_{F(PS)}}{\partial T}\right)$ over the interface. The value of $5.0\,meVK^{-1}$ is believed to represent an average of the coefficients for this distribution. The position of the Fermi level with respect to the conduction band in the PS layer is influenced by thermal generation of minority carriers. The series resistance R_s represents the net resistance of depleted PS and non-active region in the silicon substrate, and its value is also largely controlled by thermal generation of minority carriers (electrons) in PS layer. This is why an increase of the barrier height ϕ_b and a decrease of the series resistance R_s with temperature are observed.

5.3.3 Capacitance-voltage characteristics of porous silicon

The capacitance-voltage $C(V)$ characteristics of the same structures were also measured in the temperature range of 77-300 K. The frequency and the peak-to-peak amplitude of the sinusoidal test voltage were 100 Hz and 100mV, respectively. Figure 5.15 shows the capacitance dependence on voltage at room temperature of Al/PS/p-Si/Al and Al/p-Si/Al structures. Both samples have similar silicon substrate resistivity and active device area. The maximum of the peak can be referred to the position of the interface state relative to the Fermi level. The areas of the curves are proportional to

the charge density of the interface state. It can be seen from Fig. 5.15 that PS structure has more surface charge density than the silicon structure. This is expected as the nature of PS shows a very large surface to volume ratio compared to silicon. Figure 5.16 shows the $C(V)$ characteristics of Al/PS/p-Si/Al structures at different temperatures. The maximum of the peak for each curve shows again a strong shift of the Fermi level with changing temperature. This is similar to the results found from $I(V)$ characteristics of the same structure.

Figure 5.17 represents the plot of $1/C^2$ as a function of applied voltage for the same structure as in Fig. 5.15 at room temperature. The resulting graph shows linear behaviour, indicating that the heterojunction junction between p-Si and PS is abrupt and the voltage dependence of capacitance can be expressed as in Equation (5.14). From equation (5.15), the ratio of the intercept on the ordinate at $V = 0$ to the slope in Fig. 5.17 gives a value of 2.78 V for the built in potential V_b. This is a rather high value for built in voltage, but could be attributed to the high resistance and the band gap widening of PS. Using equation (5.15), the donor concentration N_D in PS was estimated to be 0.95 $x10^{16}$ cm^{-3}. The acceptor concentration N_A of the p-Si used, permittivity of the free space ε_o, the dielectric constants of silicon ε_1 and PS ε_2 are taken to be 1.5 x 10^{15} cm^{-3}, 8.85 x 10^{-14} Fcm^{-1}, 11.9, and 40, respectively.

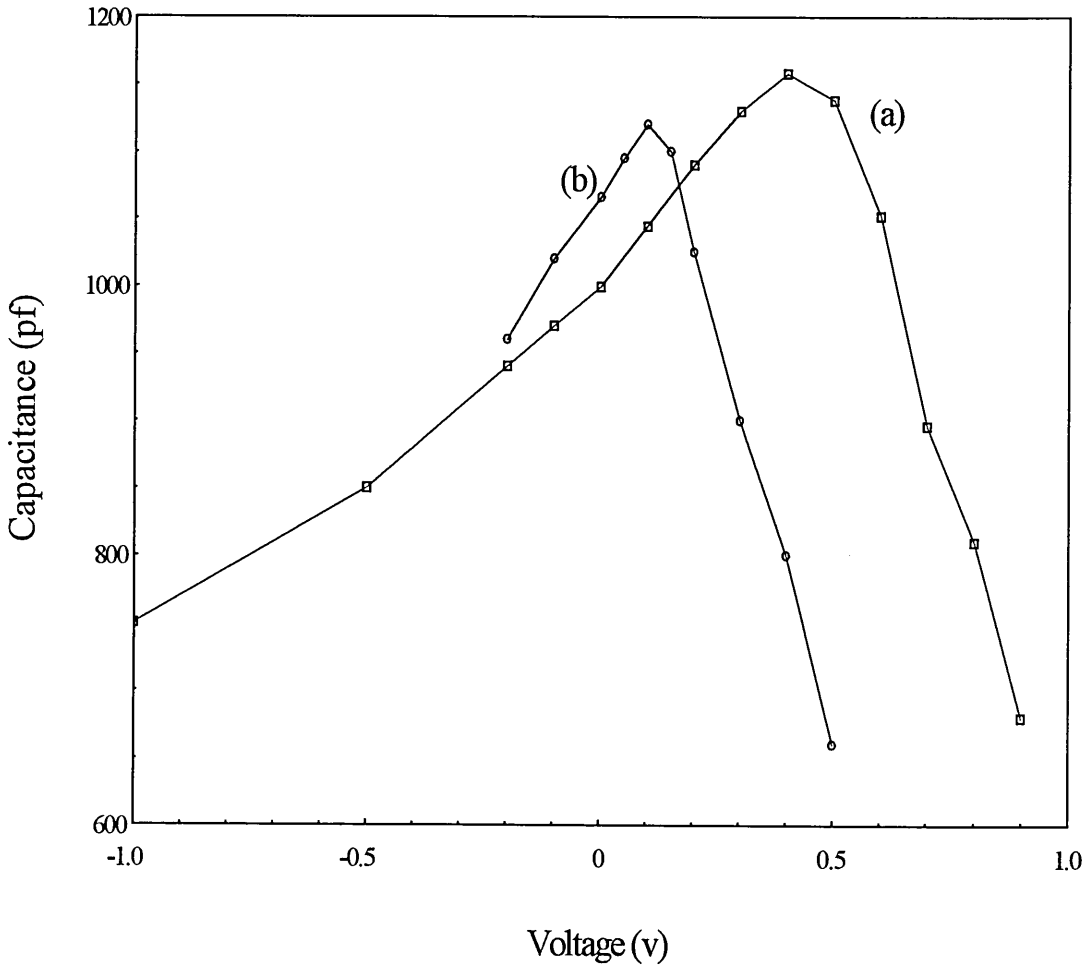


Figure 5.15 Capacitance-voltage characteristics of (a) Al/PS/p-Si/Al and (b) Al/p-Si/Al structures at room temperature.

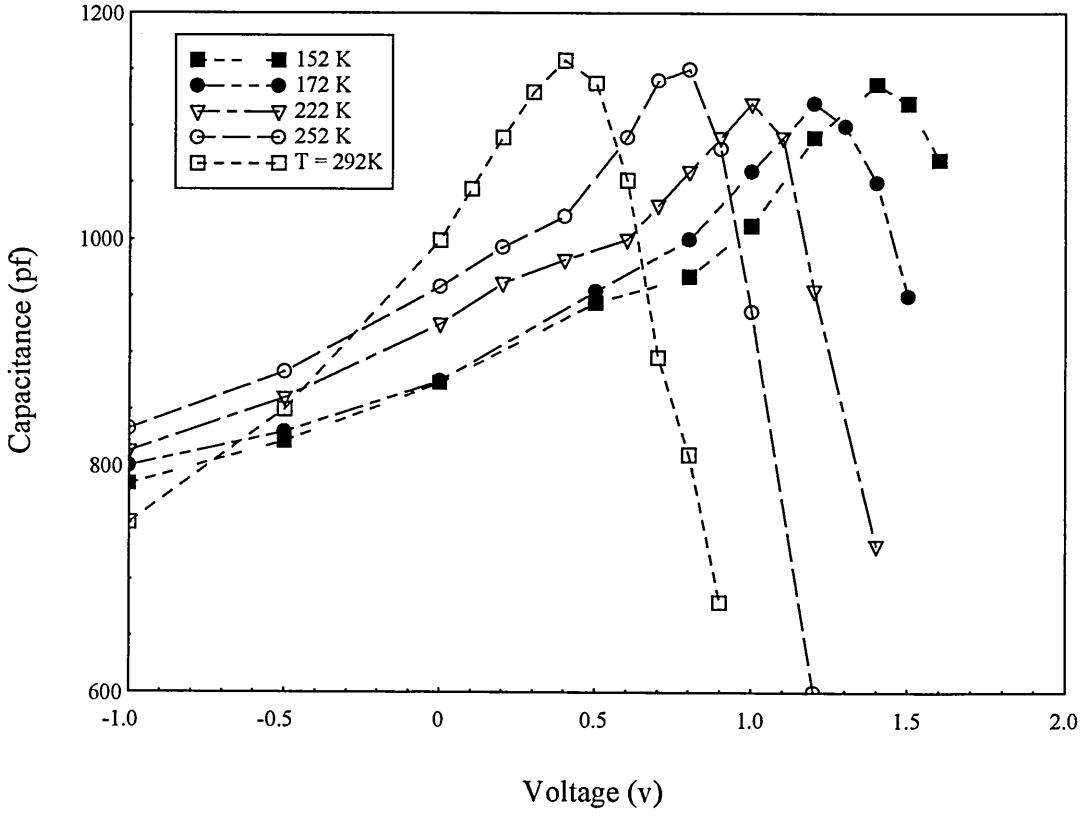


Figure 5.16 Capacitance-voltage characteristics of Al/PS/p-Si/Al structure at different temperatures using the same PS sample as in Fig. 5.15.

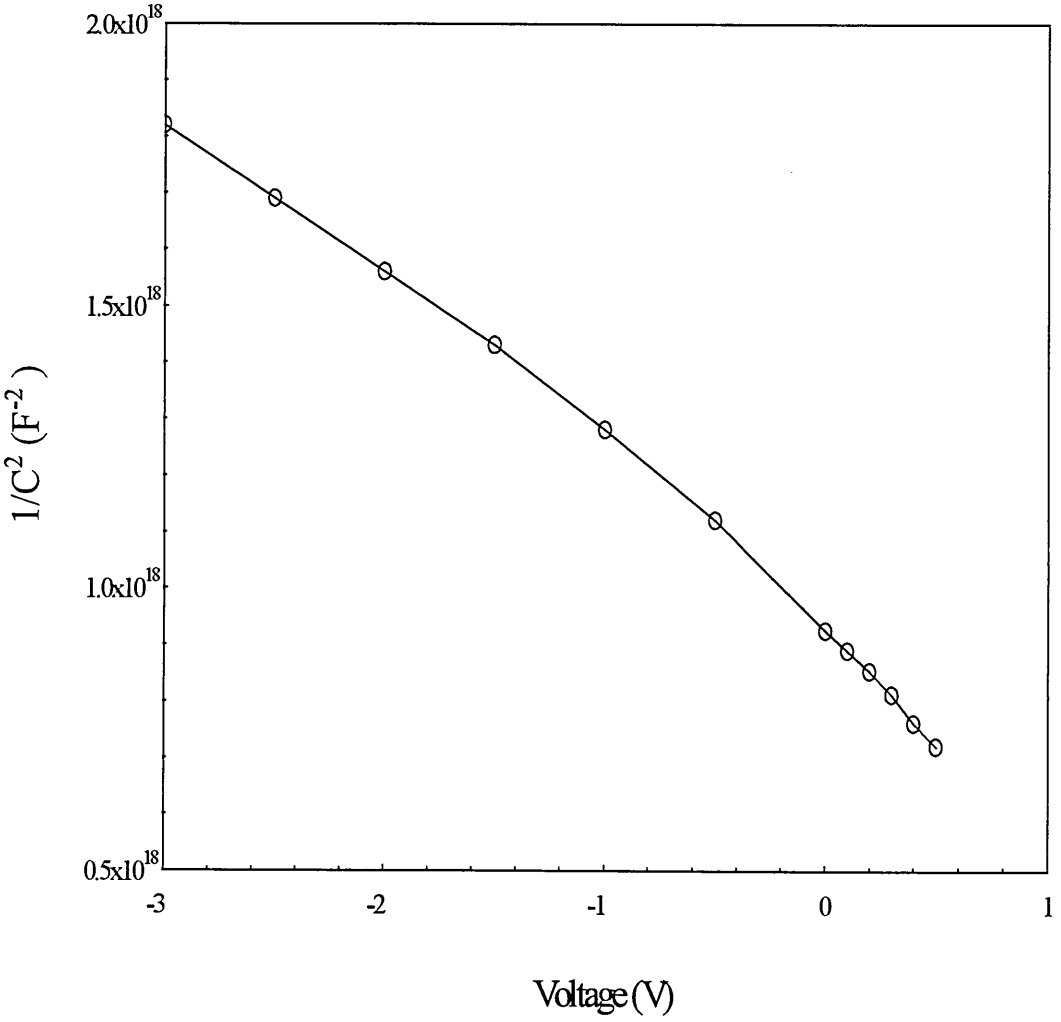


Figure 5.17 Dependence of $1/C^2$ on V for Al/PS/p-Si/Al structure at room temperature for the same PS sample used in Fig. 5.15.

CHAPTER SIX

AC ELECTRICAL PROPERTIES OF POROUS SILICON

6.1 Introduction

Valuable information about the properties of a dielectric material may be obtained by performing a.c. measurements over a wide range of frequencies and temperatures. Capacitance and conductance measurements would yield useful information concerning the loss mechanisms, permittivity and conduction processes in the material.

The first part of this chapter deals with general theoretical aspects of the a.c. conduction and the dielectric properties of dielectric material. The effect of the various parameters which control the conduction processes at different levels of applied electric field and temperatures will also be discussed.

The results of the a.c. conduction properties of light emitting devices based on PS are discussed. The dielectric properties of PS which have been derived from the conductance and capacitance measurements will be discussed in detail. Conduction mechanism models responsible for the a.c. conduction in PS will also be studied under a wide range of frequencies and temperatures.

6.2 Theoretical background

6.2.1 A.c. conduction

The total measured conductivity (σ_{tot}) at a given frequency ω contains d.c. and a.c. components and can be written as [Mott and Davis 1979]:

$$\sigma_{tot} = \sigma_{dc} + \sigma_{ac} \tag{6.1}$$

where σ_{dc} and σ_{ac} are the d.c. and a.c. conductivities, respectively.

Hence, the a.c. conductivity can be obtained by subtraction of the measured d.c. conductivity from the total conductivity measured at a frequency ω. In general, and for a very wide variety of crystalline and non-crystalline materials, the a.c. conductivity is found to increase approximately linearly with frequency for a very wide range of frequencies and can be expressed as:

$$\sigma_{ac} = A\,\omega^{s} \tag{6.2}$$

where ω is the angular frequency, A is a constant (in S/m/Hz), and s is an index which has a frequency and temperature dependencies [Elliott 1987].

Elliott (1977) proposed a model for the mechanism responsible for the a.c. conductivity in chalcogenide materials which has also been applied to many thin dielectric films including PS films [Ben-Chorin et al 1994, Parkhutik 1996]. This model considers the conductivity to be mainly caused by hopping of charge carriers between two sites over a potential barrier separating them. According to this model the value of the index s is usually between 0.5 and 2, whereas normal band type a.c. conductivity is expected to be dominating the conduction for the values of s less than 0.5 (a.c. conductivity is largely frequency independent).

However, we can gain a better idea about the conduction process by considering the temperature, as well as the frequency dependence of the electrical conductivity. The

a.c. conductivity σ_{ac} is generally weakly temperature dependent (in some cases it is almost completely temperature independent) at low temperatures which leads to a low activation energy in this range of temperatures. At high temperatures, the free band conduction process is usually responsible for the conduction in the materials as the electrons located at higher energy levels could be exited easily to the conduction band.

The a.c. conductivity according to Elliott's model is given by:

$$\sigma_{ac}(\omega)=\frac{\pi^2 N^2 \varepsilon}{24}\left[\frac{8e^2}{\varepsilon W_m}\right]^6 \frac{\omega^s}{\tau_o \beta} \tag{6.3}$$

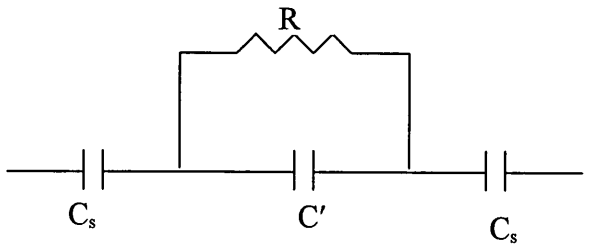
where N is the density of localized states, ε is the permittivity, τ_o is the effective relaxation time, e is the electron charge, and W_m is the barrier height separating two sites (can be approximately equated to the optical energy gap of the material). The term β is temperature dependent, tending to zero as the temperature (T) decreases. Additionally β is inversely proportional to the magnitude of the optical band gap W_m as

$$\beta = \frac{6kT}{W_m} = 1 - s \tag{6.4}$$

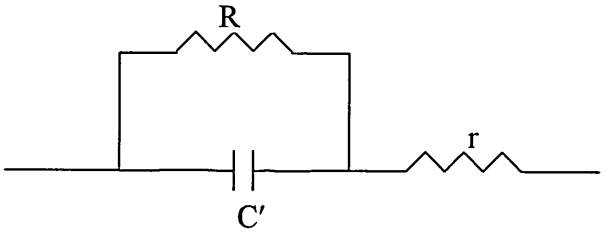
where k is Boltzmann's constant. Thus, the slight departure of the value of s from unity can be used to deduce the value of W_m. Usually the value of W_m is estimated from other data rather than using β through equation (6.4), since β is such a small quantity and susceptible to large errors [Elliott 1977].

6.2.2 Capacitance and Loss Tangent

Various equivalent circuit models have been presumed to describe the effects of frequency and temperature upon the capacitance and loss tangent of a thin film device. An early model proposed by Simmons et al (1970) describes the thin film structures in term of a temperature dependent resistance R shunted by a fixed capacitance and in series with two capacitances as shown in the equivalent circuit in Fig. 6.1 (a). In this figure, C_s is the capacitance of Schottky barriers expected when using blocking contacts and C' is the interior capacitance of the bulk.



(a)



(b)

Figure 6.1 Equivalent circuit representations from models of a.c. behavior in thin films. (a) Simmons model. (b) Goswami and Goswami model.

According to this model the measured series capacitance C is given by

$$C = \frac{C_s}{2}\left[\frac{1+(\omega C'R)^2}{1+\omega^2 C'(C_s/2+C')R^2}\right] \tag{6.5}$$

and the loss tangent (tan δ) is given by

$$\tan\delta = \frac{C_s}{2}\left[\frac{\omega R}{1+\omega^2 C'(C_s/2+C')R^2}\right] \tag{6.6}$$

The temperature dependence of the a.c. properties is determined through the variation of the interior resistance R via a thermal activation process described by

$$R = R_o \exp\left(\frac{E_a}{kT}\right) \tag{6.7}$$

where R_o is a constant, E_a an activation energy and T is the absolute temperature. In this model, the loss tangent (tan δ) is predicted to have a maximum value at a particular frequency.

Later, Goswami and Goswami (1973) proposed another model to describe the dynamic characteristics of thin film structures. This model assumes the capacitor system to contain a single frequency dependent capacity element C' in parallel with a temperature dependent resistance R, and both connected to a series low value lead resistance r as shown in Fig. 6.1 (b). The total impedance of this circuit (Z) is given by

$$Z = \frac{R}{1+j\omega RC'} + r = \frac{R+r\left(1+\omega^2 R^2 C'^2\right)}{1+\omega^2 R^2 C'^2} - j\frac{\omega R^2 C'}{1+\omega^2 R^2 C'^2} \tag{6.8}$$

According to this model, and from the second part of equation (6.8) the measured series capacitance C is given by

$$C = C' + \frac{1}{\omega^2 R^2 C'} \tag{6.9}$$

From this equation we can predict the decrease of the measured series capacitance C with increasing frequency falling to a constant value of C' at high frequencies. The temperature dependence of the a.c. characteristics, according to this model, is determined through the same way as described by Simmons et al (1970). The loss tangent is expressed as

$$\tan\delta = \frac{\left(1+\frac{r}{R}\right)}{\omega R C'} + \omega r C' \tag{6.10}$$

The first part of equation (6.10) dominates the value of tan δ at low frequencies, whereas at high frequencies, the term $\omega rC'$ dominating the value of tan δ which then becomes directly proportional to frequency. Thus, the above equation predicts a decrease in tan δ at low frequencies and an increase in tan δ at high frequencies. This model predicts a minimum in loss tangent, as it could be seen from equation (6.10), at a particular frequency which can be expressed as

$$\omega_{min} = \frac{1}{C'(rR)^{1/2}} \tag{6.11}$$

6.2.3 Impedance spectroscopy

Impedance spectroscopy is the term given to the analysis of the dielectric properties of a material with respect to frequency and temperature. The analysis of the dielectric constant ε is very important in order to gain an understanding of the dielectric properties of any material. Generally, the dielectric constant can be written as a complex number with ε′ and ε″ being the real and imaginary parts respectively and both are frequency dependent.

$$\varepsilon = \varepsilon' - j\varepsilon'' \tag{6.12}$$

The real part, ε′, decreases from a maximum value at low frequencies to 1 at high frequencies and it represents the relative permittivity that we use in calculating the capacitance. The imaginary part, ε″, is zero at low and high frequencies and having a maximum value when $\omega = 1/\tau$, as τ is the relaxation time, and it represents the energy lost in the dielectric medium [Kasap 1997].

Considering the thin film structure as a capacitive system, then the admittance, *Y*, the reciprocal of impedance of the capacitive system, is given by

$$Y = j\frac{\omega A \varepsilon_o \varepsilon(\omega)}{d} \tag{6.13}$$

where *A* is the active area of the structure, *d* is the thickness of the structure, and ε_o is the absolute permittivity. Using ε as a complex number as was given in equation (6.12), equation (6.13) can be written as

$$Y=\frac{\omega A\varepsilon_o\varepsilon''(\omega)}{d}+j\frac{\omega A\varepsilon_o\varepsilon'(\omega)}{d}=G+j\omega C \tag{6.14}$$

where C is the measured capacitance and is given by

$$C=\frac{A\varepsilon_o\varepsilon'}{d} \tag{6.15}$$

and G is the measured conductance and is given by

$$G=\frac{\omega A\varepsilon_o\varepsilon''}{d}$$

or, as G is a quantity related to σ_{ac} by the sample geometry,

$$\sigma_{ac}=\omega\varepsilon_o\varepsilon'' \tag{6.16}$$

The loss tangent ($\tan\delta$) is the relative magnitude of ε'' with respect to ε'.

$$\tan\delta=\frac{\varepsilon''}{\varepsilon'} \tag{6.17}$$

Hence, from equations (6.16) and (6.17), it is possible to establish absolute values for both the real and imaginary parts of the dielectric constant from the conductivity and loss tangent data.

6.3 Experimental results and discussions

6.3.1 A.c. conduction of porous silicon

The a.c. electrical measurements were performed on porous silicon (PS) layers of typical thickness estimated to be in the range of 10-15 μm coated with thin metal contacts (Al or Au) of about 50 nm in thickness. The active area of the devices was found to be 0.2 cm^2. All measurements were taken in the dark and under vacuum better than 10^{-5} torr. The amplitude of the alternating signal was 100 mV peak-to-peak with a bias voltage $V = 0$.

The variation of the a.c. conductivity (with frequency at different temperatures (152 - 292 K) is shown in Fig. 6.2. It is clear that at low temperatures (below 200 K) and low frequencies the conductivity exhibits a significant frequency dependence following the general power law expressed in equation (6.2). However, as the temperature rises the conductivity becomes less frequency dependent and remains almost constant at room temperature for frequencies less than 10 KHz. Similar behaviour has been observed by several researchers for different PS samples (with different fabrication conditions) [Ben Chorin et al 1993, Parkhutik 1996].

The temperature dependence of the a.c conductivity is compared with that of the d.c. conductivity in Fig. 6.3 which represents the conductivity as a function of inverse temperature. Below a specific temperature, which increases with increasing frequency, the conductivity reaches a frequency dependent saturated value giving a low activation energy in the range of (0.08 - 0.15 eV). At high frequencies (1 MHz) the conductivity becomes temperature independent for the entire temperature range (152 - 292 K).

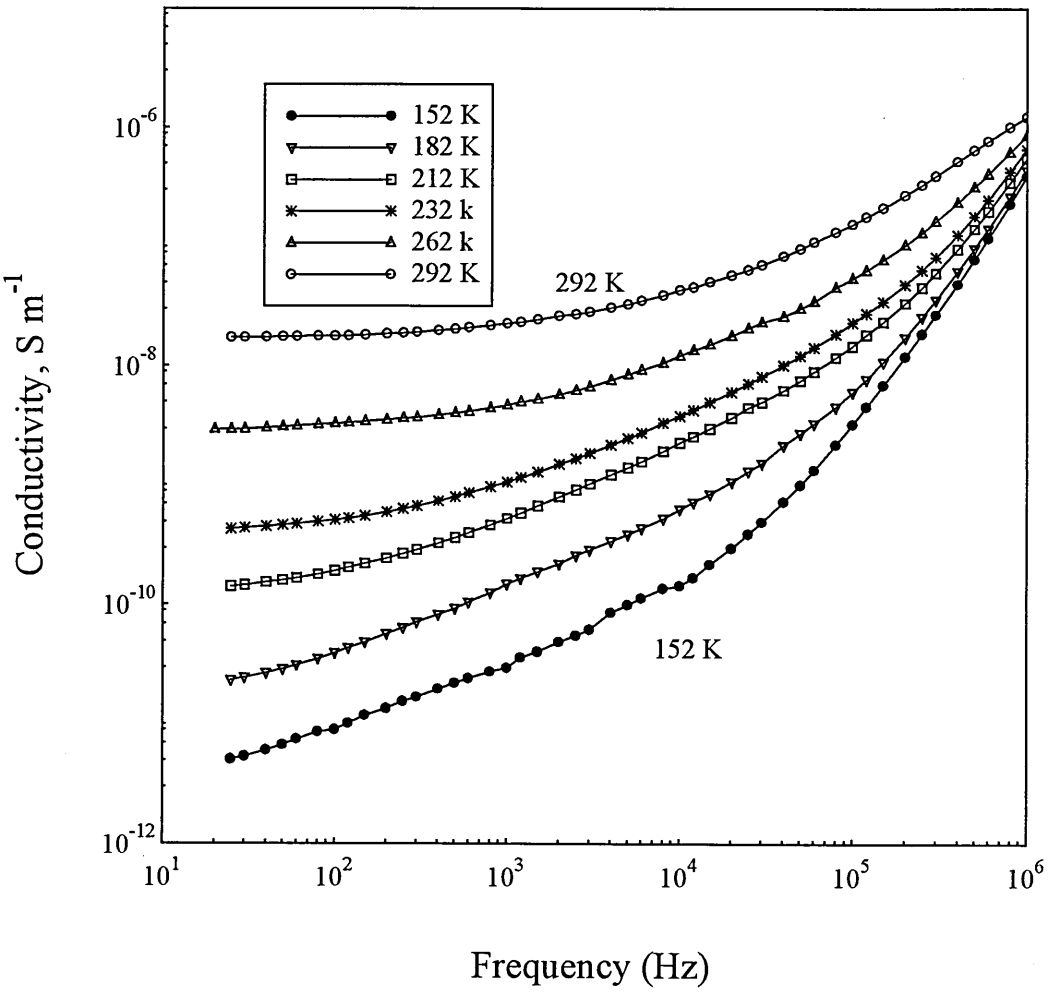


Figure 6.2 Frequency dependence of the a.c. conductivity of Al/PS/p-Si/Al structures at different temperatures

However, at high temperatures and low frequencies the conductivity changes exponentially and appears to have a thermally activated behaviour. The activation energy found to be frequency dependent and having values of 0.35 eV and 0.2 eV at low and high frequencies respectively at room temperature.

The values of *s* were derived from the slopes of $\log(\sigma_{ac})$ versus log(frequency) at different temperatures. The variation of the index *s* with the temperature is illustrated in Fig. 6.4 over two different frequency ranges. The values of *s* were generally found to decrease with increasing temperature, and moreover, it shows higher values at higher frequencies for a given temperature as shown in Table (6.1).

Frequency (Hz)	*152 K*	*182 K*	*212 K*	*242 K*	*272 K*	*292 K*
10^2 - 10^3	0.562	0.528	0.3	0.12	0.084	0.055
10^3 - 10^5	0.98	0.9	0.727	0.6	0.468	0.364

Table 6.1 The value of the index *s* as a function of temperature at two frequency ranges.

It may be observed from Figs. 6.2 and 6.4 that the conductivity can be expressed as a function of frequency according to equation (6.2) with the value of *s* not exceeding unity and decreasing with increasing temperature. The data shown in Fig. 6.2 indicate that there are two mechanisms responsible for the electrical conduction of PS.

At high frequencies there is a linear dependence of a.c. conductivity on frequency as the value of the index *s* is in the range of 0.6 - 1. This type of dependence might be ascribe to conduction by hoping of charge carriers between localized states through the

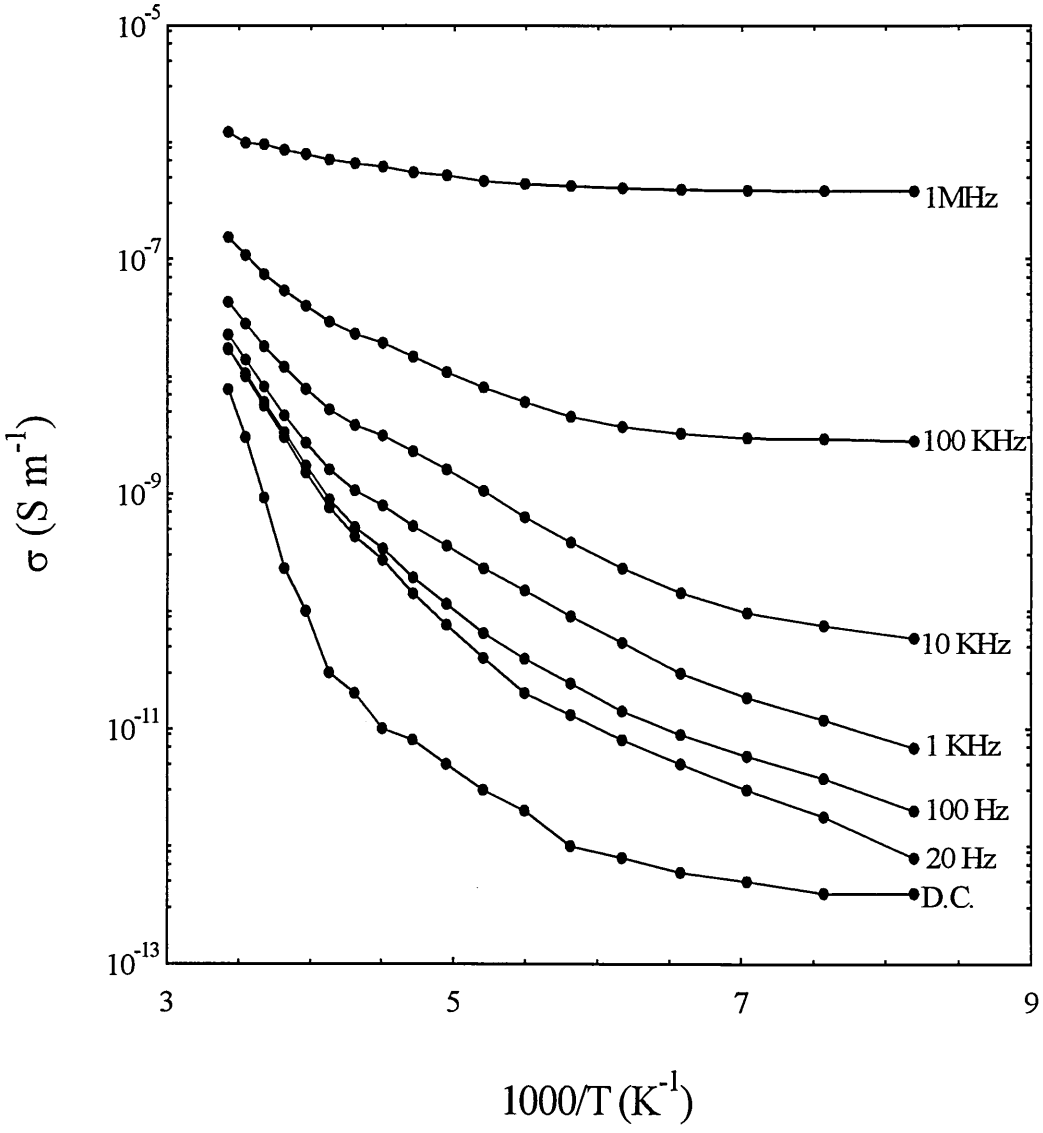


Figure 6.3 Dependence of a.c. conductivity on inverse temperature at different frequencies for the same structure as in Fig. 6.2.

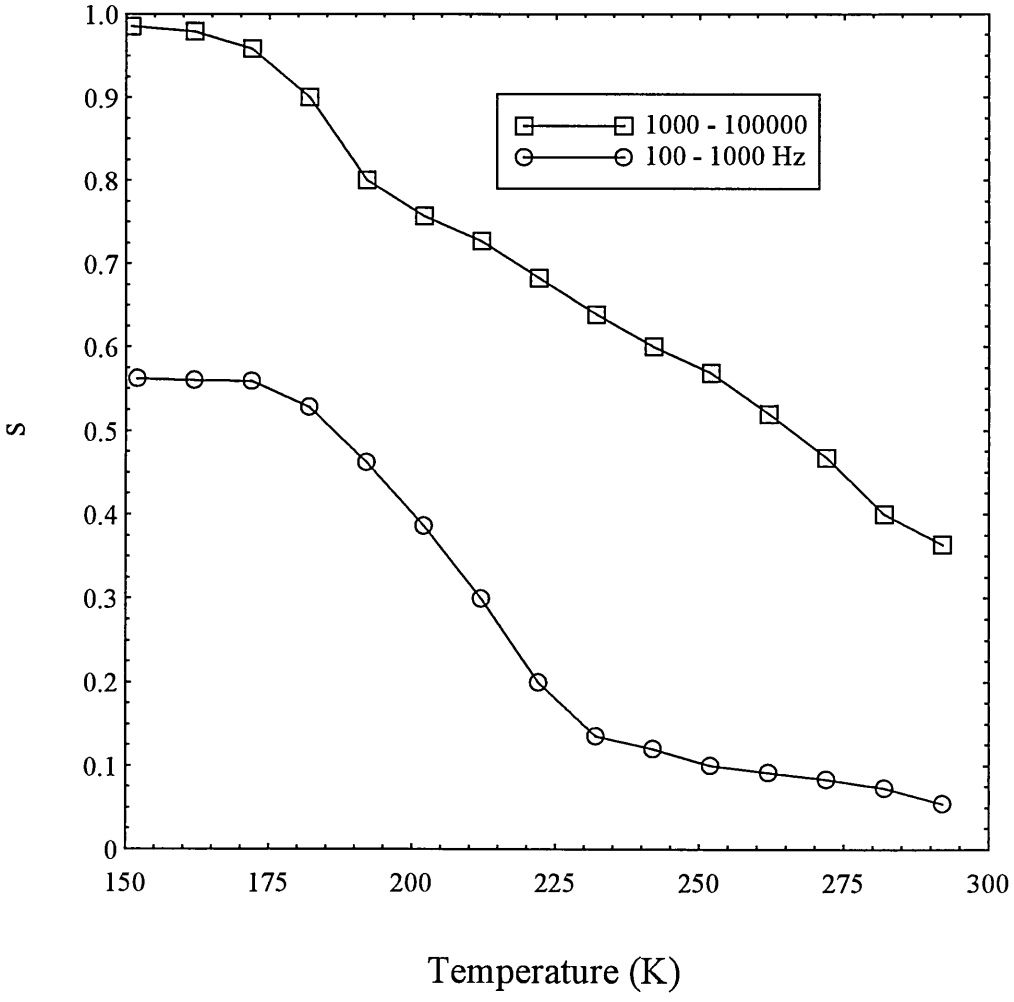


Figure 6.4 Dependence of the index *s* on temperature at two frequency ranges for the same structure as in Fig. 6.2.

PS layer. The values of s, particularly at low temperatures and high frequencies, are qualitatively consistent with the calculations based on the model of Elliott (1977). According to this model, the a.c. conductivity of PS is given by equation (6.3) and the index s is predicted to be temperature dependent following equation (6.4). Higher values of s were also observed at frequencies greater than 10^5 Hz approaching a value of 2 at very high frequencies and low temperatures. This kind of behaviour could be attributed to the experimental artifact related to the contact resistance [Mott and Davis 1979] or it could be related to some PS properties which are not clear at the moment. At low frequencies the conductivity shows less pronounced frequency dependence with the value of the index s less than 0.45. This indicates that the diffusion transport of charge carriers through the PS layer is the dominant transport mechanism. Similar results have also been reported for PS samples with Al layer on top as a contact layer [Ben Chorin et al 1993, Cruz et al 1998]. They concluded that for frequencies up to 10^4 Hz and at temperatures below 200 K the value of s is about 0.95. Ben Chorin et al (1993) also reported values of s exceeding unity at higher frequencies. The low frequency conductivity, with small values of s (of about 0.3), was also found by Parkhutik (1996) and attributed to the diffusion transport of charge carriers through the PS layer. The same conduction behaviour was found to be responsible for the conduction in amorphous silicon as the value of s is about 0.95 at low temperatures and high frequencies. It was attributed to the hopping of charge carriers transport mechanism as the value of the index s was found to be temperature dependent [Mott and Davis 1979, Grasso et al 1992].

The temperature dependence of the a.c. conductivity at low temperatures shown in Fig. 6.3 indicates that hopping of charge carriers dominates the conduction process as the activation energy is low and the conductivity increases with frequency. The values of

the activation energy E_a shown in Table (6.2) were calculated from the slope at each point of temperature at particular frequency in Fig. 6.3 as the a.c. conductivity σ_{ac} is believed to increase exponentially with the temperature T according to the following expression:

$$\sigma_{ac} = \sigma_o \exp(-E_a / kT) \tag{6.18}$$

where σ_o is the value of σ_{ac} at $1/T = 0$ and k is Boltzmann's constant.

At higher temperatures and low frequencies the activation energy is almost independent of frequency with an average value of 0.35 eV. This high value of activation energy indicates a free band conduction process resulting from charge carriers which are exited from energy levels within the forbidden gap. These values of activation energies are close to the values which has been found by Parkhutik (1996) for the as-formed (with no post-treatment) PS samples. He concluded that the activation energy for a.c. conduction of PS depends essentially on the quantity of HF acid solution remaining in the pores after the fabrication. He found a value of 0.08 eV in completely wetted PS samples (even at low frequencies) while in dry samples the activation energies could exceed 0.4 eV.

6.3.2 Capacitance and loss tangent measurements of porous silicon

The capacitance of PS films was measured as a function of frequency in the range 20 - 10^6 Hz at various temperatures, for the same sample as in Fig 6.2. At low temperatures (below 182 K) the capacitance is almost frequency independent, whereas at higher temperatures the capacitance decreases rapidly with increasing frequency and subsequently approaches the low temperatures value at high frequencies as shown in

Frequency	*E_a at Low Temperatures (< 240 K)*	*E_a at High Temperatures (> 240 K)*
20 Hz	0.19 eV	0.35 eV
100 Hz	0.16 eV	0.35 eV
1 KHz	0.136 eV	0.32 eV
10 KHz	0.13 eV	0.28 eV
100 KHz	0.1 eV	0.2 eV
1 MHz	0.08 eV	0.08 eV

Table 6.2 A.c. activation energies E_a as a function of frequency at two temperature ranges.

Fig 6.5. The results are also plotted in Fig. 6.6 showing the dependence of the capacitance on temperature at three different frequencies. At low temperatures (below 182 K) all the curves merge into a single one and start to separate at higher temperatures. The capacitance shows temperature independence at low temperature region, whereas at high temperatures the capacitance rises steeply with increasing temperature.

Figure 6.7 represents the variation of the loss tangent (tan δ) with frequency at various temperatures for the same PS sample. It is clearly shown that tan δ decreases with increasing frequency at the low frequency range and attains a minimum value (tan δ_{min}) then slowly increases with frequency at higher frequencies. The position of (tan δ_{min}) is found to be shifted to higher frequency as the temperature increases. For all the

studied frequency range tan δ was found to increase with increasing temperature as shown in Fig. 6.7.

The behaviour of the capacitance and loss tangent when the signal frequency and the sample temperature are varied can be interpreted by the model of Goswami and Goswami (1973) assuming that Al electrodes act as ohmic contacts for PS films (PS being an n-type material as was discussed in the previous chapter). According to this model, the PS device structure can be presented by the equivalent circuit shown in Fig. 6.1 (b). The measured capacitance C of the structure is given by equation (6.9). This equation predicts that the measured capacitance C decreases with increasing frequency and falls to a constant value C' for all the temperatures. According to this equation, for any given frequency the measured capacitance C increases with temperature due to the decrease in the value of interior resistance R with increasing temperature as predicted clearly in equation (6.7). All of these trends in behaviour are clearly demonstrated in Figs. 6.5 and 6.6. The loss tangent tends to behave exactly as was predicted by Gaswami and Gaswami model (Fig. 6.7) and is given by equation (6.10). Initially tan δ decreases with increasing frequency at lower frequencies as the term ω^{-1} is the dominating factor in equation (6.10). This decrease in tan δ is followed by a minimum loss tangent value at a frequency given by equation (6.11). The value of tan δ_{min} is found to be shifted towards higher frequencies with increasing temperature because of the decrease in the value of the interior resistance R. The values of ω_{min} at different temperatures are shown in Table (6.3).

Temperature (K)	152	182	212	232	262	292
$(\omega_{min}/2\pi)$	1 KHz	2 KHz	4 Khz	6 KHz	8 KHz	10 KHz

Table 6.3 The value of ω_{min} as a function of temperature.

A different equivalent circuit model has been proposed by Parkhutik et al (1996) for the electrical impedance of different PS samples. The proposed circuit consisting of two R-Q elements connected in series and both connected in parallel with a Q element (Q is a constant phase element). The values of the elements in the equivalent circuit are depend on the post treatment of PS layer and the volume of the sponge-like phase of PS.

6.3.3 Dielectric properties of porous silicon

The dielectric constants (ε′ and ε″) of PS films were calculated using equations (6.16) and (6.17) at different temperatures for the same sample as in Fig 6.2. The variation of ε′ and ε″ as a function of frequency at room temperature is shown in Fig. 6.8. It is clear from Fig. 6.8 that ε′ has a large frequency dispersion which can be describe as a Debye type dispersion and is given by [Hill et al 1969]

$$\frac{\varepsilon' - \varepsilon'_{\infty}}{\varepsilon'_{o} - \varepsilon'_{\infty}} = \frac{1}{1+(f / f_{o})^{2}} \tag{6.19}$$

where ε'_o and ε'_∞ are the low and high frequency dielectric constants (ε′), f is the measured frequency and f_o is the relaxation frequency which is the reciprocal of the relaxation time ($f_o = 1/\tau$). The values of ε'_o and ε'_∞ were estimated from the measured ε′

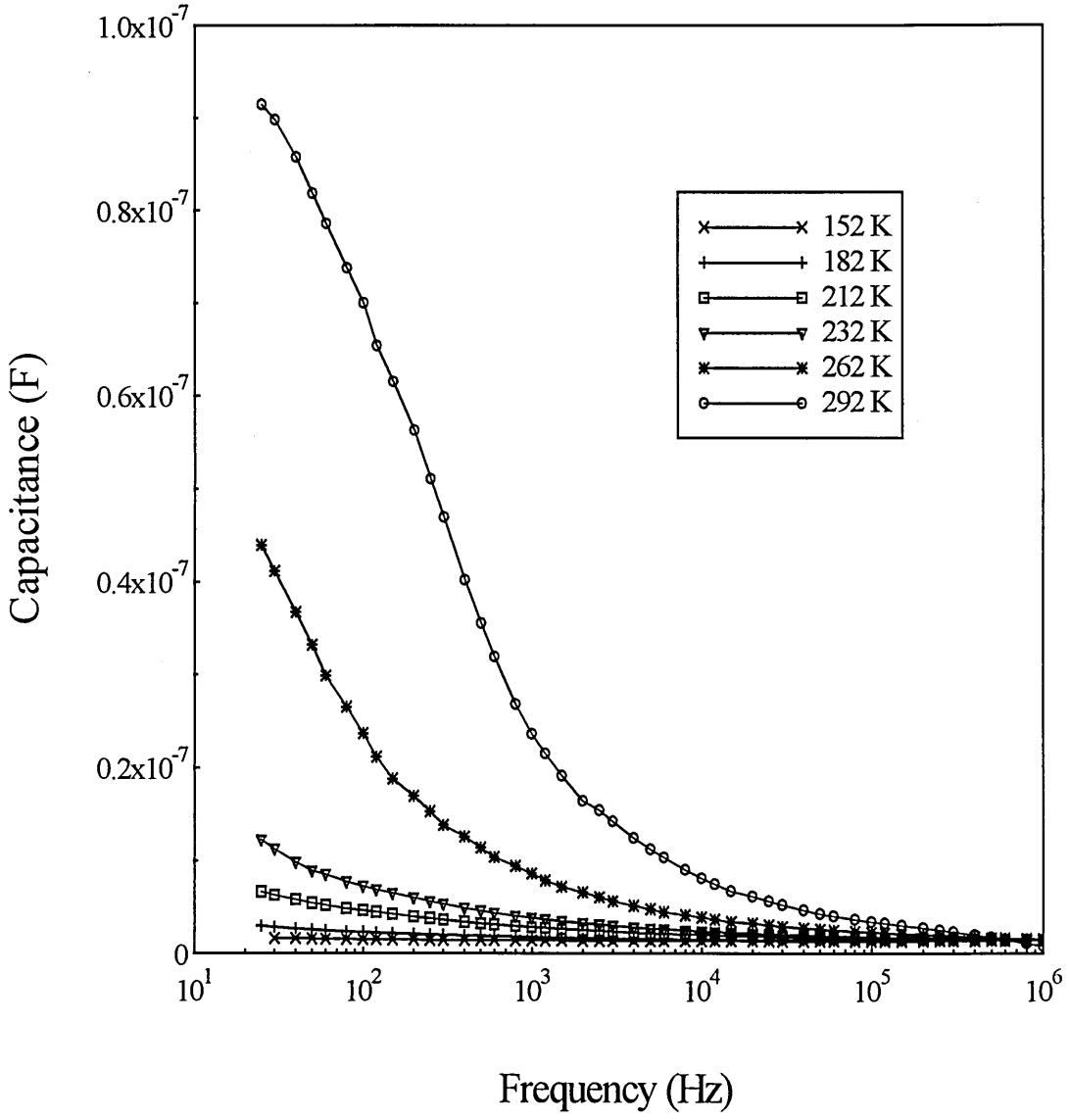


Figure 6.5 Dependence of capacitance on frequency at different temperatures for the same structure as in Fig 6.2.

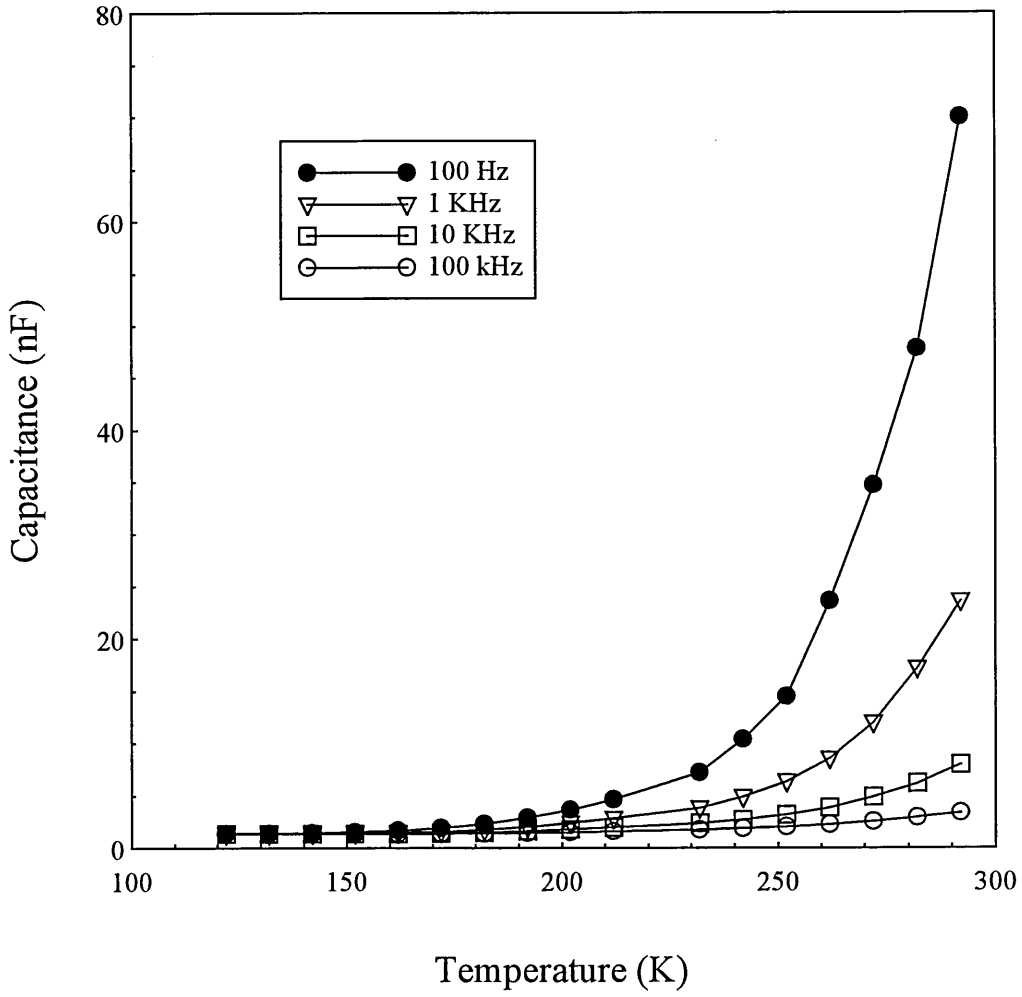


Figure 6.6 Temperature dependence of capacitance at three different frequencies for the same structure as in Fig. 6.2.

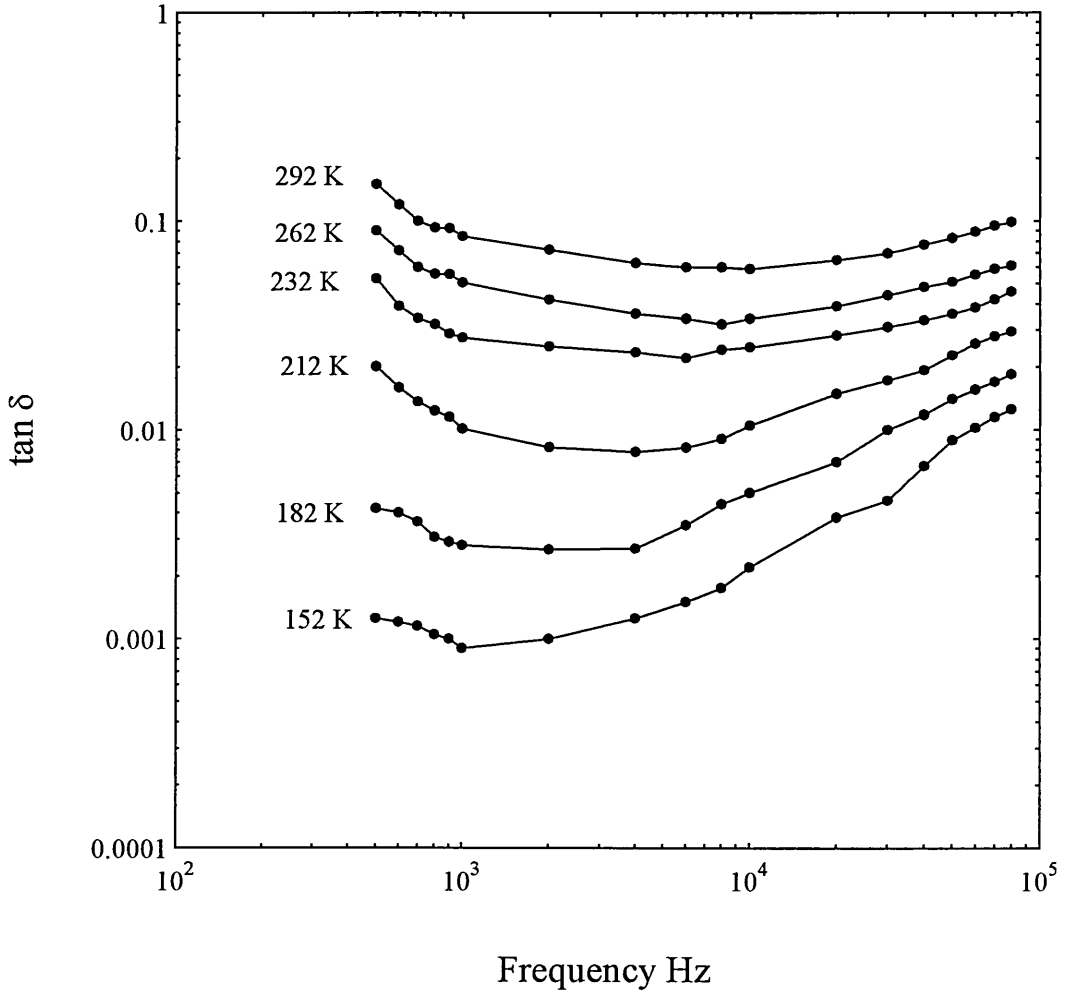


Figure 6.7 Dependence of the loss tangent (tan δ) on frequency at different temperatures for the same structure as in Fig 6.2.

as a function of frequency and substituted in equation (6.19) to give the value of ε' at the relaxation frequency ($f = f_o$). The effective relaxation time (τ) was found of about 3.3×10^{-4} sec at room temperature which is close to the value of 3.5×10^{-4} sec found by Parkhutik et al (1996) for as-formed PS Samples. Comparing the value of the dielectric constant of the silicon substrate (11.9) to the value of the low frequency dielectric constant of PS (40 for this sample) could clearly explain how the structure of the silicon has been changed from a semiconductor material to an insulator with high dielectric constant. Higher values of ε'_o have been reported for different PS samples prepared from both p-type and n-type silicon substrates [Parkhutik et al 1996]. Furthermore, these workers concluded that ε' and ε'' dependencies on frequency for the PS samples filled with ethyl alcohol are qualitatively similar to those of freshly made samples with ε'_o value of about 300.

This method of obtaining information about the relaxation mechanism could be open to some criticism, taking into account that the decrease of ε' at low frequencies could be an erroneous measurement leads to wrong values of ε'_o. It has been suggested by Gupta and Mansingh (1994) that in the absence of the ε'' peak, information about the relaxation mechanism can be obtained from the dielectric modulus representation. The real part and imaginary part of dielectric modulus can be derived from ε through

$$M = (\varepsilon)^{-1} = M' + M''$$
$$= \frac{\varepsilon'}{(\varepsilon')^2 + (\varepsilon'')^2} + j\frac{\varepsilon''}{(\varepsilon')^2 + (\varepsilon'')^2} \qquad (6.20)$$

where M' and M'' are the real and imaginary parts of the dielectric modulus respectively.

According to this model, a plot of M'' against frequency should give a peak at the relaxation frequency f_o [Gupta and Mansingh 1994]. The normalized plot of the imaginary part of the dielectric modulus (M''/M''_{max}) as a function of frequency at room temperature is shown in Fig. 6.9. It is clear that the relaxation frequency of PS is about 2700 Hz (at the peak of Fig. 6. 9) which give a value of 3.7×10^{-4} for the relaxation time. This value of relaxation time is in agreement with the value found earlier and indicating that the estimated value of ε'_o from Fig. 6.8 is practically applicable.

The real part of the dielectric constant (ε') as a function of frequency at different temperatures is shown in Fig. 6.10. At low temperatures, ε' is almost temperature independent having a weak frequency dispersion, whereas at higher temperatures it shows strong frequency dispersion and temperature dependence. It may be noted from Figs. 6.2 and 6.10 that the variation of ε' with frequency is small in the region where conductivity shows a linear frequency dependence indicating that there is some contribution from hoping conduction in the measured ε'.

Figure 6.11 illustrates the variation of ε' and ε'' as a function of temperature at four different frequencies. The dielectric constant is believed to increase with temperature in an exponential fashion of the type [Parkhutik et al 1996]

$$\varepsilon = A \exp(-\frac{E_a}{kT}) \tag{6.20}$$

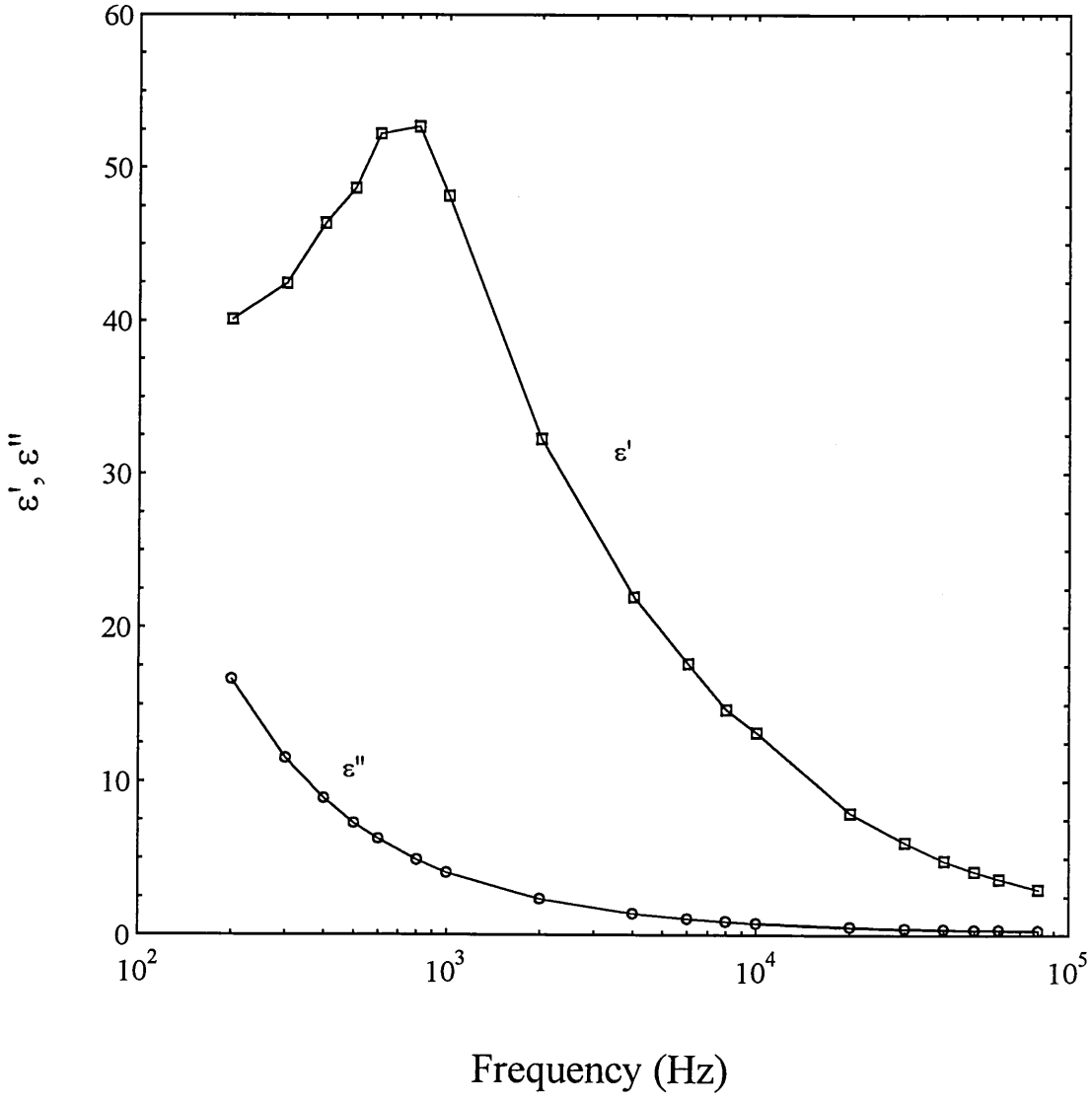


Figure 6.8 Frequency dependence of real and imaginary part of the dielectric constant for the same structure as in Fig. 6.2.

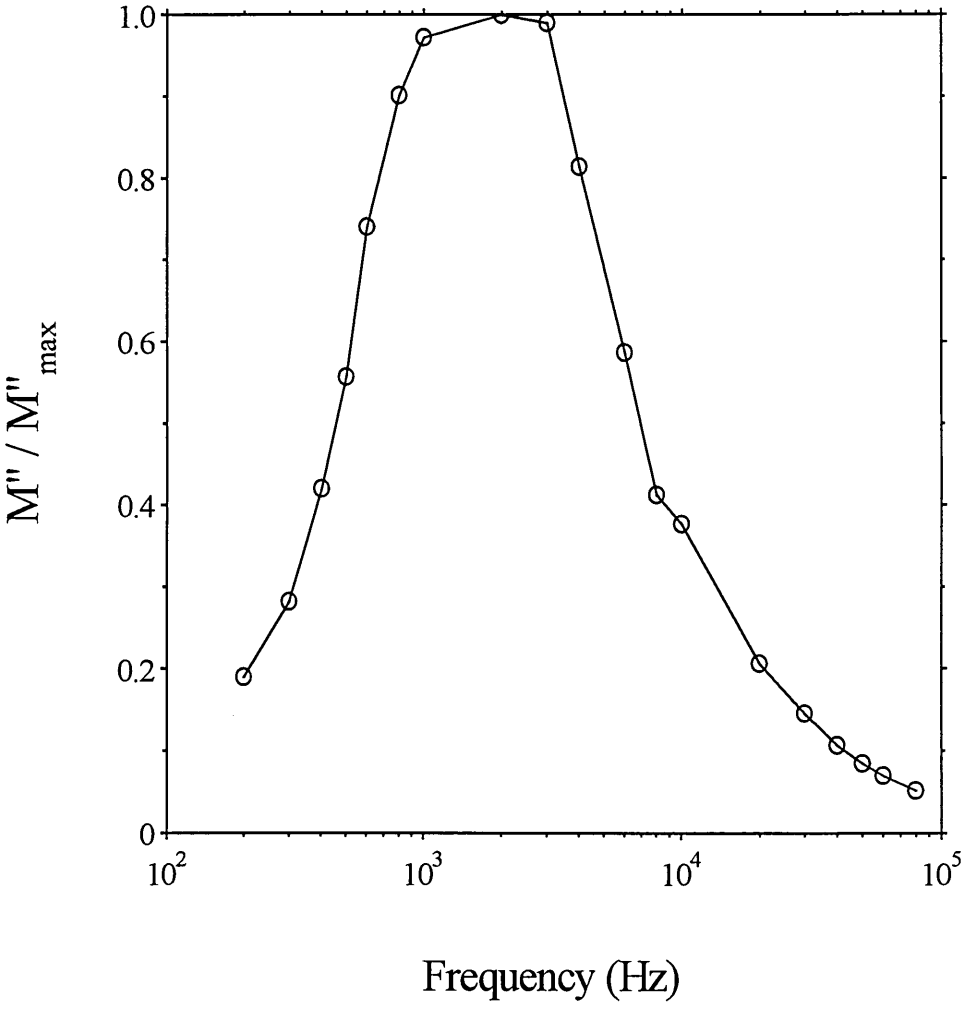


Figure 6.9 Normalized plot of M'' / M''max vs frequency at room temperature for the same PS sample as in Fig. 6.2.

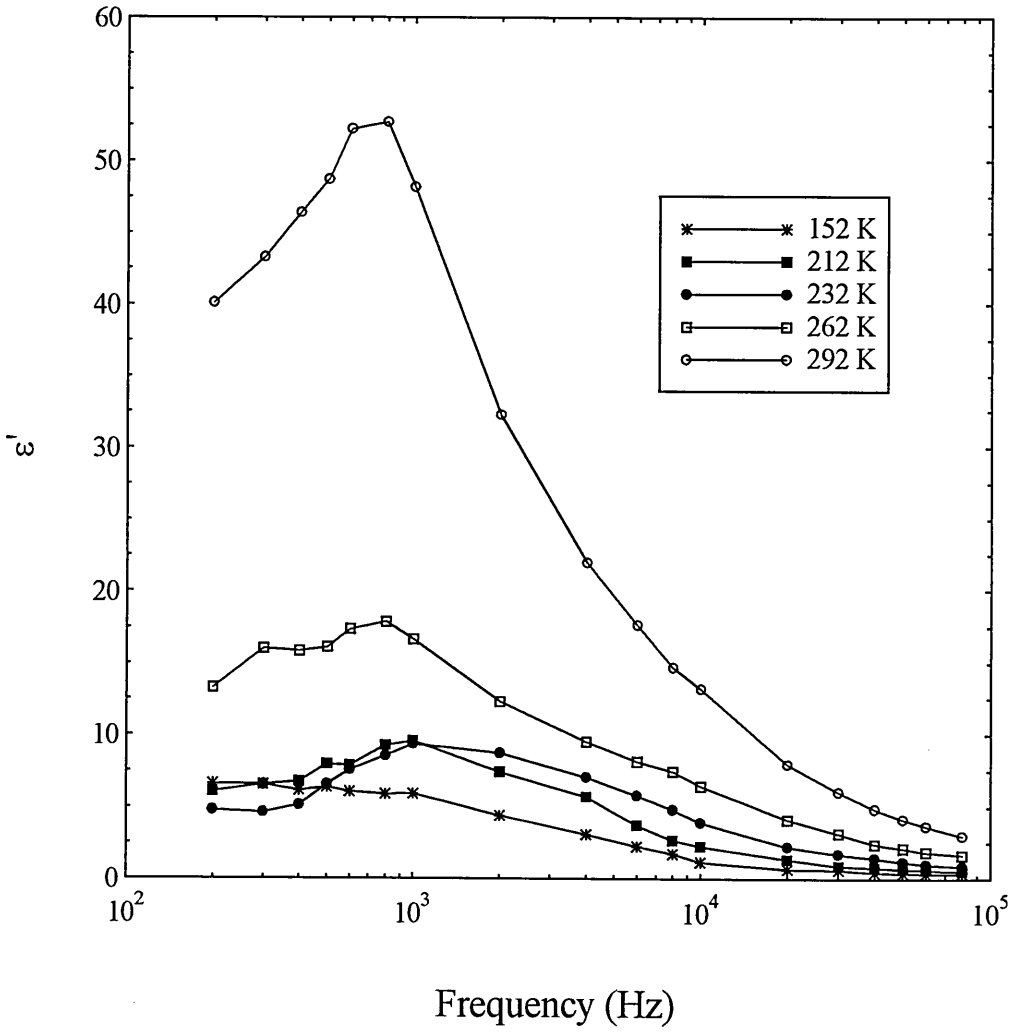
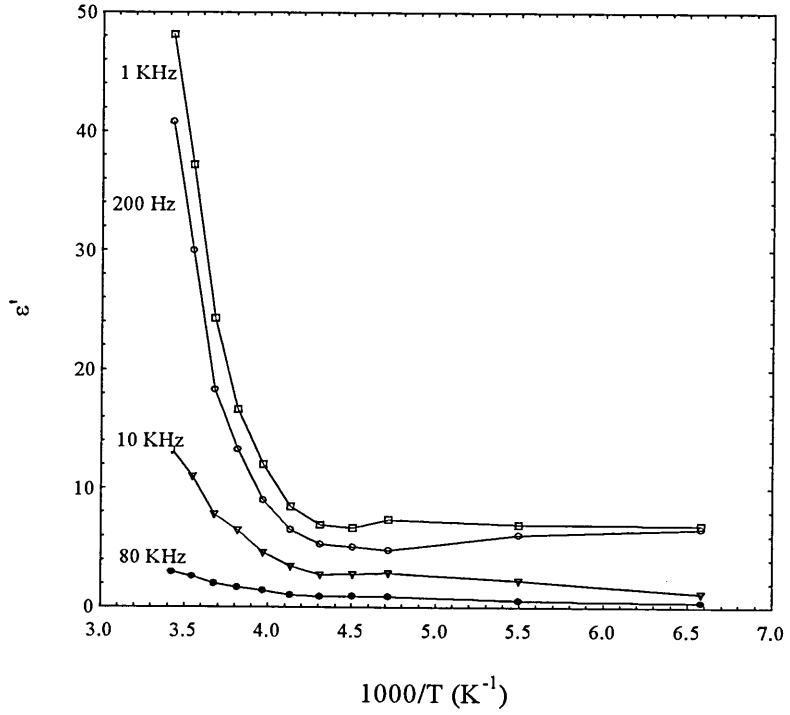
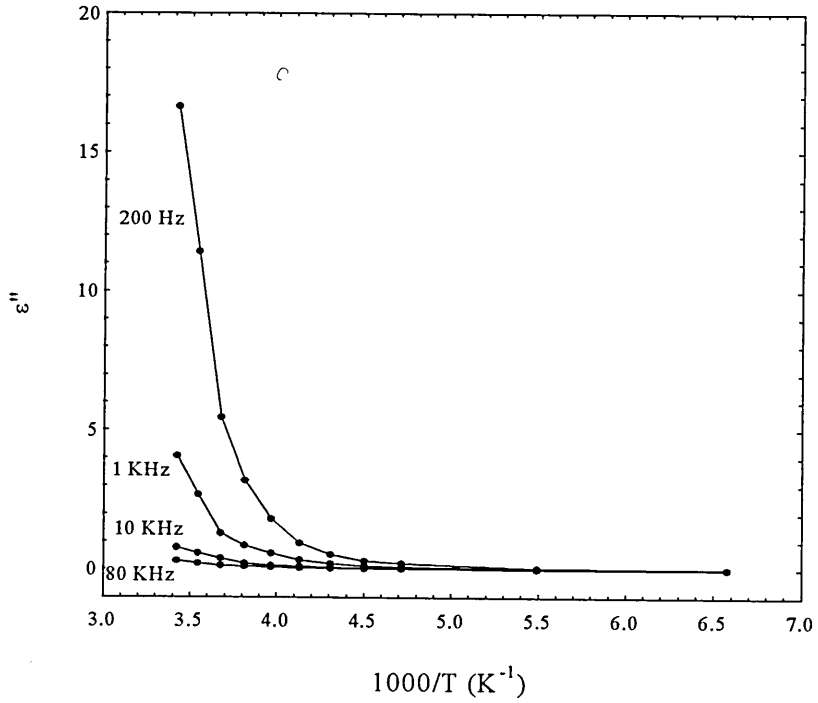


Figure 6.10 Frequency dependence of the real part of the dielectric constant at different temperatures for the same structure as in Fig. 6.2.



(a)



(b)

Figure 6.11 Temperature dependence of the real (a) and imaginary (b) parts of the dielectric constant of the same PS sample as in Fig. 6.2.

where ε is the dielectric constant (ε′ or ε″) and A is a constant representing the value of ε at high temperature. The ε′(T) curves show two parts: one corresponds to the low temperature region with activation energy of about 0.06 eV and another at higher temperatures with activation energy of about 0.22 eV at low frequencies and 0.15 eV at high frequencies. The ε″(T) curves represent the presence of electrical conductivity ,and the activation energies for this conductivity as calculated from the slop of ε″ vs $1/T$ dependencies at high temperatures is about 0.33 eV at low frequencies and 0.22 eV at higher frequencies. A lower activation energy of about 0.13 eV has been estimated for the low temperature region. These values of activation energies are similar to the values found using the σ($1/T$) curves as described in section 6.3.1.

It can be observed that the strong temperature dependence of ε′ starts at higher temperature for higher frequencies indicating that f_o increases with increasing temperature. It is also observed that at the high temperature region where there is a strong temperature dependence of ε′ at a given frequency is the same at which the total measured conductivity (σ_{tot}) approaches σ_{dc}. In other words, the σ_{dc} is the dominating conduction in this temperature region.

It is important to mention that all the a.c. electrical characteristics of PS were found to be reproducible for the PS samples produced under different fabrication conditions. The results were qualitatively similar for all PS samples but the value of the conductivity may be changing depending upon the fabrication conditions, especially the anodization time which controls the thickness of the PS layer and then the resistivity of the device.

CHAPTER SEVEN

PHOTOELECTRONIC PROPERTIES OF POROUS SILICON

7.1 Introduction

In this chapter the photoelectric properties of metal/Si/PS/metal structure have been studied to complete the electrical characterisation of porous silicon (PS). The photovoltaic measurements were carried out on different PS samples fabricated under different fabrication conditions. Measurements of the photoconduction in PS films over wide range of temperatures will be discussed throughout this chapter. The properties investigated include the photoconduction spectrum and dark and illuminated $I(V)$ characteristics of different PS samples at different temperature.

7.2 Theoretical background

Photocurrent is the emission of electrons from a material due to illumination with a monochromatic light with energy higher than the absorption band edge of the material [Wood 1994, Kasap 1997]. To investigate the photocurrent characteristics the current-voltage ($I(V)$) measurements in the dark and under illumination should be studied as the photocurrent is the different between the two.

$$I_{ph} = I_{ill} + I_d \tag{7.1}$$

where I_{ph} is the photocurrent, I_{ill} is the current under illumination and I_d is the dark current. A typical example of the I(V) characteristic of a pn junction under dark and

illumination conditions is shown in Fig. 7.1. The open circuit voltage (V_{oc}) is the voltage produced due to the light under very high resistive load (open circuit condition). The short circuit current (I_{sc}) is the current created by the light, with no applied voltage, for a very small resistive load (short circuit condition). V_m and I_m are the voltage and current at the maximum power point due to the light incidence [Hovel 1975, Milnes and Feucht1972]. The relationship between I_{sc} and V_{oc} can be expressed as:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_{sc}}{I} + 1\right) \tag{7.2}$$

where I is the pre-exponential factor, q is the electron charge, n is the ideality factor, k is Boltzman constant, and T is the temperature.

The photovoltaic devices, during illumination, can be presented by the equivalent circuit shown in Fig. 7.2. The presence of the diode is to represent the fact that the photocurrent is effective under reverse bias only. The shunt resistance (R_{sh}) and the series resistance (R_s) play a very important factor in the performance of the device as they control the values of V_{oc} and the I_{sc} [Hovel 1975, Chopra 1983). Ignoring the effect of the series and shunt resistances, the short circuit current for a photovoltaic device is predicted to increase linearly with increasing light intensity. This prediction therefore suggests a logarithmic dependence of Voc with the light intensity according to equation 7.2.

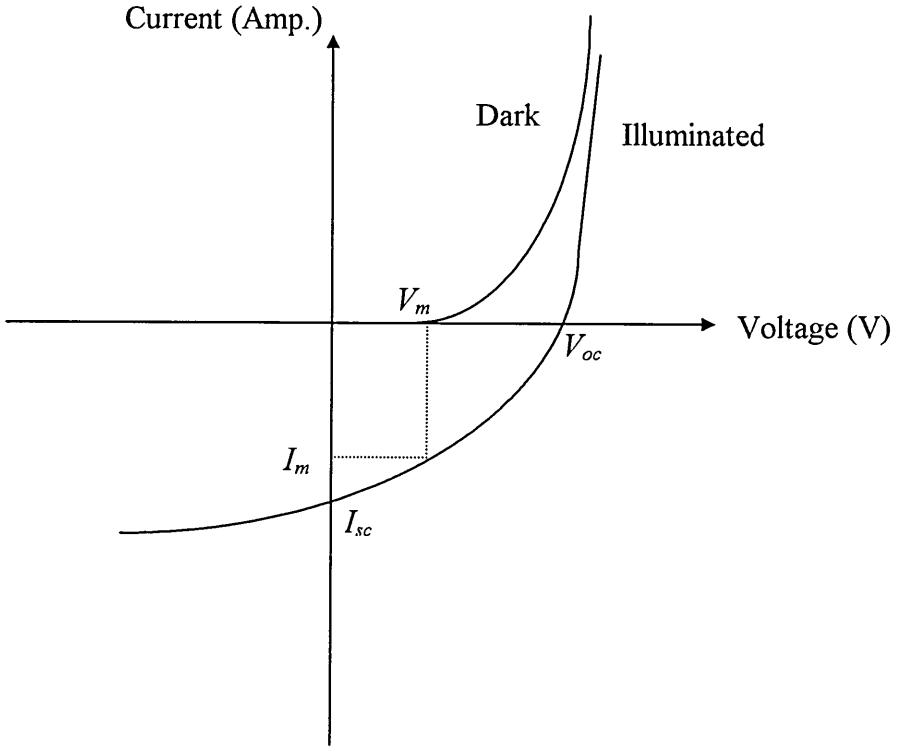


Figure 7.1 $I(V)$ characteristic of a typical pn junction under dark and illuminated conditions.

The conversion efficiency η of the device can be used to assess the device performance and is given by:

$$\eta = \frac{V_{oc} I_{sc}}{P_{in}} FF \tag{7.3}$$

where P_{in} is the input optical power incident on the material (in watts) and FF is the fill factor which is defined as the maximum fraction of the product of V_{oc} and I_{sc} available as output power and given by:

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \tag{7.4}$$

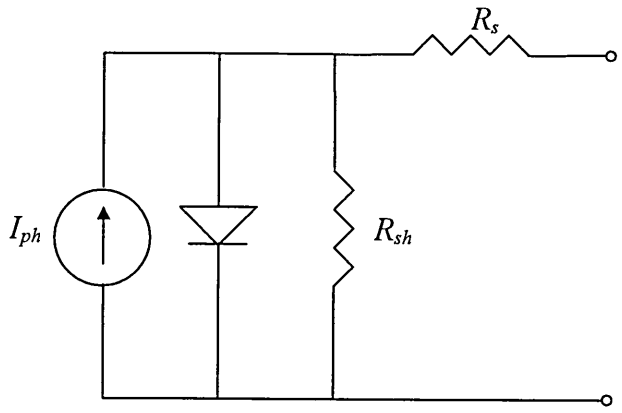


Figure 7.2 Equivalent circuit of a photovoltic structure.

The shunt resistance (R_{sh}) can be estimated from the reverse bias of the illuminated $I(V)$ where the current change linearly with the bias voltage. While the series resistance (R_s) may be determined from the slope of the illuminated $I(V)$ under high forward bias voltages ($V>V_{oc}$). In an ideal pn junction photovoltaic devices the values of R_S and R_{sh} are zero and ∞ respectively. In any pn junction (or hetrojunction) it is known that the increase in the R_s dose not affect the V_{oc} but it lowers the I_{sc} and consequently decreases the fill factor (FF) of the device. Similarly, R_{sh} dose not affect the I_{sc} but it affect the V_{oc} and then the FF.

For the PS samples the series resistance represents the contact resistance, and the silicon and PS resistances. Since the PS resistance is very high compared to the contact resistance and the silicon resistance, the thickness of the PS will have a

significant effect on the R_s value and then the value of the I_{sc}. The shunt resistance indicates of the presence of the leakage current and represents the connected undepleted crystalline silicon channels. These channels allow more alternative conduction paths through the structure in which carriers do not encounter the PS/Si junction (leakage current) [Palsule et al 1997]. With increasing formation time of the PS the probability of producing these connected channels from one electrode to another will decrease and the shunt resistance will increase accordingly. The thickness of the PS layers should have only small effect on the fill factor FF and the efficiency η of the device as the short circuit current will decrease and the open circuit voltage will increase with increasing the thickness of the layer.

7.3 Experimental results and discussions

7.3.1 Photoconduction spectra

The photoelectric properties of PS were evaluated for a number of samples of Au/PS/p-Si/Al structures. The PS layers were formed using different anodisation conditions. The results were similar for all samples formed under the same anodisation time (samples with the same thickness) regardless the other anodisation conditions. The samples under investigation were fabricated by the anodisation of p-type silicon substrate in a 1:1 solution of HF acid (49% in water) and ethanol at a current density of 25 mA/cm^2 in various anodisation time. From the SEM images, PS layers thicknesses were estimated to be between 5-20 μm. The thickness of the Au layer coated on top of the PS layers was about 50 nm. The active device area was about 0.3 cm^2.

The photoconduction spectra obtained under different positive bias voltages (PS at negative polarity and the silicon substrate at positive polarity) at room temperature shows an identical dependence at all voltages as shown in Fig. 7.3. No dependence on the applied bias was observed. For the negative bias (PS at positive polarity), the photocurrent spectra shows a shift in the peak wavelength toward lower energies with increasing bias voltage as shown in Fig. 7.4. In order to understand this spectral dependence, it is important to compare the absorption spectra of crystalline silicon and PS. The energy band gap of PS is estimated to be 1.7-1.8 eV [Balagurov et al 2000, Ciurea et al 1998, Martin-Palma et al 2000]. Koshida et al (1993), and Palsule et al (1997) found that the absorption length of PS is at its peak at 1.7-1.8 eV and the absorption coefficient of crystalline silicon is at least one order of magnitude larger than PS. Thus, for all the devices investigated in this study, the PS film is transparent to light below this energy (light with wavelength higher than 700 nm). Since the peak of the photocurrent spectra is in this energy range, it is clear that the most of the absorption takes place in the crystalline silicon part of the device. Hence, the sharp cut-off at 1000 nm wavelength (as shown in Fig. 7.3) corresponds to the room temperature bandgap of the silicon substrate. For photon energies above 1.7-1.8 eV (less than 700 nm wavelengths) the absorption in PS becomes more significant depending on the thickness of the PS layer, as shown in Fig. 7.5. In all PS samples, the photocurrent spectra peak is in the range of 700-800 nm at low applied voltage. The reason behind this shape of the photocurrent spectrum at low wavelengths is that even though most of the electron hole pairs are generated in PS the carriers cannot reach the built in electric field and then cannot diffuse towards the respective collecting electrode [Dafinei and Dafinei 1999, Ozaki et al 1994, Palsule et al 1997, Tsuo et al 1993, Wang et al 1997].

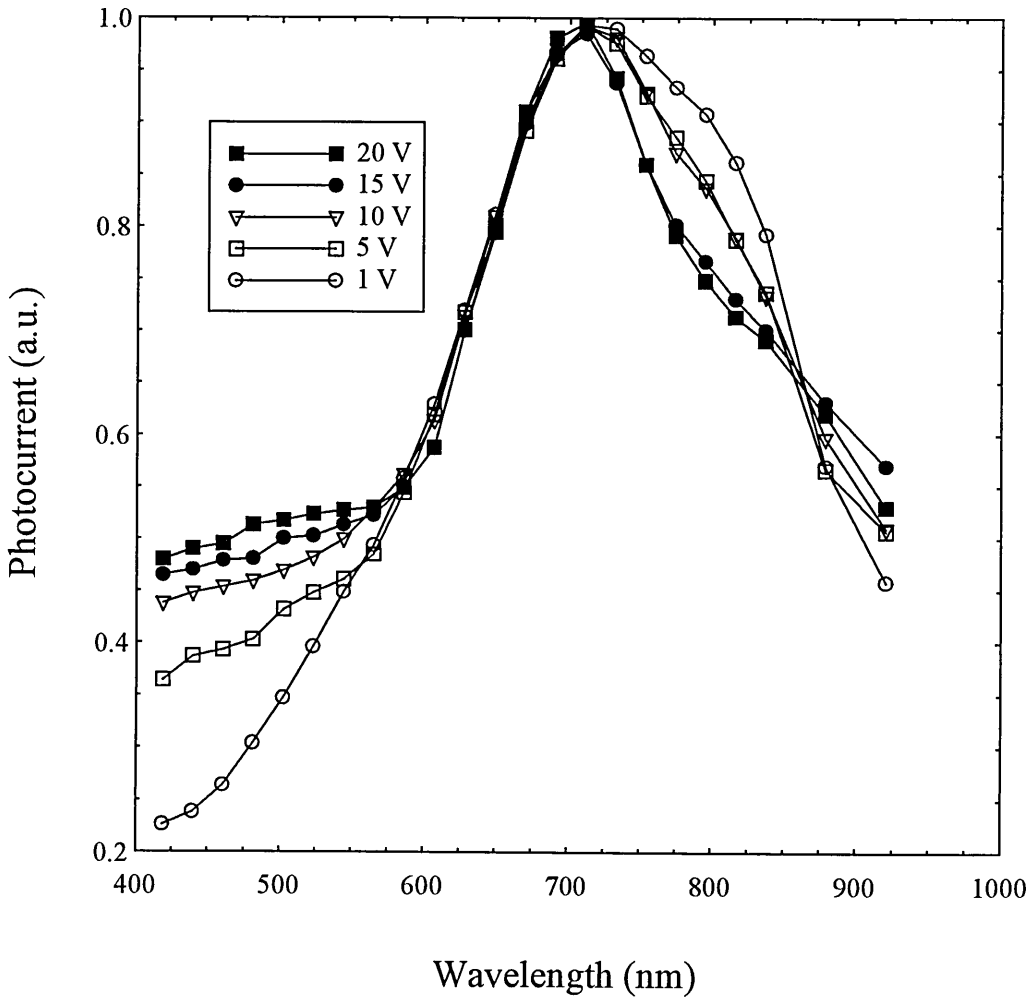


Figure 7.3 Photocurrent spectral response of Au/PS/p-Si/Al structure at room temperature as a function of the positive bias voltage.

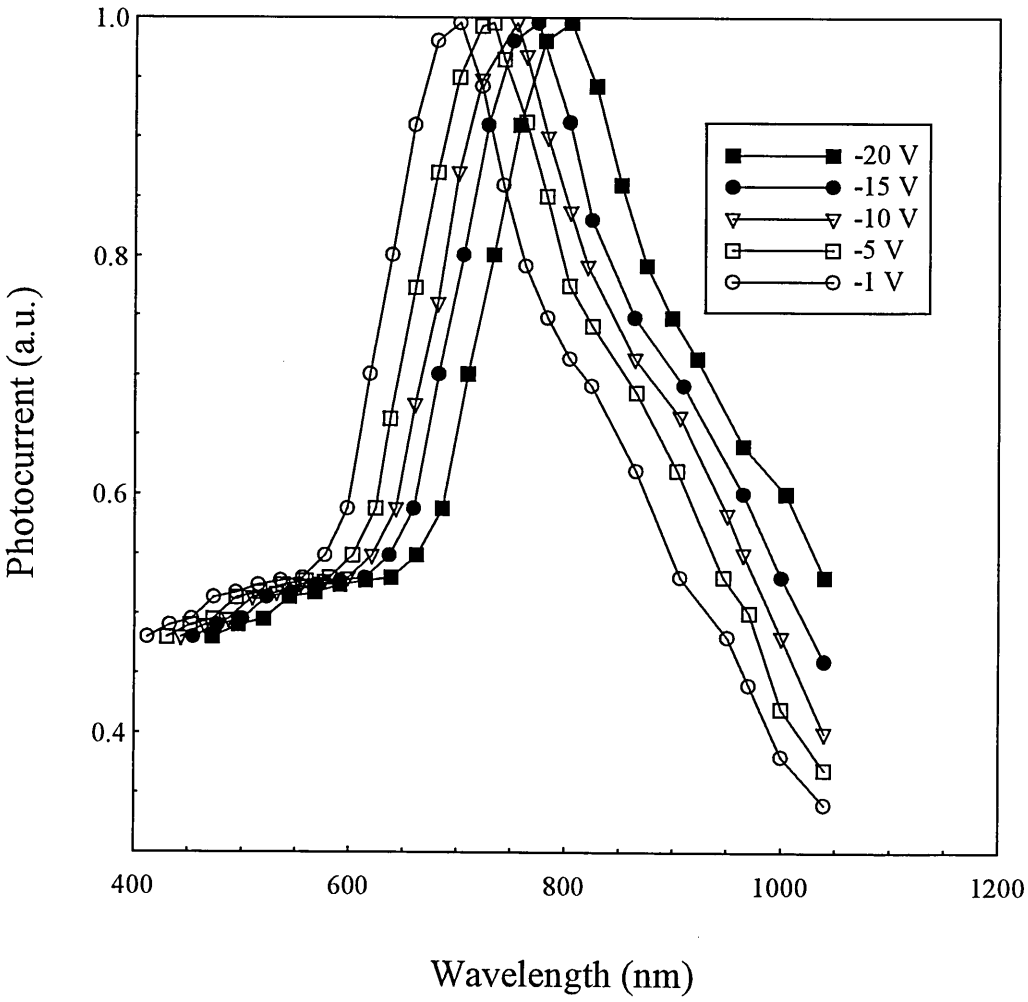


Figure 7.4 Photocurrent spectral response of Au/PS/p-Si/Al structure at room temperature as a function of the negative bias voltage.

Moreover, due to the absorption in PS, light reaching the crystalline silicon at these energies will be considerably attenuated and hence, the density of photogenerated electron hole pairs will be low resulting in drop off at these energies. Heben and Tsuo (1993) observed a peak at 2.5 eV (500 nm wavelength) with a bending shoulder at 1.7 eV. The bending shoulder attributed to the excitation of the silicon substrate by wavelengths that are transmitted through the PS layer, while the higher energy photocurrent was referred to the excitation of the carriers generated within the PS layer. Similar results were reported by Ozaki et al (1994) where the peak of the photoconduction spectra was observed to be applied voltage dependent, and at low voltages the peak was at 500 nm.

The photoconduction spectra as a function of the applied voltage, Figs. 7.3 and 7.4, can be explained by the existence of the hetrojunction between the PS and the silicon substrate, as shown in the band diagram of the device in Fig. 5.13, chapter 5. When a bias voltage applied to the device, most of the potential drop is produced across the PS layer. For the positive bias voltages, Fig. 7.3, the photoelectrons generated in the silicon region will move to the interior of silicon substrate and cannot contribute to the photoconduction current. Under this situation, the intrinsic property of PS appears in the spectral response, and the concentrations of photoelectrons do not depend on the applied voltage. In the case of negative bias applied to the device, Fig. 7.4, the photoexited electrons generated in the silicon substrate move toward the PS layer and have a chance of contribution to the photoconduction effect. As the bias voltage increases, this additional component becomes predominant over the original photoconduction in the PS layer, and as a result the overall spectral response shows a shift toward higher wavelength.

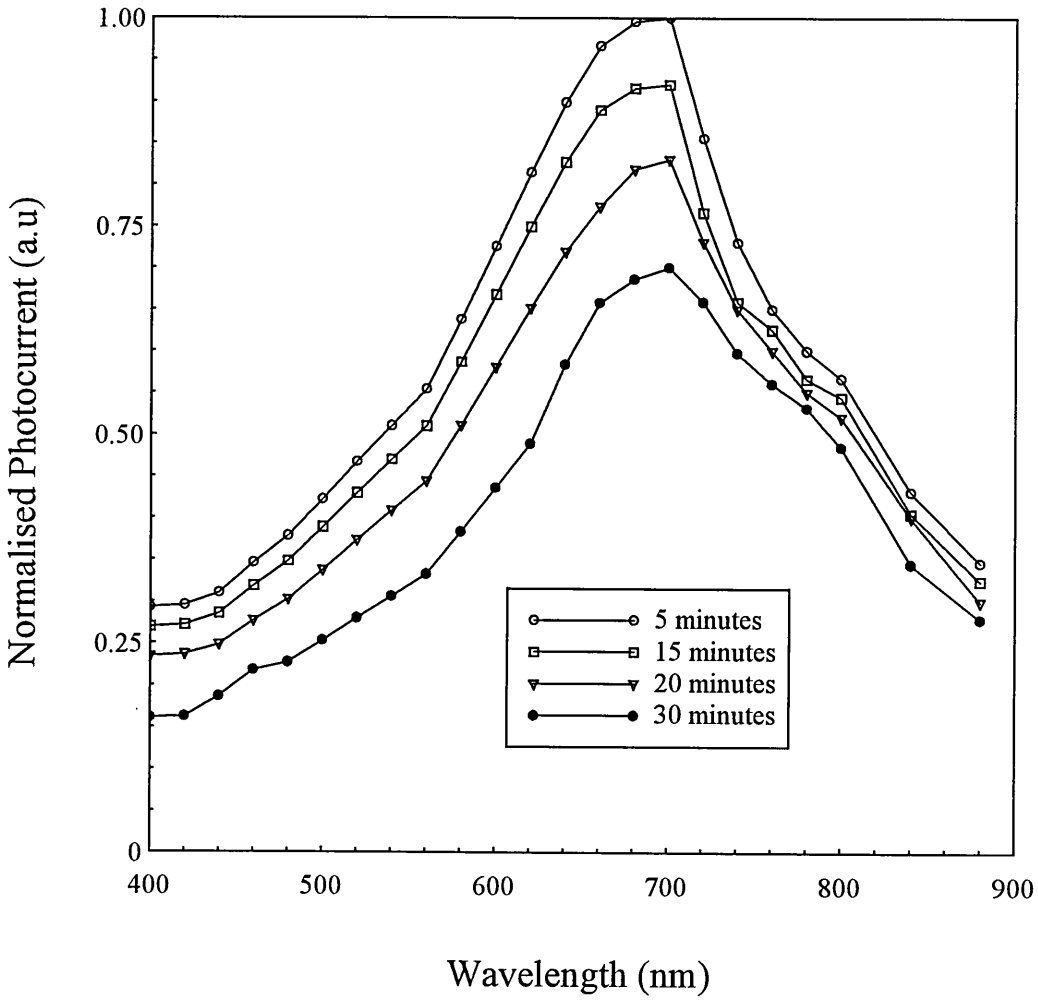


Figure 7.5 Room temperature phtocurrent spectral response of Au/PS/p-Si/Al structure as a function of PS anodisation times (PS thicknesses) at 1 V bias voltage.

The behaviour of the photocurrent spectra with the increase in the thickness of the PS layer can be explained in term of the changing in the series resistance R_s of the device, Fig. 7.5. In the structure of PS devices the current flow perpendicular to the PS film, and the series resistance will be proportional to the PS thickness. Since the PS resistivity is very high, changes in the thickness will make a significant change in the short circuit current. As the thickness of the PS layer is increased, the series resistance will increase resulting in a decrease in the short circuit current. Further more, the increase in the PS thickness leads to an increase the shunt resistance R_{sh} which results in an improvement in the open circuit voltage. These results are supported by the results of the d.c. measurements presented in chapter 5 as the increase in the anodisation time will result in a more complete depletion of holes in the region and higher bandgap. The increase in the bandgap of PS leads to higher barrier height for electrons going from silicon to PS, and hence decreasing the short circuit current.

7.3.2 Photocurrent-voltage characteristics of PS

A typical $I(V)$ characteristics of Au/PS/p-Si/Al devices at room temperature in the dark and under illumination are plotted in Fig. 7.6. The anodisation time for the PS layer used in this measurement was 5 minutes and the corresponding layer thickness was estimated to be 5 μm. The device exhibits a well rectified $I(V)$ curve in the dark as it was explained in chapter 5. Under illumination, negative photocurrents arise with applying positive voltages giving a short circuit current I_{sc} of 0.5 μAmp and open circuit voltage V_{oc} of 170 mV. The conversion efficiency η obtained for this device was 0.05 % and the corresponding FF was 0.27. Similar results were found for PS samples fabricated in the same fabrication conditions and stored for more than two months under laboratory conditions. The small value of I_{sc} and V_{oc} lead to very low η. For all

the PS samples the I_{sc} and V_{oc} values increase with the illumination intensity. Values of (0.3-1.4 μAmp) and (150-350 mV) where reported for I_{sc} and V_{oc} by other researchers [Dimova-malinovska et al 1997, Lee et al 1999].

The photovoltaic responses of the Au/PS/p-Si/Al structure were found very dependent on the thickness of the PS layer and on the anodisation time. In Fig. 7.7., $I(V)$ characteristics of PS structure were compared for PS layers at different thicknesses. It could be noticed that the increase in the PS layer thickness leads to a proportional decrease in the value of I_{sc}, while the value of V_{oc} increases uniformly. Hence, the change in the PS layer thickness has a very small effect on the fill factor FF as expected in equation 7.4. The photovoltaic parameters for the devices in Fig. 7.7 are summarised in table 7.1. These results are in full agreement with the photocurrent spectrum of the PS structure at different thickness shown in Fig. 7.5. The change in I_{sc} and V_{oc} with the PS layer thickness could be related to the variation in R_s and R_{sh} with the layer thickness. As the thickness of the PS layer increased, R_s would increase resulting in a decrease in I_{sc}. At the same time, an increase in R_{sh} due to an increase in the PS layer thickness would result in an increase in V_{oc}. Because of the decrease in I_{sc} and the increase in the V_{oc}, there were no significant changes in the value of FF or η. The Highest overall conversion efficiency η for a PS structure at room temperature was 0.055% for a PS layer with 20 μm thickness (30 minutes anodisation time). These results are similar to the data reported by Menna et al (1995), Palsule et al (1997), and Ribes et al (1996).

From the $I(V)$ plots under illumination, the value of the series resistance R_s for the PS devices in Fig. 7.7 were estimated from the slope of the plots in the forward bias at high voltages. From the reverse bias of the $I(V)$ characteristics, the shunt resistance

R_{sh} were calculated from the high negative bias voltages. In all devices, a high value of R_s was observed, and this is believed to be due to the high resistance of PS layer as was clarified in chapter 5 [Ray et al 1998]. The high value of R_s undermined the performance of the device by reducing both I_{sc} and FF. The value of the series resistance measured under illumination is slightly less than the value of those measured in the dark. This is could be a consequence of the photoconductive effects of the PS layer.

The effect of the anodisation time on the values of both R_s and R_{sh} can be clearly noticed in table 7.1. The increase of R_s with increasing PS anodisation time is responsible for decreasing I_{sc} as expected. However, the value of R_{sh} increased with the anodisation time and that will improve the value of V_{oc} keeping the value of FF unaffected. These results are expected as the photocurrent spectrum at different thicknesses of PS layers, Fig. 7.5, shown a reduction of the value of the photocurrent with increasing anodisation time. Such behaviour is expected in heterojunction cells as the increase in the anodisation time will expand the bandgap of the PS layer and increase the barrier height for the electrons moving from the silicon substrate to the PS.

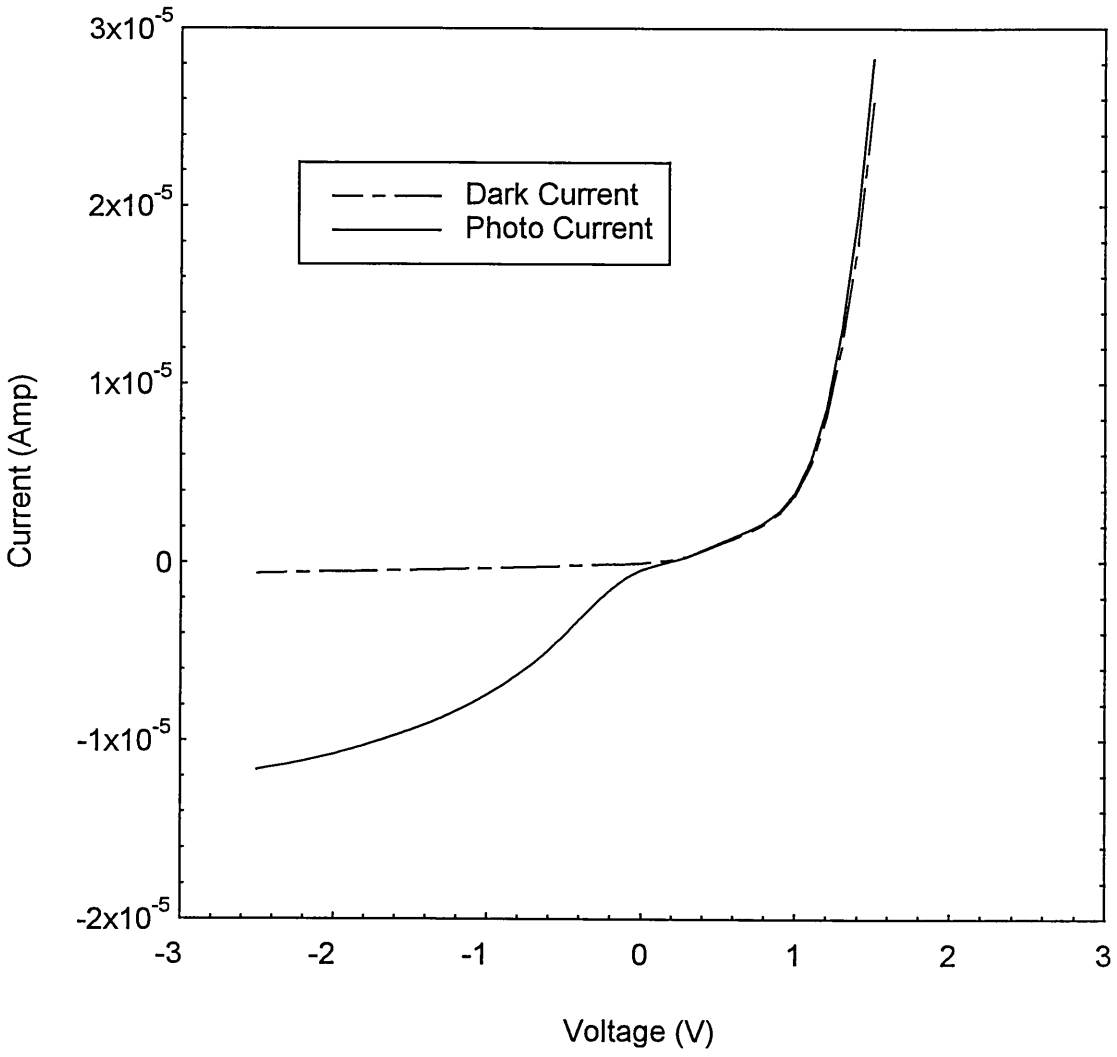


Figure 7.6 $I(V)$ characteristics in the dark and under illumination of Au/PS/p-Si/Al structure at room temperature.

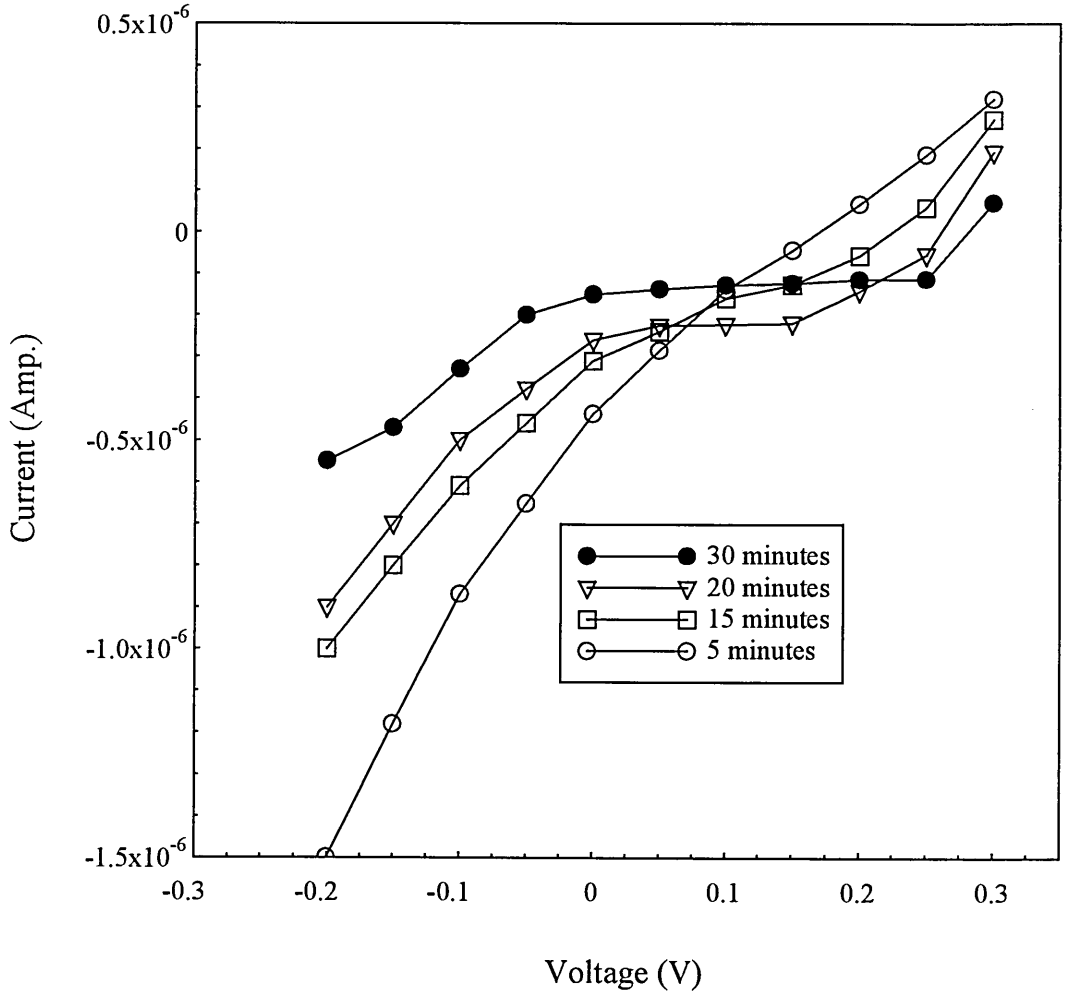


Figure 7.7 *I*(*V*) characteristics under illumination of Au/PS/p-Si/Al structure at room temperature as a function of PS anodisation time.

Anodisation Time (minutes)	I_{sc} (μAmp.)	V_{oc} (mV)	FF	R_s (KΩ)	R_{sh} (MΩ)
5	0.5	170	0.27	0.35	1.5
15	0.33	224	0.26	0.42	1.78
20	0.25	262	0.265	0.485	2
30	0.15	280	0.28	0.55	2.3

Table 7.1 The photovoltaic parameters of the Au/PS/p-Si/Al structures used in Fig. 7.5.

For a more detailed study of the transport mechanisms in the PS structures the temperature dependence of the dark and illuminated current in the range 152-192 K were measured. The photovoltaic parameters for the PS sample used in Fig. 7.6 are summarised in Table 7.2. Both I_{sc} and V_{oc} clearly increase with temperature and almost saturate at higher temperatures. The temperature dependent measurements of dark current in PS shows two different activation energies. As shown in Fig. 5.9, chapter 5, 0.7 eV and 0.22 eV were estimated for high and low temperature regions, respectively. The I_{sc} of the device under this investigation shows activated behaviour at low temperatures and saturates at higher temperatures. This suggests that I_{sc} seems not to be restricted by the conductivity of the PS structure.

Figure 7.8 shows the temperature dependence of the photocurrent as a function of negative bias voltages. The electrical conduction mode at higher temperatures is a thermal activation type and the estimated activation energy is about 0.74 eV. This is very close to the value of the activation energy measured under dark conditions. At low temperatures below about 200 K, the photocurrent tend to show a slight temperature dependence and the activation energy is estimated to be 0.38 eV and 0.47 eV at high

and low bias voltages, respectively. It shall be noticed that the activation energy under illumination is slightly higher than the value measured in the dark in this region of temperatures. This is could be due to the effect of the photoexcited electrons in the silicon substrate. Both under dark and illumination conditions the transition temperature of 200 K corresponds to the critical point at the change in the carrier transport mechanism from the thermal activation mode to the more likely recombination one.

Temperature (K)	I_{sc} (nAmp)	V_{oc} (mV)	FF
292	500	170	0.27
272	494	170	0.265
252	490	167	0.255
222	416	160	0.22
202	389	150	0.21
182	370	127	0.2
162	330	108	0.18
152	243	99	0.173

Table 7.2 The photovoltaic parameters of the Au/PS/p-Si/Al structure used in Fig. 7.3.

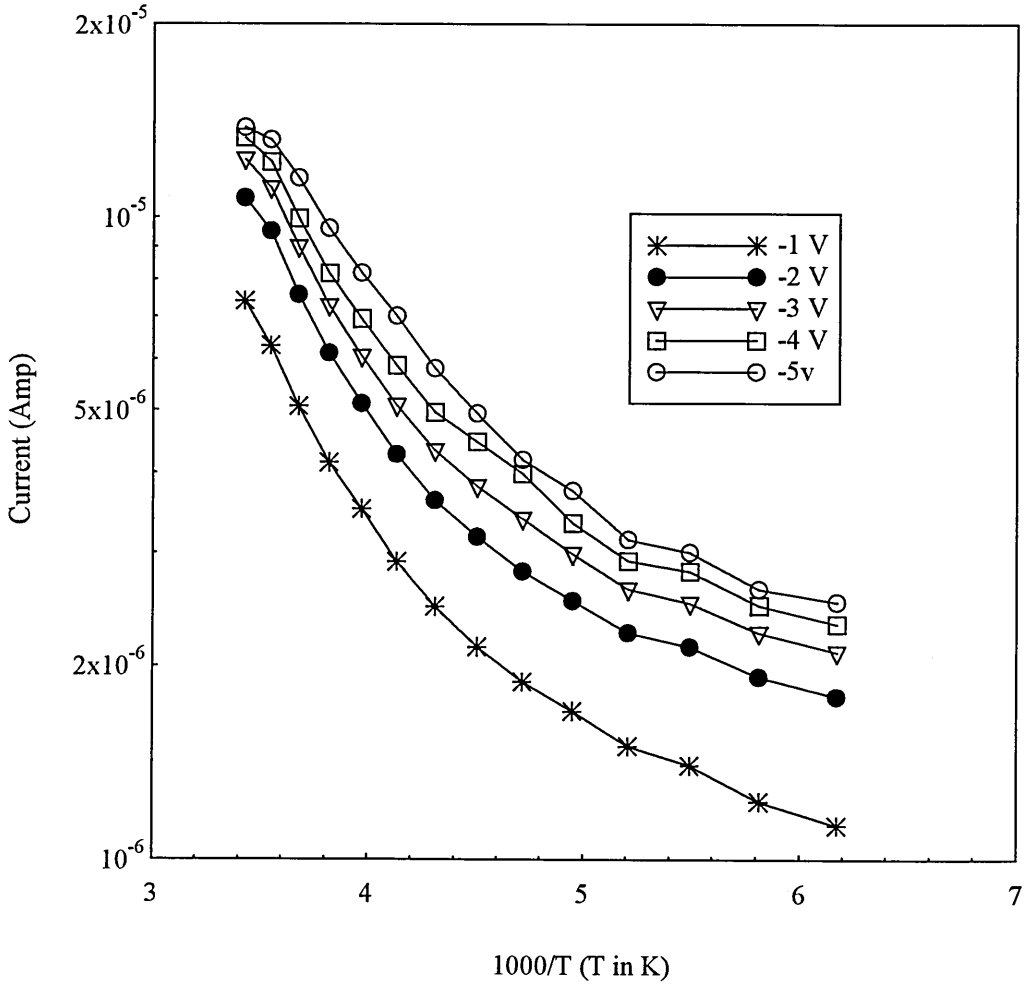


Figure 7.8 Temperature dependence of the photocurrent for a PS layer at different negative bias voltages.

CHAPTER EIGHT

CONCLUSIONS AND FURTHER WORK

8.1 Fabrication characteristics of porous silicon

Different PS layers have been fabricated to study their structural, electrical, and photoelectrical properties. A PTFE electrochemical cell was designed to process silicon samples up to 2 inch diameter. Different theories have been explained for the formation mechanisms of PS in terms of the depletion of hole carriers. The effect of doping level on the number of pores and the pore size was also illustrated. Models to define the chemical dissolution of silicon during the formation of PS have been detailed in this study.

Scanning electron microscopy (SEM) of PS samples with different fabrication conditions have been examined. SEM micrographic images show that high resistivity silicon substrates produced a PS layer with large pore size. On the other hand, PS samples fabricated from heavily doped substrates showed high porosity and smaller pore size. The porosity and the thickness of the PS layers were estimated from the SEM studies of the cross section of the layers.

8.2 Electrical measurements and conduction properties

Current-voltage characteristics of sandwich structures of PS films utilising different metal electrodes in different combinations have been measured in the temperature range between 152 and 300 K. PS layers were prepared from p-type silicon

substrates having different resistivities in the range between 8 and 350 Ωcm. Measurements were also performed on PS films fabricated under different conditions using various anodisation conditions, HF acid concentrations, and anodisation time. The results show a rectifying current-voltage, $I(V)$, behaviour for all PS structures regardless of the metal electrode combination used. The fabrication conditions showed a little effect on the resistivity of the structures as they control the porosity and the PS layer thickness. These results indicate that the interface between the metal electrode and PS layer may not be responsible for the rectification behaviour. The observed rectification current, however, found to be caused by the barrier between p-Si and PS layer.

Based on the work described in this thesis, it was found that PS films fabricated from p-type silicon substrates behave like n-type silicon due to the depletion of their majority carriers (holes). Moreover, the photoelectrical properties of PS structures showed a clear widening in PS band gap compare to the band gap of the silicon substrate. Therefore, a heterojunction between the PS layer and p-Si was found responsible for the current transport in metal/PS/p-Si/metal structures. A band model was proposed to describe the conduction in Al/PS/p-Si/Al devices. From the structure, it was found that electrons are the charge carriers responsible for the current through the structure.

Using measurements of current as a function of temperature, values of ideality factor (n), saturation current (I_s), activation energy (E_a) and the barrier height (Φ_b) were derived for metal/PS/p-Si/Al structures. The ideality factor was found to decrease linearly with increasing temperature from 1.13 at 150 K to 1.01 at 290 K. These values of ideality factors are interpreted as evidence that the PS/p-Si junction characteristics

are controlled by carrier diffusion in the PS. The low value of ideality factor is consistent with the diffusion model of charge carriers in an ideal p-n junction.

The barrier height of metal/PS/p-Si/Al structures was found to be temperature dependent. A value of 0.7 eV was found for the barrier height at room temperature. Variation of $\ln(I_s/T^2)$ with inverse temperature indicated two different values of activation energy corresponding to two dominant conduction processes. Recombination conduction process are believed to be dominant at low temperature as the activation energy did not exceed 0.22 eV. At high temperatures, a value of 0.7 eV for activation energy indicates that thermionic emission diffusion process is responsible for the current transport in the PS structure.

The universal power law (ω^S) dependence of conductivity on frequency has been exhibited by PS films sandwiched between two metal electrodes. The a.c. conductivity was found to follow this law with index s approaching unity at low temperatures and high frequency regions. This indicate a dominant hopping conduction process at low temperatures and high frequencies. Conversely, at higher temperatures and low frequencies the diffusion transport through the PS layer is found to be the dominant transport mechanism as the value of s did not exceed 0.2. Measurements of a.c. conductivity as a function of inverse temperature show very low activation energies at low temperatures and high frequencies. At higher frequencies (1 MHz) the a.c. conductivity becomes almost temperature independent and the activation energy did not exceed 0.08 eV. At higher temperatures and lower frequencies the conductivity appears to have activated behavior. Values of 0.35 eV and 0.2 eV were calculated for activation energies at low and high frequencies, respectively, at room temperature.

It was found that the dependence and loss tangent data were consistent with the model of Goswami and Goswami (1973). The value of the capacitance found to increase with increasing temperature and decrease with increasing frequency. However, the value of loss tangent found to increase with increasing temperature and decrease with increasing frequency at the low frequency range until reaching a minimum value where the value starts to increase slowly with increasing frequency.

The dielectric properties of PS have also been studied in the present work. The real and imaginary parts of the dielectric constant of PS were found to decrease with increasing frequency. A relaxation time of 3.3×10^{-4} Sec was estimated for different PS samples at room temperature. High values of dielectric constant at low frequencies were observed and indicated that PS has insulation properties much higher than the silicon substrate.

The photoconduction spectra of Au/PS/p-Si/Al structures were also investigated as a function of applied voltage and PS layer thicknesses. The spectra shows a red shift at increased negative bias voltage. For the positive bias, the peak wavelength was independent of the applied voltage. In general, the peak wavelength was observed at about 700-800 nm. This behaviour was ascribed to the existence of the heterojunction between the p-Si and the PS layer. The photoconduction spectra of PS also shows that PS behaves as a wide band semiconductor sensitive to the visible light. The measurements of photocurrent as a function of PS layer thickness shows a clear decrease of photocurrent with increasing layer thickness. These results were explained in terms of a changing of the device series resistance with varying PS layer thickness. This is supported by the fact that PS band gap increases with increasing PS layer thickness and, hence, increases the barrier height between p-Si and PS.

Current-voltage characteristics of Au/PS/p-Si/Al structures under illumination have shown an increase of the open circuit voltage with increasing PS layer thickness. In contrast, the short circuit current was found to decrease with increasing PS layer thickness. Values of 170 mV and 0.5 μAmp. were estimated for open circuit voltage and short circuit current, respectively, for 5 μm thick PS layer.

8.3 Suggestions for further work

In the present investigation, the electrical properties of PS films were studied on metal/PS/p-Si/Al structures. However, self-supported PS layers characteristics would add valuable information on the conduction properties of PS.

As PS represents a potential candidate for applications in gas sensing technology, the effect of exposure to various toxic gases and vapours on the conductivity, activation energy, and the capacitive properties should be studied. Similarly PS fabrication conditions should be investigated in order to optimise the film sensitivity for specific gas or vapour. The temperature range covered in the present work was suitable to observe conduction mechanisms in different PS structures. Sensor materials, however, must be thermodynamically stable at high temperatures. Therefore, it is suggested that electrical measurements should be performed for temperatures up to at least 750 K.

REFERENCES

(A)

Amato G., Di Francia G., Menna P., and Ninno D., Europhys. Lett., 25, (1994) 471.

Amisola G. B., Behrensmeier R., Galligan J. M., Otter A. F., Namavar F., and Kalkoran N. M., App. Phys. Lett., 61, (1992) 2595.

Anderson R. C., Muller R. S., and Tobias C. W., Sens. Actuator A, 23, (1990) 835.

Angelucci R., Poggi A., Dori L., Cardinali G. C., Parisini A., Pizzochero G., Trifiro F., Cavani F., Critelli C., and Boarino L., Thin Solid Film, 297, (1997) 43.

Araki M., Koyama H., and Koshida N., Appl. Phys. Lett., 69 (20), (1996) 2956.

Arita Y., and Kuranari K., Jap. J. Appl. Phys., 36, (1997) 1035.

Astrove E. V., Belov S. V., Lebedev A. A., Remenjuk A. D., and Rud V., Thin Solid Films, 255, (1995) 196.

Averkiev N. S., Kapitonova L. M., Lebedev A. A., Remenyuk A. D., Smirnova N. N., and Shik A. Ya., semiconductors, 30, (1996) 1135.

(B)

Badoz, P., Bensahel, D., Bomchil, G., Ferrieu, F., Halimaoui, A., Perret, P., Regolini, J., Sagnes, I., and Vincent, G., Mat. Res. Soc., 283, (1993) 97.

Balagurov L. A., Yarkin D. G., and Petrova E. A., Mat. Sci. Eng. (B), 69, (2000) 127.

Bar-lev, A., Semiconductors and Electronic Devices, Third Edition, 1993.

Barret S., Gaspard F., Herino R., Ligeon M., Muller F., and Ronga I., Sensors and Actuators A, 33, (1992) 19.

Barry Bebb H., and Williams E. W., Semiconductors and Semimatels, Academic Press New York and London, 1972.

Bayliss S. C., Anstee P., Hutt D. A., Zhang Q., Danson N., Bates J., and Waddliove A., J. Appl. Phys., 76, (1994) 5171.

Beale M. I. J., Chew N. G., Uren M. J., Cullis A. G., and benjamin J. D., Appl. Phys. Lett., 46, (1985) 86.

Belyakov L. V., Goryachev D. N., Sreseli O. M., and Yaroshetskii, Semiconductors, 27, (1993) 1078.

Ben-Chorin M., Moller F., Kokh F., J. Lumin., 57, (1993) 159.

Ben-Chorin M., Kux A., and Schechter I., Appl. Phys. Lett., 64, (1994) 481.

Bessais B., Ezzaouia H., Elhouichet H., Queslati M., and Bennaceur R., Semicond. Sci. Technol., 11, (1996) 1815.

Bilenko D. J., Belobrovaja O.Ya., Coldabanova O. Yu., Jarkova E. A., Khasina E. I., Polyanskaya V. P., Melinkova T. E., Mysenko I. B., Smirnov V. V., and Filipova G. O., Sensors and Actuators, 79, (2000) 147.

Boarino L., Baratto C., Geobaldo F., Amato G., Comini E., Rossi A. M., Faglia G., Lerondel G., and Sberveglieri G., Mat. Sci. Eng., B69-70, (2000) 210.

Bogue R. W., Biosensors and Bioelectronics, 12 (1), (1997) xxvii.

Bomchil G., Halimaoui A., and Herino R., Appl. Surf. Sci., 41, (1989) 604.

Bomchil G., Herino R., Barla K., Pfister J. C., J. Electrochem. Soc., 130 (7), (1983) 1611.

Bomchil, G., and Halimaoui, A., Microelec. Eng., 8, (1988) 293.

Brace A. W., The technology of Anodising Aluminium, Technicopy Limited, 1968.

Brandet M. S., Fuchs H. D., Stutzmann M., Weber J., and Cardona M., Solid State Commun., 81, (1992) 307.

Bsiesy A., and Vial J. C., J. Lummin., 70, (1996) 310.

Bsiesy A., Nicolau Y. F., Ermolieff A., Muller F., and Gaspard F., Thin Solid Films, 255, (1995) 43.

Buda F., Kohanof J., and Parrinello M., Phys. Rev. Lett., 69, (1992) 1272.

(C)

Canham L. T., Appl. Phys. Lett., 57 (10), (1990) 1046.

Canham L. T., Leong W. Y., Beale M. I. J., Cox T. I., and Tayler L., Appl. Phys. Lett., 61, (1992) 2563.

Canham L. T., Physics World, (March 1992) 41.

Chand S., and Kumar J., J. Appl. Phys., 80, (1996) 288.

Chand S., and Kumar J., Semicond. Sci.Technol., 10, (1995) 1680.

Chelikowsky J. R., and Cohen M. L., Phys. rev. B, 14, (1976) 556.

Chopra A., Thin Films Solar Cells, Plenum, New York, 1983.

Ciurea M. L., Baltog I., Lazar M., Lancu V., Lazanu S., and Pentia E., Thin Solid Films, 325, (1998) 271.

Ciurea M. L., Pentia E., Manea A., Belu-Marian A., and Baltog I., Phys. Stat. Sol. B, 195, (1996) 637.

Cruz H., Luis D., and Capuj N. E., J. Appl. Phys., 83, (1998) 7693.

Cullis A. G., and Canham L. T., Nature, 353, (1991) 335.

Cullis A. G., Canham L. T., and Dosser O. D., Mat. Res. Soc. Proc., 256, (1992) 7.

Cullis A. G., Canham L. T., Williams G. M., Smith P. W., and Dosser O. D., J. Appl. Phys., 75, (1993) 493.

(D)

Dafinei A. S., and Dafinei A. A., J. Non-Crys. Solids, 245, (1999) 92.

Delerue C., Lannoo M., Allan G., and Martin E., Thin Solid Films, 255, (1995) 27.

Deresmes D., Marissael V., Stievenard D., and Ortega C., Thin Solid Films, 255, (1995) 258.

Diligenti A., Nannini A., Pennelli G., Pellegrini V., Fuso F., and Allegrini M., Thin Solid Films, 276, (1996) 179.

Dimitrov D. B., Phys. Rev,. 51, (1995) 1562.

Dimova-Malinovska D., Tzolov M., Tzonov N., and Nesheva D., Thin Solid Films, 297, (1997) 285.

Dittrich Th., Kliefoth K., Sieber I., Rappich J. Rauscher S., and Timoshenko V. Yu., Thin Solid Films, 276, (1996) 183.

(E)

Ellis B., Semiconductor Opto-Electronics, London Butterworth, 1973.

(F)

Fauchet P. M., J. Lumin., 70, (1996) 294.

Fellah S., Wehrespohn R. B., Gabouze N., Ozanam F., and Chazalviel J. N., J. Lumin., 80, (1999) 109.

Filippov, V. V., Pershukevich, P. P., Bondarenko, V. P., and Dorofeev, A. M., Phys. State Solid (B), 184, (1994) 573.

Foll H., Appl. Phys. A, 53, (1991) 8.

Foucaran A., Sorli B., Garcia M., Pascal-Delannoy F., Giani A., and Boyer A., Sensors and Actuators, 79, (2000) 189.

(G)

Gaburro Z., Bellutti P., Chierchia R., Mulloni V., and Pavesi L., Mat. Sci. Eng., B69-70, (2000) 109.

Gee A., J. Electrochem. Soc., 107, (1960) 787.

Gelloz B., Appl. Surf. Sci., 108 (4), (1997) 449.

Gelloz B., and Bsiesy A., Appl. Surf. Sci., 135, (1998) 15.

Gelloz B., Nakagawa T., and Koshida N., Appl. Phys. Lett., 73 (14), (1998) 2021.

Gole J. L., DeVincentis J. A., and Seals L., J. Phys. Chem. B, 103 (6). (1999) 979.

Goryachev D. N., Polisskii G., and Sreseli O. M., Semiconductors, 34 (2), (2000) 221.

Goryachev D. N., Sreseli O. M., and Belyakov L. V., Semiconductors, 31 (7), (1997) 716.

Gösele U., and Lehmann V., World Scientific, (1995) 17.

Goswami A., and Goswami A. P., Thin Solid Films, 16, (1973) 175.

Goudeau P., Naudon A., Bomchil G., and Herino R., J. Appl. Phys., 66, (1989) 625.

(H)

Halimaoui, A., Oules, C., and Bomchil, G., Appl. Phys. Lett., 59 (3), (1991) 304.

Heben M. J., and Tsuo Y. S., Mat. Res. Soc. Symp. Proc., 283, (1993) 353.

Henley V. F., Anodic Oxidation of Aluminium and its Alloys, Pergamon Press, Oxford, 1982.

Herino R., Billat S., Bsiesy A., Gaspard F., Ligeon M., Mihakcescu I., Muller F., Romastain R., and Vail J. C., Phisica Scripta T, 45, (1992) 300.

Herino, R., Bomchil, G., Barla, K., Bertrand, C., and Ginoux, J. L., J. Electrochem. Soc., 134, (1987) 1994.

Herino, R., Bomchil, G., Barla, K., Bertrand, C., and Ginoux, J. L., J. Electrochem. Soc., 134, (1994) 1987.

Hlinomaz N., Kima O., Hospodkova A., Hulicius E., Oswald J., Sipek E., and Kocka J., Appl. Phys. Lett., 64 (23), (1994) 3118.

Hovel H. J., Semiconductors and semimetals, Solar cells, Vol. 11, Academic Press, New York, 1975.

(I)

Ioffe A. F., Physics of Semiconductors, Infosearch Ltd, London, 1960.

Iyer S. S., and Xie Y. H., Porous Silicon, World Scientific, (1995) 53.

(K)

Kaifeng L., Yumin W., Lei Z., Shenyi W., and Xiangfu Z., Chin. Phys. Lett., 11, (1994) 289.

Kalkhoran N. M., Namavar F. and Maruska H. P., Mat. Res. Soc. Proc., 256, (1992) 89.

Kasap S. O., Principles of Electrical Engineering materials and devices, Irwin/McGraw Hill, New York, 1997.

Kazou I., Thin Solid Films, 84, (1981) 103.

Ke M., Williams R. H., Westwood D. I., and Recharson B. E., J. Microelectr. Eng., 31, (1996) 195.

Ke M., Matthai C. C., Pavlov A., and Laiho R., Appl. Surf. Sci., 123, (1998) 454.

Kelly M. T., and Bocarsly A. B., Coordination Chem. Rev., 171, (1998) 251.

Koch F., Petrove-Koch V., Muschik T., Nikolov A., and gavrilenko V., Mat. Res. Soc. Symp. Proc.,283, (1993) 197.

Kooij E. S., Despo R. W., and Kelly J. J., Appl. Phys. Lett, 66 (19), (1995).

Korol E.B., and Kikkarin S. M., tech. Phys. Lett., 26 (3), (2000) 223.

Koshida N., and Gelloz B., Current Openion in Colloid and interface Science, 4, (1999) 309.

Koshida, N., and Koyama, H., Appl. Phys. Lett., 60 (3), (1992) 347.

Koshida, N., and Koyama, H., Mat. Res. Soc., 283, (1993) 337.

Koshida, N., and Koyama, H., Optoelectron. Dev. Tech., 7 (1), (1992b) 103.

Koshida, N., Koyama, H., Jap. J. Appl. Phys., 30 (7), (1991) L1221.

Koyama H., Shima N., and Koshida N., Phys. Rev. B, 53 (20), (1996) 13291.

Kozlowski F., and Lang W., J. Appl. Phys., 72, (1992) 5401.

Krotkus A., and Pasiskevicius V., Electron. Lett., 28, (1992) 1137.

(L)

Lalic N., and Linnros J., J. Appl. Phys., 80 (10), (1996) 5971.

Lavine J. M., Sawan S. P., Shieh Y. T., and Bellezza A. J., Appl. Phys. Lett., 62 (10), (1993) 1099.

Lazarouk S., Bondarenko V., Jaguiro P., Lacquaniti N., Monica S. La., Maiello G., Masini G., Ferrari A., J. Non-Crys. Solids, 198-200, (1996) 973.

Lebedev A. A., Remenyuk A. L., and Rud Yu. V., Semiconductors, 27, (1995) 1017.

Lee M. K., and Peng K. R., Appl. Phys. Lett., 62, (1993) 3159.

Lee M. K., Wang Y. H., and Chu C. H., Solar Energy Materials and Solar Cells, 59, (1999) 59.

Lehmann V., and Gösele U., Appl. Phys. Lett., 58, (1991) 856.

Lehmann V., Cervand H., and Gösele U., Mat. Res. Soc. Proc., 256, (1992) 3.

Lockwood D. J., Aers G. C., Allard L. B., Bryskiewicz B., Charbonneau S., Houghton D. C., McCaffrey J. P., and Wang A., Can. J. Phys., 70, (1992) 1184.

Lopez H. A., and Fauchet P. M., Appl. Phys. Lett., 75 (25), (1999) 3989.

Luth H., Thust M., Stefen A., Kordos P., and Schoning M. J., Mat. Sci. Eng., B69-70, (2000) 104.

Lysenko V., Boarino L., Bertola M., Remaki B., Dittmar A., Amato G., and Barbier D., Microelectro. J., 30, (1999) 1141.

(M)

Mabrook M. F., Ray A. K., Ghassemlooy Z., and Brown S., IEE Materials for Displays, (1995) 14.

Mares J. J., Kristofic J., and Hulicius E., Thin Solid Films, 255, (1995) 272.

Mares J. J., Kristofik J., Pangrac J., and Hospodkova A., Appl. Phys.Lett., 63, (1993) 180.

Martin-Palma R. J., Guerrero-Lemus R., Moreno J. D., Martinez-Duart J. M., Gras A., and Levy D., Mat. Sci. Eng. (B), 69, (2000) 87.

Maruska, H. P., Namavar, F., and Kalkhoran, N. M., Mat. Res. Soc., 283, , (1993) 383.

Maruyama, T., and Ohtani, S., Appl. Phys. Lett., 65 11, (1994) 1346.

Mathur R. G., Vivechana, Mehra R. M., Mathur P. C., and Jain V. K., Thin Solid Films, 312, (1998) 254.

Matsuda, A., Matsuno, Y., Katayama, S., Tsuno, T., Tohge, N., and Minami, T., J. Amer.Ceram. Soc., 73 (8), (1990) 2217.

McGinnis S.P., Das B., and Dobrowolska M., Thin Solid Films, 365 (1), (2000) 223.

Memming R., and Schwartz G., Surf. Sci., 4, (1966) 109.

Menna P., Francia G. D., and Ferrara V.L., Sol. Energy Mater. Sol. Cells, 37, (1995) 13.

Mikrajuddin, Shi F. G., and Okuyama K., Microelec. J., 31, (2000)187.

Mikrajuddin, Shi F. G., and Okuyama K., Microelect. J., 31, (2000) 187.

Milnes A. G., and Feucht D. L., Hetrojunctions and metal-semiconductor junctions, Academic Press, New York, 1972.

Missous M., and Rhoderick E. H., Electron. Lett., 22, (1986) 477.

Molnar K., Mohacsy T., Varga P., Vazsonyi E., and Barsony I., J. Lumin., 80, (1999) 91.

Moss T. S., Optical Properties of Semiconductors, Butterworths, London, 1961.

Motohiro T., Takeda Y., Hyodo s. A., Hioki T, and Noda S., Porous Silicon, World Scientific, (1995) 99.

Muller F., Herino R., Ligeon M., Gaspard F., Romestain R., Vial J. C., and Bsiesy A., J. Lumin., 57, (1993) 283.

(N)

Namavar, F., Maruska, H. P., and Kalkhoran, N. M., Appl. Phys. Lett., 60 (20), (1992) 2514.

Nishimura K. Nagao Y., and Ikeda N., Jpn. J. Appl. Phys., 37, (1998) L303.

Nyrup S. B., Poulsen M., and Veje E., J. Porous Matt., 7, (2000)267.

(O)

Ogasawara K., Momma T., and Osaka T., J. Electrochem. Soc., 142 (6), (1995) 1874.

Ozaki T., Araki M., Yashimura S., Koyama H., and Koshida N., J. Appl. Phys., 76 (3), (1994) 1986.

(P)

Pacebutas, V., Krotkus, A., Simkiene, I., and Viselga, R., J. Appl. Phys., 77 (6), , (1995) 2501.

Palsule C., Liu S., Gangopadhyay S., Holtz M., Lamp D., and Kristiansen M., Solar Energy Mat. Siler Cells, 46, (1997) 261.

Pankove J. I., Optical Processes in Semiconductors, Dover Publications, New York, 1971.

Parkhutik V. P., Thin Solid Films, 276, (1996) 195.

Parkhutik V. P., Surf. State Electr., 43, (1999) 1121.

Parkhutik V. P., Glinenko L. K., and Labunov V. A., Surf. Tech., 20, (1983) 265.

Parkhutik V. P., Matveeva E. S., and Calleja R. D., Electrochemica Acta, 41, (1996)1313.

Pasiskevicius V., Deringas A., and Krotkus A., Appl. Phys. Lett., 63, (1993) 2237.

Pavesi L., Guardini R., and Bellutti P., Thin Solid Films, 297, (1997) 272.

Peng, C., Tsybeskov, L., and Fauchet, P., Mat. Res. Soc., 283, (1993) 121.

Perkowitz S., Optical Characrerisation of Semiconductors, Academic Press, New York: London, 1993.

Peter L. M., and Wielgosz R. I., Appl. Phys. Lett., 69 (6), (1996) 806.

Popkirov G. S., and Ottow S., J. Electroanal. Chem., 429, (1997) 47.

Proot J. P., Delerue C., and Allan G., Appl. Phys. Lett., 61, (1992) 1948.

Pulsford N. J., Rikken G. L. J. A., Kessener Y. A. R. R., Lous E. J., and venhuizen A. H. J., J. Lumin., 57, (1993) 181.

Pulsford N. J., Rikken G. L. J. A., Kessener Y. A. R. R., Lous E. J., and venhuizen A. H. J., J Appl. Phys., 75, (1994) 636.

(R)

Rajaraman R., Copalan P., and Premila M., Solid State Commun., 102 (1), (1997) 65.

Ray A.K., Mabrook M. F., Nabok A. V. and Brown S., J. Appl. Phys., 84 (6), (1998) 3232.

Read A. J., Needs R. J., Nash K. J., Canham L. T., Calcott P. D. J., and Qteish A., Phys. Rev. Lett., 69, (1992) 1232.

Rees, G., Physics World, (January 1991) 23.

Ribes A. C., Damaskinos S., Tiedje H. F., Dixon A. E., Brodie D. E., Duttagopta S. P., and Fauchet P. M., MRS Symp. Proc. Mater. Res. Soc., 426, (1996) 581.

Rice T. M., Solid State Physics, Academic Press, 1977.

Riess W., karg S., Dyakonov V., Meier M., and Schwoere M., J. Lumin., 60, (1994) 906.

Riley D. J., Peter L. M., and Wielgosz R. I., Abst. Pap. Am. Chem. S, 201, (1996) 184.

Roy A., Chainani A., Sarma D. D., and Sood A. K., Appl. Phys. Lett., 61, (1992) 1655.

(S)

Sakai T, Suzuki T., and Zhang L., Jpn J. Appl. Phys., 34, (1994) 179.

Sanders G. D., and Chang Y. C., Phys. Rev. B., 45, (1992) 9202.

Sawada S., Hamada N., and Ookubo N., Phys. Rev., 49, (1994) 5236.

Schechter I., Ben-Chorin M., and Kux A., Anal. Chem., 67, (1995) 3727.

Schwarz R., Wang F., Ben-Chorin M., Grebner S., Nikolou A., and koch F., Thin Solid Films, 255, (1995) 23.

Simons A. J., Cox T. I., Uren M. J., and Calcott P. D. J., Thin Solid Films, 255, (1995) 12.

Skryshevsky V. A., Appl. Surf. Sci., 157 (3), (2000) 145.

Smith R. L., and Collins S. D., J. Appl. phys., 71, (1992) R1.

Sparkes J. J., Semiconductor Devices, Chapman Hall, London, 1994.

Steigmeier E. F., Delly B., and Auderset H., Physica Scripta T, 45, (1992) 305.

Steiner P., Kozlowski F., Sandmaier H., and Lang W., Mat. Res. Soc., 283, , (1993) 343.

Stievenard D., and Deresmes D., Appl. Phys.Lett. 67, (1995) 1570.

Streetman B.G., Solid State Electronic Devices, Fourth Edition, Prentice Hall, New Jersey, 1995.

Street R. A., Hydrogenated Amorphous Silicon, Cambridge University Press, 1991.

Stutzmann M., Brandt M., rosenbauer M., Weber J., and Fuchs H. D., Phys. Rev. B, 47, (1993) 4806.

Sze, S. M., Physics of Semiconductor Devices, Second Edition, Wiley, New York, 1981.

(T)

Takasuka E., and Kamei K., Appl. Phys. Lett., 65, (1994) 484.

Teschke O., Appl. Phys. Lett., 64 (15), (1994) 1986.

Thust M., Schoning M. J., Schroth P., Malkoc U, Dicker C. I., Stefen A., Kordos P., and Luth H., J. Molecular Catalysis B, 7, (1999) 77.

Tsuo Y. S., Heben M. J., Wu X., Xiao Y., Moore C. A., Verlinden P., and Deb S. K., Mat. Res. Soc. Symp. Proc., 283, (1993) 405.

Tsybeskov L., Duttagupta S. P., and Fauchet P. M., Solid State Commun., 95 (7), (1995) 429.

Tung R. T., Appl. Phys. Lett., 58, (1991) 2821.

Turner D. R., J. Electrochem. Soc., 105, (1958) 402.

(U)

Uhlir A. Jr., Bell. Syst. Tech. J., 35, (1956) 333.

Unagami T., and Seki M., J. Electrochem. Soc. 125 (8), (1978) 1339.

Unagami T., J. Electrochem. Soc., 127, (1980) 476.

Ünal B., and Bayliss S. C., J. Appl. Phys., 80, (1996) 3532.

(V)

Vial J. C., Bsiesy A., Gaspard F., Herino R., Ligeon M., Muller F., Romestain R., and Macfarlane R. M., Physical Review B, 45, (1992) 14171.

Vikulov V. A., Strikha V. I., Sktyshevsky V. A., Kilchitskaya S. S., Souteyrand E., and Martin J. R., J. Phys. D-Appl. Phys., 33, (2000) 1957.

Voos M., Leheny R. F., and Shah J., Radiative Recombination, in Handbook on Semiconductores, North Holland Publishing Company, 1980.

(W)

Wang B., Wang D., Zhang L., and Li T., Thin Solid Films, 293, (1997) 40.

Wood D., Optoelectrinic Semiconductor Devices, Practice Hall, New York, 1994.

(X)

Xue F., Bao X., and Yan F., J. Appl. Phys., 81, (1997) 3175.

(Y)

Yan F., Bao X., and Gao T., Sol. State Comm., 91, (1994) 341.

Yarkin D. G., Semiconductors, 33, (1999) 180.

Yeh E. C. C., Chan G. H., Shieh, T. H., and Hsu K. Y. J., Phys. Stat. Solid. (A), 165, (1998) 63.

(Z)

Zhang X. G., Collins S. D., Smith R. L., J. Electrochem. Soc., 136 (5), (1989) 1561.

Zhang X. G., J. Electrochem. Soc., 138 (12), (1991) 3750.

Zheng J. P., Jiao K. L., Shen W. P., Anderson W. A., and Kwok H. S., Appl. Phys.Lett., 61, (1992) 459.

Zimin S. P., Semiconductors, 34, (2000) 353.

APPENDIX

LEAST SQUARE FITTING PROGRAM

```
1  Is=0.72e-12;
2  q=1.602e-19;
3  V=0.4;
4  T=152;
5  K=1.38e-23;
6  I=0.3e-6;
7  range=I*0.05;
8
9  steps=100;
10
11 sat=0;
12
13 ni=zeros(1,50);
14 nr=zeros(1,50);
15
16 for  n=1.01:0.001:1.2,
17    Rs=50;sat=0;
18 while  sat==0,
19    temp=(q) * (V-I*Rs) / (K*T);
20    I_temp=1-exp(-1*temp);
21    Ix=Is*exp(temp/n);
22    Ix=Ix*I_temp;
23
24  if abs(Ix-I)<range,
25    disp(Rs) , disp(n);
26    sat=1;
27  end
28 Rs=Rs+steps;
29 end
30 end
31
```