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Research and Development of CdS/CdTe solar cells incorporating ZnTe layers

Fijay Bin Fauzi

A thesis submitted in partial fulfillment of the requirements of Sheffield Hallam University for the degree of Doctor of Philosophy

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Declaration

I hereby declare that this thesis is my own work and it has not been submitted elsewhere for any award.

Abstract

This thesis presents experimental work and analysis in research and development of low-cost thin film solar cells. In this work, three semiconducting materials were studied. These semiconducting materials are from group II-VI or also known as 'two-sixers' from periodic table. The semiconductors are cadmium sulfide (CdS), cadmium telluride (CdTe) and zinc telluride (ZnTe).

All of these layers were obtained by growing them using electrodeposition in aqueous solutions. In this project, electrodeposition using 2-electrode system was employed to deposit all of the semiconductors. The decision was taken to avoid contamination that might be happening due to the leakage of foreign ions such as K^+ and Ag^+ contained in the reference electrode into the electrolyte.

To help in optimizing the semiconducting layers, three characterization techniques were used frequently. These techniques are optical absorption, x-ray diffraction (XRD) and photoelectrochemical (PEC) cell measurements. These techniques were used to study the optical, structural and electrical conductivity type of the electrodeposited layers respectively. After optimizing the layers using the above three techniques (optical absorption, XRD and PEC), other advance analytical techniques (SEM, XRF, D.C. conductivity measurement, photoluminescence and UPS) were used to fully characterize the materials. This information was also used to further optimize the material layers.

At the later stage of this project, research was concentrated on fabricating and assessing solar cell devices. Initial devices fabricated had glass/FTO/CdS/CdTe/Au structure. Current-voltage (I-V) measurement was employed to assess the performance of solar cell devices by measuring the open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF) and conversion efficiency (η). The highest efficiency obtained from this solar cell structure was 10.1%. However, this structure had low fill factors in the range of 0.25 to 0.4.

To solve this problem, an insulating layer was incorporated into the device to create metal-insulator-semiconductor type structures. Results have shown that by electrodepositing insulating p-type ZnTe layers on top of CdTe, the fill factor can be improved.

Acknowledgement

In the name of Allah, the most Beneficent, the most Merciful. Peace and blessing of Allah be upon to His noble prophet Muhammad (*Sallallahu Alaihi Wassallam*).

I would like to take this opportunity to thank my Director of Studies, Professor I.M. Dharmadasa for his excellent guidance and tireless motivation. I also appreciate the contribution made by my second supervisor Dr. Aseel Hassan in helping me to complete this thesis. I remain indebted to the staff of Materials and Engineering Research Institute (MERI) especially Prof Douglas Cleaver, Deeba Zahoor, Vinay Patel, Bob Burton, Yashodhan Purandare, Vikas Kumar, Corrie Houton, Gillian Hill and others due to their sincerity of helping me in completing this research programme.

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List of Publications

Journal Publications:

1. **F Fauzi**, D G Diso, O K Echendu, V Patel, Y Purandare, R Burton and I M Dharmadasa, *"Development of ZnTe layers using an electrochemical technique for applications in thin-film solar cells"*, Semicond. Sci. Technol. **28** (2013) 045005 (10pp).

2. O K Echendu, A R Weerasinghe, D G Diso, **F Fauzi** and I M Dharmadasa, *"Characterization of n-Type and p-Type ZnS Thin Layers Grown by an Electrochemical Method"*, Journal of Electronic Materials 42 (2013) April 2013, Volume 42, Issue 4, pp 692-700.

3. D G Diso, **F Fauzi**, O K Echendu, A R Weerasinghe and I M Dharmadasa, *"Electrodeposition and characterisation of ZnTe layers for application in CdTe based multi-layer graded bandgap solar cells"*, Journal of Physics: Conference Series 286 (2011) 012040.

4. O K Echendu, A R Weerasinghe, **F Fauzi** and I M Dharmadasa, *"High short-circuit current density CdTe solar cells using all-electrodeposited semiconductors"*, Thin Solid Films 556 (2014) pp 529-534.

5. N. A. Abdul-Manaf, O. K. Echendu, **F. Fauzi**, L. Bowen and I. M. Dharmadasa, *"Development of polyaniline using electrochemical technique for plugging pinholes in cadmium sulfide/ cadmium telluride solar cells"*, Journal of Electronic Materials 43 (2014) pp 4003-4010.

6. I.M. Dharmadasa, O.K. Echendu, **F. Fauzi**, H.I. Salim, N.A. Abdul-Manaf, J.B. Jasinski, A. Sherehiy and G. Sumanasekera, *"Study of Fermi level movement during CdCl2 treatment of CdTe thin films using Ultra-violet Photoemission Spectroscopy"*. (Submitted to Materials Chemistry and Physics on 26/09/2014).

7. D.G. Diso, **F. Fauzi**, O.K. Echendu and I.M. Dharmadasa, *"Optimisation of CdTe Electrodeposition Voltage for Development of CdS/CdTe solar cells"*, (submitted to Coatings on 13/10/2014).

8. I. M. Dharmadasa, O. K. Echendu, **F. Fauzi**, N. A. Abdul Manaf, H. I. Salim, T. Druffel, R. Dharmadasa and B. Lavery, "*Effects of CdCl2 treatment on deep levels in CdTe and their implications on thin film solar cells; A comprehensive photoluminescence study*". (Submitted to Coatings on 15/12/5014).

Conference Publications:

1. H M Yates, D W Sheel, I M Dharmadasa, O K Echendu and **F Fauzi**, *"The effects of TCO properties on all electrodeposited CdS/CdTe PV solar cells"*, PVSAT-9, Swansea University, 10-12 April 2013.

2. O K Echendu, A R Weerasinghe, D G Diso, **F Fauzi** and I M Dharmadasa, *"n-CdTe based multi-layer graded bandgap solar cell using all electrodeposited semiconductors"*, PVSAT-9, Swansea University, 10-12 April 2013.

3. I M Dharmadasa, O K Echendu, R Dharmadasa and **F Fauzi**, *"Distortion observed in current-voltage characteristics of photovoltaic solar cells"*, 27th EU PVSEC, Frankfurt, 24-28 September 2012.

4. **F. Fauzi**, N.A.A Manaf, O.K. Echendu and I M Dharmadasa, "*Electrochemical deposition of organic and inorganic pin-hole plugging layers for CdS/CdTe solar cells"* Solar Asia 2013, University of Malaya, 22-24 August 2013.

5. O K Echendu, **F Fauzi**, L Bowen, and I M Dharmadasa, "*All electrodeposited, multilayer graded bandgap solar cells using II-VI semiconductors"* 28th EU PVSEC, Paris, 30 September – 4 October 2013.

6. N. A. Abdul-Manaf, O. K. Echendu, **F. Fauzi**, L. Bowen and I. M. Dharmadasa, *"Electrodeposition and Characterization of polyaniline to develop organic/inorganic hybrid solarc cells based on cadmium telluride"*, 28th EU PVSEC, Paris, 30 September – 4 October 2013.

7. O. K. Echendu, **F. Fauzi** and I. M. Dharmadasa, *"Effect of ($CdCl_2$+CdF_2) treatment on the conversion efficiency of CdS/CdTe solar cell"*, PVSAT-10, Loughborough University, 23-25 April 2013.

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Chapter 1: Introduction

1.1 Global needs for renewable energies

According to the recent survey by United Nations (UN), world's population is expected to reach 9.6 billion by 2050. This is an increase of 33% from the current population that stands at 7.2 billion people [1]. One of the factors that contribute to the increase of human population is the improvement of human healthcare system. For examples, the usage of vaccine to combat fatal diseases such as tuberculosis and also the decline of birth mortality. Another factor that helps the growth of human population is the sufficient food supply due to the better advancement in agricultural technologies. The usage of synthetic fertilizers and pesticides is the methods used today to increase the yield of from the crops planted. The huge increase of human population means more energy (for example, electricity) is needed to support the continuity of convenience living.

Dependency on fossil fuels such as coal, petroleum and natural gas is not the answer for sustainable energy supply. It is because these energy sources are limited and will exhaust in the future. Burning more fossil fuels to cater the demand for energy will do more harm than good. Since fossil fuels are limited in supply, gradually the consumers will have to pay more for energy. This change is inevitable because demands for energy will exceed supplies.

It is well known that fossil fuels are one of the contributing factors to the greenhouse effect. Fossil fuels will emit greenhouse gases to the environment after burning. Carbon dioxide (CO_2) and methane (CH_4) are the examples of greenhouse gases. Greenhouse gases accumulated at the space will absorb the heat radiated from the sun and retransmit it back to the Earth's surface. This reaction creates global warming due to the inability of the Earth to quickly dissipate heat to the atmosphere.

In 2006, Paramount Pictures released a documentary film titled The Inconvenient Truth. This film featured Al Gore, a politician, environmental activist and also the former candidate for president of United States of America (USA). According to Al Gore, data from Keeling curve showed that the concentration of CO_2 (measured in parts per million volume - ppmv) in atmosphere keeps increasing every year since 1958 [2]. From this film, the viewers can learn about the negative impacts of global warming.

Among the negative impacts are massive flooding, drought, wide spreading of vector-borne diseases and many more.

In order to reverse the effects of global warming, it is necessary to reduce the carbon emission. Carbon emission can be reduced by planting more trees, driving electric vehicles, using energy efficient bulbs and also utilizing renewable energies for electricity generation.

1.2 The sources of renewable energy

Renewable energy is defined as "the energy from a source that is not depleted when used" [3]. The sources of renewable energy are as follows.

1.2.1 Wind energy

Flow of wind naturally carries kinetic energy. By using appropriate equipments, this kinetic energy can be converted into electrical energy. Wind energy is the renewable energy that has been used for more than one thousand years [4]. In Netherlands, initially wind turbines were used to drain water from the farmlands into the river. Later, wind energy was used for agricultural purposes.

In Europe, the presence of strong wind at North Sea has been exploited by nearby countries such as United Kingdom and Denmark by building onshore and off-shore wind farms. Currently United Kingdom has the largest off-shore wind farm in the world known as the London Array. This wind farm has the installed capacity up to 630 MW and located 11 km to the north of North Foreland [5]. In Denmark, wind turbines with 3000 MW capacity have been installed before the end of 2005 [6]. By the end of 2007, electrical energy generated from the wind farms can supply 20% of its energy demand. Wind energy industry in Denmark also has provided jobs for nearly 29 000 people in 2008 [7].

There are two types of wind turbine; horizontal axis wind turbine (HAWT) and vertical axis wind turbine (VAWT). HAWT is the one that is widely used nowadays. The schematic diagram of HAWT is shown in Figure 1.1.

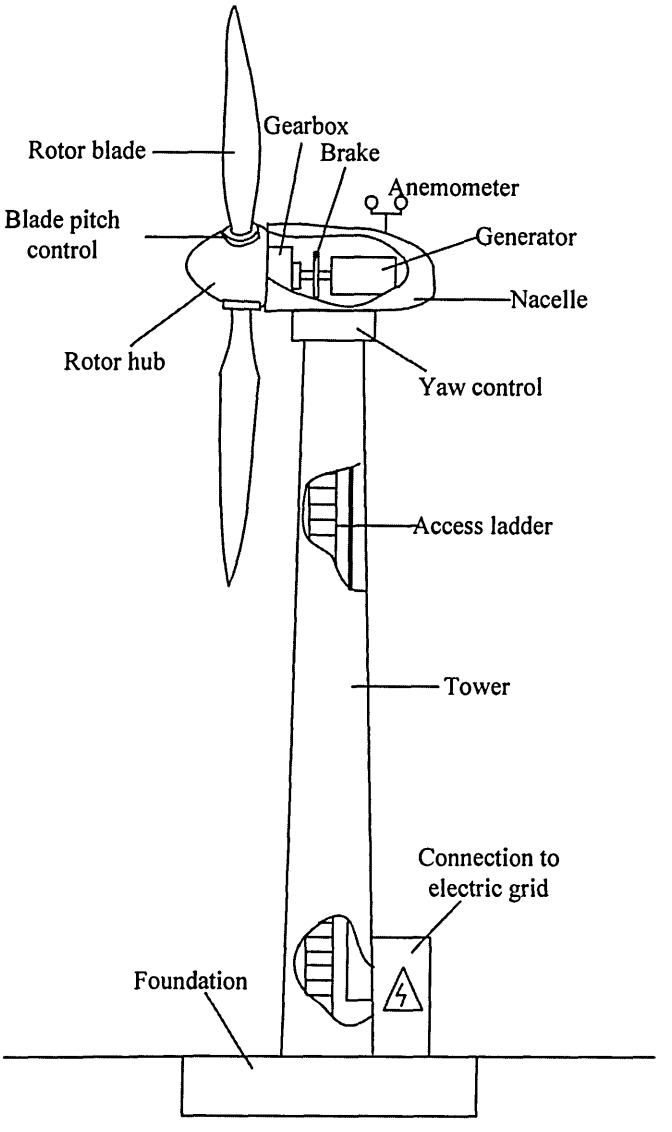

Figure 1.1: Horizontal axis wind turbine (HAWT) showing its main components. Redrawn from [8].

Basic components of HAWT consist of blades, gearbox, electrical generator, tower and yaw. After considering operational cost, maintenance cost and efficiency, few components are incorporated into the system such as controller, brake, anemometer and transformer. The blades are designed to have the same profiles like the aeroplane wings as shown in Figure 1.2. High speed wind flows at the top will create low pressure region while the low speed air stream at the bottom creates high pressure. The whole process finally induces lift upon the blades.

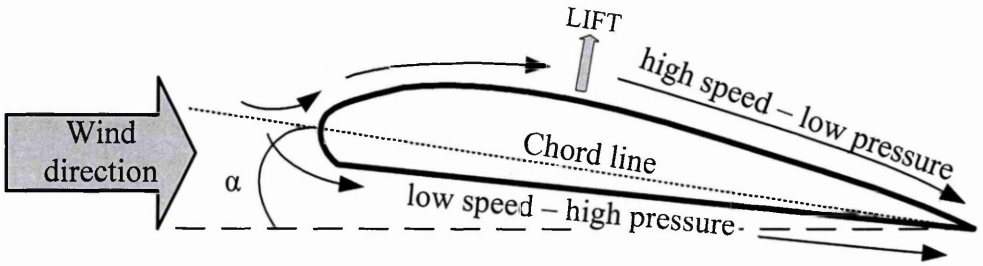

Figure 1.2: Aerodynamic helps induced lift on wind turbine blades. Redrawn from [9].

When the wind blows towards a wind turbine, the blades will rotate and so does the rotor hub. Rotor hub is connected to the low speed shaft. The connection between the low speed shaft and high speed shaft is implemented by the gearbox. Gearbox will increase the speed of the high speed shaft with respect to the low speed shaft but it depends on the gear ratios inside the gearbox.

A wind turbine is designed to operate below the maximum wind speed. This is called cut-out speed [10]. Above the cut-out speed, a wind turbine cannot withstand the force and strains asserted by the wind and could be damaged under severely harsh conditions. To solve this problem, wind turbines should have two main control mechanisms, the pitch control and yaw control.

Pitch control, as shown in Figure 1.3(a) is useful in slowing down the angular speed of a wind turbine. In pitch control mechanism, the blades will adjust their orientation relative to the wind direction until the maximum angle of attack, α is exceeded. When it happens, the blades are stalled and the lift will drop, thus slowing down the angular speed.

To have the maximum angular speed, the orientation of the nacelle should be directed towards the oncoming wind. Yaw control (Figure 1.3(b)) is employed to turn the nacelle vertically in order to ensure the direction of the nacelle always facing the oncoming wind.

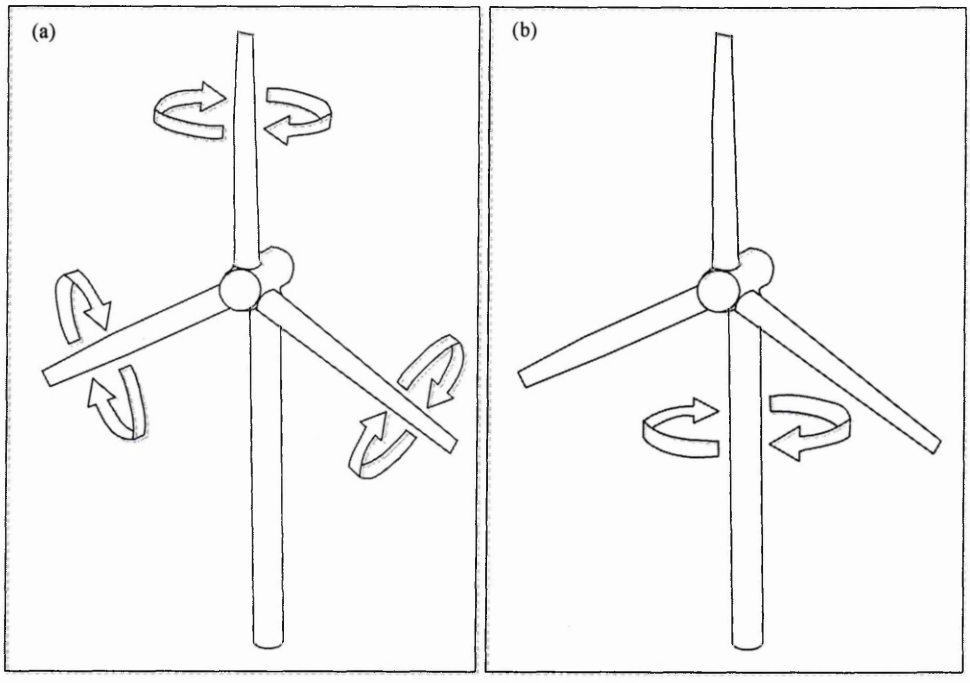

Figure 1.3: Pitch control (a) and yaw control (b) are employed to safeguard wind turbine from damages and to ensure highest possible power extracted from the oncoming wind respectively. Redrawn from [11].

Wind energy is abundant, clean and can be operational for 24 hours a day. However, wind energy harvesting is location specific and in addition, the direction and speed of wind are uncontrollable. The uncontrollability of wind direction and speed make the output from wind turbine difficult to be fixed constant.

1.2.2 Geothermal energy

Water trapped below the surface of the Earth is heated by molten and very hot solid rocks called magma. Magma is normally found at certain places on Earth, where the volcanic activities are present. Water that comes from the rain for example, can flow between the rocks that build-up Earth's crust and finally arrive close to the magma zone. Water that is located between the Earth's surface and magma will be heated up to 280°C naturally. This area is known as geothermal zone. Geothermal zone is located between 600 to 1500 m underground [12]. To extract this heated fluid, production well must be built. Production well is created by drilling down to the geothermal zone as shown in Figure 1.4. When the geothermal zone is found, the hot fluid will come to the Earth's surface driven by its own pressure. When the fluid comes up, it will be

channelled to the separator where water and steam are separated. Steam is used to drive steam turbine and generate electricity.

After driving the steam turbine, the steam will be turned back into water by condensation and sent back to the injection well together with the water collected in the separator. It is important to send the water back to the geothermal zone because without this feedback system, the fluid extracted at the production well be depleted too fast before it is replenished. Geothermal energy is clean, renewable and has almost zero CO_2 emission but the cost of electricity coming from this technology is still expensive compared to fossil fuels. The main reason is; to build a geothermal power plant, the cost will be higher compared to the fossil fuel power plants. This is due to the drilling works involved.

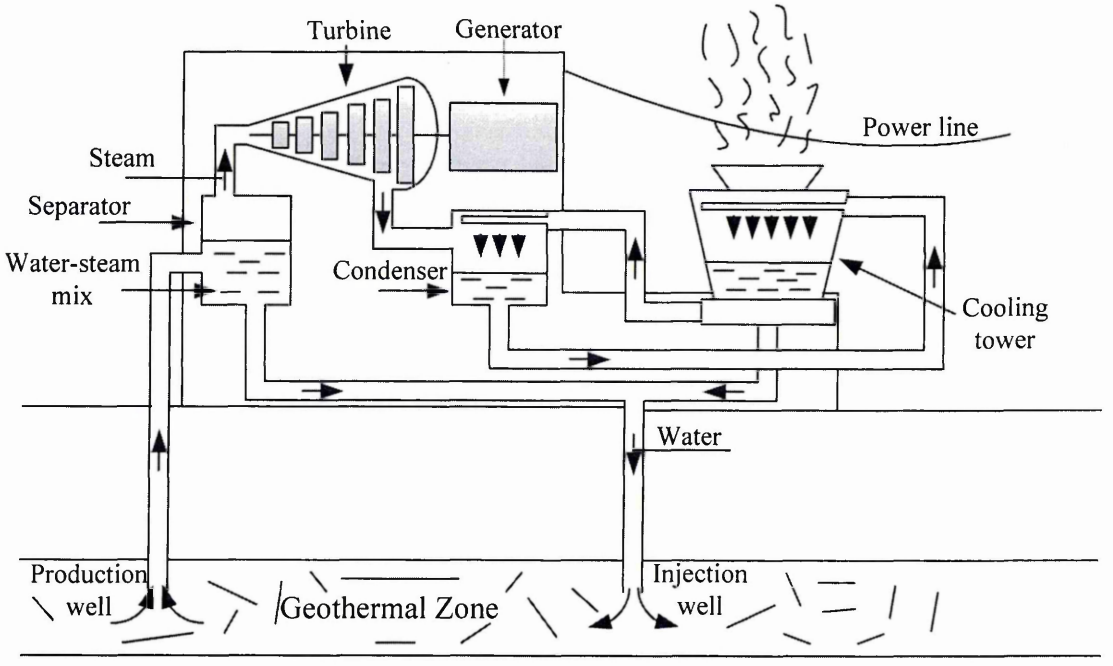

Figure 1.4: Main features of a geothermal energy system. Redrawn from [13].

1.2.3 Hydroelectricity

Hydroelectricity (shown in Figure 1.5) is the conversion of potential energy of water to electrical energy. Hydro power has been used for hundreds of years. People during the ancient civilisation used water mill for agricultural purposes such as grinding grains and irrigation. To utilize hydro power, dam must be built at the most strategic location across a river. When a dam is constructed, the flow of water from one side to

the other side can be controlled. Close to the dam huge water reservoir will be built to increase the water storage.

The next task for hydropower engineers is to install turbines and intakes. Installation of intakes will allow hydro power plant operators to control the flow of water through the turbines. The control of water flow through the turbines will determine the electrical power output. If the demand for electrical power is high, more intakes will be open so that more turbines will be driven thus generates more power. Hydro power plant can be built to supply electrical power in gigawatt range. Examples given, Three Gorges Dam in China (22.5 GW) [14], Itaipu Dam at Brazil and Paraguay border (14 GW) [15] and Tucurui Dam in Brazil (8 GW) [16]. Besides fossil fuel and nuclear power plants, hydropower plants also capable for supplying electricity for base load demand to households and industries. The available power, P can be calculated from Equation 1.1 [17],

$$P = \eta.\rho.Q.g.h \tag{1.1}$$

Where;

P is the power in watts
η is the dimensionless efficiency of the turbine
ρ is the density of water in kilograms per cubic metre
Q is the flow in cubic metres per second
g is the acceleration due to gravity
h is the height difference between inlet and outlet

Even though hydro power has zero fuel cost and nearly zero CO_2 emission during operation, the cements and metals used in the construction of a dam are the sources for CO_2 and CH_4 emission. The capital cost to build a hydropower plant is hugely expensive. The cost includes civil engineering works, land reclamation, population relocation, etc. Besides that, the construction of hydropower plant could lead to the deteriorations of environmental quality nearby the power station. News regarding these issues have been reported in *Nature* magazine in May 2011 [18].

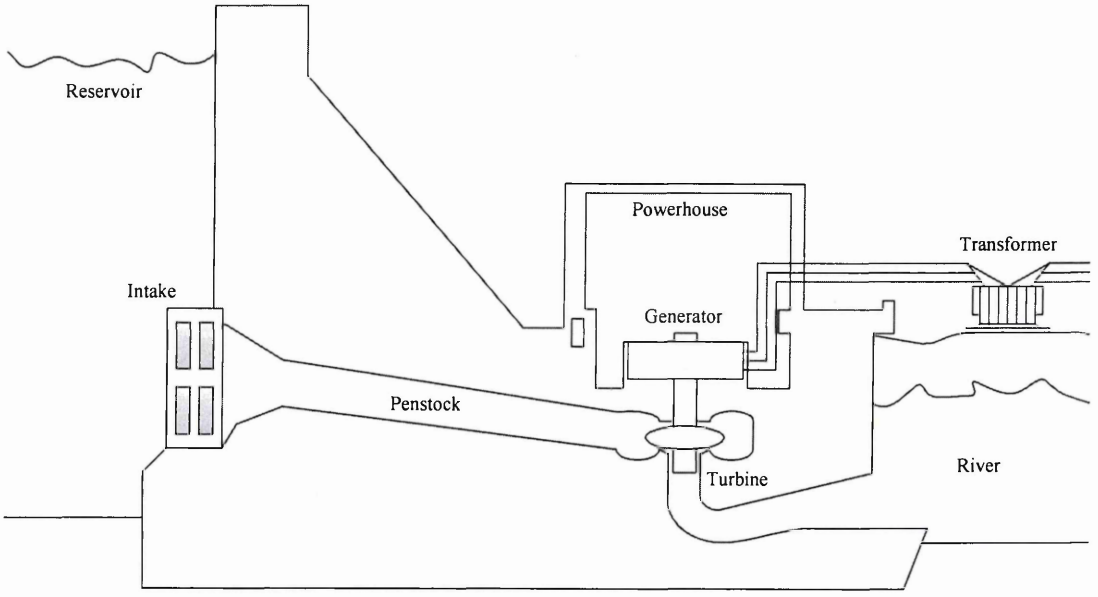

Figure 1.5: A typical hydroelectricity system showing its main features. Redrawn from [19].

1.2.4 Tidal energy

Tidal power uses the same concept as in hydropower electricity (shown in Figure 1.6). In some countries where estuaries are available, water barrage can be built to capture and store huge volume of water. Water can be captured when the high tide occurs. The captured water is stored at the basin. When the tide becomes low, water from the basin will be released back to the sea. The flow of water back to the sea will drive turbines and thus generates electrical power. Tidal electricity that employs this kind of mechanism is hugely expensive and needs feasibility studies before the construction begin to ensure least impact on the environment especially aquatics life.

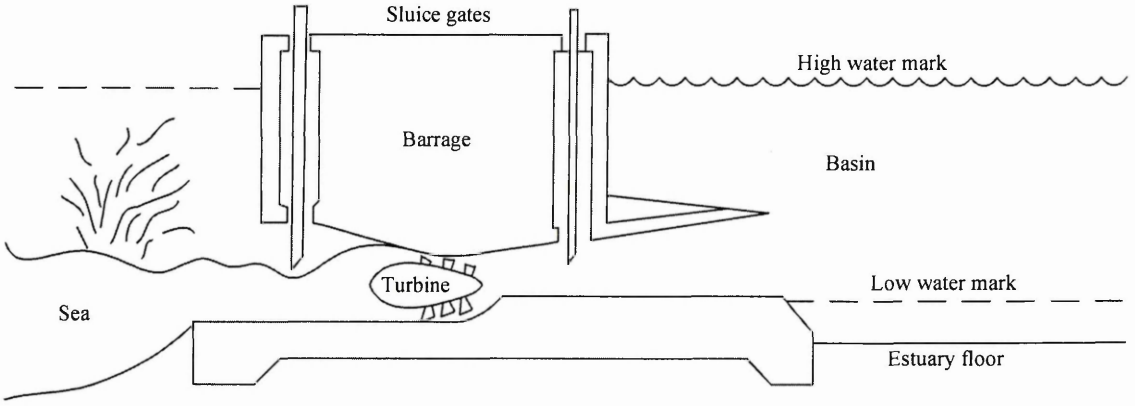

Figure 1.6: Schematic diagram of a typical tidal power generator. Redrawn from [20].

1.2.5 Oscillating water column (wave energy)

Oscillating water columns (OWC) are built along the sea shores and use air as the fluid to rotate the turbines inside. When wave hit the water columns, the air trapped inside water columns will be pushed to go inside the tunnel as shown in Figure 1.7(a). The air pressure asserted on the turbine will induce torque and rotates the turbine. When the wave recedes, the atmospheric pressure will push the air inside but from the opposite direction as shown in Figure 1.7(b). In OWC, Wells turbine is used. Wells turbine (Figure 1.7) is specially engineered so that no matter which direction the wind flows, the rotation is fixed in only one direction. This will ensure the constant rotation of turbines producing electrical power.

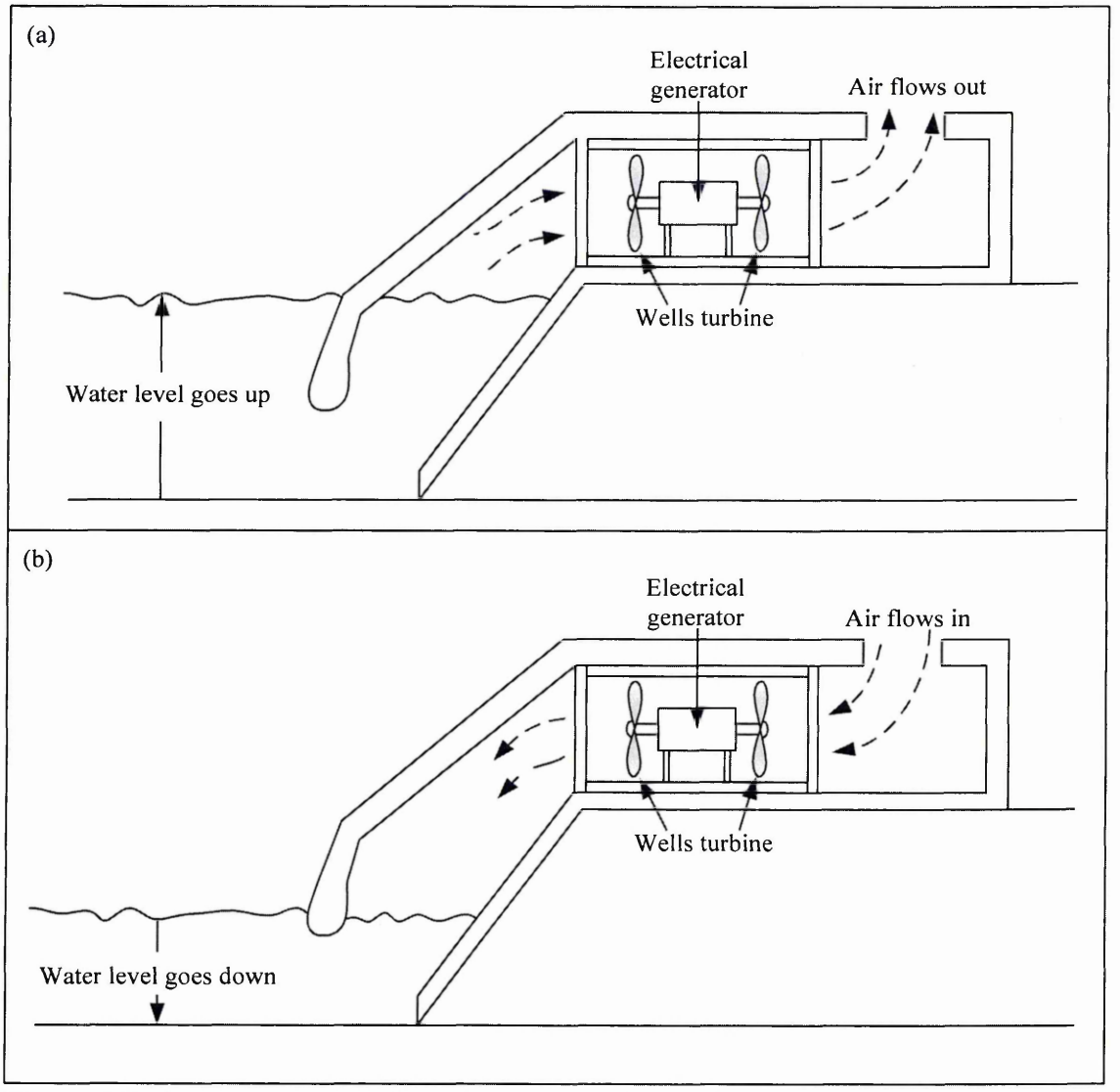

Figure 1.7: An ocean water column is engineered to maintain continuous output power from the powertrain installed inside.

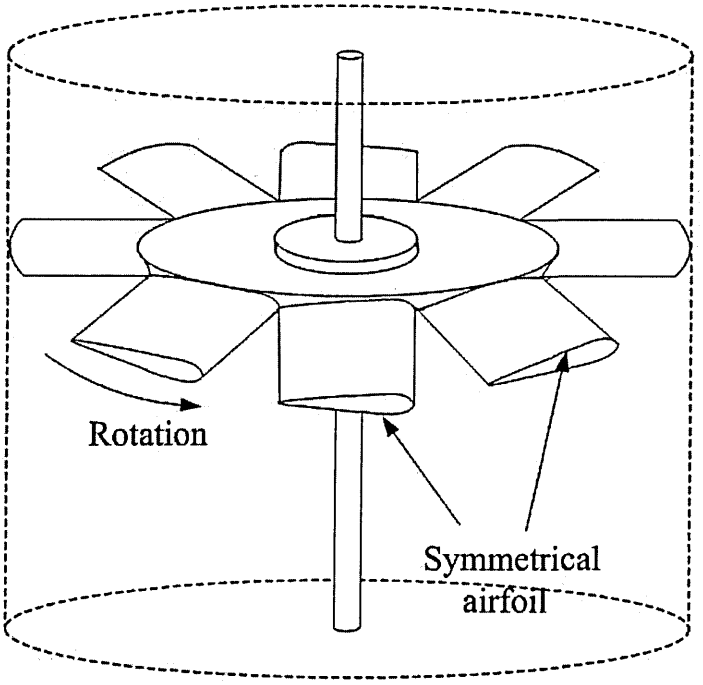

Figure 1.8: Wells turbine has symmetrical airfoil for all blades to ensure only one-way rotation. Redrawn from [21].

1.2.6 Biomass energy

Biomass energy is already being used nowadays. Lack of landfills available today, drives the policymakers to think the alternative ways of managing wastes. Any waste that is biodegradable is the source of biomass. The sources of biomass are shown in Figure 1.9. Some biomass energy systems depend on the production of synthetic gas (syngas) from biomass sources. Syngas is the mixture of carbon monoxide (CO) and hydrogen (H_2). The next sub-section will be discussing about anaerobic digestion and gasification.

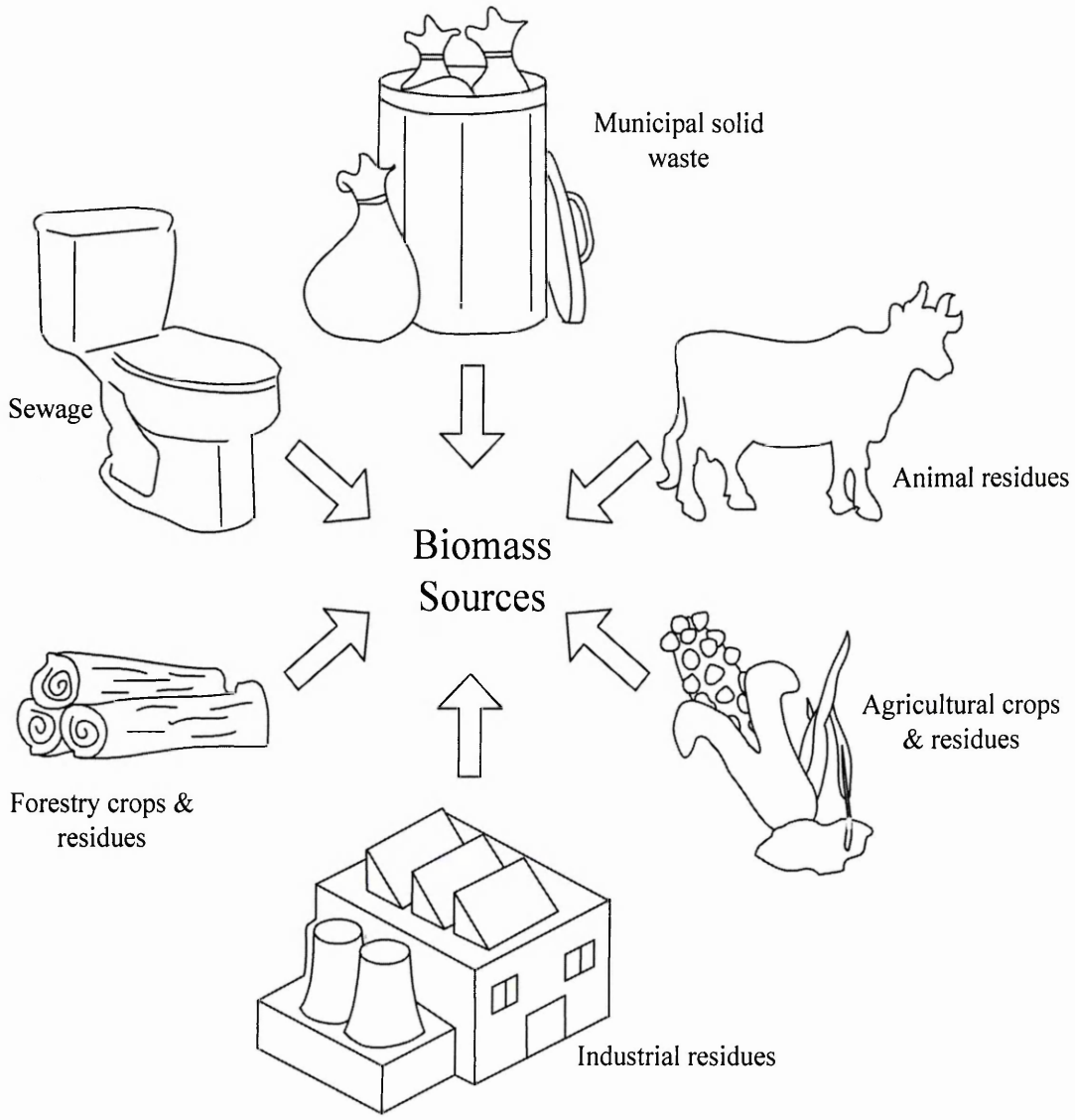

Figure 1.9: Various sources for biomass energy. Redrawn from [22, 23].

1.2.6.1 Anaerobic digestion

In anaerobic digestion, bacteria from methanogens family digest the biological wastes and produce CH_4, H_2S and NH_3. Figure 1.10 shows the process of producing biogas from anaerobic digestion. Biodegradable waste is collected and dumped into the storage pit. From the storage pit, the size of waste is reduced using mincer and then stored. The waste will be transferred to the fermentation tank. In the fermentation tank, methanogens bacteria, which is naturally occurring, will digest the biological waste and produce biogas. To generate electricity from biogas, the combustion of biogas is done inside a gas turbine.

Alternatively, biogas can also be upgraded to biomethane by removing other gases. As a result, biomethane content could be 96% of methane gas [24]. Waste collected from the fermentation tank is rich in nutrients such as ammoniums and phosphates and can be used as fertilizer.

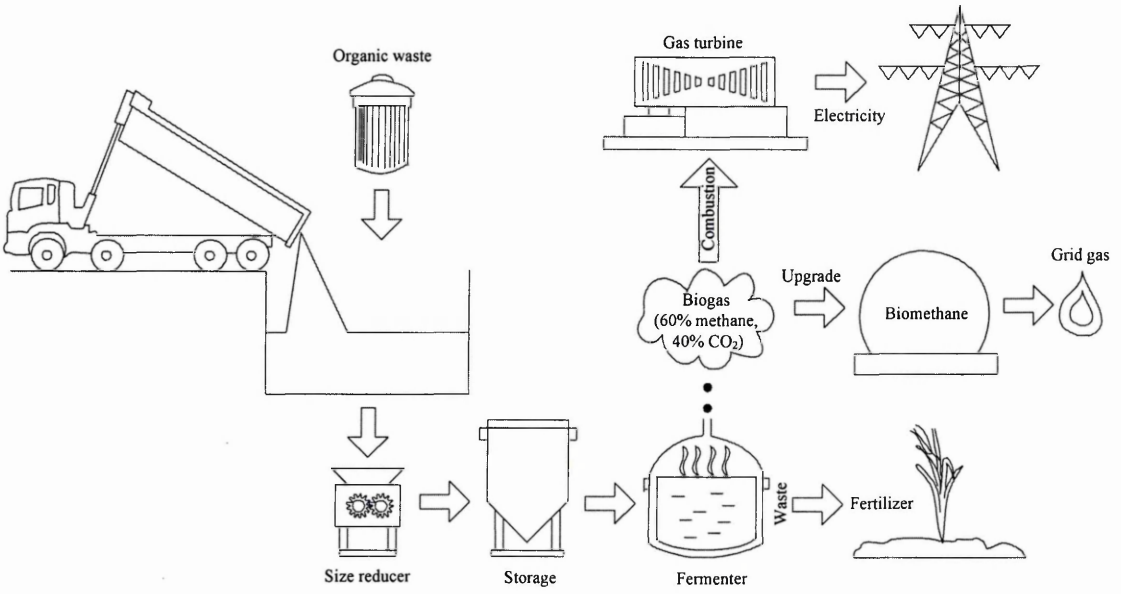

Figure 1.10: Electricity generation from anaerobic digestion. Redrawn from [25,26].

1.2.6.2 Gasification

Gasification is a form of chemical reaction of biomasses in oxygen-starved environment. Woods together with forestry residues and industrial wastes are biomasses that cannot be biodegraded by anaerobic bacteria. Syngas can be extracted from these wastes through gasification process as shown in Figure 1.11. Any carbon containing substance can be used as the feedstock. High temperature and pressure around 1400°C and 6900 kPa [27] respectively are used in gasification process. Firstly, chemical reaction called pyrolysis happens inside the gasifier thus producing chars and volatiles such as methane, hydrogen and tars. In the next stage, carbon containing compounds react with oxygen to form CO_2 and heat, which later will be utilized for futher reactions.

When chars (carbon containing material) react with steam, the syngas is produced according to the chemical rection;

$$C + H_2O \rightarrow H_2 + CO \qquad (1.2)$$

Gaseous constituents will go to the top of the gasifier and will undergo clean-up process. Firstly, any particle that co-exists with syngas will be removed. At the second stage, sulfur will be removed. Finally syngas that contains two of its main components (CO and H_2) is produced. Steam reforming and water-gas shift are the next major steps involved in order to obtaine methane and hydrogen. Both gases are normally employed for combustion in gas turbine. To minimize the waste of heat energy, steam turbine can be incorporated into the system. This is to utilize the heat energy coming out from syngas combustion and convert the heat into electrical energy.

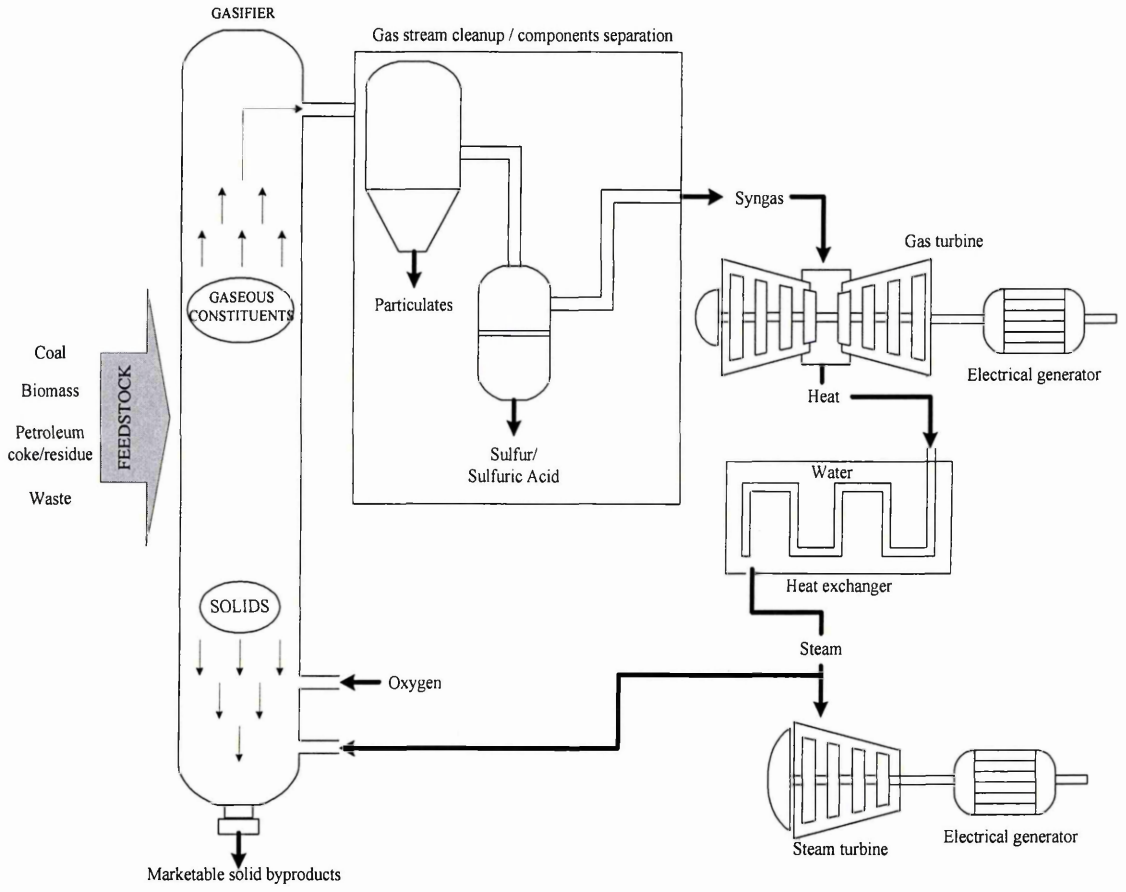

Figure 1.11: Electricity generation from gasification. Redrawn from [28].

The main advantage of using biomass energy is the sources of biomass are easy to get. Since biomass sources can be obtained from waste, they can be classified as cheap fuels. Utilizing biomass energy is also helpful in solving landfill problems. Increasing number of population means the need for bigger landfills is inevitable. Biomass energy can help in minimizing this problem because instead of sending more wastes to the landfills, the wastes can be converted into energy.

Biomass sources carry low energy per unit weight compared to fossil fuels. However, depending on location, biomass energy can be utilized to supply electricity for base load.

1.2.7 Solar energy

Sunlight is a form of energy originates from the sun. Sunlight emits electromagnetic radiation that consists of three radiation regions which have different frequencies. These radiations are ultraviolet (UV), visible (Vis) and infrared (IR) and commonly represented as the solar spectrum as shown in Figure 1.12. Ultraviolet radiation has wavelengths that are less than 400 nm. For visible radiation, the wavelengths are between 400 nm to 700 nm and above 700 nm is an infrared region. Figure 1.12 shows that the magnitude of spectral irradiance is different between the radiation at the top of the atmosphere and radiation at sea level. It shows that solar spectrum that reaches the Earth's surface has undergone attenuations and absorptions at the atmosphere. Hazardous ultraviolet radiation will be absorbed by the ozone layer. As a result, the solar spectrum that reaches the Earth is safe for all live forms.

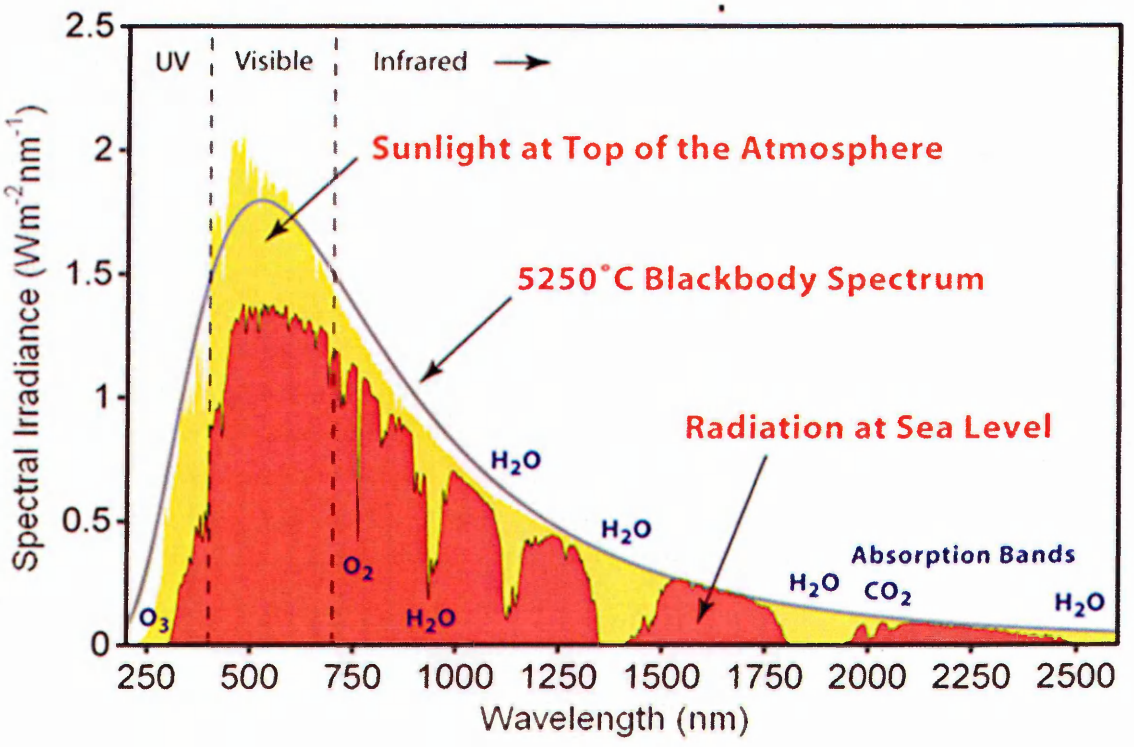

Figure 1.12: Solar spectrum showing spectral irradiance against wavelength. Three radiation regions (UV, Vis and IR) are also shown [29].

The solar irradiance (measured in Wm^{-2}) is governed by the air mass coefficient (simply known as air mass - AM). Air mass coefficient is defined as reciprocal of cos Θ_z. Where Θ_z is the angle between the actual position of the sun with respect to the zenith as shown in Figure 1.13 [30].

$$AM = \frac{1}{\cos \Theta z} \tag{1.2}$$

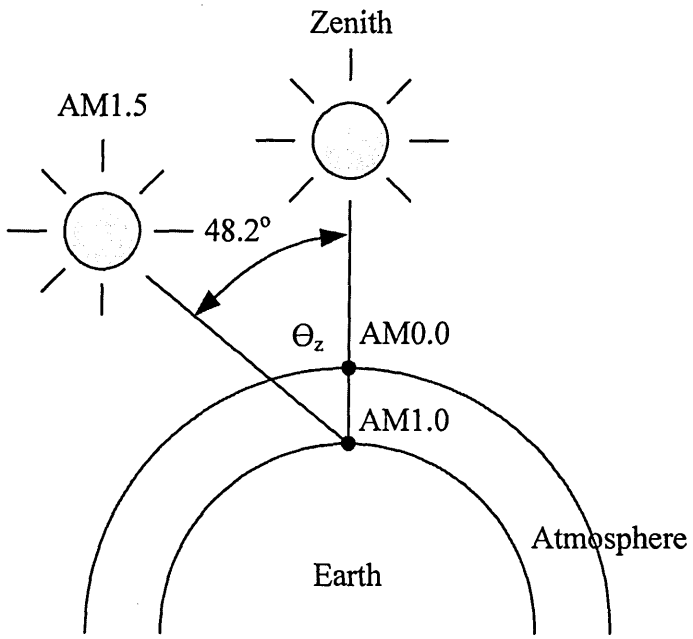

Figure 1.13: Determination of air mass coefficient based on the position of the sun with respect to the zenith.

When the sun stands at the zenith, the air mass coefficient at the top of the atmosphere is known as AM0.0. The power incident per unit area (solar irradiance) at this location is ~1367 Wm^{-2} [30]. This value is designated as the solar constant. At the sea level, the air mass is known as AM1.0 and the solar irradiance will further reduce to just over ~1000 Wm^{-2} [31]. This reduction is due to the absorption and scattering of the incident radiation by particulate matter, clouds and air molecules [30]. If the sun moves 48.2° from the zenith, the power incident per unit area on the Earth's surface is equivalent to ~1000 Wm^{-2}. At this location, air mass coefficient is known as AM1.5 and it is widely used among the solar cells researchers around the world to evaluate the performance of solar cells and solar panels [29].

There are two ways to harvest solar energy and convert it directly into heat or electrical energy. The first method is known as solar thermal conversion. Generally, thermal conversion works by absorbing heat radiated from the sun using appropriate equipments. The heat absorbed can be used for other purposes. One of the examples of utilization of solar energy is concentrated solar tower. Section 1.2.7.1 will explain more about solar thermal conversion technology.

The second method is the photovoltaic (PV) conversion. Photovoltaic cell is an electronic device that converts light energy directly into electrical energy. In this conversion, special materials are used to absorb light (photons). Energy of the photons will later be converted into electrical energy when photons interact with valence electrons inside the absorbing materials. Further explanations of photovoltaic conversion are given in section 1.2.7.2.

1.2.7.1 Solar thermal conversion (Concentrated Solar Tower)

Concentrated solar tower utilizes heat from the sun. Incoming radiation is reflected towards the top of the solar tower with the help of many heliostats. During the daytime, the heliostats are controlled to assure the maximum heat radiation is projected to the top of the solar tower. Temperature at the top of the solar tower can go up to 550°C or higher depending on designed system. Figure 1.14 shows how the solar tower is operated.

Molten salt is pumped from the storage up to the top of the tower to be heated. Molten salt is used because it has higher boiling point than water and does not dissipate heat as quickly as water. The heated molten salt is channelled to the hot molten salt tank. The hot molten salt tank needs to be properly insulated because it serves as the energy storage. The heat energy stored for 15 hours has been demonstrated by Gemasolar power plant in Spain [32]. Heat energy stored here can be used during the night. The hot molten salt will be sent to the heat exchanger where it acts as a fuel to boil water and turn the water into steam. Later, the steam is used to drive the steam turbines. Electrical energy is generated when the steam turbine is connected to the electrical generator.

The first two solar towers were built in 1984. Firstly, the 2.5 MW THEMIS tower was built in the French Pyrenees, followed by the 1 MW Molten-Salt Electric Experiment in the United States of America (USA) [33]. Spain has solar towers with capacity exceeding 10 MW. The PS10 power plant with 10 MW output is the world's

first commercial solar tower [34]. United States of America currently has the largest concentrated solar power plant in the world with 354 MW capacity [35].

Solar tower is better compared to solar photovoltaic system in terms of the period of electricity generation. The utilization of molten salt as the energy storage makes possible for this system to produce electrical energy for 24 hours a day. However, this system could not encourage the public to produce their own electrical energy. Currently, many developed countries around the world such as United Kingdom, USA, Germany, etc, encourage their citizen to install their own solar panels. In return, the governments will purchase the energy produced by any household through the system called feed-in tariff.

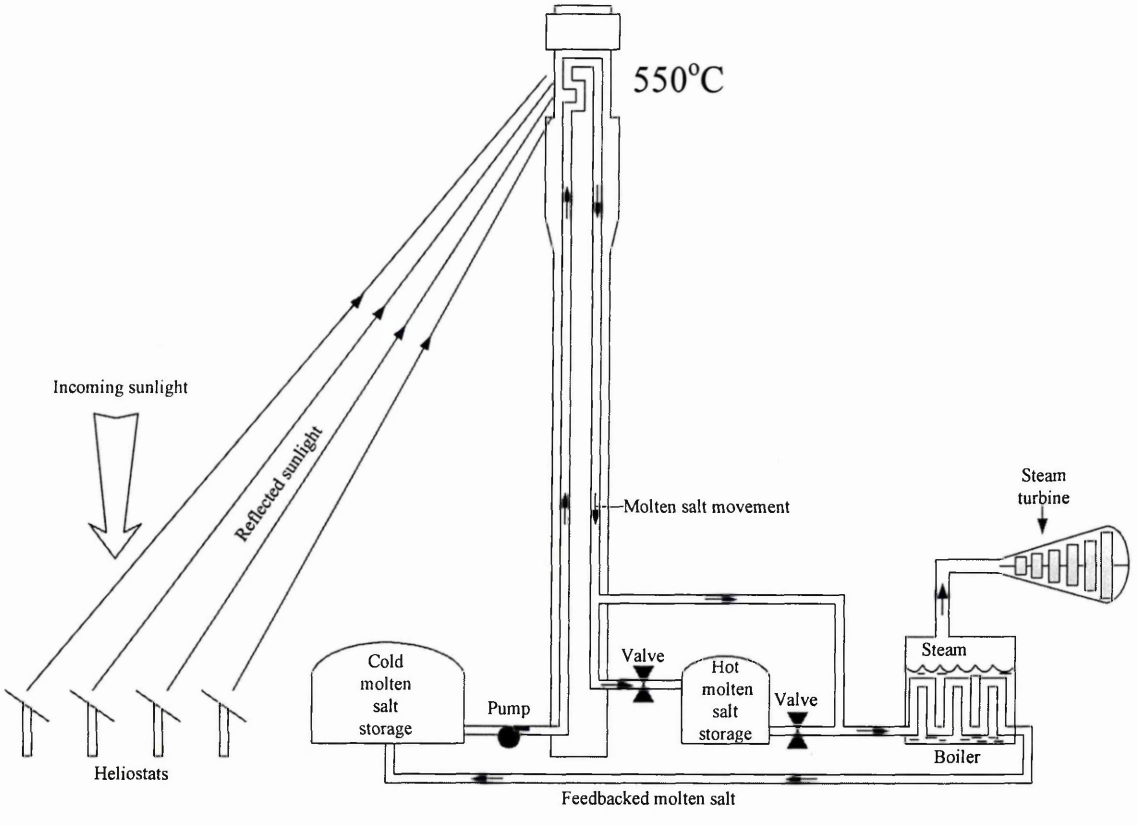

Figure 1.14: Schematic diagram of a concentrated solar power plant.

1.2.7.1 Photovoltaic (PV) conversion

There are some materials that can absorb light (photons) and convert the energy of the incident photons into electrical energy. These materials are known as absorber materials incorporated in solar cells. When photons are absorbed, these photons will interact with the valence electrons of the solar cell materials by giving off their energy

to the valence electrons. Since valence electrons gain more energy, they will move to the higher energy states or may be liberated from the host atom. The liberated electrons are now free to move inside the crystal of the absorbing material and can create useful current if they are separated and transported to an external electrical circuit.

Four basic steps must be brought together simultaneously in order to achieve effective photovoltaic energy conversion [36]:

i. solar cells absorb photons
ii. charge carries (electron-hole pairs - EHPs) are created
iii. separation of charge carriers before recombination
iv. transport of charge carriers through external circuit to provide useful electrical current.

Figure 1.15 shows how a solar cell works in converting photons into useful current. The heart of an efficient solar cell is the built-in electric field or simply a photovoltaic (PV) active junction. In simple words, the role of a PV junction (for example, p-n junction) is to sweep away photo-generated electrons and holes to the opposite directions. By sweeping electrons and holes to the opposite directions, these charge carriers will be forced to move through the external circuit thus creating an electrical current. Further explanations about p-n junction are given in Chapter 2.

Solar cells should have metal contacts at the front and the back. The role of metal contacts is to efficiently collect charge carriers by providing low electrical resistance at these interfaces. This will increase the efficiency of solar cells.

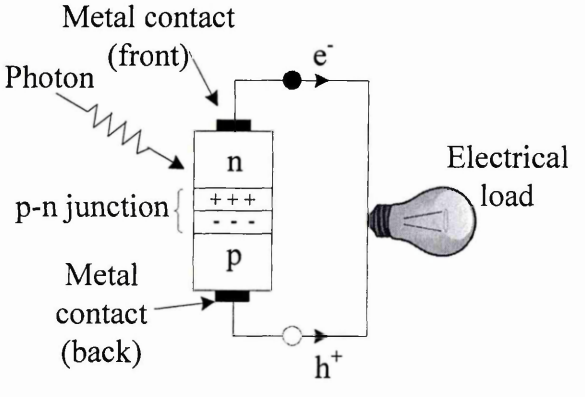

Figure 1.15: The role of a p-n junction is to absorb light, create electron-hole pairs and then sweep these charge carries to the opposite directions.

1.3 Aim and objectives

During the past two decades, research progress in CdS/CdTe solar cell has been stagnated due to lack of understanding in this complex electronic device. Majority of research groups work on p-n hetero-junction structure between n-type cadmium sulfide (n-CdS) and p-type cadmium telluride (p-CdTe). After Britt and Ferekides reported 15.8% efficiency in 1993 [37], the efficiency of the CdS/CdTe just increased to 16.5% after 8 years [38].

In 2002, Dharmadasa *et al* proposed a new model to explain the photovoltaic activity of CdS/CdTe solar cells. They proposed that in the future, the development of CdTe solar cells should be based on the new design which is the n-n hetero-junction between n-CdS/n-CdTe plus large Schottky barrier at the back of the cell [39]. In this paper, they have reported 18% conversion efficiency. The solar cells were fabricated using electrodeposited CdTe from non-aqueous solution (ethylene glycol) at temperature of 160°C.

However, the primary use of ethylene glycol as the automobiles' coolant and anti-freeze agent raise concerns about the toxicity. The safer way to electrodeposit semiconducting materials is by substituting ethylene glycol with deionized or double distilled water as the solvent. In fact, the performance of CdTe solar cells electrodeposited from an aqueous electrolyte is satisfactory if judging from the reported efficiencies by BP Solar (14.2%) [40] and Baker *et al* (13.5%) [41].

The main aim of this research project is to contribute towards the development of low-cost high efficiency thin film solar cells. Most works carried out in this project are based on the previous works reported by D.G. Diso [42]. In his works, he has identified the suitable growth voltages to electrodeposit CdTe layers using 2-electrode system in an aqueous electrolyte. From his work, he found that the suitable voltages to grow CdTe layers are from 1570 mV to 1580 mV. He also reported the highest efficiency of 7.6% with solar cell structure shown in Figure 1.16.

Both semiconductors; cadmium sulfide (CdS) and cadmium telluride (CdTe) layers were grown by electrodeposition. In literature, the structure is written as glass/conducting glass/CdS/CdTe/back contact [43,44]. Significance progress has been achieved previously, this research is the continuation of works from D.G. Diso [41]. In simple words, this is a long term project of making reproducible low-cost and high efficiency solar cells.

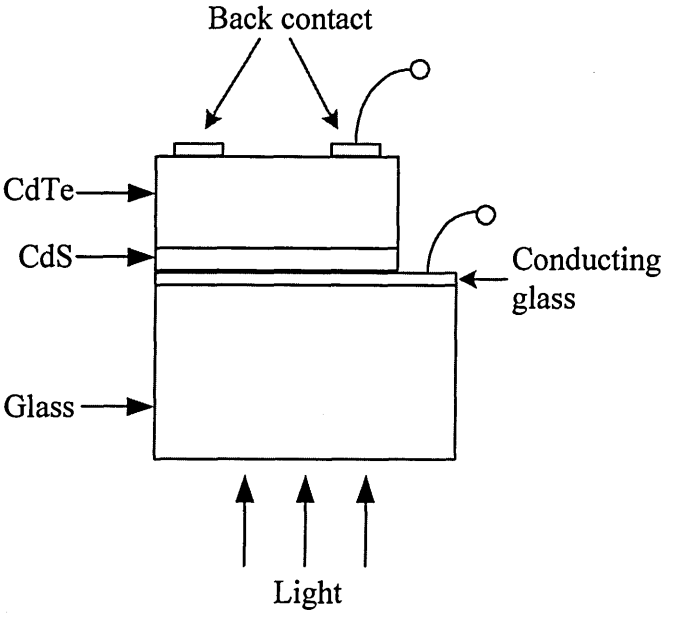

Figure 1.16: The schematic diagram of the basic CdS/CdTe solar cell.

This research project involves material growth by low-cost electroplating technique, materials characterisation, solar cell fabrication, assessment and development. Therefore, the objectives of this research are as follows:

i. To optimise the electrodeposition of three semiconducting materials; CdS, ZnTe and CdTe using electrodeposition with 2-electrode system in aqueous electrolytes.
ii. To study the structural, optical, electrical, compositional and morphological properties of the electrodeposited layers using facilities available at Materials and Engineering Research Institute at Sheffield Hallam University.
iii. To fabricate CdS/CdTe thin film solar cells using all electrodeposited layers. Two solar cell structures were fabricated. Firstly, the glass/TCO/CdS/CdTe/ metal structure. Secondly, the glass/TCO/CdS/CdTe/ZnTe/metal structure.
iv. To assess the performance of the fabricated thin film solar cells using current-voltage (I-V) measurement and developed these devices by optimising all processing steps to achieve highest possible efficiencies.

1.4 Summary

This chapter started with the economic and environmental issues facing humanity nowadays. It is obvious that the dependency on fossil fuels is not the answer for healthier and greener planet. Gradual replacement of fossil fuels with renewable energies as the prime energy source is the best answer for energy security.

Among the renewable energies discussed in section 1.2, solar energy seems to be the best candidate for terrestrial renewable energy application [36]. Solar energy is free, abundant, environmental friendly and produces near zero carbon emission.

At the last section of this chapter, the aim and objectives of this research programmed were also presented.

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2.1 Introduction

A brief introduction of solar cell and photovoltaic (PV) effect has been presented in Chapter 1. As a continuation, this chapter will firstly, introduce the intrinsic and extrinsic materials for solar cells application followed by the explanation on how the electron-hole pairs (EHPs) are created and separated inside a solar cell.

2.2 Solar energy materials

In physics, materials can be classified into three groups. They are conductors, insulators and semiconductors. Table 2.1 shows the classification of conductor, semiconductor and insulator materials. They are separated with each other according to their electrical conductivity and bandgap values.

Table 2.1: Classisfication of materials according to their electrical conductivities and bandgaps [1].

Parameter	Conductors	Semiconductors	Insulators
Conductivity (S)$(\Omega cm)^{-1}$	~ 10^{6}-10^{0}	~ 10^{0}-10^{-8}	~ 10^{-8}-10^{-20}
Bandgap (E_g) (eV)	≤ 0.3	~ 0.3-2.5	~ 2.5-10

Solar cells are fabricated from semiconductors. Materials for semiconductor are assigned into particular groups according to their position in periodic table. Table 2.2 lists the elements used for the production of semiconducting materials.

Table 2.2: Elements used for producing semiconducting materials according to their position in periodic table [1].

Group - I	Group – II	Group - III	Group – IV	Group - V	Group - VI
Cu	Zn	B	C	N	S
Ag	Cd	Al	Si	P	Se
		Ga	Ge	As	Te
		In	Sn	Sb	

Semiconducting materials include elemental semiconductors such as carbon, silicon and germanium and also compound semiconductors. Compound semiconductors are produced from the chemical reaction of two or more elements as listed in Table 2.2. If one element from group II is chemically reacted with one element from group VI through chemical reaction, the resulting materials are known as II-VI semiconductors. Examples of II-VI semiconductors are ZnTe, CdS and CdTe. Similarly, if one element from group III is chemically reacted with one element from group V, the resulting materials are known as III-V semiconductors.

Ternary and quaternary compound semiconductors are produced through the chemical reaction of three and four elements respectively. Table 1.3 shows various types of semiconducting materials.

Table 2.3: Examples of semiconducting materials. Materials shown are elemental, binary, ternary and quaternary compound semiconductors.

Semiconductor family	Examples of Semiconductors
Group IV Elemental semiconductors	C, Si, Ge
III-V binary semiconductors	AlN, AlP, AlAs, GaN, GaP, GaAs, InP,
II-VI binary semiconductors	ZnS, ZnTe, ZnO, CdS, CdSe, CdTe,
Ternary compound semiconductors	$CuInSe_2$, $Cd_xHg_{(1-x)}Te$, $Al_xGa_{(1-x)}As$
Quaternary compound semiconductors	$CuInGaSe_2$ (CIGS), Cu_2ZnSnS_4

2.2.1 Intrinsic and extrinsic materials

Silicon is the most researched semiconductor in the past 70 years. The discovery of p-n junction in 1940 by American physicist, Russell Ohl has led to the invention of electronics devices such as diodes, LEDs, transistors, solar cells etc [2]. Any pure material with very low impurities is called intrinsic materials. Inside intrinsic silicon, the silicon atoms are bound with each other with covalent bonding as shown in Figure 2.1.

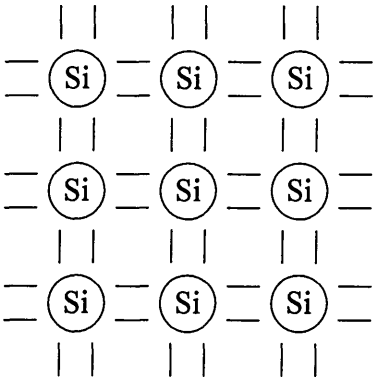


Figure 2.1: Covalent bonding in silicon crystal lattice.

If one of the valence electrons in Figure 2.1 receives sufficient energy, for example, heat from surrounding, it can untie itself from the covalent bond and move inside the crystal. This unbound electron can now contribute to the flow of electrical current. By having more free electrons, the magnitude of electrical current can be increased.

In device physics, it is more appropriate to present intrinsic semiconductors with energy band diagram as shown in Figure 2.2. A conventional energy band diagram normally shows the valence band (E_V), conduction band (E_C), forbidden bandgap (E_g) and Fermi level (E_F). The black dots in Figure 2.2 represent the valence electrons. At Fermi level, the probability of finding an electron is 0.5 according to the Fermi-Dirac probability function, $f_F(E)$ shown in Equation 2.1 [3].

$$f_F(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)} \tag{2.1}$$

Where;

E is the electrons energy (eV)

E_F is the Fermi level (eV)

k is the Boltzmann constant (1.38×10^{-23} JK^{-1})

T is the temperature (K).

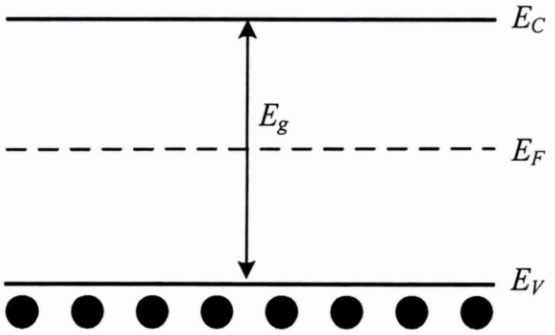


Figure 2.2: Conventional energy band diagram of intrinsic material showing the position of valence band, conduction band and Fermi level.

The valence band represents the highest energy level occupied by electrons while the lowest unoccupied energy band is known as the conduction band. The energy gap between the bottom of the conduction band and the top of the valence band is called the bandgap. Bandgap represents the minimum energy (in eV) that is needed for an electron to be excited from the valence band to the conduction band. Different semiconductors will have different bandgap values. Conventionally, the Fermi level for an intrinsic material is positioned at the middle of the bandgap.

When an electron is promoted to the conduction band after receiving sufficient energy, it will create a vacancy in the valence band. This electron vacancy is known as a 'hole' and is represented by a white dot in Figure 2.3.

In order to create useful current, electrons in conduction band must be transported through an external circuit before they recombine with holes.

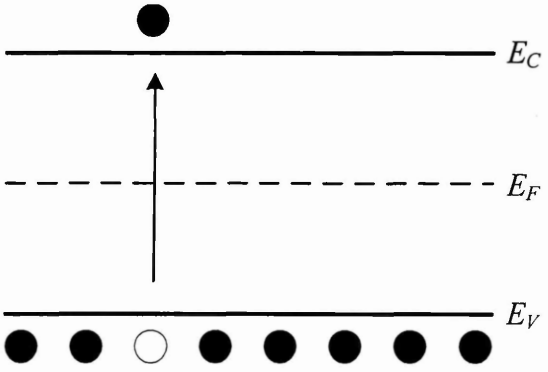


Figure 2.3: Creation of a hole in the valence band when an electron receives energy greater than the bandgap.

To increase the magnitude of electrical current, impurities can be added to the intrinsic materials as shown in Figure 2.4. In Figure 2.4, other elements such as phosphorus can be added into the silicon lattice. In this case, phosphorus (P) is called donor atom because it has an extra valence electron compared to silicon. This process is known as doping. By doping silicon with phosphorus, silicon now has more free electrons inside its lattice. Since it has impurities, it is no longer an intrinsic material. It has become an extrinsic material or simply known as an n-type material. The energy band diagram for n-type materials is shown in Figure 2.5. For n-type materials, the position of Fermi level is close to the conduction band.

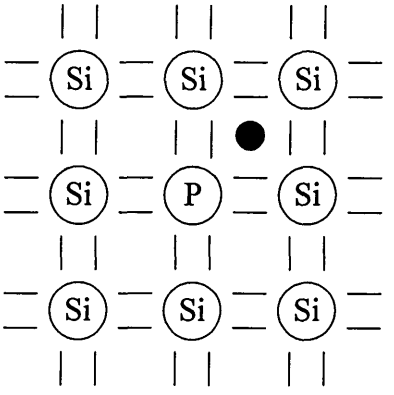


Figure 2.4: Covalent bonding between silicon atoms and phosphorus (P) atoms. P is called donor atom because it has one electron more than silicon atom.

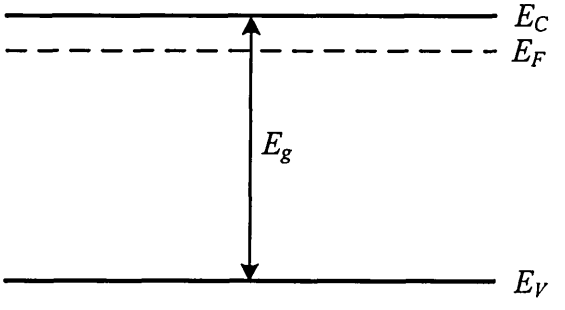


Figure 2.5: Energy band diagram for n-type material. Fermi level is positioned close to the conduction band.

If silicon is doped by atoms that have one electron less, for example, boron (B), it is called a p-type material. Figure 2.6 shows the bonding of boron atoms with silicon atoms. Since boron has one valence electron less than silicon, it is called acceptor atom. The energy band diagram for p-type materials is shown in Figure 2.7. For p-type

materials the position of Fermi level is close to the valence band. Table 2.4 summarizes the differences between n-type and p-type materials.

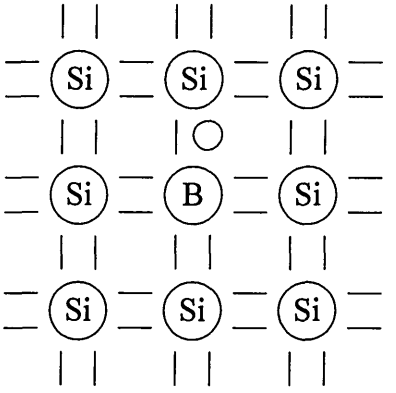


Figure 2.6: Covalent bonding between silicon atoms and a doping atom, boron (B). B is called an acceptor atom because it has one electron less than silicon atom.

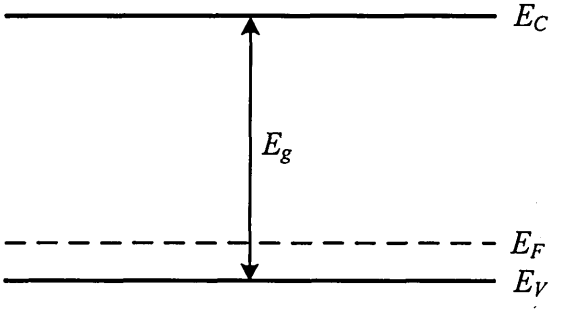


Figure 2.7: Energy band diagram for p-type materials. The Fermi level is positioned close to the valence band.

Table 2.4: Differences between n-type and p-type semiconductors.

n-type semiconductors	p-type semiconductors
• doped with donor atoms, native defects or composition variation • electrons are the majority charge carrier • holes are the minority charge carrier • Position of Fermi level is close to the conduction band	• doped with acceptor atoms, native defects or composition variation • holes are the majority charge carrier • electrons are the minority charge carrier • Position of Fermi level is close to the valence band

2.3 Solar cell interfaces

2.3.1 p-n junction

The heart of efficient solar cells lies within the photovoltaic active region. When two different semiconductors (p-type and n-type) are adjacent next to each other as shown in Figure 2.8, excessive electrons from the n-type material will diffuse into the p-type material. This leads to the leaving of positively charge ions at the vicinity of p-type material whilst the excessive holes from the p-type material diffuse into the n-type material, leaving the negatively charge ions at the vicinity of the n-type material.

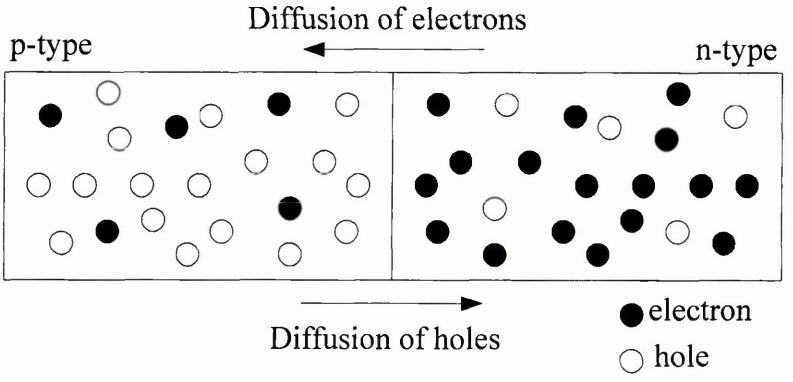


Figure 2.8: Directions of diffusion of electrons and holes.

This interaction will continue until the creation of a 'barrier' with particular width that prevents excessive electrons from the n-type material diffuse into the p-type material and vice versa. This 'barrier' is known as a p-n junction. In a p-n junction, a layer of negatively charge ions now sit inside the p-type material at the vicinity of n-type material. Inside the n-type material, a layer of positively charge ions now sit at the vicinity of the p-type material. Because of two layers from differently charged ions face with each other inside the p-n junction, electric field $\left(E_{mf} = -\frac{dV}{dx}\right)$ develops due to the electrostatic potential difference. The electric field is responsible in separation of photo-generated EHPs and minimizes the recombination. These two charged layers within the p-n junction are called depletion region because the concentration of free charge carriers is low within this region. Figure 2.9 shows the formation of p-n junction.

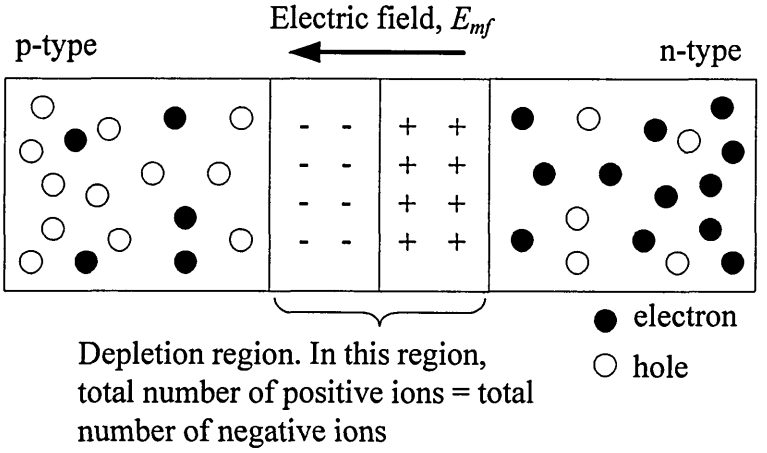


Figure 2.9: The formation of a p-n junction under equilibrium condition.

The formation of a p-n junction can also be represented with the energy band diagram. The band bending in Figure 2.10 represents the p-n junction or depletion region of Figure 2.9. This kind of junction is also called homo-junction because the intrinsic material used for both n- and p-type materials is same. The magnitude of the built-in potential V_{bi} (V) can be estimated using Equation (2.2) [3];

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{2.2}$$

Where;

q is the elementary charge (1.6×10^{-19} C)

N_a is the density of acceptor impurity atoms (cm^{-3}) in the p-type material

N_d is the density of donor impurity atoms (cm^{-3}) in the n-type material

n_i is the intrinsic concentration of electrons (cm^{-3})

The width of the depletion region W (cm) can be calculated using Equation 2.3 [3];

$$W = \left[\frac{2\varepsilon_s V_{bi}}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{\frac{1}{2}} \tag{2.3}$$

Where;

ε_s is the permittivity of semiconductor (Fcm^{-1})

For the abrupt p^+-n junction where $N_a >> N_d$, the width of depletion region can be simplified into Equation 2.4;

$$W = \left[\frac{2\varepsilon_s V_{bi}}{qN_d}\right]^{\frac{1}{2}} \tag{2.4}$$

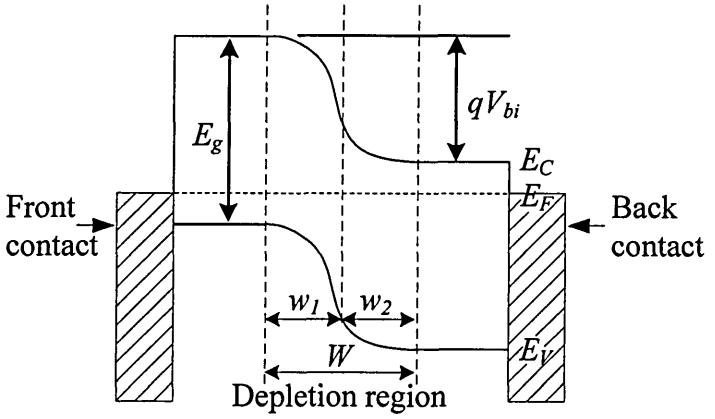


Figure 2.10: The band diagram of a p-n junction. The band bending represents the depletion region.

Figure 2.11 shows the role of efficient p-n junction in a solar cell. In an ideal scenario, p-n junction will absorb photons, create EHPs, separate charge carriers and transport these mobile charge carries to the external circuit to create useful current before they recombine. If the p-n junction is too narrow, recombination will easily happen because electrons can tunnel through the junction and if it is too wide, the strong electric field is absent, thus making the separation of EHPs becomes poor.

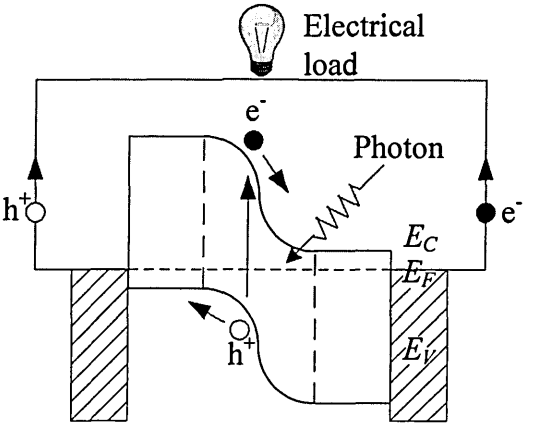


Figure 2.11: Schematic diagram showing the creation and transport of EHPs to the external circuit by a p-n junction within a solar cell.

2.3.2 p-i-n junction

In p-i-n junctions, an intrinsic (i-type) semiconductor is sandwiched between two semiconducting layers as shown in Figure 2.12. This arrangement aligns the Fermi level of two semiconductors through the i-type material. The i-type material in the middle is responsible in creating a strong electric field for the device. It is important to note that in practical, it is very difficult to produce pure i-type semiconductor. The band diagram shown in Figure 2.12 is for pupose of discussion.

The major advantage of p-i-n structure is the possibility of getting high open circuit voltage, V_{oc} due to the presence of high potential barrier (φ_b) that is comparable with the band gap of the p-type materials ($\varphi_b \approx E_g$). Amorphous silicon solar cell, and CdTe solar cell using p-ZnTe, i-CdTe and n-CdS are two examples of solar cells fabricated using this p-i-n structure [4-6].

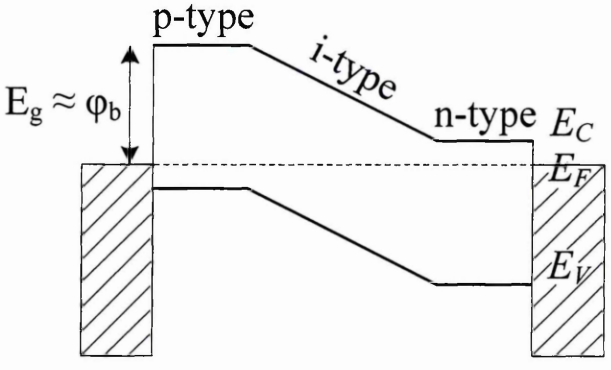


Figure 2.12: p-i-n structure showing the possibility of fabricating solar cells with high potential barrier, ($\varphi_b \approx E_g$).

2.2.3 Hetero-junction

Hetero-junction is a simple modification of p-n junction. In hetero-junction interface, two different materials with different energy bandgaps are joined together to form the junction. It is different from homo-junctions because in homo- junction devices, the p-type and n-type materials originate from the same intrinsic material. Figure 2.13 shows the formation of hetero-junction with n-type material on the left while the p-type material on the right. Notice that because of two different semiconductors used, the device has two different bandgaps. During the absorption of photons, the material with wider bandgap (E_{gl}) will absorb high energy photons thus

creating EHPs. The low energy photons will be transmitted to be absorbed by the second layer (E_{g2}). This is a selected step photons absorption and beneficial in minimizing thermalisation in solar cells.

Hetero-junction provides a huge advantage in thin films solar cells fabrication mainly in the aspect of doping. As mentioned before, silicon solar cell is a homo-junction device and controlling the suitable level of doping is a very challenging task and requires expensive equipments. In contrast, fabrication of thin film solar cells is simpler because certain semiconductor such as CdS is normally an n-type material. If p-type CdTe is grown on CdS, then the hetero-junction is formed and one will have a working solar cell [7-9].

One of the weaknesses of hetero-junction is it has narrow band bending. This leads to easier recombination of EHPs, thus contributing to low short circuit current. Since this interface requires one semiconductor to be grown on top of other semiconductor, detrimental surface states or defects due to the lattice mismatch between the two materials is possible. This will lead to detrimental performance of the solar cells.

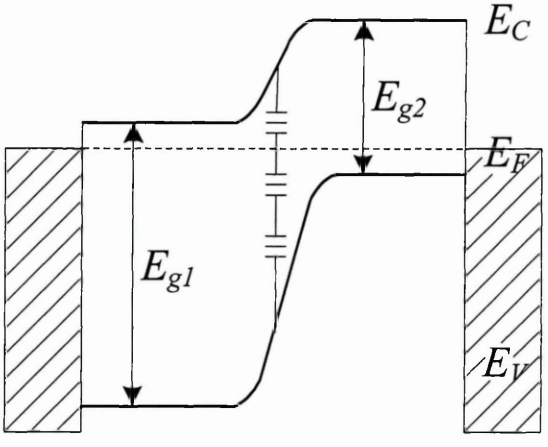
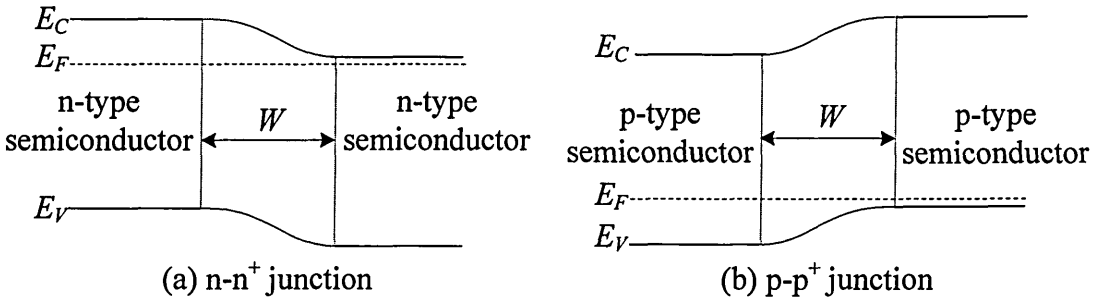


Figure 2.13: Hetero-junction energy band diagram showing surface states at the interface.

2.3.4 Graded bandgap multilayer devices

The built-in electric field can also be created using only one type of semiconductor [10-11]. These interfaces are known as n-n^+ or p-p^+ junction interface as shown in Figure 2.14. The electric field created from these individual structures is low

compared to p-n junction. However, if connected in parallel with many layers, a strong built-in electric field can be produced. Solar cell device created with semiconductor with variable material compositions are known as graded bandgap multi-layer solar cells.



(a) n-n^+ junction (b) p-p^+ junction

Figure 2.14: The junction interfaces created from (a) n-n^+ and (b) p-p^+ junction. Note the presence of low potential barriers and hence weak electric fields.

Figure 2.15 shows the band diagram of multi-layer graded bandgap solar cells (MGBSCs) [12]. MGBSCs can be fabricated by starting from the p-type or n-type window materials. If fabrication starts from the p-type material, the electrical conductivity of the solar cell will gradually change from p^+-p-i-n-n^+ as shown in Figure 2.15 (a) while Figure 2.15 (b) shows the n^+-n-i-p-p^+ structure if the starting material is n-type. Both devices share similarity by having the widest bandgap layers to face the sunlight. These devices are so designed such that the high energy photons will be absorbed first. The low energy photons will be absorbed by the narrow bandgap layers later. In simple words, these photovoltaic cells are capable of absorbing photons from ultra-violet, visible and infra-red region and at the same time minimizing the thermalisation effects.

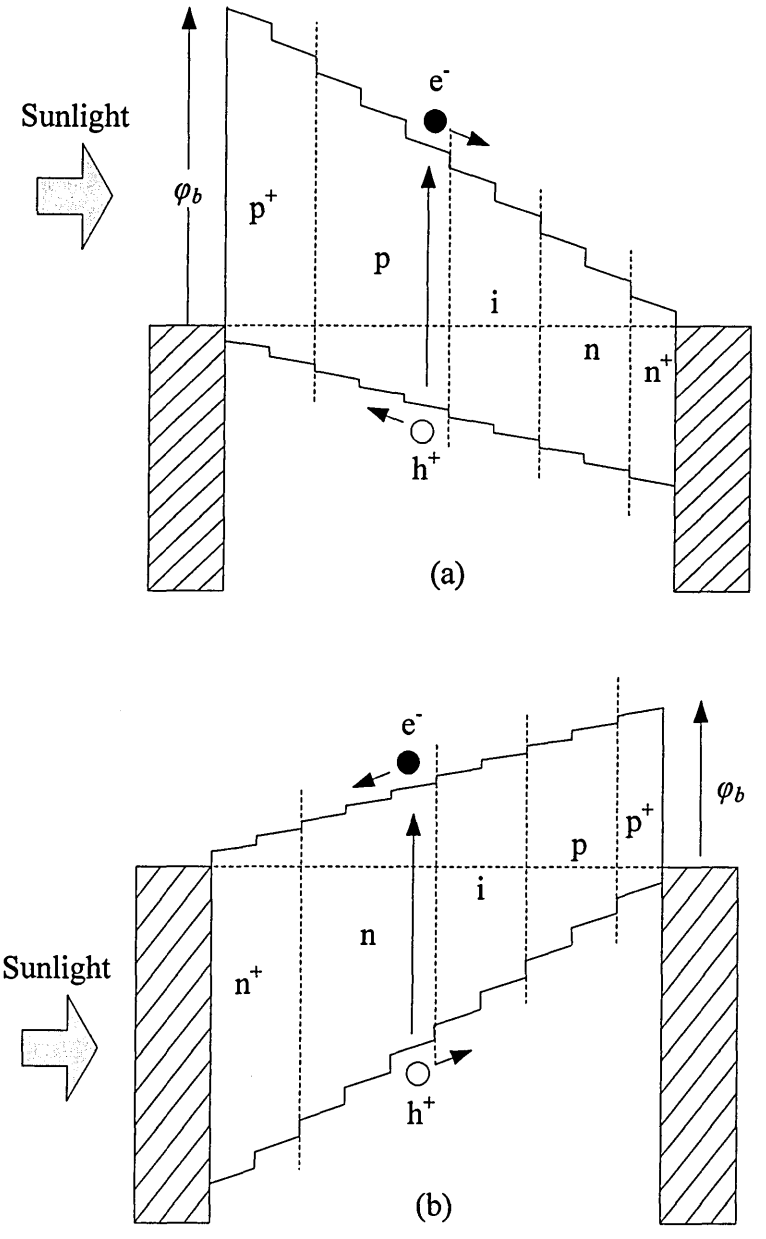


Figure 2.15: The band diagram of multi-layer graded bandgap solar cell with (a) p^+-p-i-n-n^+ and (b) n^+-n-i-p-p^+ structure [12].

Both structures are fully depleted devices because the built-in electric field expands through the entire structure from the first layer up to the last layer. This is also an added advantage because the presence of strong electric field will help in minimizing recombination of electrons and holes thus increasing the short circuit current density, J_{sc}. By comparing both solar cells, it is obvious that fabrication of p^+-p-i-n-n^+ structure is preferable because of the higher potential barrier thus producing higher open circuit voltage, V_{oc} compared to n^+-n-i-p-p^+ structure.

In addition to absorption of all photons from ultra-violet, visible and infra-red region, the device structures can create additional charge carriers incorporating impurity photovoltaic effect and impact ionisation. Since the impurity photovoltaic effect is built into these devices, they can absorb heat energy from the surroundings [13,14].

2.3.5 Metal-semiconductor (or Schottky) contact

Schottky contact is formed when metal is brought into intimate contact with semiconductor. Figure 2.16 (a) shows the formation of a Schottky barrier device between n-type semiconductor and metal contact. Due to the lower work function of the semiconductor (φ_s) against the work function of the metal (φ_m), electrons will flow from semiconductor to the metal. The flow of electrons to the metal will leave positively charged donor atoms in the semiconductor. Negatively charged electrons now accumulate at the metal's surface. When negatively and positively charged layers, sit close to each other, the electric field built-up at the interface as shown in Figure 2.6 (b). When thermal equilibrium is achieved, the potential barrier, φ_b is formed. The formation of φ_b is given by;

$$\varphi_b = \varphi_m - \chi \tag{2.5}$$

Where χ is the electron affinity of the semiconducting material.

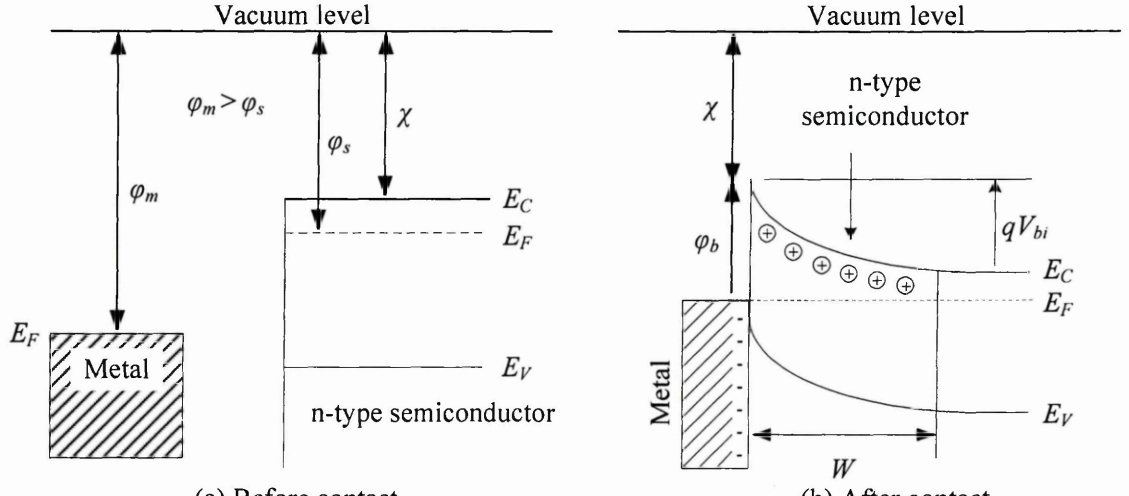


Figure 2.16: The energy band diagram showing the formation of potential barrier at metal/n-type semiconductor interface.

The potential barrier formed as shown in Figure 2.16 is achieved when the moderate doping of 10^{15} - 10^{17} cm^{-3} is fullfilled. When the width of depletion region (W) is considerable and the potential barrier is equal or larger than 0.4 eV, the rectifying electrical properties of the device is given by the Equation (2.6) [3];

$$J_D = A^*T^2 e^{\left(\frac{-q\phi_b}{kT}\right)} \cdot \left[e^{\left(\frac{qV}{nkT}\right)} - 1\right] \tag{2.6}$$

Where,

J_D is the dark current density (Acm^{-2})

A^* is the effective Richardson constant for thermionic emission ($Acm^{-2}K^{-2}$)

n is the deality factor of the diode

V is the external applied voltage (V)

2.3.6 Metal-insulator-semiconductor (MIS) contact

The potential barrier, φ_b at the metal-semiconductor (MS) contact is generally lower than the potential barrier of p-n junction devices as shown in Figure 2.17. It means that by having low potential barrier, the open circuit voltage, V_{oc} of the MS devices is also less than the V_{oc} obtained from p-n junction solar cells. To obtain higher φ_b (and higher V_{oc}), a very thin layer can be incorporated into MS solar cells as shown in Figure 2.18.

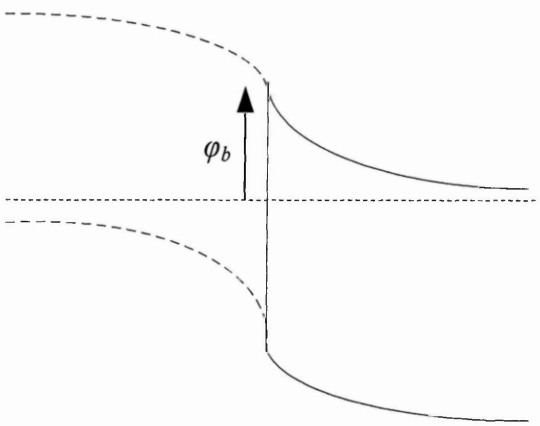


Figure 2.17: Band diagram showing the potential barrier, φ_b of MS devices is half of the p-n junction devices.

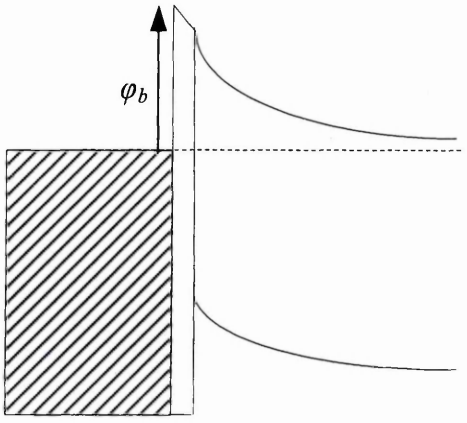


Figure 2.18: Incorporating insulating layer between metal and semiconductor to increase the potential barrier.

If organic material such as polyaniline (PANi) is used, the positive effects are twofold [15]. Not only the V_{oc} increases, but at the same time it minimizes the interaction between metal and semiconductor due to the in and out diffusion of semiconductor and metal elements and improve the stability and lifetime of photovoltaic devices. The inclusion of insulating materials will slightly change Equation (2.6). The symbols χ_i (in eV) and δ (in Å) are the mean barrier height and the thickness of the insulating layer respectively [16].

$$J_D = A^*T^2 e^{(-\chi_i^{0.5}\delta)} e^{\left(\frac{-\phi_b}{kT}\right)} \cdot \left[e^{\left(\frac{qV}{nkT}\right)}\right] \tag{2.7}$$

2.4 Photovoltaic action

The photon energy, E_p (in Joule, J) is defined as;

$$E_p = \frac{hc}{\lambda} \tag{2.8}$$

Where;

h is the Planck's constant (6.63×10^{-34} Js)

c is the speed of light (3×10^8 ms^{-1})

λ is the wavelength of the photon (m)

Conventionally, energy of a photon is written in electron-volt (eV) unit where 1 J is equivalent to 6.25×10^{18} eV. By solving equation (2.9);

$$E_p = \frac{(6.63 \times 10^{-34})(3 \times 10^8)}{\lambda}$$

$$= \frac{1.989 \times 10^{-25}}{\lambda} \tag{2.9}$$

Equation 2.9 has to be multiplied with 6.25×10^{18} eV to convert the energy unit into electron volt. Equation 2.9 becomes Equation 2.10 where;

$$E_p = \frac{1.24 \times 10^{-6}}{\lambda} \tag{2.10}$$

Equation 2.10 can be simplified into Equation 2.11 where λ is expressed in μm.

$$E_p = \frac{1.24}{\lambda} \tag{2.11}$$

For a single photon to generate EHP, the energy carried by the photon must be equal or higher than the bandgap of the solar cell. When a solar cell is exposed to light, it will absorb photons. Photons will interact with the valence electrons by transferring their energy to the valence electrons. If sufficient energy has been transferred to the valence electrons, these electrons can break from their host atoms and get excited to the conduction band. Conduction band at the minimum level is now filled with electrons while holes are left in the valence band. If the incoming photons have energy higher than the bandgap of semiconductor, only a portion of the energy will be used to excite the valence electrons while the remaining energy will be lost as heat. If the photons energy is less than the bandgap, it will pass through the semiconductor without absorption and creating any mobile charge carrier.

The efficiency of EHPs created also depends on the bandgap properties. Generally, bandgap of semiconductors are classified into direct and indirect bandgap. Examples of indirect and direct bandgap semiconductors are silicon and gallium arsenide, respectively. Figure 2.19 shows the energy band diagram for direct and indirect semiconductors. The vertical axis represents energy while the horizontal axis

represents momentum of electrons. Notice that for indirect bandgap semiconductor, the bottom of the conduction band is displaced from the peak of the valence band. In the case of direct bandgap semiconductor, the bottom of the conduction band is aligned with the peak of the valence band.

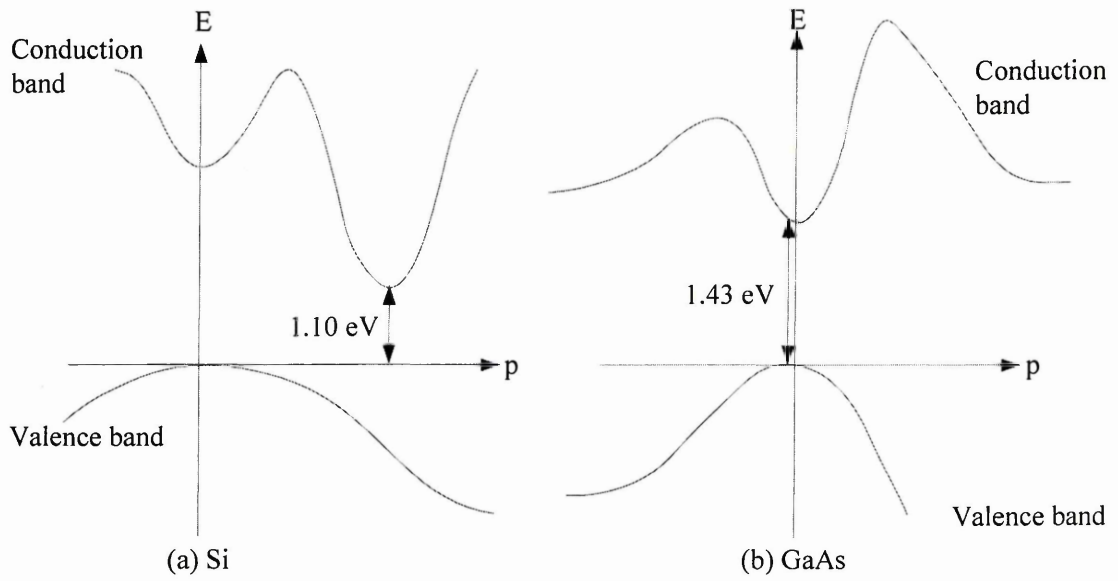


Figure 2.19: Energy-momentum diagram for (a) indirect (Si) and (b) direct bandgap materials (GaAs). Redrawn from [17,18]

Indirect bandgap solar cell (Si) is less efficient compared to direct bandgap semiconductors in terms of creating EHPs even though the bandgap is smaller than the direct bandgap semiconductor (GaAs). To explain this mechanism, consider de Broglie's equation (Equation 2.12), where p ($kgms^{-1}$) is the momentum of a particle [3].

$$\lambda = \frac{h}{p} \tag{2.12}$$

From Equation (2.8) we know that high energy photons will constitute in shorter wavelengths. However, according to Equation (2.12), short wavelength will constitute in higher momentum of a photon. This means, high energy photons will carry higher momentum compared to the low energy photons.

Now if we consider absorption of a photon with energy of 1.1 eV by silicon solar cell, the photo-generated electron must overcome the displacement at the momentum axis in order to enter the conduction band. Since this photon carries little momentum, the displacement along the momentum axis is very unlikely.Therefore in Si,

the probability of excitation of an electron from valence band to the conduction band is high if the energy of the photons is greater than the bandgap because high energy photons also carry larger momentum.

For the low energy photons, to preserve the momentum along the horizontal axis, the excitation of an electron from the valence band to the conduction must be assisted by emission or absorption of phonons. Phonon is a unit of vibrational energy originated from the oscillation of atoms in the semiconductor's lattice. The vibration of lattice can be caused by thermal energy or outside forces. Figure 2.20 shows the excitation of an electron in indirect semiconductor.

When one electron absorbs photon, it will be excited vertically along the energy axis to a definite level within the bandgap. At this point, with the help of phonon emission or absorption, the excited electron can be moved to the conduction band minimum. It is important to note that a phonon carries smaller energy than a photon. But its momentum is larger than a photon because the momentum of a phonon is defined as ($p = h \div a$) where h is the planck constant and a is th lattice paremeter and normally in the range of 2-5 Å.

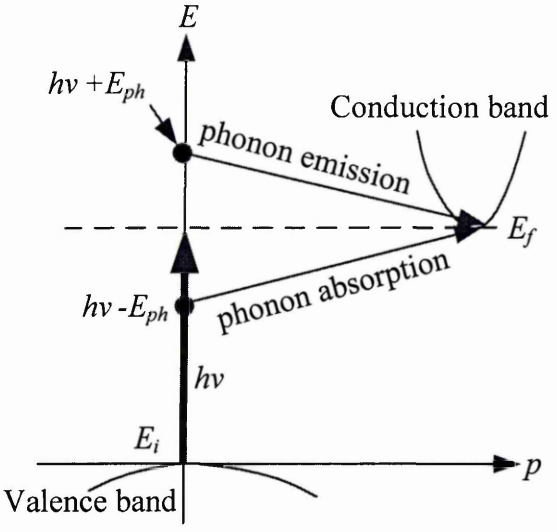


Figure 2.20: The excitation of an electron from valence band to the conduction band in indirect semiconductor with the assist from photon absorption or emission.

For the direct bandgap semiconductor (GaAs), a photon with energy of 1.45 eV will enter the conduction band easier than Si solar cell since the displacement between the top of the valence band and the bottom of the conduction band is absent.

Another important aspect that should be considered when designing solar cells is the absorption coefficient, α (cm^{-1}). Semiconductors with high absorption coefficient require less material to fabricate and simultaneously reducing the cost of solar cell fabrication. This means the thickness of the solar cell can be reduced to the tenth of micro metres. The relationship between thickness, x (cm) and the absorption coefficient is provided by Equation (2.13) [19];

$$x = \frac{\ln\left(\frac{I_o}{I}\right)}{\alpha} \tag{2.13}$$

Where;

I_o is the intensity of light at the surface (Wcm^{-2})

I is the intensity of light at depth x (Wcm^{-2})

2.4.1 Role of defects and impurities in carrier generation and recombination

Defects are typically present within any semiconductor material regardless the growth technique used. This means that the presence of defects is inevitable even in the semiconductors that have been grown using high temperature techniques such as Bridgemann, Czochralski or float-zone. In semiconductor, defects are defined as anything that alters the ideal crystal structure of semiconductor. Defects can exist as point defects, line defects, planar defects, etc [20]. However, deep discussions about the type of defects, their characteristics, etc. are outside the scope of this thesis. This subsection will present the discussion about the role of defects and impurities in carrier (electron-hole pair) generation and recombination.

Figure 2.21(a) and 2.21(b) shows the band diagram of n-CdS/n-CdTe solar cells. As reported by Dharmadasa in 1998 [19], there are five main defects level located at the n-CdTe and metal back contacts interface. These defects levels are named as E_1 to E_5. The high subscript numbers such as E_4 and E_5 indicate the position of defect levels close to the valence band. While the low subscript numbers from E_1 and E_2 indicate the position of defect levels close to the conduction band. Lastly, E_3 is the defect level located at the middle of the bandgap.

In the case of Figure 2.21(a), when the high concentration of defects is located at E_5, the Fermi level will be pinned at this location when metal contacts are deposited on

top of n-CdTe. As a result, high Schottky barrier is formed. High Schottky is favourable because it creates large electric field (or band bending) which is responsible for the transport of mobile charge carriers to the external circuit. Due to the large band bending, the electrons can be accelerated towards the external circuit with high speed thus minimizing recombination of electrons and holes.

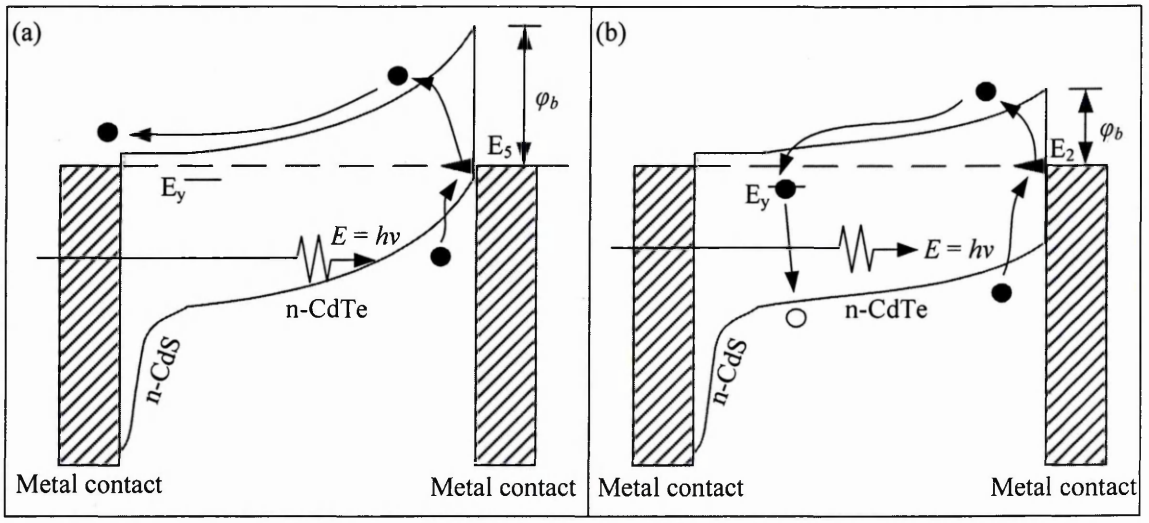


Figure 2.21: (a) If strong electric field is present, electrons will move to the external circuit at high speed hence minimizing the recombination with holes. (b) If weak electric field is present, the electrons will move to the external circuit with low speed thus easily recombine with holes.

In the case of Figure 2.21(b), the magnitude of electric field created is small due to the weak band bending. As a result, the acceleration of electrons to the external circuit is slow thus increasing the probability of electrons to recombine with holes inside the material. The situation could be worst if there are existences of defects level (E_y) within the bandgap. This defect (E_y) can act as the electrons trap and assist the recombination of electrons and electrons. Low speed electrons can be trapped easily by this defect level. High recombination rate of electron and holes will reduce the number of mobile charge carriers transported to the external circuit. As a result, magnitude of current detected in the external circuit is low hence reducing the conversion efficiency.

It is important to note that in both cases, defect levels can be exploited in the creation of mobile charge carriers utilizing low energy photons. This mechanism is also known as impurity photovoltaic effect. In the first step, low energy photons ($E \leq 1.45$ eV) can promote the electrons from valence band to the defect levels (E_2 or E_5). In the

second step, again the low energy photons ($E \leq 1.45$ eV) can excite the electrons to the conduction band. The utilization of thermal energy (from the infra-red region) is possible since the low energy photons can also excite electrons to the conduction band.

However, the key to effective utilization of these defects lies in the creation of the electric field. If strong electric is present, the defects in the semiconductor can affect the solar cell devices positively.

2.5 Summary

This chapter started with the introduction of solid materials. Generally, solid materials are divided into three groups. They are conductors, insulators and semiconductors. Solid materials are assigned to their corresponding groups according to their bandgaps and electrical properties.

The introduction to the energy band diagram of solid and the concept of electron-hole pairs is also presented in this chapter. For the next chapters, the band diagram will be used repetitively in order to explain the photovoltaic properties of solar cells.

Materials for solar cells application are semiconductors and classified as n-, i- and p-type materials. These materials are useful in fabricating photo-active layers called the depletion region. Depletion region can be produced by combining n-n, p-p, n-p and p-i-n materials. Depletion region can also be produced by intimate contacting between semiconductor and metal layers.

Direct and indirect bandgap properties of semiconducting layers are also important in determining the suitable thickness for solar cells fabrication. Direct bandgap semiconductors with high absorption coefficient usually require less material in solar cells fabrication compared to the indirect bandgap semiconductors. As for indirect semiconductors, due to the low probability, electrons in these materials require phonons to assist in the creation of e-h pairs.

Defects are phenomena that naturally occur in any semiconductor regardless of the growth technique. Even though defects can negatively affect solar cells performance by assisting the recombination process, they can also be exploited to enhance the creation of e-h pairs within the device, provided that strong and effective electric field is present.

2.6 References

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3.1 A brief history of photovoltaic research and development

Photovoltaic effect was discovered by French physicist Edmund Becquerel in 1839. However, due to the availability of cheap fossil fuels in the early 1900s, photovoltaic technology was not significantly developed. The research and development of photovoltaic devices was given serious attention in the early 1970s. The 'driving force' behind the rapid development of photovoltaic technologies was due to the oil crisis during that time.

Figure 3.1 shows the evolution of photovoltaic technologies. This figure was originally published by University of New South Wales [1]. Figure 3.1 shows that photovoltaic technologies can be divided into 3 generations. The first generation is the high cost-high efficiency solar cells. Silicon and gallium arsenide (GaAs) solar cells are associated with the first generation solar cells. These materials are the most researched semiconductors in last four decades. Both monocrytalline silicon and GaAs solar cells have achieved efficiency beyond 24% for lab scale devices [2]. Even though devices based on these two materials carry high efficiencies, both materials are expensive to produce. The US dollar per watt ratio ($/W) for the first generation solar cells is equal or higher than 1.00 $/W.

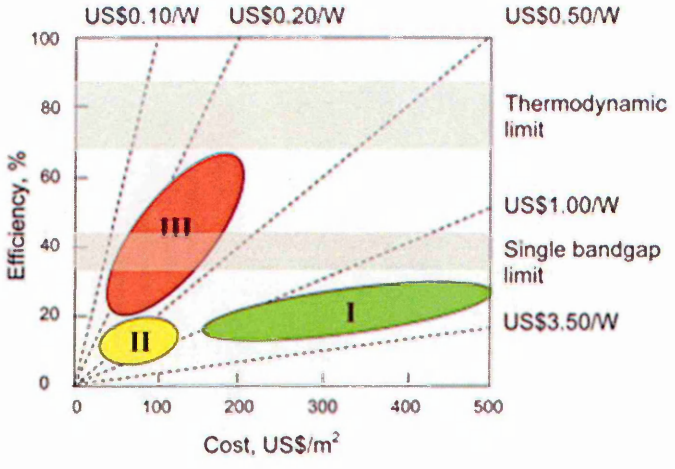

Figure 3.1: Classification of generations in photovoltaic technologies. Classifications are made based on the cost-output power ratio measured in US dollars per watt ($/Watt) [1].

Thin film solar cells such as cadmium telluride (CdTe) and copper indium gallium diselenide (CIGS) belong to the second generation. Second generation is the low cost-low efficiency solar cells. Thin film photovoltaic technologies emphasize on using fewer materials for solar cells fabrication and at the same time trying to cut down the cost of manufacturing solar panels by utilizing high throughput manufacturing technologies. However, the main drawback of using thin layers (less than 2 μm thick) is the lower efficiency of the cells. The US dollar per watt ratio for second generation solar cells is between 0.20 $/W to 1.00 $/W.

Finally, third generation solar cells are the low cost-high efficiency solar cells. Third generation solar panels might be coming from thin film devices that can reach conversion efficiency beyond 22% or from the first generation cells where the production cost has been reduced drastically perhaps due to the economy of scale or the transfer of solar panels manufacturing activities to the countries where the production cost is lower.

3.2 Types of solar cells

Nowadays, there are many types of solar cells that are being studied. Solar cells today have been fabricated using inorganic and organic materials. Whatever the materials used, the principle operation of solar cells is still the same. Which means, every solar cell regardless the materials used, must be able to effectively absorb light, produce electron-hole pairs, separate charge carries efficiently and then transport the electrons to the external circuit before recombination takes place.

3.2.1 Silicon solar cells

The first silicon solar cell was reported by Russell Ohl from Bell Laboratories in 1941, but the efficiency was less than 1% [3]. Significant breakthrough came in 1954 when the conversion efficiency reached up to 6% [4]. This achievement was mainly came from the substitution of lithium with boron as the p-type dopant. The efficiency exceeding 10% was soon reached in 1955 [4].

In 1962, Mandelkorn *et al* have reported the new conversion efficiency of 15% [5]. The solar cell devices were fabricated using phosphorous doped substrate and this was the main reason behind the significant breakthrough. In 1974, textured surface

solar cell was introduced by Haynos and co-workers. The pyramidal features on the surface of the solar cell (Figure 3.2) can be obtained by anisotropic etching [6]. These pyramidal features are useful to enhance the absorption of photons by deflecting light from the side of the pyramids downward as shown in Figure 3.3. In 1976, the efficiency of the textured surface solar cell had reached 17% [3].

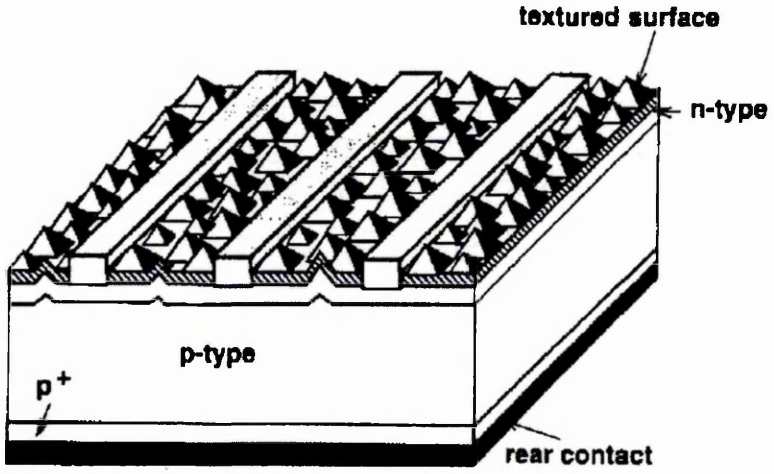

Figure 3.2: Pyramidal surface solar cell obtained by chemical etching [3].

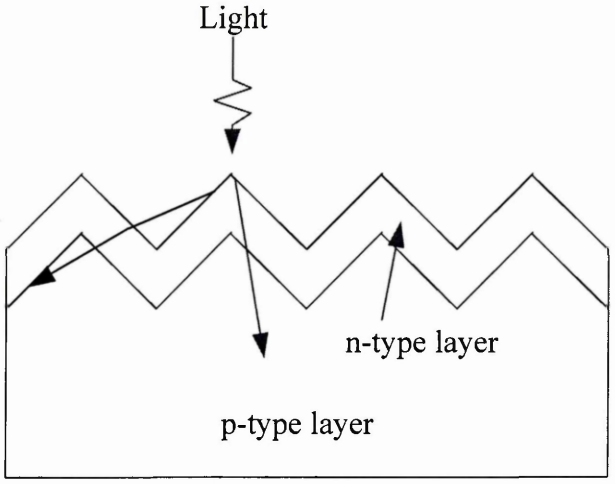

Figure 3.3: Pyramidal surface helps to deflect light downward.

The new efficiency record was attained in 1984 when a group of researchers from University of New South Wales (UNSW), Australia reported the conversion efficiency of 19.1% [7]. The solar cell structure fabricated is known as passivated emitter solar cell (PESC). PESC was derived from the metal-insulator-semiconductor (MIS) type front blocking contact. Further improvement towards the doping

concentration at the front and the back of the cell further improved the efficiency up to 20.6% in 1986 [3]. The cross section of PESC is shown in Figure 3.4.

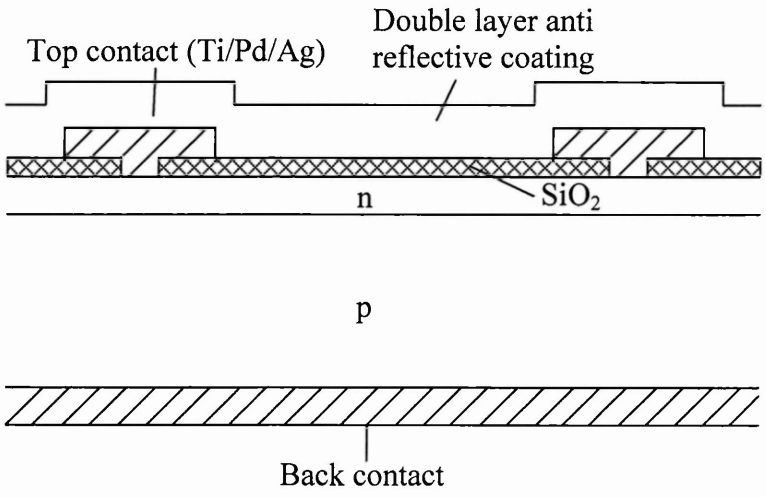

Figure 3.4: Passivated emitter solar cell (PESC) structure. Redrawn from [7].

Point contact solar cells were introduced by a group of researchers from Stanford University. This new design was emphasized upon minimizing surface recombination at the back of the solar cells. The solar cells' efficiency of 22.3% was reported in 1988 [8]. This record, however, was overtaken by UNSW after one year. In 1989, with the knowledge learnt from the point contact solar cells, a research group from UNSW, improved the design of their passivated emitter solar cells. This new design is known as passivated emitter locally diffussed (PERL) [4] cells and is shown in Figure 3.5. The role of the inverted pyramids at the front of the cell is to improve the rear reflectance. This solar cell device has recorded the efficiency of 24.7% in 1999 [9].

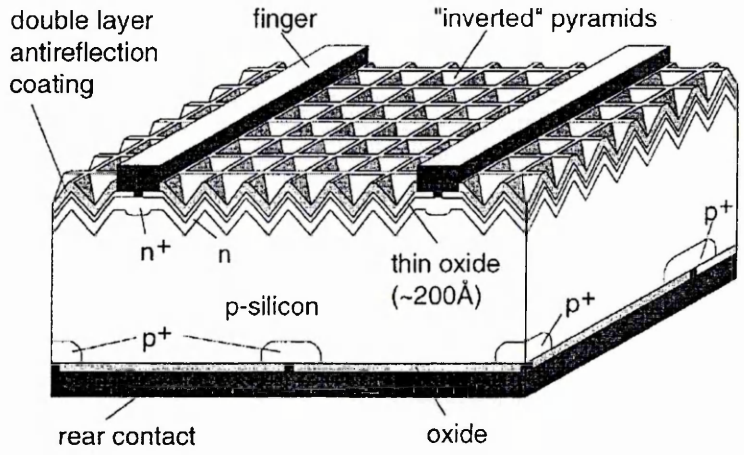

Figure 3.5: Passivated emitter rear diffused (PERL) solar cell structure [9].

Silicon solar panels are the most dominant product in terms of the market share in photovoltaic industry. Figure 3.6 shows the bar chart of shipment of solar panels in 2013 from fifteen largest solar panel suppliers in the world [10]. All the solar panel suppliers shown in Figure 3.6 are suppliers of silicon solar panels except for First Solar and Solar Frontier. First Solar and Solar Frontier produce CdTe and CIGS solar panels respectively.

From the bar chart, these thirteen silicon solar panel suppliers had shipped panels with capacity nearly 21.4 GW in 2013. This number represents 89.5% of the overall market share (~22.9 GW).

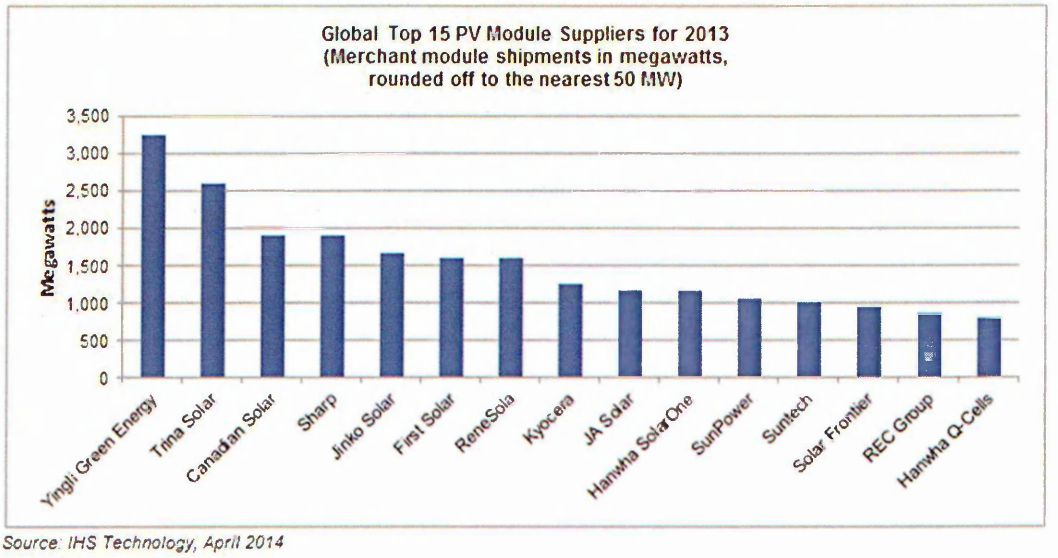

Figure 3.6: Shipment of solar panels throughout the world in 2013 from fifteen largest solar panels suppliers in the world [10].

There are 3 types of silicon solar cells that have been commercialised. The lists are as follows:

(a) Monocrystalline silicon

Raw material for silicon solar cells comes from sand (SiO_2). The process of making monocrystalline solar panels is shown in Figure 3.7. The process starts with the reduction of SiO_2 to Si using carbon. This process is called coke reduction where SiO_2 is reacted with carbon by heating at the temperature of 1500°C to 2000°C. The chemical reaction of coke reduction is shown in Equation (3.1) [11].

$$SiO_2 + C \rightarrow Si + CO_2 \quad (3.1)$$

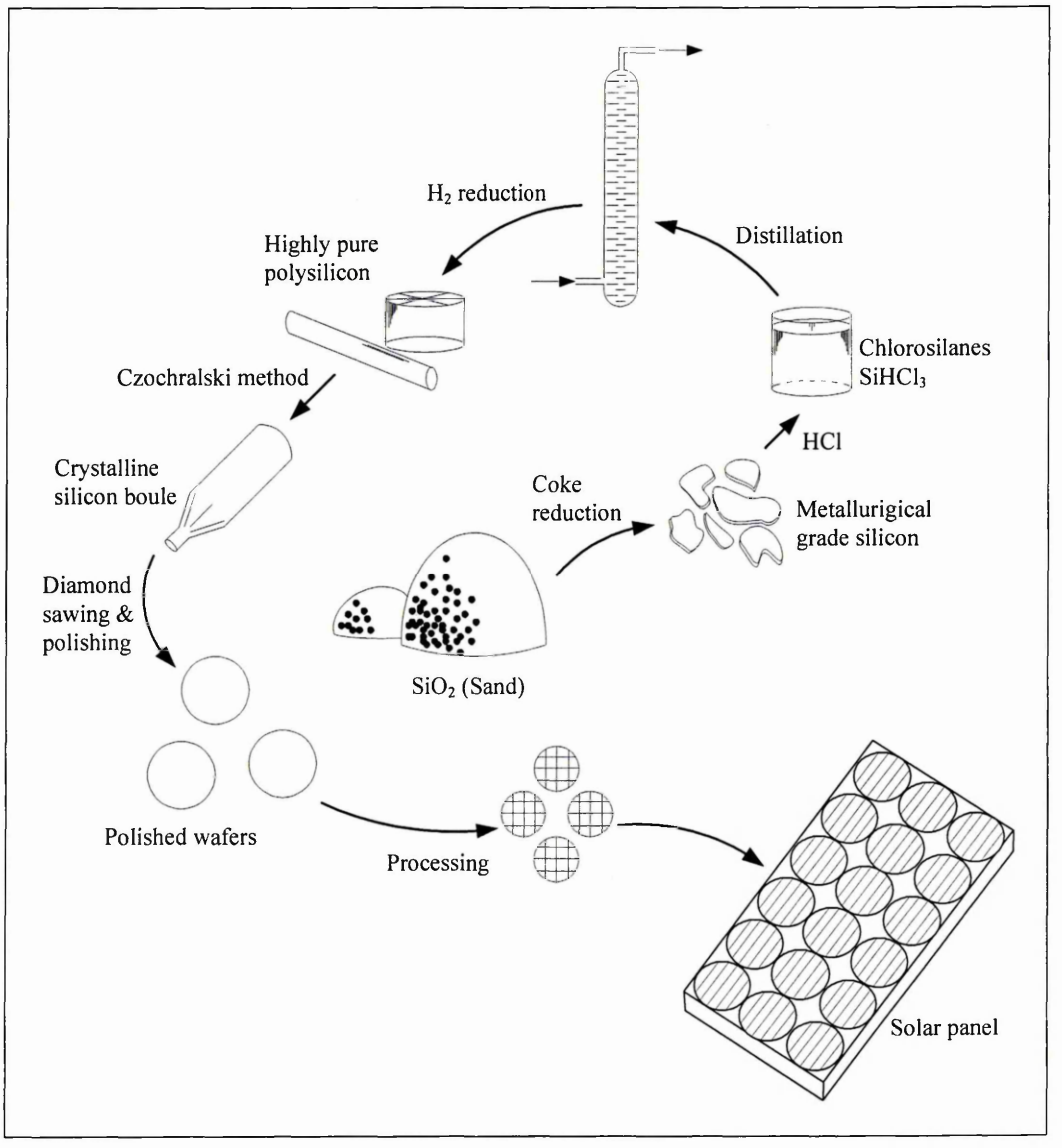

Figure 3.7: The process of making monocrystalline solar panels starting from raw materials. Redrawn from [12].

After this process, metallurgical grade silicon (MGS) with 99% purity is produced [13]. In the next step, the MGS is reacted with HCl to form trichlorosilane. The reaction mechanism is shown in Equation (3.2) [14].

$$Si + 3HCl \rightarrow SiHCl_3 + H_2 \quad (3.2)$$

Trichlorosilane is a colourless liquid and has boiling temperature of 31.8°C. Trichlorosilane is then distilled to remove the remaining impurities such as $FeCl_3$, $AlCl_3$, and BCl_3. Trichlorosilane is heated in hydrogen environment between 200 and 300 hours at 1100°C [14]. This process will reduce the hydrogen from trichlorosilane and produce high purity polysilicon with 99.99999% purity [13];

$$SiHCl_3 + H_2 \rightarrow Si + 3HCl \tag{3.3}$$

Silicon boule shown in Figure 3.7 is produced by Czochralski method. The polysilicon is melted at high temperature (~1400°C) inside a crucible. Then, seed crystal is dipped into molten silicon. After that the seed crystal is pulled slowly upward while rotating simultaneously as shown in Figure 3.8. The silicon boule will solidify during the pulling process. The temperature gradient, pulling rate and rotation speed influence the size of the single crystal. To produce p-type silicon wafers, the p-type dopant (boron, B) is introduced during the crystal growth. Normally, the length of the silicon boule is about 1 m with the diameter of 10-15 cm [15]. Using diamond saw, the silicon boule will be sliced into 160 to 200 μm thick silicon wafers [16].

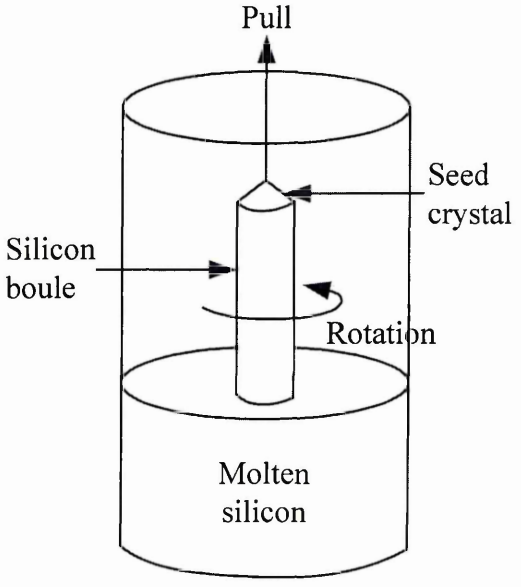

Figure 3.8: Czochralski method. The seed crystal is dipped into molten polysilicon and then pulled upwards while rotating to produce silicon boule. Redrawn from [16].

The p-n junction will be formed when the p-type silicon wafers are heated in the n-type dopant environment. This process makes n-type dopant (phosphorous, P) diffuses into the top surface of the p-type wafers and leads to the creation of p-n junction. To complete the solar cells, two metal contacts need to be made at the front and back of the cells.

(b) Multicrystalline silicon

Monocrystalline solar panels are expensive due to the requirement of high temperature to melt the silicon. In addition to that, producing silicon boules from Czochralski method is a time consuming process. The circular shape of monocrystalline wafers is not economic for making solar panels. This is because the circular shape will leave lots of empty spaces between the wafers. This problem can be solved by cutting the silicon boules into squares. However, this process will result in more waste in terms of materials, money and time.

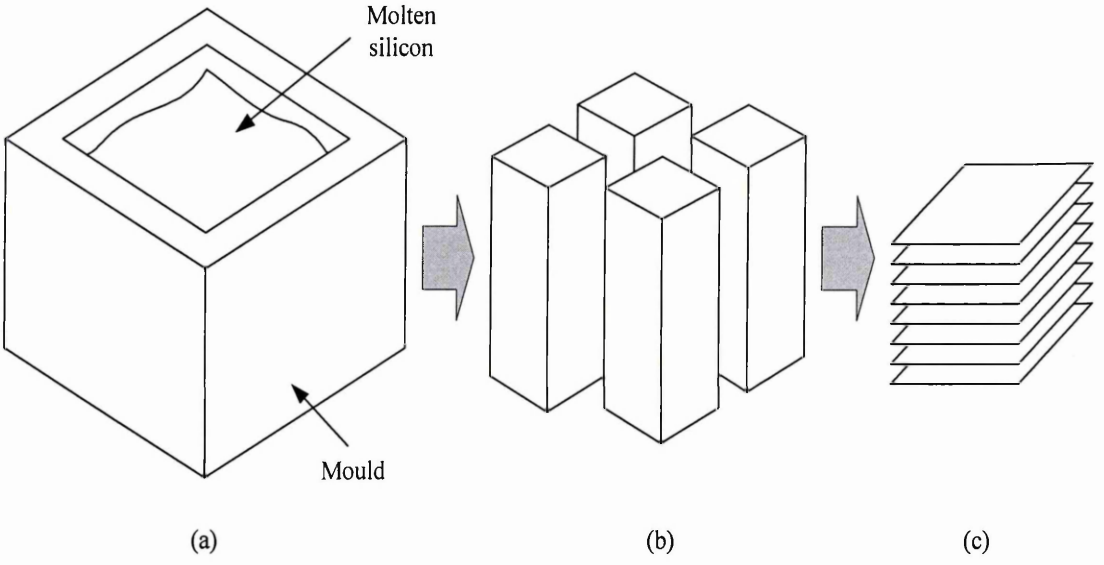

Figure 3.9: The production of multicrystalline silicon wafers. (a) Polysilicon feedstock is melted inside a mould. (b) After the molten silicon solidifies, it is divided into ingots. (c) The ingots are then sliced into wafers. Redrawn from [15].

If the Czochralski method is skipped, the production cost can be lowered. Skipping Czochralski method will result in producing multicrystalline silicon. Figure 3.9 shows the production process of multicrystalline silicon.

The process starts with the melting of polysilicon inside moulds. When the molten silicon solidifies, it is cut into ingots and finally sliced into wafers. The process is simpler and faster compared to monocrystalline process. The efficiency of multicrystalline solar cells is usually lower than monocrystalline solar cells. These are due to the imperfection of the crystal structure and also the existence of grain boundaries. The presence of impurities in the mould could also be the contributing factor for the low efficiency. Multicrystalline silicon solar cell has the highest efficiency of 20.4% to date [17].

(c) Amorphous silicon (a-Si)

Silicon can also exist in the amorphous form. Dangling bonds could present in amorphous silicon due to the imperfections of the crystal structure. In solar cell, dangling bonds are defect that responsible of trapping electrons. As a result, amorphous silicon solar cells will suffer from low short circuit current density. To passivate the 'trapping' behaviour of dangling bonds, hydrogen atoms can be added to the crystal structure as shown in Figure 3.10. The process is known as hydrogenation or hydrogen passivation. In literature, hydrogenated amorphous silicon is written as (a-Si:H).

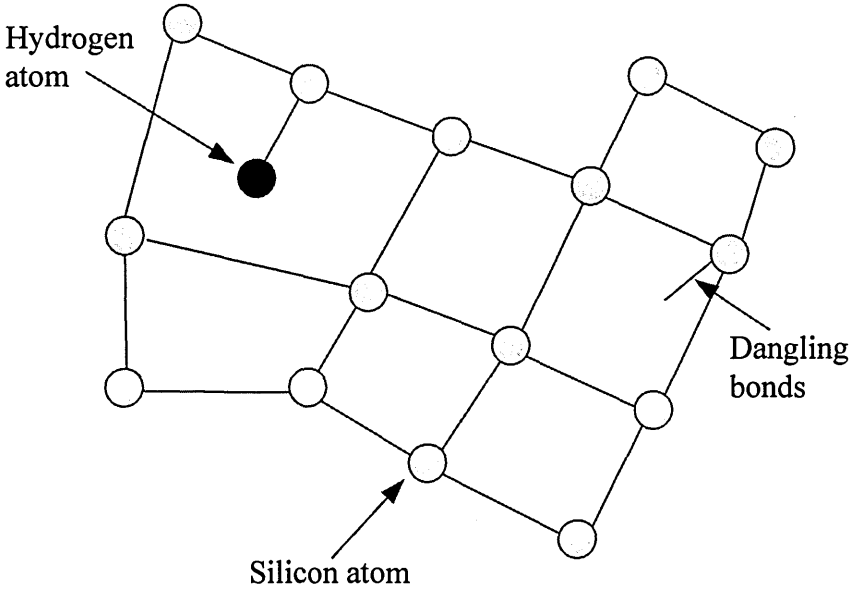

Figure 3.10: Passivating dangling bonds through the addition of hydrogen atoms in amorphous silicon. Redrawn from [18].

However, the addition of hydrogen atoms to the lattice makes the efficiency of amorphous silicon solar cell deteriorates gradually when exposed to light [19]. To improve the stability, the p-i-n junction device is designed. The schematic drawing of p-i-n device is shown in Figure 3.11.

In this design, the intrinsic semiconductor layer (i-layer) is sandwiched between the p-type semiconductor and n-type semiconductor. Electron-hole pairs (ehp) are generated at the i-layer where the strong electric field is present.

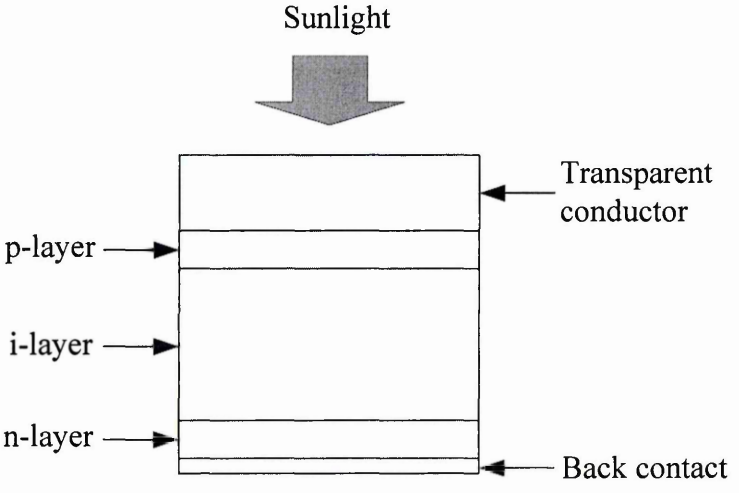

Figure 3.11: Schematic diagram of amorphous silicon solar cell with a p-i-n junction.

P-i-n junction (a-Si:H) solar cell has attained highest efficiency record of 10.09% [20]. The result was published in 2009 by researchers from Oerlikon Solar Lab, Switzerland. In their devices, ZnO layers deposited by low pressure chemical vapour deposition (LPCVD) was used as the front and back contact. The i-layer with the thickness of 250 nm was deposited by plasma enhanced chemical vapour deposition (PECVD) technique.

3.2.2 Chalcogenide solar cells

Chalcogenide solar cells contain at least one chemical element from group VI. In this subsection, three types of solar cell are discussed. They are cadmium telluride (CdTe), copper indium selenide or copper indium gallium diselenide (CIGS) and copper zinc tin sulfide (CZTS) solar cells.

Thin-film CdTe solar cell device was first reported in 1963 by Cusano [21]. It was two layers solar cell where the p-type material was Cu_2Te and the n-type material was CdTe. Cusano reported that this solar cell was a p-n hetero-junction device. Although the efficiency reported was 6%, which was satisfactory at the time, the device suffered a stability problem. This was due to the Cu diffusion into the CdTe layers and gradually lowered the efficiency of the cell [22].

In 1972, Bonnet and Rabenhorst came up with a new improvement [23]. The Cu_2Te layer was replaced by CdS. This created hetero-junction structure between n-CdS and p-CdTe. Both layers were grown by high temperature vapour deposition technique. Figure 3.12 shows the solar cell structure. This structure is called substrate because the materials' deposition starts from the back contact. The back and front contacts was made from copper-molybdenum foil and evaporated indium respectively. The maximum efficiency reported was 6%.

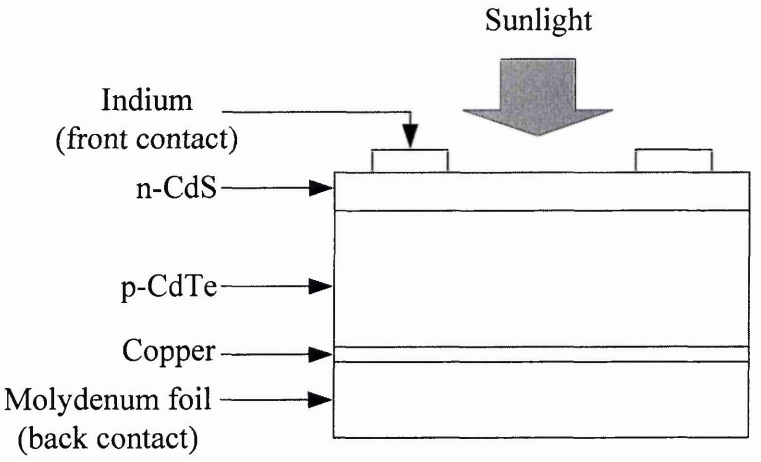

Figure 3.12: CdTe thin-film solar cell fabricated by Bonnet and Rabenhorst in 1972.

Screen printed CdTe solar cell was introduced in 1976 by Nakayama *et al* [24]. Figure 3.13 shows the fabricated solar cell device. This structure is called superstrate and nowadays is more preferable among researchers than the substrate structure. In this structure, the front contact (In_2O_3) is first deposited followed by CdS and then CdTe. Even though this device was fabricated within the non-vacuum environment, efficiency reported has improved to 8.1%.

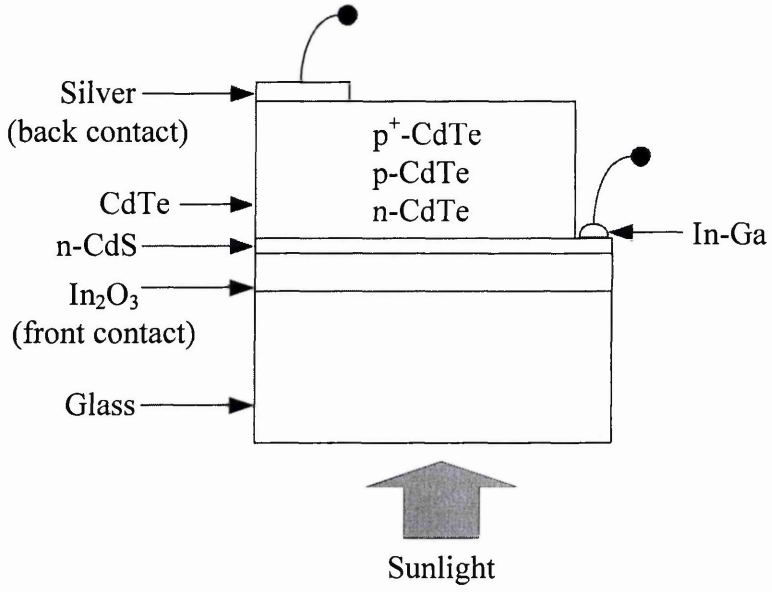

Figure 3.13: CdS/CdTe solar cell fabricated by Nakayama *et al* in 1976. Efficiency reported was 8.1%.

In 1982, Fulop *et al* fabricated CdTe solar cell using electrochemical technique. CdTe was electrodeposited on a metal substrate to obtain n-CdTe. Then high work function metals such as gold was vacuum evaporated to make Schottky contact to the n-CdTe. The efficiency reported was of 8.7% [25].

The 10% efficiency barrier was overcome by Tyan and Albuerne also in 1982 [26]. Close space sublimation (CSS) technique was employed to deposit both CdS and CdTe layers.

During the late 1980s several publications regarding the positive effects of inclusion of $CdCl_2$ during device processing steps toward the efficiency of CdTe solar cell were published [27,28,29]. Ringel *et al* [29] have shown that post deposition annealing with $CdCl_2$ has increased the efficiency of the cells from 1.3% to 8.6%. Capitalizing from this positive result, Britt and Ferekides carried out $CdCl_2$ treatment on their devices and reported the conversion efficiency of 15.8% in 1993 [30]. The solar cell fabricated by Britt and Ferekides has the similar structure as in Figure 1.28 with the inclusion of MgF_2 as the anti-reflection coating on the glass substrate.

After 1993, progress of CdS/CdTe solar cells was stagnated for almost a decade. In 2002, Dharmadasa *et al* proposed a new model for understanding the photovoltaic (pv) effect of CdS/CdTe solar cell [31]. The strength of this new concept is, it has two rectifying junctions (see Figure 3.14). The first junction is the n-n hetero-junction at the n-CdS/n-CdTe interface and the second junction is the large Schottky junction at the n-

CdTe/metal interface. The band diagram of this new design is shown in Figure 3.14. This new design came up after comprehensive studies on metal-n-CdTe interface [32].

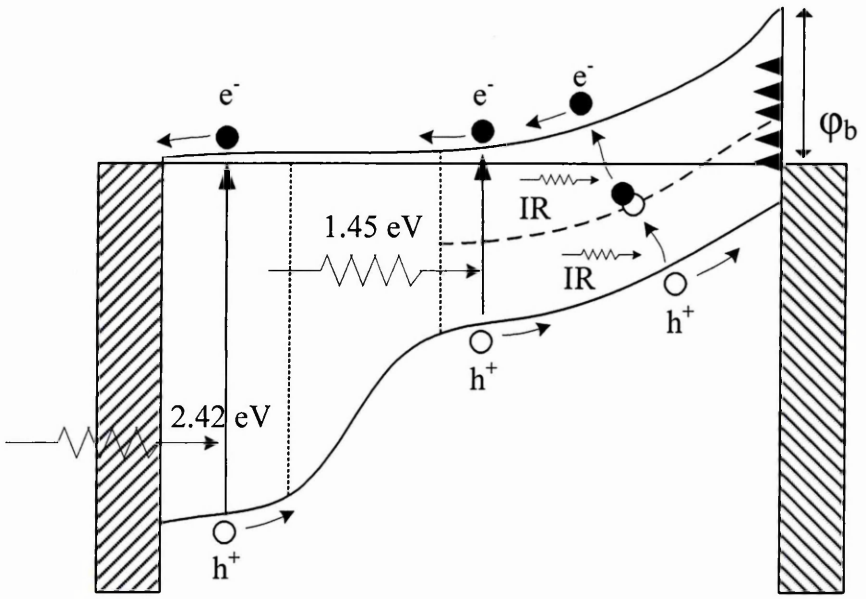

Figure 3.14: The band diagram of CdS/CdTe solar cell as proposed by Dharmadasa *et al.* The solar cell has two rectifying junctions helping each other for enhancing pv action. Redrawn from [31].

Dharmadasa discovered that by carrying out chemical etching on the surface of n-CdTe, the stoichiometry between tellurium and cadmium can be modified. Acidic etching gives the n-CdTe, Te-rich surface while the basic etching produces Cd-rich surface [32].

To produce high efficiency devices, Cd-rich surface is preferable. The reason is by having Cd-rich surface, the Fermi level of CdTe semiconductor is pinned at defect levels 0.96 eV or 1.18 eV below the conduction band minimum as shown in Figure 3.15. These two defect levels are the most preferable if large Schottky barrier is wanted at the back contact. This new design produced conversion efficiency of 18% as reported in 2002 [31].

The highest efficiency of CdTe solar cell was reported by First Solar in August 2014 with 21% [33].

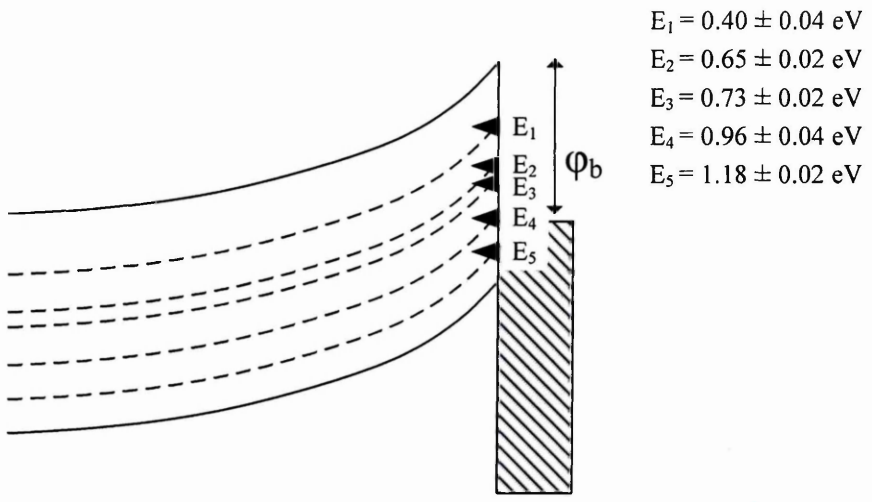

Figure 3.15: Five main defect levels (E_1 to E_5) experimentally observed for metal-n-CdTe interface. Acidic etching preferentially produces E_1-E_3 defect levels while the basic etching preferentially produces E_4-E_5 defects levels. Fermi level pinning can take place at one of these five defect levels. Redrawn from [32].

Copper indium diselenide (CIS) solar cell was first developed in 1974 by Wagner and co-workers [34]. The efficiency of the solar cell was reported as 5%. In 1975, the same group improved the cells by incorporating SiO anti-reflective coating and the efficiency increased to 12% [35]. Efficiencies of CIS solar cells have progressed steadily starting in the late 1980s. Mitchell *et al* has reported 14.1% in 1988 [36] and in 1990, Hedstrom *et al* reported 15.4% efficiency [37].

CIS material has bandgap between 0.95 eV to 1.00 eV [36] while the bandgap for $CuGaSe_2$ is close to 1.70 eV [38]. If CIS is alloyed with Ga, graded bandgap $CuInGaSe_2$ (CIGS) solar cell can be produced, with the bandgap of the device gradually changes from 1.00 eV to 1.70 eV. The first CIGS solar cell devices were reported in 1987 with 10.2% efficiency [39]. The conversion efficiencies of CIGS solar cells gradually improved to 16.9% in 1993 [37] and 19.9% in 2008 [40]. The efficiency of $CuInGaSe_2$ has passed 20% in 2010 [41]. To date, highest efficiency attained from CIGS solar cell is 20.8% [42].

Conventional CIGS solar cell structure is shown in Figure 3.16. Device fabrication starts with the sputtering of back contact molybdenum layer. CIGS layers are deposited usually by co-evaporation of individual elements (Cu, In and Ga) followed by selenization at temperature between 400°C to 600°C in selenium atmosphere [43]. CdS layer is then deposited by chemical bath deposition. The i-ZnO

and n-ZnO:Al layers are deposited by sputtering technique and lastly aluminium/nickel front contacts are made by vacuum evaporation or sputtering [12].

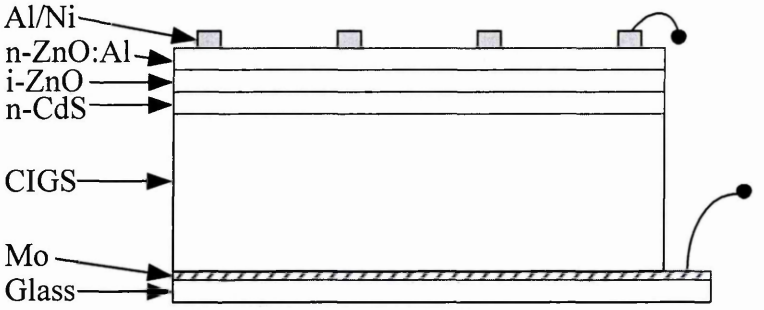

Figure 3.16: Schematic diagram of conventional CIGS solar cell. Redrawn from [12].

Concerns due to the scarcity and increasing price of indium, has led to the introduction of Cu_2ZnSnS_4 (CZTS) solar cell. The photovoltaic effect of CZTS was observed in 1988 by Ito and Nakazawa [44]. CZTS solar cell has achieved highest efficiency of 8.4% [45]. The derivative of CZTS solar cell, $Cu_2ZnSn(S,Se)_4$ (CZTSSe) has performed better than CZTS. In 2013, 11.1% efficiency $Cu_2ZnSn(S,Se)_4$ solar cell has been reported [46].

3.2.3 III-V solar cells

III-V solar cells are photovoltaic device that contain elements from group III and V. Two of the most prominent III-V solar cells are gallium arsenide GaAs and indium phosphide (InP). Highest efficiencies recorded for GaAs and InP are 27.6% and 19.1% respectively [47,48]. These compound semiconductors are renowned for their high mobility of charge carriers. Sze and Irvin have reported the mobility of electron for GaAs semiconductor is 7000 $cm^2V^{-1}s^{-1}$ [49] while for InP, the electron mobility is ~5400 $cm^2V^{-1}s^{-1}$ [50]. Both values represent the electron mobility at 300 K.

III-V solar cells have their own derivatives. These derivatives can be produced by alloying with other elements. For example, AlGaAs solar cell is the product of alloying GaAs semiconductor with Al [51] and GaInP is produced by alloying InP with gallium [52].

Conventional growth techniques used to grow these semiconducting layers are either molecular beam epitaxy (MBE) or chemical vapour deposition (CVD). Since

these growth techniques are costly, III-V solar cells couldn't be utilized for large area photovoltaic solar energy applications.

However, III-V solar cells are more resistance to radiation damage. Because of this advantage, multi-junction III-V solar cells are used to power satellites in the outer space. Multi-junction solar cell is made by connecting 2 or more solar cells in series as shown in Figure 3.17. The connection between the cells is implemented by tunnel junction. Conventionally, if 3 layer multi-junction solar cell is fabricated, the p-i-n diode with the widest bandgap will be facing the sunlight. The purpose of having widest bandgap semiconductor as the first layer is to absorb high energy photons from the ultraviolet region. The second p-i-n diode will absorb photons from the visible region and the last p-i-n diode will absorb photons from the infra-red region. The main advantage of utilizing series connection is the production of high open circuit voltage. Sharp Corporation has reported world's highest power conversion efficiency of 39.5% for triple junction cell in 2013 [53].

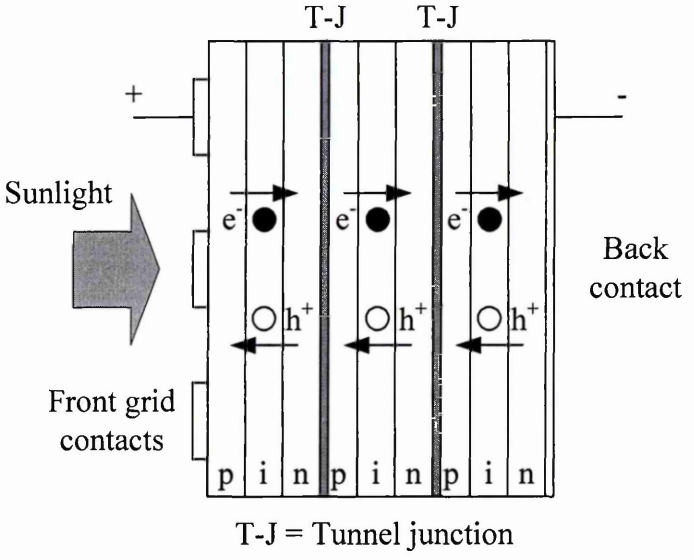

Figure 3.17: Triple junction solar cell connected in series. Redrawn from [12].

3.2.4 Dye-sensitized solar cells (DSSCs)

Dye-sensitized solar cell (DSSC) was invented by Grätzel and O'Regan in 1988 [54]. DSSC is easy to fabricate. The simplified fabrication process of DSSC is explained in Figure 3.18.

The fabrication process starts with the adhesion of titanium dioxide (TiO_2) paste on transparent conducting oxide (TCO). This process is called 'screen printing'. As shown in Figure 3.18(a), the TiO_2 paste is spread evenly on TCO. After that, the heat-treatment process is carried out. After the heat-treatment, the TiO_2 layer will adhere firmly to the TCO and then TiO_2 layer is dipped into a beaker containing dye molecules. This process is known as sensitisation and is shown in Figure 3.18 (b). Next, another TCO is used as the cathode. A hole is drilled on the back of the cathode to allow the injection of redox system-capable electrolyte (usually iodide/triiodide couple) [55] (Figure 3.18 (c)). The cell is now ready for testing (Figure 3.18 (d)).

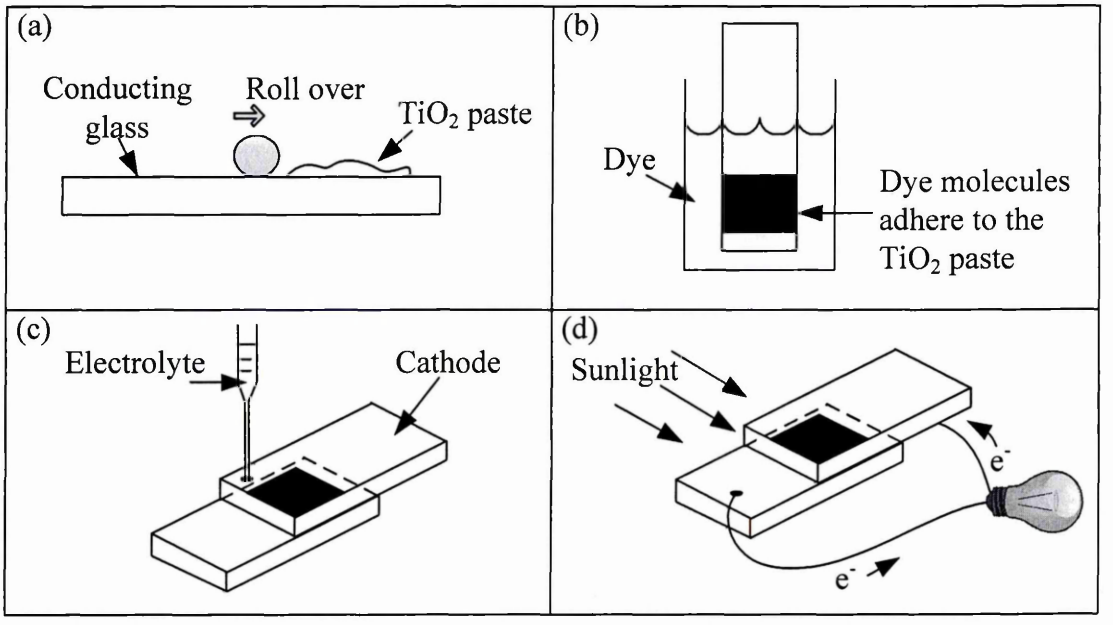

Figure 3.18: Fabrication process of DSSC. (a) TiO_2 is spread evenly on TCO. (b) After heat treatment, the TiO_2 paste is dipped into a dye solution. (c) Redox system-capable electrolyte is injected into the hole made at the back of the cathode. (d) DSSC is now ready for testing [56].

Principle of operation of DSSC is shown in Figure 3.19. When dye molecules absorb photons, the electrons are excited and then injected into the conduction band of TiO_2 as shown in Figures 3.19 (a) and (b). Electron will move to the external circuit and will be collected by the iodide/triiodide electrolyte (also known as mediator). The mediator will donate the electron back to the dye molecules (Figure 3.19 (c)). Next, the mediator becomes positive ions and ready to accept new electrons (Figure 3.19 (d)).

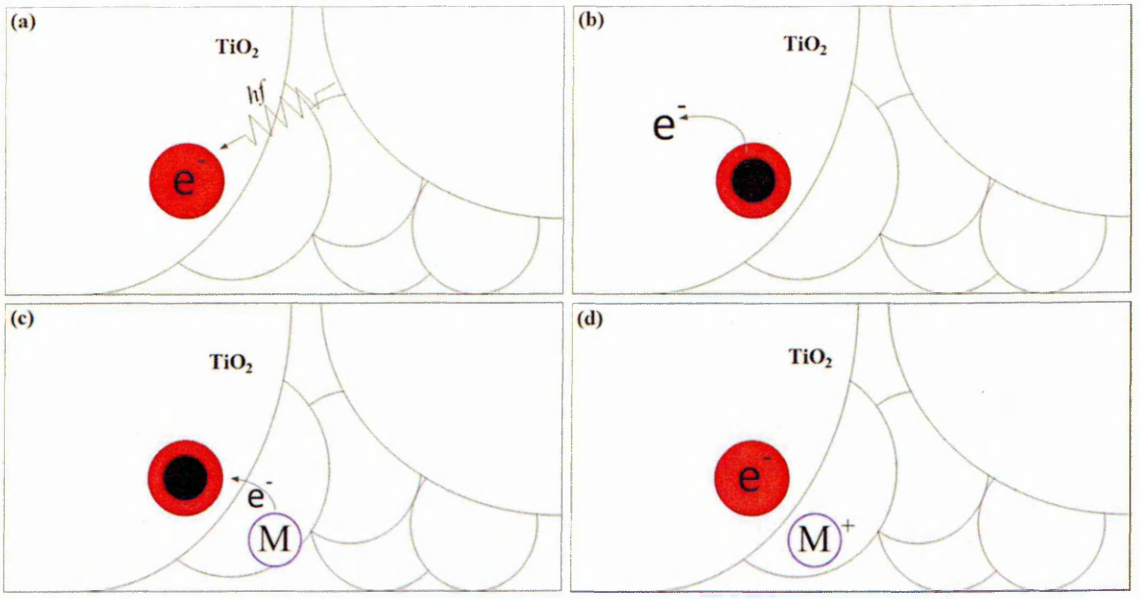

Figure 3.19: Principle of operation of DSSC. (a) Dye molecules absorb photons. (b) After photons absorption, electrons are injected into the conduction band of the TiO_2 and transported to the external circuit. (c) The electrolyte (mediator) will collect electrons from the external circuit and donate the electrons to the dye molecules. (d) The mediator becomes positive ions and ready to accept new electrons [56].

Even though the low cost and ease of fabrication have been the 'selling points' for DSSC, the commercialization of this technology is still far from realization. One of the factors is the sealing of the liquid electrolyte which is difficult to solve. The other factor is the stability of electrolyte. Grätzel in his review article suggested that the redox cycle of the electrolyte should sustain 10^8 turnover cycles which is equivalent to 20 years of exposure to light [55]. Highest efficiency of DSSC is 11.9% and has been reported by Sharp Corporation in 2012 [2].

A new generation of DSSC known as perovskite solar cell was introduced in 2013. Perovskite solar cell evolves from the efforts of replacing the liquid electrolyte in DSSC with solid material. The history of perovskite solar cell is presented in detail by Snaith [57]. Currently, the highest efficiency of perovskite solar cell is 20.1% [58].

3.2.5 Organic solar cells (OSCs)

Organic solar cells (OSCs) are the photovoltaic device fabricated from organic semiconductors. In OSC, the organic compounds usually made from polymers are used to absorb photons and create mobile charge carriers. The photovoltaic activity of the

organic semiconductors was observed by Kearns and Calvin in 1958 [59]. OSC differs from inorganic solar cells in many ways.

Firstly, in inorganic solar cells, when photons are absorbed, the mobile charge carries (electron-hole pairs) are created instantaneously. These charge carriers are swept to the opposite directions with the help of built-in electric field inside the inorganic materials within a pv active junction. Meanwhile, in organic solar cells, the free charge carries are not instantaneously created. Instead, the absorption of photons only creates bounded charge carriers also called the excitons as shown in Figure 3.20. It is worth noting that the binding energy of excitons in organic semiconductors is very large (~0.5 eV). As a comparison, the binding energy of inorganic semiconductors is ~ 0.01 eV. Thermal energy at room temperature which is close to ~0.025 eV is not sufficient to break the excitons into mobile charge carriers [60]. In order to produce mobile charge carriers, the excitons have to be dissociated with the help of additional energy.

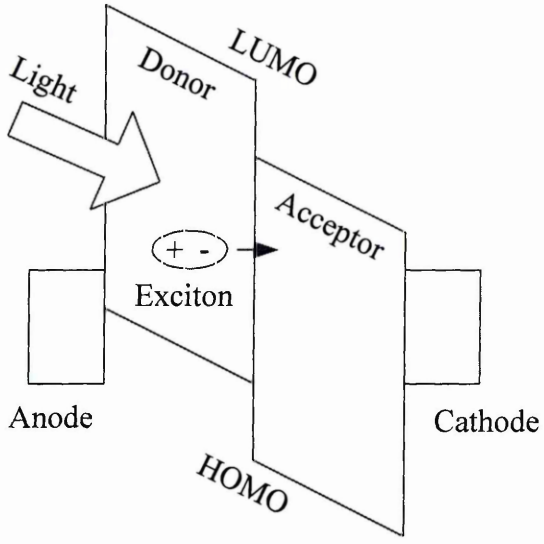

Figure 3.20: The energy band diagram of organic semiconductors. Absorption of photons in organic semiconductor creates excitons. The donor-acceptor interface provides additional energy to dissociate excitons into mobile charge carriers. Redrawn from [60].

The discovery of donor-acceptor materials by Tang in 1986 has helped to solve this problem [61]. The dissociation of photo-generated excitons seems possible at the donor-acceptor interface. The energy difference between the electron affinity of the acceptor and donor materials provides the sufficient energy to break the excitons into mobile charge carriers. Mobile charge carries can only be produced if the energy offset

at the donor-acceptor interface exceeds the binding energy of the excitons [60]. When mobile electrons and holes are produced, the electrons are excited into the lowest unoccupied molecular orbital (LUMO) while the holes are left at the highest occupied molecular orbital (HOMO) as shown in Figure 3.21. Electrons are collected at the cathode while holes are collected at the anode. LUMO and HOMO are analogous to conduction band and valence band in inorganic semiconductors respectively.

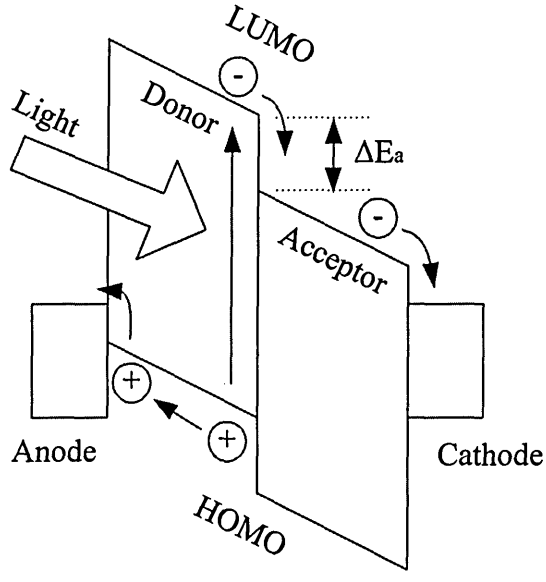

Figure 3.21: Mobile charge carriers are produced if the energy at the donor-acceptor interface is larger than the binding energy of the excitons. Electrons and holes are collected at the cathode and anode respectively. ΔE_a is the energy offset at the donor-acceptor interface. Redrawn from [60].

In organic solar cell, the anode is made from TCO while the low work function metals such as aluminium (Al) or magnesium (Mg) are used as the cathode.

Up until now, various types of donor and acceptor layers have been put to test. Examples of donor materials are copper phthalocyanine (CuPc), poly(2-methoxy-(5-ethylhexyloxy)-1,4-phenylene-vinylene) (MEH-PPV) and poly(2-methoxy-5-(3,7, dimethyloctyloxy)-1,4-phenylenevinylene) (MDMO-PPV). For the acceptor materials, the examples are perylene derivative 3,4,9,10-perylene tetracarboxylic bis-enzimidazole (PTCBI), fullerene (C_{60}) and Phenyl-C61-butyric acid methyl ester (PCBM). The confirmed highest efficiency for OSC is 11.1% [2].

New generation of PffBT4T-2OD: C71BM (donor:acceptor) materials have been reported in 2014 [60]. This type of donor showed promising result by producing highest conversion efficiency of 10.8%. In addition, it is also insensitive to the choice of fullerenes [62].

The major advantages of using organic semiconductors over the inorganic semiconductors are the low cost of the active layers (donors and acceptors), fast fabrication and the capability of depositing the active layers on flexible substrates using roll to roll process.

Although it seems very attractive, the stability issue is a major concern for organic semiconductors. Kumar and Chand [60] in their comprehensive review article stated that OSCs can degrade under both dark and illuminated condition. The major cause for the cell degradation is the interaction of OSCs with oxygen and moisture.

3.3 Summary

This chapter has discussed about various types of solar cells. The extensive research in photovoltaic devices gained serious attention in 1970s even though the photovoltaic effect was discovered in 1839.

Nowadays, solar cells can be categorized by inorganic and organic solar cells. For inorganic solar cells, tremendous effort has been devoted to improve the understanding of the science behind solar cells. As a result of decades of research, the efficiencies of inorganic solar cells have gone beyond 20% for single junction devices.

Inorganic solar cells have evolved from being the high cost-high efficiency solar cell (first generation) to become the low cost-low efficiency solar cell (second generation). The next target for inorganic solar cells is to be the low cost-high efficiency devices (third generation). Third generation solar cells should be able to deliver dollar per watt ratio between 0.10 $/W to 0.30 $/W.

The highest efficiency of organic solar cells is about half of the inorganic solar cells. However, organic solar cell offers ease and fast device fabrication compared to inorganic solar cells. The very low cost of raw materials used in organic solar cell is also an attracting factor for this device to be seriously developed. If at least, the stability issues of organic solar cells can be solved, this device will surely be the material of choice for indoor renewable energy applications.

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4.1 Introduction

This chapter provides information about the growth techniques used in thin film fabrication. Generally, the techniques to deposit thin-film semiconductors can be divided into two categories; vapour phase depositions and liquid phase depositions.

4.2 Vapour phase deposition (VPD) techniques

In semiconductors' growth, vapour phase deposition is deposition technique where the desired materials or layers change from gaseous phase to solid when interact with the substrates. Vapour phase deposition is a high cost technique to grow semiconductors because usually the deposition process is carried out in vacuum chambers. However, the presence of vacuum environment reduces the impurity content in the deposited materials. In this subsection, four vapour phase deposition techniques are presented. These include molecular beam epitaxy (MBE), sputtering, close space sublimation (CSS) and chemical vapour deposition (CVD).

4.2.1 Molecular beam epitaxy (MBE)

Molecular beam epitaxy (MBE) is a renowned technique used to deposit single crystal thin films. Deposition of materials is done in an ultra-high vacuum (less than 10^{-7} Pascal) environment. To deposit semiconductor layers, for example GaAs, ultra-high purity Ga and As precursors will be loaded separately inside the effusion cells. These effusion cells will be heated to the temperatures that allow the Ga and As atoms to sublime. Computer controlled shutters are used to control the emission of atoms or molecules from these two elements. Ga and As atoms will escape the effusion cells and travel to the substrate where these atoms will react with each other and deposit on the substrate. MBE technique allows precise control of doping because no chemical reactions occur before the atoms reach the substrate. Depending on materials, substrate temperature can vary between 400°C to 800°C.

Thickness of the deposited materials can be monitored in-situ with the Reflection High Energy Electron Diffraction (RHEED) gun. Electron emitted from the

gun will be projected to the substrate. Then, the electrons are reflected and fall on the fluorescent screen. The diffraction patterns appear on the fluorescent screen will provide the indication about the ongoing status of a new atomic layer created.

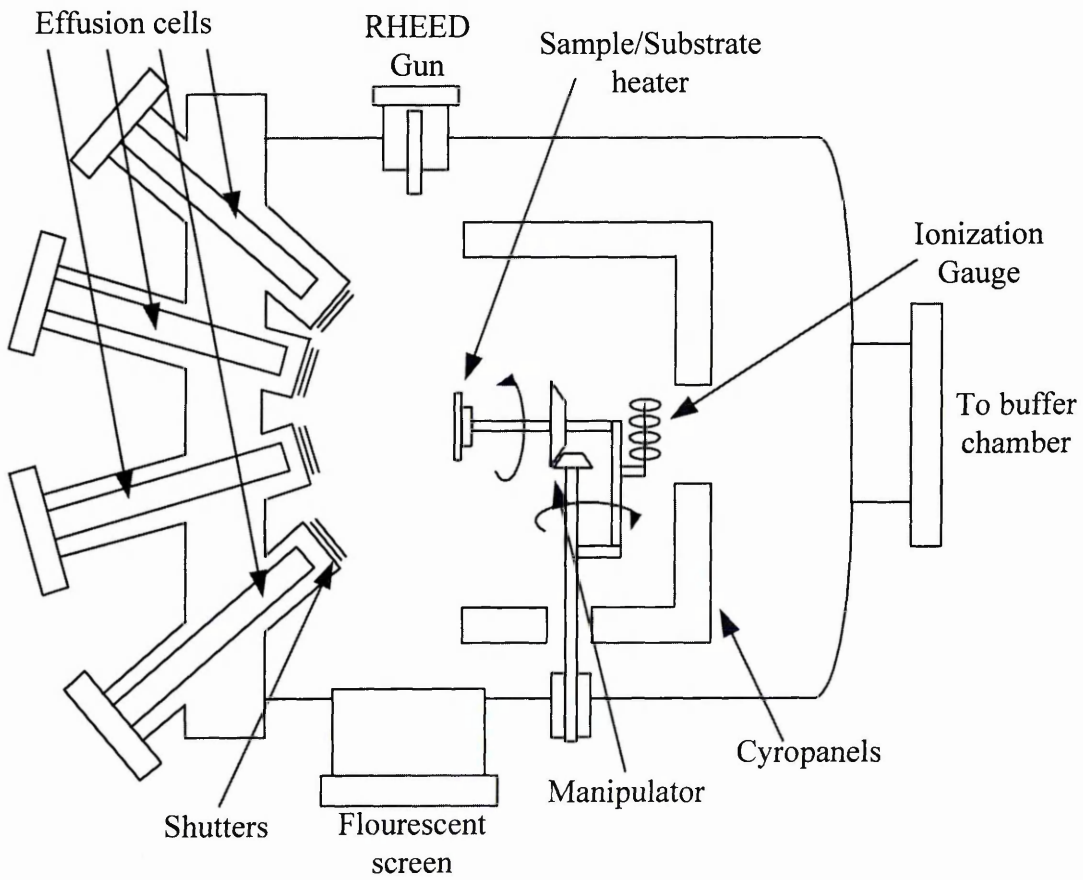

Figure 4.1: Molecular beam epitaxy system showing its main components. Redrawn from [1].

At position X_1 (Figure 4.2 and 4.3), the reflected electrons beam will result the highest intensity. This is because at this stage, the surface of the substrate is still smooth. Gradually over time, few islands are created on the substrate. As a result, the incident beam will scatter and the intensity of the reflected beam decreases (X_2 position). At X_3, intensity is at the lowest point because this is the stage where most of the islands are created. At X_4, the electrons beam intensity comes back to the same level as X_2 because at this stage the islands merge together and leave few voids. Finally at X_5, these voids will be filled and a new layer is completed. The electrons beam intensity goes up again to the level that is almost similar to X_1. As the summary, every completed period as shown in Figure 4.2 indicates the completion of a single atomic layer.

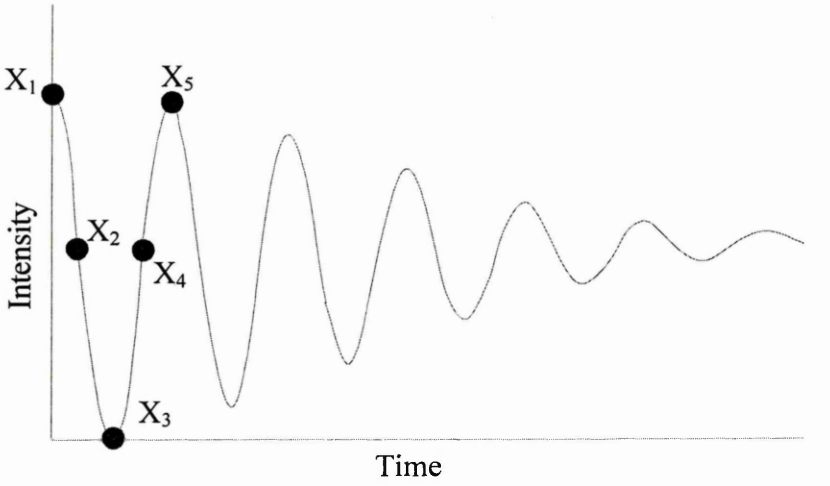

Figure 4.2: Intensity of the reflected electron beams indicate the ongoing status of newly created single atomic layer. Redrawn from [2].

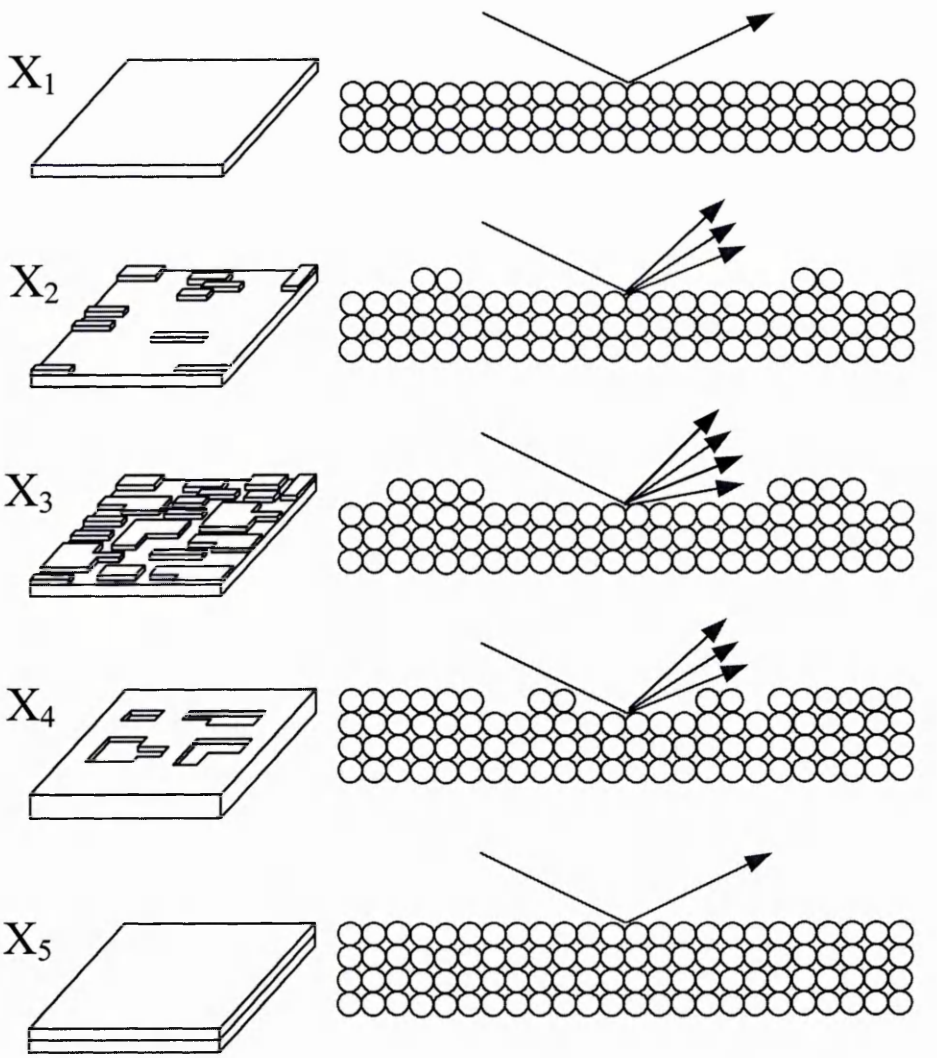

Figure 4.3: Scattering of RHEED electrons beam is at the highest level when many islands are created but reduces when these islands merge together. Redrawn from [1].

MBE has the capability to provide high quality epitaxial growth of various semiconductors but it is a very high cost technique. Commonly, MBE is used to grow semiconductors on small substrates. The growth rate for a single layer is slow (from 10 nm per minute to 300 nm per minute). These drawbacks make MBE unsuitable for mass production of solar panels. However, this technique is preferred for producing multi-junction solar cells. Multi-junction solar cells commonly used in satellite applications. For this kind of purpose, cost is not the issue because the efficiency of the solar cells matters the most.

4.2.2 Sputtering

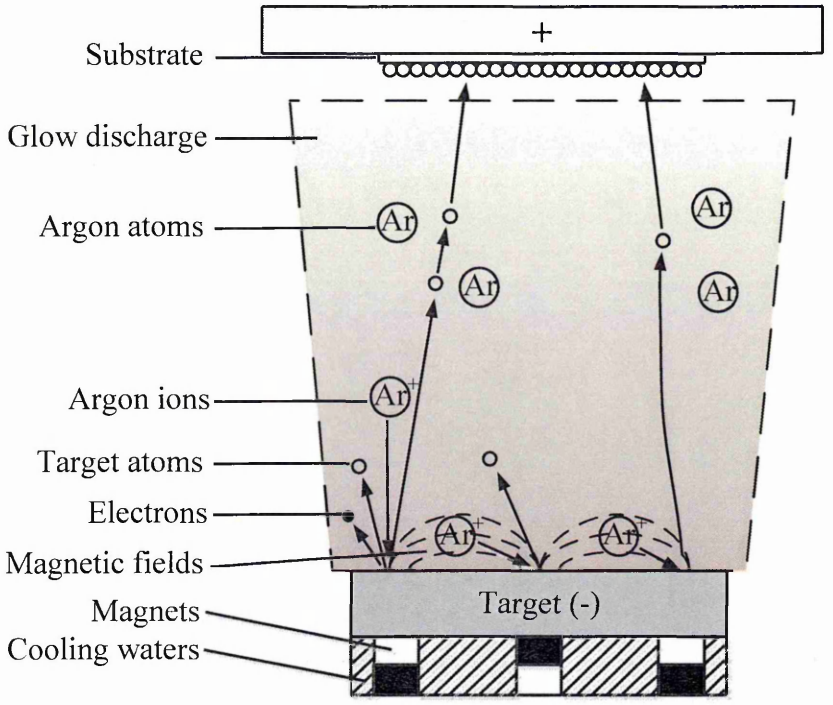

Figure 4.4: Sputtering deposition system with its main components. Redrawn from [3].

Sputtering deposition is a reliable alternative to deposit materials that have high melting points. In sputtering deposition, material that is intended to be deposited (the target) will not be heated to its melting point. Conversely, the target will be bombarded with inert foreign ions such as Argon (Ar). To start the sputtering deposition, the substrate will be loaded into the deposition chamber. From this point, air will be pumped out from the deposition chamber using a turbo pump. This is done to create vacuum space inside the deposition chamber. When it is vacuumed, Argon gas will be released into the chamber. At the target, high voltage DC supply will be switch-on thus

creating plasma cloud near the target where Ar atoms are ionized. Ionization of Ar will produce free electrons and positive Ar ions (Ar^+). The Argon atoms that are moving freely inside the plasma cloud will collide with the free-moving electrons. The collision between Argon atoms and these electrons will create secondary Argon ions and secondary free electrons. Argon ions are positively charged. Since the target has negative polarity, the Argon ions will now accelerate towards the target and knock off the atoms on the target's surface. The target's atoms will accelerate to the substrate and condense on the substrate's surface.

To improve the efficiency of the process, magnetic bars are installed near the target. These magnetic bars will create magnetic field near the target to confine the movement of Ar^+ and free electrons. If these two particles are confined, the production rate of Ar^+ will increase thus reducing the deposition time. In addition to that, the confinement of these two particles in the plasma cloud will help to reduce the damages on the substrate caused by the bombardment of Ar^+ and electrons.

4.2.3 Close space sublimation (CSS)

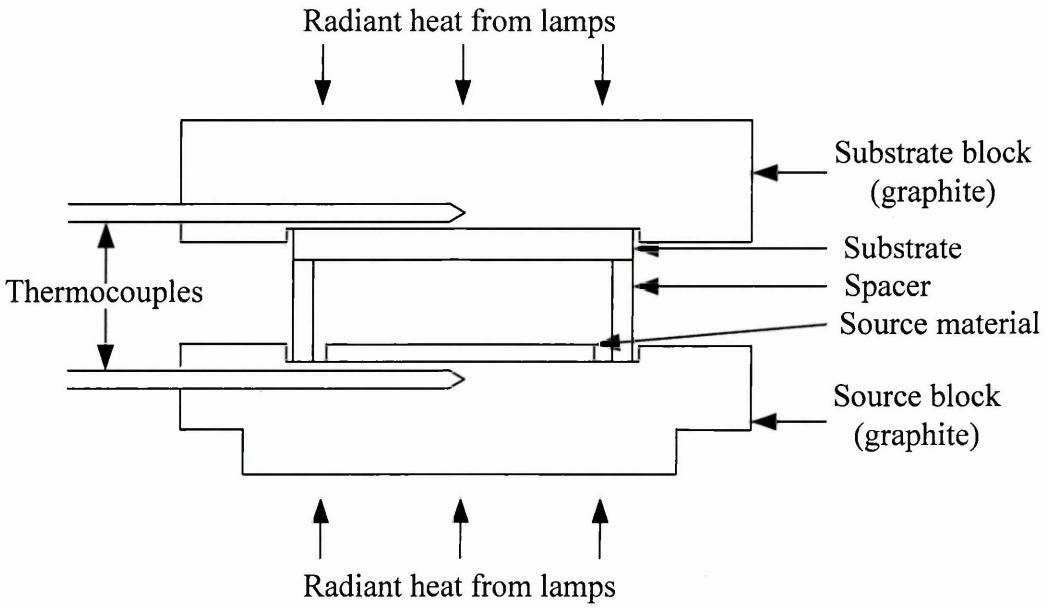

Figure 4.5: The set-up of close space sublimation deposition system. Redrawn from [4].

In close space sublimation (CSS) technique, the deposition substrate is suspended horizontally while the source material is placed below the substrate. The gap

between the source and the substrate is about few millimetres (1 to 5 mm) [5]. Both substrates and source materials are heated with halogen lamps. The temperature measurements are monitored using thermocouples as shown in Figure 4.5. If CdTe layers are to be deposited, high purity CdTe wafers grown from Bridgman's method is used as the source material [6]. The growth rate of CdTe layers by CSS is estimated around (2-3) μm/min with source and substrate temperatures of 500°C and 600°C, respectively [7,8]. Currently, CSS is the best growth technique to grow CdTe layers because the highest efficiency of CdS/CdTe solar cells was obtained from this technique. CdTe solar panels were proven manufacturable and scalable using this technique. First Solar, utilizes CSS technique to produce their solar panels.

4.2.4 Chemical vapour deposition (CVD)

Chemical vapour deposition (CVD) is defined as the formation of solid film caused by reaction of gaseous reactants that contain the required constituent. CVD is widely used to deposit dielectric materials such as SiO_2 and Si_3N_4 and also metals such as tantalum, aluminium and copper. In CVD, to deposit thin films, the gaseous reactants are transported to the deposition chamber as shown in Figure 4.6. Gaseous reactants include source gas, carrier gas and dopant gas.

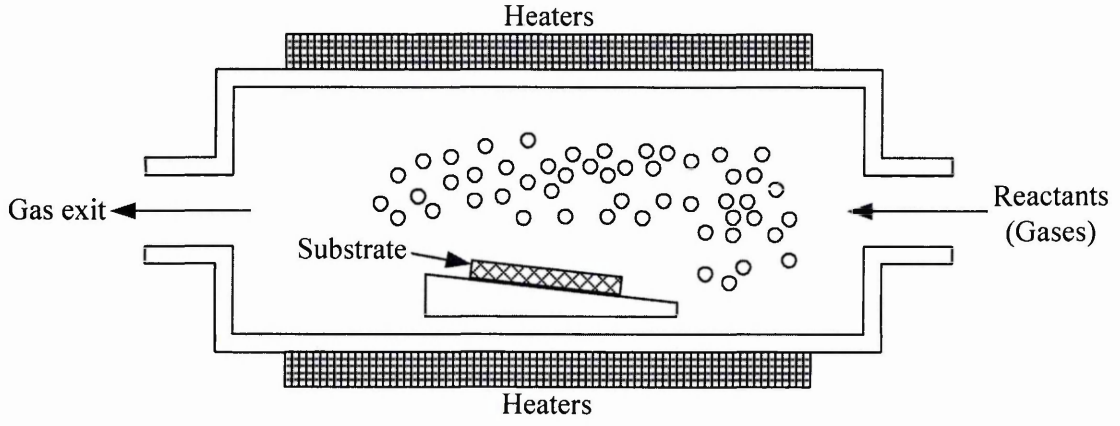

Figure 4.6: Chemical vapour deposition system showing three main subsystems. These subsytems are (i) gas delivery to the deposition chamber (ii) gas exit from the chamber and (iii) heaters. Redrawn from [9].

For example, if thin film CdTe is to be deposited, dimethylcadmium (DMCd)

and dimethyltellurium (DMTe) will be the source gas and high purity H_2 is the carrier gas [10]. At the deposition chamber the deposition mechanism starts with the adsorption of the desired species on the substrate surface. The reactions happened at this stage are driven thermally by the heaters as shown in Figure 4.6. Since gaseous atoms come in contact with the substrate, this makes possible for CVD to produce epitaxial layers. The undesired elements and by products will be transported out from the reaction chamber. The process variables involved in CVD are the reaction temperature, partial pressure of the gases and the pressure of reaction chamber.

CVD has several advantages. Firstly, CVD produces uniform layers over a large area of substrate. CVD is multidirectional deposition, so the compositional gradient of the as-deposited materials is almost non-existence across the substrate.

The disadvantages of CVD mostly involved safety and contamination. For example, a precursor like arsine (AsH_3) which is used as the precursor to deposit GaAs is toxic and can ignite fire when comes in contact with air.

4.3 Liquid phase deposition (LPD) techniques

Liquid phase deposition (LPD) (or wet chemical deposition) is a growth technique normally carried out in non-vacuum environment. Since the vacuum system is not used, it makes liquid phase deposition a low-cost technique to deposit semiconducting materials. The scaling-up process is easier to implement compared to vapour phase deposition. If deposition process is carried out within a vacuum chamber, the size of the substrates will be limited by the size of the vacuum chamber. Usually in LPD the precursors or substances used for deposition process will be dissolved in either aqueous or non-aqueous solution. In contrast to VPD, the desired materials change from liquid phase to solid. Examples of LPD include electrodeposition (ED), chemical bath deposition (CBD), screen printing and spray pyrolysis.

4.3.1. Electrodeposition

Electrochemical deposition or simply known as electrodeposition is one of the non-vacuum deposition techniques. It is widely used to deposit metals onto electrical conducting surfaces. This is done to protect certain products from corrosion and to enhance the aesthetic values. Electrodeposition set-up consists of anode (counter

electrode), cathode (working electrode), reference electrode, voltage supply, electrolyte, stirrer and hot plate. These components together with electrical connections to the potentiostst are shown in Figure 4.7.

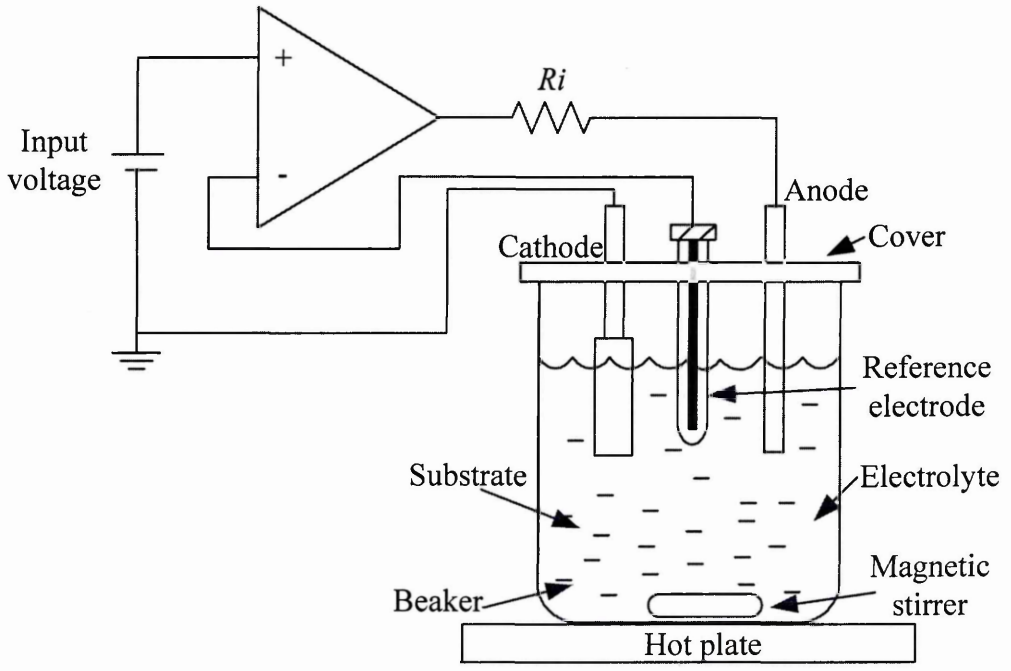

Figure 4.7: Three-electrode electrodeposition system set-up showing the essential components and electrical connections to the potentiostat.

Figure 4.7 shows the set-up of 3-electrode system. In this system, the voltage is measured between the cathode and reference electrode. Because of concentration of electrolyte inside the reference electrode is not changing during deposition, voltage measured is very stable with almost no fluctuations. However, in 3-electrode system, the electrolyte contained in the reference electrode (such as $AgCl_2$ or KCl) might leak and contaminate the electrolyte. If the leakage happens, it will drastically affect the efficiency of CdTe solar cells. The deteriorations of CdTe solar cells efficiency after being contaminated by Cu^{2+} and Ag^{1+} ions was reported by Dennison [11].

To prevent the leakage from happening, the best way is to omit the reference electrode as shown in Figure 4.8. Removing the reference electrode will not only reduce the impurity sources but also simplify the system and at the same time reduce the cost because the reference electrode has lifetime and must be replaced when needed. Most of the reference electrode has limiting temperature of operation at 70°C. Therefore, removal of the reference electrode allows materials to be grown at 85°C in aqueous

solution to grow with improved crystallinity. In 2-electrode system, voltage is measured between the cathode and the anode. The consequence of using 2-electrode is the instability of the electrode potential. However, previous researches have shown that its effect of the semiconductor layers' quality is insignificant [12,13].

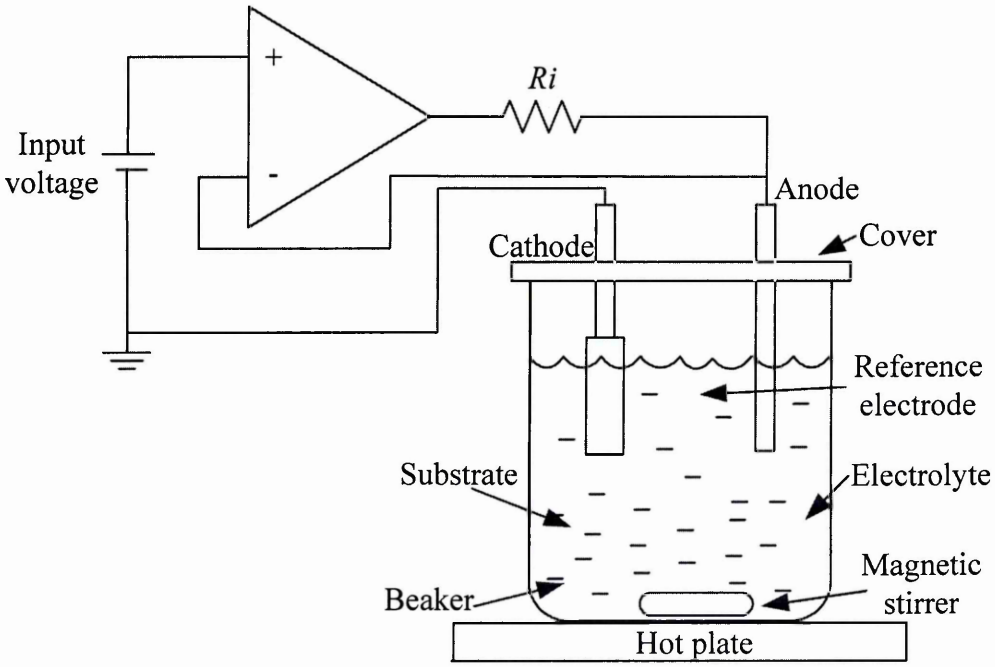

Figure 4.8: Two-electrode electrodeposition system set-up showing the essential components and electrical connections to the potentioststst

Thickness, T (in cm) of the electrodeposited materials can be calculated from Equation (4.1) [14].

$$T = \frac{1}{nFA} \times \frac{ItM}{\rho} \tag{4.1}$$

Where;

n is the number of electrons involved in depositing one mole of substance

F is the Faraday's constant (96485 $Cmol^{-1}$)

A is the area in (cm^2)

I is the average current (A)

t is the deposition time (s)

M is the molar mass of the substance ($gmol^{-1}$)

ρ is the density of the deposited film (gcm^{-3})

To understand how electrodeposition works, consider the electroplating of copper onto an iron (Fe) substrate shown in Figure 4.9(a) and 4.9(b). In Figure 4.9(a) and 4.9(b), copper bar is used as the anode while the iron substrate is used as the cathode. When copper bar is dipped into the $CuSO_4$ solution, the Cu atoms lose two electrons and become copper ions (Cu^{2+}). Cu^{2+} ions then, dissolve into the $CuSO_4$ solution. At the anode;

$$Cu - 2e \rightarrow Cu^{2+} \tag{4.2}$$

When the voltage supply is turned-on, the Cu^{+2} ions will be attracted to the cathode which is the negative terminal. At the cathode, the Cu^{+2} ions will receive two electrons and will be discharged and deposit as Cu atoms on the iron substrate. The chemical reaction happens at the cathode is;

$$Cu^{2+} + 2e \rightarrow Cu \tag{4.3}$$

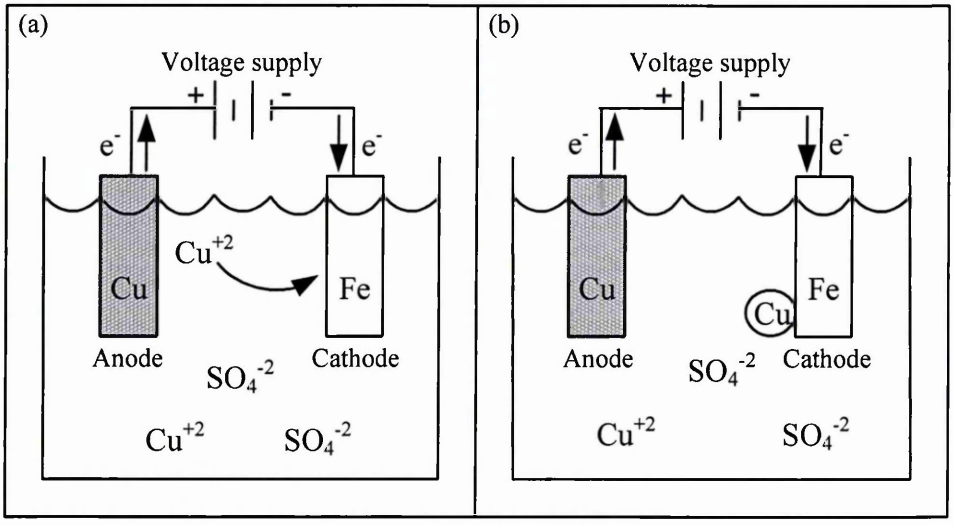

Figure 4.9: The electrodeposition of copper atoms onto iron substrate. When voltage supply is turn-on, cations will be attracted to the Fe cathode (a) At the Fe cathode, Cu^{2+} will receive two electrons and deposit on the cathode's surface (b).

It is important to note that the reduction of Cu^{+2} to form Cu will only proceed if the potential applied is less (more negative) than the standard reduction potential of Cu^{+2} (+0.34 V vs. SHE at 25°C) [15]. The above example is about the deposition of single element onto a substrate. This means only one cation is needed in the electrolyte.

However, in electrodeposition of semiconductors, the number of cations in the solution can be more than one. This is because binary compound semiconductors such as ZnTe, CdS and CdTe need two cations inside the solution. If ternary or quaternary compound semiconductor is to be electrodeposited, then three or four cations should be inside the chemical solution. The examples of quaternary compound semiconductors are copper indium diselenide (CIS) and copper indium gallium diselenide (CIGS).

Electrodeposition of semiconductors was first tried on silicon in 1865 followed by germanium in 1866 [16]. However, work on these two semiconductors were slowly reduced due to the low quality of the electrodeposited materials. Electrodeposition of CdTe initiated by Panicker *et al* in 1978 has drawn research interest in electrodeposited CdTe as the absorber material for solar cell applications [17]. Four years later, Fulop *et al* reported electrodeposited CdTe solar cell has achieved 8.7% efficiency [18]. Up till today, BP Solar still holds the record of highest efficiency of electrodeposited CdTe from aqueous solution at 14.2% for lab-scale devices [19].

Beside its simplicity, electrodeposition is also scalable and manufacturable technique for producing solar panels. The scalability and manufacturability of this technique have been proven by BP Solar in the late 1990s [20]. This programme produced 0.94 m^2 CdS/CdTe solar panels with efficiency ~11.0%, demonstrating the manufacturability of this technology.

4.3.2 Chemical bath deposition (CBD)

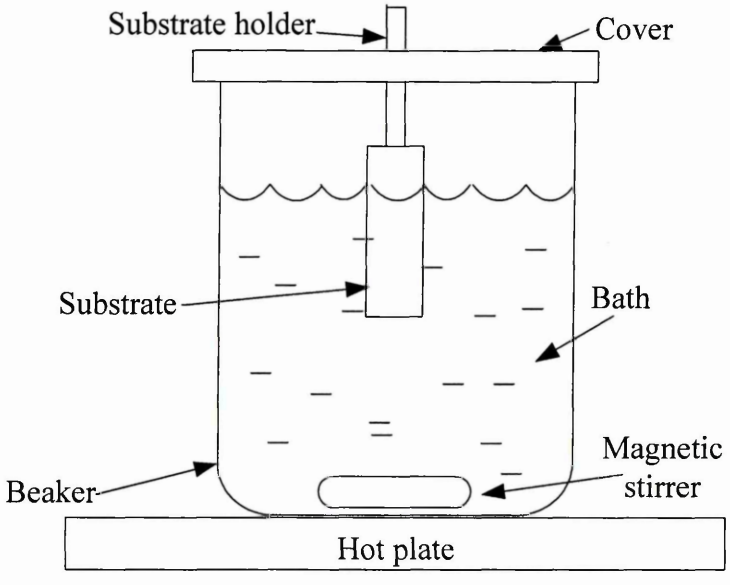

Figure 4.10: Schematic diagram of standard chemical bath deposition apparatus.

Chemical bath deposition is a widely used technique to deposit CdS onto conducting glass for CdTe based solar cells application. CBD is a fast, simple and low-cost technique to deposit uniform layers onto substrates. Similar to electrodeposition, this technique is also scalable and manufacturable. Chemical bath deposited materials such as CdS usually have good adhesion to the substrates. Figure 4.10 shows the set-up of CBD deposition. It is very similar to electrodeposition except that it does not require power supply. The prerequisite for depositions to happen is the solution prepared must be able to precipitate at certain temperature and pH. According to Chu *et al* [21], the precipitation of CdS will happen if the product of ions' concentration exceeds the solubility product of CdS. When reactions occur, the precipitated CdS will deposit and adhere to the substrate. The deposition time can vary depending on the required thicknesses. The longer the deposition time, the higher the thickness of the film will be. The major drawback of CBD is the unrecyclable waste that contains cadmium left in the beaker or tank after deposition. Cadmium is toxic and dangerous to the environment. Managing this waste is expensive and should be handled in extreme care so that it will not cause harm to the environment.

4.3.3 Screen printing

The essence of screen printing process is the preparation of paste of the material that wants to be deposited. In CdTe thin films deposition, preparation for CdTe paste starts with the ball milling of high purity (99.999% pure) mixture of Cd and Te powder in water [22]. $CdCl_2$ and propylene gylcol were later added as the fluxing agent and binder respectively. Next, the paste will be screen printed on the substrate as shown in Figure 4.11. Mask is used to provide voids for the paste to fill-in and touch the substrate while the roller or squeegee is used to spread the paste evenly. The paste is then dried at temperature of 120°C. When the paste is dry, the sintering process starts by heating the CdTe layers at high temperature (600°C to 700°C) for 1 hour [23]. The quality of the semiconducting layers is determined by the drying temperature, the sintering temperature and viscosity of the paste [24].

The highest conversion efficiency for screen printed CdTe solar cell with 12.8% was reported by Matsumoto *et al* in 1984 [25].

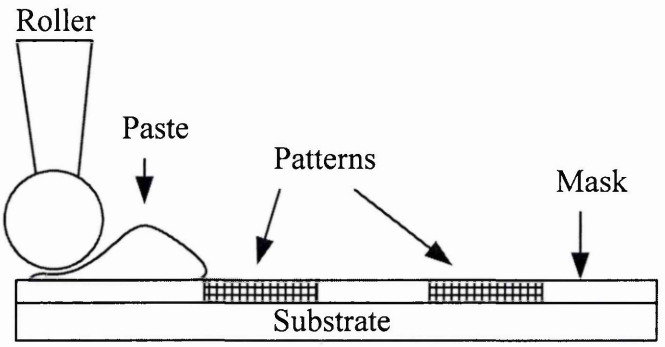

Figure 4.11: Schematic diagram of screen printing process.

4.3.4 Spray pyrolysis

Spray pyrolysis was invented by Hill and Chamberlin in 1964 [26]. Spray pyrolysis has two essential components which are the atomizer and the temperature controller. Figure 4.12 shows the spray pyrolysis deposition system. The role of the atomizer is to spray small droplets on the heated substrate while the temperature controller is employed to heat the substrate to the desired temperature.

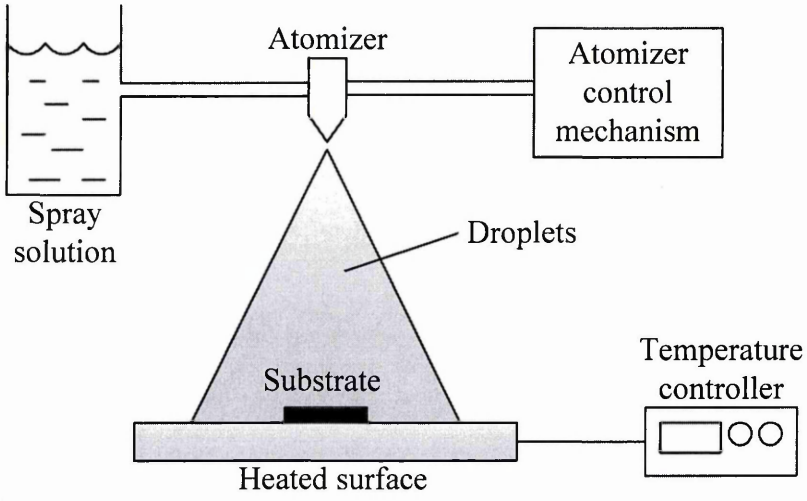

Figure 4.12: Schematic diagram of spray pyrolysis system showing two of its main components; the atomizer and temperature controller. Redrawn from [27].

The properties of the deposited films are governed by the substrate temperature, solution concentration, and rate of spray [28,29]. The spray solution should at least contain elements desired in the resultant film. CdS was among the earliest materials that have been studied and deposited by this technique. Table 4.1 listed the usable starting

materials for CdS deposition. Initial works on spray deposited CdS semiconductor were reported by Chamberlin and Skarman in 1966 [28].

Table 4.1: Usable starting materials for depositing CdS using spray pyrolysis [28].

Cd	S
Cadmium propionate	Thiourea
Cadmium acetate	N,N, dimethyl thiourea
Cadmium formate	allythiourea
Cadmium chloride	thiolocetic acid
Cadmium nitrate	2-thiozoline-2-thiol ammonium thiocyanate

In 1977, Ma and co-workers have fabricated CdS/CdTe solar cell by spraying CdS solution on CdTe single crystal substrate. They have reported the maximum 6.5% conversion efficiency [30]. However, this record was broken by Ahrenkiel and co-workers when they reported higher conversion efficiency of 12.7% in 1991 [31].

Advantages of using spray pyrolysis include low-cost, scalable, uniform coverage across substrates and fast deposition.

4.4 Summary

Various thin film deposition techniques have been presented in this chapter. Deposition techniques for thin film solar cells can be categorized into two groups; vapour phase deposition and liquid phase deposition.

In general, vapour phase depositions are costly technique because the deposition process is carried out inside vacuum chamber while liquid phase depositions require no vacuum system. This makes liquid phase depositions less expensive.

The best efficiency for CdS/CdTe solar cell obtained from vapour phase deposition is 21% through CSS [32] as reported in 2014. On the other hand, liquid phase deposition has recorded best efficiency of 14.2% in 1991 and 18% in 2002 from electrodeposition technique [19,33].

It is obvious that vapour phase depositions and liquid phase depositions have their own advantages and disadvantages. Regardless the deposition technique used, in solar cell research and development, three most important factors that should be considered are low-cost, scalability and manufacturability [34].

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5.1 Materials characterisation techniques

In Chapter 4, various types of thin film deposition techniques have been presented. After deposition process is completed, thin films have to undergo several characterisation techniques in order to optimize the quality of the deposited materials. Some of the important material properties that are worth studying for are structural, optical, electrical, morphological and compositional. This sub-section will present the characterisation techniques that have been used throughout this research programme.

5.1.1 Optical absorption

Optical absorption is a simple and fast technique to determine the bandgap of semiconductor materials. Figure 5.1 shows the process of estimating the band gap of semiconductors.

The light from the source is selected and transmitted by the diffraction grating. If energy of the incident light is higher or equal to the bandgap of the tested samples, the light will be absorbed. Any unabsorbed light will be transmitted to the photodiode. The photodiode will convert the light into electrical signal and this signal will be amplified. The output can be seen from the computer monitor.

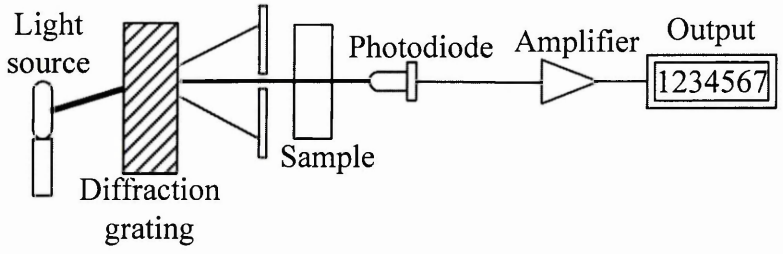

Figure 5.1: The set-up of the optical absorption showing its main components. Redrawn from [1].

The bandgap is obtained by extrapolating the straight line portion of the $(\alpha hv)^2$ *vs. hv* curve to the *hv* axis. The intersection on the *hv* axis gives the energy bandgap

according to the Tauc relation in Equation (5.1) [2];

$$(\alpha hv) = C(hv - E_g)^{\frac{n}{2}} \tag{5.1}$$

Where α is the absorption coefficient of the sample, h is the Planck's constant, v is the frequency of the incident photon, C is a constant depending on the refractive index of the sample, E_g is the optical bandgap of the sample and the value of n is 1 for direct bandgap and 4 for indirect bandgap semiconductors. All of the optical absorption results presented in this thesis were obtained using Cary 50 UV/Vis spectrophotometer.

5.1.2 X-Ray diffraction (XRD)

XRD is one of the most important techniques in materials' analysis. By carrying out the XRD, the phases of the tested materials can be identified together with their crystal structure and crystallite sizes.

In the XRD test, a sample is placed in the middle of x-ray tube and x-ray detector as shown in Figure 5.2. The x-ray tube will provide the incident x-rays and gradually move upward. This movement will change the incident angles continuously. The detector on the right will detect the diffracted x-rays.

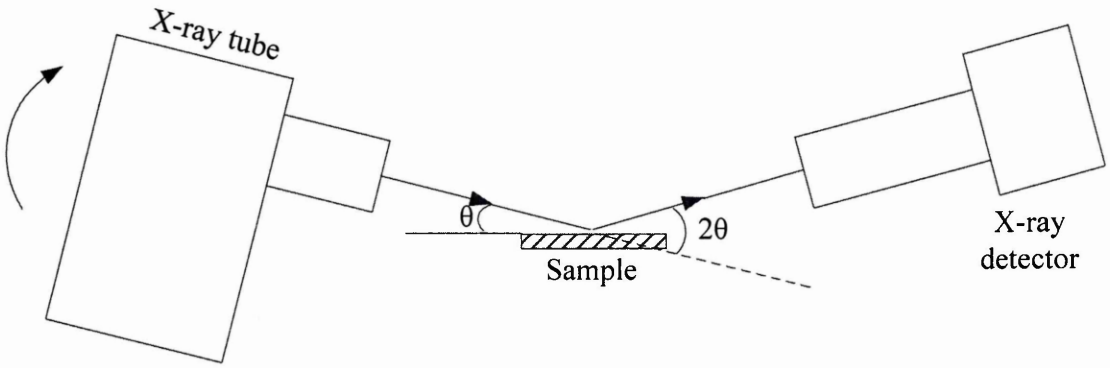

Figure 5.2: In XRD measurements, the x-ray tube will provide the incident rays while the diffracted rays are detected by the x-ray detector.

Diffraction of wave is defined as various phenomena that happen when wave travels through small opening or slit. In classical physics, the interaction between waves after passing through slits is described as interference.

Atoms in crystal lattice cause x-ray scattering and under certain conditions a large number of scattered rays either reinforce themselves (constructive interference) or cancel with each other. Figure 5.3 shows the interactions between the incident x-rays with wavelength λ and the atoms inside the crystal of solid materials. Diffraction of x-rays occurs when atoms reflect the incoming x-rays. From Figure 5.3, the length, w is equal to;

$$w = d \sin\theta \tag{5.2}$$

Where d and θ are the inter-planar spacing and the angle between the atomic plane and the x-rays beam, respectively. The path difference between the consecutive top and bottom x-rays is defined by,

$$2w = 2d \sin\theta \tag{5.3}$$

Two separate diffracted waves will undergo constructive interference, if and only if, the path difference is equal to any integer value of the wavelength, λ [3]. Then Equation (5.3) becomes,

$$n\lambda = 2d \sin\theta \tag{5.4}$$

Where n is a positive integer. Equation (5.4) is known as Bragg's Law.

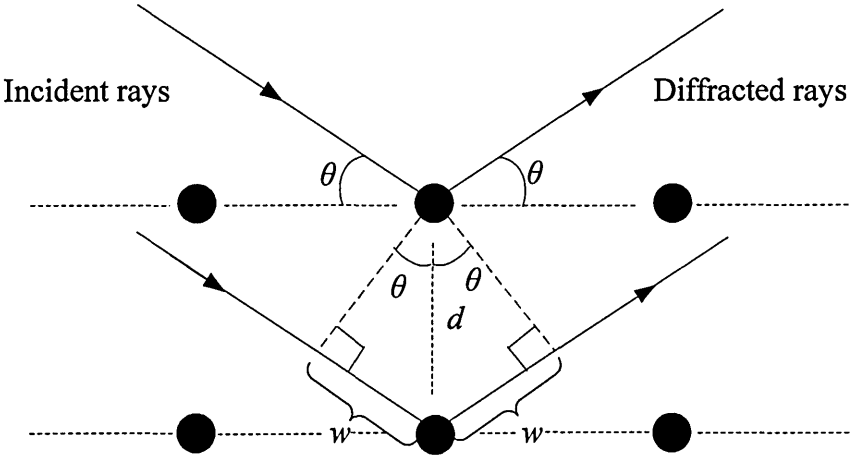

Figure 5.3: Incident and diffracted x-rays paths when they interact with atoms inside solid crystals.

The XRD output is a plot of series of peaks as shown in Figure 5.4, with the number of x-ray counts as the function of the diffraction angle, 2θ. Analysis of the full width at half maximum (FWHM) on the highest peak yields the information about the crystallite sizes (D) using the Debye-Scherrer equation as given in Equation (5.5).

$$D = \frac{0.94\lambda}{\beta \cos\theta} \tag{5.5}$$

Where D is the crystallite size (nm), λ is the wavelength of incident radiation (Å), β is the full width at half maximum (FWHM) (radian) and θ is the angle of diffraction.

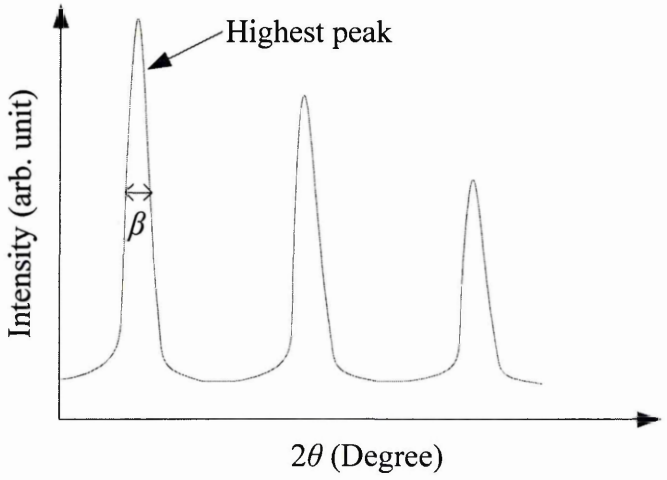

Figure 5.4: Typical output from x-ray diffraction. The highest peak is used to obtain the crystallite sizes of the sample that being tested.

XRD equipment used in this research programme is Philip X'Pert Pro with excitation wavelength of 1.5406 Å. The source voltage of 40 kV and current 40 mA were employed.

5.1.3 Photoelectrochemical (PEC) measurement

The PEC measurement is a fast and simple technique used to determine the electrical conductivity of semiconductors. This system can be calibrated using materials with known electrical conductivity. The experimental set up of the PEC measurement is shown in Figure 5.5. PEC cell is a liquid/solid junction solar cell. When a sample (semiconductor) is immersed into the electrolyte, the transfer of charge carriers between

electrolyte and the semiconductor will occur in order to achieve equilibrium. This interaction will be noticed from voltage variation at the voltmeter. When the light is turned on, the electrons in the valence band will be excited to the conduction band of the semiconductor and the readings of the voltmeter will change.

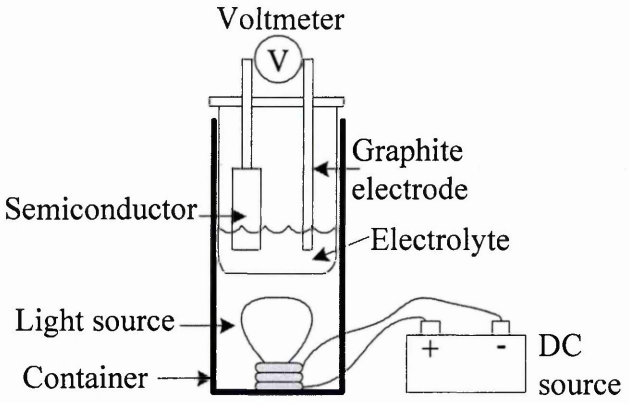

Figure 5.5: The set-up of PEC measurements showing all the essential components.

For the p-type material, the band bending will be downward. This will make the excited electrons in the conduction band roll downward to the right as shown in Figure 5.6 (a). The positive ions (H^+) will be attracted to the semiconductor's surface and discharge to form hydrogen molecules according to Equation (5.6):

$$4H^+ + 4e \rightarrow 2H_2 \tag{5.6}$$

At the graphite electrode, the hydroxide ions will release electrons and form water and oxygen molecules according to Equation (5.7).

$$4OH^- - 4e \rightarrow 2H_2O + O_2 \tag{5.7}$$

For the n-type material, the band bending will be upward. This will make the excited electrons in the conduction band roll downward to the left as shown in Figure 5.6 (b). Electrons will move from the semiconductor to the graphite electrode making the positive ions (H^+) attracted and discharge to form hydrogen molecules (refer to Equation (5.6)). While at the semiconductor's side, the water molecules will receive holes and form oxygen and hydrogen ions (refer to Equation (5.7)). Conclusively, the PEC measurement is an analogous process similar to electrolysis of water.

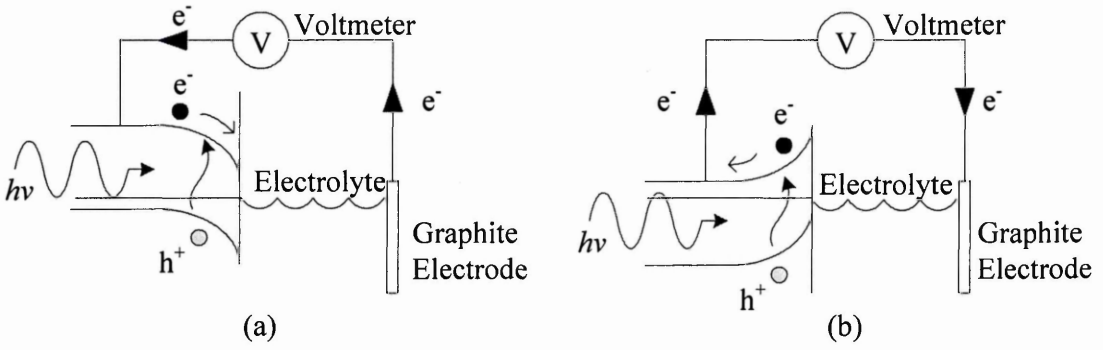

Figure 5.6: Energy band diagram of PEC cell arrangements for (a) p-type and (b) n-type semiconductor. Redrawn from [4].

If the magnitude of voltage during the light is turn on (V_L) is lower than when the light is turn off (V_D), the electrical conductivity of the semiconductor is p-type. Otherwise, it is n-type. The difference between V_L and V_D is called the PEC signal. The PEC signal is a rough indicator of doping level. If the PEC signal is high, one can say that the doping level is close to optimum value.

In this research programme the electrolyte used for obtaining PEC signal for CdS, CdTe and ZnTe samples was sodium thiosulfate ($Na_2S_2O_3$) with molarity of 0.1M.

5.1.4 X-ray fluorescence (XRF)

The x-ray fluorescence (XRF) is a technique used to determine the composition of elements in the tested samples. The composition of elements in solid, powdered or liquid form can be determined by this technique.

The principle operation of XRF can be seen in Figure 5.7. When the atoms of a sample are exposed to the x-ray source, the electrons from low energy state will absorb the photons and then get ejected to the higher energy states and create vacancies. This condition will create an unstable ion. The electrons from high energy state will move to fill in the vacancies. In order to do so, the electrons from high energy states will release the x-ray fluorescence. The x-ray fluorescence is a unique emission because difference elements will produce different emissions. The characteristic of the emitted x-ray will be analyzed by the computer and then the composition of the elements in the sample can be determined.

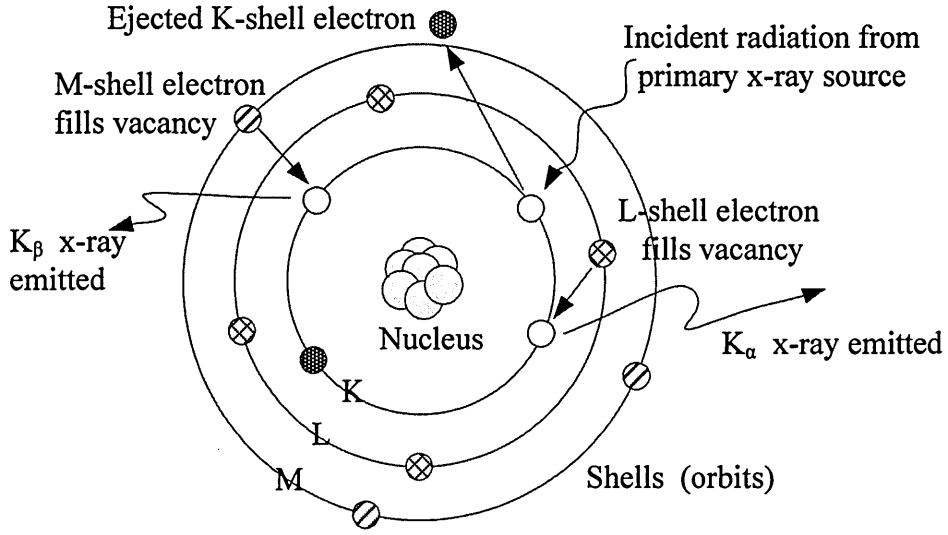

Figure 5.7: The principle of operation of x-ray fluorescence. Redrawn from [5].

Figure 5.8 shows the process of analyzing the composition in a tested sample. The x-ray is generated at the x-ray tube. When the sample is incident by the x-ray, the x-ray fluorescence will be emitted. The x-ray fluorescence will be detected and analyzed by the analyzing crystal. The analyzing crystal will diffract photons towards the detector with various wavelengths. From the detector, all of the data collected will be sent to the computer for analysis. In this study, compositional analysis of semiconducting layers was carried out using Philips Magix PRO XRF system.

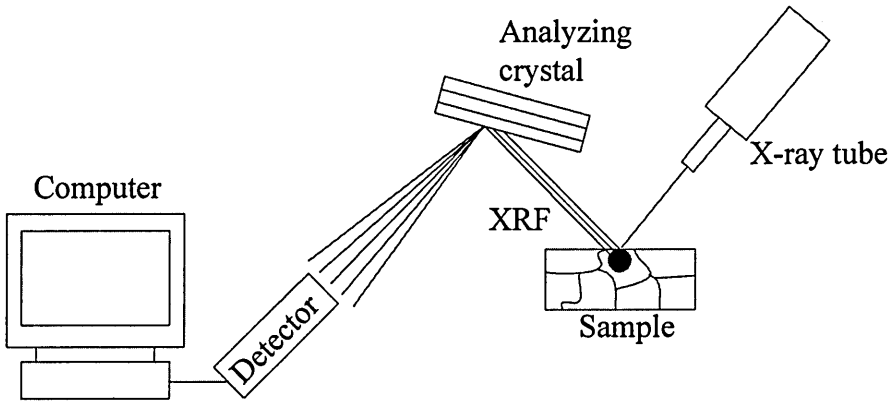

Figure 5.8: The XRF set-up showing all the essential components. Redrawn from [6].

5.1.5 Scanning electron microscopy (SEM)

In glass lens-based microscopes, the light source is focused towards samples using lenses to obtain magnifying images. In scanning electron microscope (SEM) technique, electrons are used as the 'light source'. SEM can produce high resolution and clear images with magnification up to 500 000 [7]. SEM uses electromagnets to control the magnification. Scanning process starts with the generation of electron beam by the electron gun. In SEM, accelerating voltage can vary between 2 kV to 30 kV [8]. The electron beam is accelerated towards the anode and then travels through magnetic lens where they are focused into a very small spot as shown in Figure 5.9. Next, the electron beam passes the scanning coils which deflect the electrons horizontally and vertically before hitting the sample. Once the beam hits the sample, electrons and X-rays are ejected from the sample.

The ejected electrons are detected by backscattered electron detector and secondary electron detector. The backscattered electron detector will detect the high energy electrons which are resulted from the interaction between the nuclei of atoms and the incident electrons. The low energy electrons come from the repulsion between the incident electrons and the electrons present in the sample and they will be detected by the secondary electron detector. These electrons are converted into images that can be viewed on the computer screen. Samples prepared for SEM should be electrically conductive. This is to avoid the build-up of negative charges on the sample's surface.

The non-conductive surface can be coated with carbon or gold [9]. The thickness of the conductive layer should be very thin (10 to 15 nm) so that it does not affect the image significantly. After coating, the sample will be fixed to a metallic sample holder and silver paint will be applied to the edges of the sample. This is done to 'connect' the sample with the metallic sample holder so that the build-up electrons can be dissipated. SEM results presented in this thesis were acquired using FEI Nova Nano SEM machine.

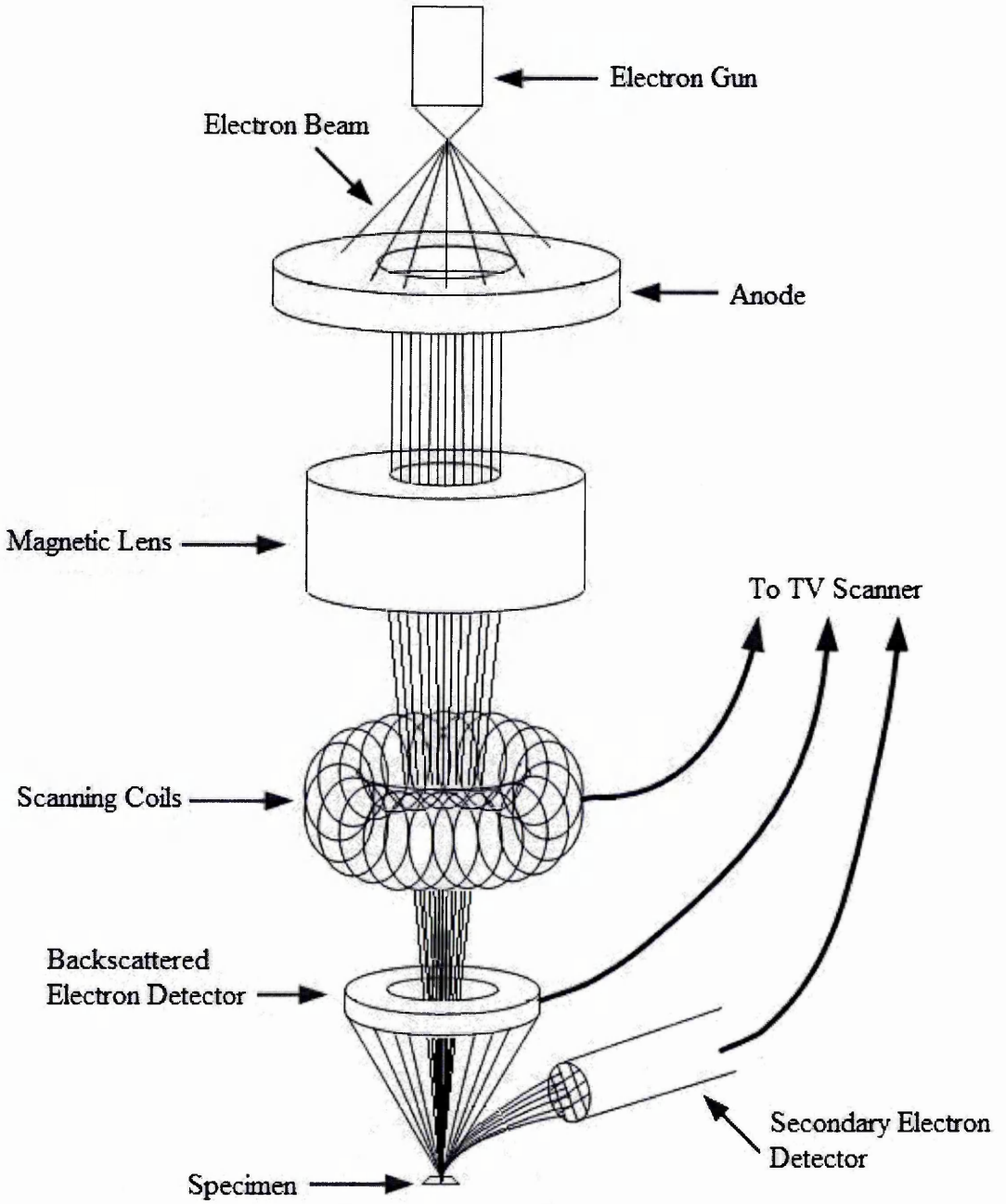

Figure 5.9: The SEM operation showing all the typical components. Redrawn from [9].

5.1.6 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is similar to SEM in some aspects. For examples, both systems need vacuum environment in order to work properly and both systems contain electron gun to produce electron beam. However, accelerating voltage for TEM is higher than SEM (up to 300 kV) [11]. Magnification of TEM images can be as high as 50×10^6 [12]. Figure 5.10 shows how TEM works.

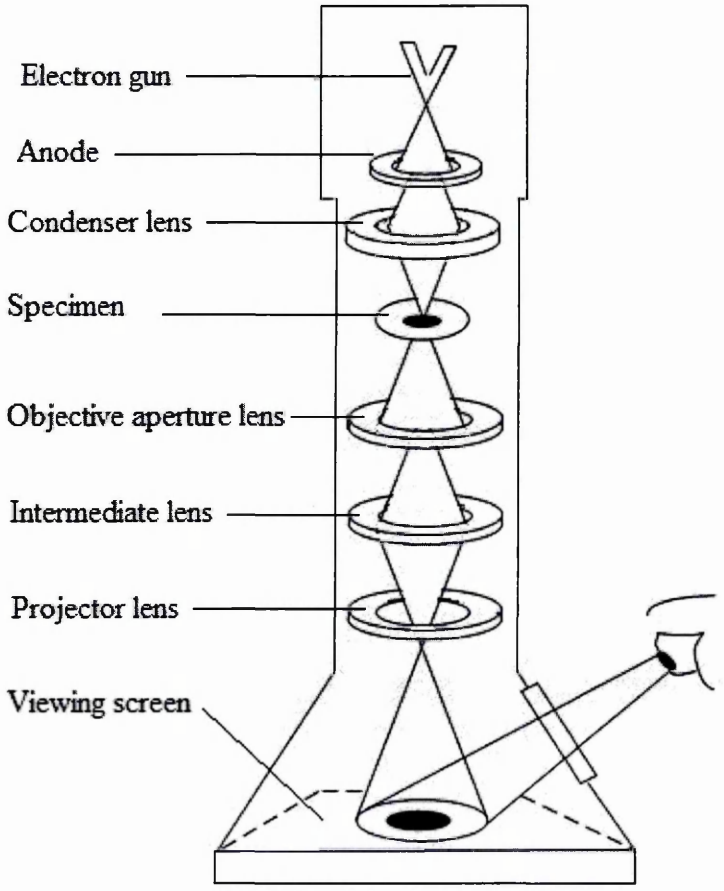

Figure 5.10: The internal view of TEM system showing its main components. Redrawn from [13].

Similar to SEM, TEM also works by means of focusing the electron beam towards the sample. However, in TEM, instead of focusing the electron beam onto tiny spot, the electron beam is illuminated on the whole sample. Sample or specimen for TEM, should be very thin (~100 nm) in order to allow the electron beam to pass through the sample and produce images. From Figure 5.10, one can see that the location of the specimen is in the 'middle' not like SEM where the specimen is positioned at the 'end'.

5.1.7 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is another technique that can be used to study the morphology of thin-film samples. Figure 5.11 shows the principle operation of AFM system.

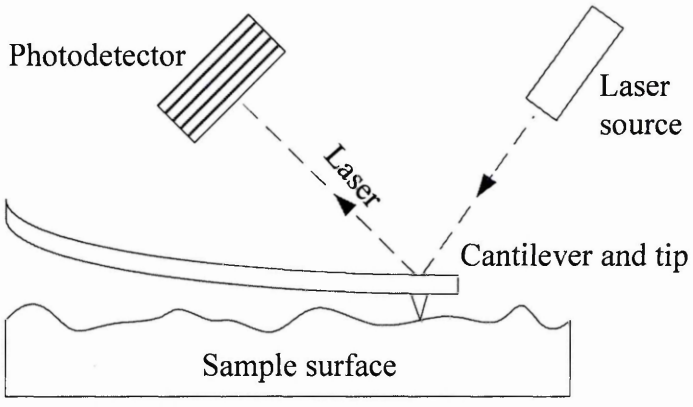

Figure 5.11: The schematic drawing showing the operating principle in AFM system.

In AFM technique, a fine tip of about 50 nm size, is used to scan the surface of a sample [14]. During the scan, the attractive and repulsive forces between the atom in the surface of the sample and the atom at the tip will deflect the cantilever. The deflection of the cantilever will affect the laser beam and any changes upon the laser path length will be detected by the photodetector. Information captured by the photodiode will be turned into electrical signal and sent to the data processing unit where the topography image is constructed.

AFM magnification can go up to 10^8 which is higher than electron microscopy techniques [14]. Unlike SEM or TEM, which can only produce 2D images, AFM can produce pseudo 3D images. The other advantage of AFM is the non-requirement of vacuum system.

5.1.8 Photoluminescence (PL)

Photoluminescence (PL) is a technique used to study the defect levels in semiconductors. In this technique, a strong light source (photon - usually a laser) is employed to excite electrons in the valence band into the conduction band. After that, the photo-excited electrons in the conduction band will fall back into the valence band. Any single electron that falls back to the valence band will emit light (luminescence). These mechanisms are depicted in Figure 5.12 (a).

Output from photoluminescence spectroscopy is in the form of spectrum consist of several peaks. The intensity of the peaks as shown in Figure 5.12 (b) is the indicator of defect density presence at a particular defect level (DL). If there are no defect levels between the conduction band and valence band, only one peak can be seen. This single

peak represents the bandgap of the investigated semiconductors. Photoluminescence is carried out at low temperatures, for example T = 77 K in order to avoid any thermally agitated electron to be present in the conduction band [15].

This technique is also useful to investigate the effects of chemical etching on the surface of semiconductors. Sobiesierski and co-workers carried out studies on effects of acidic and basic etching on n-type CdTe crystal using PL. They later discovered that the defect density on the CdTe surface can be altered by chemical etching [16].

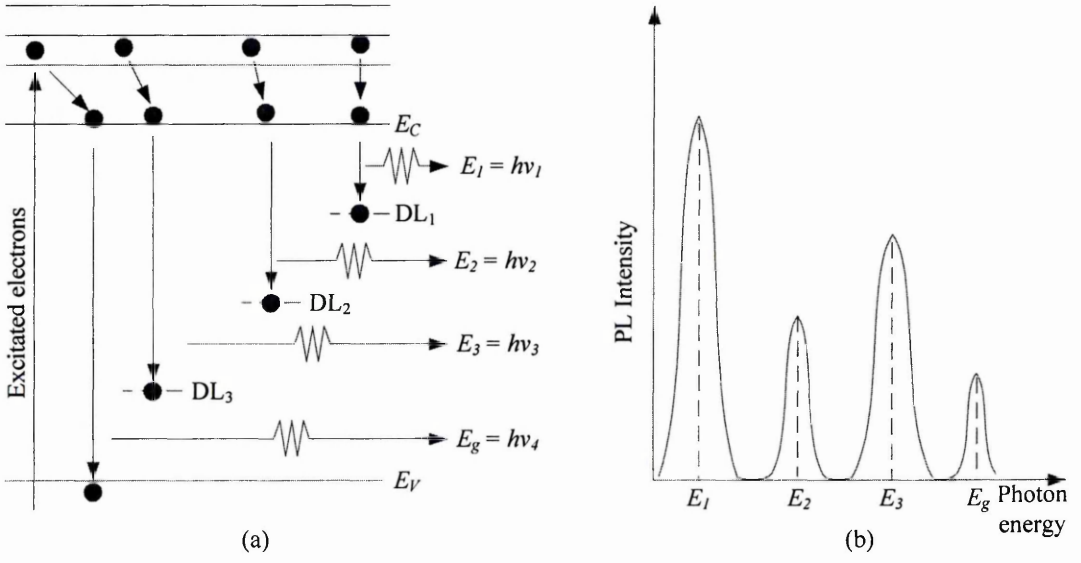

Figure 5.12: (a) Schematic diagram showing how photoluminescence technique assists in determining defect levels in the bandgap. DL_1 to DL_3 are the defect levels present in the bandgap. (b) Peak intensities showing the density of defects at various defect levels.

5.1.9 Ultra-violet photoelectron spectroscopy (UPS)

Ultra-violet photoelectron spectroscopy (UPS) is a spectroscopy technique widely used to study the band structure of semiconductors [17]. In this thesis, UPS was employed to study the position of Fermi level for as-deposited and $CdCl_2$ treated CdTe. Results of UPS study for electrodeposited CdTe will be discussed in Chapter 7.

In 1905, Albert Einstein proposed the idea of photoelectric effect. Simply, the photoelectric effect is a phenomenon where electrons are ejected from the surface of a material when it is shined by light (photons). The ejected electrons are also called photoelectrons. The kinetic energy, E_k contained in a single photoelectron is given by [18],

$$E_k = hv - \phi \quad (5.8)$$

Where,

hv is the photon energy

ϕ is the work function of the material

Equation (5.8) shows that the kinetic energy of a photoelectron depends on the energy of the incident photon. So, ultra-violet photoelectron spectroscopy operates based on this principle.

Figure 5.13 shows the principle operation of UPS. This spectroscopy technique employs low ultra-violet energy (10 eV to 45 eV) to excite photoelectrons in the valence band to vacuum level. Photoelectrons that are ejected from the surface will be detected by electron detector and computer analysis is needed to analyse the kinetic energy of the electrons. Since UPS is a surface sensitive technique, the experiments are performed in ultra-high vacuum environment (~10^{-9} Torr) to avoid any surface contamination [19].

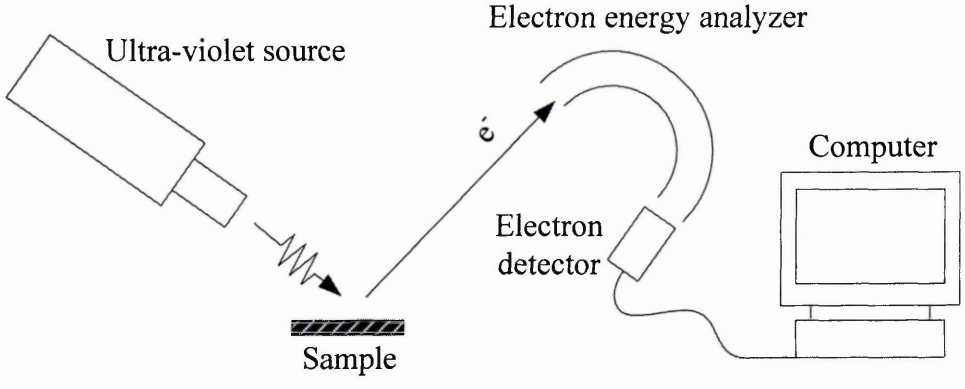

Figure 5.13: Schematic diagram showing the principle operation of UPS.

5.1.10 DC electrical measurements

Electrical resistivity and conductivity of thin film samples in this research programme were determined using DC electrical measurement. In this simple technique, computerised variable DC voltage source was applied to the semiconducting layer as shown in Figure 5.14. For example, the applied voltage can start from -1.0 V and if 0.2 V increment is set, the voltage will automatically increase to -0.8 V, -0.6 V and finally stop at 1.0 V. The value of direct current, I will be recorded at every voltage increment.

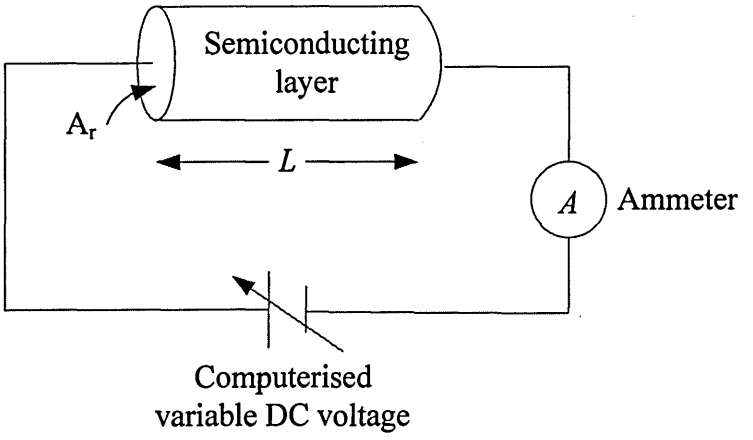

Figure 5.14: The schematic diagram of DC electrical measurement showing all the necessary components.

The linear graph showing the linear relationship between the direct current and applied direct voltage can be plotted as shown in Figure 5.15.

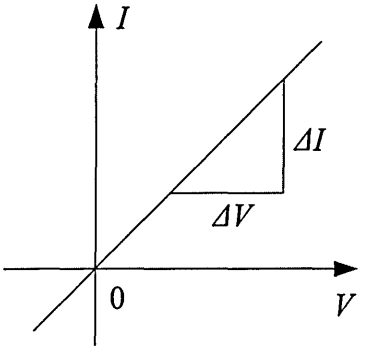

Figure 5.15: Linear curve showing the relationship between direct current and voltage.

The resistance of semiconductor, R (Ω) can be calculated from Ohm's Law as shown in Equation (5.9). Where,

$$R = \frac{\Delta V}{\Delta I} \tag{5.9}$$

The resistivity of semiconductor, ρ (Ωcm) can be calculated from Equation (5.10) [20]. Where A_r (cm^2) and L (cm) are the surface area and the thickness of the semiconducting layer respectively,

$$\rho = \frac{RA_r}{L} \tag{5.10}$$

The conductivity (Scm^{-1}) of the semiconducting layer, σ can be determined by taking the reciprocal of ρ. The accuracy of this technique mainly depends on the quality of low-resistance ohmic contact made to the semiconducting layer.

5.2 Device characterisation techniques

After the optimisation of all semiconducting layers with the aid of characterisation techniques, solar cell fabrication would soon follow. The fabrication of CdTe based solar cells will further be discussed in Chapter 9. This sub-section will present the device characterisation techniques conventionally used to assess the performance of lab-scale solar cell devices. Only two characterisation techniques are presented here which is the current-voltage (I-V) measurement and the capacitance-voltage (C-V) measurement.

5.2.1 Current-voltage (I-V) measurement

Current voltage (I-V) measurement is the most important technique in photovoltaic devices evaluation. Current-voltage measurement is divided into two conditions. As a start, the current-voltage measurement was carried out under dark condition. However, the conversion efficiency of a solar cell can't be determined under dark condition. So, the measurement under illuminated condition is carried out to observe the photo-activity of the cell and determine the conversion efficiency.

5.2.1.1 Measurement under dark condition

Under dark condition, any solar cell will behave like an ordinary diode. Figure 5.16 shows the assessment of a Schottky barrier type, ideal solar cell under dark condition. When an external voltage is applied across the solar cell, it will experience high current only in forward biasing. During reverse biasing, the current measured should be very low or zero.

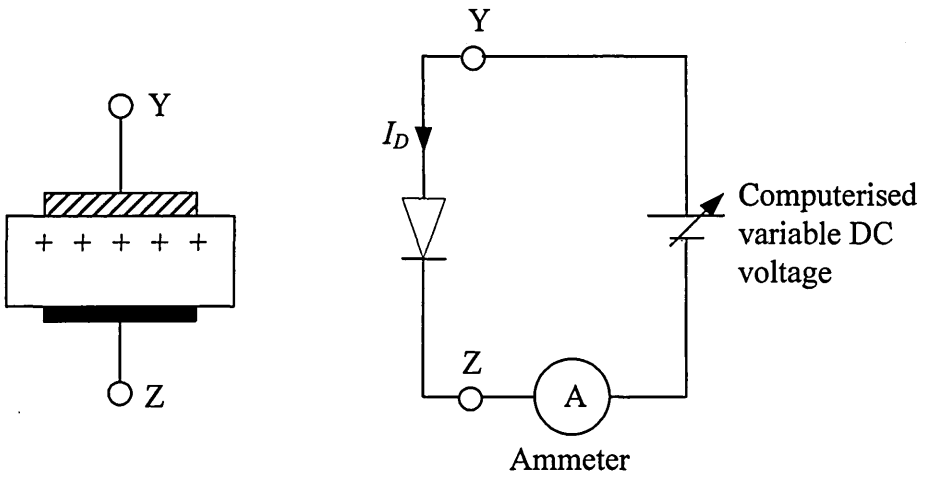

Figure 5.16: (a) Schematic diagram of an ideal Schottky barrier solar cell and (b) the equivalent circuit when evaluated under dark condition.

In dark condition, diode behaviour was represented by Equation (2.6) in Chapter 2. This equation is renamed as Equation (5.11) for easy reference.

$$I_D = SA^*T^2\exp\left(\frac{-q\emptyset_b}{kT}\right)\cdot\left[e^{\left(\frac{qV}{nkT}\right)}-1\right] \tag{5.11}$$

Where,

I_D is the dark current (A)

A^* is effective Richardson constant for thermionic emission ($Acm^{-2}K^{-2}$)

n is the ideality factor of the diode

S is the contact area (cm^2)

V is the applied voltage (V)

or,

$$I_D = I_0\cdot\left[\exp^{\left(\frac{qV}{nkT}\right)}-1\right] \tag{5.12}$$

where $I_0 = SA^*T^2\exp^{\left(\frac{-q\emptyset_b}{kT}\right)}$ is the reverse saturation current. For external voltage applied at 75 mV or higher ($V \geq 75$ mV),

$$\exp^{\left(\frac{qV}{nkT}\right)} \gg 1 \tag{5.13}$$

So, Equation (5.13) can be simplified as,

$$I_D = I_0 \cdot \left[\exp^{\left(\frac{qV}{nkT}\right)}\right] \tag{5.14}$$

By taking natural logarithm for both sides, Equation (5.14) can be arranged as,

$$\ln I_D = \frac{qV}{nkT} + \ln I_0 \tag{5.15}$$

Converting Equation (5.15) into base-ten logarithmic form reveals,

$$2.303 \log_{10} I_D = \left(\frac{q}{nkT}\right) V + 2.303 \log_{10} I_0 \tag{5.16}$$

For convenience, Equation (5.16) is divided by 2.303. Equation (5.16) is rewritten as,

$$\log_{10} I_D = \left(\frac{q}{2.303nkT}\right) V + \log_{10} I_0 \tag{5.17}$$

A plot of $\log_{10} I_D$ versus applied voltage (V) is shown in Figure 5.17. The rectification factor (RF) is defined as the ratio between forward bias current, I_F and reverse bias current, I_R at a particular voltage (for example $V = 1$ V). So, RF = $I_F \div I_R$. Typical value for an efficient solar cell should be at least ~10^3 [21].

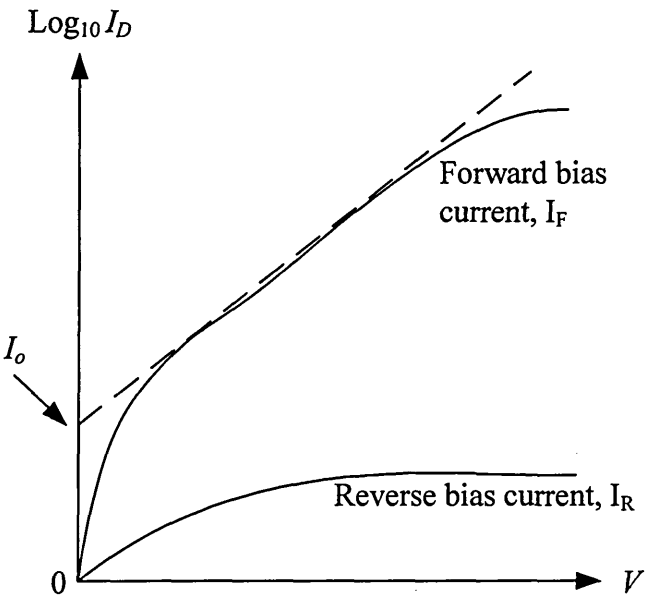

Figure 5.17: The log-linear I-V curves for solar cell measured in the dark. The values of reverse bias current have been changed to positive for easy comparison. Current values are in log scale while voltage values are represented in linear scale.

The ideality factor (n) can be determined from the straight line portion in Figure 5.17;

$$\text{Gradient} = \left(\frac{q}{2.303nkT}\right) \tag{5.18}$$

In practical devices, the value of n is between 1.00 and 2.00. If the current transport through potential barrier is only dominated by thermionic emission, the value of n is 1.00. If the metal-semiconductor interface is full of recombination & generation (R&G) centres, and the current transport is only by R&G process, the value of n becomes 2.00 [21].

The determination of barrier height, ϕ_b is carried out by using Equation (5.17) and (5.19). Intersection of the $\log_{10} I_D$ axis with the highest gradient provides a more accurate value for I_0.

$$I_0 = SA^*T^2\exp\left(\frac{-q\phi_b}{kT}\right) \tag{5.19}$$

5.2.1.2 Measurement under illuminated condition

Measurement under illuminated condition is the most important assessment in solar cells research and development activities. Only by carrying out this measurement, the efficiency of a solar cell can be determined. Under illuminated condition, a solar cell can be treated as a diode having a current source. Figure 5.18 shows the equivalent circuit of an ideal Schottky barrier solar cell under illumination together with its equivalent circuit.

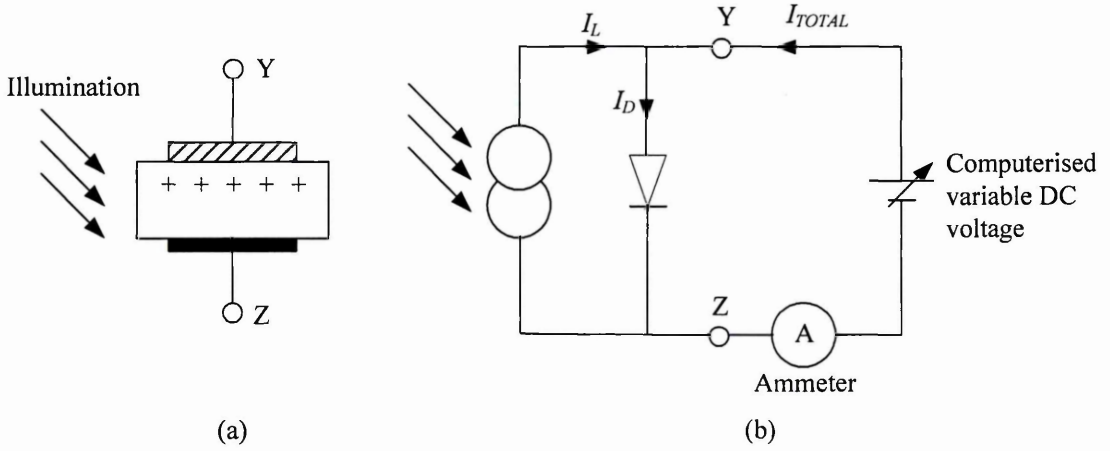

Figure 5.18: (a) Schematic diagram of an ideal Schottky barrier solar cell and (b) the equivalent circuit when evaluated under illuminated condition.

Therefore the total current flow in the device is given by Equation (5.20);

$$I_{TOTAL} = I_D - I_L = I_0 . \exp^{\left(\frac{qV}{nkT}\right)} - I_L \qquad (5.20)$$

Equation (5.12) and (5.20) are plotted together in Figure 5.19. Notice that the horizontal axis is the representation of the applied voltage, V. There are three important parameters need to be considered in solar cells assessment.

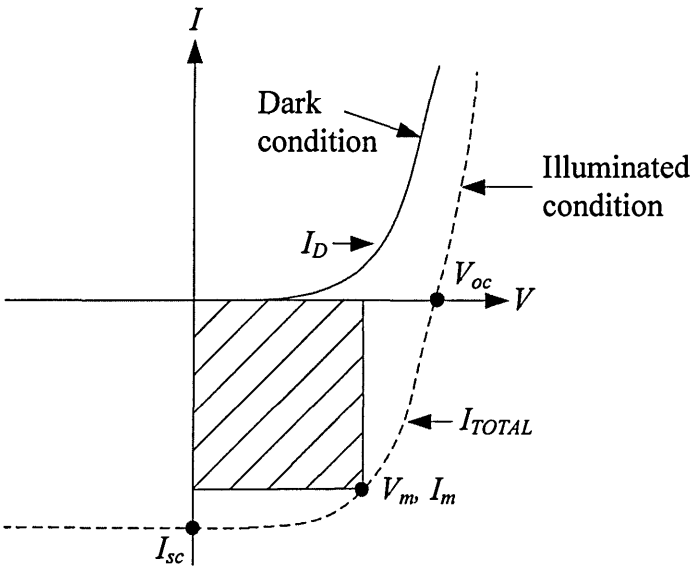

Figure 5.19: Linear-linear I-V curves showing the characteristics of a solar cell under dark and illuminated conditions.

(a) Short circuit current, I_{sc} (A) is measured when the two contact are short circuited or when there is zero voltage across two contacts. This is simply, $I_L = I_{sc}$ and conventionally expressed as short circuit current density, J_{sc} ($mAcm^{-2}$) to make any easy comparison between devices with different contact sizes.

(b) Open circuit voltage, V_{oc} (V) is the voltage measured when there is no current flow in the external circuit which means I_{TOTAL} equals to zero. From Equation (5.20),

$$0 = I_0 . \exp^{\left(\frac{qV_{oc}}{nkT}\right)} - I_L \tag{5.21}$$

Substituting $I_0 = SA^*T^2\exp^{\left(\frac{-q\emptyset_b}{kT}\right)}$ reveals,

$$SA^*T^2\exp^{\left(\frac{-q\emptyset_b}{kT}\right)} \cdot \exp^{\left(\frac{qV_{oc}}{nkT}\right)} = I_L \tag{5.22}$$

For convenience, I_L is substituted with I_{sc} and Equation (5.22) is expressed in current density. By taking natural logarithm at both sides,

$$\ln \exp^{\left(\frac{-q\emptyset_b}{kT}\right)} \cdot \ln \exp^{\left(\frac{qV_{oc}}{nkT}\right)} = \ln\left(\frac{J_{sc}}{A^*T^2}\right) \tag{5.23}$$

$$\frac{q}{kT}\left(-\frac{\emptyset_b}{1}+\frac{V_{oc}}{n}\right)=\ln\left(\frac{J_{sc}}{A^*T^2}\right) \tag{5.24}$$

$$V_{oc}=n\left[\emptyset_b+\frac{kT}{q}\ln\left(\frac{J_{sc}}{A^*T^2}\right)\right] \tag{5.25}$$

Equation (5.25) shows that the V_{oc} is influenced by n, ϕ_b, J_{sc} and T. Obviously, the high value of n is desirable to obtain high V_{oc}. But in practice, the high value of n (for example, n = 2.00) will create more R&G problems which is not helpful in transporting more charge carriers through the external circuit. The value of n between 1.00 and 2.00 is desirable in this case. Increasing ϕ_b will also increase the V_{oc}. One of the ways to achieve it is by incorporating insulator between metal and semiconductor. This interface is known as metal-insulator-semiconductor interface (MIS) [22]. The side by side comparison of band diagram for MS and MIS are shown in Figure 5.20.

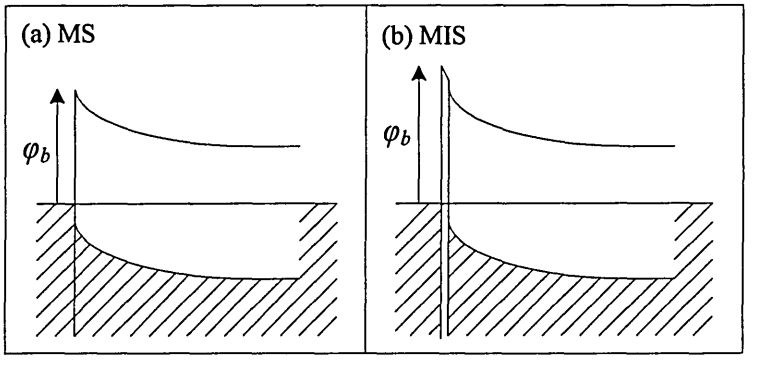

Figure 5.20: Incorporating insulator between metal and semiconductor to increase φ_b.

(c) The fill factor, FF is define as,

$$FF=\frac{V_m I_m}{V_{oc} I_{sc}}=\frac{P_m}{V_{oc} I_{sc}} \tag{5.26}$$

where V_m and I_m are the maximum voltage and current respectively. Both values represent a point on I_{TOTAL} curve in Figure 5.19, indicating the highest power that can be delivered to the load. Finally, the efficiency of a solar cell is calculated by using Equation (5.27).

$$\eta = \frac{V_{oc}J_{sc}FF}{P_{in}} \times 100 \quad (5.27)$$

Where, P_{in} is the input power per unit area (0.1 Wcm^{-2}) under AM1.5 condition.

It is noteworthy that up till now, the discussions only concentrated on an ideal solar cell. However, in practical devices, the existence of shunt resistance, R_{sh} and series resistance, R_s is inevitable. So the equivalent circuit should also include these parameters. Figure 5.21 shows the equivalent circuit of a solar cell under illumination with the inclusion of R_{sh} and R_s. Shunt resistance is associated with the leakage paths present in a solar cell while the series resistance is an indication of internal resistance that naturally exist in any electronic device.

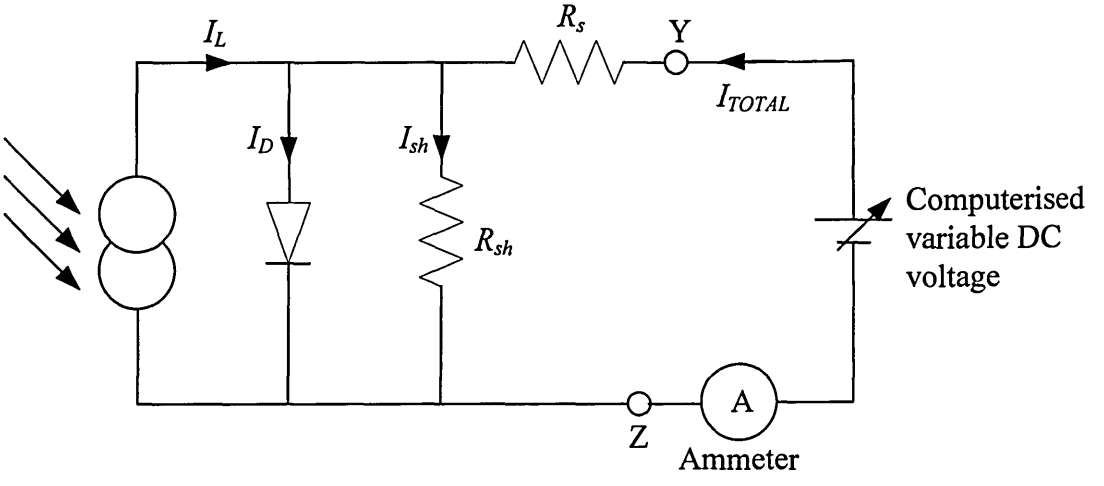

Figure 5.21: Equivalent circuit of a practical solar cell showing shunt resistance, R_{sh} and series resistance, R_s.

Figure 5.22 shows I-V curve where the estimation of R_s and R_{sh} values can be made using Ohm's Law (Equation 5.7). Series resistance can be determined by calculating the gradient of I-V curve when a diode is forward biased (first quadrant), while shunt resistance is calculated when the diode is in reverse bias condition (third quadrant).

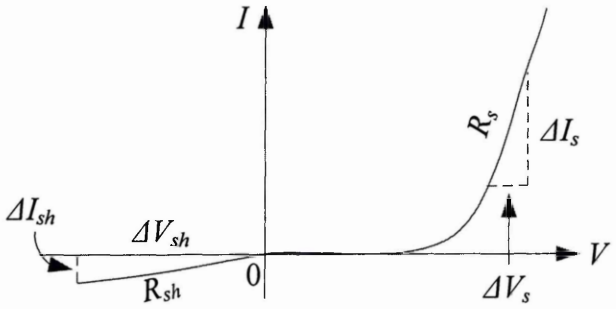

Figure 5.22: Determination of R_s and R_{sh} using Ohm's Law with the aid of I-V curve.

Both parameters are related to the fill factor of a solar cell. Maximizing the values of R_{sh} (ideally $R_{sh} \rightarrow \infty$) and minimizing R_s (ideally $R_s \rightarrow 0$) will improve the fill factor. Figure 5.23 shows how R_{sh} and R_s affect the I-V curve.

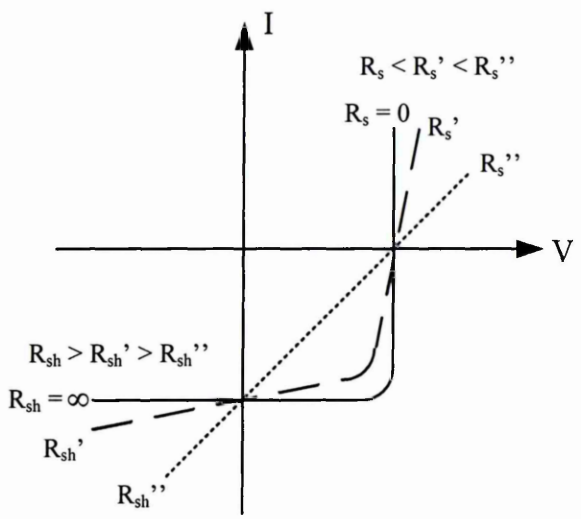

Figure 5.23: Detrimental effects of low R_{sh} and high R_s in solar cells. Redrawn from [21]

5.2.2 Capacitance-voltage (C-V) measurement

Capacitance-voltage (C-V) measurement is the other essential technique used in characterisation of diodes. By utilizing C-V measurement, the doping concentration, potential barrier height and width of depletion region can be determined. Positive and negative charges that exist side by side in p-n junction or Schottky diode are analogous to parallel plate capacitors. The capacitance, C (in F) of a depletion layer is defined as,

$$C = \frac{\varepsilon_S A_r}{W} \tag{5.28}$$

Where,

$\varepsilon_s = \varepsilon_o \varepsilon_r$ is the permittivity of semiconducor (Fcm^{-1})

ε_o = is the permittivity of free space (8.85×10^{-14} Fcm^{-1})

ε_r = is the relatif permittivity

A_r is the contact area (cm^2)

W is the width of depletion region (cm)

If capacitance is described in capacitance per unit are (C_A), Equation (5.28) becomes,

$$C_A = \frac{C}{A_r} = \frac{\varepsilon_S}{W} \tag{5.29}$$

The depletion region width, W for an abrupt p^+-n junction was described in Chapter 2 as [18],

$$W = \left[\frac{2\varepsilon_S V_{bi}}{qN_d}\right]^{\frac{1}{2}} \tag{5.30}$$

By substituting Equation (5.30) into Equation (5.29),

$$\frac{C}{A_r} = \frac{\varepsilon_S}{\sqrt{\frac{2\varepsilon_S V_{bi}}{qN_d}}} \tag{5.31}$$

$$C_A = \sqrt{\frac{qN_d\varepsilon_S}{2V_{bi}}} \tag{5.32}$$

Equation (5.32) should be slightly modified to accommodate the external applied voltage, V. Thus,

$$C_A = \sqrt{\frac{qN\varepsilon_S}{2(V_{bi} - V)}} \tag{5.33}$$

$$C_A = \sqrt{\frac{qN\varepsilon_s}{2}}\,(V_{bi} - V)^{-\frac{1}{2}} \tag{5.34}$$

In Equation (5.34), N is known as the uncompensated carrier density. For p-type semiconductors, $N = N_a - N_d$ but for n-type semiconductors, $N = N_d - N_a$. The plot of C_A versus applied voltage is depicted in Figure 5.24 [23]. The value of capacitance per unit area (C_0), when $V = 0$ indicates the capacitance in the depletion region when zero bias is asserted upon the diode. After obtaining C_0, the width of depletion region can be determined using Equation (5.29).

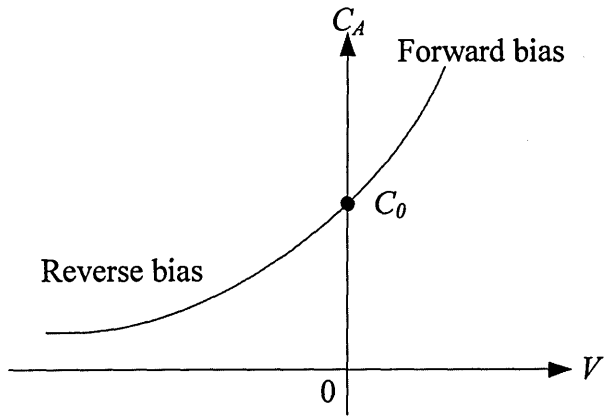

Figure 5.24: Plot of capacitance per unit area, C_A versus applied voltage, V. The value of C_0 is useful in obtaining the width of depletion region. Redrawn from [23].

To acquire the doping concentration and built in voltage (V_{bi}), the solution for $1/C^2$ must be derived first. From Equation (5.33),

$$C_A^2 = \frac{qN\varepsilon_s}{2(V_{bi}-V)} \tag{5.35}$$

$$\frac{1}{C^2} = \frac{2}{qN\varepsilon_s A^2}(V_{bi} - V) \tag{5.36}$$

A graph $1/C^2$ versus V can be plotted as shown in Figure 5.25. The graph is known as Schottky-Mott plot [24]. From Schottky-Mott plot, the value of V_{bi} can be determined from the intersection when $1/C^2 = 0$.

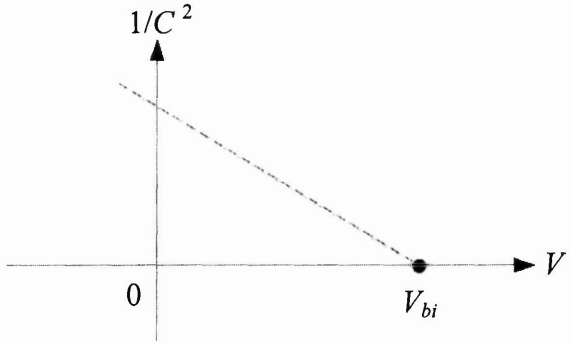

Figure 5.25: Schottky-Mott plot of an ideal diode showing the intersection at $1/C^2 = 0$ where V_{bi} is obtained.

If Equation (5.36) is differentiated with respect to V, we will obtain,

$$\frac{d\left(\frac{1}{C^2}\right)}{dV} = -\frac{2}{qN\varepsilon_s A^2} \tag{5.37}$$

By acquiring the slope of Schottky-Mott plot manually, the doping concentration of the diode can be determined using Equation (5.37).

5.3 Summary

This chapter has unveiled the materials and devices' characterisation techniques that have been utilized throughout this research programme. The studies of optical, structural, morphological and electrical conductivity are some examples of important properties of materials that are worth studying in order to optimize semiconducting layers intended for solar cells fabrication.

After the optimisation of semiconducting layers, thin film solar cells were fabricated using the knowledge obtained from materials characterisations. This is to ensure good quality materials were used for solar cells fabrication. Fully fabricated solar cells will have to be evaluated using I-V measurement in order to optimize device processing steps. C-V measurement is also essential in device assessment works in order to see the optimum doping concentration.

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6.1 Introduction

Cadmium sulphide (CdS) is a wide bandgap semiconducting layer normally used as the hetero-junction partner in CdTe based solar cells. As presented in Chapter 3, CdTe solar cell has two structures. The first structure is called substrate, which means solar cells fabrication starts from the absorber layer. In the second structure, the superstrate, fabrication of solar cells starts from the window layer. In both cases, CdS is the layer that facing the light.

One of the important properties for semiconducting materials to be used as a window layer is, it must be a wide bandgap material. This is to allow high energy photons from the ultra-violet region to be absorbed by the window layer while low energy photons from visible and infra-red region will be absorbed by the low bandgap absorber material. CdS is a binary compound semiconductor from II-VI group in periodic table with a bandgap of 2.42 eV [1]. Other semiconductors have also been tried as the window layer in CdTe based solar cell. For examples, ZnS, $Cd_{(1-x)}Zn_xS$ and ZnO [2-4]. However, highly efficient devices (> 15%) usually have CdS as the window layer as reported by Bosio *et al*, Britt and Ferekides and Dharmadasa *et al* [5-7].

In the literature, there are several deposition techniques that have been used to deposit CdS. Among these techniques are spray pyrolysis [8], sputtering [9], metal organic chemical vapour deposition (MOCVD) [10], chemical bath deposition (CBD) [11], etc. Currently, chemical bath deposited CdS (CBD-CdS) is the best layer for thin film solar cells application. It is because, in this technique, deposition happens by means of chemical reaction between the ions inside a chemical solution. When the reaction stops, CdS layer will adhere firmly onto its substrate with almost no voids (pinholes) between the grains. In addition to that, CBD is also a low-cost technique and easy for scaling-up. On the other hand, CBD produces lots of toxic waste after the deposition completed. Managing waste that contains toxic elements such as cadmium from a batch process is tedious and expensive.

To minimize waste from CdS deposition and at the same time preserving the low cost and scalable advantages of CBD, it is therefore necessary to find an alternative way to deposit CdS layers. In this project electrodeposition is a technique of choice to

deposit CdS window layer. This is due to the fact that electrodeposition is a continuous process with low temperature deposition, scalable and produces minimum waste.

In this research programme, all the electrodeposition works were carried out using 2-electrode system. This means the reference electrode was omitted. The decision was taken due to several reasons that have been stated earlier in Chapter 4.

6.2 Preparation of CdS electrolyte

To electrodeposit CdS, two chemical solutions containing the source of Cd and S ions were prepared separately. The first solution that contains 0.3M $CdCl_2.H_2O$ was prepared in a 300 ml beaker containing deionised water. $CdCl_2$ serves as the Cd source. The pH of the bath was adjusted to 2.00 ± 0.02 using diluted HCl and NH_4OH. This newly prepared $CdCl_2$ bath was stirred overnight. The source of sulphur comes from 0.6M $Na_2S_2O_3$ which was diluted in 100 ml of deionised water in a separate volumetric flask. Both chemicals were purchased from Fisher Scientific, United Kingdom and were used as received.

All of the semiconducting layers used in this project were deposited on transparent fluorine doped tin oxide (SnO_2:F - FTO). The substrates were prepared by cleansing in soap solution, methanol and acetone. Deionised water was used between these cleaning agents for rinsing purposes. The substrates were dried under a stream of nitrogen gas between 5 to 10 seconds before being tied-up to a carbon rod with PTFE tape. In this project, high purity (99.995%) carbon rod was used as the anode while the glass/FTO was used as the cathode/substrate. A DC voltage was provided using Princeton Applied Research Model 362 potentiostat.

In term of stability, the bath needs to be filtered at least once a month to remove the sulphur precipitates. After the sulphur precipitates are removed, the electrolyte can be used as normal.

6.3 Results and discussions

6.3.1 Voltammogram

Prior to deposition of CdS layers, 0.2 ml of $Na_2S_2O_3$ was added into $CdCl_2$ bath using a pipette. Cyclic voltammetry was carried out with the aid from Gillac

computerised potentiostat (ACM Instruments) to determine the suitable deposition voltage range (or deposition window). Figure 6.1 shows the voltammogram of 0.3M $CdCl_2$ containing 0.2 ml of $Na_2S_2O_3$. The voltammogram of the bath was recorded at the temperature of ~80°C with the scan rate of 3 mVs^{-1}.

According to analysis reported by Rami *et al* and Sasikala *et al* [12-13], reduction of SO_3^{2-} ions happened at lower cathodic potentials while the reduction of Cd^{2+} ions occurred at the higher cathodic potentials. The complete reaction for the formation of CdS compound is given by Fatas *et al* [14];

$$Cd^{2+} + S_2O_3^{2-} + 2e^- \rightleftharpoons CdS + SO_3^{2-} \quad (6.1)$$

From the voltammogram, the suitable voltage range for the formation of near stoichiometric CdS was identified to be between 1300 mV to 1500 mV. During the reverse cycle, the dissolution of elemental cadmium and cadmium from CdS starts at ~1260 mV (point A) while the dissolution of elemental sulphur occurs at ~520 mV (point B).

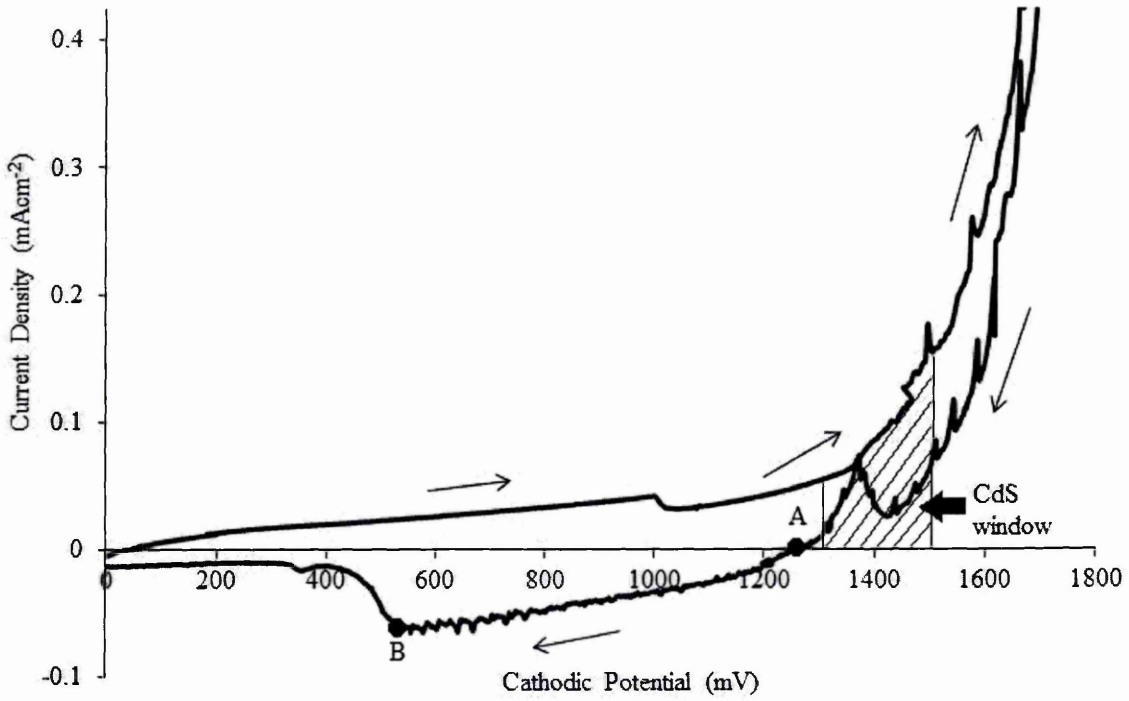


Figure 6.1: A typical cyclic voltammogram for an electrolyte containing 0.3M of $CdCl_2$ and 0.2 ml of 0.6M $Na_2S_2O_3$ at pH = 2.00 ± 0.02 and temperature of ~80°C.

The noise on the cyclic voltammogram could be associated with the instability of the electrod potential in 2-electrode system. Alternativr explanation is the effect of hydrogen bubbling on the cathode.

6.3.2 Visual appearance

After the deposition window has been determined, several samples were grown from 1300 mV to 1540 mV to see the appearance and quality of the electrodeposited CdS layers. Figure 6.2 shows the visual appearance of 14 samples which were grown at different cathodic potentials (V_g).

It is obvious from Figure 6.2 that the bright yellow colour of CdS layers only can be seen when the voltages are equal or higher than 1400 mV. At 1300 mV the colour of the electrodeposited layer was light yellow meaning the correct stoichiometry between cadmium and sulphur was not yet achieved. At 1460 mV, the CdS layers appear to be a mixture of yellow-green colour. This colour mixture is due to the Cd-richness presence in that layer.

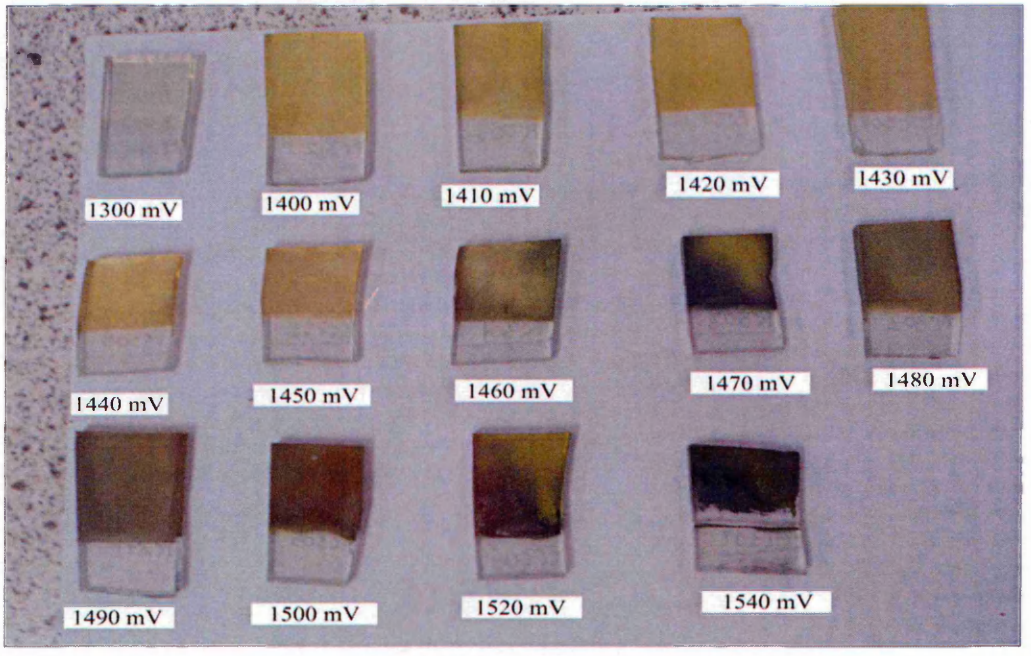


Figure 6.2: Electrodeposited CdS layers showing the colour transition due to the increase in deposition voltages.

Further increasing of the cathodic potentials resulted in more greenish colour of the electrodeposited layers. Careful observation of the sample grown at 1500 mV

reveals that there are small holes on it, which means this layer had cadmium dendrites due to the very high cadmium content in the layer. Increasing the deposition voltage beyond 1500 mV will encourage more 'peeling-off' of the electrodeposited layers from the substrate's surface. This is the indication that the deposition voltage should be no higher than 1490 mV.

From this result, the deposition window can be further narrowed down to just 50 mV, starting from 1440 mV to 1490 mV. Further optimisation of the electrodeposited CdS layers were carried out with the assistance from XRD and optical spectroscopy.

6.3.3 X-ray diffraction

Figure 6.3 shows the XRD patterns for as deposited CdS layers grown at different cathodic potentials. At these different cathodic potentials, all samples showed polycrystalline nature with poor crystallinity.

The XRD patterns in Figure 6.3 were compared with Joint Committee on Powder Diffraction Standards (JCPDS) file no. 01-075-1545 to confirm the hexagonal structure of the as-deposited CdS layers. The highest peak can be seen at 26.6°, representing hexagonal (002)H plane. However, for crystallites size analysis, this peak was ignored because it coincides with the FTO peak at the same angle [15]. So the next highest peak at 28.3°, corresponds to hexagonal (101)H peak was chosen to determine the crystallite sizes. Other peaks that correspond to hexagonal planes are (100)H and (110)H which have occurred at 24.8° and 43.7° respectively.

The cubic phases also present in these as-deposited layers. The evidence can be seen from the two peaks at 30.8° and 44.1°. Both peaks represent (200)C and (220)C planes respectively according to JCPDS file no. 01-075-0581. The cubic peak at 30.8 obtained the highest intensity when the V_g was 1450 mV. The existence of sulphur phase is also observed in the layers. This argument is supported by the co-existence of (044)O orthorhombic sulphur peak that can be seen at 31.8°.

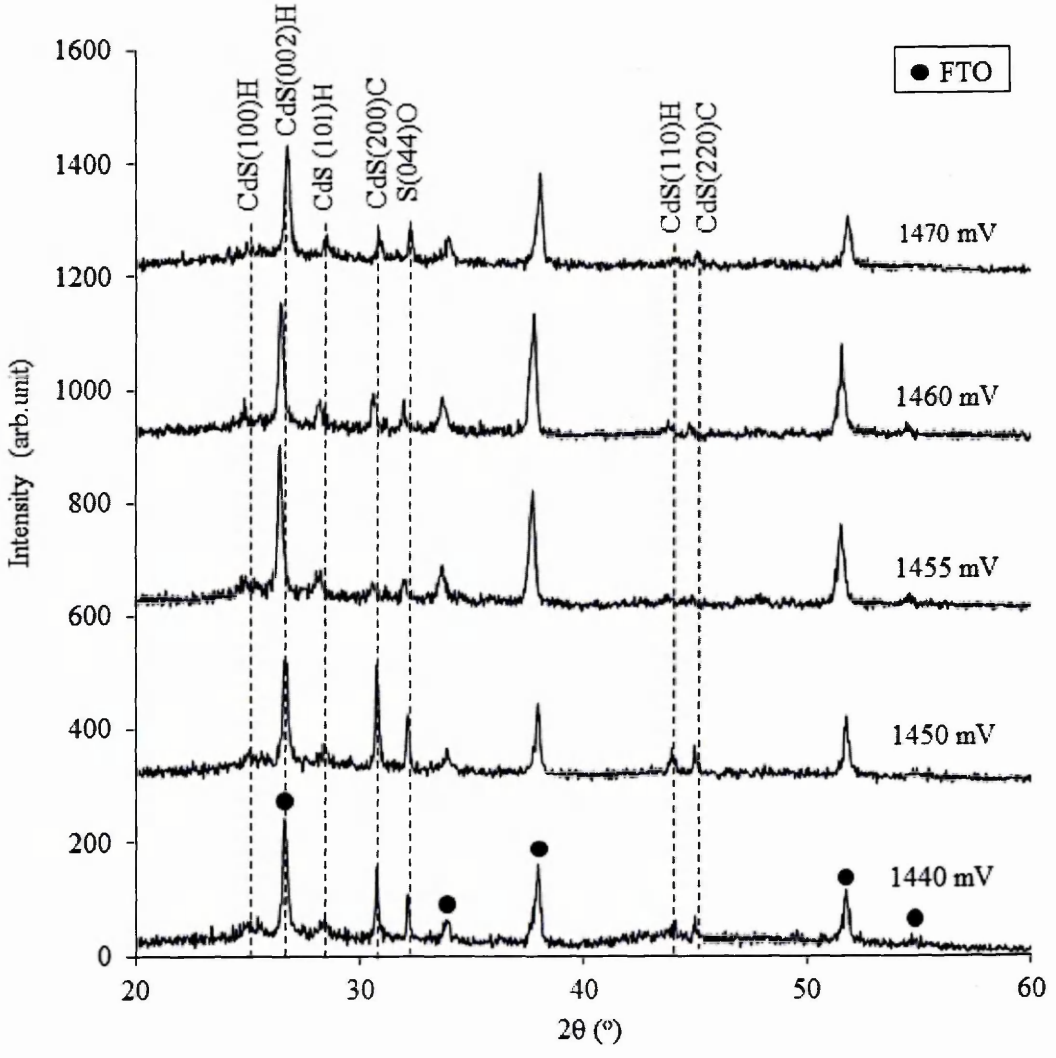


Figure 6.3: The XRD patterns of as-deposited CdS samples grown at different cathodic potentials.

However, the intensity of these peaks seemed controllable through cathodic potential. By applying higher cathodic potentials (V_g > 1450 mV), the intensity of cubic phase peaks and sulphur peak could be reduced. This is because, at higher cathodic potentials, more cadmium was deposited onto the layers, thus reducing the sulphur content. Metin and Esen have also reported that as-deposited CdS from chemical bath deposition had a mixture of cubic and hexagonal CdS [16]. All of the samples in Figure 6.3 were annealed at 400°C for 20 minutes in air and the results are shown in Figure 6.4.

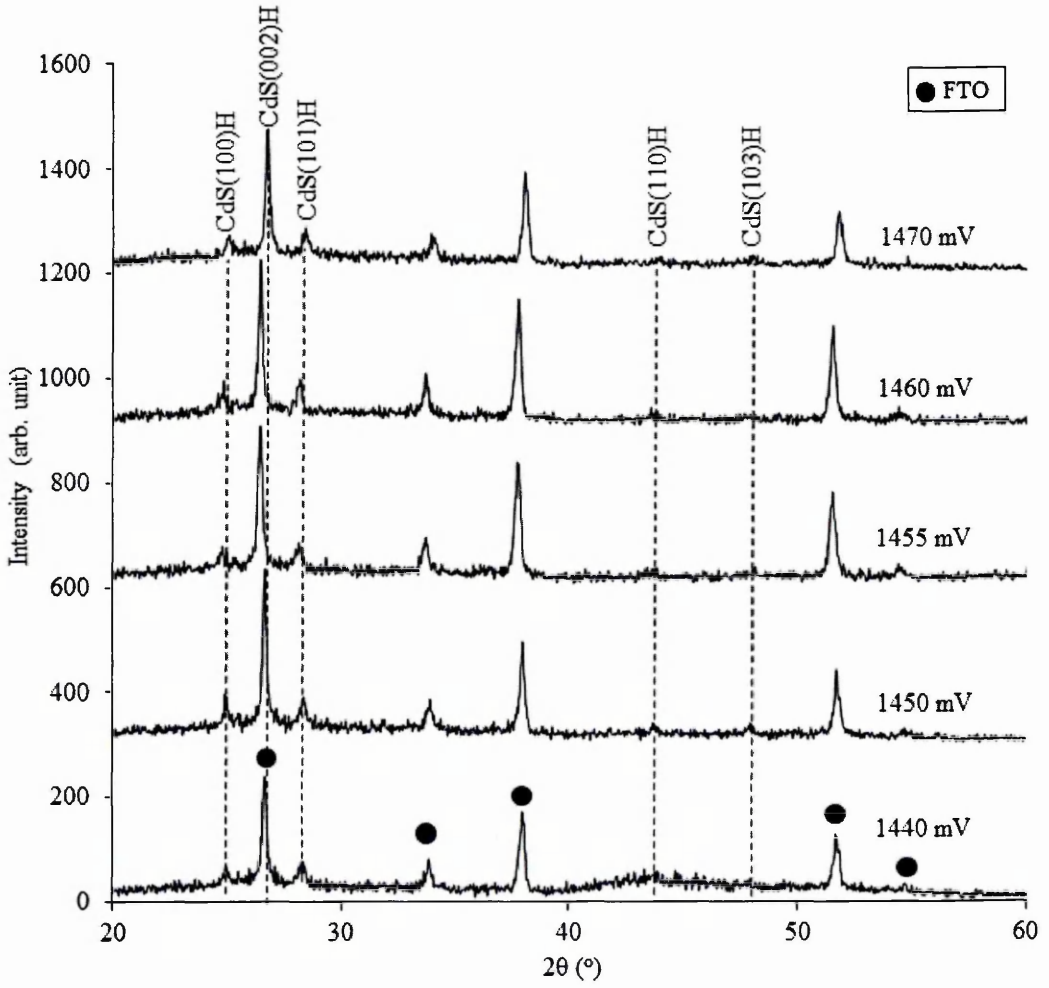


Figure 6.4: The XRD patterns of CdS samples heat-treated in air at 400°C for 20 minutes.

Before annealing, all samples were cut into 3 pieces. The purpose of dividing one sample into three was to study the effects of annealing in air with and without $CdCl_2$ treatment. After the heat-treatment in air, the cubic phase peaks and the single sulphur peak (044)O were not observed. All samples show peaks that are associated with the hexagonal phase only. This shows that heat-treatment promotes recrystallization and changes the structure of the metastable cubic phase into more stable hexagonal phase [17,18]. An additional hexagonal peak can also be seen at 47.8°. The peak of interest, (101)H shows increase in intensities due to the improved crystallinity after heat treatment. Debye-Scherrer equation as stated in Equation (5.5) was used to calculate the size of crystallites for as-deposited and heat-treated samples.

Tables 6.1 and 6.2 show the calculation of crystallite sizes using Debye-Scherrer equation. By comparing both results, we can see that the crystallite sizes increased after annealing was carried out upon all samples. From both tables, crystallite sizes were

found to increase between 1 to 5 nm after annealing. The increase in crystallite sizes was found from the reduction in full width at half maximum (FWHM) of XRD peak. By getting smaller FWHM, the crystallite sizes produced after annealing should be larger. The increase of crystallite sizes after annealing is common observation for electrodeposited CdS and similar results have been reported by Mondal *et al* [19].

Han *et al* in 2013 has published scientific report highlighting the benefits of heat-treatment of CdS layers in the presence of $CdCl_2$. In this paper, this group had experimented different heat-treatment of CdS layers in several conditions such as annealing in argon and oxygen environment. Finally, they discovered that CdS layers that have been annealed in $CdCl_2$ + Ar produced the highest conversion efficiency for CdS/CdTe solar cells. Deducing from this report, annealing of electrodeposited CdS layers with $CdCl_2$ was also carried out.

Table 6.1: Crystallite sizes for as-deposited samples calculated using (101) peak as the reference.

Growth voltage (mV)	Growth time (min)	2θ (°)	FWHM (rad)	Crystallite size (nm)
1440	60	28.2	0.014	10
1450	60	28.3	0.011	14
1455	60	28.4	0.014	10
1460	60	28.4	0.007	22
1470	60	28.3	0.009	16

Table 6.2: Crystallite sizes for heat-treated samples calculated using (101) peak as the reference.

Cathodic potential (mV)	Growth time (min)	2θ (°)	FWHM (rad)	Crystallite size (nm)
1440	60	28.4	0.010	15
1450	60	28.3	0.009	17
1455	60	28.0	0.014	11
1460	60	28.2	0.006	23
1470	60	28.2	0.008	18

Prior to $CdCl_2$ treatment, saturated $CdCl_2$ solution was prepared by dissolving $CdCl_2$ powder with 99.999% purity into 100 ml deionized water. The $CdCl_2$ treatment was carried out by dipping the as-deposited samples into the solution for 10 seconds and then the samples were taken out and allowed to dry. After the samples dried, heat - treatment in air at 400°C for 20 minutes was carried out. Similar heat treatment temperature and annealing time were employed so that the comparison between two different heat treatment conditions can be analysed accurately.

The XRD diffractograms for $CdCl_2$ treated samples are shown in Figure 6.5. Results show that $CdCl_2$ treated layers also have similar patterns with normal heat treatment. Only peaks associated with hexagonal phase (100)H, (002)H, (101)H, (110)H and (103)H are present. Closer look at (101)H peaks reveals that there is a small decrease in the FWHMs when compared to samples heat-treated without $CdCl_2$ (Figure 6.4). This means that heat-treatment with $CdCl_2$ produces larger crystallites than samples without $CdCl_2$ treatment.

Table 6.3 shows the values of crystallite sizes for $CdCl_2$ treated samples, also calculated using Debye-Scherrer equation. From this table, all CdS layers show enlargement of crystallites. Majority of the samples produced crystallites larger than 20 nm. Largest size was found to be 26 nm. When comparison was done within the values tabulated in Table 6.2 and Table 6.3, it shows that $CdCl_2$ treatment assisted in promoting large grains growth but the effect is not substantial. The increments of crystallite sizes are between 1 nm to 10 nm. However, if the comparison between Table 6.1 and Table 6.3 is carried out, the crystallite sizes increase between 1 nm to 16 nm. Therefore, based on crystallite sizes study, heat-treatment with $CdCl_2$ is preferable for obtaining large grain sizes.

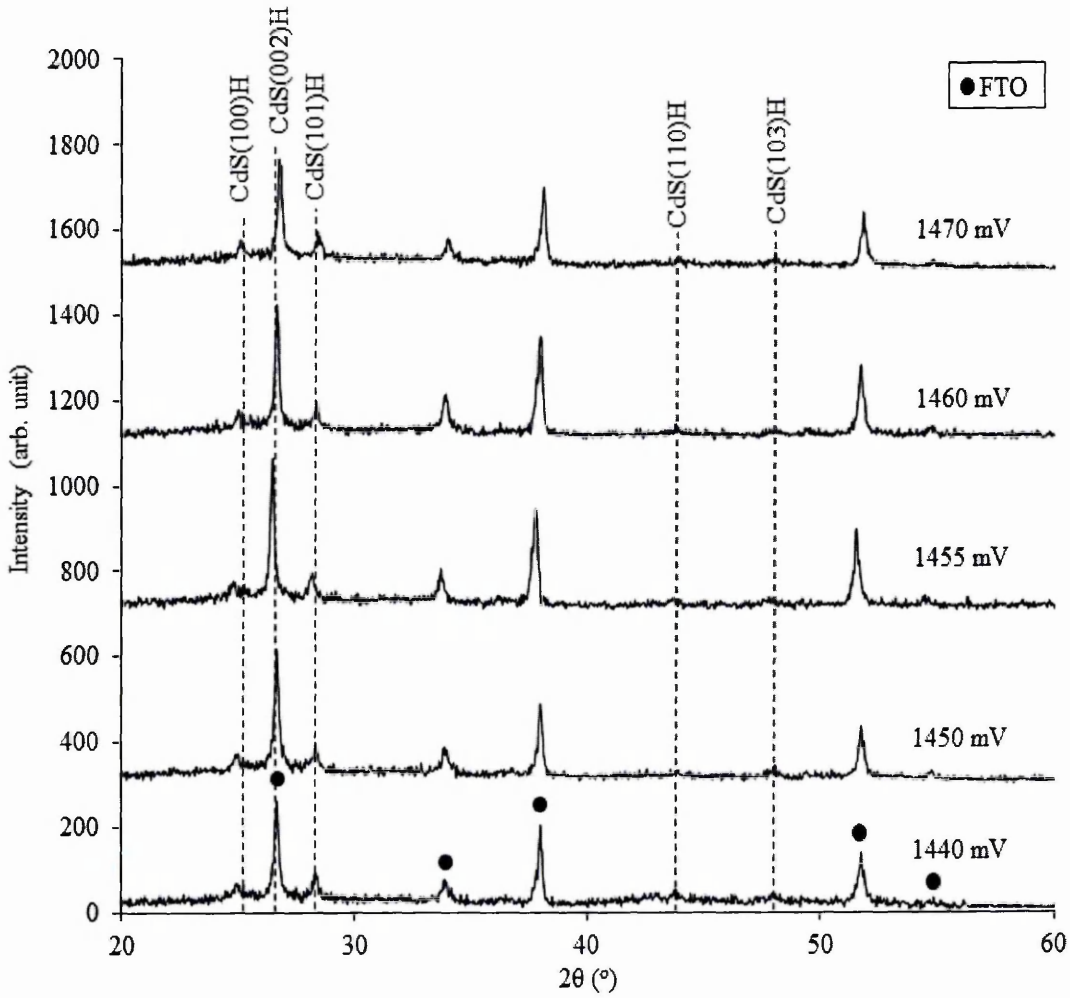


Figure 6.5: The XRD patterns of CdS samples heat-treated in air at 400°C for 20 minutes after $CdCl_2$ treatment.

Table 6.3: Crystallite sizes for $CdCl_2$ treated samples calculated using (101) peak as the reference.

Growth voltage (mV)	Growth time (min)	2θ (°)	FWHM (rad)	Crystallite size (nm)
1440	60	28.3	0.006	26
1450	60	28.3	0.006	23
1455	60	28.1	0.007	22
1460	60	28.3	0.006	23
1470	60	28.3	0.008	19

Figure 6.6 shows the comparison of XRD intensity of (101) peak between the as-deposited, heat-treated with and without $CdCl_2$ treatment. In this figure, one can see

that heat-treatment with $CdCl_2$ is the better way to achieve better crystallinity of the electrodeposited CdS layers. For cathodic potentials between 1440 mV to 1470 mV, we can see that after $CdCl_2$ treatment, the intensity of (101)H peaks, in majority, settled around 90 to 100 counts. The intensity plot in Figure 6.6 can assist in reducing the deposition window to just 30 mV (1440 mV to 1470 mV).

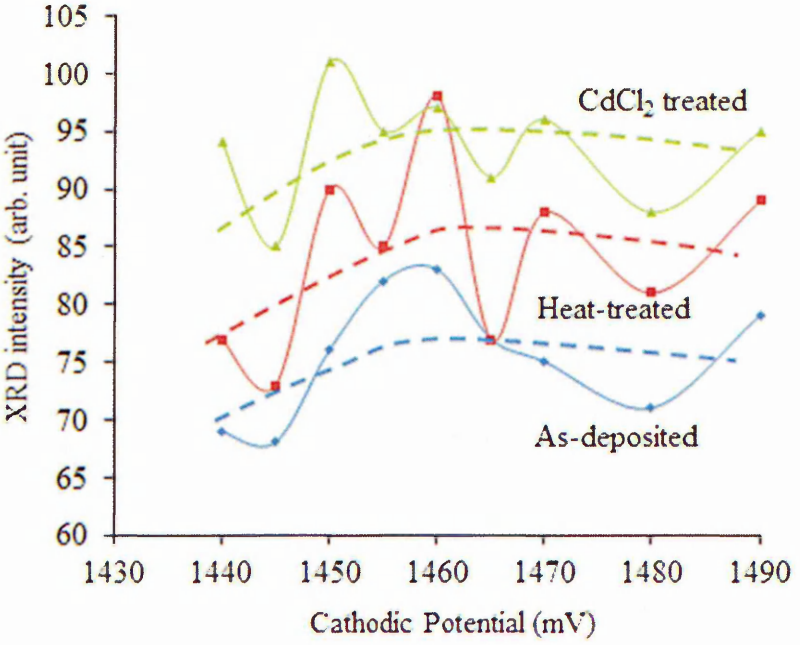


Figure 6.6: Comparison of XRD intensities of (101) peak between as-deposited, heat-treated and $CdCl_2$ treated CdS layers. Dashed lines shows the trend of XRD intensities against the cathodic potentials.

6.3.4 Optical absorption spectroscopy

The essence of optical spectroscopy experiment is to measure the bandgap and transmittance percentage of semiconducting materials. By carrying out optical spectroscopy on as-deposited, heat-treated and $CdCl_2$ treated CdS samples as in Figure 6.7, the nature of the layers when responded towards the incident monochromatic light can be analysed. CdS layers used in Figure 6.7(a) was electrodeposited at 1455 mV while in Figure 6.7(b), the cathodic potential was 1460 mV.

The results show that for as-deposited samples, if excess sulphur is present in the CdS layers, the absorption of light will be very strong and this behaviour is not favourable because of two reasons. Firstly, the bandgap of the as-deposited CdS is not in the range 2.4-2.6 eV as normally reported in literatures [10,12-13]. The bandgap

values in the range of 2.20 to 2.27 eV for both cases indicated that the materials were not at the right stoichiometry yet between cadmium and sulphur. Secondly, strong photo-absorption in CdS layers will reduce the efficiency of CdS/CdTe solar cells. Scientific works reported by McCandless and Hegedus and Krishnakumar *et al* suggested that thinning of CdS window layer is essential to improve spectral response in the region below the CdS bandgap [20-21]. So it is more favourable for semiconducting CdS layers to have high optical transmittance.

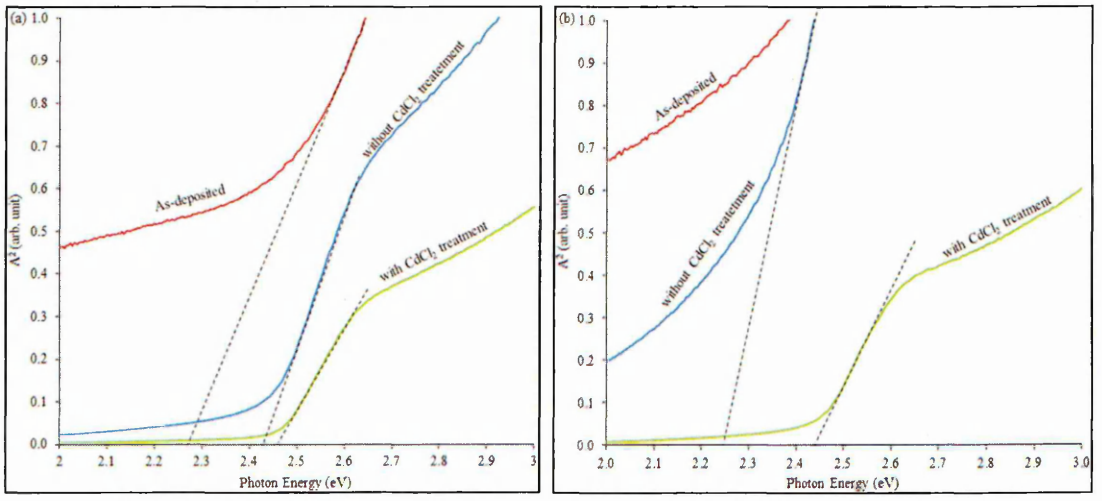


Figure 6.7: Optical absorption curves for CdS samples grown at (a) 1455 mV and (b) 1460 mV. Both samples were heat treated in air at 400°C for 20 minutes.

Figure 6.8 shows the optical absorption curves for samples annealed without and with $CdCl_2$ treatment as a function of growth voltage. This study was carried out to see the trend when electrodeposited samples undergone different heat treatment conditions. Clearly, annealing without $CdCl_2$ produced layers with inconsistent bandgap edges as depicted in Figure 6.8 (a). In this figure, the bandgap edges vary between 2.25 eV to 2.45 eV. Samples grown at 1455 mV had undergone complete thermal reaction. So the excess sulphur in the layers have reacted with any elemental cadmium or sublimed. As a result, near stoichiometric composition between cadmium and sulphur was achieved. Due to this reaction, bandgap edges came close to the bulk values of 2.42 eV. For the samples that did not achieve complete thermal reaction and still contained excess sulphur, the bandgap edges settled below 2.40 eV.

When electrodeposited samples were heat treated with saturated $CdCl_2$ solution, all samples showed bandgap edges close to 2.42 eV. It was achieved due to the reaction

of excess cadmium with any untreated sulphur in the layers thus producing additional CdS bondings. Dharmadasa has proposed the same reaction mechanism in his comprehensive review paper regarding the role of excess cadmium during $CdCl_2$ treatment of cadmium telluride semiconductors [22]. This results show that addition of $CdCl_2$ helps the conversion of elemental sulphur present in the layers to turn into CdS thin films that are close to stoichiometric level regardless of the cathodic potential. In simple words, $CdCl_2$ treatment of electrodeposited CdS 'guarantees' the bandgap of electrodeposited CdS close to the bulk value (2.42 eV).

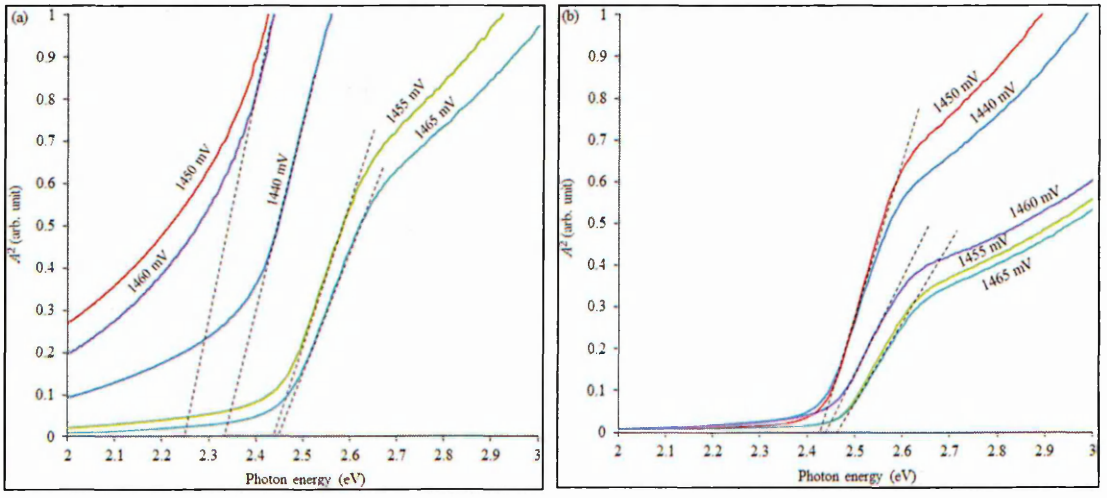


Figure 6.8: Optical absorption curves of CdS samples annealed at 400°C for 20 minutes (a) without $CdCl_2$ treatment and (b) with $CdCl_2$ treatment.

The relationship between absorbance, A and transmittance, T is given in Equation (6.2) where [23],

$$A = \log_{10}\left(\frac{1}{T}\right) \tag{6.2}$$

From the absorbance curves in Figure 6.8(a) and Figure 6.8(b), the transmittance curves can be derived by using Equation (6.2). The transmittance curves as a function of wavelength are plotted in Figure 6.9. Figure 6.9(a) represents the transmittance of heat-treated samples while Figure 6.9(b) represents the transmittance of $CdCl_2$ treated samples. The wavelength of 512 nm is marked on both graphs to relate with the bandgap of CdS (2.42 eV). As have been discussed before in Chapter 1, solar spectrum is divided into three regions according to the wavelengths. These three regions are

ultraviolet (UV), visible and infrared (IR). The boundaries between them have been drawn in both figures for convenience.

By studying both figures, one can see that the optical transmittance curves of heat-treated samples are weak in the 300 nm to 500 nm region. At the 470 nm 'knee', the highest optical transmittance is around 18% for the heat-treated samples. Samples that have been treated with $CdCl_2$ show improved transmission of light in this region with the highest transmittance up to 28% at 470 nm 'knee'.

If observations are made in the region higher than 512 nm, clearly all $CdCl_2$ treated samples achieve 80% optical transmittance between 512 nm to 700 nm. For heat-treated samples, none of the samples had achieved transmittance beyond 80% in the visible region. It shows that in the long wavelength regions (> 512 nm), the optical transmittance for $CdCl_2$ treated samples is consistent even though different cathodic potentials were applied.

Finally in the infrared region, all $CdCl_2$ treated samples show high optical transmittance within 90%. Whilst for the heat-treated samples, none of the samples had achieved 90% transmittance. Since CdS is used as the window layer in CdS/CdTe solar cells fabrication, high optical transmittance is more preferable than high absorbance. This study unveils that $CdCl_2$ treatment is an important step to be carried out before the growth of CdTe layers because it improves the optical transmittance of the electrodeposited CdS throughout the entire region, from UV to IR.

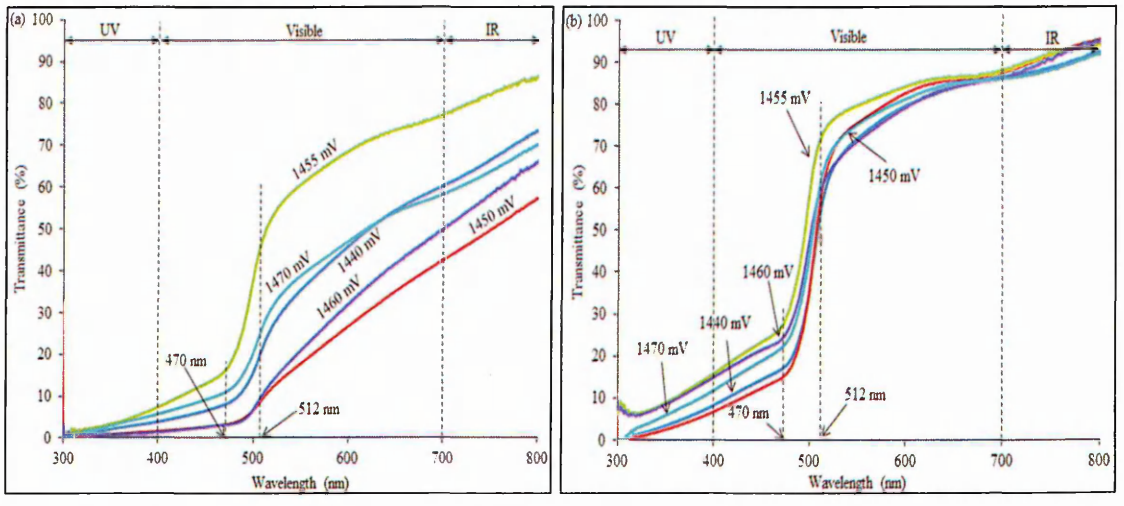


Figure 6.9: Transmittance curves of CdS samples annealed at 400°C for 20 minutes (a) without $CdCl_2$ treatment and (b) with $CdCl_2$ treatment.

6.3.5 X-ray flouroscence (XRF)

X-ray flouroscence (XRF) studies were performed to see the effects of changing the cathodic potential towards the composition of Cd and S. All samples were electrodeposited for 60 minutes. In this project, Philips Magix PRO XRF system was utilized. Several samples were grown with different cathodic potentials as shown in Table 6.4. Table 6.4 shows the atomic percentage of sulphur and cadmium after the samples were heat-treated in air and with and without $CdCl_2$ treatment.

Table 6.4: Relative changes in the atomic percentage of electrodeposited CdS grown at different cathodic potentials. Results shown are for heat-treated and $CdCl_2$ treated samples using the values for as-deposited films as the reference.

Cathodic potential (mV)	Atomic Percentage (at%)			
	Heat-treated		$CdCl_2$ treated	
	S	Cd	S	Cd
1420	-0.97	19.01	-8.86	170.66
1430	-0.43	9.15	-7.90	181.92
1440	2.10	-40.73	-7.41	143.58
1450	-2.24	83.65	-5.10	189.35
1460	1.13	20.26	-6.30	168.02
1470	0.35	-6.45	-6.22	115.23
1480	-0.63	14.05	-7.88	176.58
1490	-0.09	2.12	-6.51	146.93
Average	-0.10	12.63	-7.00	161.54

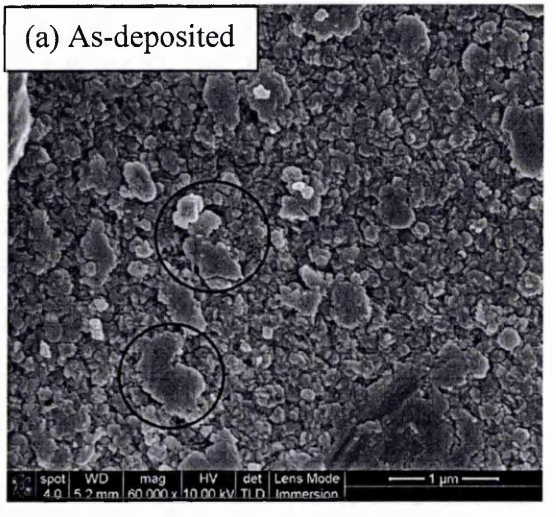
Table 6.4 shows that on average, after heat-treatment, the sulphur content in the layers reduces by 0.10%. On the other hand, the cadmium content increses to about 13%. After $CdCl_2$ treatment the sulphur content decreases even further. For the $CdCl_2$ treated samples, all samples show the decrease in sulphur content after the treatment. The average reduction of sulphur shown in Table 6.4 is 7.00%. At the same time, the XRF results show that high percentage increase of cadmium in CdS layers after the chemical tretment. All samples show more than 100% increase of cadmium. The average percentage increse of cadmium after tretment is close to 162%.

However, it should be noted that these atomic percentage values are useful for comparison but the absolute percentage values can be away from the exact values due to uncertainty in calibration.

6.3.6 Scanning electron microscope (SEM)

Scanning electron microscopy (SEM) studies were carried out for the sample grown at the best crytallinity as deduced from XRD results. The cathodic potential of choice was 1450 mV. It was chosen because this cathodic potantial produced the highest crystallinity after $CdCl_2$ treatment as shown in Figure 6.6. The SEM images for as-deposited, heat-treated and $CdCl_2$ samples are shown in Figure 6.10.

Surface morphology for the as-deposited sample shows that the size of the grains is between 100 nm to 200 nm. From Figure 6.10(a), there are grains that combine to create agglomerations with the sizes between 700 nm to 1000 nm. These agglomerations are circled in Figure 6.10(a) for easy reference. When anneling was carried out at 400°C for 20 minutes, the grain sizes were found to have almost similar size to the as-deposited CdS. The grain sizes were expected to increase based on the crystallite sizes calculation made previously in section 6.3.3. This phenomena is not observed in SEM because the increment of crytallite sizes is very small which is between 1 nm to 10 nm only. The agglomerations with the size up to 1000 nm can also be seen in the heat-treated sample.



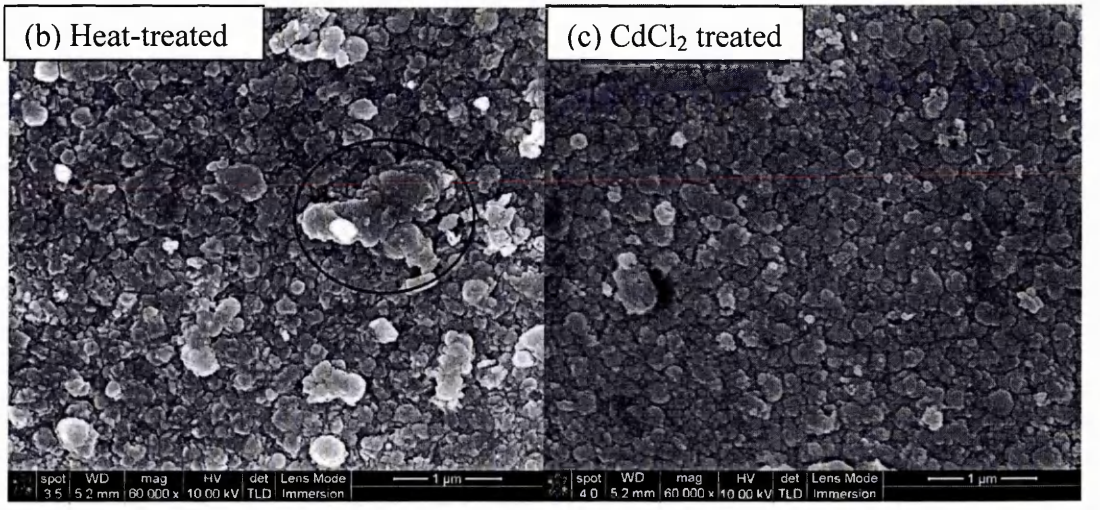


Figure 6.10: SEM images obtained from samples grown at cathodic potential of 1450 mV. Circles represent agglomerations.

After anneling in the presence of $CdCl_2$, (Figure 6.10(c)) the grain sizes still look similar to the previous two results. But the huge agglomerations as observed in Figure 6.10(a) and 6.10(b) have gone thus creating uniform morphology across the entire surface.

SEM cross section for the as-deposited CdS with magnification of 250 000x is shown in Figure 6.11. The sample was grown at cathodic potential of 1440 mV for 60 minutes. The high magnification is used so that the demarcation between CdS and FTO can be seen cearly. From this figure, the thickness of the CdS layer is estimated to be close to 200 nm. CdS layer shows very high density characteristic. There is no defects or cracks observed within the CdS layer.

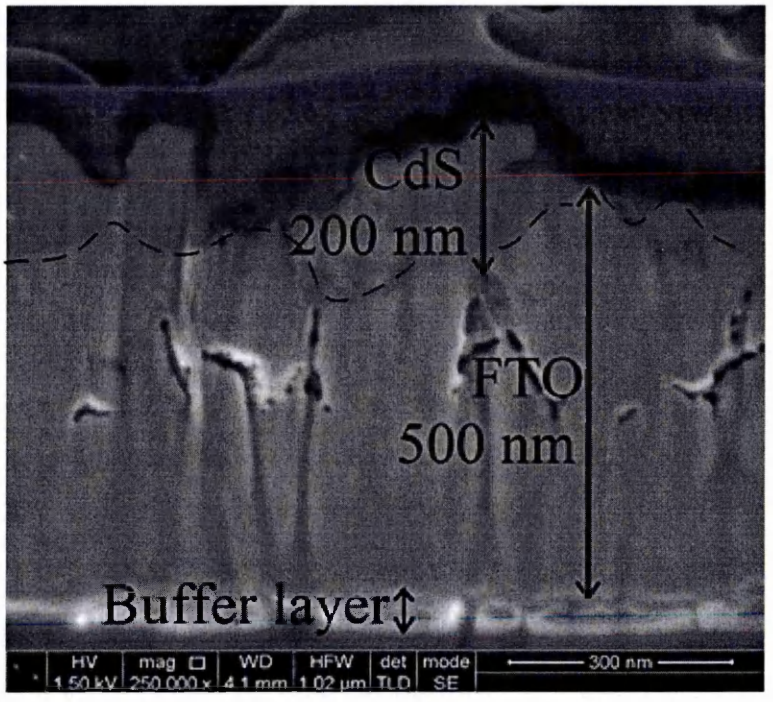


Figure 6.11: SEM cross section image with 250 000x magnification for of as-deposited CdS samples grown at cathodic potential of 1440 mV for 60 minutes. The thickness of the CdS layer is estimated close to 200 nm. (Courtesy: Leon Bowen, Durham University)

The thickness of the FTO layer is estimated to be close to 500 nm. Few voids are observed in Figure 6.11. The presence of these voids suggested that they might be originated from manufacturing process or it could be from the 'cut and snap' process performed throughout the sample preparation for SEM experiment.

The thin buffer layer with the thickness estimated to be close to 70 nm might serve as the sodium diffusion barrier. Commercial glass products are made from soda lime glass. Soda lime glass usually contains Na_2O and also K_2O. In CdS/CdTe solar cells fabrication, annealing of electrodeposited or chemical bath deposited CdS at temperarure of ~ 400°C is necessary to improve the quality. Sodium diffusion might occur due to the increase of atoms mobility inside soda lime glass. Sodium is a p-type dopant and if it diffuses into CdS, which is a stable n-type material, the layer will become resistive due to the self-compensation effect. Therefore, the presence of buffer layer is helpful in order to surpress sodium diffusion into CdS.

6.3.7 Photoelectrochemical (PEC) cell measurement

Photoelectrochemical (PEC) cell measurements of CdS layers electrodeposited with different cathodic potential are tabulated in Table 6.5. From this table, the electrical conductivity type of as-deposited, heat-treated and $CdCl_2$ treated layers can be seen clearly.

Table 6.5: PEC cell measurements of as-deposited, heat-treated and $CdCl_2$ treated CdS layers.

	PEC Signal (mV)		
Cathodic potential (mV)	As-deposited	Heat-treated	$CdCl_2$ treated
1420	-4	-11	-36
1430	-4	-14	-41
1440	-2	-14	-23
1450	-3	-7	-16
1460	-6	-22	-52
1470	-5	-19	-42
1480	-1	-6	-43
1490	-7	-21	-23

Results show that the conductivity of CdS is always n-type regardless whether the electrodeposited layers were annealed or not. It means, even though the as-deposited samples are rich in sulphur, there exist some kind of defects that prevents the conductivity to change from n-type to p-type. The nature of these defects is still unknown. This behaviour is opposite to electrodeposited CdTe and CIS where electrical conductivity can be changed from p-type to n-type when higher cathodic potentials are applied [24,25].

All values displayed in Table 6.5 are plotted in Figure 6.12 for easy reference. From Figure 6.12, all of the heat-treated samples show improved n-type conductivity. The improvement of n-type conductivity was due to the sublimation of excess sulphur at temperature of 400°C thus producing relatively higher Cd content in the materials. Cadmium is a metallic element and if CdS has more Cd, the magnitude of n-type conductivity should increase. By comparing the heat-treated and $CdCl_2$ treated samples,

it is obvious that $CdCl_2$ treatment enhances the n-type conductivity of the CdS semiconductors. All the $CdCl_2$ treated layers show improved n-type conductivity indicating higher donor atoms within the semiconductors.

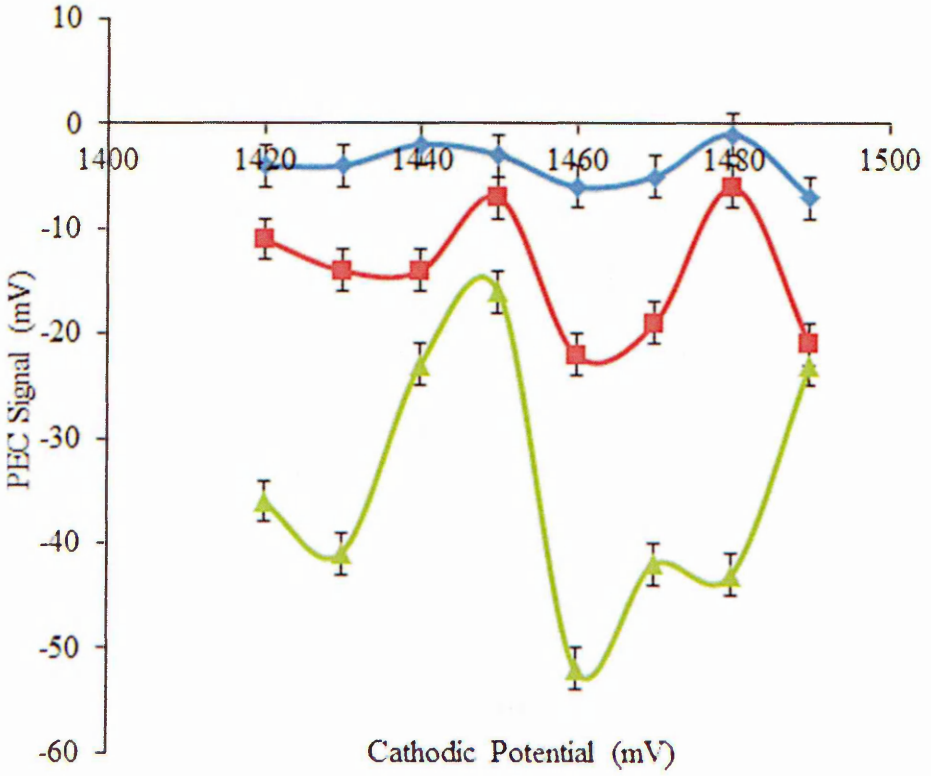


Figure 6.12: Comparison of PEC signals from as-deposited, heat-treated and $CdCl_2$ treated n-type CdS layers.

6.3.8 D.C. electrical conductivity measurements

To study the resistivity of electrodeposited semiconductors, three samples with thickness of 200 nm was used. Since CdS is an n-type semiconductor, few aluminium contacts with the size of 0.0314 cm^2 were evaporated on top of the CdS layers using a vacuum evaporator at pressure of 10^{-6} Torr. Aluminium was chosen because of its low work function property hence making ohmic contacts with CdS layers [26]. Since the contact area and thickness were known, the resistivity of the as-deposited, heat-treated and $CdCl_2$ treated CdS materials can be calculated using Equation (5.9) and (5.10) from Chapter 5. Results of electrical resistivity (ρ) of electrodeposited CdS materials using current-voltage (I-V) measurement are shown in Table 6.6.

Table 6.6: The I-V measurement of as-deposited, heat-treated and $CdCl_2$ treated CdS layers.

	Resistivity (ρ) ($\times 10^4$ Ωcm)				
Sample	1st	2nd	3rd	4th	Average
As-deposited	5.8	5.9	5.8	5.8	5.8
Heat-treated	3.6	3.4	3.3	3.2	3.4
$CdCl_2$ treated	3.5	3.0	3.2	2.9	3.2

For each sample, 4 different points were measured and the averages of these measurements were used as the final value. This study reveals that resistivity of electrodeposited layers can be lowered by heat-treatment in air. Same results have also been reported by Zaibari *et al* and Oumous and Hadiri [17,27]. The resistivity of electrodeposited CdS can further be decreased by $CdCl_2$ treatment. It can be seen from Table 6.6 where the lowest resistivity of 3.2×10^4 Ωcm was obtained from $CdCl_2$ treated sample in contrast to 3.4×10^4 Ωcm obtained from heat-treated sample. This study once again shows that besides structural, optical, compositional and morphological benefits, $CdCl_2$ treatment is also helpful in decreasing the resistivity of electrodeposited CdS layers.

6.4 Conclusion

Cadmium sulphide semiconducting layers have been successfully deposited using electrochemical technique with 2-electrode system. All layers presented in this chapter were deposited at 80°C and pH = 2.00 ± 0.02. In this study, six characterisation techniques were employed to determine the suitable deposition voltage. In the end, the best deposition voltage was found to be between 1440 mV to 1470 mV.

Results obtained show that the as-deposited CdS semiconductors were rich in sulphur. Cubic and hexagonal phases were present in these layers. By annealing the as-deposited CdS in air for 400°C for 20 minutes, the sulphur content could be reduced, thus bringing the electrodeposited CdS semiconducting layers closer to the stoichiometric level.

Annealing the as-deposited layers in the presence of $CdCl_2$ can improve the CdS quality by enlarging the crystallite sizes and enhancing the n-type conductivity. In addition, the optical spectroscopy results showed that regardless of the cathodic

potentials applied, the bandgap of the $CdCl_2$ treated CdS always very close to the bulk value of 2.42 eV and also produce better layers in terms of optical transmittance. Last but not least, the $CdCl_2$ treatment also affects the electrodeposited CdS positively by decreasing its electrical resistivity.

After thorough investigations, it can be concluded that $CdCl_2$ treated CdS layers are the most suitable for CdS/CdTe device fabrication.

6.5 References

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7.1 Introduction

The history of CdTe solar cells has been presented in Chapter 3. From the informations provided in this chapter, we know that the first report on CdTe solar cell was published in 1963 by Cusano [1]. The cell was fabricated using vapour deposition technique where the vacuum system was also present. Since this discovery, vapour deposition technique was utilized in research and development of high efficiency CdTe based solar cells [2-3].

The first report on liquid phase (or wet chemical) deposition of CdTe layers was published in 1976 by Nakayama *et al* [4]. CdTe solar cell fabricated by screen printing technique showed promising result by achieving 8.1% conversion efficiency. This report had beaten the 6% efficiency record reported by Bonnet and Rabenhorst in 1972 [2]. It is important to note that the solar cell devices reported by Bonnet and Rabenhorst were fabricated by high temperature vapour deposition technique. It shows that CdTe is a 'special' material because even with the low cost technique, the quality of wet chemical deposited CdTe layers is still satisfactory. Besides screen printing technique, other wet chemical deposition that shows promising results is electrodeposition.

Electrodeposition of CdTe in an aqueous solution was initiated by Panicker *et al* in 1978 [5]. Four years later, Fulop *et al* claimed 8.7% conversion efficiency with electrodeposited CdTe solar cell [6]. Over the years, electrodeposition had gained serious attention among academics and industries because it was seemed as a low cost, scalable and manufacturable technique. Electrodeposition was proven to be scalable and manufacturable when BP Solar had successfully commercialised 10.6% efficiency solar panels with the size of 0.94 m^2 in late 1990s [7].

Besides the advantages mentioned above, the deposition of either n-type or p-type CdTe can be implemented through electrodeposition. This process is known as intrinsic doping where the electrical conductivity of CdTe can be altered between n-type and p-type simply by changing the stoichiometry between Cd and Te. Takahashi *et al* [8] and Patil *et al* [9] have reported that when CdTe layers are rich in Cd, the electrical conductivity is n-type. On the other hand, when the layers are Te-rich, the electrical conductivity is p-type [8,9]. Apart from CdTe, there are other semiconductors that can be made as p-type or n-type materials through electrodeposition simply by changing the

stoichiometry among the elements inside the semiconductors. ZnS and CIS are some of the examples given [10,11].

In this research programme serious attention was given in understanding the device structures and material issues. One of the most important aspects in solar cells fabrication is the impurity control. In 1994, Dennison reported that the presence of foreign ions' for examples, copper and silver even at parts per billion levels (ppb) is detrimental to the performance of electrodeposited CdTe solar cells [12]. The effects are significant when the ions concentration exceeds 14 ppb for Ag^{+} and 38 ppb for Cu^{2+}. Typical reference electrodes used nowadays are Hg_2/Hg_2Cl_2 and Ag/AgCl. Therefore, it is safer to omit the reference electrode for electrodeposition of CdTe. This decision was taken to avoid the leakage of detrimental ions that might occur from the electrolyte inside the reference electrode to enter the deposition electrolyte.

Other advantage of omitting the reference electrode is the deposition temperature can be increased. Increasing the deposition temperature up to 90°C might not be possible when Hg_2/Hg_2Cl_2 reference electrode is used. This is because, the safe operating temperature for Hg_2/Hg_2Cl_2 is 60°C [13]. So by removing the reference electrode the temperature of the electrolyte can be heated up to 90°C for aqueous solutions. In semiconductors research and development, high temperature deposition is favourable because it produces larger grains and better crystallinity of the deposited materials. To increase the temperature of deposition electrolyte beyond 100°C, non-aqueous solution can be used [14].

Lastly, by omitting the reference electrode the overall cost to set-up the electrodeposition system could be reduced. This is because the reference electrodes have a lifetime and must be replaced when needed. In terms of cost, it is more beneficial for a long term project.

7.2 Preparation of CdTe electrolyte bath

An aqueous electrolyte for CdTe deposition was prepared by dissolving 166.4 g of $CdSO_4$ powder (99% purity) in 800 ml of deionised water. The molarity of this electrolyte was 1.0M. The pH of the electrolyte was adjusted to 2.00 ± 0.02 using diluted H_2SO_4 and NH_4OH. The electrolyte was stirred overnight to make sure that all of the $CdSO_4$ powder would be fully dissolved. The electrolyte had to be purified for at least 40 hours before deposition of CdTe layers can be initiated.

TeO_2 powder (99.999% purity) was used as the source of Te. Te solution with the molarity of 0.03M was prepared by dissolving ~1.2 g of TeO_2 powder in a separate 250 ml volumetric flask containing a mixture of concentrated sulphuric acid (H_2SO_4) and deionised water. The TeO_2 solution is also stirred overnight to increase the solubility of the TeO_2 powder. Both chemicals were supplied by Sigma-Aldrich UK. Substrates for CdTe layers are prepared in the same way as for electrodeposition of CdS layers. CdTe electrolyte bath is crystal clear and stable. The bath can be used continuously for indefinite lifetime.

7.3 Results and discussions

7.3.1 Voltammogram

Before the deposition of CdTe layers, 2 ml of TeO_2 was added into $CdSO_4$ bath using a pipette. Similar to CdS deposition, the voltammogram was recorded at the temperature of ~80°C with the scan rate of 3 mVs^{-1} using Gillac computerised potentiostat. Figure 7.1 shows the voltammogram of 1.0M $CdSO_4$ aqueous solution containing 2 ml of TeO_2.

From Figure 7.1, we can see that the deposition of Te begins at 140 mV (point A). Tellurium should deposit first due to the fact that the redox potential for Te is more positive (E_o = + 0.53 V) than Cd (E_o = -0.40 V) [15]. The reduction of $HTeO_2^+$ ion to form Te atoms is given as [5];

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \quad (7.1)$$

After point A, electrical current increases linearly across region 1 up to point B. The deposition of Cd starts at ~950 mV (point B) and the current starts to rise again. The formation of CdTe is given by [5];

$$Cd^{2+} + Te + 2e^- \rightarrow CdTe \quad (7.2)$$

The increase of electrical current in region 2 is higher than region 1 due to the co-deposition of Te and Cd and formation of the CdTe compound. In addition to that, the production of H_2 and O_2 molecules also happens in this region due to the electrolysis

process. Beyond 1500 mV, the current increases rapidly because the rate of production of H_2 and O_2 molecules becomes more significant. The suitable deposition window for stoichiometric CdTe layers is identified within 1500 mV to 1600 mV region. This is based on analysis of the previous scientific works by Muftah and Diso [16-17]. At the higher voltage end, it is also possible to form Cd-dendrites in addition to CdTe. During the reverse cycle, the dissolution of elemental Cd and Cd from CdTe starts in the voltage range of 1430 mV (point C) and 780 mV (point D). Finally the stripping of elemental Te from the FTO substrate occurs below 300 mV (point E).

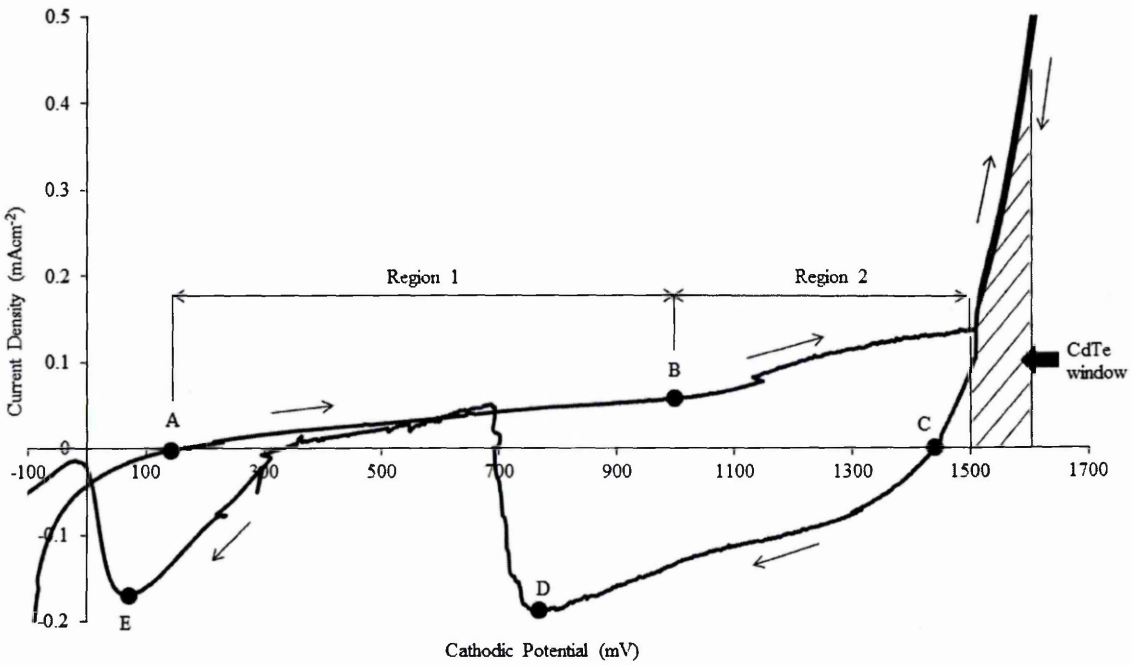

Figure 7.1: Cyclic voltammogram for an aqueous electrolyte containing 1.0M of $CdSO_4$ and 2 ml of 0.03M TeO_2 at pH = 2.00 ± 0.2 and temperature of 80°C.

Comprehensive work by Muftah and Diso in 2010 and 2011 respectively had identified the best deposition voltage range (or deposition window) for electrodeposition of CdTe layers using 2-electrode system [16-17]. The deposition window was identified to be between 1570 mV to 1580 mV. CdTe layers are rich in Te from 1570 mV to 1575 mV. From 1577 mV to 1580 mV the layers are Cd-rich. The transition point at 1576 mV is where the layers are expected to have the 1 to 1 ratio between Cd and Te. This point is where the intrinsic (i-type) CdTe is deposited. Since the suitable deposition window has been identified before, the characterisation works for electrodeposited CdTe were focused within this 10 mV window.

7.3.2 X-ray diffraction

Figure 7.2 shows the XRD patterns of electrodeposited CdTe layers on FTO. All samples were grown for 120 minutes using 2-electrode system. Five different cathodic potentials (V_g) were employed to see the effects upon changing the voltage towards the crystallinity of the deposited layers.

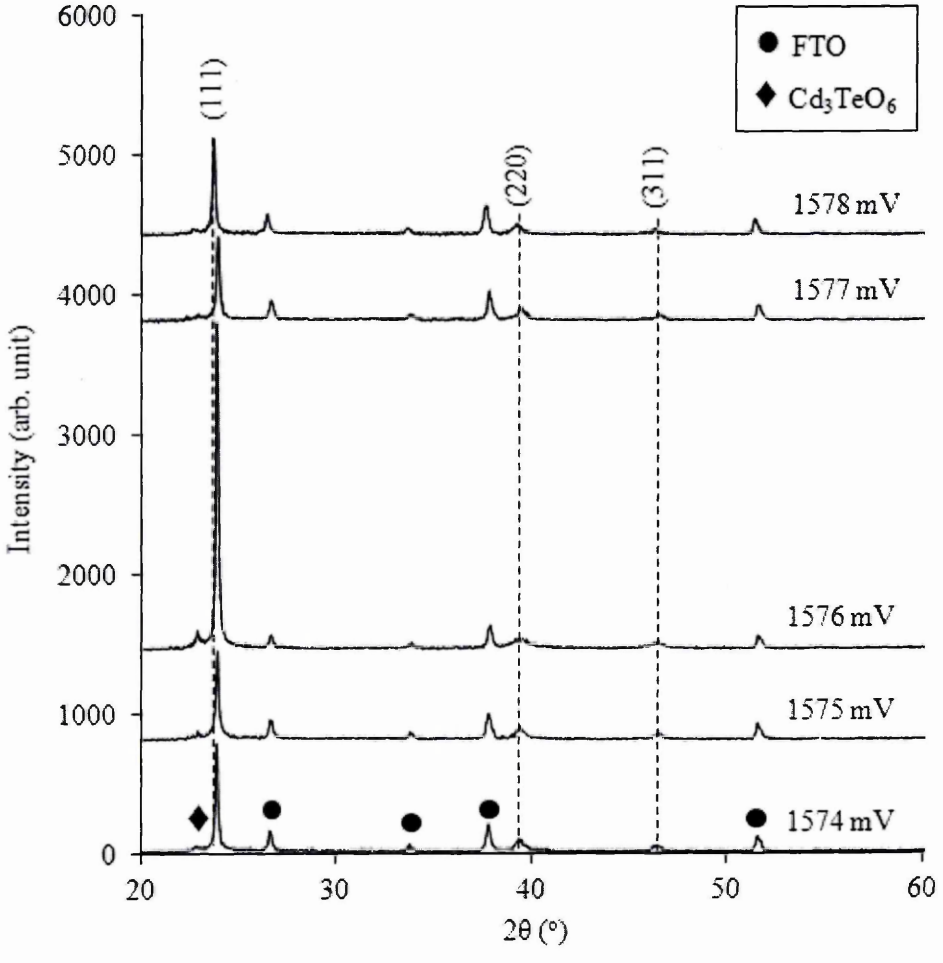

Figure 7.2: The XRD patterns of as-deposited CdTe samples grown at different cathodic potentials.

Results show that the as-deposited CdTe layers are polycrystalline cubic structure with preferred orientation along (111) planes occurring at 23.8°. The other planes that exist in this cubic structure are (220) and (311) which occurred at 39.5° and 46.2°, respectively. These three peaks match closely with JCPDS file no. 01-075-2086. From these five diffractograms, the highest (111) peak can be seen when the cathodic potential applied was 1576 mV. However, the intensity of (111) peak was also

depended on the thickness of deposited layers. To investigate whether the thickness of the as-deposited samples influenced the intensity of (111) peak, the thickness of all layers was calculated using Faraday's Law from Equation (4.3) in Chapter 4 and the results are shown in Table 7.1.

Table 7.1: Thickness of the as-deposited CdTe layers (in μm) as a function of cathodic potentials calculated using Equation (4.3) in Chapter 4.

Cathodic potential (mV)	Growth time (min)	Average current density ($\mu A/cm^2$)	Thickness (μm)
1570	120	99.3	0.51
1571	120	84.8	0.43
1572	120	145.2	0.74
1573	120	81.7	0.42
1574	120	84.2	0.43
1575	120	98.1	0.50
1576	120	164.1	0.84
1577	120	84.3	0.43
1578	120	98.2	0.50
1579	120	146.2	0.75
1580	120	148.4	0.76

Table 7.1 shows that, since the deposition time was fixed to 120 minutes for all samples, the thickness of the as-deposited CdTe layers depends on the current density when the deposition process was going on. Higher current density will result in higher thickness of CdTe layers. Thickness of the electrodeposited CdTe layers varies between 0.42 μm to 0.84 μm. The plot of the XRD intensities from (111) peaks versus cathodic potentials are shown in Figure 7.3. The thickness curve is also drawn for comparing the XRD intensity with the thickness of the electrodeposited layers. Three highest intensity counts in this figure were circled for easy reference. By studying Figure 7.3, one can see that there is a pattern that tells something about the Te addition.

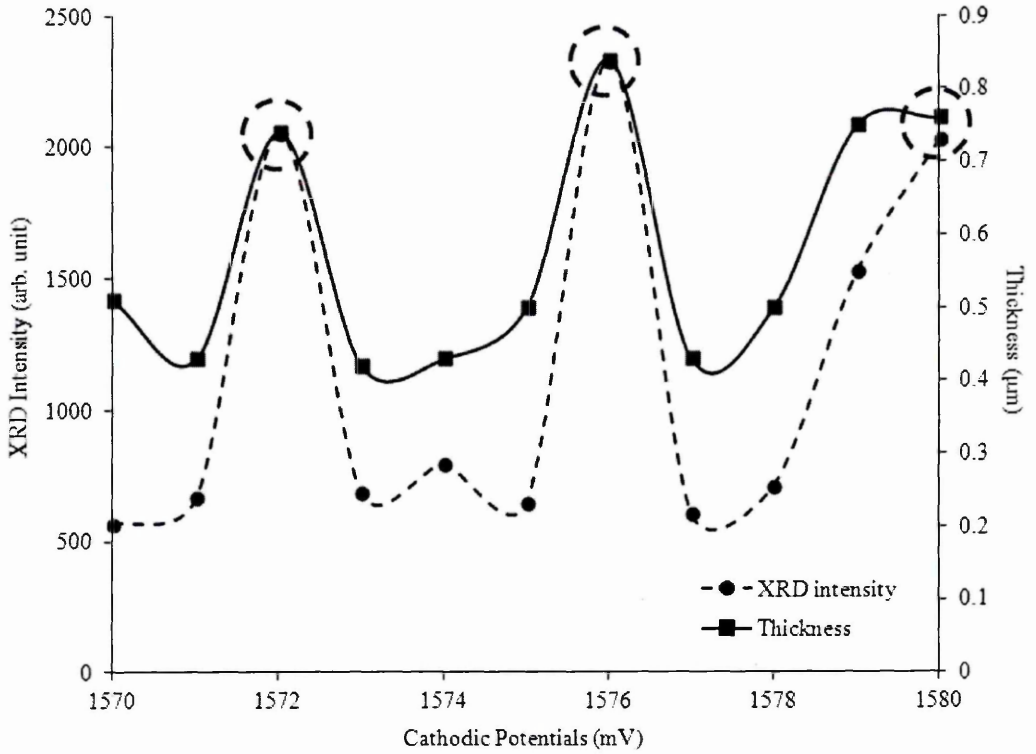

Figure 7.3: The plot of XRD intensity counts for (111) peak grown for 120 minutes using different cathodic potentials. High peaks are circled for easy reference. The thickness curve is also provided to see the relationships between XRD intensity and layers' thickness.

In this research programme, Te was diluted in concentrated sulphuric acid. However, the exact concentration of Te couldn't be quoted due to the low solubility of Te in acidic solutions [18]. Figure 7.3 shows that addition of TeO_2 into the bath takes some time before it was fully dissolved. When Te was fully dissolved into the bath, thicker CdTe thin films will be deposited on the FTO substrates due to the increase in current density. So when XRD characterization was performed, the thin films will produce (111) peak with very high intensity (see 1572 mV). The change of cathodic potentials within 1 mV intervals had little impact on current density if the solubility of Te was low. When Te exhausted, the intensity of (111) peak decreased again (see 1573 mV, 1574 mV and 1575 mV) because the thickness of the electroplated thin films was low. When TeO_2 was added for second time, the intensity of (111) peak increased again if Te fully dissolve into the bath (see 1576 mV) and then decreased to 600-800 counts when Te concentration was low (see 1577 mV and 1578 mV). This 'alternating' pattern seems repeatable but the control of Te concentration is difficult by manual adding in order to obtain consistently similar CdTe thin films.

It is important to note that a small peak occurred at 22.6° was detected in the as-deposited CdTe layers. This peak was identified to be cadmium tellurate (Cd_3TeO_6) according to JCPDS file no. 01-076-1007. The existence of Cd_3TeO_6 indicates the possibility of Te precipitation on the surface of these thin films. Figure 7.2 shows Te precipitation is more pronounce in the thicker layers (see 1576 mV). To gain more information on this peak, three samples were grown using different growth times but with the same cathodic potential. All samples were grown at 1576 mV and the results of this experiment are shown in Figure 7.4.

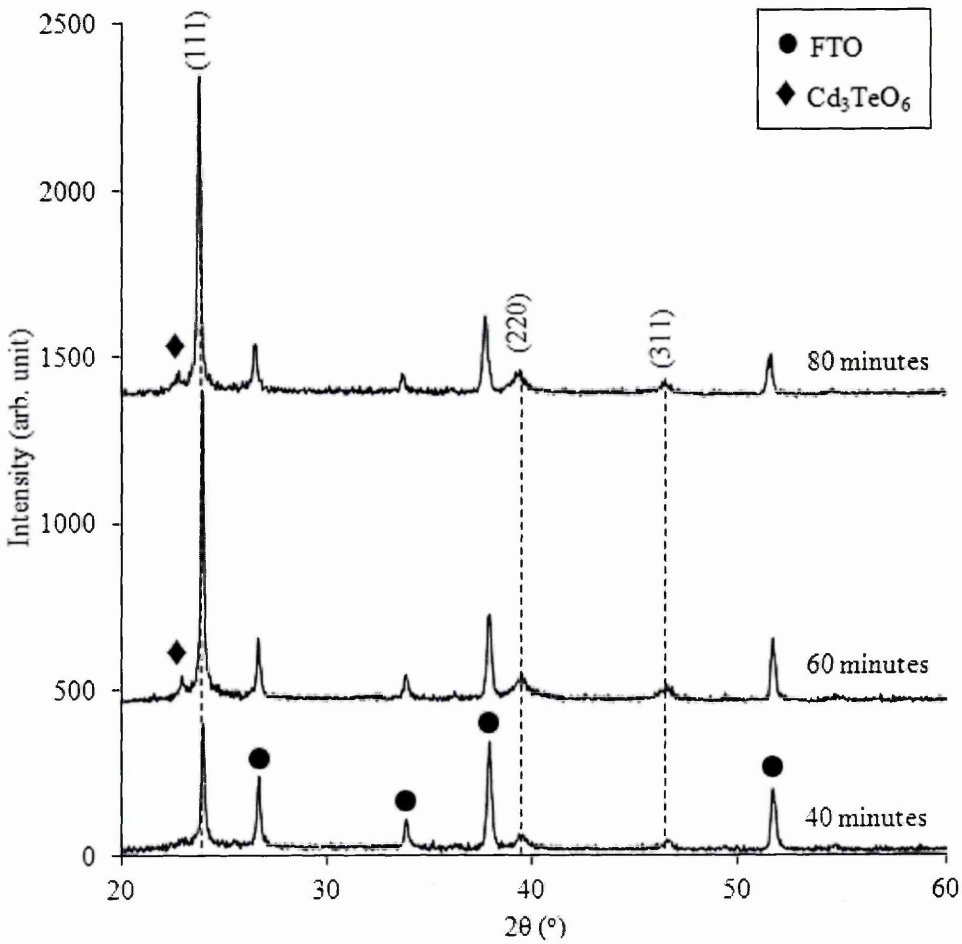

Figure 7.4: The XRD patterns of three samples with different growth times. All samples were grown at 1576 mV.

Figure 7.4 reveals that samples grown for 60 minutes and 80 minutes show the existence of Cd_3TeO_6 peak at 22.8°. Cd_3TeO_6 peak was not observed for sample grown for 40 minutes. The thickness of these three samples was calculated and the results are shown in Table 7.2. From Table 7.2, cadmium tellurate peaks can be seen clearly from

the XRD diffractograms if the thickness of the as-deposited layers is equal or higher than 0.5 μm. This observation is also true when analysis was accomplished for samples shown in Table 7.1 and Figure 7.2.

Clearly, when the thickness of the as-deposited thin films less than 0.5 μm (see 1574 mV and 1577 mV), the cadmium tellurate peaks are weak. The cadmium tellurate peaks are high when the thickness is equal or higher than 0.5 μm (see 1575 mV, 1576 mV and 1578 mV). These experiments confirmed that the precipitation of Te species is strongly related to the thickness of the electrodeposited CdTe layers. This indicates that the Cd_3TeO_6 layers establish as the growth time or layers' thickness increases.

Table 7.2: Thickness of the as-deposited CdTe layers (in μm) as a function of growth time calculated using Equation (4.3) in Chapter 4.

Cathodic potential (mV)	Growth time (min)	Average current density ($\mu A/cm^2$)	Thickness (μm)
1576	40	253.90	0.43
1576	60	225.23	0.58
1576	80	182.05	0.62

Figure 7.5 shows the XRD patterns for CdTe layers heat-treated at 400°C for 15 minutes after $CdCl_2$ treatment. Romeo *et al* has reported that in general, "$CdCl_2$ may work as fluxing agent to break atomic diffusion barriers at grain boundaries". As a result, this will lead to [19]:

- increase of the grain sizes thus improving the crystallinity
- interdiffusion between CdS and CdTe
- removing of several defects at the junction region

XRD patterns in Figure 7.5 shows that the intensity of (111) peaks is higher after $CdCl_2$ treatment. This is the indication that the crystallinity of CdTe grains improves after $CdCl_2$ treatment. The intensity of (220) peaks also increase, but the intensity of (311) peaks seems similar to the as-deposited samples. Figure 7.5 also shows that the intensity of Cd_3TeO_6 peaks increases a little bit after $CdCl_2$ treatment. This effect may

be caused by the reaction of excess cadmium and oxygen with Te precipitates while annealing thus producing additional Cd_3TeO_6 bonds [20].

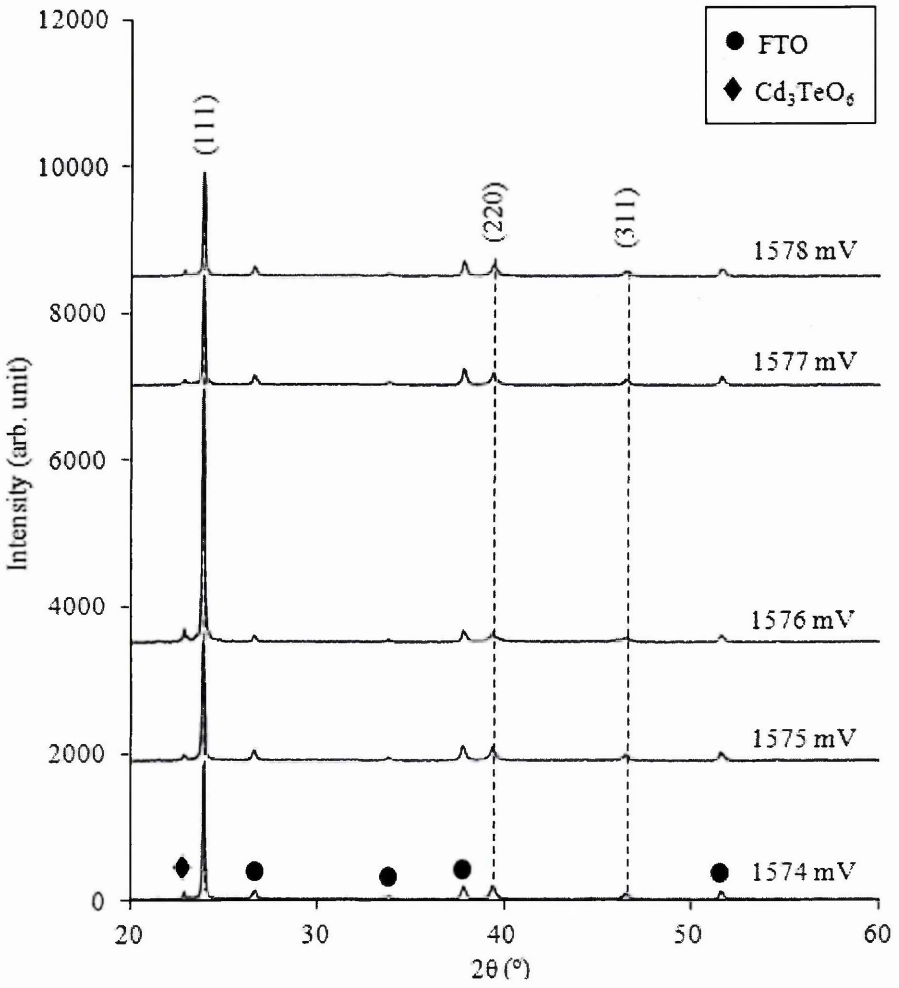

Figure 7.5: The XRD patterns of CdTe samples heat-treated in air at 400°C for 15 minutes after $CdCl_2$ treatment.

Heat-treatment with $CdCl_2$ + CdF_2 was also performed to study the effects of chlorine and fluorine mixture on structural, optical, morphological and electrical properties of electrodeposited CdTe thin films. The positive effects of doing heat-treatment in Freon ($HCFCl_2$) gas environment have been reported by Romeo *et al* [21]. Significant improvement reported was the enlargement of the grain sizes. The grain sizes of CdTe grew from 5 to 10 μm after annealing in Freon gas environment [21].

$CdCl_2$ + CdF_2 treatment was carried out by adding ~0.2 g of CdF_2 powder (99.999% purity) into concentrated $CdCl_2$ solution. The $CdCl_2$ + CdF_2 treatment was completed by dipping the as-deposited samples into the solution for 10 seconds and then the samples were taken out and allowed to dry. Similar to $CdCl_2$ treatment, all samples

were annealed in air at 400°C for 15 minutes. The XRD characterization was performed after this treatment and the results are shown in Figure 7.6.

Figure 7.6 shows that $CdCl_2$ + CdF_2 treatment followed by annealing in air also produces better crystalline materials compared to as-deposited CdTe. Similar to $CdCl_2$ treatment case, the existence of cadmium tellurate peaks can still be observed in all $CdCl_2$ + CdF_2 treated samples but with weaker intensities. Figure 7.7 summarizes all the intensity value for (111) peak for the purpose of easy comparison between the as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers. This figure shows that annealing in air after $CdCl_2$ or $CdCl_2$ + CdF_2 treatment improves the crystallinity of the as-deposited CdTe thin films. However, if comparisons are made between $CdCl_2$ and $CdCl_2$ + CdF_2 treatments, the intensities of (111) peaks are higher for $CdCl_2$ treated than $CdCl_2$ + CdF_2 treated samples except for the samples grown at 1571 mV and 1576 mV.

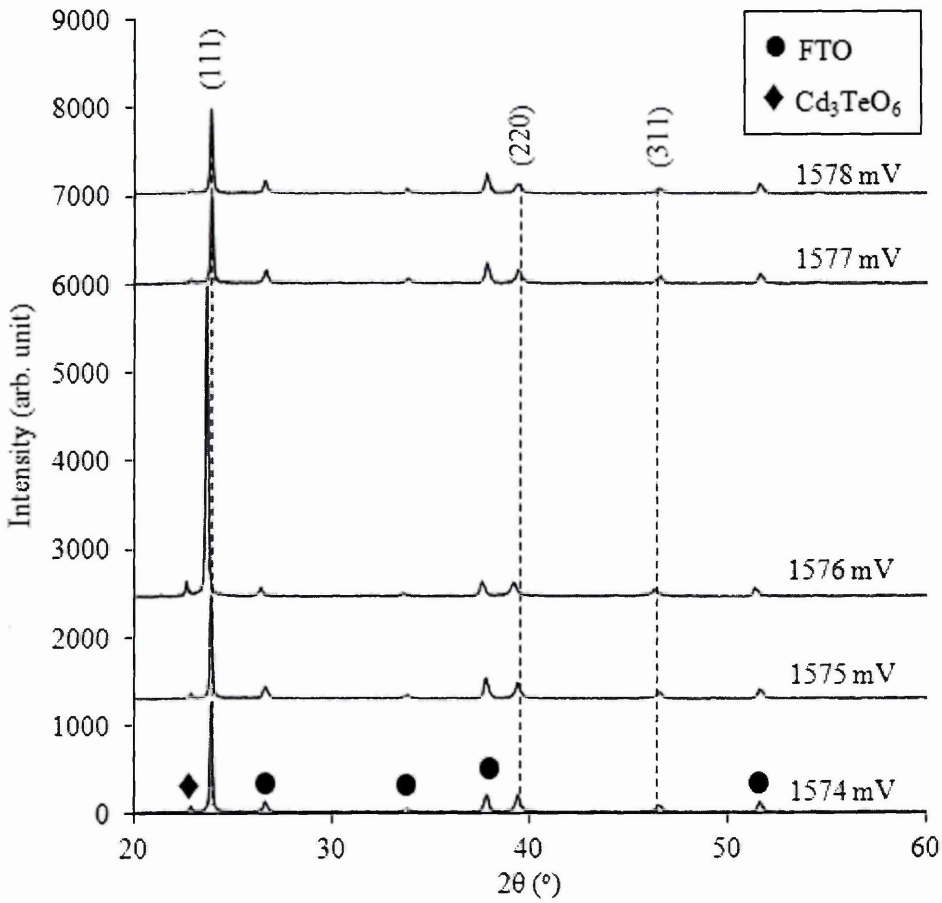

Figure 7.6: The XRD patterns of CdTe samples heat-treated in air at 400°C for 15 minutes after $CdCl_2$ + CdF_2 treatment.

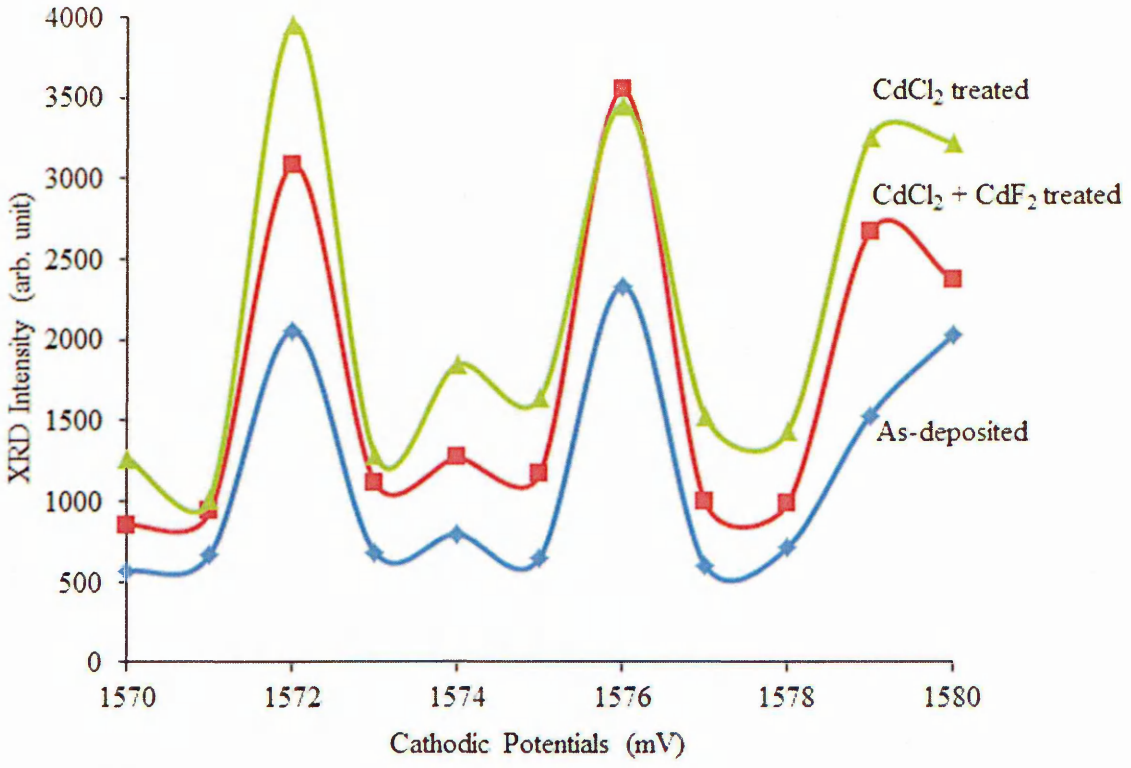

Figure 7.7: The comparison of XRD intensities of (111) peak for as-deposited, $CdCl_2$ and $CdCl_2 + CdF_2$ treated layers.

Figure 7.8 shows the crystallite sizes (in nm) for as-deposited, $CdCl_2$ treated and $CdCl_2 + CdF_2$ treated layers calculated using Debye-Scherrer equation. Trend lines are drawn for the purpose of seeing the effects of cathodic potentials on the size of the crystallites. The calculations are made by using (111) peaks as the reference. It can be seen that, in general, layers that had undergone heat-treatment gained larger crystallite sizes. Cathodic potentials had little influence on the size of the crystallites. This argument was deduced due to the absence of linear trend in the as-deposited curve. The average size of the crystallites was calculated for all three cases. The average crystallite sizes of the as-deposited, $CdCl_2$ treated and $CdCl_2 + CdF_2$ treated layers are 49.8 nm, 60.5 nm and 58.8 nm respectively. This means $CdCl_2$ treated samples gained slightly larger (1.7 nm larger) crystallites than $CdCl_2 + CdF_2$ treated layers. Generally, if crystallite sizes are calculated using Debye-Scherrer equation, samples with higher peaks should give higher crystallite sizes.

Further analysis on crystallite sizes were accomplished to find the reason behind the low intensity of (111) peaks observed in $CdCl_2 + CdF_2$ treated samples. Table 7.3 listed the crystallite sizes for $CdCl_2$ and $CdCl_2 + CdF_2$ treated thin films. For the as-

deposited layers, the values are not shown because device fabrication requires heat-treated layers.

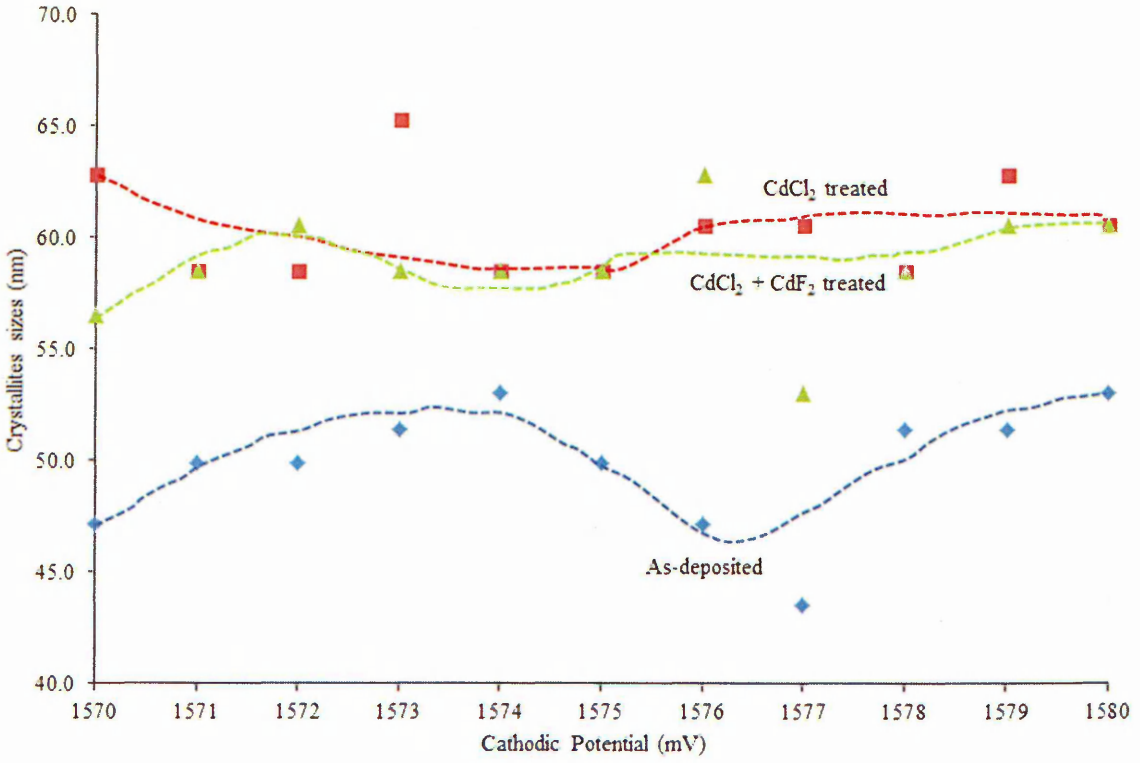

Figure 7.8: Crystallite sizes for as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers calculated using (111) peaks as the reference. The trend lines are drawn for each case.

In Table 7.3, the differences between the crystallite sizes from $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers are shown. If the crystallite sizes from $CdCl_2$ treated layers are larger than $CdCl_2$ + CdF_2 treated samples, the values are positive and vice-versa. Samples with higher (111) peak intensity as depicted in Figure 7.7 are given 'check mark' (✓).

It is interesting to see that $CdCl_2$ + CdF_2 treated samples grown at 1572 mV, 1574 mV, 1575 mV, 1578 mV and 1580 mV had equal or higher crystallite sizes compared to the $CdCl_2$ treated layers. It is also important to note that the XRD intensity of (111) peaks of these five $CdCl_2$ treated samples are higher than $CdCl_2$ + CdF_2 treated layers. This detail analysis unveils that even though the XRD intensities from $CdCl_2$ + CdF_2 treated layers are lower; the crystallite sizes could be equal or higher than $CdCl_2$ treated samples. This finding indicates that the lower intensities of (111) peaks from $CdCl_2$ + CdF_2 treated samples could be caused by another mechanism.

Addition of F before heat-treatment enhances improvement in solar cell devices (see later in section 9.3.1). Therefore $CdCl_2$ + CdF_2 treatment provides enhanced improvements than $CdCl_2$ treatment. As reported in reference [22], there exists a sudden phases when heat-treatment temperature is ~385°C, collapsing (111) peak and turning the material into more polycrystalline phase. It seem that the $CdCl_2$ + CdF_2 treatment is getting closer to this transition and hence just started to reduce the intensity of (111) peak.

Table 7.3: Crystallite sizes for $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers calculated using (111) peaks as the reference. The differences between the size of crystallites are shown. Samples with higher XRD intensities are given 'check mark' (✓).

Cathodic potential (mV)	Crystallite size (nm)			Higher (111) peak intensity	
	$CdCl_2$ treated (A)	$CdCl_2$ + CdF_2 treated (B)	A-B	A	B
1570	62.8	56.5	6.3	✓	
1571	58.5	58.5	0.0		✓
1572	58.5	60.6	-2.1	✓	
1573	65.2	58.5	6.7	✓	
1574	58.5	58.5	0.0	✓	
1575	58.5	58.5	0.0	✓	
1576	60.6	62.8	-2.2		✓
1577	60.6	53.0	7.6	✓	
1578	58.5	58.5	0.0	✓	
1579	62.8	60.6	2.2	✓	
1580	60.6	60.6	0.0	✓	

7.3.3 Optical absorption spectroscopy

Optical absorption spectroscopy studies were conducted by dividing one sample into three pieces to observe the differences between as-deposited, $CdCl_2$ and $CdCl_2$ +

CdF_2 treated thin films. Figure 7.9 shows seven optical absorption curves for as-deposited samples only. These curves are divided into two groups, A and B.

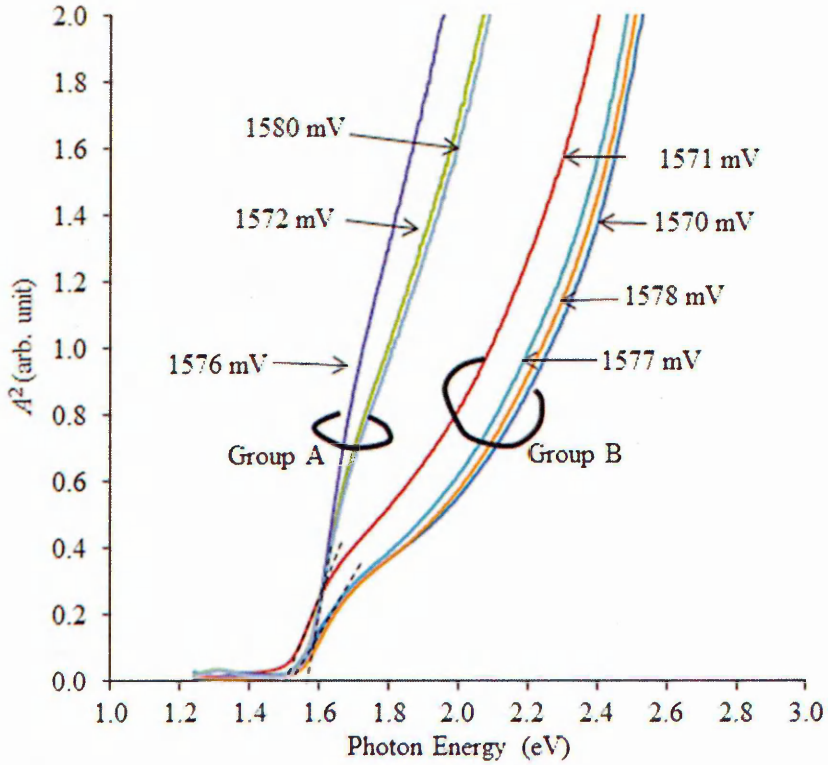

Figure 7.9: Optical absorption curves for as-deposited samples grown at different cathodic potentials.

For group A, the thicknesses are higher than 145 nm. For group B the thicknesses are between 80 nm to 100 nm. The thickness values were taken from Table 7.1. The absorbance of photons from group A is stronger than group B due to the higher thickness. As we can see, sample grown at 1576 mV has the strongest absorbance in group A because the thickness of this layer is the highest (164 nm). The bandgaps of group A are 1.55 eV while for group B, the bandgaps are 1.50 eV. CdTe bandgap between 1.44 eV to 1.50 eV are well accepted values in literature [23-24]. The larger bandgaps of group A could be caused by the quantum effects due to smaller grains. This can also be caused due to the presence of pin-holes and therefore light passing through these pin-holes.

When these samples were heat-treated in air at 400°C for 15 minutes after $CdCl_2$ treatment, all samples showed 1.50 eV bandgap as depicted in Figure 7.10. The decrease of bandgap from 1.55 eV to 1.50 eV might be resulted from the reaction of excess Cd from $CdCl_2$ and Te precipitates thus producing additional useful CdTe [20].

This process can also make the grains larger and cover pin-holes in the layer. As a result, the bandgap values can be reduced. Major improvement can be seen at the 'knee' area where the curves were 'straighten' after heat-treatment. Some improvements can also be seen in particular samples. For example, samples grown at 1570 mV, 1571 mV, 1572 mV and 1580 mV had an improved absorbance. Other samples also gained improvement in absorbance curves but it was minimal.

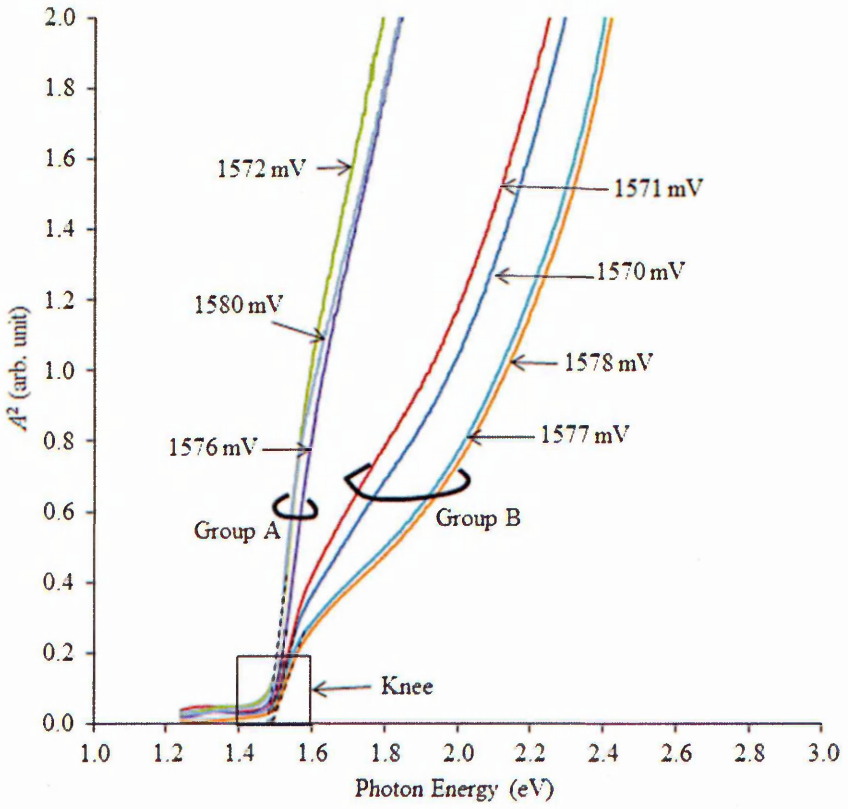

Figure 7.10: Optical absorption curves for several samples heat-treated at 400°C for 15 minutes after $CdCl_2$ treatment.

Finally, Figure 7.11 shows optical absorption curves for CdTe heat-treated with $CdCl_2$ + CdF_2. All layers showed similar bandgap (1.50 eV) and curves straightening at the 'knee' area. These results are similar to the $CdCl_2$ treated layers. Samples grown at 1572 mV, 1577mV and 1578 mV showed improved absorbance curves compared to the as-deposited layers. From optical absorption studies, it was found that the improvements of absorbance curves are random. This means, the improvement of the absorbance curves for annealed samples was unpredictable. Optical absorption studies revealed that it is important to have similar amount of chemicals on top of CdTe surface and also

similar processing conditions. This is because residual chemicals such as $CdCl_2$ and Cd_3TeO_6 could change the absorption curves.

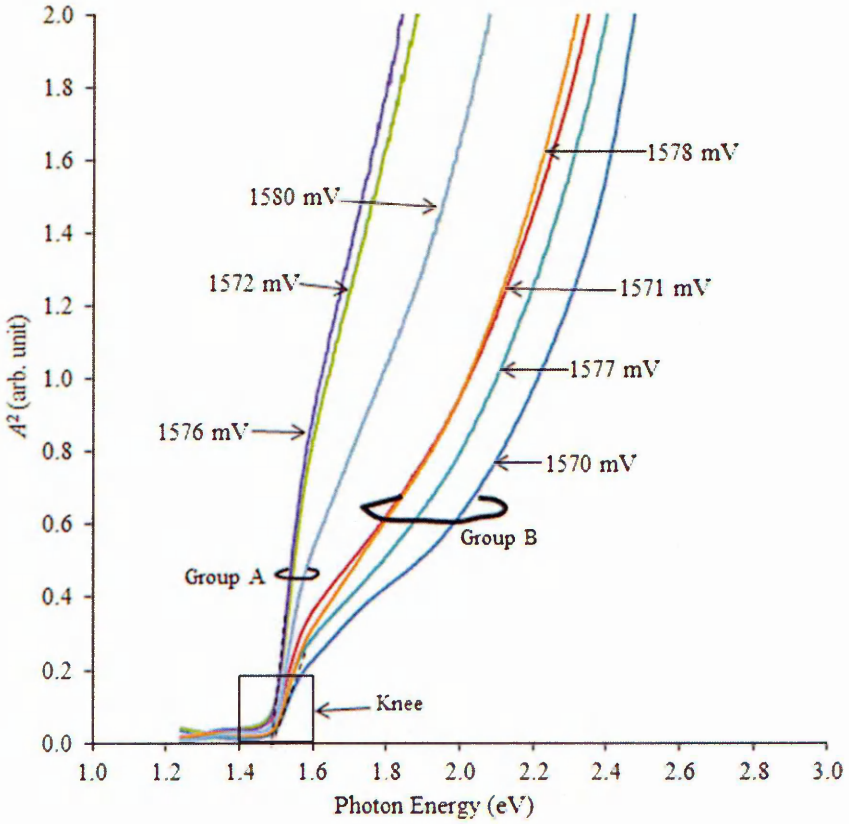

Figure 7.11: Optical absorption curves for several samples heat-treated at 400°C for 15 minutes after $CdCl_2$ + CdF_2 treatment.

7.3.4 Scanning electron microscopy (SEM)

In SEM, the morphological studies were conducted on samples with the highest (111) peak from Figure 7.3. Samples grown at 1572 mV, 1576 mV and 1580 mV had the highest (111) peaks. The morphological studies were carried out to see the effects of chemical treatments towards the surface of CdTe thin films. All images were obtained with 60 000x magnification. Figure 7.12 shows the SEM images for as-deposited CdTe thin films. In general, very fine crystallites can be seen clearly in these images. The size of these crystallites was estimated to be below 50 nm which is in good agreement with the calculated values using Debye-Scherrer equation. These fine crystallites sitting compactly with each other thus creating 'faded' grain boundaries.

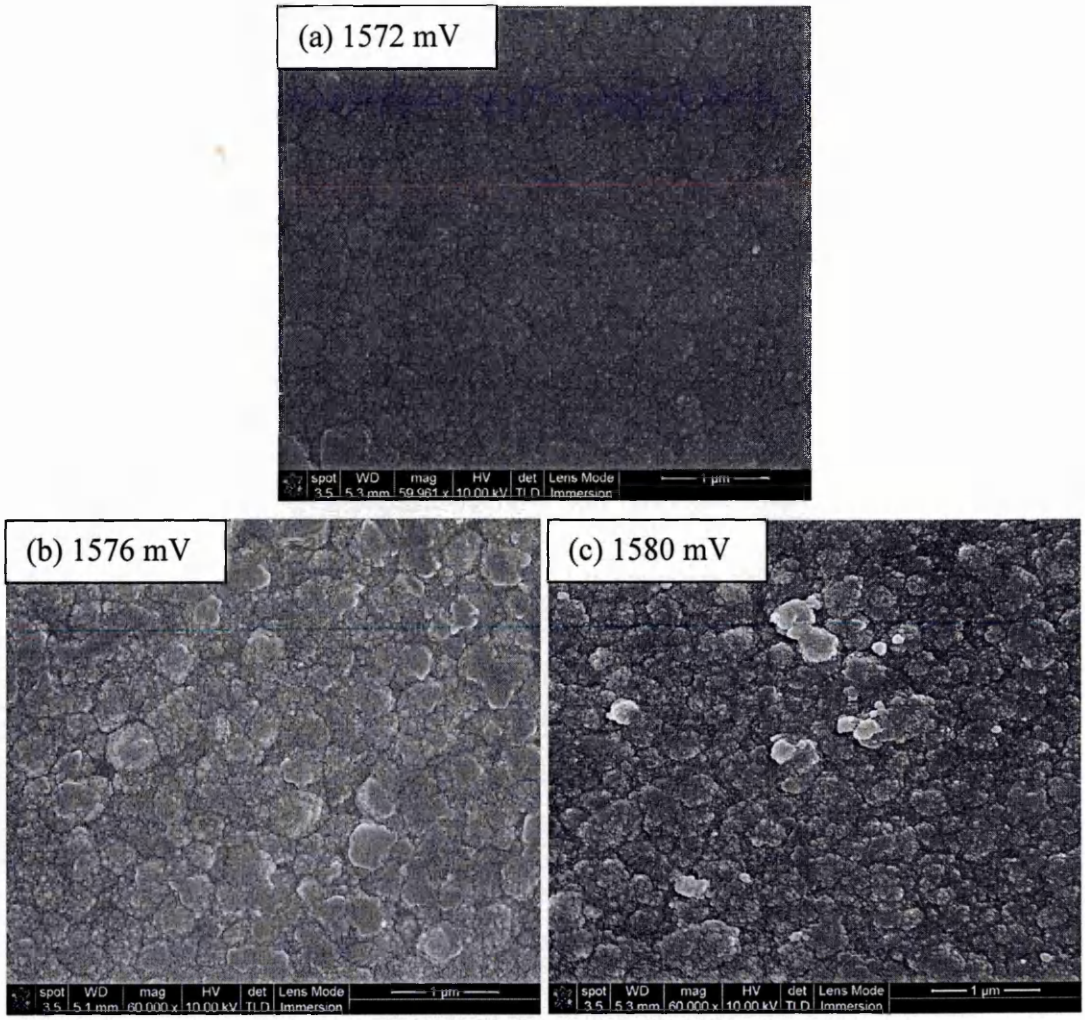

Figure 7.12: SEM images for as-deposited CdTe layers electroplated at different cathodic potentials.

The SEM images for $CdCl_2$ treated layers are shown in Figure 7.13. After heat-treatment in air at 400°C for 15 minutes, the fine crystallites seemed disappeared due to agglomerations. The grain boundaries seemed 'melted' due to the high temperature reactions. This leads to the overlapping and assimilating of the grain boundaries with each other. If the overlappings are imperfect, pin-holes can be seen. The pin-holes are clearly shown in sample grown at 1580 mV. If the coalescence of small grains take place and larger grains grow normal to the surface, more pin-holes can appear in the layers.

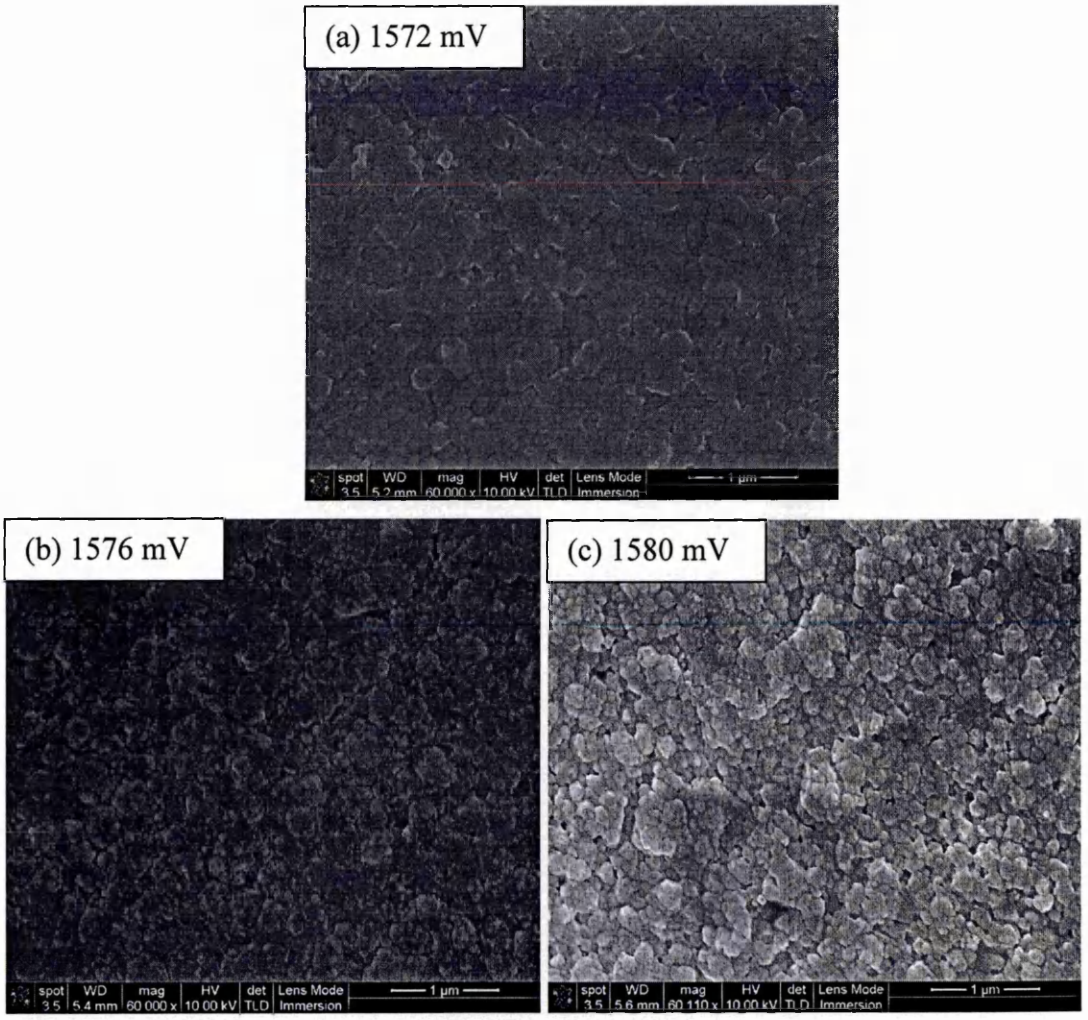

Figure 7.13: SEM images for CdTe samples heat-treated at 400°C for 15 minutes after $CdCl_2$ treatment.

Finally, the electrodeposited CdTe layers that undergone annealing at 400°C for 15 minutes after $CdCl_2$ + CdF_2 treatment are depicted in Figure 7.14. If comparisons are made between $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers, there are morphological similarity and dissimilarity between these layers. Firstly, the fine crystallites in $CdCl_2$ + CdF_2 treated layers also disappear after heat-treatment. This is similar to $CdCl_2$ treated layers. However, the grain boundaries of the $CdCl_2$ + CdF_2 treated layers (1572 mV and 1576 mV) show clear boundary lines and not overlapping between each other. Sample grown at 1580 mV shows 'melting' behaviour but this might be due to the excess chemicals on the surface. Perhaps, this could be the reason why the optical absorbance of this layer was weaker (refer to Figure 7.11 - group A).

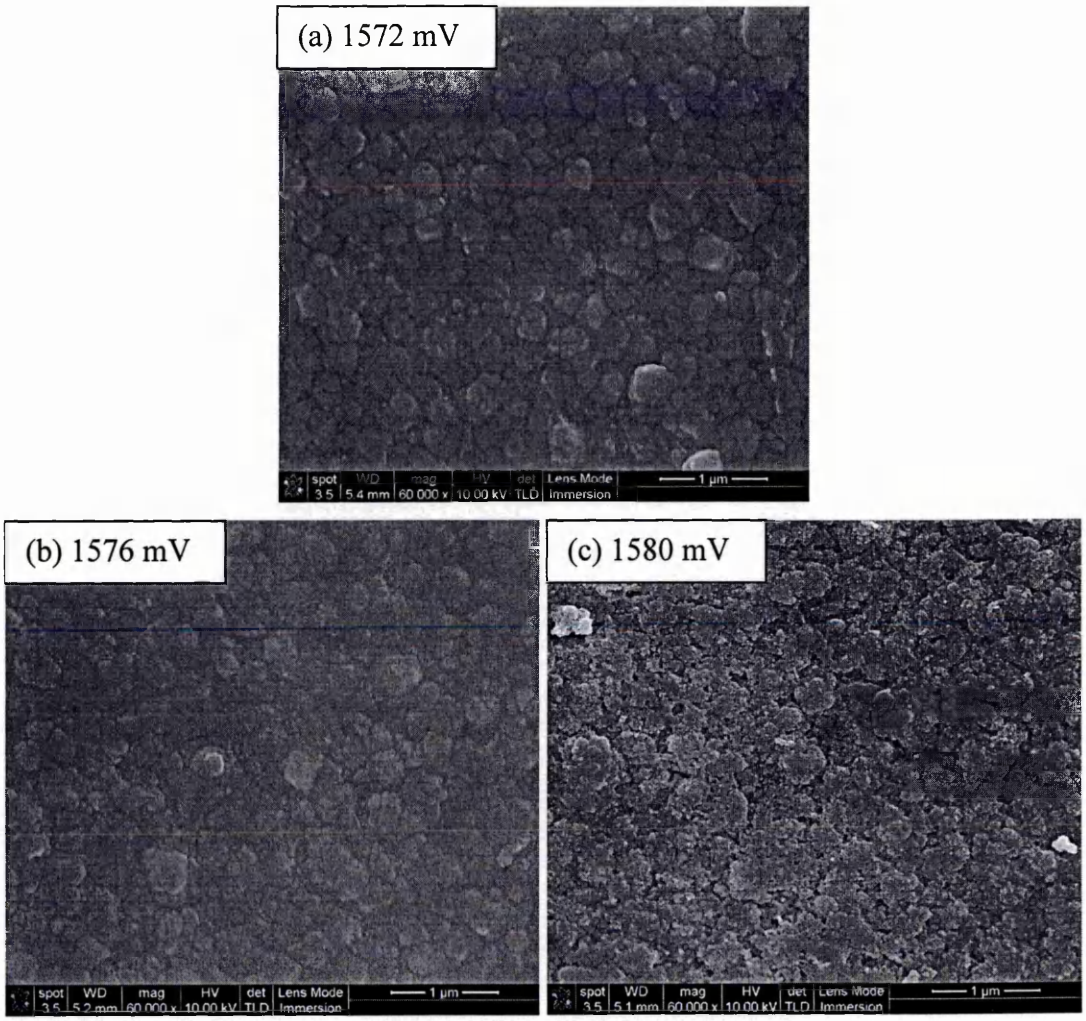

Figure 7.14: SEM images for CdTe samples heat-treated at 400°C for 15 minutes after $CdCl_2$ + CdF_2 treatment.

7.3.5 Photoelectrochemical (PEC) cell measurements

To check the effects of cathodic potentials upon the electrical conductivity of the electrodeposited CdTe layers, PEC measurements were carried out. Several samples were grown with different cathodic potentials from 1571 mV to 1580 mV. Each sample was cut into 3 pieces so that the chemical treatments can be conducted separately. Table 7.4 shows the values from PEC signal measurements and Figure 7.15 shows the curves plot for as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers.

Table 7.4: PEC measurements for as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers

Cathodic potential (mV)	PEC signal (mV)		
	As deposited	$CdCl_2$ treated	$CdCl_2$ + CdF_2 treated
1571	27	16	-42
1572	28	15	-31
1573	22	16	-14
1574	-7	24	-12
1575	-27	10	-44
1576	-30	11	-40
1577	-25	2	-45
1578	-32	5	-43
1579	-37	-31	-51
1580	-55	-37	-66

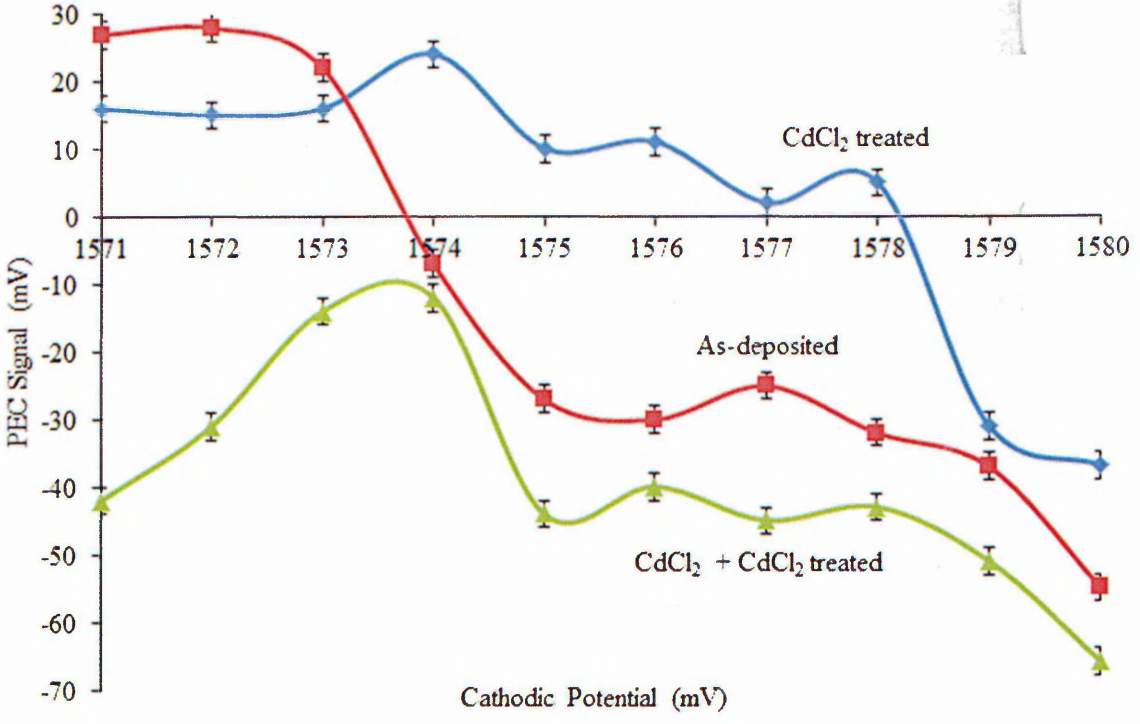

Figure 7.15: PEC measurement curves for as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated layers.

Figure 7.15 shows that the electrical conductivity of electrodeposited CdTe can be altered between p-type to n-type simply by changing the cathodic potentials. For as-deposited samples, the electrical conductivity was p-type from 1571 mV to 1573 mV

and was n-type from 1574 mV to 1580 mV. Results presented in Table 7.4 and Figure 7.15 are in good agreement with work published by Panicker *et al* and Takahashi *et al* [5,8]. When these samples were subjected to chemical treatments, interesting trends were observed.

After $CdCl_2$ treatment, the conductivity of p-type layers moves towards n-type (refer to 1571 mV to 1573 mV). However, the conductivity of n-type layers moves towards p-type after $CdCl_2$ treatment (refer to 1571 mV to 1580 mV). It is well known that chlorine usually acts as the n-type dopant for CdTe. But chlorine can also be the p-type dopant when it forms complexes with unknown defects in CdTe [20]. This reaction perhaps could explain why the electrical conductivity of n-type layers moved towards p-type after $CdCl_2$ treatment. As for the p-type layers, the conductivity moved toward n-type due to doping effects by chlorine and also the reaction between Te precipitates and excess cadmium from $CdCl_2$, hence creating additional useful CdTe.

In the case of $CdCl_2$ + CdF_2 treatment, all electrodeposited layers were n-type after heat treatment regardless of the initial conductivity type. At this stage, it is reasonable to postulate that fluorine acts better than chlorine as the n-type dopant due to the fact that the atomic radius of fluorine atoms is smaller compared to other elements in group VII [25]. Perhaps fluorine atoms could diffuse more easily in CdTe crystals and then create bonds with host atoms. This is analogous to the phosphorus-silicon bonding in silicon based devices.

The changing of conductivity type after chemical treatments means there is movement of Fermi level (E_F) within the bandgap of CdTe. The position of Fermi level was determined using ultraviolet photoelectron spectroscopy (UPS).

7.3.6 Ultraviolet photoelectron spectroscopy (UPS)

The analysis to determine the position of valence band maximum (E_V) and the movement of Fermi level (E_F) were fulfilled by performing ultraviolet photoelectron spectroscopy (UPS) mesurement. Measurements were conducted using VG Scientific MultiLab 3000 surface analysis system by our collaborator at the Conn Centre for Renewable Energy Research at University of Louisville, USA. This system was assisted with CLAM4 hemispherical electron energy analyzer and a differentially-pumped He cold cathode capillary discharge UV lamp with base chamber pressure ~10^{-9} Torr. The samples were excited with a resonance line He-I ($h\nu$ = 21.22 eV).

To observe the movement of Fermi level, $CdCl_2$ treatment was carried out twice. The first annealing was performed at 400°C for 8 minutes and the second heat-treatment was conducted at 400°C but for 16 minutes.

For UPS studies, half of the one CdTe sample was covered with sputtered gold film and the other half was left exposed. The UPS spectras were obtained from gold film and CdTe. Figures 7.16(a), (b) and (c) are the UPS spectrums obtained from the gold film.

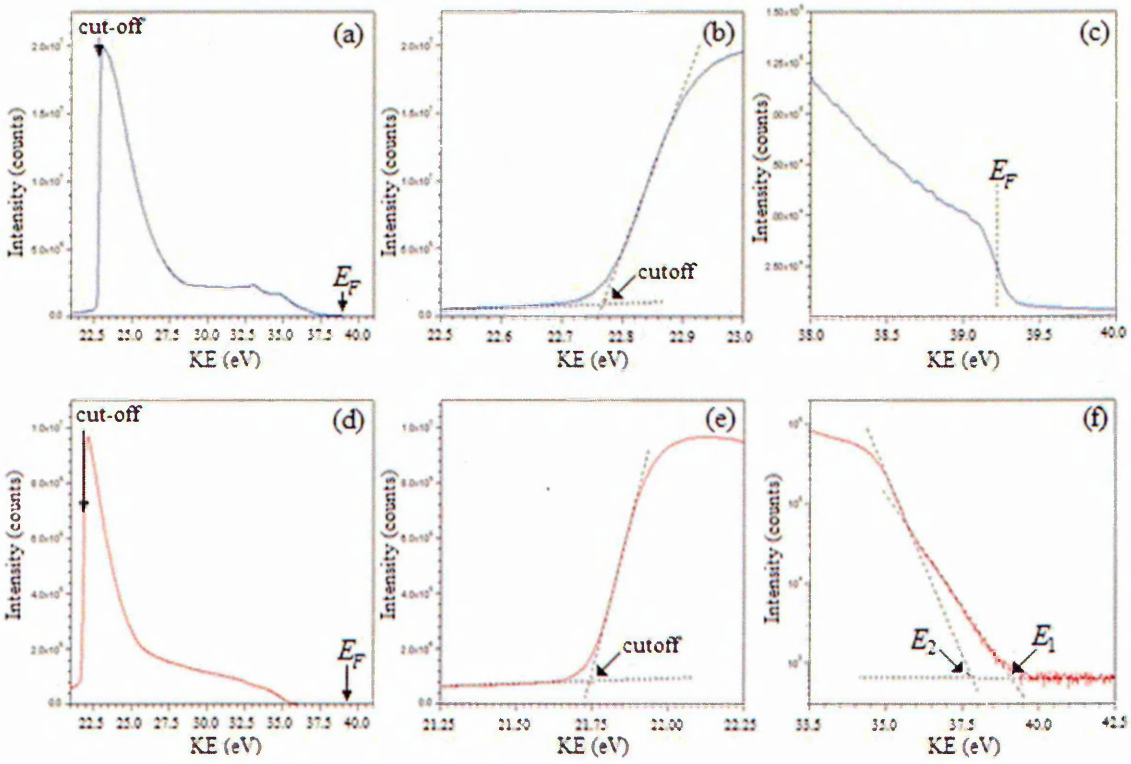

Figure 7.16: Typical UPS spectra obtained for gold film and CdTe layer; (a) UPS spectrum obtained for gold layer, (b) low KE cut-off edge for gold, (c) high KE Fermi level edge for gold, (d) a typical UPS spectrum obtained for CdTe layer, (e) low KE cut-off for CdTe and (f) high KE cut-off of valence band edge for CdTe.

From Figure 7.16(a) the low kinetic energy (KE) and high kinetic energy cut-offs can be seen clearly. The low kinetic energy cut-off is the indication of ionized electrons from the deepest valence band states. Meanwhile, the high kinetic energy cut-off is the indication of electron emission from the states located at the Fermi level. Figure 7.16(b) and Figure 7.16(c) are the magnification of Figure 7.16(a) so that the kinetic energy at both cut-offs can be seen clearly. The Fermi level for gold film was determined by taking the half maximum of step height (refer to Figure 7.16(c)).

Figures 7.16(d), (e) and (f) represent the UPS spectra for CdTe. For CdTe semiconductor, the location of Fermi level lies within the bandgap and could also be pinned at deep state levels. This makes the Fermi step difficult to detect. This situation is different in metallic materials such as gold where the position of Fermi level is at the top of the valence band. Hence, Fermi step can be determined easily. In the case for CdTe layers, Fermi level was assumed to equalize across the interface because it was in direct contact with the gold film. Therefore, the position of Fermi level was derived similarly in the way used for gold film.

The bandgap of CdTe was assumed to be 1.44 eV for doping the position of Fermi level. Table 7.5 shows the results for as-deposited CdTe. The first column from the left is the high kinetic energy cut-off of the gold film. Next to it is the column for the high kinetic energy cut-off of the CdTe. Two values were given since no clear cut-off could be seen (refer to Figure 7.16(f)). After obtaining both cut-offs, the position of Fermi level can be determined. Results showed that the position of Fermi level for as-deposited CdTe thin film was 0.36 eV below the conduction band minimum or 1.08 eV above the valence band maximum. This means the as-deposited CdTe was n-type. The results obtained are in good agreement with PEC measurements since this layer was electrodeposited at 1576 mV.

Table 7.5: Summary of several parameters measured by UPS for as-deposited CdTe.

Au E_F cut-off (eV)	CdTe E_F cut-off (eV)		E_F - E_V (eV)		E_C - E_F (eV)		Marked as
39.22	38.11	38.17	1.11	1.05	0.33	0.39	S_1
			1.08		0.36		

After first step of $CdCl_2$ treatment, the position of Fermi level moved towards the middle of the bandgap as shown in Table 7.6. It means that the conductivity type of electrodeposited CdTe had tendency to change from n-type towards p-type after annealing. This result once again shows consistency with the PEC measurements. After first step of $CdCl_2$ treatment, the location of Fermi level was 0.55 eV below the conduction band or 0.89 eV above the valence band maximum.

Table 7.6: Summary of several parameters measured by UPS after the first step of $CdCl_2$ treatment.

Au E_F cut-off (eV)	CdTe E_F cut-off (eV)	E_F - E_V (eV)	E_C - E_F (eV)	Marked as
39.22	38.33	0.89	0.55	S_2

After the second step of $CdCl_2$ treatment, the position of Fermi level moved closer to the conduction band minimum. Fermi level of CdTe finally settled at 0.18 eV below the conduction band minimum. All the parameters are shown in Table 7.7. This time, $CdCl_2$ treatment made the conductivity of CdTe behave more n-type. The movement of Fermi level closer to the conduction band after the second step treatment could be interpreted as doping effect if chlorine replaces Te.

Table 7.7: Summary of several parameters as measured by UPS after the second step of $CdCl_2$ treatment.

Au E_F cut off (eV)	CdTe E_F cut off (eV)	E_F - E_V (eV)	E_C - E_F (eV)	Marked as
39.22	37.96	1.26	0.18	S_3

Fermi level positions of CdTe with respect to the conduction band for as-deposited, the first and second step of $CdCl_2$ treatments are tabulated in Table 7.8. The positions of Fermi level in the bandgap and its movements are shown in Figure 7.17 for easy reference.

Table 7.8: Summary of Fermi level positions of electrodeposited CdTe with respect to the conduction band (E_C - E_F) for as-deposited and after $CdCl_2$ treatments.

E_C - E_F (eV) For as-deposited CdTe	E_C - E_F (eV) After 1st $CdCl_2$ treatment	E_C - E_F (eV) After 2nd $CdCl_2$ treatment
0.36	0.55	0.18

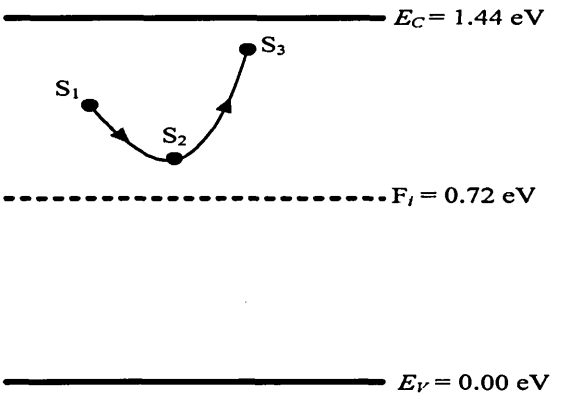

Figure 7.17: The initial Fermi level position for as-deposited CdTe thin film (S_1) and its movement after $CdCl_2$ treatments (S_2 for step 1 and S_3 for step 2).

Since conductivity type of this CdTe layer and also the Fermi level positions are known, the electron concentration can be calculated from Equation (7.3) [26];

$$n = N_c \exp\left(\frac{-(E_C - E_F)}{kT}\right) \tag{7.3}$$

Where;

n is the electron concentration (cm^{-3})

N_c is the effective density of states in the conduction band ($7.9 \times 10^{17}\ cm^{-3}$)

k is the Boltzmann constant ($1.38 \times 10^{-23}\ JK^{-1}$)

T is the temperature (300 K).

The calculated electron concentrations are displayed in Table 7.9. This result provides very useful information about the doping effect in $CdCl_2$ treatment. In addition to increasing the grain sizes, improving the crystallinity and removing of defects, etc, internal & external doping also happens simultaneously during $CdCl_2$ treatment.

Table 7.9: The calculated electron concentrations with respect to the position of Fermi level in the bandgap.

Fermi level position	$E_C - E_F$ (eV)	n (cm^{-3})
S_1	0.36	7.26×10^{11}
S_2	0.55	4.73×10^{8}
S_3	0.18	7.57×10^{14}

Schulmeyer *et al* had reported that the Fermi level could settle above or below the midgap after $CdCl_2$ treatment [27]. This work determined the position of Fermi level using photoelectron spectroscopy on close space sublimated CdTe (CSS-CdTe) grown at ANTEC. They have measured positions of Fermi level and the final devices efficiency after different $CdCl_2$ treatment. They also plotted the η versus Fermi level position in the bandgap and showed that the highest efficiency was achieved when the Fermi level is in the upper half of the bandgap. This means the high performance devices are obtained when the CdTe material has n-type electrical conduction. The UPS work presented here have confirm this is the case and both electrodeposited CdTe and CSS-CdTe behave in the same way.

7.3.7 D.C electrical conductivity measurements

To study the resistivity of electrodeposited CdTe semiconductors, three samples with thickness of 540 nm was used. Since CdTe can exist as n-type, i-type and p-type semiconductors [17], the PEC measurement had to be carried out upon all three samples before either gold or aluminium back contacts can be evaporated. Since all samples have shown n-type conductivity, aluminium contacts with the size of 0.0314 cm^2 were evaporated on top of the CdTe layers using a vacuum evaporator at pressure of 10^{-6} Torr. The resistivity of the as-deposited, $CdCl_2$ treated and $CdCl_2$ + CdF_2 treated CdTe were calculated using Equation (5.9) and (5.10) from Chapter 5. Results of the electrical resistivity (ρ) of electrodeposited CdTe materials using current-voltage (I-V) measurement are shown in Table 7.10.

Table 7.10: The electrical resistivity calculated from I-V measurements for as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated CdTe layers.

	Resistivity (ρ) (Ωcm)				
Sample	1st	2nd	3rd	4th	Average
As-deposited	12583	12350	11822	13404	12540
$CdCl_2$ treated	9088	9665	8010	8039	8071
$CdCl_2$ + CdF_2 treated	9850	9148	9262	9468	9432

Similar to CdS resistivity measurements, 4 different points were measured and the averages of these measurements were used as the final value. The resistivity of as-

deposited layers is the highest among these three cases with 1.25×10^4 Ωcm. The resistivity values obtained for as-deposited layers are in good agreement with other work reported in literatures. In general, the reported resistivity values of the electrodeposited CdTe layers are in the range of 10^4 Ωcm to 10^7 Ωcm [28-30].

Clearly from Table 7.10, the best average resistivity (8.0×10^3 Ωcm) was obtained when the layers were heat-treated with $CdCl_2$. When fluorine was included, the average resistivity raised up to 9.4×10^3 Ωcm. The increase of resistivity after fluorine inclusion might be due to the additional doping effects of fluorine. This study reveals that resistivity of electrodeposited layers could be reduced by chemical treatments.

7.4 Conclusion

CdTe thin films have been successfully electrodeposited at 80°C and pH = 2.00 ± 0.02 in an aqueous solution employing 2-electrode system. It was found that the current density was influenced by Te dissolution in the electrolyte. The conductivity type of as-deposited CdTe materials can be altered between n-type and p-type simply by changing the deposition voltage.

Optical absorption spectroscopy showed that thicker CdTe layers will absorb photons more efficiently. If chemically treated with $CdCl_2$ or $CdCl_2$ + CdF_2, the bandgap of the electrodeposited CdTe thin films decreased from 1.55 eV to 1.50 eV regardless the cathodic potentials applied.

Heat treatment in air after $CdCl_2$ or $CdCl_2$ + CdF_2 treatment improved the crystallinity and also enlarged the crystallite sizes of electrodeposited CdTe thin films. The mixture of chlorine and fluorine produced better surface morphology than layers treated with chlorine only. The conductivity of CdTe layers that have been chemically treated with $CdCl_2$ moved towards n-type for originally p-type layers and vice versa. However, after the inclusion of fluorine, the conductivity remained n-type regardless of the deposition voltage and initial electrical conductivity. This is an important finding due to the fact that this project is more focused towards the fabrication of n-n hetero-junction CdS/CdTe solar devices.

UPS measurements also confirmed that the conductivity of as-deposited n-CdTe changed towards p-CdTe after the first $CdCl_2$ treatment. External doping could also happen after the second $CdCl_2$ treatment because when analyses were carried out, electron concentration was found to be higher than as-deposited CdTe. The as-deposited

CdTe layers showed high resistivity ~1.25 × 10^4 Ωcm. After chemical and heat treatments, the resistivity of the electrodeposited layers reduced to ~(8-9) × 10^3 Ωcm.

After thorough investigations, it was found that chemical treatment of CdTe layers is a very important step not to be missed for fabrication of high efficiency photovoltaic devices (see later in Chapter 9). This is because this step is beneficial in inproving the structural, optical, morphological and electrical conductivity of the electrodeposited CdTe thin films.

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8.1 Introduction

Zinc telluride (ZnTe) is the third electrodeposited thin film semiconductor that has been developed in this research project. The development of ZnTe was intended to be used as the p-type window layer or as the back contact material between CdTe and metal in glass/FTO/CdS/CdTe/ZnTe/metal thin film solar cell configuration.

Similar to CdS and CdTe, ZnTe is also a direct bandgap II-VI semiconductor. Stoichiometic ZnTe thin films have brick-red colour. The reported bandgap values for ZnTe in literature are between 2.10 eV to 2.26 eV [1-3]. Various deposition techniques have been employed to deposit ZnTe semiconductor. Among the techniques are thermal evaporation [4], molecular beam epitaxy [5] and metal organic chemical vapour deposition [6].

Electrodeposition of ZnTe layers has been reported by several authors. Mahalingam *et al*, Rakhsani and Pradeep, Neumann-Spallart and Koenigstein are few reported publications regarding the electrodeposition of ZnTe using aqueous solutions [7-9]. Some groups have also reported the electrodeposition of ZnTe materials using non-aqueous solutions. Chaure *et al* and Heo *et al* are among the authors that published their work on electrodeposition of ZnTe in the non-aqueous medium [10,11].

However, all of the electrodeposition work by the authors mentioned above was carried out using 3-electrode system. The first report about the electrodeposition of ZnTe employing 2-electrode system was reported in 2010 by Diso [12]. The experimental work reported by Diso was conducted using aqueous solution with zinc sulfate ($ZnSO_4$) as the precursor. This chapter reports about electrodeposition of ZnTe layers utilizing 2-electrode system with zinc chloride ($ZnCl_2$) as the precursor.

The electrodeposited ZnTe materials were characterized by x-ray diffraction (XRD), optical spectroscopy, scanning electron microscopy (SEM), x-ray fluorescence (XRF), photoelectrochemical (PEC) cell measurement and D.C. electrical measurement to study the structural, optical, morphological, compositional and electrical properties respectively. These characterization techniques were utilized in order to identify the best deposition voltage for obtaining the near stoichiometric ZnTe semiconductor.

8.2 Preparation of ZnTe electrolyte bath

Zinc chloride ($ZnCl_2$) powder with 98% purity was used as the precursor to prepare an aqueous electrolyte for deposition of ZnTe thin films. $ZnCl_2$ with weight of 5.45 g was measured with electronic weight balance and then diluted in a beaker containing 800 ml of deionized water making the molarity of the bath equals 0.005M. The chemical was supplied by Sigma-Aldrich, UK and used without any treatment. The solution was stirred overnight before being purified for 40 hours. Zinc chloride bath is a stable solution with no precipitation observed even at high temperature. The pH of the bath was adjusted to 4.50 ± 0.02 using diluted hydrochloric acid (HCl) and ammonium hydroxide (NH_4OH).

Electrodeposition of ZnTe layers was carried out at temperature of 80°C. Since the electrodeposition was carried out using 2-electrode system, the reference electrode was omitted. The glass/FTO substrate was used as the cathode while a high purity carbon rod (99.995% purity) was used as the anode.

The source of Te was obtained from TeO_2 (99.999% purity) which was also supplied by Sigma-Aldrich, UK. Te solution was prepared separately by dissolving 0.05 g of TeO_2 powder in 100 ml volumetric flask containing a mixture of concentrated HCl and deionized water. After complete dissolution of TeO_2 the solution was diluted by adding deionized water into the flask. Prior to deposition of ZnTe thin films, 2 ml of TeO_2 solution was added into $ZnCl_2$ bath using a pipette. The glass/FTO substrates were prepared in similar ways as in electrodeposition of CdS and CdTe work.

8.3 Results and discussions

8.3.1 Voltammogram

Figure 8.1 shows the voltammogram of an aqueous electrolyte containing 0.05M of $ZnCl_2$ and 2 ml of TeO_2 solution. The voltammogram was recorded at T = 80°C and pH = 4.50 ± 0.02 by using computerised Gillac potentiostat. The scan rate employed was 3 mVs^{-1}. The result of voltammogram with a complete forward/reverse cycle is shown in Figure 8.1. Similar to electrodeposition of CdTe, Te should deposit first on the glass/FTO substrates because the reduction potential of Te (E_o = + 0.53 V) is more positive than Zn (E_o = -0.76 V). The current density peaks at 950 mV (point A) which

meant the reduction of $HTeO_2^+$ to Te. This potential is different from that for CdTe deposition (Figure 7.1); this is because of different chemical composition of the baths used. The balanced equation for the reaction is given as:

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \quad (8.1)$$

After the peak at point A, the current density reduces a little before peaking again at point B. At this point, the electrodeposition of Zn begins. The reduction of Zn^{+2} cations to form ZnTe is given as:

$$Zn^{2+} + Te + 2e^- \rightarrow ZnTe \quad (8.2)$$

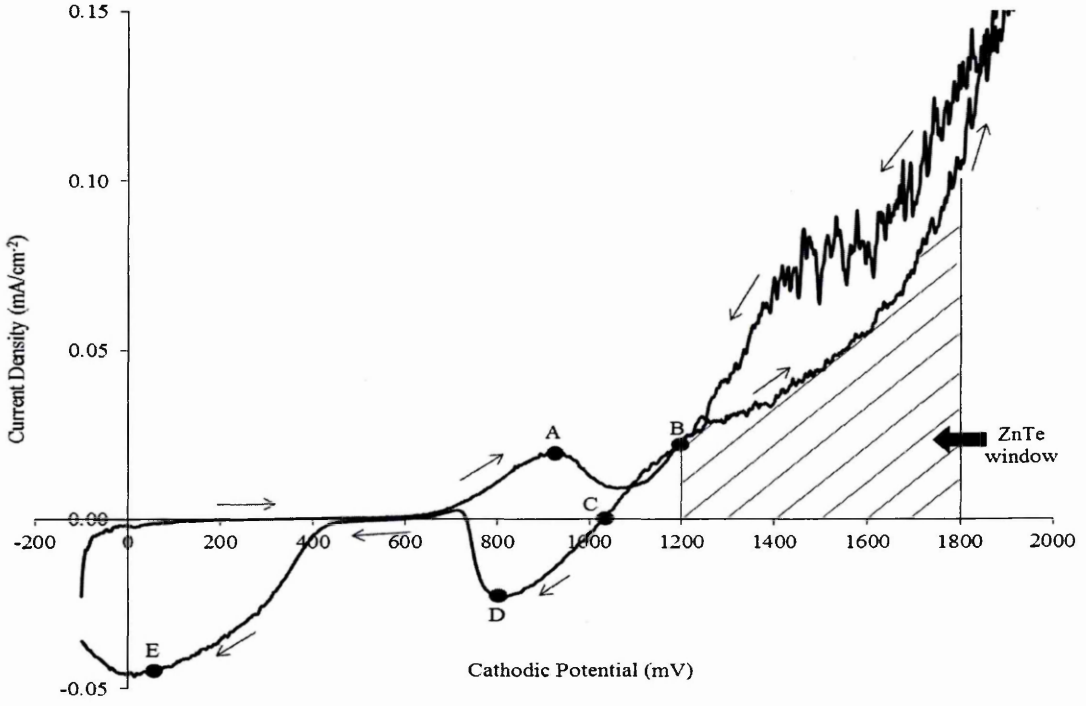

Figure 8.1: The cyclic voltammogram of an aqueous electrolyte containing 0.05M of $ZnCl_2$ and 2 ml of TeO_2 at pH = 4.50 ± 0.02 and T = 80°C [13].

Beyond point B, the current density increases drastically due to the electrolysis of water. It is important to note that the minimum cathodic potential needed to break the water molecule is ~1200 mV [14]. From the voltammogram, the suitable applied cathodic potentials for the formation of near stoichiometric ZnTe is between 1200 mV to 1800 mV. On the reverse cycle, the dissolution of elemental Zn and Zn from ZnTe

layers starts at ~1020 mV and ~800 mV (point C and D) respectively. The dissolution of Te can be seen at ~75 mV (point E) accompanied by high negative current.

8.3.2 X-ray diffraction (XRD)

Following the result from the voltammogram, the suitable deposition window to electrodeposit near stoichiometric ZnTe semiconductors was found to be in the range of 1200 mV to 1800 mV. Therefore, several samples were grown with 25 mV intervals starting from 1200 mV up to 1800 mV. All layers were deposited for 60 minutes. After the deposition process completed, the samples were taken out from the electrolyte and dried under a stream of nitrogen gas for 5 seconds.

Figure 8.2 shows the x-ray diffraction (XRD) patterns for several samples electrodeposited for 60 minutes. The lowest cathodic potential shown here is 1225 mV. At this cathodic potential, the peaks associated with ZnTe are absent.

Besides the FTO peaks, only (101) peak could be seen which belongs to hexagonal Te. This peak match with JCPDS files no.00-036-1452. The absence of Zn or ZnTe peaks indicates that at lower cathodic potentials, ZnTe could not be deposited due to the insufficient voltage to drive Zn^{2+} cations to accept two electrons to form Zn atoms.

As the cathodic potentials were increased, a weak (111) cubic ZnTe peak emerged at $2\theta = 25.5^{o}$ after higher cathodic potential (1300 mV) was applied. The XRD intensity of this peak continuously getting higher as the cathodic potential was increased. The highest (111) peak is observed when the cathodic potential equals 1675 mV, because at this cathodic potential, the composition of Zn and Te atoms is very close to 1:1 ratio. If the cathodic potentials were increased beyond 1675 mV, the intensity of (111) peak decreased again due to the higher content of zinc incorporated in the layers.

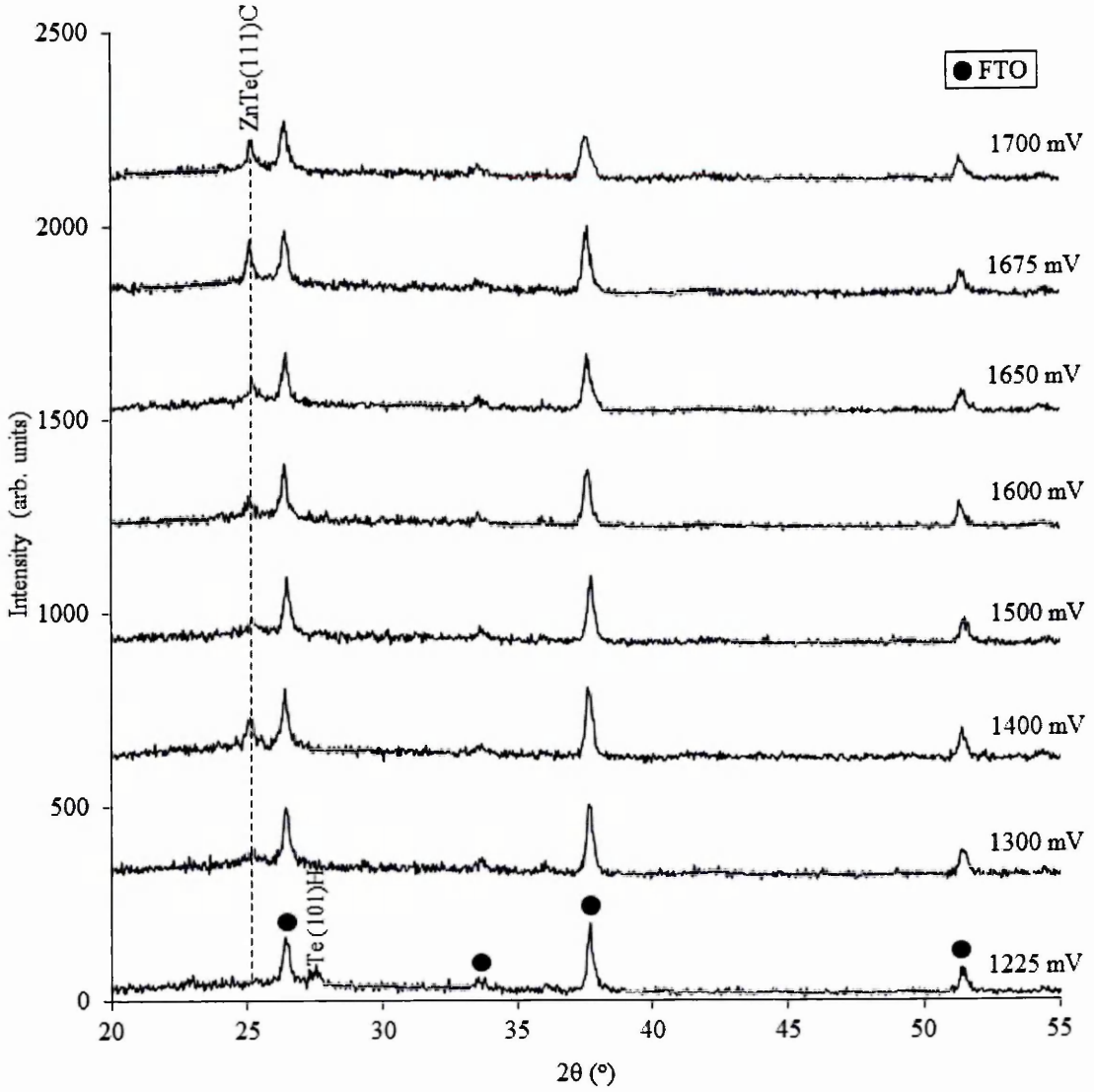

Figure 8.2: The XRD patterns for layers grown at different cathodic potentials for 1 hour. The highest (111) peak is observed when cathodic potential equals 1675 mV [13].

The search for the optimum cathodic potential was continued by growing several samples at the vicinity of 1675 mV. Figure 8.3 shows a new set of samples grown at the vicinity of 1675 mV.

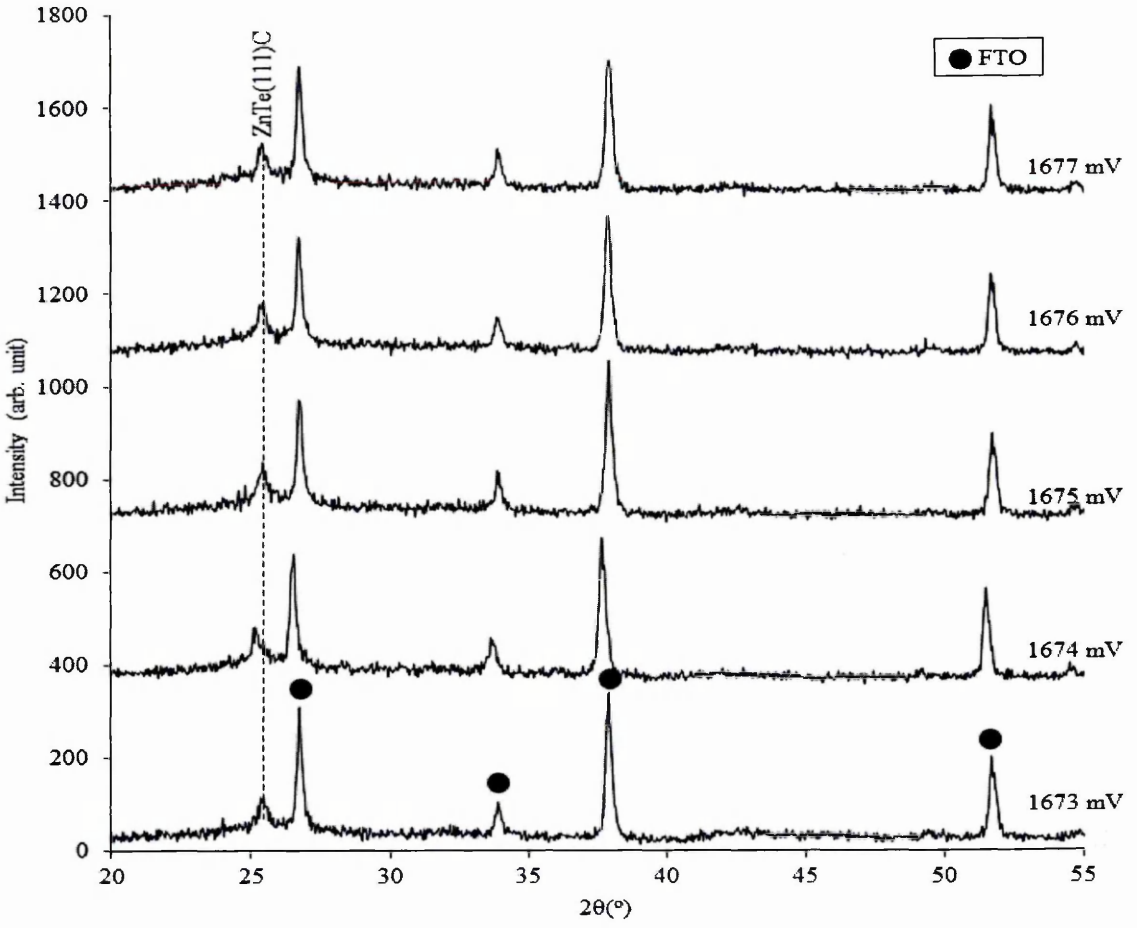

Figure 8.3: The XRD patterns for layers grown at the vicinity of 1675 mV. All samples were grown with 1 mV difference with each other.

In general, all (111) peaks in Figure 8.3 seem like having the same intensities with each other. However, after the XRD patterns are magnified, it is obvious that sample grown at 1675 mV has the highest (111) intensity as depicted in Figure 8.4. Yet, cathodic potentials of 1674 mV and 1676 mV were not being left out and still be considered as the deposition voltages that could produce high quality ZnTe layers. This is because relatively the XRD intensities of (111) peaks from both samples are also high.

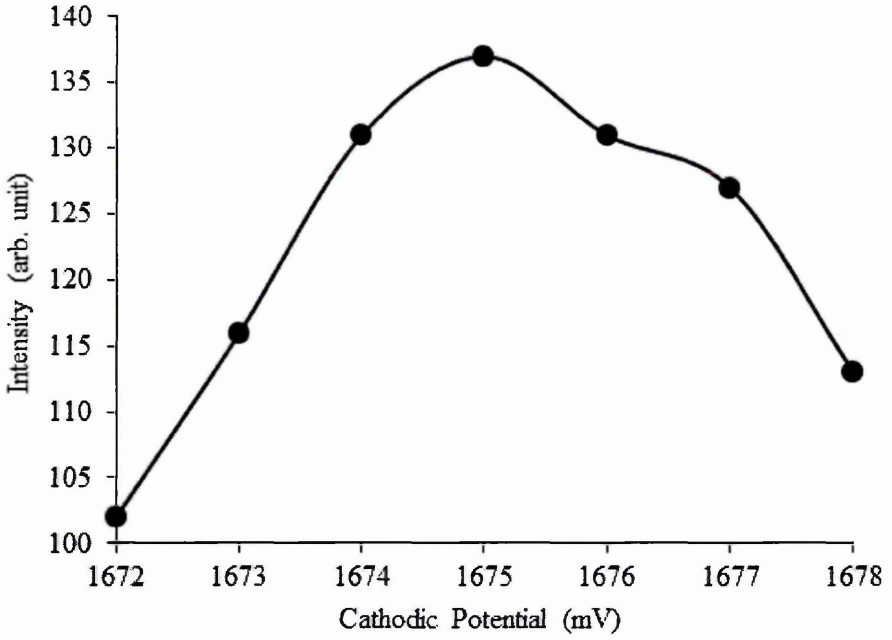

Figure 8.4: The intensities of (111) peak after magnification of the XRD patterns. Sample grown at 1675 mV shows the highest intensity.

The next task was to do comparison for as-deposited and heat-treated layers. Figure 8.5 displayed the XRD patterns for samples grown at 1674 mV, 1675 mV and 1676 mV. In this figure, the ZnTe layer grown at 1675 mV still has the highest (111) peak followed by 1676 mV and 1674 mV. Two additional ZnTe peaks with low intensities were observed in Figure 8.5. These peaks are (220) and (311) which were observed at $2\theta = 42.2^{o}$ and 49.8^{o} respectively. The presence of 3 peaks in every XRD pattern tells that the electrodeposited ZnTe layers are cubic and polycrystalline material with high preferential orientation along (111) plane.

The crystallite sizes on as-deposited ZnTe layers were calculated using Debye-Scherrer equation with (111) peak as the reference. All of the calculated crystallite sizes are tabulated in Table 8.1. ZnTe sample that has been electrodeposited at 1675 mV shows the highest crystallite size of 22 nm. The crystallite sizes for samples deposited at 1674 mV and 1676 mV are 19 nm and 20 nm respectively.

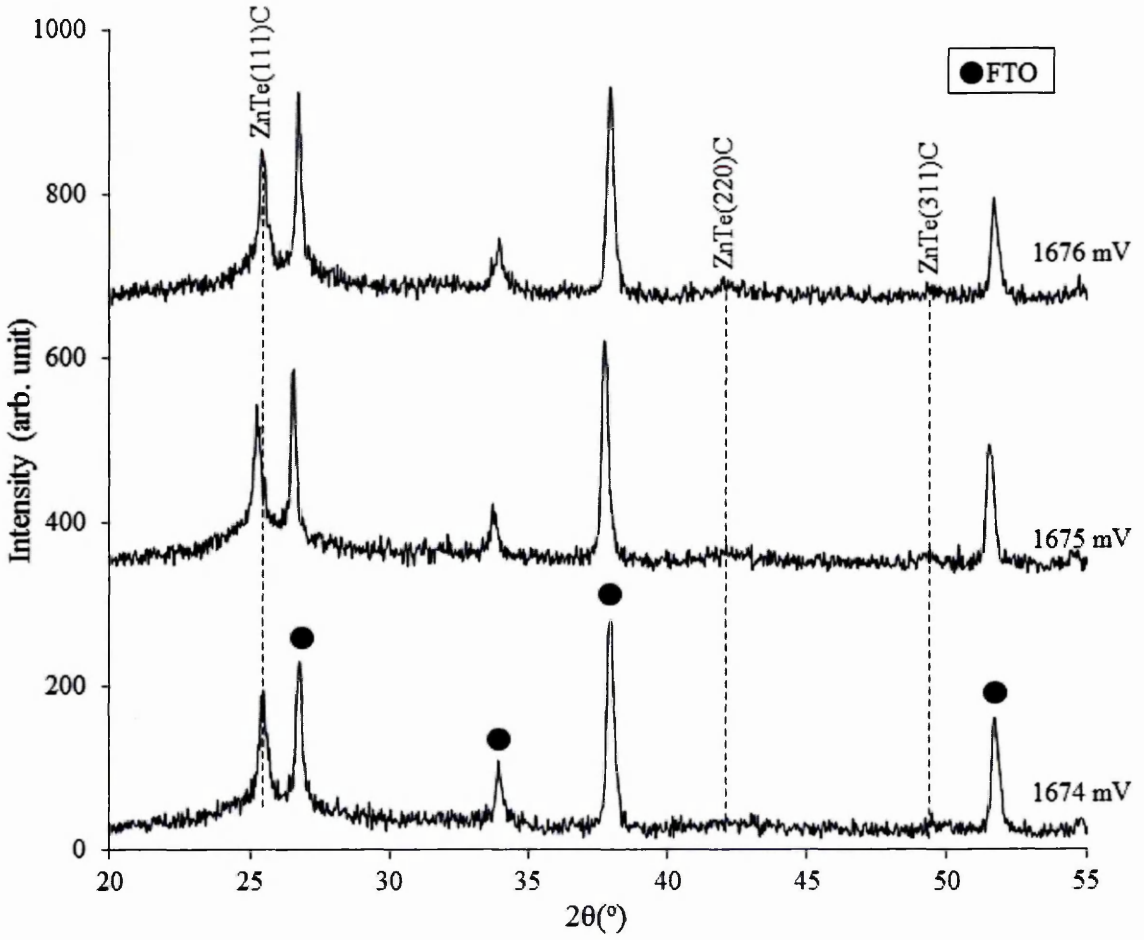

Figure 8.5: The XRD patterns for as-deposited samples grown with different cathodic potentials. Two extra peaks were observed at $2\theta = 42.2^{\circ}$ and 49.8°.

Table 8.1: Crystallite sizes for as-deposited ZnTe samples calculated using (111) peaks as the reference.

Growth voltage (mV)	Growth time (min)	2θ (°)	FWHM (rad)	Crystallite size (nm)
1674	60	25.5	0.008	19
1675	60	25.2	0.007	22
1676	60	25.4	0.008	20

All three samples in Figure 8.5 were heat-treated in air at 300°C for 7 minutes and the results are shown in Figure 8.6. After heat treatment, all (111) peaks gained higher intensity. The (220) and (311) peaks also gained higher intensity but the improvement was not significant. The improvement of the XRD intensities indicates that heat-treatment improves the crystallinity of the as-deposited ZnTe materials.

Similar to as-deposited samples, the crystallite sizes for heat-treated samples were also calculated using Debye-Scherrer equation and shown in Table 8.2. In Table 8.2, we can see that all as-deposited ZnTe layers gained enlargement of the crystallites. Sample that has been grown at 1676 mV gained the largest enlargement from 20 nm to 24 nm. This is the increment of 4 nm after annealing.

Sample that was electrodeposited at 1674 mV had the crystallite sizes increased from 19 nm to 20 nm. The last sample that was deposited at 1675 mV had the increment of 1 nm, from 22 nm to 23 nm. Heat-treatment of electrodeposited ZnTe could also promote the existence of mixed phases in the layers. From Figure 8.16, one can see that the existence of weak peaks at $2\theta = 24.3^{o}$ from the samples deposited at 1675 mV and 1676 mV. These peaks could emerge due to the reaction of precipitated tellurium with oxygen since the annealing was carried out in the air. Fauzi *et al* have identified that this peak might correspond to Te (100), TeO_2 (111) or $ZnTeO_2$ (200) [13].

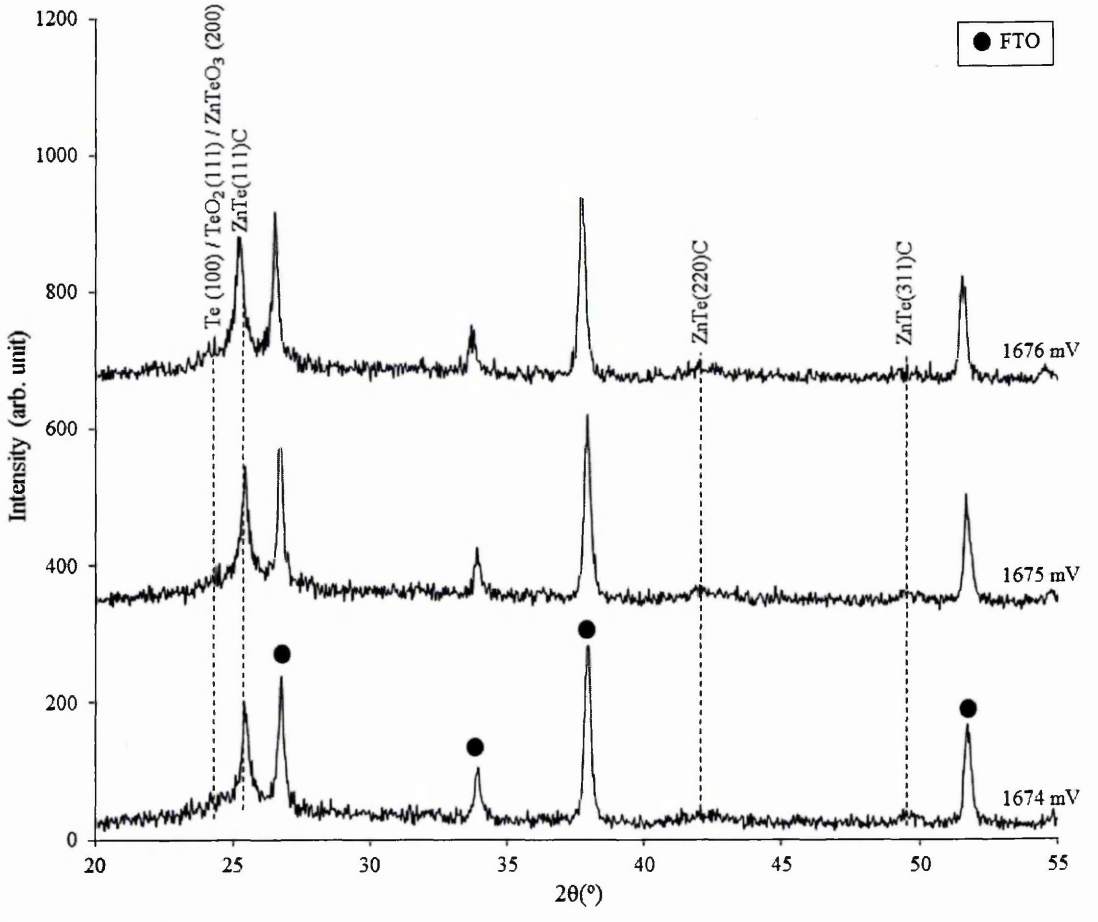

Figure 8.6: The XRD patterns for heat-treated samples grown with different cathodic potentials. Peaks associated with ZnTe gained higher intensity after annealing. Annealing could also leads to the existence of mixed phases as can be seen at $2\theta = 24.3^{o}$.

The efficient way to avoid the existence of mixed phases is to conduct the annealing process in argon or vacuum environment as reported by several research groups [9, 15-17]. It is important to note that the annealing at higher temperature for example, T = 350°C was also being tried. But at this temperature the intensity of (111) peak was found to be decreasing due to the loss of materials. Annealing after $ZnCl_2$ treatment was also being tried with the hope that better crystallinity could be achieved after heat-treatment. Unfortunately, all layers that have been $ZnCl_2$ treated sublimed after heat-treatment. So, for solar cells fabrication only normal heat-treatment will be utilized. For convenience, the increment of ZnTe (111) peak intensities before and after heat-treatment was depicted in Figure 8.7.

Table 8.2: Crystallite sizes for heat-treated ZnTe samples calculated using the (111) peak as the reference.

Growth voltage (mV)	Growth time (min)	2θ (°)	FWHM (rad)	Crystallite size (nm)
1674	60	25.4	0.007	21
1675	60	25.4	0.006	23
1676	60	25.1	0.006	24

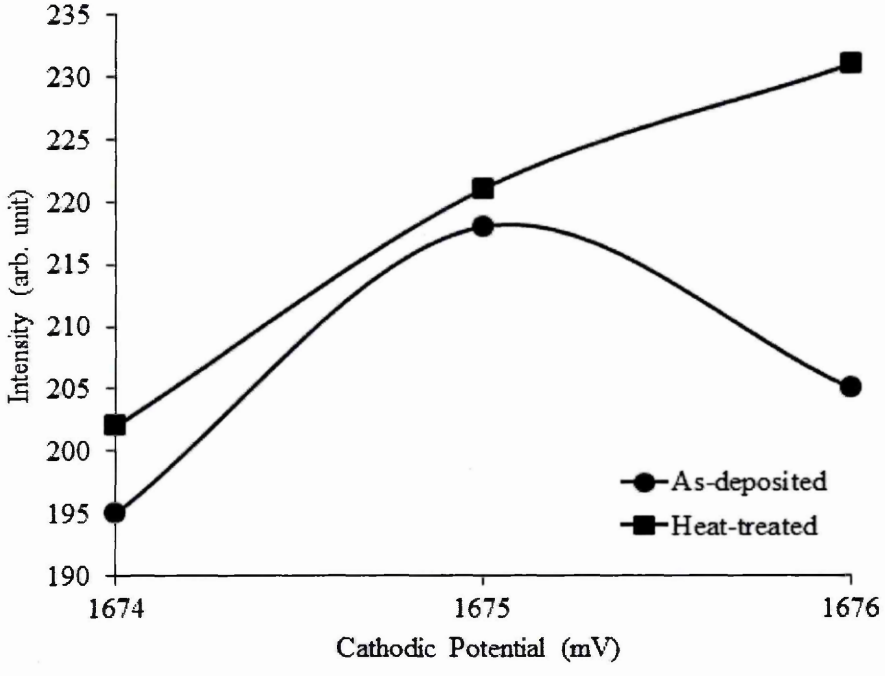

Figure 8.7: The comparison of XRD intensities of (111) peak for as-deposited and heat-treated ZnTe layers.

8.3.3 Optical absorption spectroscopy

After the XRD characterisations, all of the samples shown in Figure 8.7 were subjected to optical absorption spectroscopy studies. For comparison, the optical absorption curves for as-deposited and heat-treated ZnTe layers are shown together in Figure 8.8. The bandgap of the as-deposited samples was estimated to be 2.05 eV and after heat treatment, the bandgap decreased to 2.00 eV. It is important to note that the colour of ZnTe layers changed from brick-red to dark-red after annealing, thus making the absorbance of light stronger in the higher wavelengths' region. Scientific report by Mahalingam *et al* in 2002 stated that the bandgap of annealed layers increased after heat-treatment [7]. However, Kashyout *et al* reported that the bandgap could be higher or lower than 2.00 eV depending on the annealing temperature [15]. Results in Figure 8.8 confirmed that the changing of deposition voltage had small effects on the bandgap values of the electrodeposited ZnTe layers. This is because by changing the cathodic potential, the bandgap of the as-deposited layers doesn't change substantially.

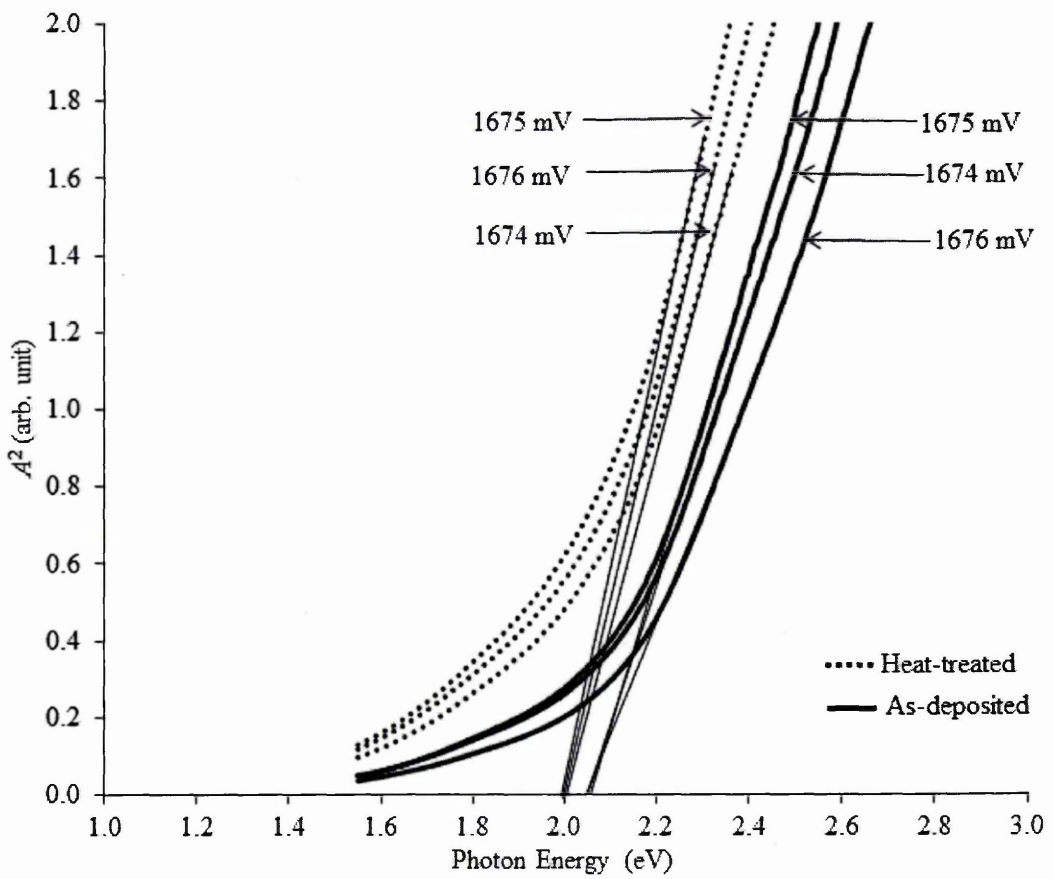

Figure 8.8: The optical absorption curves for as-deposited and heat-treated ZnTe thin films.

It is important to note that the gradient of the A^2 curves for heat-treated layers are higher than the as-deposited samples. This means that the transmittance of light in the heat-treated thin films is weaken by heat –treatment. Figure 8.9 shows the transmittance curves for both cases.

In this figure the wavelengths of 605 nm and 620 nm are marked to relate with the bandgap of the as-deposited and heat-treated samples (2.05 eV and 2.00 eV) respectively. The 'knee' area was identified to be close to 530 nm. This figure shows that for both cases, the transmittance of light is fewer than 10% for photons with wavelength less than 530 nm. Beyond 530 nm, the transmittance of light increases linearly up to 800 nm.

Light transmittance for the as-deposited samples is better compared to the annealed samples. After the 'knee' area, in the visible region, the transmittance of light for as-deposited ZnTe thin films is in between 15% to 50%. On the other hand, for the annealed films, the percentage of light transmittance is in the range of 8% to 32%.

In the infra-red region, the highest transmittance of the annealed layers is near 50%. Meanwhile, for the as-deposited layers the responses are better because the transmittance has reached up to 70% at 800 nm wavelength.

If the comparisons of light transmittance are made between CdS and ZnTe, it is clear that CdS should be the material of choice for window layer. The main reason because the transmittance of CdS is better compared to ZnTe especially in the visible and infra-red regions. If compared between annealed thin films, the transmittance of light in CdS can go up to 90% in the visible region in contrast to ZnTe which could only achieve 50% transmittance. The transmittance of CdS can be improved because it can be chemically treated with $CdCl_2$. However, for ZnTe, chemical treatment was not successful because the layers did not survive the heat-treatment.

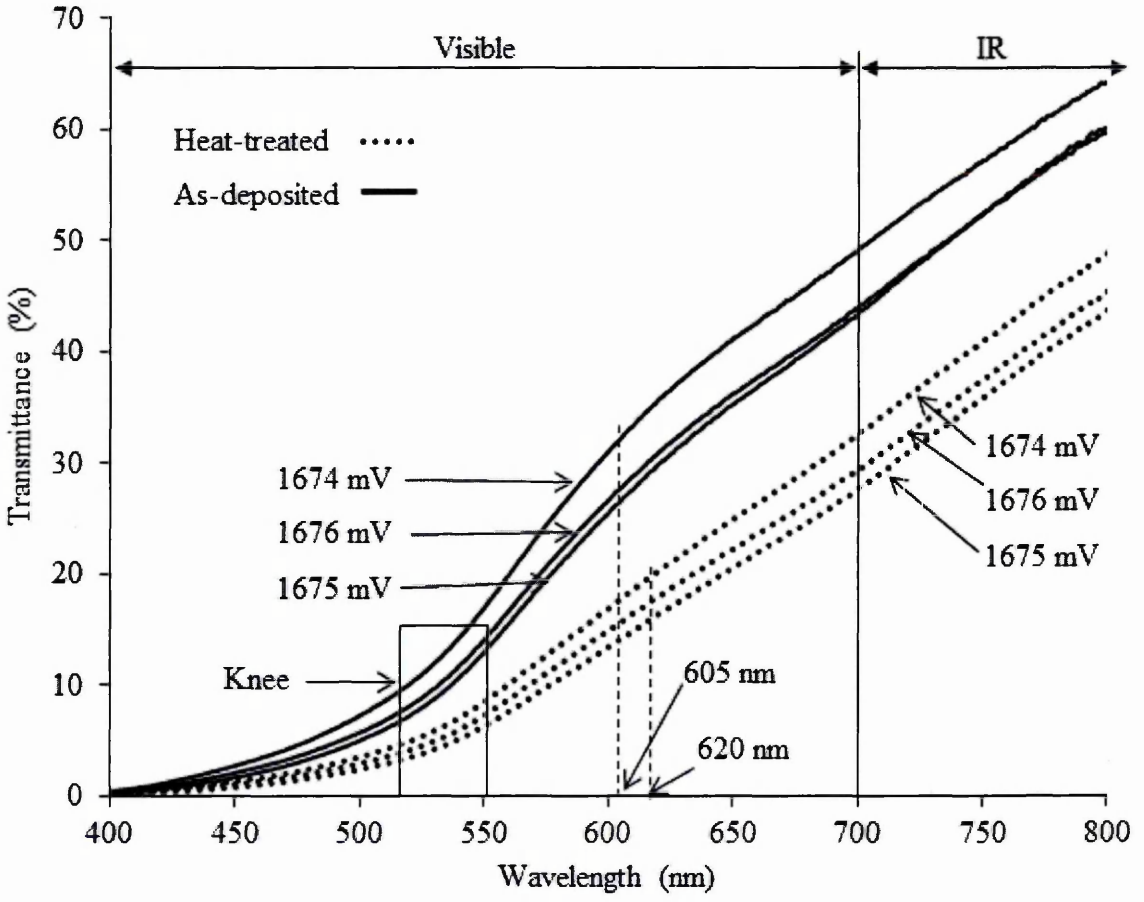

Figure 8.9: Transmittance curves of as-deposited and heat-treated ZnTe samples.

8.3.4 Scanning Electron Microscopy (SEM)

The SEM images with 100 000x magnification for as-deposited and heat-treated layers are shown in Figure 8.10. From these figures, one can see that the 'build-up' of ZnTe thin films was initiated by fine crystallites. When these crystallites grew larger in numbers, they will coalesce and then form cauliflower-like features as can be seen in the as-deposited layers. After heat-treatment in air at 300°C for 7 minutes, these coalescences adhere to each other leading to the formation of agglomerates. These agglomerates can be seen in Figure 8.10 (b) and is circled for easy visualization.

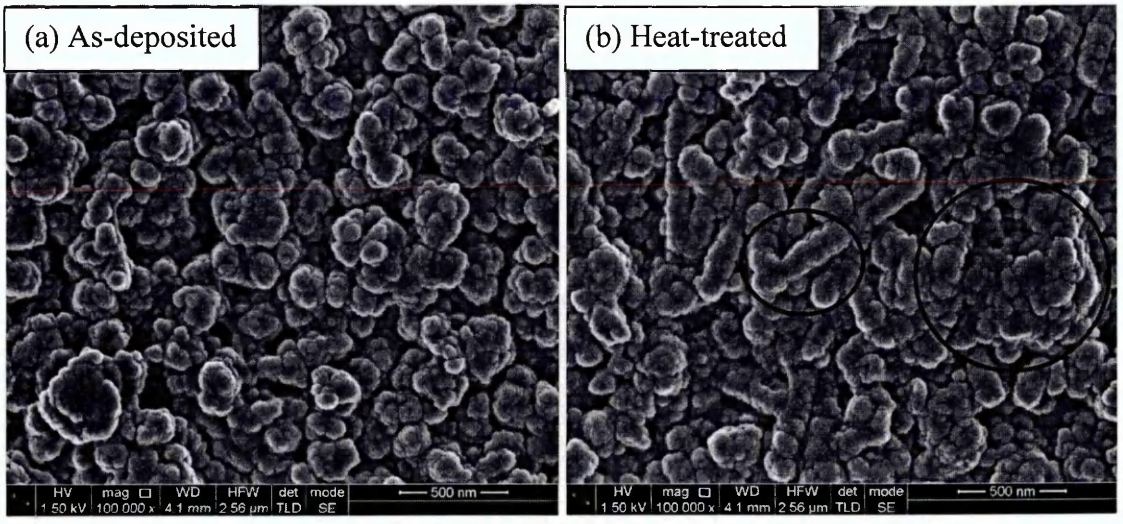

Figure 8.10: SEM images with 100 000x magnification for as-deposited and heat-treated ZnTe layers. Circles are drawn to show agglomerations. (Courtesy: Leon Bowen, Durham University).

Both images in Figure 8.10 were magnified to 250 000x and the results are shown in Figure 8.11. Obtaining high magnification images are useful in determining the crystallite sizes. The crystallite sizes estimated from both figure produce almost similar results to each other. The size of the crystallite for both cases was estimated to be between 16 nm to 21 nm.

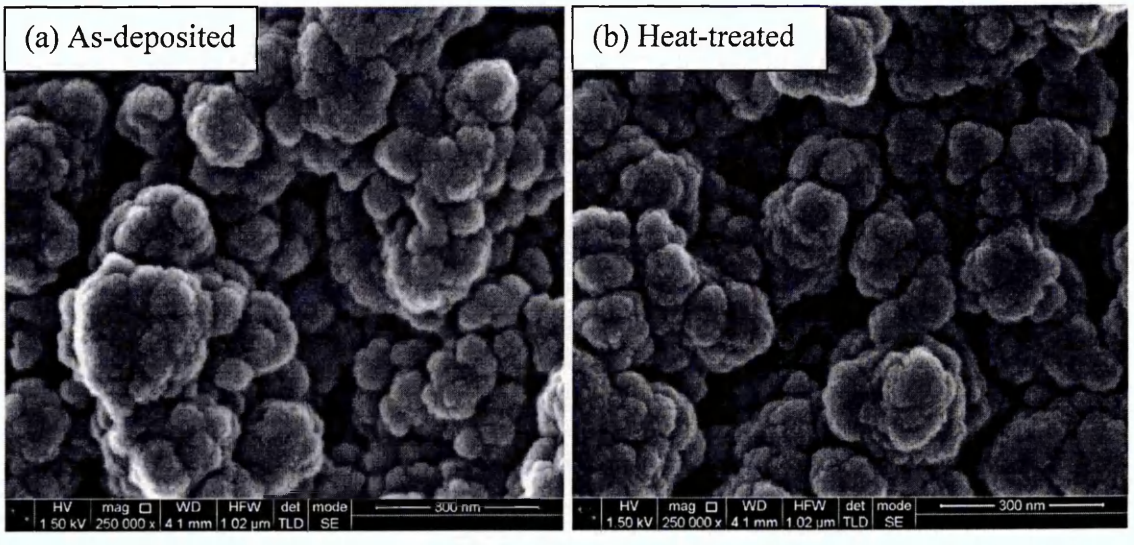

Figure 8.11: SEM images with 250 000x magnification for as-deposited and heat-treated ZnTe layers. (Courtesy: Leon Bowen, Durham University).

Figure 8.12 shows the cross section of electrodeposited ZnTe thin film with magnification of 120 000x. This film was electrodeposited for 1 hour. The average current density recorded during the growth was 139 μAcm^{-2}. The thickness of the layer is 263 nm when calculated using Faraday's Law from Equation (4.3). From the SEM image, the thickness of this layer was estimated to be close to 250 nm which is very close to the calculated value. ZnTe layer shows in this figure covers the contour of the FTO efficiently and it is a sign that ZnTe is a suitable material that could be used as the pin-hole plugging layer.

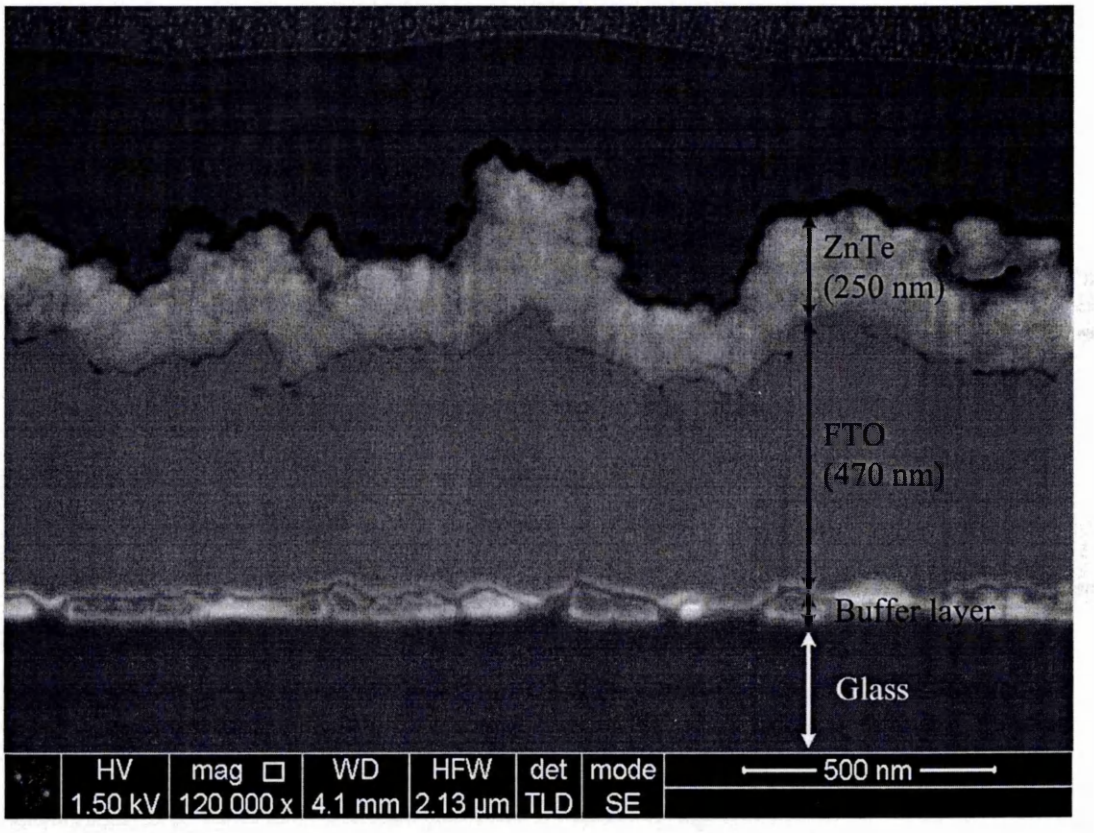

Figure 8.12: SEM cross section image of as-deposited ZnTe samples grown at cathodic potential of 1675 mV for 60 minutes with 120 000x magnification. The thickness of the ZnTe layer is estimated close to 250 nm. (Courtesy: Leon Bowen, Durham University).

8.3.5 X-ray fluorescence (XRF)

The X-ray fluorescence (XRF) experiment was performed to study the atomic percentage of zinc and tellurium when the cathodic potentials were raised gradually. The XRF result is displayed in Figure 8.13. Trend lines are drawn for the purpose of comparing the atomic percentage for both elements when subjected to the increase of

deposition voltage. One can see that the zinc content in the layers increased from 10% to 50% when the cathodic potential was changed gradually between 1225 mV to 1375 mV. Between 1400 mV to 1850 mV the atomic percentage of zinc hovering around 50% to 60% and then exceeds 60% after the cathodic potential was increased to 1900 mV. Beyond 1900 mV, the colour of electrodeposited ZnTe layers became dark due to deposition of metallic zinc.

The atomic percentage of Te is simply a 'mirror image' of zinc. The high percentage of Te at lower cathodic potentials (1225 mV to 1350 mV) is in good agreement with the XRD results discussed before. In Figure 8.2, at low cathodic potential (1225 mV), ZnTe peak (111) was absent from the XRD patterns due to the very high content of Te in the layers. However, when the cathodic potential was raised gradually, ZnTe peak (111) started to emerge and Te content in the layers was simultaneously reduced. Result from the XRF tells that near stoichiometric ZnTe thin films can be deposited in a very wide deposition window, between 1375 to 1850 mV.

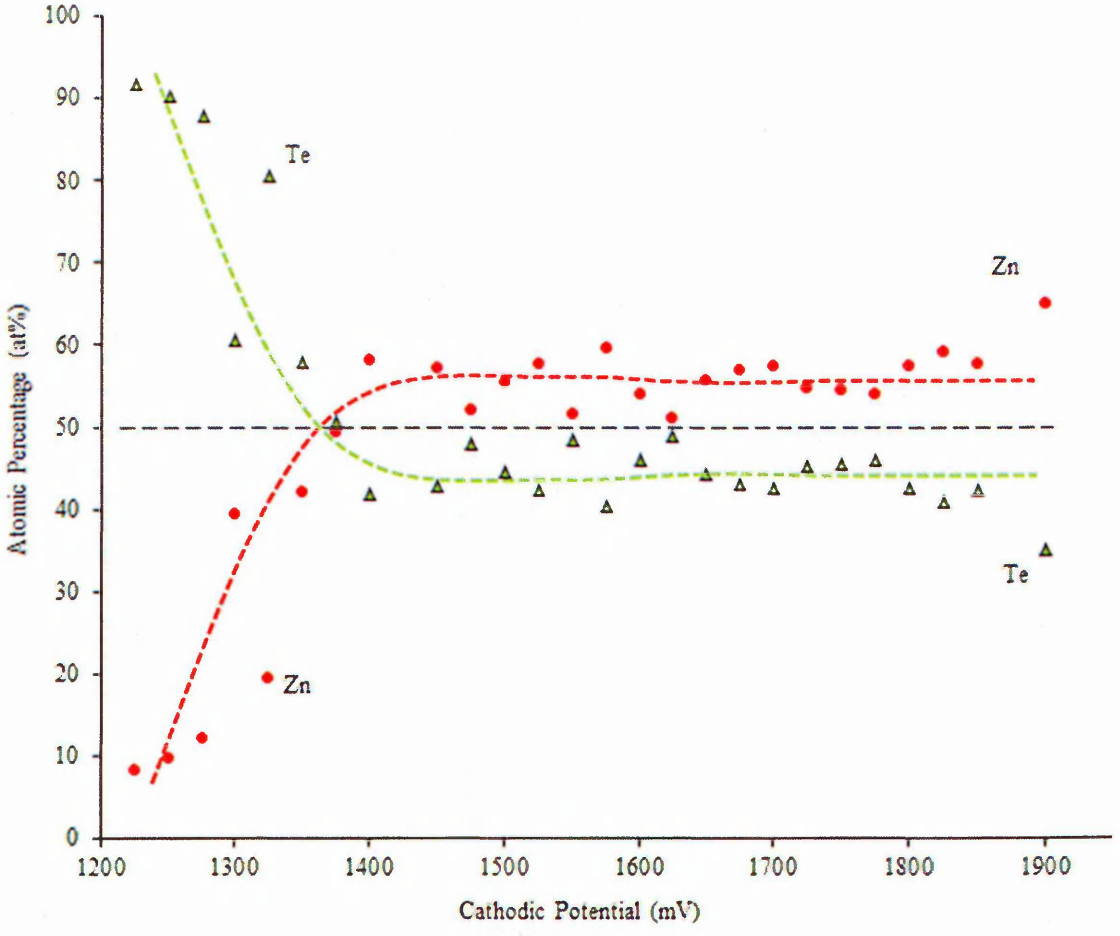

Figure 8.13: The atomic percentage of Zn and Te measured by XRF system for as-deposited ZnTe layers [13]. Trend lines are provided for enhance visibility.

The composition of Zn after heat-treatment is shown in Figure 8.14 and according to this analysis, zinc was found to be more susceptible to high temperature. Before heat-treatment, the composition of zinc fluctuated around 50% to 60% in 1375 mV to 1850 mV deposition window. But when these samples were annealed, zinc content fluctuated around 50% to 55%.

Meanwhile, the compositions of tellurium before and after heat-treatment are shown in Figure 8.15. The composition of tellurium seems to increase after annealing. This was due to the compositional decrease of zinc thus resulting in higher tellurium content compared to as-deposited samples. In the 1375 mV to 1850 mV deposition window, Te content fluctuates around 45% to 50% after heat-treatment which is the improvement from 40% to 50% for as-deposited layers.

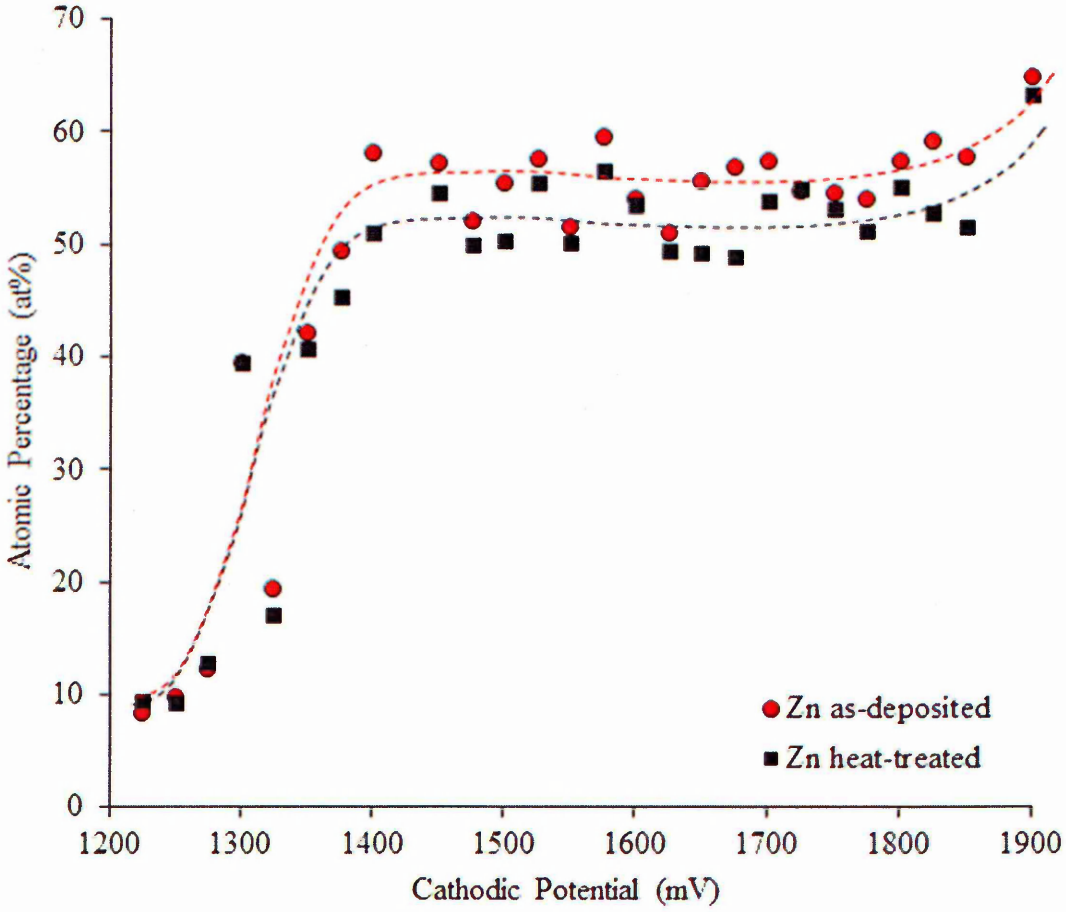

Figure 8.14: The atomic percentage of Zn in ZnTe layers before and after heat-treatment at 300°C for 7 minutes. Trend lines show the decrease of atomic percentage of Zn after the heat-treatment.

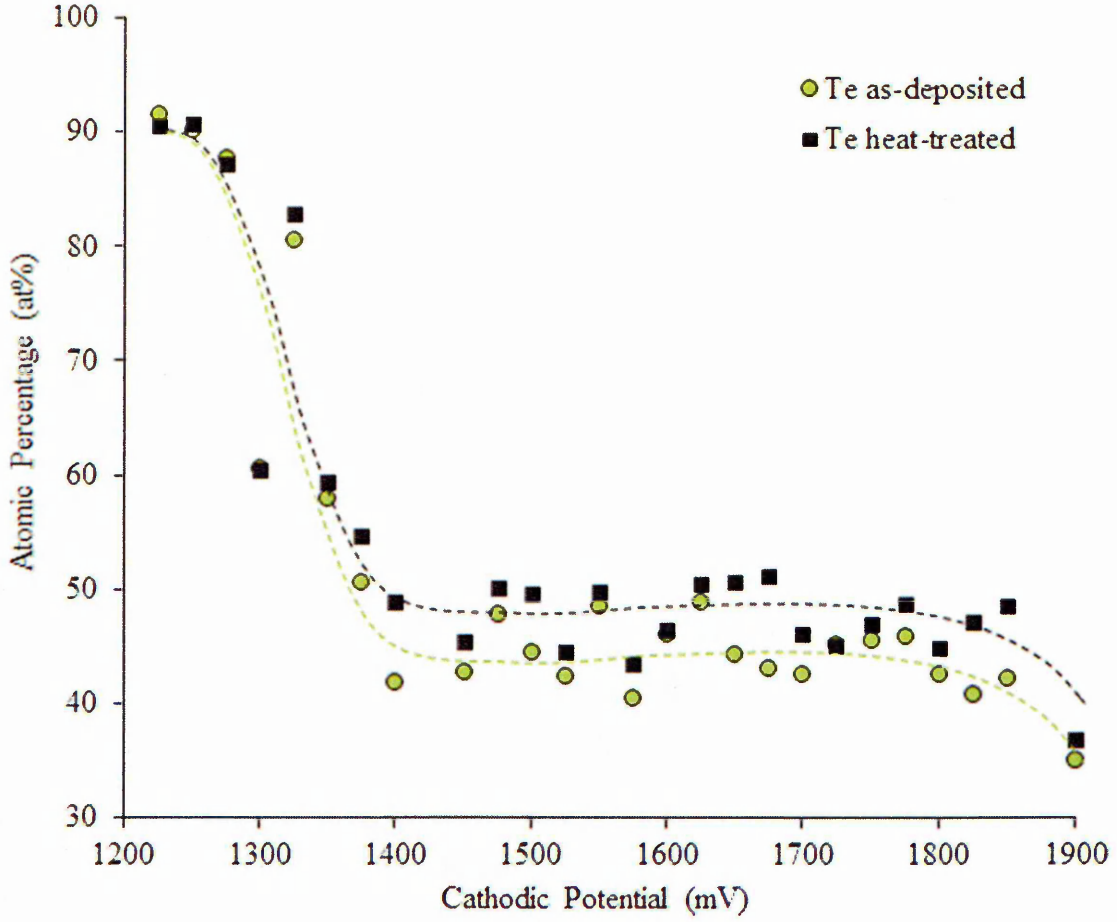

Figure 8.15: The atomic percentage of Te in ZnTe layers before and after heat-treatment at 300°C for 7 minutes. Trend lines show the increase of atomic percentage of Te the after heat-treatment.

8.3.6 Photoelectrochemical (PEC) cell measurements

The electrical conductivity type of ZnTe semiconductors was determined by PEC cell measurements. Figure 8.16 shows the electrical conductivity type of as-deposited ZnTe layers. In this figure one can see that the electrical conductivity type of ZnTe thin films is always p-type even though the majority of the layers are Zn-rich as seen in the XRF. It was expected that the conductivity of ZnTe would change from p-type to n-type if zinc content in the layers was increased. However, the n-type conductivity of ZnTe was not observed even at the cathodic potential as high as 1900 mV.

This observation is similar to CdS where the electrical conductivity remains n-type for a wide range of deposition voltage. It is sensible to postulate that defects might be responsible for keeping the electrical conductivity of these layers to remain p-type.

Samples that were electrodeposited at 1225 mV and 1250 mV showed zero electrical conductivity. This is because at these cathodic potentials, only Te was deposited. Since Te is a semi-metal with bandgap of 0.34 eV [18], there was no band bending at the solid-liquid junction interface. Therefore, PEC measurements showed zero volt reading.

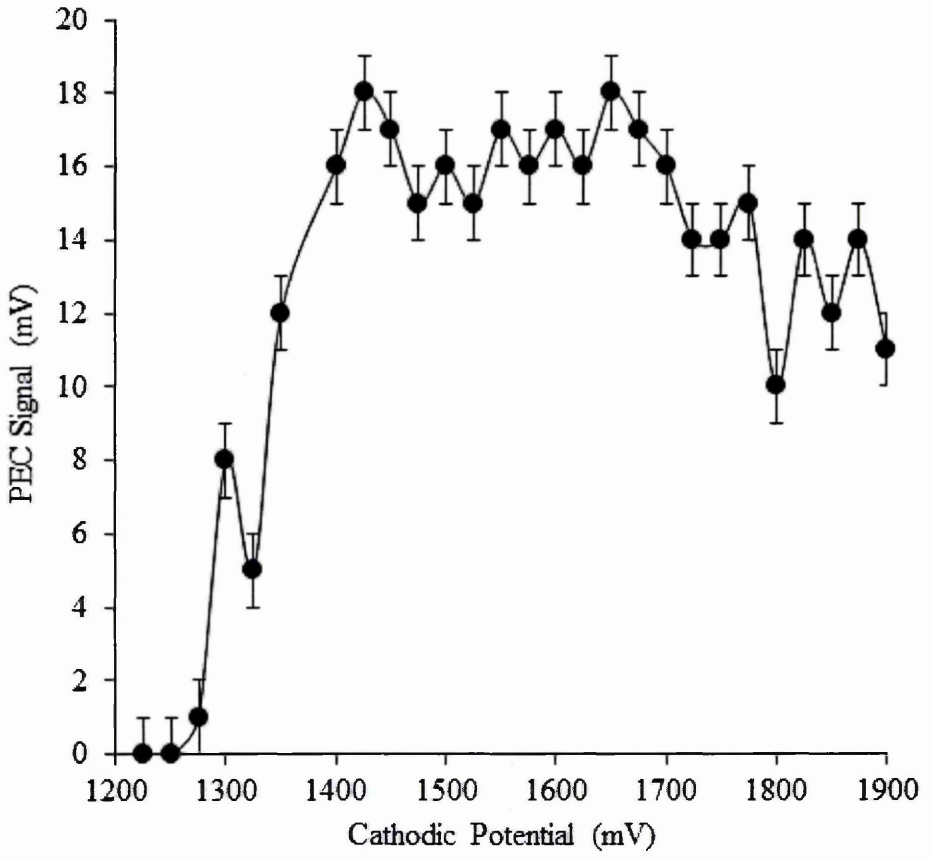

Figure 8.16: PEC signals of as-deposited ZnTe layers showing p-type electrical conductivity across a wide deposition window [13].

To see the effects of annealing upon the electrical conductivity of electrodeposited ZnTe layers, six samples were grown at the vicinity of the optimized cathodic potentials. For device fabrication, only the optimized cathodic potentials will be applied to grow ZnTe semiconductors. Similar to Figure 8.16, the electrical conductivity type of as-deposited layers remained p-type. After heat treatment at 300°C for 7 minutes, the electrical conductivity type of these thin films still remained p-type but with weaker magnitudes as shown in Figure 8.17.

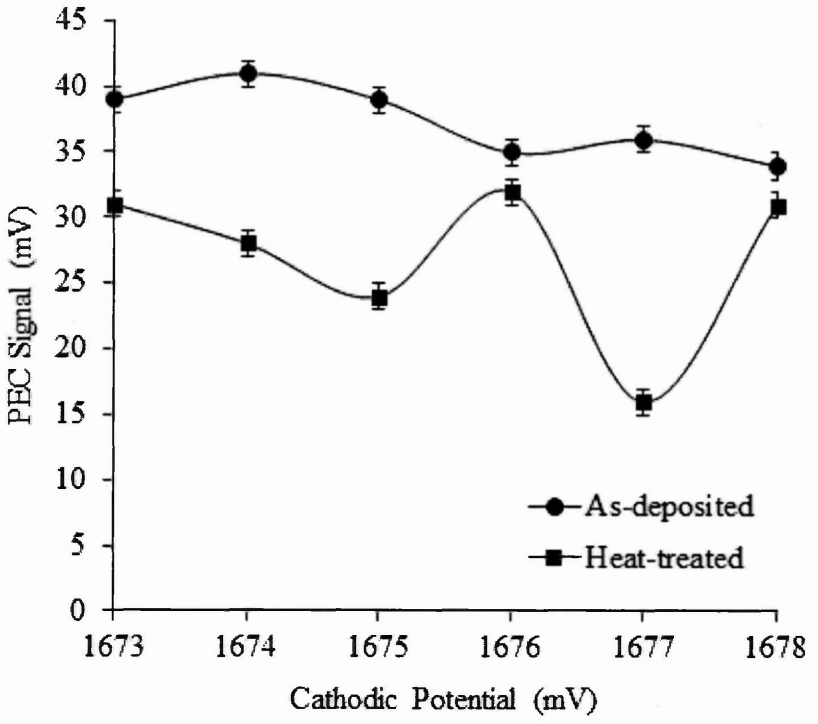

Figure 8.17: PEC signals of as-deposited and heat-treated ZnTe layers. Heat-treated layers still showed p-type conductivity but with weaker PEC signals.

The weaker magnitudes of the annealed films might be due to the variations of doping concentration and the effect of surface states because of the oxidations of Te to form TeO_2 are possible after heat-treatment as discussed in the XRD section.

8.3.7 D.C. electrical onductivity measurements

Since the as-deposited and heat-treated ZnTe thin films were both p-type semiconductors, high work function metals should be deposited to form ohmic contacts. So, for making low-resistive ohmic contacts, circular gold contacts with diameter of 2 mm were sputtered on the as-deposited and heat-treated ZnTe layers using Quorum 150T sputtering system. The thickness of the ZnTe thin films was calculated to be close to 240 nm. The I-V curves of the FTO/ZnTe/Au structure were measured and resistance of the structure was determined from linear I-V curve. The calculated electrical resistivity using Equation (5.8) for as-deposited and annealed ZnTe thin films are displayed in Table 8.3.

Table 8.3: The calculated electrical resistivity of as-deposited and heat-treated ZnTe layers.

	Resistivity (ρ) ($\times 10^4$ Ωcm)				
Sample	1st	2nd	3rd	4th	Average
As-deposited	2.8	2.0	2.3	3.6	2.7
Heat-treated	3.5	4.2	4.1	3.3	3.8

Similar to the previous work, 4 different points were measured on each sample and the averages of these measurements were used as the final value. Rakhshani and Pradeep and Ishizaki *et al* reported that the resistivity of electrodeposited ZnTe was around 10^5 Ωcm [8,19]. The average resistivity reported in this chapter (2.7×10^4 Ωcm) is one order of magnitude less. After heat-treatment, the resistivity value increased to 3.8×10^4 Ωcm. This result could happen due to the oxidation of the layers during annealing, hence prevent the intimate contact between the gold and ZnTe thin films being made. This could also arise due to the change of resultant doping concentration caused by material changes during heat-treatment.

8.4 Conclusion

The experimental work on electrodeposited ZnTe thin films utilizing 2-electrode system has revealed the best deposition voltage range to grow near stoichiometric layers. This deposition window is within 3 mV (1674 mV - 1676 mv) range. All near stoichiometric ZnTe layers showed brick-red colour and adhesion to FTOs is excellent.

Electrodeposition of ZnTe produced polycrystalline cubic structure with preferred orientation along (111) plane. Characterisation work using XRD technique shows that the crystallites of ZnTe semiconductors enlarged after heat-treatment in air at 300°C for 7 minutes. SEM images showed the 'building blocks' for ZnTe semiconductors consist of small crystallites with the size between 16 nm to 20 nm. Crystallite sizes of the as-deposited layers grew in the range of 2 - 4 nm after the heat-treatment. However, there is possibility that the heat-treated layers contain mixed phases of either Te, TeO_2 or $ZnTeO_3$. Due to the presence of these mixed phases, optical absorption spectroscopy of the annealed layers possessed higher absorbance and smaller bandgap compared to the as-deposited layers.

Compositional analysis by XRF technique unveiled that near stoichiometric ZnTe thin films can be grown from 1375 mV to 1850 mV indicating a very wide deposition window. Even though the majority of the layers measured from PEC showed Zn-richness, the electrical conductivity type remained p-type and could not be changed by increasing the Zn content in the layers. The presence of dominating native defects in the as-deposited and heat-treated layers could be the reason for this observation.

Heat-treatment encouraged the sublimation of Zn and led to the Te-richness in these semiconductors. In addition to that, heat-treatment also promotes the reaction of Zn or Te with oxygen thus creating mixed phases in these annealed thin films.

The electrical resistivity of the electrodeposited ZnTe semiconductors is lower than their annealed counterpart due to the presence of oxide layers on the surface. The electrical resistivity remained in the region of 10^4 Ωcm for both layers.

8.5 References

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9.1 Introduction

Early work on electrodeposited CdS/CdTe solar cells can be traced back to 1982 when Fulop *et al* reported promising results with 8.7% conversion efficiency [1]. In 1984, the efficiency of this device improved to 9.4% as reported by Basol [2]. The conversion efficiency of electrodeposited CdS/CdTe solar cells finally overcame the 10% barrier as reported by Woodcock *et al* 1991 with 14.2% [3].

When Britt and Ferekides reported the conversion efficiency of 15.8% in 1993, (with Close Space Sublimated CdTe), the efficiency of this device stagnated for almost a decade [4]. However, in 2002 Dharmadasa *et al* from Sheffield Hallam University (SHU), United Kingdom reported the conversion efficiency near 18.0% from CdTe layer electrodeposited in ethylene glycol at 160°C [5].

All the solar cell efficiencies mentioned above were obtained from CdTe thin films that had been electrodeposited using 3-electrode system. The first report on CdTe solar cell fabricated from layers grown using 2-electrode aqueous solution came in 2014. The report published by Echendu *et al* showed that conversion efficiency of electrodeposited CdTe thin films obtained from 2-electrode system could also overcome the 10% efficiency barrier [6]. In this research paper, the reported efficiency ZnS/CdTe solar cell structure is 12%.

Previous three chapters have discussed about the aqueous electrodeposition of cadmium sulphate (CdS), cadmium telluride (CdTe) and zinc telluride (ZnTe) semiconducting layers utilizing 2-electrode system. After the growth, these layers were characterized using several techniques in order to obtain the suitable deposition windows.

After the optimized deposition parameters were identified, the next task is to fabricate CdS/CdTe solar cells. In addition, the optimization of several parameters such as annealing temperature and period were fulfilled in parallel with device fabrications. This work was carried out in order to improve the efficiency of the solar cells to the highest possible values.

9.2 Fabrication of glass/FTO/CdS/CdTe solar cells

Cadmium sulphide layers were electrodeposited on glass/FTO substrates for about 50 to 60 minutes to produce glass/FTO/CdS structure. The thickness of CdS thin films was estimated ~250 – 400 nm. Next, the cadmium sulphide layers were $CdCl_2$ treated and then annealed in air at 400°C for 20 minutes. When the annealing stopped, CdS layers were taken out from the furnace and then allowed to cool down. When the temperature of the samples dropped to room temperature, the $CdCl_2$ residues left on the surface of CdS thin films were washed with deionized water and then dried under a stream of nitrogen gas for 10 seconds.

After CdS layers have been dried, the deposition of CdTe can be initiated. CdTe layers were electrodeposited for 4 hours. Thickness of CdTe thin films was estimated ~1.5 – 2.0 μm. This led to the production of glass/FTO/CdS/CdTe structure. The cross section of the solar cell was obtained by transmission electron microscopy (TEM) technique and the image is shown in Figure 9.1. From the TEM image the thickness of CdTe is close to the calculated value. The thickness of CdS however was found to be thinner than the calculated value. This is because after the $CdCl_2$ treatment, interdiffusion between CdS and CdTe layers could occur thus leads to thinner CdS layer as seen in Figure 9.1.

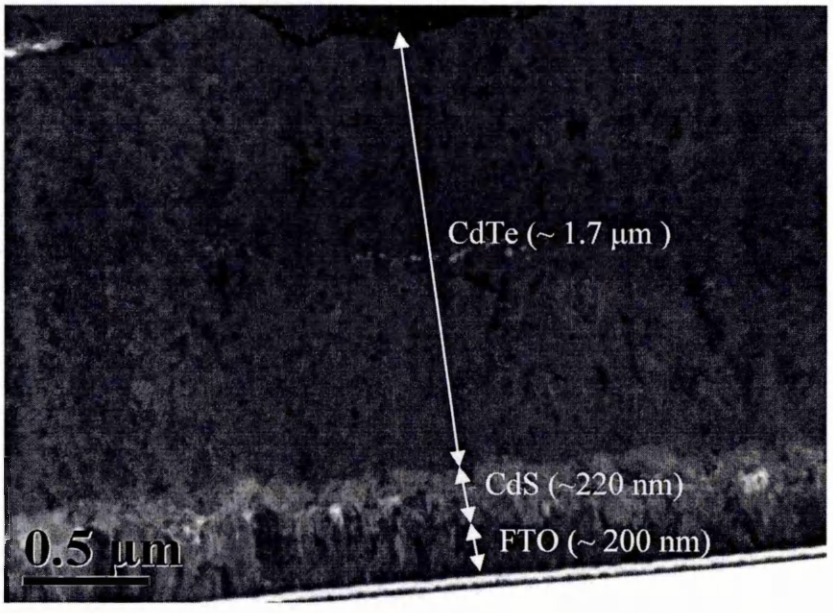


Figure 9.1: The TEM cross section image of glass/FTO/CdS/CdTe solar cell (Courtesy: Ali Abbas, Loughborough University).

Similar to CdS layers, CdTe layers also need to be treated with $CdCl_2$ or $CdCl_2$ + CdF_2. Heat-treatment in air for 450°C for 15 minutes soon followed after the chemical treatment. The chemical residues were washed away with deionized water followed by drying under a stream of nitrogen gas for 10 seconds after the CdTe layers cool down to room temperature. The next task was to perform chemical etching as described by Dharmadasa *et al* [5]. The essence of carrying out chemical etching is to enrich the surface of CdTe semiconductors with cadmium instead of tellurium. Cadmium rich is preferable because it pins the Fermi level of n-type CdTe close to the valence band (at E_4 or E_5) as depicted in Figure 9.2 (a). This leads to the creation of large Schottky barrier when high work function metal is deposited on the CdTe. Having a large Schottky barrier at the back of the device is an advantage because it creates high open circuit voltage, V_{oc}. If CdTe surface is rich in tellurium, Fermi level will be pinned at E_1, E_2 or E_3 [7]. Figure 9.2 (b) shows the dominant Fermi level pinning position for the Te-rich surface.

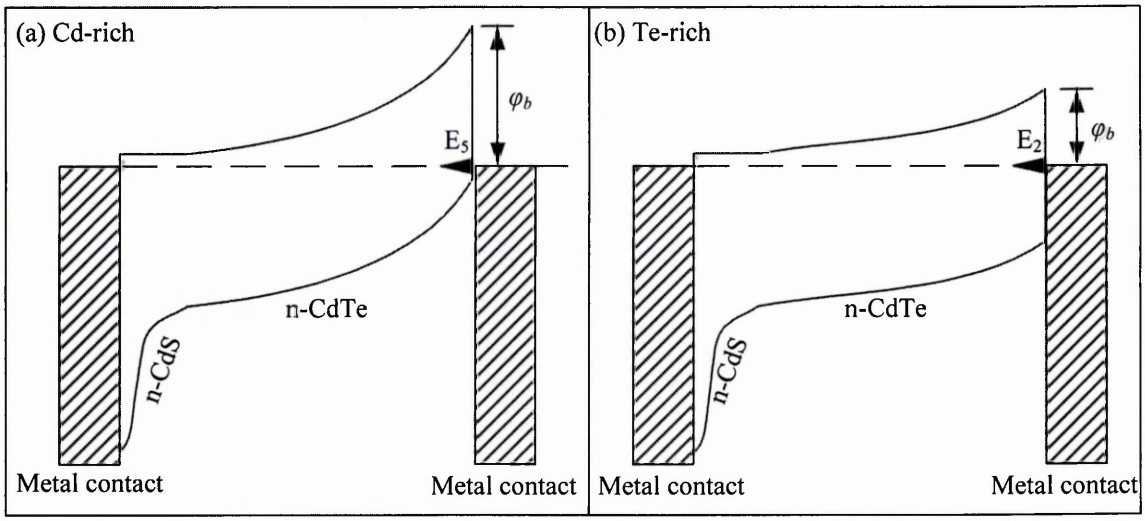


Figure 9.2: The comparison of barrier height, ϕ_b at the n-CdTe/metal interface. (a) In Cd-rich layer, Fermi level preferentially pinned at defect levels close to n-CdTe valence band. (b) In the case of Te-rich layer, the pinning position preferentially at the vicinity of the midgap.

By comparing both cases, it is obvious that the effective band bending only occur if the Fermi level is pinned close to the valence band of n-CdTe. Effective band bending also indicates the presence of strong electric field at metal-semiconductor

junction thus increasing the efficiency of separating the electron-hole pairs to the opposite side of the device.

9.2.1 The etching process of CdTe surface

The etching process started by dissolving 1 gram of potassium dichromate ($K_2Cr_2O_7$) in 20 ml of deionized water. To make it as an acidic etchant, 0.08 ml of concentrated sulphuric acid (H_2SO_4) was added. The basic solution was prepared by dissolving 0.5 g of sodium hydroxide (NaOH) and 0.5 g of sodium thiosulphate ($Na_2S_2O_3$) in a separate beaker containing 50 ml of deionized water. This basic solution was heated to ~60°C using a hot plate. Potassium dichromate and sodium hydroxide were supplied by Sigma-Aldrich, UK while the sodium thiosulphate ($Na_2S_2O_3$) was supplied by Fisher Scientific, UK. The etching process is depicted in Figure 9.3.

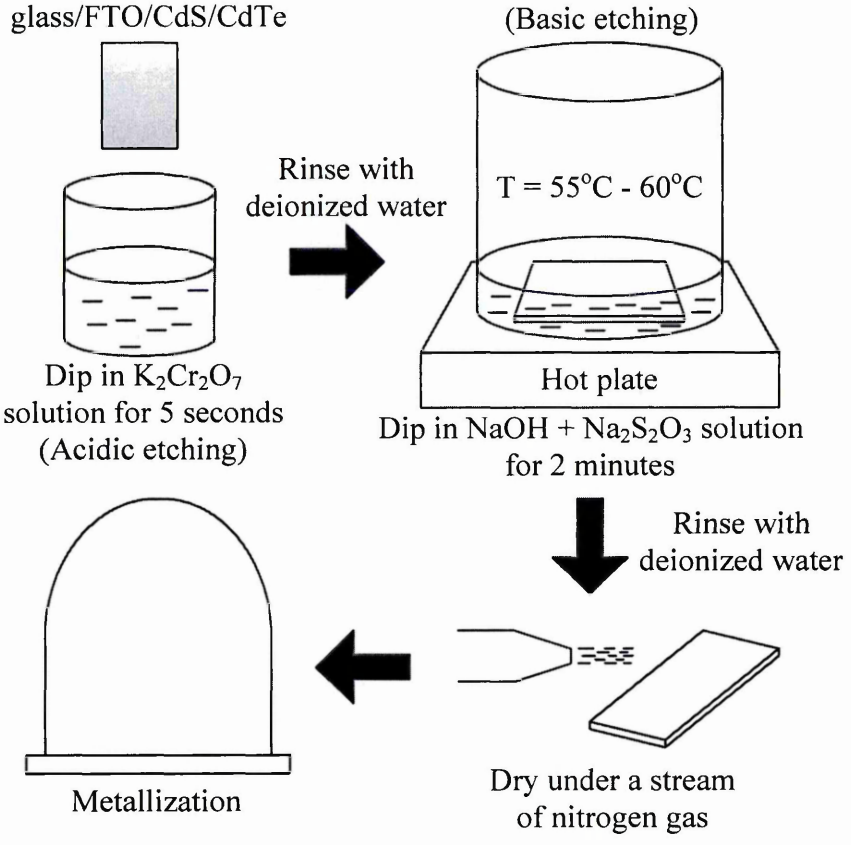


Figure 9.3: The etching process of CdTe surfaces. The first step is to dip the samples into acidic solution followed by immersing in the basic solution. After drying, the samples are transferred quickly to the metallizer.

The etching process begins by dipping the glass/FTO/CdS/CdTe samples into acidic etchant for 5 second. After rinsing with deionized water, the samples are immersed into the basic etchant for 2 minutes. Next, the samples are washed in deionized water and dried under a stream of nitrogen gas for 10 seconds and ready for deposition of metal back contacts. This process is also known as metallization.

9.2.2 Deposition of metal back contacts

Metal back contacts were deposited on CdTe surface using Edwards Auto 306 vacuum metallizer (or evaporator) assisted by FTM7 thickness monitor as shown in Figure 9.4. In this project, several circular shape back contacts with 2 mm diameter were deposited on each sample. These circular back contacts were obtained by placing the samples on a mask with many circles (2 mm diameter) as shown in Figure 9.5. When the samples are ready, they were loaded into the metallizer and the set-up of the metallization process is depicted in Figure 9.6.

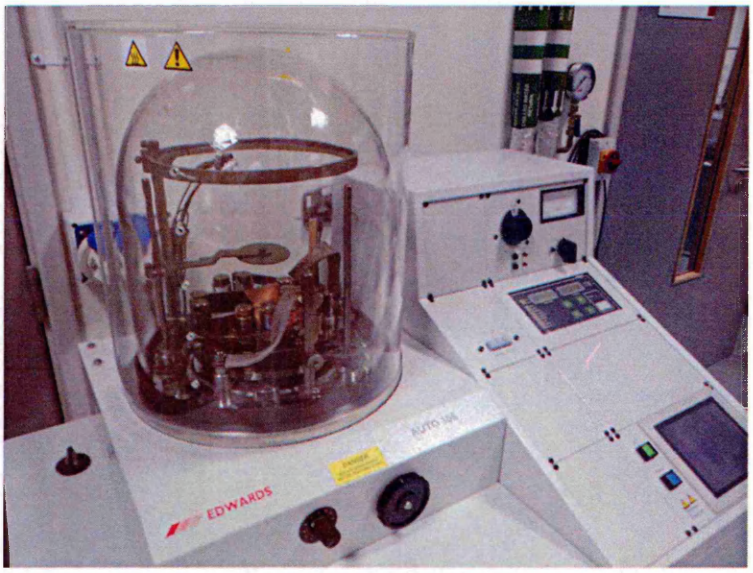


Figure 9.4: Edwards Auto 306 automatic vacuum metallizer used to deposit back metal contacts.

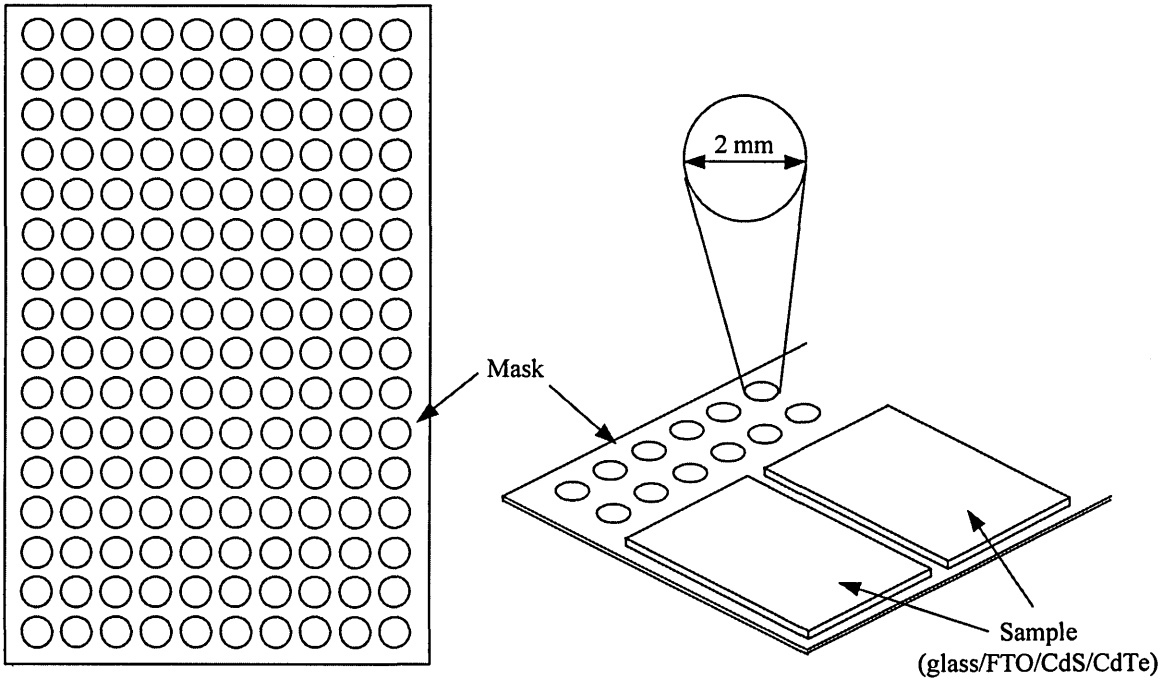


Figure 9.5: The mask used for metallization and the arrangement of glass/FTO/CdS/CdTe samples on the mask.

The deposition was carried out by placing ~4 cm of gold wire (99.999% purity) in the filament. The gold wire was rolled into spiral shape before being put into the tungsten filament. Then, the filament was heated for 1-2 minutes by passing 2 Ampere of direct current. When the filament was heated, gold wire will melt, evaporate and deposit on the CdTe surface. The thickness of the gold back contacts is about 100 nm. The chamber pressure during the metallization was kept at 10^{-6} Torr. Each circular gold contact is a solar cell as shown in Figure 9.7. These solar cells were assessed using fully automated current-voltage (I-V) measurement system.

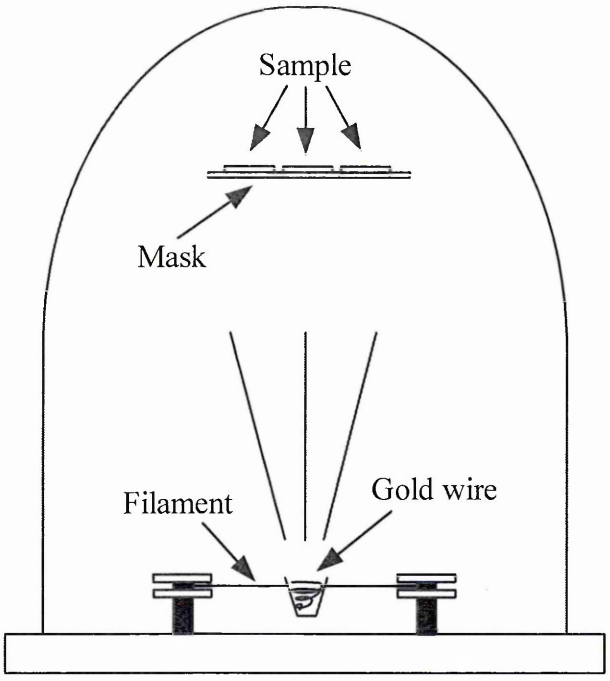


Figure 9.6: The metallization process. Gold will evaporate and then deposit on the CdTe surface when the filament is heated.

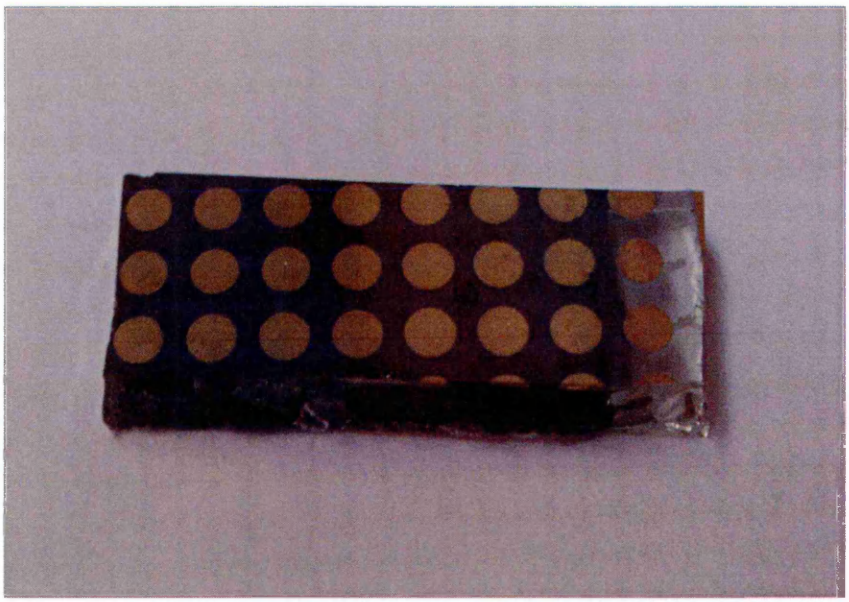


Figure 9.7: Fully fabricated glass/FTO/CdS/CdTe/Au solar cells.

9.3 Assessment of glass/FTO/CdS/CdTe/Au solar cells

The efficiency of the fabricated solar cells was assessed with current-voltage (I-V) measurement using in-house built solar simulator assisted by computerized Keithley 619 electrometer/multimeter shown in Figure 9.8. The intensity of the light from the solar simulator has been calibrated to 100 $mWcm^{-2}$ which corresponds to AM1.5.

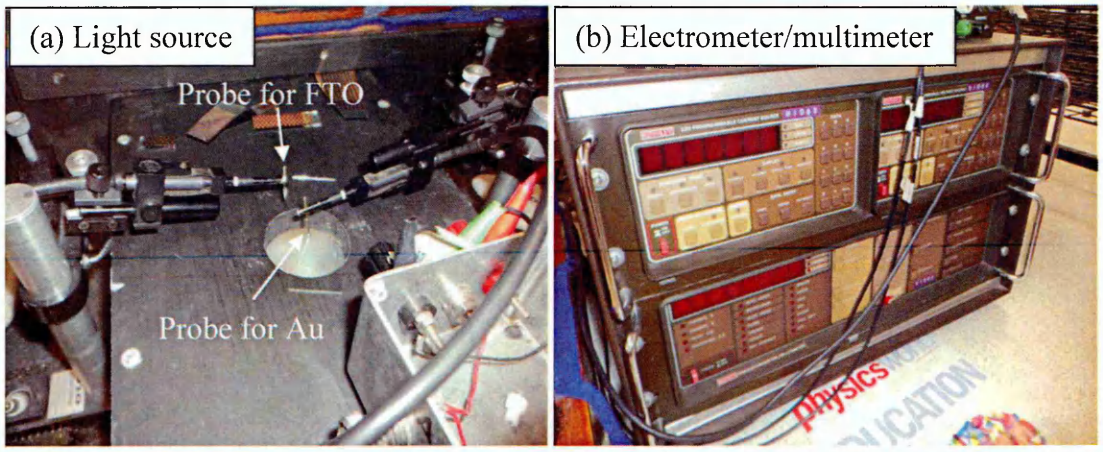


Figure 9.8: The solar in-house built solar simulator comprises of the light source and Keithley 619 electrometer/multimeter.

9.3.1 Solar cells measurement under illuminated condition

Table 9.1 displayed the results of I-V measurement for the initial solar cells. For easy referencing, this sample was given an identification number (ID) FC29. Three diodes were measured and the results are displayed in Table 9.1. From this table, the efficiencies of all devices were in the 1.1% - 1.9% with the highest open circuit voltage (V_{oc}), short circuit current density (J_{sc}) and fill factor (FF) are 480 mV, 15.9 $mAcm^{-2}$ and 0.37 respectively. The J-V curve for the cell with the highest efficiency is shown in Figure 9.9.

Table 9.1: The solar cell parameters measured from the initial sample, FC29.

Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
FC29	280	15.9	0.37	1.6
	480	8.3	0.32	1.3
	440	12.5	0.35	1.9

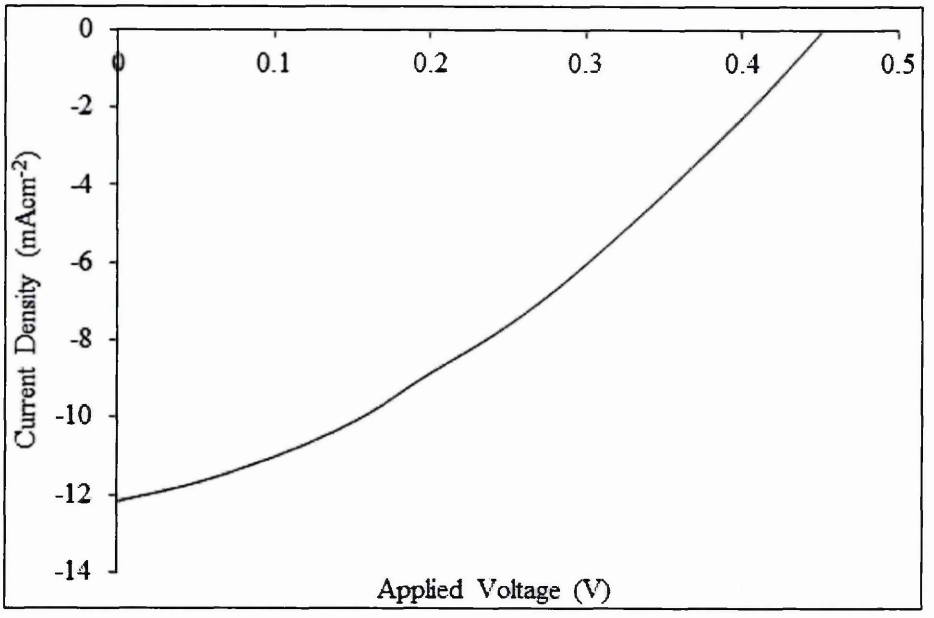


Figure 9.9: The J-V curve for the cell with highest efficiency measured from sample FC29.

The fabrication of CdS/CdTe solar cells continued. As the CdS and CdTe electrolytes were getting fewer impurities due to the self-purification process, the efficiency of the solar cells also increased. Table 9.2 shows the efficiency of fabricated cells (FC44). For these new results, the highest efficiency of CdS/CdTe solar cells has increased to 3.6%. This is the indication that the condition of the baths, especially for CdTe (from $CdSO_4$ precursor) was getting ideal for electrodeposition of high quality materials.

Figure 9.10 shows the J-V curve for the solar cell that obtained the highest efficiency (3.6%). If comparison is made between Figure 9.9 and Figure 9.10, we can see that the V_{oc} and J_{sc} have increased substantially but not the *FF*. The decrease of fill factors is acceptable because the presence of oxides layers on CdTe's surface is different from one sample to the other samples thus varying the contact resistance between CdTe and gold.

Table 9.2: The I-V measurement resulted from three different diodes (FC44).

Sample ID	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
FC44	515	7.0	0.34	1.2
	495	8.0	0.29	1.2
	560	20.0	0.32	3.6

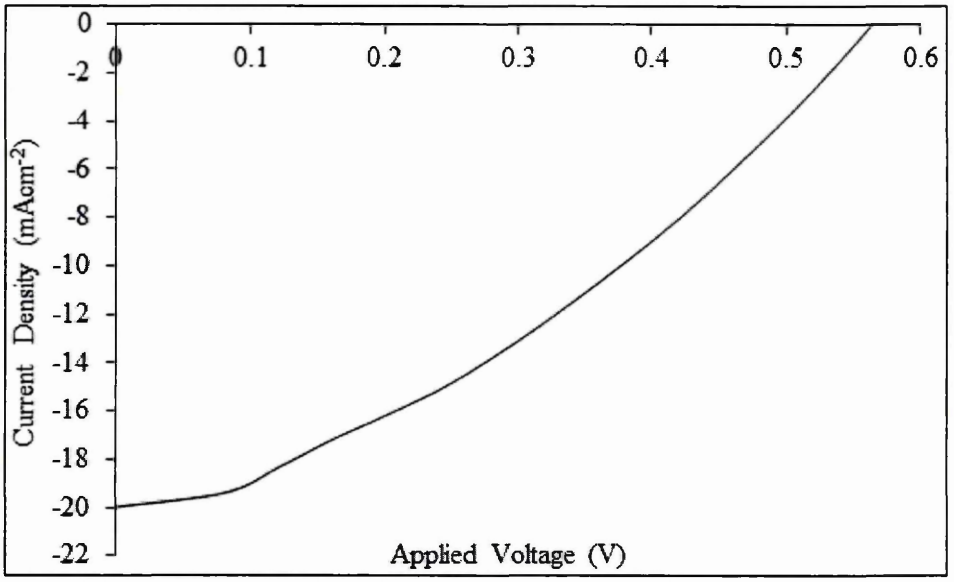


Figure 9.10: The J-V curve for the cell with highest efficiency measured from sample FC44.

It is important to note that results tabulated in Table 9.1 and 9.2 were obtained from devices that have been chemically treated with $CdCl_2$. In the next task, the chemical treatment was slightly modified by mixing the saturated $CdCl_2$ solution with 0.2 g of CdF_2. In the next experiment, 4 samples were prepared. Four samples were prepared because by doing so, the results produced could provide clear and conclusive guidance to move forward in this research project.

Table 9.3 displayed results from four samples prepared in one batch. Every sample was divided into two pieces. One half of the sample was $CdCl_2$ treated while the other half was chemically treated with $CdCl_2$ + CdF_2. After heat-treatment in air at 450°C for 15 minutes, the chemical etching process was soon followed similarly as described in section 9.2.1. Gold back contacts were evaporated on all samples as the final step before I-V measurement was carried out.

All samples in Table 9.3 clearly show that the efficiencies of $CdCl_2$ + CdF_2 samples are higher than $CdCl_2$ treated counterparts. In general, the three main parameters, (V_{oc}, J_{sc} and FF) are higher for $CdCl_2$ + CdF_2 treated solar cells. Highest V_{oc} (700 mV) has been measured from $CdCl_2$ + CdF_2 treated sample (FC71). Similarly, the highest J_{sc} (36.7 $mAcm^{-2}$ - FC72) and FF (0.47 - FC72) were also measured from $CdCl_2$ + CdF_2 treated sample. This experiment has provided clear results showing that the inclusion of fluorine could affect the device positively.

Table 9.3: The comparison of solar cell parameters measured form $CdCl_2$ and $CdCl_2$ + CdF_2 samples. Measurements were carried out from four different samples.

	$CdCl_2$ only				$CdCl_2$ + CdF_2			
Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)
FC69	350	9.6	0.28	0.9	380	11.5	0.26	1.1
	420	10.2	0.31	1.3	650	11.5	0.34	2.5
	420	10.8	0.32	1.5	650	14.0	0.38	3.5
FC71	520	7.6	0.33	1.3	610	16.6	0.45	4.6
	500	8.3	0.32	1.3	700	8.9	0.26	1.7
	490	9.6	0.32	1.5	700	11.5	0.28	2.3
FC72	550	12.7	0.40	2.8	640	16.0	0.47	4.8
	570	19.1	0.28	3.1	600	20.0	0.43	5.2
	615	26.0	0.42	6.7	600	36.7	0.46	10.1
FC79	500	10.2	0.30	1.5	600	9.6	0.38	2.2
	500	12.7	0.30	1.9	610	9.6	0.38	2.2
	510	12.7	0.30	1.9	600	13.5	0.43	3.5

To investigate how the inclusion of fluorine atoms positively affects the efficiency of these devices, characterisation of CdTe layers for both cases were performed using x-ray diffraction (XRD) and scanning electron microscopy (SEM). Figure 9.11 shows the XRD patterns for samples that have been chemically treated with $CdCl_2$ and $CdCl_2$ + CdF_2.

In both figures we can see that both chemical treatments produced similar cubic polycrystalline structure. Both XRD patterns show the presence of mixed phases - Cd_3TeO_6. Sample that has been treated with $CdCl_2$ + CdF_2 showed improved crystallinity along (111) plane because the XRD intensity at $2\theta = 23.8^{\circ}$ in Figure 9.11 (b) is higher than its counterpart. The XRD patterns presented in this section vary from the results presented in Chapter 7 where samples treated with $CdCl_2$ + CdF_2 mixture lost the preffered orientation along (111) plane.

The reason behind this observation is due to the different annealing temperatures used in both cases. In Chapter 7, the annealing temperature of all samples was 400°C while in this chapter the annealing temperature was 450°C. Two different temperature

had to be utilized because CdTe layers grow better on CdS rather than FTO. Because the better quality of CdTe layers on CdS, the anneling temperature can be raised to 450°C.

In the case of CdTe layers grown on FTO, annealing temperature had to be decreased to 400°C. If not, the layers would not survive the heat-treatment due to sublimation.

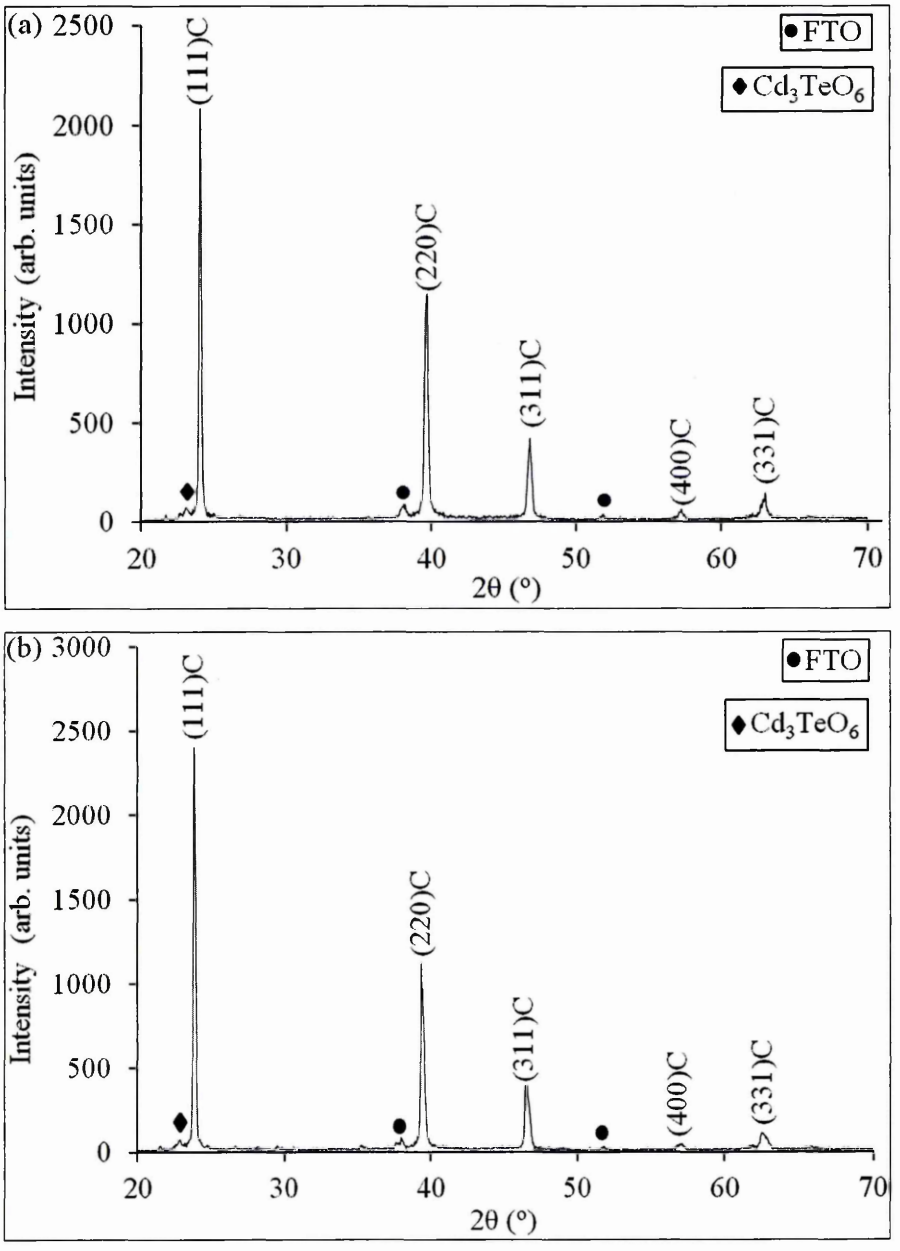


Figure 9.11: The XRD patterns of (a) $CdCl_2$ treated and (b) $CdCl_2$ + CdF_2 samples after heat treatment in air at 450°C for 15 minutes. Both samples show similar polycrystalline cubic structures.

It is important to note that results obtained in this sub-section are in good agreement with the theory published by Dharmadasa *et al* [8]. In this research paper, three stages of CdTe film have been identified. This group have shown that the preferred orientation of CdTe layers when annealed at temperature higher than 430°C is along (111) plane. In addition to that, the majority of highly efficient CdS/CdTe devices (greater than 15%) reported in literature were grown by close space sublimation (CSS) [4, 9-11]. It is noteworthy to mention that CSS is a high temperature growth technique where the source materials are heated to the temperature of 500 - 600°C and always produced larger grains with preffered orientation along (111) plane [12-14].

Figure 9.12 shows the SEM images of as-deposited, $CdCl_2$ and $CdCl_2$ + CdF_2 treated samples. The as-deposited sample in Figure 9.12(a) shows similar morphology as CdTe layers grown on FTO (refer to Figure 7.12(b)). The estimated crystallite sizes for this sample are between 50 nm to 75 nm.

After $CdCl_2$ treatment and annealing in air at 450°C for 15 minutes, the grains coalesce and subsequently produce larger grains as shown in Figure 9.12(b). The grain sizes of this $CdCl_2$ treated sample are estimated to be in the range of 300 nm to 400 nm. The 'wavy' particles in this Figure 9.12(b) are due to the $CdCl_2$ residue left on the surface.

The SEM image in Figure 9.12 (c) shows the last sample that has been chemically treated with $CdCl_2$ + CdF_2. In this SEM image, one can see that the larger grains or clusters created after the inclusion of fluorine. The largest cluster seen from this figure was estimated to be close to 2500 nm. Due to the large grains produced in $CdCl_2$ + CdF_2 treated layer, less grain boundaries are present. This is beneficial in minimizing electrons scattering and recombination in the device and echance the probability of electrons to be collected in the external circuit.

The substantial enlargement of the grain sizes after the inclusion of fluorine atoms had also been reported by Romeo *et al* in 2006 [13]. In this scientific report, this research group had shown that by annealing CdTe layers in Freon gas (HCF_2Cl), the grain sizes could enlarge from 5 μm to 10 μm.

Since chemical treatment using $CdCl_2$ + CdF_2 has produced large grains and also better performing devices, from this point, all samples would be chemically treated the same way.

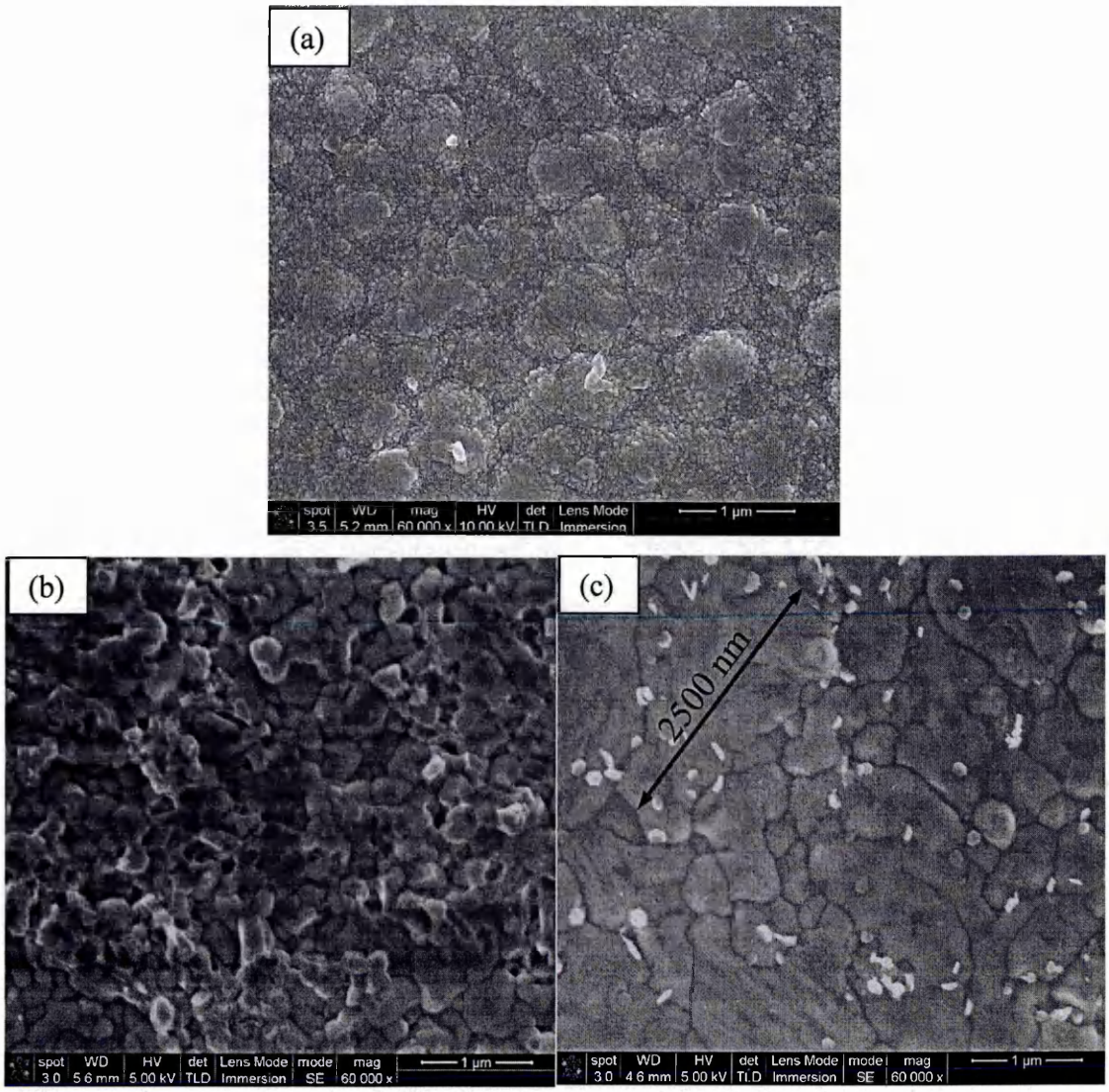


Figure 9.12: The SEM images of (a) as-deposited, (b) $CdCl_2$ treated and (c) $CdCl_2$ + CdF_2 treated. Samples in (b) and (c) were annealed in air at 450°C for 15 minutes.

The J-V curves for solar cells with the highest efficiency from both chemical treatments are shown in Figure 9.13. In this figure, the solar cell with the highest efficiency (6.2%) from $CdCl_2$ treated is compared with the 10% efficiency solar cell treated with $CdCl_2$ + CdF_2.

Up till now, the conversion efficiency of 10.1% has been recorded. In the next step, several new samples were prepared in order to check whether the 10% efficiency could be reproduced or not. Results from a new fabricated batch of samples are provided in Figure 9.14. Figure 9.14 shows the J-V curves from four solar cells which were fabricated after the 10.1% conversion efficiency was observed. The complete solar cell parameters are shown in Table 9.4

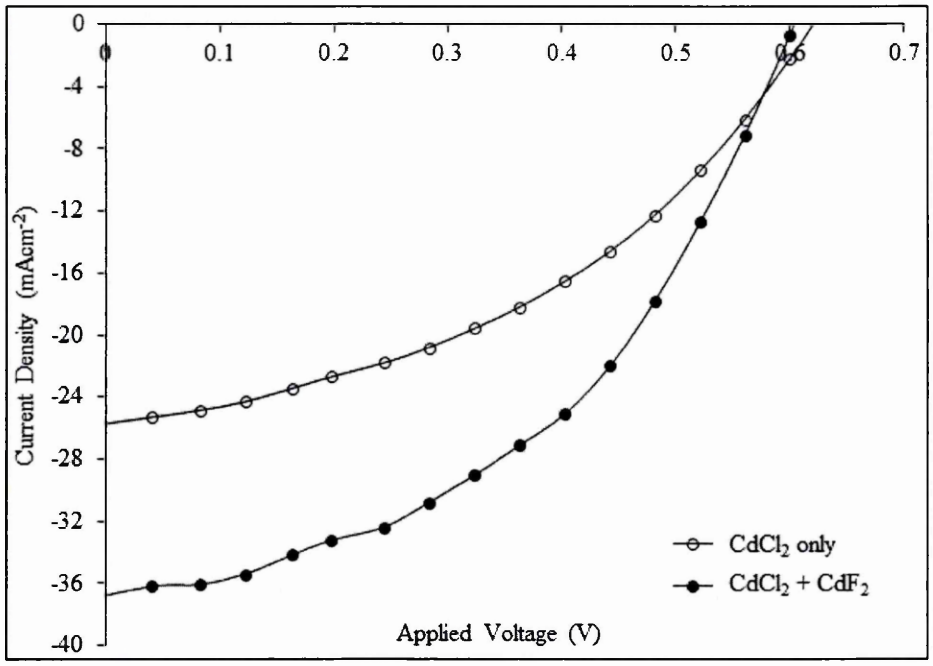


Figure 9.13: The J-V curves of the highest efficiency cells obtained from different chemical treatments.

In this new batch, the growth voltage of CdS (V_g - CdS) was varied from one sample to the other. The reason for the change was to check whether the variation of V_g - CdS had an impact on the efficiency of solar cells. CdS layers that was grown at 1450 mV (FC98) was repeated due to low average efficiency (less than 5%) and the new sample (FC100) showed improved average efficiency (~6.8%). As shown in Table 9.4, it is obvious that changing the V_g - CdS had negligible effects toward the solar cell parameters. This means cathodic potentials between 1440 mV to 1460 mV are suitable for obtaining satisfactory quality of CdS layers, which later can be used to electrodeposit CdTe layers.

In Table 9.4 the average efficiency of the four samples was calculated (first column from right). If sample FC98 is left out, we can see that the reproducibility of electrodeposited CdS/CdTe solar cells is between 6 to 7%. However, if the fill factor can be doubled, the conversion efficiency from the best cells can surpass the 10% barrier.

The observed V_{oc} of 750 mV (FC98) has surpassed the device with 700 mV produced within Solar Energy Lab, SHU reported in 2003 [15]. It is important to note that the CdTe layers reported in this scientific paper was electrodeposited in ethylene glycol at 160°C utilizing 3-electrode system. The highest current density displayed in

Table 9.4 is 39.3 $mAcm^{-2}$. However the highest fill factor measured from these solar cells was only 0.41 which can be considered very low if compared to other electrodeposited CdTe solar cell devices as shown in Table 9.5. Numbers in bold represent the average values.

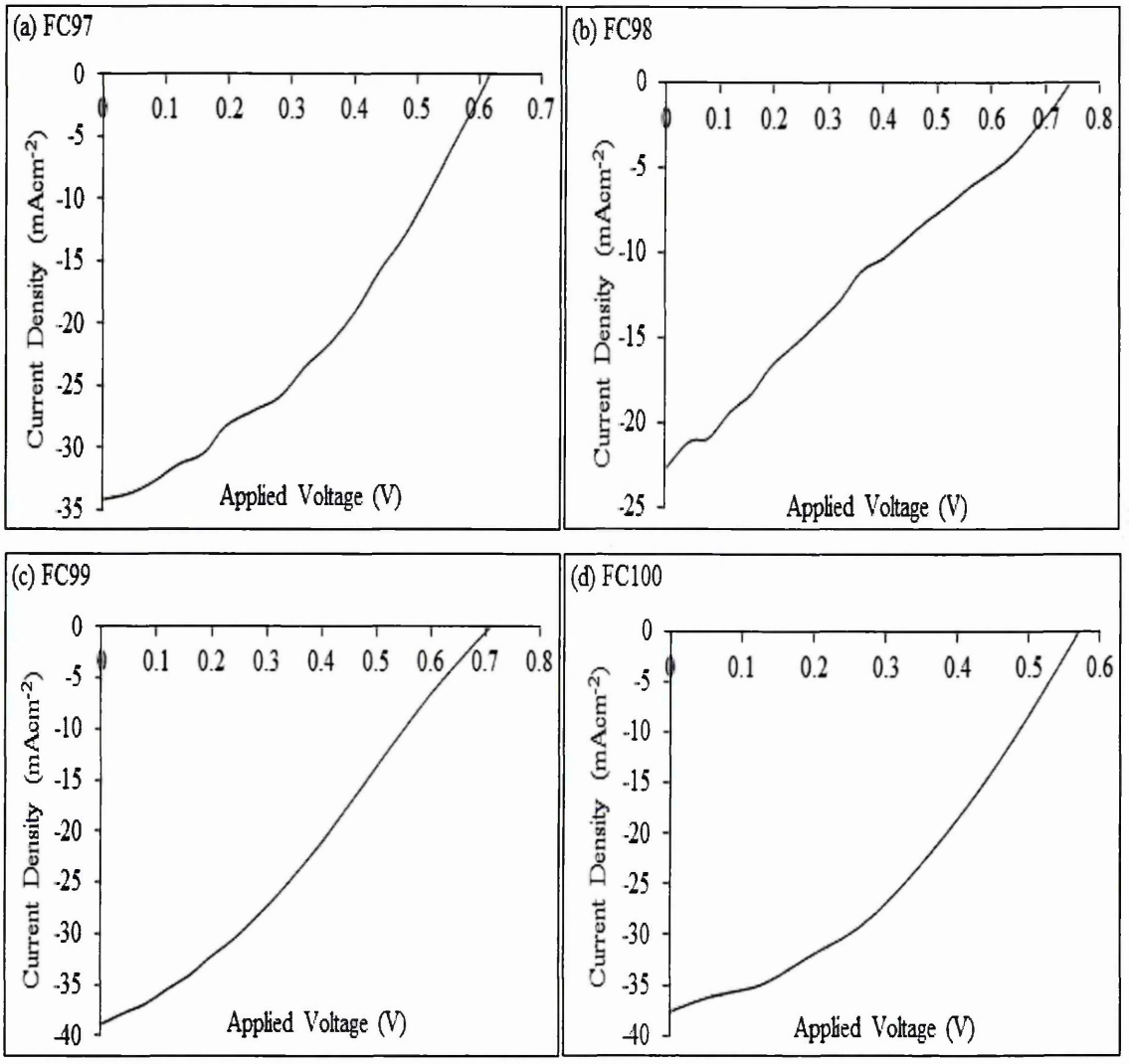


Figure 9.14: The J-V curves of solar cells with the highest conversion efficiency selected from each sample as displayed in Table 9.4 except for FC99. The solar cell selected from FC99 is shown here due to the highest V_{oc} recorded.

Table 9.4: Solar cell parameters corresponding to Figure 9.14. The cathodic potential for electrodeposition of CdS (V_g - CdS) was changed for every sample to observe the effects towards efficiency. All samples were annealed at 450°C for 15 minutes after the $CdCl_2 + CdF_2$ treatment. Numbers in bold represent the average values.

Sample ID	V_g - CdS (mV)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)
FC97	1440	620	28.0	0.27	4.7	**610**	**29.2**	**0.35**	**6.2**
		*610	34.4	0.37	7.8				
		620	27.4	0.35	5.9				
		590	26.8	0.41	6.5				
FC98	1450	*750	22.7	0.25	4.3	**710**	**24.5**	**0.25**	**4.3**
		700	28.0	0.25	4.9				
		680	22.9	0.26	4.0				
FC99	1460	650	26.8	0.27	4.7	**678**	**32.1**	**0.28**	**6.1**
		700	30.6	0.27	5.8				
		650	31.8	0.27	5.6				
		*710	39.3	0.30	8.4				
FC100	1450	500	28.7	0.40	5.7	**525**	**34.4**	**0.38**	**6.9**
		515	31.8	0.39	6.4				
		510	38.2	0.36	7.0				
		*574	38.5	0.37	8.2				

* J-V curve plotted in Figure 9.14

Table 9.5: Parameters of the electrodeposited (from aqueous solution) CdTe solar cell reported in literature.

V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)	Reference
819	23.5	0.74	14.2	[3]
788	24.4	0.70	13.5	[16]
780	23.0	0.72	12.9	[17]
758	21.0	0.65	10.3	[18]
725	21.2	0.67	10.3	[19]

Table 9.5 shows that in general, to attain double digit efficiency, the fill factor of the electrodeposited solar cells should be equal or beyond 0.60. So far, all solar cells shown in Table 9.1 to Table 9.4 could not produce fill factor greater than 0.50. In this research project, the fill factor greater than 0.50 was difficult to achieve because of the high values of series and low values of shunt resistance. The values of series and shunt resistance from the solar cells that have produced conversion efficiency greater than 7% are listed in Table 9.6. From this table, it is clear that the values of series and shunt resistance deviate severely from the ideal values. For an ideal case, the series resistance, $R_s \rightarrow 0$ and the shunt resistance, $R_{sh} \rightarrow \infty$.

As shown in Table 9.6, the lowest series resistance is 151 Ω while the highest R_{sh} shown in the table is 4451 Ω. The R_s of solar cells with double digit efficiency should be less than 200 Ω as reported by Baker *et al* [16]. The cell with ID FC72 has fulfilled this requirement but the R_{sh} still need to be improved in order to attain higher fill factor. The other three samples however show higher series resistance (> 200 Ω) and lower shunt resistance compared to FC72. Factors that contribute to high R_s and low R_{sh} are discussed below.

Table 9.6: The values of series and shunt resistance from solar cells with conversion efficiency greater than 7%.

Sample ID	R_s (Ω)	R_{sh} (Ω)	*FF*	η (%)
FC72	151	4451	0.46	10.1
FC97	254	2568	0.37	7.8
FC99	466	3574	0.30	8.4
FC100	238	2582	0.37	8.2

High series resistance could be resulted from the high resistivity values of CdS layers. As shown in Chapter 6 (section 6.38), the resistivity of electrodeposited CdS treated with $CdCl_2$ is 3.2×10^4 Ωcm. This value is considerably high because according to Basol, typical resistivity of CdS layers is between 5 to 500 Ωcm [19,20]. Annealing in vacuum environment at temperature of 400 - 500°C for 10 - 20 minutes could reduce the resistivity to 10 Ωcm as reported by Uda *et al* [21]. Annealing in H_2 atmosphere containing indium vapour is also effective in reducing the resistivity of CdS layers [22].

FTO used in this research project is also one of the contributing factors of the low fill factor. Scientific report published by Das in 1993 shows that the best front contact for CdS/CdTe solar cells is indium-doped tin oxide (ITO) compared to fluorine-doped tin oxide and indium-doped tin oxide with buffer layer (ITO/SnO_2) [23]. Table 9.7 shows the parameters of CdS/CdTe solar cells reported by Das. These devices were fabricated using three different front contacts.

Table 9.7: Parameters of electrodeposited CdS/CdTe solar cells utilizing different front contact materials [23].

Front contact	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)
FTO	722	20.4	0.55	8.1
ITO/SnO_2	701	22.3	0.57	8.9
ITO	742	23.5	0.66	11.5

In Table 9.7 we can see that the highest conversion efficiency is produced from the cell that utilized the ITO as the front contact. Second best efficiency was recorded from the ITO with buffer layer and the lowest efficiency comes from device with the front contact FTO. Table 9.9 displayed the percentage of improvement of the solar cell parameters. The percentage of improvement was calculated using FTO as the reference. The calculation was carried out to see the degree of improvement towards the solar cell parameters.

Table 9.8: The improvement of solar cell parameters presented in percentage. FTO is made as the reference.

	Improvement (%)			
Front contact	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)
FTO	0	0	0	0
ITO/SnO_2	-2.9	9.3	3.6	9.9
ITO	2.8	15.2	20	42

Obviously from this table, fill factor has benefited the most with 20% improvement after the front contact FTO was replaced with ITO. When ITO was used as the front contact, the value of all three parameters increased. As a result, the conversion efficiency also increased by 42%. It is important to note that typical sheet resistance of ITO is 10 Ω/□ [18,20]. As a comparison, the sheet resistance of FTO-TEC15 is 13 Ω/□ while FTO-TEC7 is 7 Ω/□. For deposition of thin film semiconductors, FTO-TEC15 is preferable because it was designed with less surface roughness and spikes compared to FTO-TEC7. FTO-TEC7 was designed for amorphous silicon solar cells. A very active research group from Parma University, Italy has ruled out the usage of FTO for their CdS/CdTe solar devices because of high resistivity [24]. Cadmium stannate (Cd_2SnO_4) reported in 2001 was claim to be a better front contact than ITO due to the reduced sheet resistance (7-8 Ω/□) [10].

The last factor that could contribute to the low fill factor is the etchant used during the etching process. Potassium dichromate ($K_2Cr_2O_7$) is an acidic etchant normally used to oxidize the CdTe surface. This procedure is well known and has been patented in 1984 [25]. After CdTe surface is etched with $K_2Cr_2O_7$, the next step is to etch the surface with basic etchant, the hydrazine (H_2NNH_2). According to Basol, who invented this procedure, the acidic etching step will produce tellurium rich layers with thickness of 300 to 500 Å [19]. However, basic etching step utilizing hydrazine could not remove the entire tellurium rich layers [19]. So the presence of tellurium rich or oxides of tellurium (TeO_2, $CdTeO_3$, etc) could lead to difficulty of forming intimate contact between CdTe and Au. In addition, the use of sodium hydroxide (NaOH) and sodium thiosulphate ($Na_2S_2O_3$) can also promote the self-compensation effect in CdTe layers. It is well known that element from group I such as Li, Na and K are the p-type dopant for II-VI semiconductors. By etching n-type CdTe in a solution that contains ions from group I elements, it is possible that Na atoms could diffuse into n-CdTe surface layer, dope p-type and pin the Fermi level close to the valence band. This will enable large Schottky barrier at the back contact. However, large amount of p-type dopants could diffuse into the n-CdTe and produce a resistive layer creating negative effects for devices.

The existence of low shunt resistance in the solar cell's circuit could be attributed to the presence of pin-holes in either CdS or CdTe. Electrons that flow through shunt resistors are lost due to the recombination with holes and will not be detected by the ammeter at the external circuit. Figure 9.15 shows the types of pin-holes

that can occur in CdS/CdTe solar cells. For convenience, the characteristics of these pin-holes are described in Table 9.9.

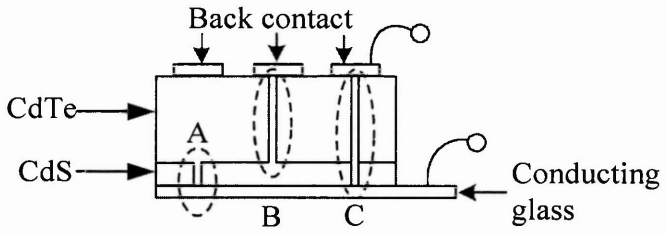


Figure 9.15: Types of pin-holes that can occur in CdS/CdTe solar cells.

Table 9.9: Characteristics of pin-hole that could occur in CdS/CdTe solar cell in reference to Figure 9.15.

Types of pin-hole	Description
A	Shunting of CdTe layers to the conducting glass
B	Shunting of the back contact to CdS layers
C	Shunting of the back contact to conducting glass

Pin-holes could present due to several factors. Pin-hole type A for example, could be present due to the spikes on the surface of FTO. It is important to note that when voltage supply is turned on during electrodeposition, the highest magnitude of electric field is at the tip of the FTO spikes. It is sensible to say that the tip of these spikes might behave as the nucleation center for CdS molecules to grow. As the molecules are stacked against each other, they will grow upwards thus leaving gaps or voids between them. These voids finally act negatively for device performance. The voids' formation is depicted in Figure 9.16 for easy visualization.

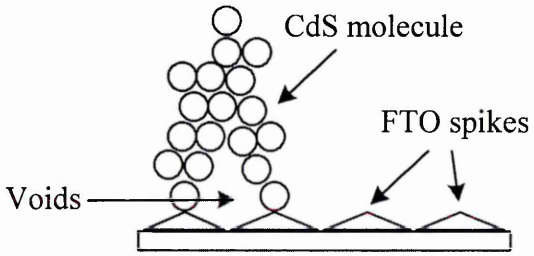


Figure 9.16: The presence of voids in CdS layers initiated by nucleation of molecules at the tip of FTO spikes.

The presence of air bubbles or insulating dust particles on the surface of CdS during the electrodeposition of CdTe is the cause for the existence of type B pin-hole. To minimize the existence of these pin-holes, continuous monitoring of electrodeposition process is needed. When the air bubbles are spotted, the cathode can be knocked with minimum force to make them disappeared.

Type C pin-hole is the most severe between these three problems. It is because, when these types of pin-holes are present, the rectifying behavior of the solar cells will completely lost thus producing only ohmic characteristic due to the metal to metal (FTO to back contact) connection. If type A pin-holes exist in CdS prior to heat-treatment, type C pin-holes could easily occur if the voids burst-up due to the high temperature hence shunting the back contacts straight to the FTO. It is worth mentioning that; heat-treatment could also contribute to the existence of type A and type B pin-holes. Due to the high temperature involved, cracks could occur in either CdS or CdTe layers [26].
To rectify the pin-holes problem, additional layer can be deposited between the CdTe layers and back metal contacts. This method has proven to be successful as reported by Tesssema and Giolando and Abdul-Manaf *et al* [27,28].

9.3.2 Solar cell device characterization using dark I-V measurements.

Current-voltage (I-V) measurements under dark condition were conducted to obtain the ideality factor, n and barrier height, ϕ_b. The ideality factor is determined by taking the highest gradient at the forward bias I-V curve as shown in Figure 9.17. This graph is called log-linear plot. A straight line is drawn after the highest gradient was determined. As a result, this straight line will intersect at the axis of the applied voltage (x-axis) and current (y-axis). The intersection of the straight line with y-axis is actually the reverse saturation current of the diode, I_o. Notice that current is measured in base-ten log scale. The actual value can be obtained by taking the antilog of I_o.

Since the intersected values of current and voltage are obtained, the gradient of the straight line can be determined and subsequently the ideality factor can be calculated using Equation 5.16. The determination of barrier height can be fulfilled with the help from Equation 5.17. Effective Richardson constant, A^* of 12 $Acm^{-2}K^{-2}$ and temperature of 300K are used in the calculations [29]. The rectification factor (RF) is calculated by dividing the forward bias current (point A) with reverse bias current (point B) at a particular voltage. Figure 9.17 can be re-plotted as a linear-linear curve as shown in

Figure 9.18. By having this graph, the threshold voltage, V_T of the diode can be determined. For convenience only cells with efficiency above 7% as tabulated in Table 9.6 are discussed in this section.

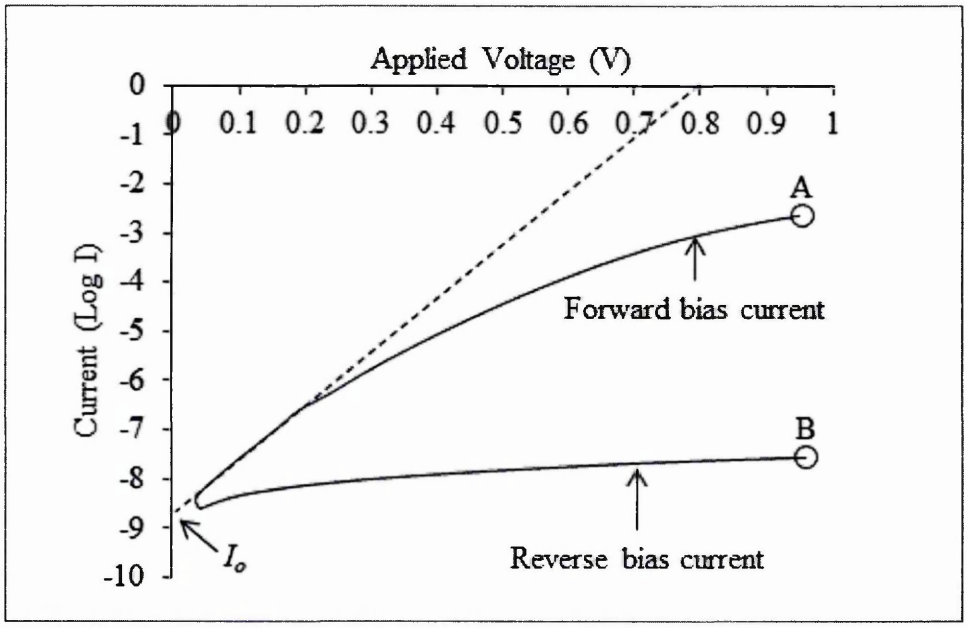


Figure 9.17: An example of I-V curve in the log-linear scale for a diode measured in the dark. A straight line is drawn after the highest gradient at the forward bias current curve has been determined.

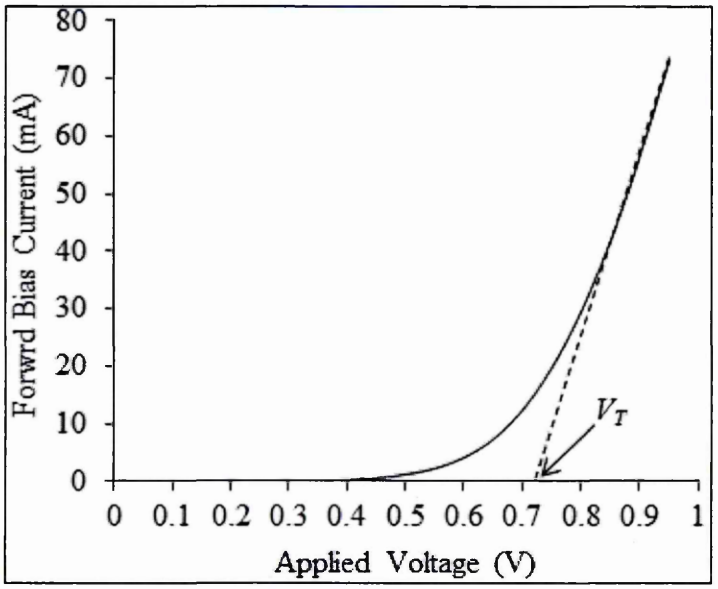
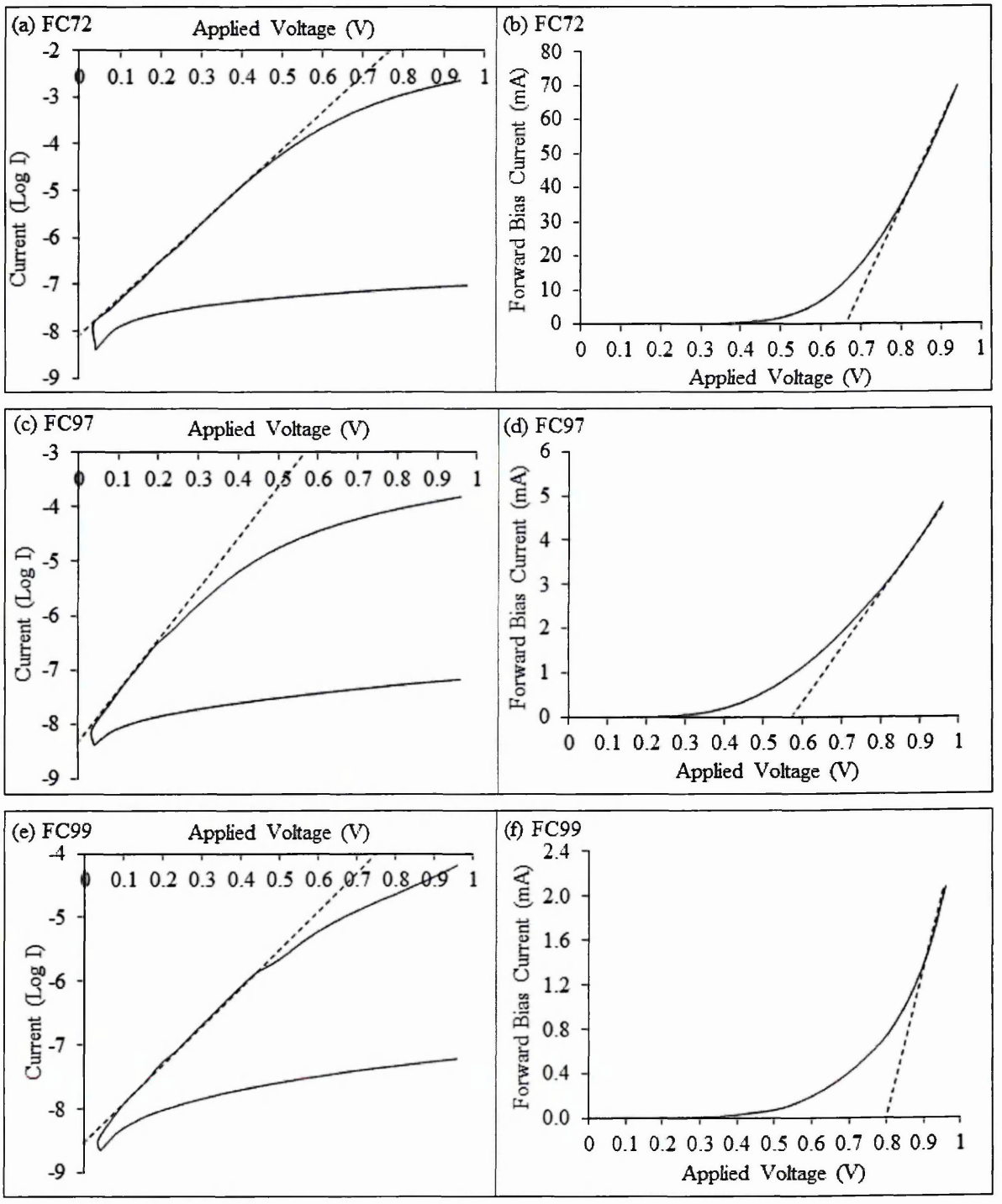


Figure 9.18: Linear-linear plot derived from log-linear graph (Figure 9.15) showing current conduction in the forward bias condition.

Figure 9.19 shows the I-V curves from four different solar cells after measurements are conducted in the dark conditions. Every log-linear curve is accompanied by its linear-linear counterpart. The linear-linear curves are shown to roughly provide the value of the threshold voltage of the solar cells. Threshold voltage should be equal to the open circuit voltage for devices with $FF = 1$ and should be less than the open circuit voltage if $FF < 1$.



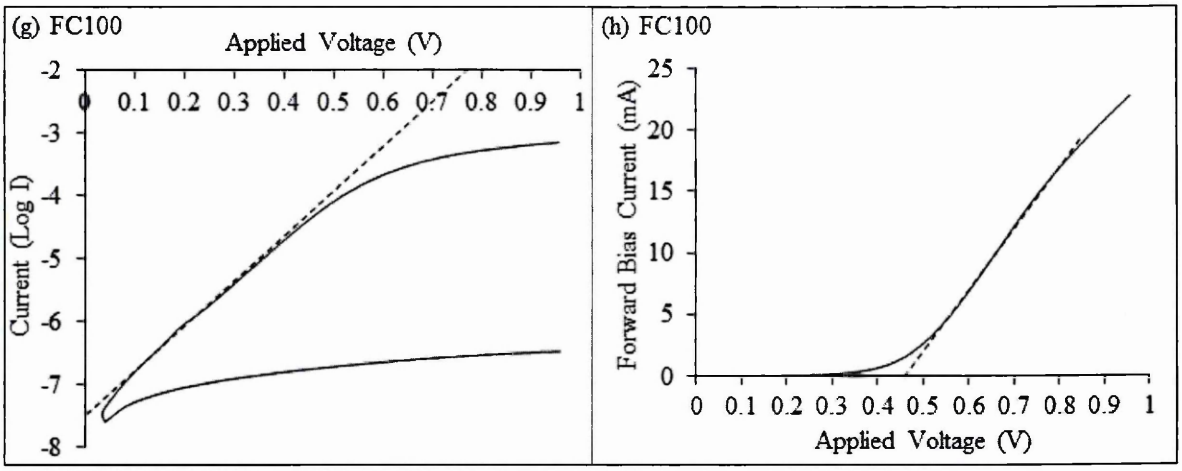


Figure 9.19: The dark I-V curves from devices producing efficiency above 7% presented in log-linear and linear-linear graphs.

For convenience, the threshold voltage, reverse saturation current, ideality factor, barrier height and rectification factor are tabulated in Table 9.10.

Table 9.10: Solar cell parameters obtained after measurement under illumination and dark conditions.

Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	V_T (mV)	I_o ($\times 10^{-9}$ A)	n	ϕ_b (eV)	RF	η (%)
FC72	600	36.7	0.46	680	7.76	1.57	0.75	$10^{4.77}$	10.1
FC97	610	34.4	0.37	585	4.68	1.10	0.78	$10^{3.36}$	7.8
FC99	710	39.3	0.30	800	2.95	1.44	0.78	$10^{3.04}$	8.4
FC100	574	38.5	0.37	460	31.6	1.74	0.72	$10^{3.06}$	8.2

In general, solar cells shown in this table can be considered as a good quality diode because rectification factors are above 10^3 [30]. The highest rectification factor was obtained from FC72 with $10^{4.77}$. Current transport mechanism from semiconductor to metal was dominated by thermionic emission and recombination due to the ideality factor between 1.00 and 2.00. However, the barrier heights are very close to the middle of the bandgap (0.72 eV) indicating the presence of strong Fermi level pinning at this position due to native defects [29]. It shows that the basic etching could not completely remove defects at this location thus leaving the surface in Te-rich condition. This observation is in good agreement with report published by Basol in 1988 [19].

The presence of defects at the metal-semiconductor interface has produced 'confusing' results of threshold voltage observed from FC72 and FC99. In these solar cells, the values of threshold voltage are higher than the open circuit voltage.

9.4 Photoluminescence studies (PL)

Photoluminescene (PL) studies were performed at University of Louisville, USA with the assistance from Professor Thad Druffel and his research group. In this study, PL peaks in the energy range from 0.55 eV to 1.85 eV were measured. Renishaw inVia Raman Microscope with a 632 nm (~1.96 eV) He-Ne laser was employed as the excitation source. A charge-coupled device (CCD) camera and a diffraction grating were utilized as the luminescence detector. CdS/CdTe sample was cooled to 80 K using Linkam THMS600/720 temperature controller stage assisted by liquid nitrogen to maintain the low temperature.

The main purpose of carrying out photoluminescence study is to study the effects of $CdCl_2$ treatment towards the density and distribution of defects in CdTe. So for the experiment, three measurements were fullfilled. The first measurement was conducted on the as-deposited CdS/CdTe layer. The second measurement was conducted on the annealed sample at 400°C for 8 minutes. The last measurement was performed after the second $CdCl_2$ treatment and subsequent annealing at 400°C for 16 minutes.

Figure 9.20 shows the photoluminescence spectra for the three cases. There are four PL peaks (T_1 to T_4) representing the defect levels in the bandgap that can be seen from this figure. The single peak representing the bandgap of CdTe, E_g can be seen at 1.50 eV. The positions of these defect levels (or PL peaks) are listed in Table 9.11.

From Figure 9.20, we can see that the first $CdCl_2$ treatment step reduces the intensity of all defect levels except the one at T_2. After the second $CdCl_2$ treatment, the intensity of all defect levels further reduces indicating the reduction of defect density at these positions. After the second treatment, defect at T_1 completely disappears while the bandgap of CdTe shifted slightly from 1.50 eV to 1.48 eV. The most dense and widely distributed defect is at T_2. Even after the second $CdCl_2$ treatment, the defect distribution at this position remains wide. Results obtained from PL measurement clearly explain why the barrier height of solar cells calculated and displayed in Table 9.10 points to 0.72 - 0.78 eV below the conduction band. This is because the high concentration of

defects located at the midgap, makes the Fermi level always pin at E_3 (or T_2). It should be noted that by pinning the Fermi level at T_3 or T_4 makes higher Schottky barrier leading to improving the band bemding or internal electric field of devices.

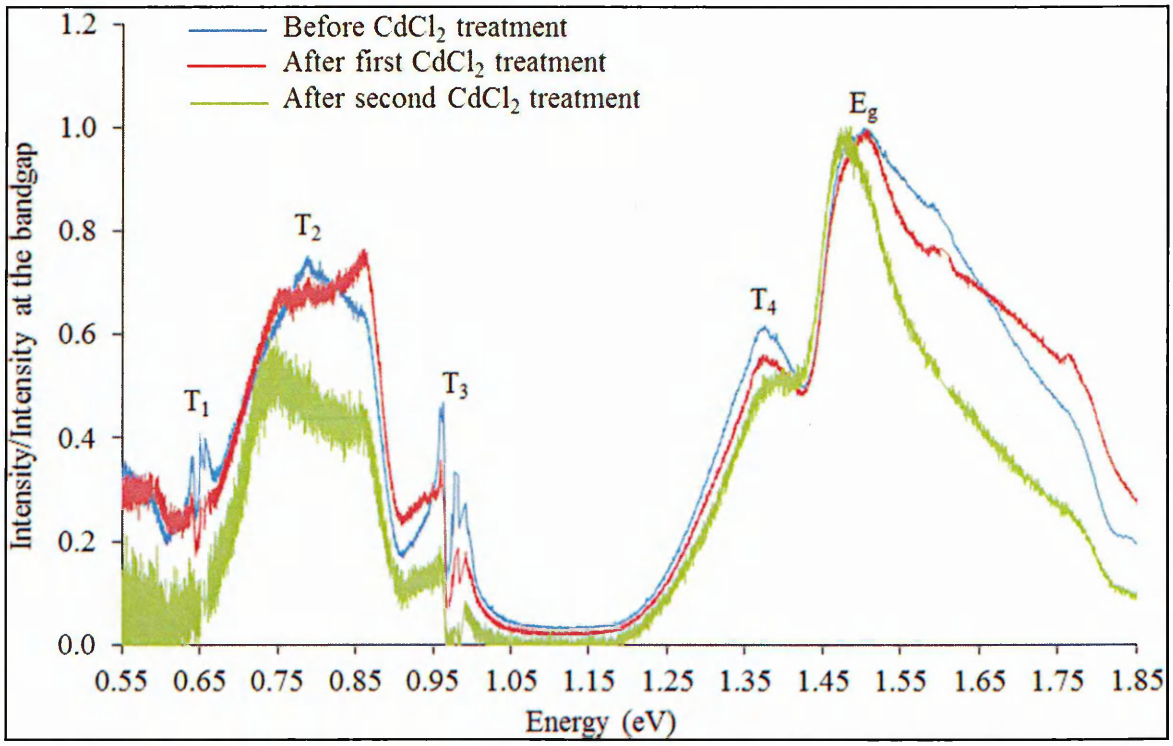


Figure 9.20: Photoluminescence spectra obtained at 80 K for as-deposited, first and second $CdCl_2$ treated CdTe layers.

Table 9.11: Photoluminescence measured at 80 K representing peaks in Figure 9.20

Energy (eV)	T_1	T_2	T_3	T_4	E_g
CdTe - As deposited	0.66	0.79	0.97	1.37	1.50
CdTe - $CdCl_2$-step 1	-	0.76	0.97	1.37	1.50
CdTe - $CdCl_2$-step 2	-	0.74	0.97	1.38	1.48

Even though $CdCl_2$ treatment could not completely remove these four defects, at least this process is beneficial in reducing the density of unwanted defects in the electrodeposited layers. An important point to highlight here is, the locations of the four defect levels showed in Table 9.11 are almost similar to the defect levels observed in high temperature melt-growth CdTe wafer [7]. This means, regardless the growth technique used, the locations of these native defects are similar in any CdTe semiconductor indicating that these levels correspond to native defects.

9.5 Possible explanation on high current density

Bandgap is a very important parameter in solar cell design. For homo-junction solar cells, knowing the bandgap means the highest V_{oc} achievable can be estimated simply by dividing the achievable p-n junction barrier height with elementary charge (1.6×10^{-19} C). The maximum J_{sc} can also be determined by assuming every single photon will create one electron-hole pair (ehp) and subsequently the electron is transported to the external circuit without any loss in the material. Figure 9.21 shows the possible maximum current density that can be produced from homo-junction solar cells [31]. The short circuit current density projected for all semiconductors in this figure is only for absorbed photons having energy equal or higher than the bandgap of the materials. Photons with energy less than the bandgap of the materials are considered not contributing to the creation of mobile charge carriers.

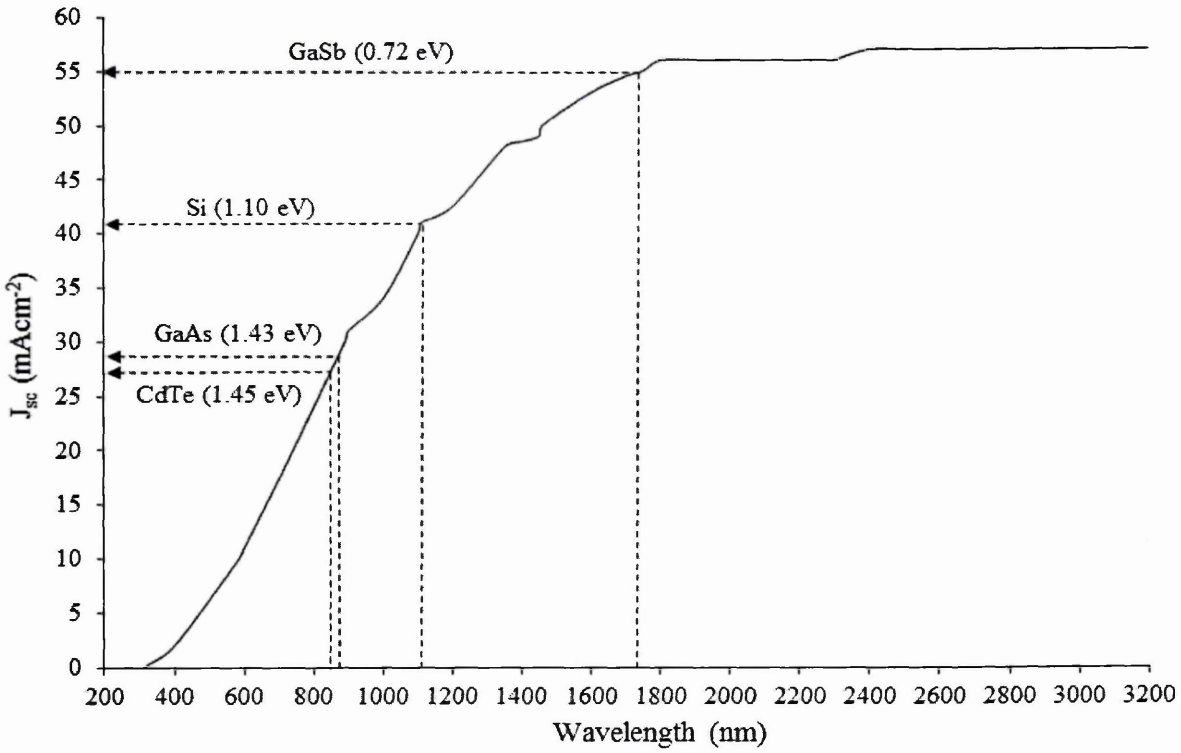


Figure 9.21: The possible maximum current density for various semiconductors as a function of wavelength. Redrawn from [31].

Obviously, material with the lowest bandgap (GaSb), will produce the highest current density. For homo-junction CdTe solar cell, the maximum current density is 27 mAcm^{-2}. However, in the previous sections, high J_{sc} of 39.3 mAcm^{-2} has been reported.

Furthermore, observation of CdTe based solar cells with excessively large Jsc values have been reported in the past by Dharmadasa *et al* (~64 $mAcm^{-2}$)[5], Chaure *et al* (~60 $mAcm^{-2}$) [15] and Echendu *et al* (~48 $mAcm^{-2}$)[6]. Clearly there are auxiliary mechanisms that help the creation of extra electron-hole pairs and therefore increasing the magnitude of short circuit current density. Therefore, it is appropriate to discuss the observation of high J_{sc} with the help of band diagrams.

Figure 9.22 shows two band diagrams that possibly exist due to the conductivity type of CdTe. Band diagram in Figure 9.22(a) represents the n-n hetero-junction interface between n-CdS and n-CdTe plus Schottky barrier at the back metal contact. Figure 9.22(b) is the band diagram of p-n hetero-junction between n-CdS and p-CdTe. It is noteworthy to recall from the PEC measurements discussed in Chapter 7, the conductivity type of CdTe thin films is n-type after chemically treated with $CdCl_2$ + CdF_2. This means the probability of obtaining band diagram as shown in Figure 9.22(a) is higher than that of Figure 9.22(b).

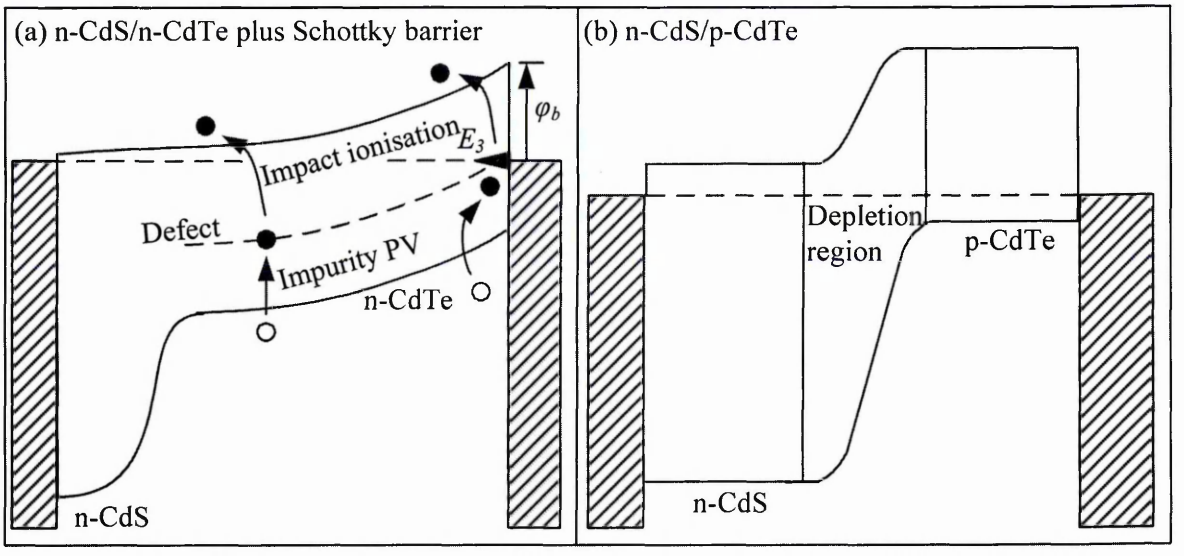


Figure 9.22: The possible band diagrams created if either n- or p-type CdTe grown on n-CdS. Note the first one is a combination of n-n junction and large Schottky barrier, while the second is a single p-n junction.

The strength of solar cell shown in Figure 9.23(a) is the existence of electric field across the entire structure. This is also known as fully depleted device [5]. So when one ehp is created, both electron and hole will move to the opposite direction instantaneously due to the shape of the band bending. In addition, ehps can be created at

almost 'any point' in the device because the electric field exists across the entire structure. For p-n hetero-junction, if the excitation of electrons occurs outside the depletion region, probability of these electrons to recombine with holes is high because of the absence of electric field.

Electron-hole pairs can be created in the n-n hetero-junction device with the assistance from surrounding heat. The surrounding heat provides energy in the form of infrared photons and this is sufficient to promote electrons from valence band to the defect level E_3. The defect level E_3 is presented in Figure 9.22(a) because this is the position that matches the calculated values of barrier height as tabulated in Table 9.10. From E_3, the electrons can be promoted to the conduction band after absorbing extra heat energy from surrounding. This mechanism is also known as impurity photovoltaic effect [32]. The photo-activity of solar cell utilizing infrared photons is not speculative because as reported by Dharmadasa *et al* in 2011, solar cells can be active under dark condition provided that efficient electric field is present in the device [32].

In the device structure shown in Figure 9.23(a), there is another mechanism to contribute to the current density. This is the combination of the impurity photovoltaic effect (IPV) and impact ionization. As shown in the band diagram heat from surrounding could promote electrons to a defect level in the bandgap through IPV effect. This electron can then be promoted to the conduction band by impact ionization from accelerating free electrons. In an optimized device structure, this can occur as an electron avalanche, effectively continuing to increase J_{sc}.

Therefore, based on these explanations, it is possible that additional ehps can be created from photons with energy less than the bandgap of the semiconductor thus increasing the magnitude of short circuit current density.

9.6 Power density (P_d) analysis

Power density (P_d) is defined as the product of V_{oc} and J_{sc}. The unit for power density is $mWcm^{-2}$ and it gives the maximum power that can be extracted from a single cell by assuming a unity fill factor.

This simple and quick analysis was performed to see how close the power density from the four best devices shown in Table 9.10 to the former world's highest efficiency CdTe solar cells. The current 21% efficiency solar cell from First Solar [33] is not included in this analysis due to the lack of data regarding its parameters.

Therefore in this analysis, only high efficiency solar cells ($\eta > 18\%$) with sufficient data available are compared with devices displayed in Table 9.10.

Table 9.12 provides the values of power density from four highest efficient solar cells in this research project. From this Table, one can see that the power densities of all cells are higher than 20 $mWcm^{-2}$. The lowest power density calculated is 21 $mWcm^{-2}$ and the highest is 27 $mWcm^{-2}$.

Power densities displayed in Table 9.12 are compared with their counterparts in Table 9.13. All power density values tabulated in Figure 9.13 are also higher than 20 $mWcm^{-2}$. From comparison, it is clear that the differences between power densities from the two groups are small. In fact, the highest power density comes from electrodeposited CdTe layers with 27 $mWcm^{-2}$.

Table 9.12: The power density calculated from the four highest efficiency solar cells as displayed in Table 9.10.

Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	P_d ($mWcm^{-2}$)
FC72	600	36.6	0.46	10.1	22.0
FC97	610	34.4	0.37	7.8	21.0
FC99	710	39.3	0.30	8.4	27.9
FC100	574	38.5	0.37	8.2	22.1

Table 9.13: Power density calculated from the former world's highest efficiency solar cells.

V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	P_d ($mWcm^{-2}$)	Team	Reference
857	28.6	0.80	19.6	24.5	General Electric	[34]
872	28.0	0.78	19.0	24.4	First Solar	[35]
852	28.6	0.77	18.7	24.4	First Solar	[35]
857	27.0	0.79	18.3	23.1	General electric	[36]

This analysis has shed light on the capability of electrodeposition to produce high quality semiconductors comparable to the high temperature deposition techniques. It is also important to note that the current densities displayed in Table 9.13 have also

exceeded the maximum J_{sc} as projected in Figure 9.22. This means, if the J_{sc} measured has exceeded the theoretical values calculated for single p-n junction with one bandgap, the result should be accepted as genuine. In fact, the observation of high J_{sc} in CdTe solar cell (> 27 $mAcm^{-2}$) has been reported in 1985 with by other research group with 36 $mAcm^{-2}$ [37].

Clearly, the way forward to increase the efficiency of CdTe solar cell is through the improvement in J_{sc}. As stated by Paudel and Yan, substantial improvement of CdTe solar cell efficiencies from 17.3% to 21% is helped by the improvement in J_{sc} [38].

9.7 Optimization of annealing temperature

So far the annealing temperature at 450°C for 15 minutes was found to be the best. However, due to the low fill factor obtained from this annealing temperature, the optimization of annealing temperature was carried out in order to find the annealing temperature that can produce high values of V_{oc}, J_{sc} and FF. The motivation for this work was initiated by the various annealing temperatures found in literature. Table 9.14 shows the annealing temperature of solar cells with efficiency above 10%.

Table 9.13: The annealing temperature and duration for electrodeposited CdS/CdTe solar cell reported in literature for cells with efficiency greater than 10%.

V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	Annealing temperature (°C)	Annealing time (min)	References
780	23.0	0.72	12.9	410	15	[17]
725	21.2	0.67	10.3	400	8-12	[19]
746	23.7	0.65	11.5	400	15	[39]

As a start, the annealing temperature of 430°C for 15 minutes was tested. Therefore, a new fabricated sample was prepared and divided into two pieces. The first piece was heat treated at 430°C for 15 minutes and the second piece was annealed at 450°C for 15 minutes.

Table 9.14 shows the solar cell parameters for two samples with different heat treatment conditions. After measuring three diodes from each sample, it is obvious that by reducing the annealing temperature, the fill factors of the solar cells with lower annealing temperature had slightly increased. However, the improvement comes with

the expense of V_{oc} and J_{sc} because on average, these parameters are higher in the sample heat-treated at 450°C for 15 minutes. When the efficiency was calculated, the average efficiency for FC110B is higher than FC110A. These results show that annealing at high temperature produced devices with better conversion efficiency. Figure 9.23 shows the J-V curves from both cases.

Table 9.14: The comparison of solar cell parameters when materials are heat-treated at 430°C and 450°C.

	FC110A				FC110B			
	430°C for 15 minutes				450°C for 15 minutes			
	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)
	420	18.2	0.32	2.4	560	19.3	0.29	3.1
	390	16.3	0.31	2.0	530	20.0	0.30	3.2
	400	17.9	0.31	2.2	540	19.8	0.28	3.0
Average	403	17.5	0.31	2.2	543	19.7	0.29	3.1

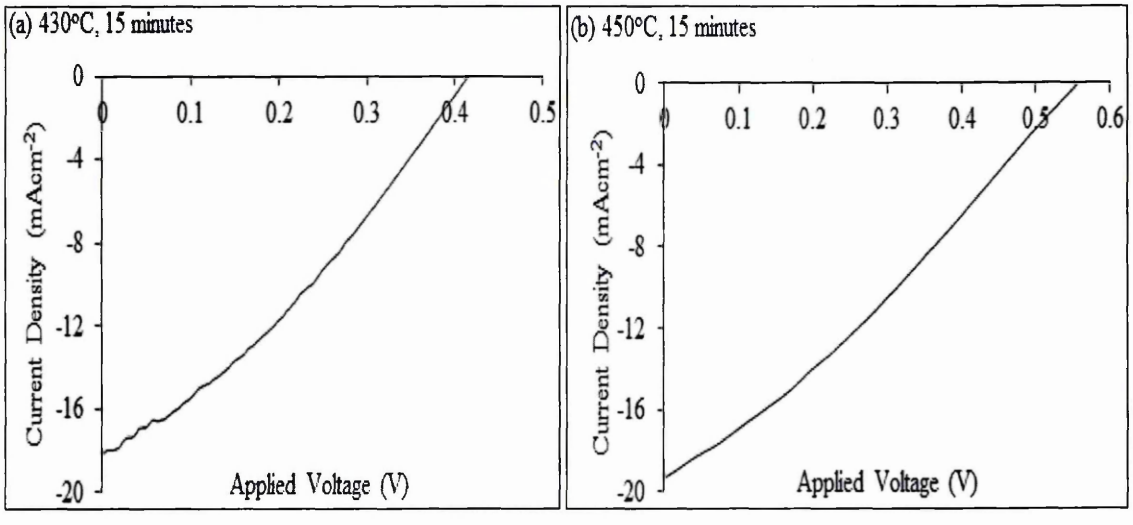


Figure 9.23: The J-V curves from highest efficiency solar cells obtained from two different annealing temperatures (430°C and 450°C).

For the next step, a new sample was prepared. This time the annealing temperature was further reduced to 410°C for 15 minutes. Similar to the previous experiment, this new sample was divided into two pieces. Heat-treatments at 410°C for 15 minutes and 450°C for 15 minutes were carried out. After the deposition of Au back

contacts, the I-V measurements were conducted on both samples. The results from I-V measurement were displayed in Table 9.15. The J-V curves from the device with highest efficiency were plotted in Figure 9.24.

Table 9.15: The comparison of solar cell parameters when materials are heat-treated at 410°C and 450°C.

	FC114A				FC114B			
	410°C for 15 minutes				450°C for 15 minutes			
	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)
	620	14.5	0.32	2.9	700	23.6	0.25	4.1
	645	14.7	0.33	3.1	630	21.7	0.25	3.4
	600	7.6	0.42	1.9	660	22.0	0.32	4.6
Average	622	12.3	0.36	2.6	663	22.4	0.27	4.0

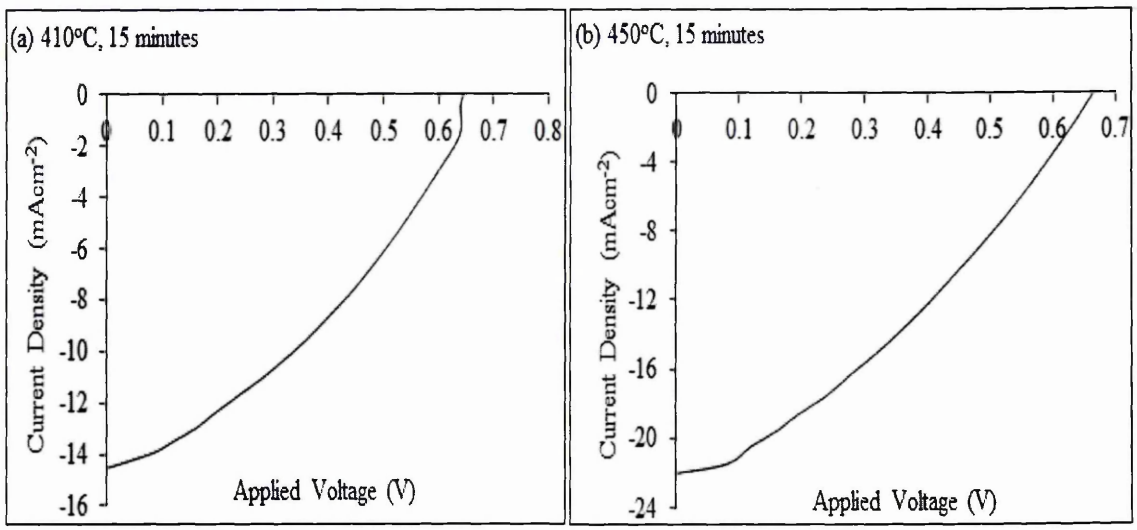


Figure 9.24: The J-V curves from highest efficiency solar cells obtained from two different annealing temperatures (410°C and 450°C).

From Table 9.15, we can see that when the annealing temperature was further reduced, the fill factor becomes higher. But unfortunately, both V_{oc} and J_{sc} were also reduced. In return, lower conversion efficiencies were obtained from the sample annealed at 410°C for 15 minutes. By looking at device efficiencies, the annealing temperature at 450°C for 15 minutes is the best annealing parameters. The last experiment presented in this subsection focused on the solar cell parameters with

respect to two different annealing times. For this experiment similar, annealing time of 400°C was employed. However, the annealing time was varied between two samples. The first sample was heat-treated at 400°C for 10 minutes while the second sample was heat-treated at 400°C for 15. Table 9.16 provides the results from the I-V measurement for both cases while Figure 9.25 displayed the J-V curves of the highest solar cells obtained from dissimilar heat-treatment conditions.

Table 9.16: The comparison of solar cell parameters when materials are heat-treated at 400°C for 10 and 15 minutes.

	FC120A				FC120B			
	400°C for 10 minutes				400°C for 15 minutes			
	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)
	510	21.9	0.48	5.4	550	22.3	0.48	5.9
	490	19.8	0.45	4.4	590	22.0	0.37	4.8
	450	20.0	0.40	3.6	490	18.3	0.46	4.1
Average	483	21.0	0.44	4.4	543	21.0	0.44	4.9

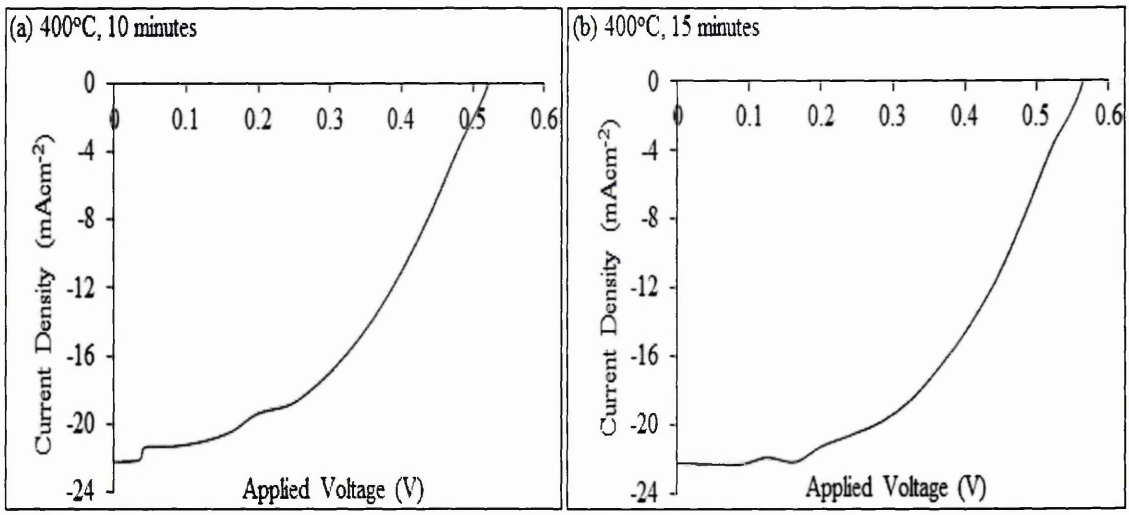


Figure 9.25: The J-V curves from highest efficiency solar cells annealed at 400°C employing two different annealing times (10 minutes and 15 minutes).

By comparing the average efficiencies, the 15 minutes annealing times give slightly higher efficiency than its 10 minutes counterpart. This slight increase is due to the higher V_{oc} resulted by extending the time of annealing. Average J_{sc} and FF for both

cases are similar. So far, 0.48 is the highest value of fill factor observed. However, V_{oc} and J_{sc} for both cases settled below 600 mV and 25 $mAcm^{-2}$ respectively thus making the reproducibility of double digit efficiency device unattainable.

The improvement of the fill factor at lower annealing temperature could be due to the less cracks or pin-holes present in the CdS or CdTe layers. All results presented in this subsection indicate that the annealing parameters found in the literature were not suitable to apply for the heat-treatment of CdS/CdTe solar cells in this research project. The reason could be due to the different furnace, properties of $CdCl_2$ solution, methodology in $CdCl_2$ treatment, etc.

9.8 Conclusion

Glass/FTO/CdS/CdTe/Au solar cells have been successfully fabricated. Both thin film semiconductors (CdS and CdTe) were deposited using low-cost electrodeposition technique. With electrodeposition at low temperature using 2-electrode system, conversion efficiency of 10.1% has been recorded. High V_{oc} and J_{sc} of 750 mV and 39.3 $mAcm^{-2}$ have been observed respectively. High J_{sc} observed was due to the existence of electric field throughout the entire solar cell structure and also assisted by impurity photovoltaic effect and impact ionisation. The inclusion on fluorine in the chemical treatment process has proven to affect the device parameters positively. Attempts to reproduce solar cells with double digit efficiency were unsuccessful due to the low values of fill factor. High resistivity of CdS layers, the usage of FTO instead of ITO and the presence of oxide layers after the chemical etching are the factors that could contribute to the high series resistance, R_s. The presence of pin-holes in CdS or CdTe or both layers is the cause for the low shunt resistance, R_{sh}.

Even though the fill factor can be increased by lowering the annealing temperature, the efficiency of CdS/CdTe solar cells becomes low due to the decrease in V_{oc} and J_{sc}. Improving the efficiency of electrodeposited CdS/CdTe solar cells through optimization of annealing parameters was proven to be tricky because in order to do so, reproducibility of solar cells around 7-8% has to be established first.

To rectify this problem, a very thin pin-hole plugging layer can be deposited between CdTe and metal back contacts to improve the fill factor. Further discussions about the fabrication of glass/FTO/CdS/CdTe/ZnTe/Au solar cells are provided in Chapter 10.

The values of ideality factor, rectification factor and barrier height were obtained through measurement under dark condition. Ideality factors calculated show values between 1.10 to 1.74. This is an indication that the current transport mechanism from semiconductor to metal was dominated by thermionic emission and recombination. Rectification factors were found to be higher than 10^3 for devices with conversion efficiency higher than 7% indicating high quality diode fabricated from electrodeposition technique. Barrier heights between 0.72 eV to 0.78 eV represent strong Fermi level pinning at the midgap location. Results from PL measurement showed the significant presence of high density and widely distributed defects at this position. Hence, minimizing defects in the middle of the bandgap was proven to be a huge challenge to overcome in order to further increase the efficiency of electrodeposited CdS/CdTe solar cells.

From power density analysis in section 9.6, all electrodeposited CdS/CdTe cells produce power densities higher than 20 $mWcm^{-2}$ which are comparable to the former world's highest efficiency solar cells. This is a sign that electrodeposition can produce high quality semiconductors comparable to other high temperature growth techniques.

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Chapter 10: Metal-Insulator-Semiconductor (MIS) type electrical contacts in solar cells

10.1 Introduction

Chapter 9 has presented the fabrication process and also the assessment of all electrodeposited thin film CdS/CdTe solar cells. In the previous chapter, solar cell with efficiency of 10.1% has been reported. However, attempts to reproduce devices with double digit efficiency were unsuccessful due to the presence of pin-holes in CdS/CdTe layers. This led to the increase of electrical current flows through the shunting paths thus lowering the fill factor. Lowering the annealing temperature was proven to be successful to improve the fill factor but it came at the expense of open circuit voltage (V_{oc}) and short circuit current density (J_{sc}). As a result, the efficiency of solar cells annealed at low temperature is low compared to the devices annealed at high temperature. Clearly, improving the fill factor through low temperature annealing is not feasible. This means an alternative solution to the pin-hole problem should be explored.

Plugging the pin-holes by incorporating additional thin layer between CdTe and the back metal contact has proven to be successful in order to improve the fill factor [1-4,7]. Pin-hole plugging layer (PPL) works by filling the gaps present in either CdS or CdTe layers as shown in Figure 10.1. Both organic and inorganic materials can be used as the PPLs. Examples of organic materials are polyaniline (PANI) [1-3], pyrrole [4], cadmium stearate [5] and C4-anthracene [6]. While for the inorganic materials, CaF_2 and ZnTe have shown promising results [7,8]. If these gaps are perfectly plugged, the shunt resistance will increase and in return, the recombination of electrons and holes will be minimized.

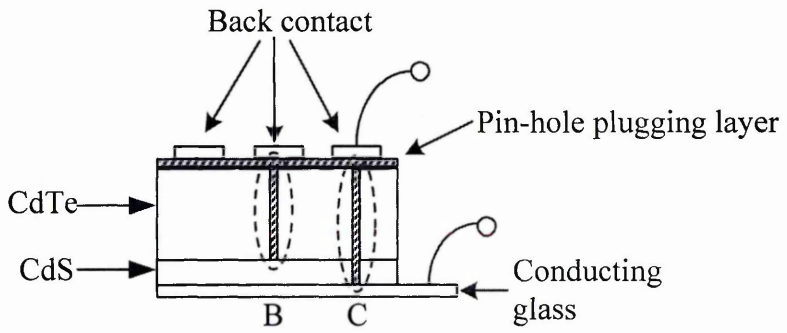


Figure 10.1: Minimizing shunting path by filling the gaps with pin-hole plugging layers.

Open circuit voltage can increase if the presence of PPLs creates metal-insulator-semiconductor structure as shown by the band diagram depicted in Figure 10.2. Since ZnTe semiconductor has bandgap of 2.26 eV [9] which is higher than CdTe (1.45 eV), the barrier height will rise, thus at the same time increasing the V_{oc}. The improvement of J-V curve after the inclusion of PPLs is depicted in Figure 10.3.

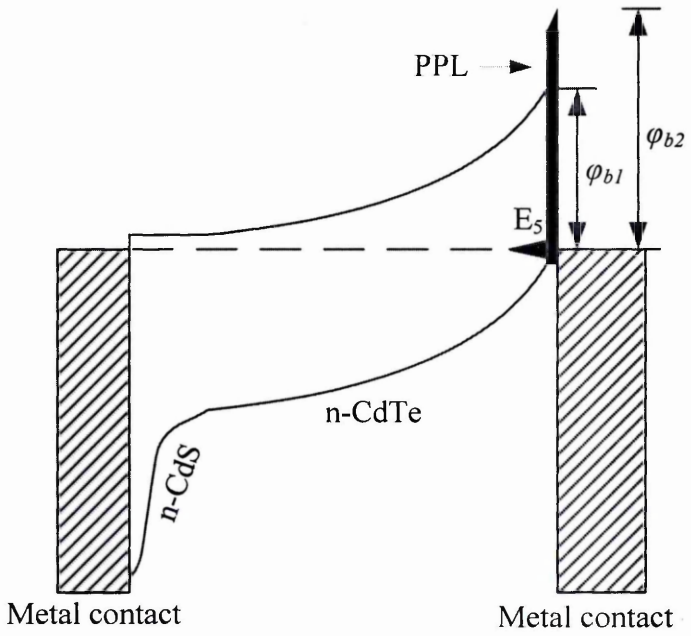


Figure 10.2: The enhancement of barrier height ($\phi_{b2} > \phi_{b1}$) helped by the inclusion of PPLs with bandgap higher than n-CdTe.

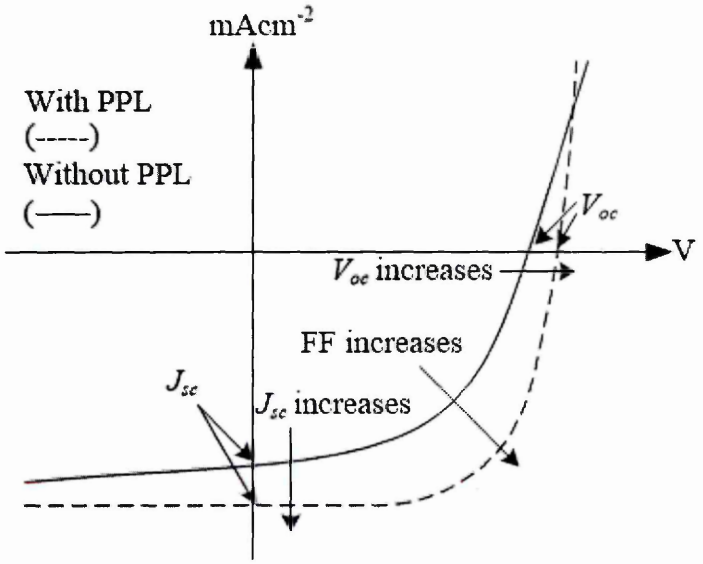


Figure 10.3: The improvement of J-V curve after the inclusion of PPLs at the back of the solar cell.

The number of e-h pairs created by incoming photons remains constant. But when there are pin-holes, photo-generated charge carriers recombine within the device, without contributing to the current in the external circuit. As soon as the shunting paths are blocked, all photo-generated e-h pairs travel in the external circuit thus increasing the J_{sc}.

From the cross-sectional SEM image in Figure 8.6, it is clear that ZnTe has a unique property of covering the contour of the FTO efficiently. Deducing from this result ZnTe was experimented as PPL.

Looking back to the history, the idea of fabricating n-CdS/i-CdTe/p-ZnTe solar cell was initiated by Meyers *et al* in 1987 [10]. The band diagram of n-CdS/i-CdTe/p-ZnTe solar cell is shown in Figure 10.4. This solar cell structure is simply known as p-i-n solar cell device. As shown in Figure 10.4, sunlight can enter the solar cell by either side due to the wide bandgap materials placed at the front and back of the device. It was introduced to the PV community as a solution to solve the problem of making low resistance contact between p-CdTe and Au/Cu at the back of the solar cell.

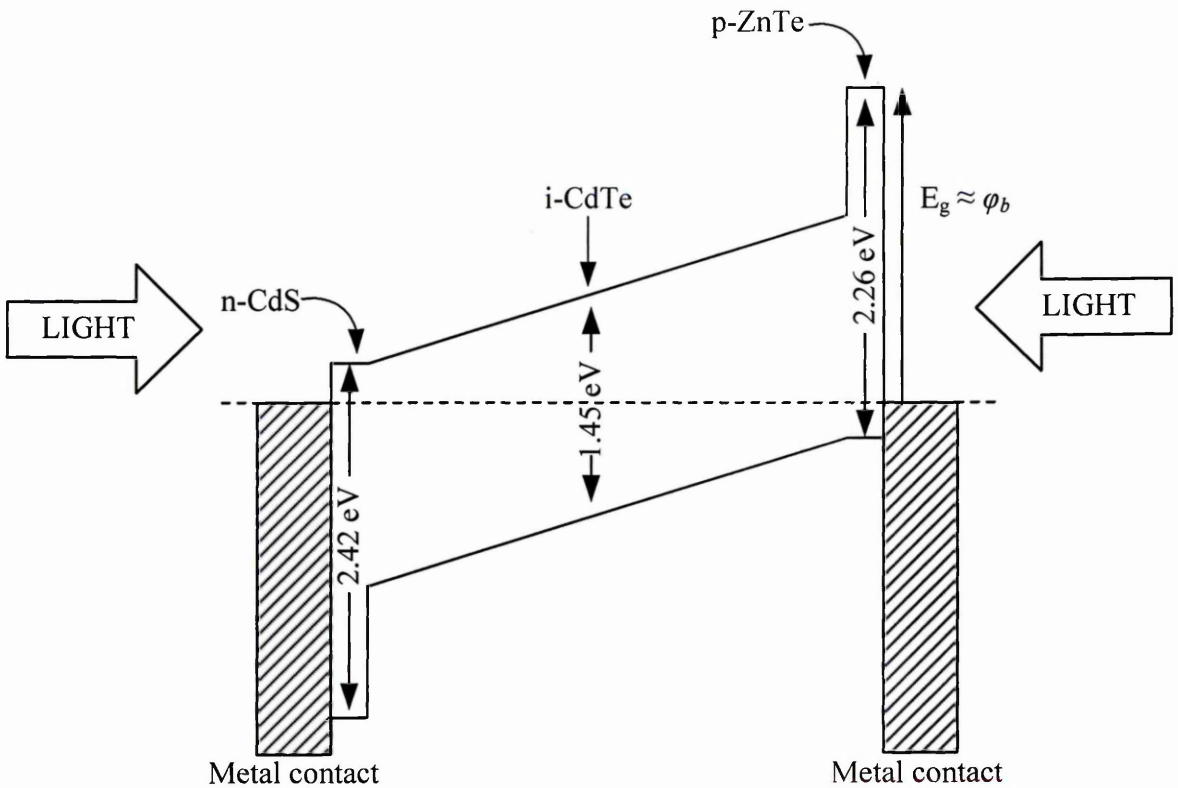


Figure 10.4: The band diagram of n-CdS/i-CdTe/p-ZnTe showing all the bandgap values for each material.

It is well known that to make ohmic contact at the p-CdTe/metal interface is a huge challenge to solve. This is because the electron affinity of CdTe is very high (~4.3 eV) and the work functions of available metal contacts (eg; Au, Cu, Ni, etc) are not high enough to create barrier height with equal or less than 0.40 eV ($\leq$ 0.40 eV) [11,12].

Solution to this problem is either by increasing the hole density at the p-CdTe/ metal interface or by depositing p-type semiconductor between p-CdTe and metal back contact [13]. ZnTe normally exists as a p-type semiconductor and due to this reason, it is the preferable solution due to the complexity of increasing the p-type dopant in CdTe layers [14]. In addition to that, numerical simulation by Sites and Pan also shows that p-i-n structure is the more convenient way of achieving open circuit voltage of 1 volt for CdS/CdTe solar cells [15].

The highest reported efficiency of n-CdS/i-CdTe/p-ZnTe is 10.7% from the undoped ZnTe [10]. However this record was overtaken in 1996 when Feng *et al* reported the conversion efficiency of 12.1% by doping the ZnTe thin film with Cu [16]. Scaling up process also showed promising result. Meyers reported conversion efficiency of 9.3% with 5.1 cm^2 size p-i-n solar cell in 1988 [17].

10.2 Fabrication of glass/FTO/CdS/CdTe/ZnTe/Au solar cells

Almost the entire fabrication process of glass/FTO/CdS/CdTe/ZnTe/Au is similar to what have been presented in section 9.2. The only different is, after the chemical etching, a very thin ZnTe thin film was electrodeposited on glass/FTO/CdS/CdTe using 2-electrode system as presented in Chapter 8. For initial trials, the deposition time was up to 20 minutes. After several samples were tested, it was found that the optimum time for electrodeposition of ZnTe was just between 3 to 4 minutes in order to get the optimized thickness. In all cases, ZnTe layers were electrodeposited using V_g = 1675 mV. After the electrodeposition of ZnTe layers, the glass/FTO/CdS/CdTe/ZnTe samples were heat-treated at 300°C for 7 minutes. Before the I-V measurement was conducted, the gold back contacts with thickness of 100 nm were sputtered on top of glass/FTO/CdS/CdTe/ZnTe using Quorum 150T sputtering system as shown in Figure 10.5.

Figure 10.5: Quorum 150T sputtering system used to deposit back metal contacts.

10.3 Assessment of glass/FTO/CdS/CdTe/ZnTe/Au solar cells

The I-V measurements of glass/FTO/CdS/CdTe/ZnTe/Au were performed using LOT Quantum Design solar simulator system assisted by Xenon light as shown in Figure 10.6. The intensity of the light has been calibrated to AM1.5 conditions (100 mW/cm^{-2}).

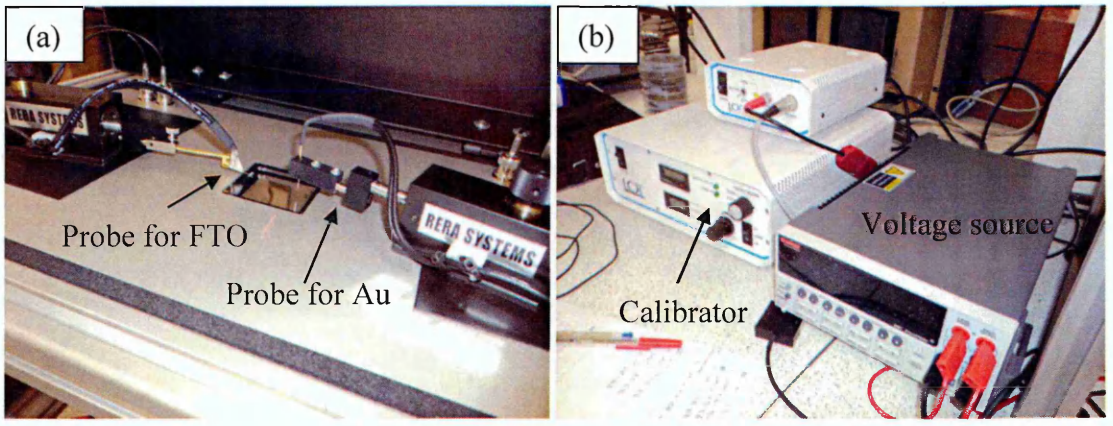


Figure 10.6: LOT Quantum Design solar simulator system. (a) Probes for FTO and Au contacts. (b) Voltage source and Xenon light calibrator.

10.4 Results and discussions

Table 10.1 shows the results of I-V measurements for glass /FTO/ CdS/ CdTe/ZnTe/ Au solar cells fabricated for the first time. In this experiment, one glass/FTO/CdS/CdTe solar cell sample was cut into three pieces. The first piece had no

ZnTe layers deposited on top of it. Zinc telluride thin films were electrodeposited on the second and the third piece for 10 and 20 minutes respectively to produce glass/FTO/CdS/CdTe/ZnTe solar cell structure. The thickness of ZnTe layers deposited for 10 and 20 minutes is ~35 and ~70 nm respectively. As shown in Table 10.1, sample without ZnTe is the best performing device. The other two samples are low performing devices because the optimum thickness of ZnTe has not yet been achieved.

Table 10.1: Results of I-V measurements for CdS/CdTe solar cells. Samples with and without ZnTe layers are compared.

FC150A				FC150B				FC150C			
No ZnTe				ZnTe 10 minutes				ZnTe 20 minutes			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
500	4.0	0.36	0.7	400	2.0	0.33	0.3	400	1.6	0.30	0.2
510	4.6	0.36	0.8	380	2.5	0.33	0.3	310	1.6	0.30	0.1
590	6.7	0.35	1.4	390	3.5	0.32	0.4	360	2.0	0.26	0.2
533	**5.1**	**0.36**	**1.0**	**390**	**2.7**	**0.33**	**0.3**	**357**	**1.7**	**0.29**	**0.2**

Bold numbers = average values

These results indicate that when the thickness of ZnTe is too high, it will affect the solar cells negatively. Thicker ZnTe layers will increase the series resistance in the solar cells thus further reducing the fill factors. The thickness of ZnTe layer was further reduced. In this new attempt, the deposition time was reduced to 5 minutes (~20 nm). The comparison of solar cell parameters between CdS/CdTe/Au and CdS/CdTe/ZnTe/Au solar cells is shown in Table 10.2.

Table 10.2: Results of I-V measurements for CdS/CdTe solar cells, with and without ZnTe layers for comparison.

Device structure	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
CdS/CdTe/Au	200	0.21	0.25	0.01
CdS/CdTe/ZnTe/Au	300	0.77	0.31	0.07

Even though the efficiency of both solar cells is extremely low, this result shows that when the thickness of electrodeposited ZnTe semiconductor is near to the optimum

values, the enhancement of V_{oc}, J_{sc} and FF is confirmed. Figure 10.7 shows the J-V curves for CdS/CdTe/Au and CdS/CdTe/ZnTe/Au solar cells.

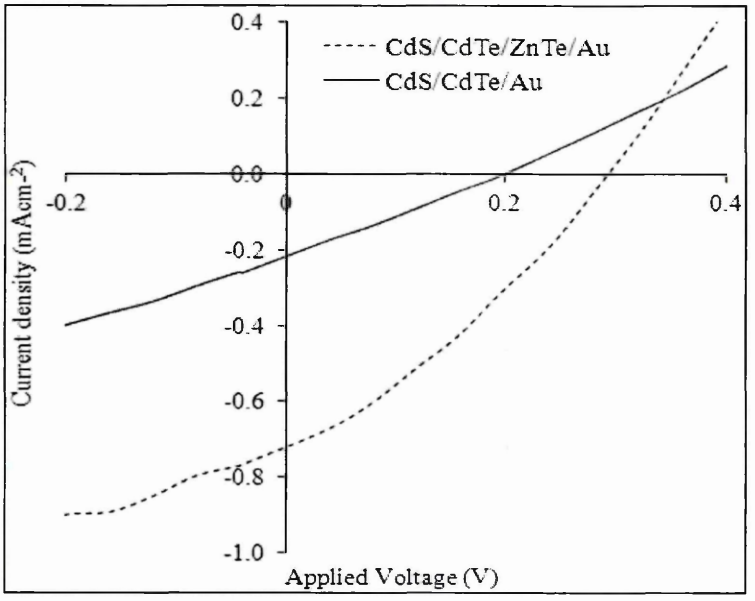


Figure 10.7: The comparison of J-V curves of glass/FTO/CdS/CdTe/Au and glass/FTO/CdS/CdTe/ZnTe/Au solar cells [8].

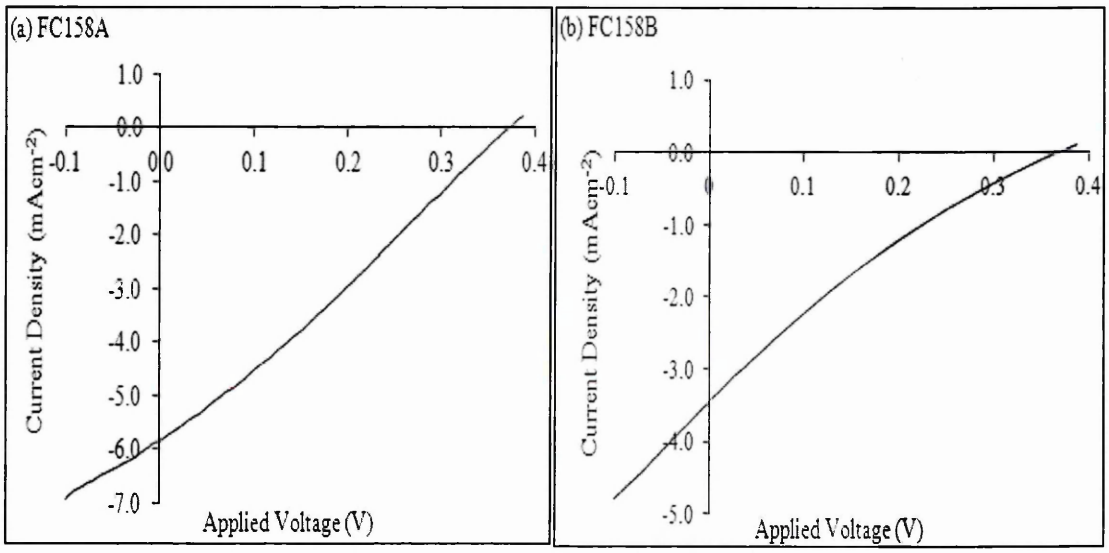
10.4.1 Reproducibility of higher device parameters (V_{oc} , J_{sc} and FF)

Since the deposition time to acquire optimum thickness of the ZnTe layers is known, several new samples were prepared in order to check whether the improvement of V_{oc}, J_{sc} and FF is reproducible using electrodeposition. Table 10.3 shows the results from three newly prepared samples. Numbers in bold represent the average values. Discussions presented in this sub-section will be concentrated on the average values. Figure 10.8 shows the J-V curves of the cells with the highest efficiency recorded from CdS/CdTe and CdS/CdTe/ZnTe solar cells.

Prior to deposition of gold back contacts, every sample was cut into two pieces. After chemical etching, half of the sample was electrodeposited with ZnTe for 3 minutes followed by heat-treatment in air for 300°C for 7 minutes. This action led to the side-by-side comparison between CdS/CdTe and CdS/CdTe/ZnTe solar cells.

Table 10.3: The comparison between CdS/CdTe/Au and CdS/CdTe/ZnTe/Au. ZnTe PPLs were heat-treated in air at 300°C for 7 minutes. Three newly prepared samples (FC158, FC 160 and FC161) were compared. Numbers in bold represent the average values.

FC158A (With ZnTe)				FC158B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
400	5.5	0.25	0.55	410	2.5	0.21	0.22
370	5.1	0.25	0.47	350	3.4	0.21	0.25
370	5.8	0.27	0.58	370	3.5	0.20	0.26
380	**5.5**	**0.26**	**0.53**	**377**	**3.1**	**0.21**	**0.24**
FC160A (With ZnTe)				FC160B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
440	5.0	0.37	0.81	270	4.2	0.25	0.28
440	5.5	0.36	0.87	340	7.1	0.26	0.63
440	5.3	0.38	0.89	130	2.9	0.24	0.09
440	**5.3**	**0.37**	**0.86**	**247**	**4.7**	**0.25**	**0.33**
FC161A (With ZnTe)				FC161B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
260	8.4	0.26	0.57	210	7.2	0.25	0.38
270	7.1	0.26	0.50	270	7.0	0.25	0.47
270	11.1	0.26	0.78	290	5.4	0.25	0.39
267	**8.9**	**0.26**	**0.62**	**257**	**6.5**	**0.25**	**0.41**



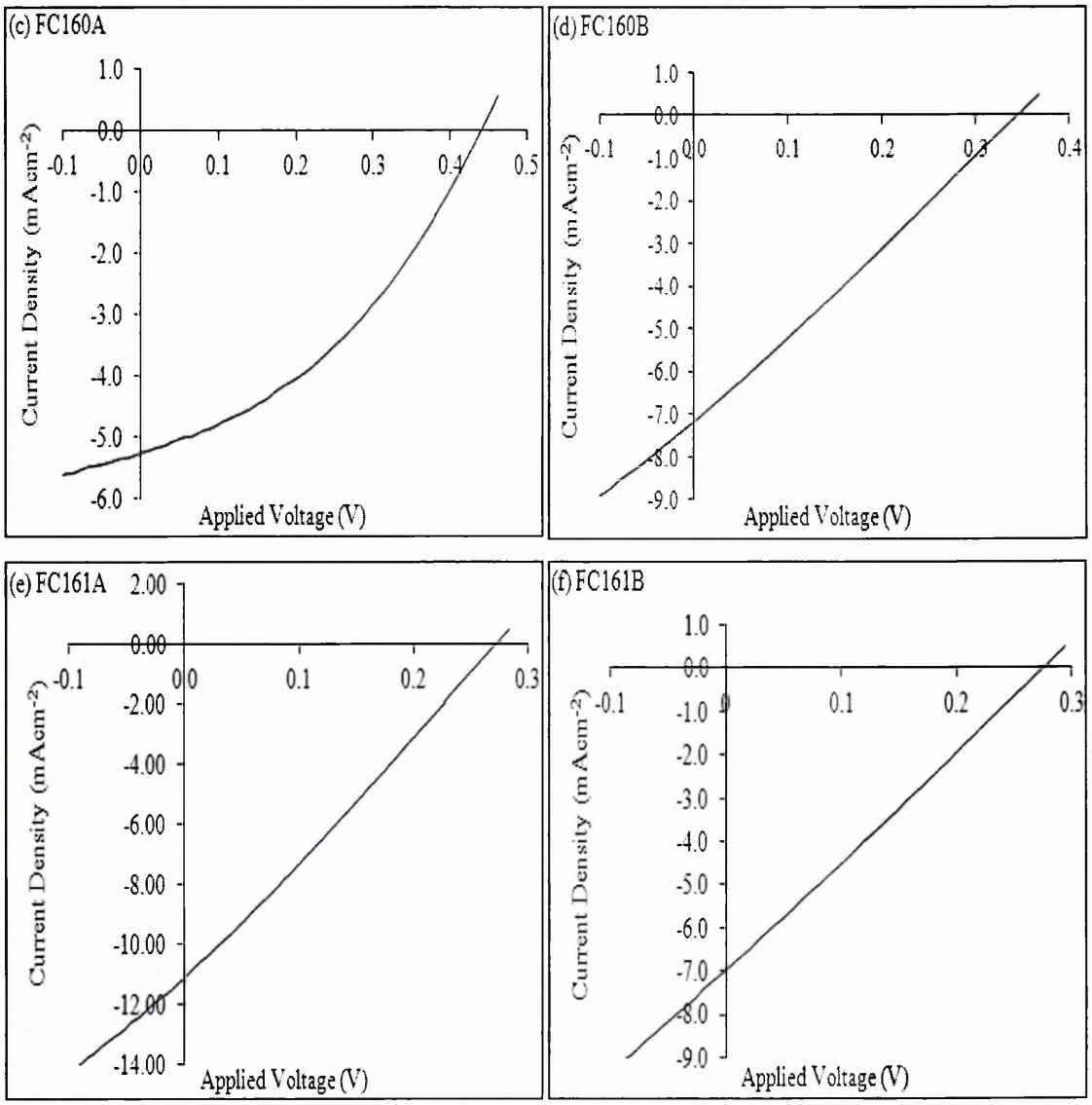


Figure 10.8: The J-V curves comparing the highest efficiency solar cells obtained from CdS/CdTe and CdS/CdTe/ZnTe solar cells.

Results from sample FC158, FC160 and FC161 show that the electrodeposition of ZnTe thin films for 3 minutes (~9-14 nm thick) affect these devices positively. On average all samples that incorporated ZnTe layers have shown higher conversion efficiency than their counterparts. The improvements can be seen in all three parameters. Although the device parameters observed are low, it is clear that the inclusion of a thin ZnTe layer enhances all three device parameters.

Since the incorporation of ZnTe layers has improved the efficiency of CdS/CdTe solar cells, efforts were later focused on reducing the processing time of CdS/CdTe/ZnTe solar cells. To achieve this goal, the heat-treatment process was skipped. Instead, after the electrodeposition of ZnTe, the gold back contacts were

directly sputtered on top of ZnTe layers. Table 10.4 shows results from a new batch of samples. In these new experiments, all ZnTe layers used were not heat-treated.

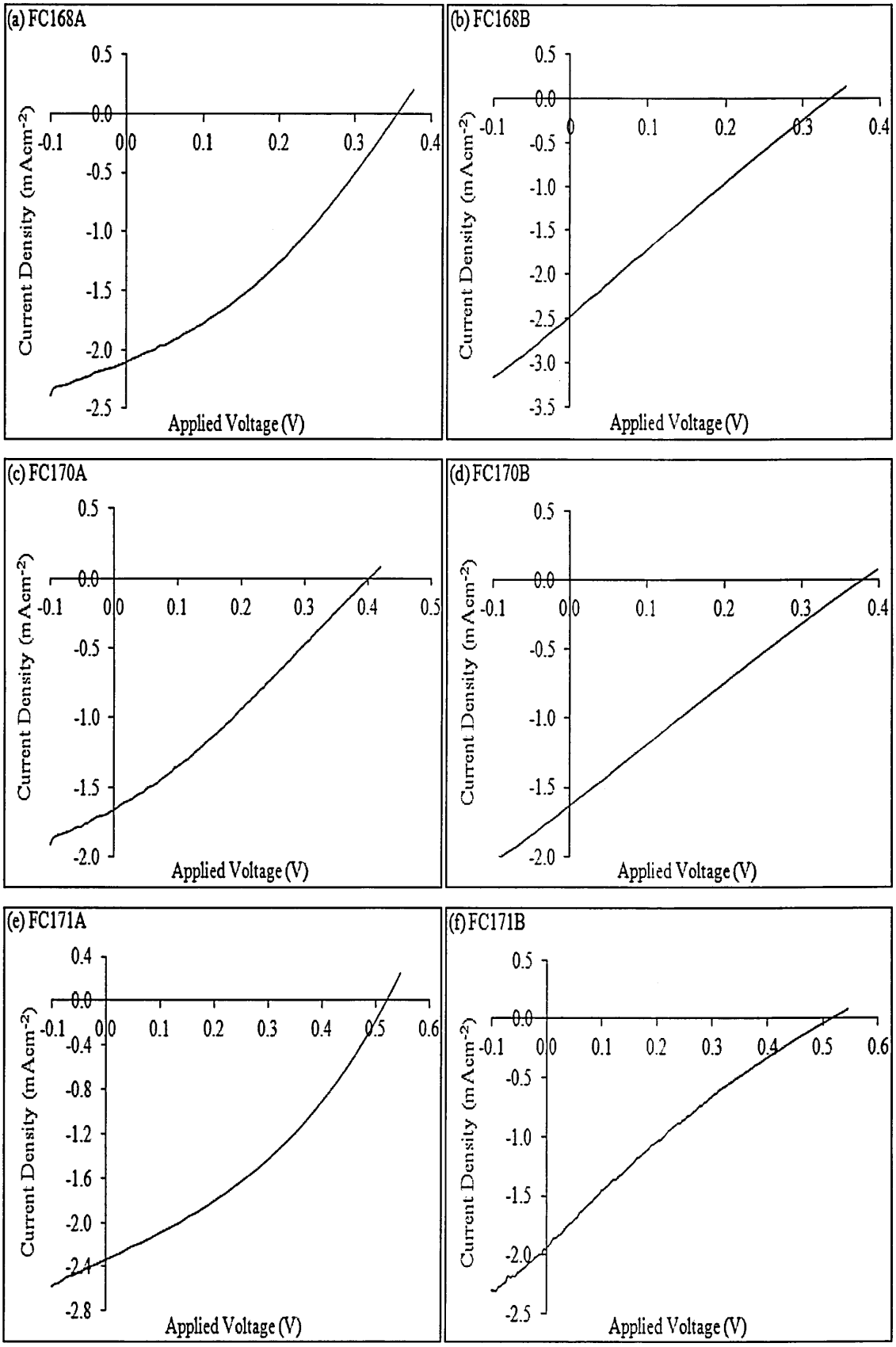
Table 10.4: The comparison between CdS/CdTe/Au and CdS/CdTe/ZnTe/Au. ZnTe layers were not heat-treated. Seven newly prepared samples (FC168 to FC185) were compared. Numbers in bold represent the average values.

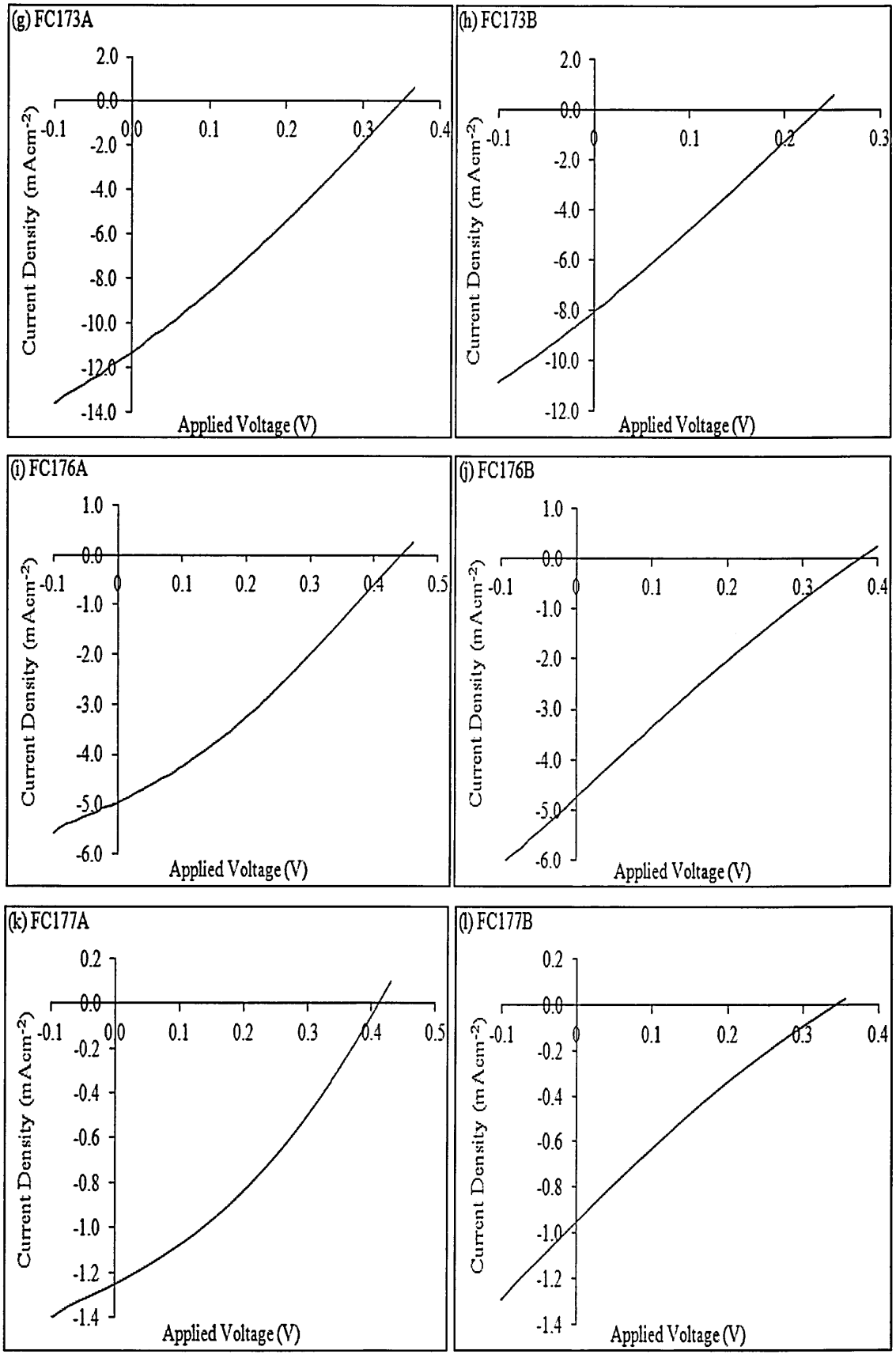
FC168A (With ZnTe)				FC168B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
380	1.5	0.36	0.21	340	1.2	0.23	0.09
360	2.1	0.34	0.26	350	1.7	0.23	0.14
350	2.0	0.34	0.24	340	2.5	0.24	0.20
363	**1.9**	**0.35**	**0.24**	**343**	**1.8**	**0.23**	**0.14**
FC170A (With ZnTe)				FC170B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
370	1.3	0.27	0.13	410	1.1	0.24	0.11
400	1.7	0.28	0.19	390	1.4	0.24	0.13
380	1.4	0.26	0.14	380	1.6	0.24	0.15
383	**1.5**	**0.27**	**0.15**	**393**	**1.4**	**0.24**	**0.13**
FC171A (With ZnTe)				FC171B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
460	1.3	0.36	0.22	510	1.9	0.22	0.21
440	1.2	0.34	0.18	510	1.3	0.21	0.14
520	2.3	0.35	0.43	390	1.1	0.22	0.09
473	**1.6**	**0.35**	**0.28**	**470**	**1.4**	**0.22**	**0.15**
FC173A (With ZnTe)				FC173B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
180	7.5	0.26	0.35	100	7.0	0.25	0.18
260	10.8	0.28	0.79	130	8.0	0.25	0.26
350	11.3	0.28	1.11	240	8.1	0.26	0.51
263	**9.9**	**0.27**	**0.75**	**157**	**7.7**	**0.25**	**0.32**

FC176A (With ZnTe)				FC176B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
430	4.3	0.31	0.57	380	4.8	0.23	0.42
410	4.7	0.31	0.60	330	4.4	0.22	0.32
440	4.9	0.31	0.67	350	3.7	0.22	0.28
427	**4.6**	**0.31**	**0.61**	**353**	**4.3**	**0.22**	**0.34**
FC177A (With ZnTe)				FC177B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
390	1.0	0.33	0.13	330	0.7	0.23	0.05
410	1.3	0.33	0.18	340	0.7	0.24	0.06
410	1.2	0.34	0.17	340	1.0	0.22	0.07
403	**1.2**	**0.33**	**0.16**	**337**	**0.8**	**0.23**	**0.06**
FC185A (With ZnTe)				FC185B (Without ZnTe)			
V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)
360	1.3	0.48	0.22	300	3.1	0.23	0.21
330	2.1	0.48	0.33	260	6.1	0.24	0.38
300	2.6	0.46	0.36	230	3.3	0.22	0.17
330	**2.0**	**0.47**	**0.30**	**263**	**4.2**	**0.23**	**0.25**

Table 10.4 shows that all CdS/CdTe/ZnTe samples produce higher fill factors than CdS/CdTe. Even without heat-treatment, the inclusion of ZnTe as PPL still affects the devices positively. This is a significant achievement in this research project because by skipping the heat-treatment process, overall device processing time can be reduced. Because, for the heat-treatment process to complete, firstly, the furnace needs to be heat-up to 300°C. This process can take up to 20 minutes. The next step is the heat–treatment of ZnTe layers for 7 minutes. After that, 15 minutes have to be reserved to allow the samples to cool down to room temperature before the deposition of back contacts can be initiated. So, roughly, between 40 to 45 minutes of processing time can be reduced. Table 10.4 also shows that all seven samples with ZnTe layers have obtained higher efficiency than samples without ZnTe. These results once again show the reproducibility of obtaining higher V_{oc}, J_{sc}, and *FF* by incorporating ZnTe through electrodeposition technique.

The J-V curves of the highest solar cells recorded for the two cases are compared in Figure 10.10.




(g) FC173A
Current Density (mAcm-2)
Applied Voltage (V)
(h) FC173B
Current Density (mAcm-2)
Applied Voltage (V)
(i) FC176A
Current Density (mAcm-2)
Applied Voltage (V)
(j) FC176B
Current Density (mAcm-2)
Applied Voltage (V)
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(l) FC177B
Current Density (mAcm-2)
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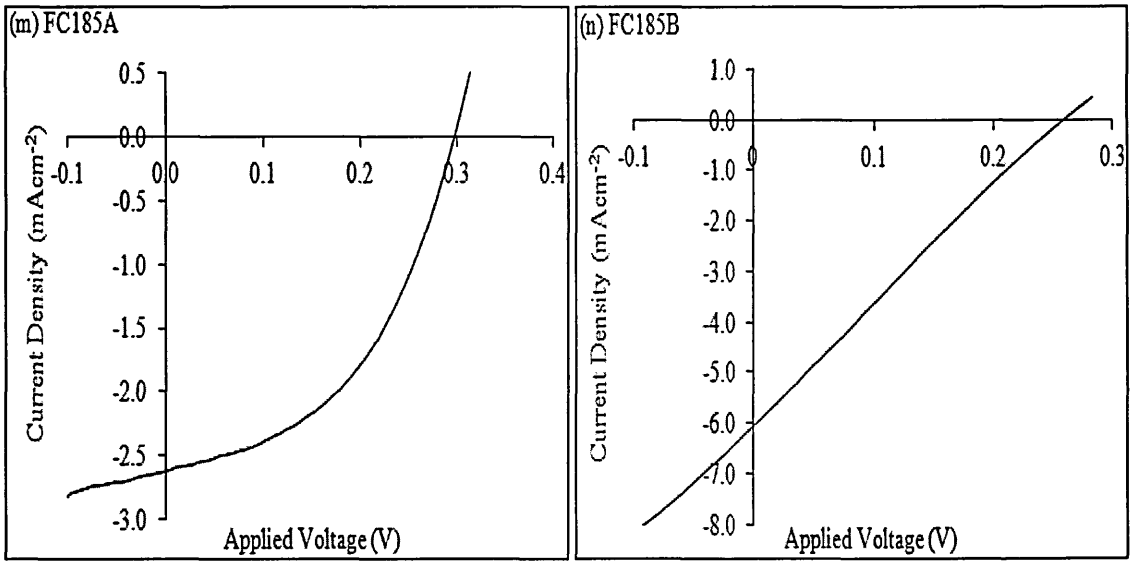

Figure 10.10: The J-V curves comparing the highest efficiency solar cells obtained from CdS/CdTe/Au and CdS/CdTe/ZnTe/Au solar cells. ZnTe layers were not heat-treated in these devices.

Table 10.5 provides the information about how far the improvements have been achieved by incorporating PPLs in CdS/CdTe solar cells. All values displayed in this table were obtained using the average values shown in bold figures.

In general, all three parameters show improvement after the inclusion of ZnTe. By looking and the average values, the incorporation of ZnTe as the last layer has improved the V_{oc}, J_{sc} and *FF* by 22%, 18.7% and 39.6% respectively. Obviously, fill factor is the better beneficiary from the incorporation of PPL in CdS/CdTe solar cells. If the improvement comes from all three parameters, we can see that on average, conversion efficiency has improved by almost 91%. Simply, if the conversion efficiency of a CdS/CdTe solar cell is 8%, the inclusion of ZnTe will take the efficiency close to 15.3%. Perhaps, the increase of conversion efficiency up to 91% seems unrealistic. However, it is sufficient if the conversion efficiency can be increased by 25 to 30% after the inclusion of ZnTe.

Table 10.5: The improvement of device parameters from CdS/CdTe/ZnTe solar cells. All values are presented in percentage (%).

Sample ID	Relative increase in %			
	V_{oc}	J_{sc}	FF	η
FC158	0.8	77.4	23.8	121.0
FC160	78.1	12.7	48.0	160.6
FC161	3.9	36.9	4.0	51.2
FC168	5.8	5.6	52.1	71.4
FC170	-2.4	7.1	12.5	15.4
FC171	0.6	14.3	59.1	86.7
FC173	67.5	28.6	8.0	134.3
FC176	21.0	7.0	40.9	79.4
FC177	19.6	50.0	43.5	166.7
FC185	25.5	-52.4	104.3	20.0
Average	**22.0**	**18.7**	**39.6**	**90.7**

As stated earlier in this chapter, the purpose of incorporating ZnTe is to increase the shunt resistance. Therefore, the shunt resistances of all solar cells displayed in Figure 10.8 and 10.9 were calculated. The method of calculating the shunt resistance is presented in Figure 5.55 (Chapter 5). Results are tabulated in Table 10.6.

Clearly, the purpose of increasing the shunt resistance through the deposition of thin film ZnTe layers has successfully been achieved. From this table all CdS/CdTe/ZnTe/Au solar cells show an increase of shunt resistance compared to their CdS/CdTe/Au counterparts except for sample FC161. Even though this sample shows slightly higher fill factor, the shunt resistance decreases with the inclusion of ZnTe layers. This observation can be explained by analyzing the straight line portion in the third quadrant of Figure 10.8(c). From this figure we can see that the gradient J-V curve for FC161B is slightly higher than FC161A thus resulting in higher shunt resistance for CdS/CdTe/Au solar cells.

Table 10.6: Shunt resistances of CdS/CdTe solar cells before and after the inclusion of ZnTe layers.

Sample ID	Shunt resistance (Ω)	
	Without ZnTe	With ZnTe
FC158	2413	2870
FC160	1830	8846
FC161	1361	1017
FC168	4616	10982
FC170	8166	12249
FC171	8166	12739
FC173	1133	1367
FC176	2377	4976
FC177	9100	19904
FC185	1769	18743

10.4.2 Thickness of ZnTe pin-hole plugging layers

Thickness of ZnTe PPLs was estimated with the help from current density versus time graphs obtained from Gillac computerized potentiostat. Figure 10.6 shows the graphs of current density versus time from four different samples. Even though all samples were electrodeposited for 3 minutes, the values of current density were recorded after 30 seconds (point A). The decision was taken because this is the point where the current densities start to stabilize. The average current densities were determined by finding the 'middle' values between point A and B. The thickness of ZnTe PPLs was calculated using Equation (4.3) presented in Chapter 4.

However, it is important to mention that the graphs of current density were not recorded for all samples. This was subjected to the availability of the computerized potentiostat. When the non-computerized potentiostat was used, the current densities were recorded manually at every 30 seconds.

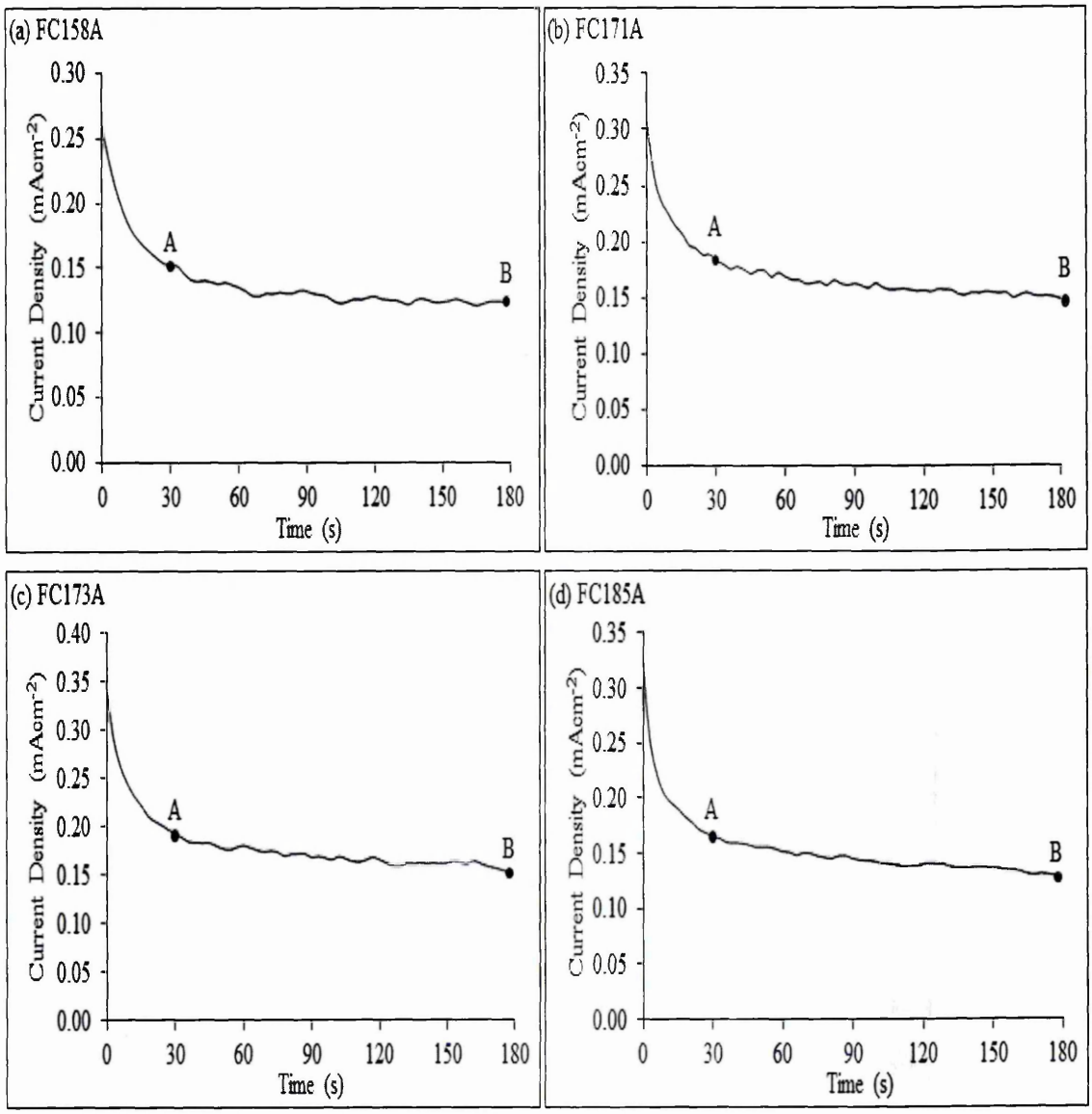

Figure 10.10: The graphs of current density versus time recorded for 3 minutes for four different samples. The 'middle' current density values between point A and B were used to calculate the thickness of ZnTe PPL.

All the average current densities were tabulated in Table 10.7. From this table, one can see that the current densities were in the range of 110 to 180 μAcm^{-2}. The thickness of ZnTe PPL for all samples calculated show the values between 9 to 14 nm. Roughly, the suitable thickness of ZnTe PPL in order to treat the pin-hole problem should be between 9 to 14 nm.

Table 10.7: The current densities and thicknesses of ZnTe PPL obtained from ten different samples.

Sample ID	Average current density (μAcm^{-2})	Thickness (nm)
FC158A	139	11
FC160A	180	14
FC161A	150	12
FC168A	120	9
FC170A	110	9
FC171A	154	12
FC173A	158	13
FC176A	108	9
FC177A	150	12
FC185A	147	12

10.5 Conclusion

The fabrication of all electrodeposited glass/FTO/CdS/CdTe/ZnTe/Au solar cells have successfully been conducted through electroplating utilizing 2-electrode system. As presented in Chapter 9, CdS/CdTe solar cells suffer from the low fill factor problem. This chapter has presented that the increase of all three device parameters is attainable through the electrodeposition of very thin ZnTe layers between CdTe and back metal contacts. ZnTe thin films were electrodeposited for a very short time (3 minutes) at the growth voltage of V_g = 1675 mV. The calculated thickness of ZnTe PPLs was found to be between ~9 to 14 nm.

The relative improvement of V_{oc}, J_{sc} and FF has been proven reproducible through the inclusion of a very thin ZnTe semiconductor between CdTe and the metal back contacts. However, the absolute values of solar cell parameters were far from the best, because of the particular batch of samples used. Shunt resistances show higher values after the inclusion of ZnTe PPLs indicating effective pin-hole plugging effect. It was also proven that the device parameters can be improved even with the non-heat-treated ZnTe layers. From the industrial point of view, this finding is beneficial in order to save time and money in the production process of solar panels.

More importantly, this chapter shows that electrodeposition is a powerful growth technique in research and development of thin film solar cells. All the important layers (window, absorber and pin-hole plugging layers) can be deposited electrochemically. In addition to that, this technique is cost effective and at the same time capable of producing high quality semiconductors.

10.6 References

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11.1 Conclusion

This thesis has presented the relevant works associated with the research and development of low-cost high efficiency CdS/CdTe thin film solar cells. To obtain the low-cost materials, all of the semiconducting layers (CdS, CdTe, and ZnTe) were electrochemically grown in aqueous solutions utilizing 2-electrode system. For attaining high efficiency, the fabrications of n-CdS/n-CdTe plus Schottky contact instead of n-CdS/p-CdTe plus ohmic contact were implemented in this research project.

Experimental chapters are presented in Chapter 6 to 10. Chapter 6 to 8 has presented the experimental results of development of semiconducting layers. In these three chapters, several material characterization techniques were utilized in order to determine the optimized deposition windows. When the optimized deposition windows were determined, all of the semiconducting layers were electrochemically deposited and the followed by the fabrication of n-CdS/n-CdTe solar cells.

Chapter 9 has focused on the fabrications and assessments of n-CdS/n-CdTe solar cells. The highest efficiency reported in this thesis is 10.1% while the highest V_{oc}, J_{sc} and FF is 750 mV, 39.3 mAcm^{-2} and 0.48 respectively. Reproducibility of double-digit efficiency devices was unsuccessful due to the low value of fill factors. As shown in Table 9.10, devices with efficiency 7% and above showed reasonably high V_{oc} (above 570 mV) and J_{sc} (above 34 mAcm^{-2}). However these devices showed low values of fill factor (less than 0.47). Further analysis has revealed that the low fill factors were caused by the high series resistance and low shunt resistance. High resistivity of by CdS layers, the usage of FTO instead of FTO and the presence of oxide layers between back metal contacts and CdTe layers are the factors that could lead to the high series resistance. While the presence of pinholes in CdS or CdTe or both layers is the cause of the low shunt resistance.

. As presented in section 9.3.1, the grains of CdTe layers grew larger after the inclusion of fluorine. As a result, $CdCl_2$ + CdF_2 has proven to be more effective than $CdCl_2$ chemical treatment in enhancing the efficiency of the CdS/CdTe solar cells.

Lowering the heat treatment temperature (below 450°C) for CdTe layers has positive effect of improving the fill factor but with the expense of V_{oc} and J_{sc}. Therefore,

an alternative way to improve the fill factors of electrodeposited CdS/CdTe was presented in Chapter 10.

Chapter 10 has presented that, relatively, the inclusion of thin (~9 to 14 nm) electrodeposited ZnTe layers between CdTe and back metal contact can enhance the fill factor values of CdS/CdTe solar cells. The V_{oc} and J_{sc} have also improved after the inclusion of ZnTe layers. More importantly, this chapter has shown that the improvement of these three parameters is reproducible by utilizing electrodeposition technique.

11.2 Suggestions for future work

Improving the V_{oc}, J_{sc} and FF through the incorporation of PPL is a credible solution in research and development of CdS/CdTe thin film solar cells. It is because this method is fast and also low cost. In addition, the improvement of all parameters through electrodeposition of ZnTe was proven reproducible.

The major hurdle encounter during this research project is the reproducibility of double digit efficiency devices (≥10%). If this problem remains unsolved, the scaling up project will be impossible to implement. In order to improve the probability of reproducing highly efficient devices, few suggestions are proposed below.

11.2.1 Preparation of electrolytes using high purity chemicals

In this research project, purity of chemicals used to prepare the deposition electrolytes was between 98 to 99%. This decision was taken because this project was focused on development of low cost CdS/CdTe thin film solar cells. High purity chemicals are normally very expensive. However, if necessary, the high purity chemicals (99.99% or higher) can be tried. The reason is, the self-purification process might not be so effective in removing all the impurities contained in low purity chemicals thus will negatively affect the efficiency of solar cells.

It is important to note that majority of highly efficient CdS/CdTe solar cell devices (>15%) were fabricated with close space sublimated CdTe (CSS-CdTe) [1-4]. In CSS, high purity CdTe source material (5N to 6N) is normally used to deposit the semiconducting layers [3-5].

11.2.2 Effective tellurium addition

In this work, Te addition was carried out at regular intervals with the continuous monitoring of deposition current density. Deposition current density for electrodeposition of CdTe was maintained between 130 to 200 μAcm^{-2}. If deposition current density dropped below 130 μAcm^{-2}, about 1 ml of diluted TeO_2 was added in the bath and no tellurium addition if it is higher than 200 μAcm^{-2}.

Researchers such as Das and Morris injected Te ions ($HTeO_2^+$) from 5N purity tellurium rod in electrodeposition of CdTe [6]. They also have several publications reporting high efficiency (≥10%) solar cells [7-9], which mean their Te addition technique is effective in improving the reproducibility of highly efficient solar cells. This method of Te addition perhaps can be tried in the future.

11.2.3 Maintaining the effective concentration of Cd^{2+} ions in the bath

Since the research and development of CdS/CdTe solar cells involve frequent repetitions of CdTe electrodeposition, maintaining the Cd^{2+} ions within the correct interval or margin is proven difficult to do. Gradually overtime, the colour of $CdSO_4$ electrolyte will change from crystal clear to light yellow perhaps due to the leaching of sulphur from CdS layers into the bath. In addition, the concentration of Cd^{2+} ions will be low gradually while at the same time SO_4^{2-} ions will be high. Cd^{2+} ions are getting low because they react with Te atoms to produce CdTe [10] thus leaving excess SO_4^{2-} ions in the bath. As a result, CdTe layers produced in SO_4^{2-} ions-rich electrolyte are poor quality semiconductors and not suitable for fabrication of thin film solar cells. Solar cells fabricated from these layers always produce low efficiency devices.

Replenishing Cd^{2+} ions with the addition of new $CdSO_4$ will not produce positive result because at the same time, SO_4^{2-} ions are also added into the bath and this action is not helpful. Replenishing Cd^{2+} ions with the addition of high purity (99.99%) Cd powder is the most appropriate solution because it will not increase the concentration of SO_4^{2-} ions in the bath.

11.2.4 Reducing the resistivity of electrodeposited CdS

The discussion about high resistivity of CdS has been presented in Chapter 6 and 9. High resistivity of electrodeposited CdS layers contributes to the high series resistance of CdS/CdTe solar cells. Conducting $CdCl_2$ treatment on electrodeposited CdS layers helps to reduce the resistivity. However, the resistivity of the layers is the region of $\sim 10^4$ Ωcm, which can be considered very high. Annealing in vacuum or H_2 environment as suggested by Uda *et al* and Yamaguchi *et al* respectively, is an experiment worth trying in order to reduce the resistivity of CdS layers [11-12].

11.2.5 Substituting fluorine doped tin oxide (FTO) with indium doped tin oxide (ITO)

The front contact FTO is also a contributor to the high series resistance. Scientific report by Das [8] has concluded that the best front contact for CdS/CdTe thin film solar cells is the ITO. So, it is neccessary to replace the FTO with the lower resistivity front contact materials. However, the high cost of ITO and scarcity of indium are the main hurdles in using these layers.

11.2.6 Lifetime studies of PPL

Since the ZnTe layers have been proven to improve all three parameters of CdS/CdTe solar cells, it is appropriate to monitor the stability of these improvements over a period of time. In addition to that, organic materials such as poly-aniline (PANI) should also be electrodeposited on top of CdTe as PPL. As a start, cathodic deposition of PANI for 3 minutes can be tried.

At the later stage, comparative study can be carried out to see which devices are more stable in the long term between CdS/CdTe, CdS/CdTe/ZnTe and CdS/CdTe/PANI solar cells.

11.2.7 Graded bandgap solar cell structure

Since a large number of semiconductors (over 10 at the present) have been developed at Sheffield Hallam University Solar Energy Group (SHUSEG), graded

bandgap solar cell structure should be developed within the group. GaAs/AlGaAs graded bandgap solar cell has been reported by Dharmadasa in 2005 [13]. This device has shown promising results by producing V_{oc} ~1200 mV and FF ~0.90 [14]. However, the device was developed using an expensive growth technique, MOCVD. Therefore, in the future, development of low-cost graded bandgap solar cell utilizing electrodeposited semiconductors should be explored within SHUSEG.

11.2.8 Incident photon to current efficiency (IPCE) or responsivity measurement

In the future, it is more approporiate if the observation of high J_{sc} (> 27 $mAcm^{-2}$) in CdS/CdTe solar cell is supported with incident photon to current efficiency (IPCE) or responsivity measurement. These measurement techniques are useful in order to validate the absorption of low energy photons in the infra-red region [15].

11.3 References

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