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## Electrical Characterisation of Defects in Wide Bandgap Semiconductors

**Osama S. Elsherif** 

A thesis submitted in partial fulfilment of the requirements of Sheffield Hallam University for the degree of Doctor of Philosophy

June 2012

## **Declaration**

I hereby declare that the work described in this thesis is my own work and it has not been submitted for any other degree.

I

Osama Elsherif

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## **Dedication**

I always remember when I used to come home late after a long day in the laboratory and my beloved sons, Omar & Mohammed, were still waiting to tell me "We Miss You Dad ..!"

To them I dedicate this work

Osama Elsherif

### **List of Publications**

#### **Publications:**

- O. Elsherif, K.D. Vernon-Parry, I.M. Dharmadasa, J.H. Evans-Freeman, R.J. Airey, M.J. Kappers, C.J. Humphreys, <u>Characterization of defects in Mg doped</u> <u>GaN epitaxial layers using conductance measurements</u>, *Thin Solid Films*, 520 (2012) 3064-3070.
- O. Elsherif, K.D. Vernon-Parry, J.H. Evans-Freeman, P.W. May, "<u>Effect of doping on electronic states in B-doped polycrystalline CVD diamond films</u>", Semiconductor Science and Technology 27 (2012) 065019.
- O. Elsherif, K.D. Vernon-Parry, J.H. Evans-Freeman, R.J. Airey, M. Kappers, C.J. Humphreys, <u>Characterisation of defects in p-GaN by admittance spectros-</u> <u>copy</u>, *Physica B* 407 (2012) 2960–2963.
- 4) **O. Elsherif**, K.D. Vernon-Parry, J.H. Evans-Freeman, P.W. May, "<u>Electrical</u> <u>Characterisation of Defects in Polycrystalline B-Doped Diamond Films</u>", *Materials Science Forum* **717-720** (2012) 1315-1318.
- 5) I.M. Dharmadasa, O. Elsherif, G.J. Tolan, "Experimental Evidence for Impurity Photovoltaic Effect in GaAs/AlGaAs Based Graded Bandgap Multi-Layer Solar Cells", Proceedings of 25<sup>th</sup> European Photovoltaic Solar Energy Conference/ 5<sup>th</sup> World Conference on Photovoltaic Energy Conversion, (2010), Pages 583-586. (Outside the scope of this thesis).
- 6) I.M. Dharmadasa, O. Elsherif, G.J. Tolan, "<u>Solar Cells Active in Complete</u> <u>Darkness</u>", Journal of Physics: Conference Series 286 (2011) 012041. (Outside the scope of this thesis).

#### **Conference Presentations:**

 O. Elsherif, J.H. Evans-Freeman, K.D. Vernon-Parry, N. Mitromara and P.W. May, "High Resolution Deep Level Transient Spectroscopy of *p*-type polycrystalline diamond on p-type silicon", 25th International Conference on Defects in Semiconductors (ICDS-25), 20–24 July, 2009, St. Petersburg, Russia.

- O. Elsherif, K.D. Vernon-Parry, J.H. Evans-Freeman, I.M. Dharmadasa, R.J. Airey, M.J. Kappers and C.J. Humphreys, "Thermal activation energies of Mg in GaN:Mg on HT- AlN/sapphire characterized by admittance spectroscopy", *UK Semiconductors 2010: Conference*, 7–8 July 2010, Sheffield, UK.
- O. Elsherif, K.D. Vernon-Parry, J.H. Evans-Freeman, R.J. Airey, M.J. Kappers and C.J. Humphreys, "Admittance spectroscopy characterisation of Mg in GaN:Mg on HT AlN/sapphire", *Defects in Semiconductors: Gordon Research conferences*, 8–13 August, 2010, New London, NH, USA.
- 4) I.M. Dharmadasa, O. Elsherif, G.J. Tolan, "Solar Cells Active in Complete Darkness", Condensed Matter and Materials Physics Conference (CMMP10), 14–16 Dec 2010, Warwick, UK.
- 5) I.M. Dharmadasa, O. Elsherif, G.J. Tolan, "Experimental Evidence for Impurity Photovoltaic Effect in GaAs/AlGaAs Based Graded Bandgap Multi-Layer Solar Cells", 25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion, 6–10 September 2010, Valencia, Spain.
- 6) I.M. Dharmadasa, O. Elsherif, G.J. Tolan, "Effective harvesting of photons for improvement of solar energy conversion efficiency", Perspectives on Materials and Technologies for Photovoltaics: One-Day Workshop, organised by the Materials & Characterisation Group of the UK Institute of Physics, 30 June 2011, Manchester, UK.
- I.M. Dharmadasa, O. Elsherif, G.J. Tolan, G. Hill and J.S. Roberts, "PV solar cells active in complete darkness", UK Semiconductors 2011: Conference, 6–7 July 2011, Sheffield, UK.
- 8) **O. Elsherif**, K.D. Vernon-Parry, J.H. Evans-Freeman, R.J. Airey, M.J. Kappers and C. J. Humphreys, "Characterisation of Defects in *p*-GaN by Admittance Spectroscopy", 26th International Conference on Defects in Semiconductors (ICDS-26), 18–22 July 2011, Nelson, New Zealand.
- 9) O. Elsherif, K.D. Vernon-Parry, J.H. Evans-Freeman, I.M. Dharmadasa and P.W. May, "Electrical characterisation of defects in polycrystalline B-doped diamond films", Silicon Carbide and Related Materials - International Conf. (ICSCRM 2011), 11–16 September 2011, Cleveland, Ohio, USA.

10) B.O. Ayomanor, O. Elsherif, K.D. Vernon-Parry, A.D. Onojah, and M. Murray, "Characterization of Crystalline Metallurgical-Grade Silicon prepared from Rice Husk Ash ", UK Semiconductors 2012: Conference, 4–5 July 2012, Sheffield, UK.

#### Abstract

Defects usually have a very large influence on the semiconductor material properties and hence on fabricated electronic devices. The nature and properties of defects in semiconducting materials can be investigated by applying electrical characterization techniques such as thermal admittance spectroscopy (TAS), deep level transient spectroscopy (DLTS) and high resolution Laplace-DLTS measurements. This dissertation presents the electrical characterisation of two different wide bandgap semiconducting materials (polycrystalline diamond and GaN) which have both recently attracted a great deal of attention because of their potential applications in the fields of power electronics and optoelectronics. Raman spectroscopy, *I-V* and *C-V* measurements were carried out as supporting experiments for the above investigations.

The first part of this work focuses on studying the effect of B concentration on the electronic states in polycrystalline diamond thin films grown on silicon by the hot filament chemical vapour deposition method. A combination of high-resolution LDLTS and direct-capture cross-section measurements was used to investigate whether the deep electronic states present in the layers originated from point or extended defects. There was good agreement between data on deep electronic levels obtained from DLTS and TAS experiments. A number of hole traps have been detected; the majority of these levels show an unusual dependence of the DLTS signal on the fill pulse duration which is interpreted as possibly the levels are part of extended defects within the grain boundaries. In contrast, a defect level found in a more highly doped film, with an activation energy of ~0.37 eV, exhibited behaviour characteristic of an isolated point defect, which we attribute to B-related centres in the bulk diamond, away from the dislocations.

The second part of this thesis presents electrical measurements carried out at temperatures up to 450 K in order to study the electronic states associated with Mg in Mg-doped GaN films grown on sapphire by metalorganic vapour phase epitaxy, and to determine how these are affected by the threading dislocation density (TDD). Two different buffer layer schemes between the film and the sapphire substrate were used, giving rise to different TDDs in the GaN. Admittance spectroscopy of the films finds a single impurity-related acceptor level. It is observed in these experiments that admittance spectroscopy detects no traps that can be attributed to extended defects, despite the fact that the dislocations are well-known to be active recombination centres. This unexpected finding is discussed in detail.

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#### **1. Introduction**

#### 1.1 Overview

In 1952, Hall presented the first germanium based power device with the highest breakdown voltage and switching capabilities [1], and since that time the semiconductor industry has been continuously developing. Germanium was the preferred semiconductor material until the end of the 1950's when silicon started to replace germanium, having superior electrical properties and offering the best native oxide (SiO<sub>2</sub>) among all known semiconductors. The ability to form a thin native oxide layer was one of the primary factors which led silicon to becoming the most preferred semiconductor. This layer can serve as an electrical insulator, a barrier material during implantation/diffusion, as an important layer in the MOS device structures, or as an interlayer dielectric in multichip modules.

For many decades, semiconducting silicon has dominated the electronics industry; it has been widely studied and understood, also techniques have been developed to control and enhance its features. Nowadays, the vast majority of the fabricated semiconductor devices require the implementation of silicon. Remarkable technological achievements include high frequency operations, the fabrication of silicon based power devices, and MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). Silicon nanostructures are an increasingly important component of many devices. MOSFETs suffer from significant limitations due to the high on-state resistance induced by the increase in the off-state performance, giving rise to overall losses [2]. In addition, due to its small bandgap (1.12 eV), low carrier mobility and relatively poor thermal conductivity, silicon may have reached its maximum potential and therefore be incapable of meeting the increasing demands of the electronics industry. These limitations are indicative that different materials are necessary for future generations of electronic devices, particularly for power electronics, RF, optoelectronics and lasers that cover a wider range of the electromagnetic spectrum.

Wide bandgap (WBG) materials have recently attracted a great deal of attention because of their applications in efficient light-emitting devices (LEDs) and potential for use in high-power, high voltage, high-temperature and high-frequency electronic operations. Silicon carbide (SiC), gallium nitride (GaN), and diamond are amongst the WBG semiconductors that have already started to be investigated for power and optical applications [3-5]. However, these materials have to be thoroughly investigated, bottlenecks in the development and fabrication of the desired electronic devices have to be solved, and much work is required in order to develop the necessary techniques to control the properties of these semiconducting materials. Furthermore, the ever growing requirements for downscaling of device dimensions gives rise to complicated physical phenomena. As scaling increases, the presence of defects in the semiconductor becomes increasingly detrimental to the device performance and a vast amount of research has been performed to identify and eliminate them or control their behaviour. In addition to the study of defects, investigation of novel semiconducting materials has increased during the last few decades in order to provide an alternative that can have sufficiently good properties to one day replace the silicon technology. A wide range of experimental techniques have been developed to ensure adequate information about the properties of these defects can be obtained and is subsequently used in order to produce more efficient devices.

The present work investigates the electrical properties of two WBG materials: GaN and semiconducting diamond. Electrical characterisation of defects was performed using suitable techniques for this purpose, namely high resolution Laplace Deep Level Transient Spectroscopy (LDLTS) and Thermal Admittance Spectroscopy (TAS).

#### **1.2** Aim and motivation of this work

In this research the existence of deep traps is investigated in two different semiconductor systems; B-doped polycrystalline diamond and Mg doped GaN epitaxial layers. These materials have huge potential for different applications, as briefly discussed next.

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The first aim of this work was to determine the effect of B concentration on the electronic states in polycrystalline diamond thin films grown on silicon by the HF-CVD (hot filament chemical vapour deposition) method. The second was to study the electronic states associated with Mg doping in GaN films grown by MOVPE (metalorganic vapour phase epitaxy) on sapphire substrates, and to determine how these are affected by differing threading dislocation densities (TDDs).

The main focus of this research is to investigate the electrical properties of defects in both semiconductors, as the processes that occur at deep levels within the bangap of either of the mentioned materials can limit the performance and service lifetime of devices made from them. Despite many years of diamond research, little is known about native and extrinsic defects in CVD polycrystalline diamond films. The work reported in the first part of this thesis is aimed to help understanding B-related defects in CVD diamond grown on silicon substrates, also enhance scientific knowledge and assist in the future study and implementation of similar structures. The second part of this thesis is aimed to provide useful information about the interaction of Mg dopants with TDDs in GaN. The interaction of p-type dopants in GaN and the high level of dislocation density in the material (due to the lack of available lattice matched substrates) are key bottlenecks in the development of GaN-based devices. Some of the defect states are nonradiative recombination centres and cannot be observed by optical techniques. The application of sensitive electrical characterisation tools such as admittance spectroscopy and high resolution Laplace DLTS has enabled the extraction of new interesting data on the defect states found in these materials.

#### **1.3** Properties of specific wide bandgap materials: GaN and diamond

The predicted physical properties of WBG semiconductors such as SiC, GaN and diamond indicate that those materials have outstanding electrical properties and could introduce disruptive technology in to the semiconductor industry and eventually replace silicon technology. Table 1.1 compares some of the physical characteristics of these semiconductors to Si and gallium arsenide (GaAs).

Knowledge of crystal structure and lattice constant values are important in determining some of the crystal's physical and electrical properties. Semiconductor materials such as silicon and diamond have cubic structure, whereas compound semiconductors such as GaAs and GaN can have more than one crystal structure; can be either cubic or hexagonal (wurzite). SiC can be cubic or one of several different hexagonal crystal structures. The cubic crystals are characterized only by the lattice constant parameter (a), while the hexagonal structures are characterized in the hexagonal plane by a lattice constant and by the distance between the hexagonal planes (c), as tabulated in Table 1.1.

Property	Si	GaAs	6H-SiC*	4H-SiC*	GaN	Diamond
Bandgap (eV)	1.12	1.43	3.03	3.26	3.45	5.54
Dielectric constant, <i>ɛ<sub>r</sub></i>	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field (kV cm <sup>-1</sup> )	300	400	2500	2200	2000	10000
Electron mobility ( cm <sup>2</sup> .V <sup>-1</sup> .s <sup>-1</sup> )	1400	8500	500	1000	1250	2200
Hole mobility (cm <sup>2</sup> .V <sup>-1</sup> .s <sup>-1</sup> )	450	400	101	115	850	850
Thermal conductivity (W.cm <sup>-1</sup> .K <sup>-1</sup> )	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity (×10 <sup>7</sup> cm.s <sup>-1</sup> )	1	1	2	2	2.2	2.7
Crystal structure	Cubic	Cubic	Wurtzite	Wurtzite	Wurtzite	Cubic
Lattice Constant at 300 K (Å)	5.43	5.65	a=3.08 c=15.11	a=3.08 c=15.11	a=3.189 c=5.185	3.56

Table 1.1 Physical properties of different semiconductors [6].

<sup>\*</sup> 6H-SiC and 4H-SiC are Silicon Carbide polytypes. 4H-SiC wafers exhibit higher mobilities.

One of the major limitations of Si is higher temperature operation, since at room temperature the intrinsic carrier concentration of Si is about  $10^{10}$  cm<sup>-3</sup>, and it rapidly

increases with increasing temperature. It is the most temperature-dependent of the above mentioned materials due to its small bandgap. At elevated temperatures (>150°C) Si based devices will tend to behave more as an intrinsic semiconductor, and the designed doping will have no effect on the properties of the material as the Fermi level will be at a comparable position in the bandgap to the intrinsic level. In contrast, WBG materials such as diamond have extremely low intrinsic carrier concentrations even at high temperatures, hence should be able to maintain their electrical properties, preventing device failure. This makes diamond a better choice for devices to be used in high-power systems, transportation, defence, and space applications.

Another important aspect of device operation is the leakage current of rectifying contacts; for example, in Schottky contacts the current transport mechanism depends on the barrier height at the metal-semiconductor interface. The barrier height is partially related to the bandgap of the material, and its value can be as high as three quarters of the bandgap depending on the work function of the metal used. For WBG semiconductors the barrier height is high, which limits the thermionic emission related leakage currents. Table 1.1 illustrates that GaN and diamond have higher carrier mobility than Si, however at elevated temperatures mobility decreases due to phonon scattering, reducing the current through the device, therefore materials with higher mobilities may be more suitable for higher temperature applications. The carrier mobility is directly proportional to the drift velocity of carriers; as in principle the carriers in a semiconductor will move under the influence of a small electric field, with a drift velocity in addition to their thermal velocity. However, as the electric field becomes larger, the drift velocity increases less rapidly and finally approaches a saturation drift velocity [6]. In WBG semiconductors, saturated drift velocities are more than twice as large as that of silicon. Therefore, WBG materials are expected to yield higher frequency switching capabilities than silicon based devices, because the saturated drift velocity of a semiconductor material is directly proportional to the high-frequency switching capability.

WBG semiconductors have higher electric breakdown field than Si or GaAs, which is required for manufacturing of devices with high breakdown voltages, and hence can be

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useful for the fabrication of MOSFETs and Schottky diodes with high voltage rating. Also higher doping densities can be used, which entails that the drift region of power devices can be made thinner and with lower resistance.

#### 1.4 Applications of GaN

Because of the unique material properties, as discussed above, GaN-based devices are promising not only as high-speed devices, but also as high-temperature and high-voltage devices suitable for operating in chemically hostile environments. Furthermore, group III nitride materials, including GaN, indium nitride (InN), and aluminum nitride (AlN) have attracted a great deal of attention because of their wide applicability to optoelectronic devices such as LEDs. Figure 1.1 illustrates that GaN-based material systems can be tuned to cover a wide range of wavelengths, from red to UV (650 to 200 nm) by alloying with AlN and InN.



Figure 1.1 Bandgap vs. lattice constant of III-Nitride semiconductors [7]



Figure 1.2 Applications of GaN-based semiconductors [9]

Ongoing technological developments have resulted in crack-free GaN surfaces, the discovery of a p-type dopant for GaN and eventually the fabrication of p-n homojunction green and blue LEDs. This has now opened up new opportunities for general white light illumination systems [8], as introducing blue LEDs fills the missing element of RGB (red-green-blue) primary colours. Figure 1.2 shows a wide range of applications for devices fabricated from GaN or III-nitride compounds, encompassing violet laser diodes, UV detectors, and High Electron Mobility Transistors (HEMTs) which are the next generation of RF power transistor technology that offers the unique combination of higher power, higher efficiency and wide bandwidth.

Nowadays, GaN-based violet laser diodes (emitting 405 nm radiation) are used to read the Blu-ray Discs which can hold about five times the amount of information that can be stored on a DVD. GaN also has great potential as a spintronics material when doped with a suitable transition metal such as manganese.

#### **1.5** Applications of semiconducting diamond

Even though diamond still in its infancy as a semiconductor material; diamond devices have been made and tested [10]. Devices include: p-n diodes, UV emitting p-n diodes, p-i-n diodes, various types of radiation detectors, high voltage Schottky diodes and photoconductive or electron beam triggered switches. Also there has been a large focus on the development of diamond devices for RF applications; this is driven by experimental efforts [11-14] in investigating unipolar devices, such as MISFETs (metalinsulator-semiconductor field effect transistor), MESFETs (metal epitaxial semiconductor field effect transistor) and JFETs (junction field effect transistor).

Only H-diamond has a stable negative electron affinity surface; the bulk conduction band lies above the vacuum level, and hence conduction band electrons are readily emitted. This has attracted interest in investigating the possibility of constructing a negative electron affinity diamond vacuum collector transistor which is expected to have exceptional high frequency and temperature operation capabilities.

Diamond is transparent from ultraviolet to far infrared (225 nm to ~100  $\mu$ m) wavelengths, except for an absorption band resulting from two phonon absorption between 2.5-6.5  $\mu$ m, as shown in Figure 1.3. This makes diamond an ideal material for multispectral optical applications. It is known that only multiphonon processes can lead to absorption. Diamond contains only a single type of atom, hence there is no electric dipole coupling between photons and phonons; however, impurity atoms will allow these electric dipoles to form.



Figure 1.3 Optical transparency of CVD diamond in the UV, Visible, IR and far IR [15].

Pure diamond remains transparent even at elevated temperatures and radiation intensities because the large bandgap (5.45 eV) prevents thermal generation of charge carriers across the bandgap even at high temperatures. Experimental reports [16] show that a natural diamond window survived a 1 s exposure to a focused 1 kW laser beam with a peak irradiance of 1MW cm<sup>-2</sup>. The diamond window was unaffected by the exposure.

Diamond can be used for coating soft IR optics with a high index coating to serve as an anti-reflective as well as a protective coating. Therefore, diamond's extreme thermal conductivity, hardness, and chemical resistance (extremely chemically inert) are of importance for various optical applications.

#### **1.6** Thesis outline

Chapter 2 provides an overview of defects, their types and effect on the properties of semiconducting materials. It also briefly discusses doping of wide bandgap semiconductors. Finally, reviews of defects in CVD diamond and *p*-GaN are provided.

Chapter 3 describes the growth techniques used in this work to grow thin films of CVD diamond and p-GaN. The chapter discusses the importance of CVD growth techniques, problems associated with these methods, and the current technological developments to improve the CVD processes.

Chapter 4 describes the theory of the depletion region, p-n junction, the structure and operation of Schottky diodes and focuses on the theory of electrical characterisation methods for characterising devices. These include *C*-*V*, *I*-*V*, DLTS, the high resolution Laplace DLTS, and Thermal Admittance Spectroscopy.

Chapter 5 presents the experimental setup used for the electrical characterisation of all diodes in this project. Details of the hardware and software for each technique are provided.

Chapter 6 provides details about the growth, surface characterisation, and device processing and fabrication of the Schottky diodes on both the CVD diamond and p-GaN films.

Chapter 7 describes and discusses the results obtained from the electrical characterisation of defects in Schottky structures of CVD diamond grown on silicon.

Chapter 8 describes and discusses the results obtained from the electrical characterisation of defects in Schottky structures of *p*-GaN grown on sapphire.

Chapter 9 summarizes the results and provides conclusions about the defects investigated in the two wide bandgap materials in this work. Finally, based on these results, some suggestions for future work are presented.

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#### 2. Defects in GaN and semiconducting diamond

#### 2.1 Overview of defects

What defines semiconductors is that they have a bandgap that separates the highest fully occupied valence bands from the lowest unoccupied conduction bands. Pure semiconductors are useless in many electronic applications unless they contain specific atomic impurities (dopants) whereby the electrical properties of semiconductors can be controlled. Dopants may be introduced during growth or post-growth. Post-growth doping can be typically controlled by the use of photolithography on selected areas and subsequently doped further by techniques such as diffusion [1] and ion implantation [2]. The functionality of all modern electrical devices is based on doped semiconductors; the incorporation of dopant atoms can change the ability of a semiconductor to conduct electricity, rendering the material n-type or p-type.

Basically, anything that alters the ideal crystal structure of a semiconductor will, in fact, affect its optical and/or electronic properties. These distortions are called *defects*. Defects can have a very large influence on the material properties; for example, resistivity of the material, carrier mobility and lifetime, and its optical properties are all dependant on the precise defects present and their concentrations. They introduce energy states in the forbidden gap of a semiconductor. Defects may be classed as line defects, planar defects, bulk defects or point defects. The first three can be avoided when growing some semiconductor crystals; vacancies and self-interstitials (both point defects) will always occur in solids at thermal equilibrium. Dopant species may be present either as interstitial or as substitutional point defects. Figure 2.1 and Figure 2.2 illustrate some examples for typical point and extended defects in semiconductors.

**Point defects** can be classified into intrinsic defects (native defects), formed only from the host atom types, and extrinsic defects (impurities) consisting of foreign atoms. Deviations from the perfect crystalline periodicity of the solid constitute point defects. These can be missing atoms (vacancies), atoms at the wrong lattice site (antisite/ substitutional defects) [3-4], atoms in between the ordinary lattice sites (interstitial defects) or complexes that form between different kinds of point defects.



**Figure 2.1** Typical point defects in semiconductors. The grey circles represent the host atoms (*e.g.*, silicon) and the black represent foreign atoms (*e.g.*, oxygen in silicon).



**Figure 2.2** Typical extended defects in semiconductors. The grey circles represent the host atoms and the black represent foreign atoms.

Line defects form when some of the atoms of the crystal lattice are misaligned (also known as *dislocations*) [5]. The termination of a plane of atoms in the middle of a crystal causes edge dislocations; adjacent planes bend around the edge of the terminating plane. Dislocations may move if the atoms from one of the surrounding planes break their bonds and re-bond with the atoms at the terminating edge. Other types of line defects can be either "screw" dislocations, in which a helical path is traced around the dislocation line, or "mixed", which is neither pure edge nor pure screw.





*Misfit dislocations* may be edge, screw or mixed in nature. Misfit describes the sort of strain that introduced the dislocation, i.e. they are caused by lattice mismatch strain introduced during epitaxial growth that subsequently relaxes to give dislocations (and reduce the strain) either as the layer gets thicker or on annealing. At the ends of any misfit dislocation there will always be two *threading dislocations*. These must thread to a surface or form a loop so that the two ends of the dislocation can join. Figure 2.3 illustrates how misfit and threading dislocations occurring in Si/SiGe heterostructures due to the silicon lattice. These threads are at 60° since they glide on the Si (111) lattice plane.

**Planar defects** can occur when the crystallographic direction of the lattice abruptly changes. This usually occurs when two crystals begin growing separately and then meet; that forms a planar defect due to discontinuity of the perfect crystal structure across a plane, i.e. grain boundaries separate regions of different crystalline orientation (*grains*) within a polycrystalline solid. They tend to decrease the electrical and thermal conductivity of a material. Planar defects can also occur when the stacking sequence of the atomic planes is interrupted by the insertion or deletion of one plane. These are most common in face-centred cubic crystal structures where the ideal stacking sequence is ABCABCABC... Stacking faults are necessarily bounded by dislocations.



**Figure 2.4** Grain Boundaries separate regions of different crystalline orientation within a polycrystalline solid [7].

Finally, **Bulk defects** are formed when impurities cluster together and form small regions of a different phase (this may also be called *Precipitate*), and if a number of vacancies coalesce then they form a *Void*.

#### 2.2 Shallow and deep defects

According to the positions of defect levels in the band gap with respect to the conduction or valence band edge, defects in semiconductors are generally placed in one of two categories: shallow-level defects or deep-level defects.

Shallow levels, acting as either donors or acceptors, contribute electrons or holes respectively and determine the conduction properties of the semiconductor. An impurity or native defect will alter the electrical properties of a semiconductor if it either acts as a donor, contributing electrons to the conduction band, or as an acceptor, creating holes in the valence band. Whether an atom acts as a donor or an acceptor is dependent on the location of the defect in the crystal lattice. For example, a group IV atom in a III-V semiconductor substituting a group III atom will only need three electrons to complete the four bonds to its closest neighbours and the last outer-shell electron will occupy the conduction band and hence act as a free charge carrier. In this case the group IV atom will act as a donor. If it is instead located on a group V lattice site, there will be one outer-shell electron site empty, which will act as an acceptor.

The same impurity atom can actually act both as an acceptor and a donor depending on the position of the Fermi level [8]. Acceptors have shallow defect levels slightly above the valence band edge and donors have shallow defect levels slightly below the conduction band edge. In this way the positions of the dopant's defect levels are of great importance for the concentration of charge carriers.

Shallow levels have small binding energy, typically 0.01 eV, and are almost fully ionized in silicon at room temperature. On the other hand, deep level defects bind the carriers more strongly and lead to highly localized states in the forbidden gap [8]. Deep

levels, which are defect levels located in the middle of the band gap, have a tendency to interfere with the optical functionality of semiconductors.



Figure 2.5 Radiative and non-radiative recombination processes.

Figure 2.5 illustrates the situation when an electron-hole pair is created as a photon of sufficiently high energy hv (higher than the bandgap) is absorbed by the material. The carriers quickly thermalize to the limits of the conduction and valence bands, the excess energy is transferred to the crystal lattice (phonon emission). The electrons and holes can radiatively recombine, giving rise to a photon emission. Also an electron from the conduction band can be captured by an empty defect in the bandgap of the semiconductor. The yield of the photon emission is governed by a competition between radiative recombination processes. For indirect bandgap materials, the radiative recombination is only possible with the assistance of momentum-conserving phonons and/or traps (trap assisted recombination process). In cases such as B-doped diamond, a single phonon emission is not sufficient to match the difference in level energies, multiple phonons are typically required for such transitions. In addition, the probability of creating photons in defective materials is very low, as the defects would quench the photoluminescence.

A high concentration of defect levels deep within the band gap can thereby lower the efficiency of optical devices considerably. If defects are studied and understood these problems may be avoided, and semiconductors could even be engineered in such a way to make native defects work in favour of the desired electric properties [9].

#### 2.3 Doping of wide bandgap semiconductors: GaN and diamond

There is a great deal of interest in overcoming obstacles associated with doping of wide bandgap materials. For example, most natural diamonds are insulators and thus doping of electrically active impurities such as boron or phosphorus is required to turn the diamonds into *p*-type or *n*-type, respectively. However, the tight bonding of carbon atoms makes incorporation of dopant species difficult. Large substitutional dopant atoms will introduce significant lattice distortion and can therefore only be incorporated substitutionally at very low concentrations. Only relatively small atoms such as B can be incorporated in solid solution at useful concentrations in order to replace carbon in vacancy sites. Doping techniques such as diffusion, used in silicon and related materials, are not possible in diamond due to the extreme strength of the C-C bond in the material.

In addition, it is necessary to ensure that doping can introduce relatively shallow acceptor or donor that can enhance conduction even at room temperature. For example, in GaN, oxygen and silicon are known to be shallow donors but still there is a problem in finding an efficient shallow acceptor for producing p-type material; magnesium and beryllium are currently used but their activation energies are higher than optimum, so that not all the acceptors are ionised at room temperature. This results in quite low conductivities at room temperature. Doping techniques such as ion implantation, which work well with silicon technology, are not successful in controlling the doping process for most wide bandgap materials. For example, Si implants can be used to convert p-type GaN into n-type, however, it has been reported that ion implantation induces lattice defects, which are hard to remove by subsequent annealing [10]. Implantation doping in diamond is problematic due to the difficulty in removing implantation damage which compensates donors [11]. Therefore, doping of wide bandgap materials is best done during growth.

In CVD grown diamond, *p*-type doping has been achieved by the introduction of B into substitutional sites, forming an acceptor level at about 0.37 eV above the valence band. In synthetic diamond, *n*-type doping with N is possibly achieved by introducing nitromethane or  $N_2$  in the precursor gas, N introduces a very deep donor level at about 1.7 eV. There have been some attempts to find a shallow donor in diamond by introduction of group I elements (Li and Na) to occupy interstitial sites in diamond and contributing to conduction with their outer electron, however, the experimental results have shown high resistivities and could not verify the theoretical computations [12]. A much shallower donor level than N has been successfully achieved by using phosphorus as a dopant, however, the donor level of P is still relatively deep (0.6 eV below the conduction band).

The search for a suitable dopant to yield shallow donor levels in diamond has motivated much theoretical modelling work [13]. Co-doping the diamond with more than one element has been considered theoretically to yield shallower levels than simple n-type doping. This is achieved by introducing a group VI element (O or S) bounded to a group III element (such as B). Another mode of obtaining *n*-type diamond by the combination of two donor atoms and a single acceptor in close proximity such as H and B will give rise to a single donor, but this may be shallower than that of an isolated single donor. This is due to the fact that energy levels of isolated impurities tend to shift at lower donor or acceptor levels when complexes are formed. Recently, *n*-type conduction has been discovered by the exposure of a B-doped diamond to a hydrogen (deuterium) plasma. The experimental results show that conversion takes place when the D/B ratio is about two. However, heating the samples at high temperatures (above 650°C) causes the original p-type conductivity to return [14]. This may be due to the break-up of the complexes responsible for the formation of the shallow donor level. Although co-doping has promised much, no satisfactory theoretical explanation for experimental findings has been given so far.

Boron is known as the most effective acceptor in diamond if it is to be used in electronic devices [15], although its acceptor level is deep by the standards of related materials; meaning that full ionisation of the dopant at room temperature is unlikely to be

achieved. The status of p-type diamond has been well documented [14], a major improvement in producing p-type diamond was achieved by the development of diamond film growth using CVD by different methods (hot filament, microwave plasmas or direct current glow discharge); either in the form of single crystal homoepitaxial layers or as polycrystalline films [16]. CVD facilitates the doping process by incorporating B substitutionally into the diamond lattice during the CVD growth by adding a boron compound (such as  $B_2H_6$ ) into the environment above the substrate. Generally, a low boron concentration converts insulating diamond to a p-type semiconductor. A gradual change from semiconducting to metallic state and then to a superconducting state is observed as the boron doping level increases from  $10^{18}$  cm<sup>-3</sup> to above  $10^{21}$  cm<sup>-3</sup> [17,18], as the band starts to overlap with the valence band. However it is also known that more than ten percent of boron atoms incorporated into diamond do not act as acceptors [19,20]. Some may be electrically inactive; it has been suggested that some boron atoms are passivated by association with other impurities such as hydrogen [20] although annealing schedules can reduce the concentration of these complexes. It is also a possibility that boron may segregate into highly defective regions of the material which could result in complexes of B with vacancies and boron interstitial defects [21,22]. In polycrystalline diamond films B may also segregate to the grain boundaries and be trapped there as inert impurities.

It has been reported [23] that hole mobility for B-doped polycrystalline diamond can be improved by increasing the grain size and that such material can exhibit much better field effect transistor (FET) properties than single-crystal material. The mechanisms underpinning these findings are still not clear; this underscores the ongoing requirement for a deeper and more thorough understanding of the physics of defects in polycrystalline diamond.

Advances in GaN doping have been limited by several factors such as the lack of a lattice-matched substrate, which implies highly defective material and the fact that the most commonly used acceptor dopant, Mg, can be easily compensated by hydrogen.
The activation energy of the Mg acceptor is quite high, reportedly in the range 120 - 250 meV [24-27]. This fact, together with the compensation of Mg by H, implies that at room temperature the ionised acceptor concentration  $(N_a^+)$  is well below the total magnesium concentration  $(N_a)$  measured by secondary ion mass spectrometry (SIMS) [28]. It is believed that the high specific resistance of the *p*-GaN layer is due to the reduction of the hole concentration with increasing Mg-doping concentration, which has been attributed to the self-compensation effect in metalorganic vapour phase epitaxy (MOVPE) grown Mg-doped GaN layers [29].

Currently the most important problems and open issues related to p-type doping in GaN remain the lack of understanding of the defects responsible for performance degradation in GaN-based devices; these still include acceptor doping and the formation of robust, reliable and well-characterised electrical contacts to p-GaN.

### 2.4 Review of defects in CVD-Diamond: beneficial and detrimental

This review will not attempt to discuss many of the defects most commonly seen in natural diamonds or n-doped diamond, as the interest for this research is limited to B-doped CVD diamond.

The use of the term "defects" implies that their presence in the material is detrimental. However, this is only true in some cases where the incorporation of dopant atoms is essential. For example, doping of diamond with boron is necessary to produce p-type material, whereas finding a suitable n-type dopant remains problematic. Other defects, such as the nitrogen-vacancy (N-V centre) in diamond, which has desirable properties by acting as a single photon-source or a quantum bit in a quantum computer [30], which has attracted a great deal of attention for potential uses in novel fields of spintronics, quantum cryptography and quantum computing. In its isolated form, nitrogen is a deep donor with an activation energy of 1.7 eV [18]. Nitrogen in CVD diamond is unlikely to be in the form of aggregates but it is commonly found as a nitrogen-vacancy complex. Diamond has gained a considerable increasing interest since the discovery that it is possible to grow polycrystalline diamond films by various chemical vapour deposition (CVD) methods using a hydrocarbon gas, e.g. methane, in an excess of hydrogen, as process gases (discussed further in section 3.2). CVD diamond has to be grown in a hydrogen-rich environment [31], the incorporation of hydrogen in CVD diamond is significant. The hydrogen atoms are known to play a number of crucial roles in the CVD process; they react with stable gas-phase hydrocarbon molecules and produce highly reactive carbon-containing radical species such as CH<sub>3</sub> which can diffuse to the substrate surface and react, forming the C-C bond necessary to propagate the diamond lattice. In addition, hydrogen terminates the CVD diamond surface, i.e. hydrogen atoms terminate the dangling C bonds on the diamond surface and prevent them from cross-linking, thereby reconstructing to a graphite-like surface.

It is well documented that CVD diamond surfaces exhibit negative electron affinity [32-35], i.e. the vacuum level lies below the bottom of the conduction band. In this case electrons have no potential barrier for their escape to vacuum, i.e. they are free to leave the surface. H removal from the diamond surface results in reconstruction of the surface and hence leads to the restoration of a positive electron affinity. Cui et al [32] have reported that the lowering of the electron affinity in CVD diamond to a value of -1.3 eV was due to the presence of hydrogen on the diamond surface, hence allowing cold electron emission from a hydrogen-terminated diamond surface. It has been shown by Takeuchi et al. [35] that the observed photoelectron emission in an intrinsic B-doped diamond films (hydrogenated diamond surfaces) is attributed to direct photo-excitation from the valence band to the vacuum and does not depend on the position of the Fermi level. The electron affinity in that work was found to be -1.1 eV. Maier et al. [36], using Hall effect measurements, have provided experimental evidence of high surface conductivity in H-terminated diamond surface immediately after growth due to their exposure to atomic hydrogen in the gas-phase. This conductive layer was postulated to be due hydrogen-related acceptors with a very low activation energy (~50 meV), a RT surface carrier concentration of about  $10^{13}$  cm<sup>-2</sup> and hole mobilities of ~70 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>. This low resistive layer disappeared upon heating at 200°C. The negative electron affinity of the H-terminated diamond surface facilitates all electron emission processes such as thermionic emission, emission of secondary electrons induced by photons, by electrons, by ions and by an external electric field [33].

However, the presence of hydrogen in the bulk of the crystal is less understood as compared with surface hydrogen. Hydrogen is known to passivate dopants in diamond [20,35]. As a result of such passivation, shallow donor centers are formed [38]. After growth, the diamond films are usually contaminated with hydrogen; lattice vacancies such as hydrogen-vacancy [39] and hydrogen-nitrogen-vacancy [40] complexes have been observed experimentally in negative charge states. It has also been shown that hydrogen can increase diamond film surface conductivity, and mobile H diffuses to form complex pairs with B in p-type diamond and passivate the electrically active defects [38]. Hence the electrically active B content appears reduced, although annealing schedules can reduce the concentration of these complexes. It is also a possibility that boron may segregate into highly defective regions of the material which could result in complexes of B with vacancies and boron interstitial defects [21, 22]. The BH and BH<sub>2</sub> complexes in B-doped diamond have been theoretically investigated [41]; the associated acceptor levels were predicted to be E<sub>v</sub>+4.44 eV and E<sub>v</sub>+1.14 eV, respectively. The associated donor levels were found to be  $E_c$ -4.84 eV and  $E_c$ -2.80 eV, respectively. The BH donor level at  $E_c$ -4.84 eV (corresponding to  $E_v$ +0.6 eV) is found to be at the same energy level as the donor level of the vacancy [42]. These are in good agreement with recent results measured by isothermal transient spectroscopy [43]. The atomic structure of the complex defect BH<sub>3</sub> is less understood, it is predicted to form a donor level at  $E_v$ +0.20 eV [44]. Recently, it has been reported [43, 45] that in B-doped diamond hole traps with ionisation energies between 0.7-1.6 eV are most likely due to hydrogen related defects.

One of the major problems with polycrystalline diamond films is a tendency to contain high defect densities due to their non-homogeneous structure and abundance of grain boundaries. Grain boundaries invariably contain a high density of lattice defects such as defect clusters and dislocations. In polycrystalline diamond films B may also segregate to the grain boundaries and be trapped there as inert impurities. Monocrystalline diamond does not have these problems but large-scale production is still thought to be largely impracticable due to growth requirements and fairly low growth rates of high pressure-high temperature (HPHT) diamond which limits the monocrystal size to volumes of about 1 cm<sup>3</sup>. Therefore, heteroepitaxial CVD of polycrystalline diamond films on Si substrates remains the industrial growth method of choice for many devices. High quality polycrystalline diamond films have recently been reported [31,46], with grains range in size from micrometres to less than 5 nm.

It is known that B in diamond forms an acceptor level at about 0.37 eV, however, it has been confirmed that the activation energy of the B acceptor level changes with B content in the diamond films [12, 18, 46-50]. As the B doping increases the activation energy of the acceptor decreases, due to broadening of the defect band while the effect of grain boundaries becomes weaker [50]. In polycrystalline diamond the areal density of the grain boundaries decreases as the layer gets thicker. There has been clear experimental evidences showing the columnar nature of the polycrystalline diamond growth up from the surface of the silicon substrate using different CVD growth methods.



**Figure 2.6** Secondary electron micrograph of a cross-section through a 6.7  $\mu$ m-thick diamond film on Si grown by HF-CVD, showing the columnar nature of the growth up from the surface. [51]



**Figure 2.7** Secondary electron micrograph of a cross-section through a 4 μm diamond film on Si grown by MWP-CVD [52].

Figure 2.6 and Figure 2.7 show cross-sections through microcrystalline diamond films, grown on silicon by different groups, showing the growth to be essentially columnar.

Although the grain boundaries are usually mechanically quite strong, there are discontinuities in the structure which affect the bulk properties. The boundaries between the crystals are imperfect due to misalignment of adjacent grains, e.g. stacking faults, dislocations, and because they may contain impurities or non-diamond carbon.

Isolated vacancy defects in boron-doped single-crystal diamonds behave as deep electron donors/acceptors; their electronic properties depend on the charge state. For example, the +/0 state is at  $E_v$  +0.6 eV and the energy level for the 0/- state is at  $E_c$  -2.5 eV [53]. Experimental studies, based on monitoring the changes induced by electron irradiation in the optical absorption features associated with these centres in a number of natural and synthetic diamonds, have revealed a series of sharp lines called GR1-8, of which the GR1 line (zero-phonon line at 1.673 eV, due to neutral vacancies V<sup>0</sup>), at 741 nm is the most prominent and important [54].

B interacts with carbon interstitials creating a neutral boron–interstitial complex with a sharp optical absorption at 2250 nm (0.552 eV) [53]. To the best of my knowledge, no evidence is known so far for boron-vacancy complexes [55].

Silicon has been identified as a common defect in diamond films grown by CVD; it originates from the silicon substrate or from the walls of the CVD reactor. Silicon reacts with vacancies in the diamond; the substitutional silicon traps a migrating vacancy creating a Si-vacancy complex (semi-divacancy) [56]. This trap is a deep donor having an activation energy of 2 eV, situated above the valence band [57]. Isolated silicon defects have been identified in diamond by the presence of a sharp optical absorption peak at 738 nm [58] and by EPR (electron paramagnetic resonance) [56].

Over the last two decades various activation energies and capture cross-sections have been reported for majority carrier traps in semiconducting diamond using capacitance transient spectroscopy techniques such as DLTS [59-71]. However, some of these data may have been misinterpreted due to the low resolution of the experimental measurements. Recently valuable information about defects in monocrystalline [43,45,63,64] and polycrystalline [65-67] diamond films have been obtained.

In boron-doped homoepitaxially grown CVD diamond, thermal and optical-DLTS have shown that there is a deeper electronic level than the boron acceptor at 1.25 eV above the valence band [68]. This trap was identified as the positively charged vacancy, and the optically induced transition between the boron and the vacancy at 0.9 eV was observed as well as the direct ionisation of the vacancy [69,70]. Using this technique, it was possible to see passivation of boron after deuteration, although there was no evidence of shallow donors. Charge-based-DLTS (Q-DLTS) has been used to detect a number of trapping levels, of which few have been identified with specific defects. One, at 0.36 eV, is clearly associated with boron and has a capture cross-section of  $1.3 \times 10^{-13}$  cm<sup>2</sup> [71]. Traps with cross-sections of  $\sim 10^{-12} - 10^{-14}$  cm<sup>2</sup> and activation energies of 1.14 eV and 1.23 eV been observed in undoped CVD diamond films using Thermally Stimulated Currents (TSC) and Photoinduced Current Transient Spectroscopy (PICTS) with concentrations around  $10^{16}$  cm<sup>-3</sup> [72], but these are not definitely identified with any defects, although the positively charged vacancy is a good candidate.

Traps with very small capture cross-section values (less than  $10^{-15}$  cm<sup>2</sup>); imply that these centres are repulsive or neutral and these capture cross-section values may be correspond to donor traps in a *p*-type material or may be extended defects. A summary of the deep levels related to boron, hydrogen, or native defects in B-doped CVD diamond is tabulated with their estimated capture cross- section values in Table 2.1.

Reference	Тгар	Energy level (eV)	capture cross- section $\sigma$ (cm <sup>2</sup> )	Experimental Method
[73,74]	Bs	$E_v + 0.3$ to 0.38	-	DLTS & Resistivity Measurements
[71]		$E_{v} + 0.36$	1.3×10 <sup>-13</sup>	Hall offect & DI TS
	B-related	$E_v + 0.25$	4.5×10 <sup>-19</sup>	
[43,75]*	Bs	$E_{v} + 0.2$	-	Theoretical calcula- tions
[67]	Extended (B-related)	$E_{v}$ + 0.21 to 0.23	-	Laplace DLTS
[65]	Extended (B-related)	$E_{v}$ + 1.1 to 1.3	~ 10 <sup>-18</sup>	Q-DLTS
[64]*	Dislocation- Related	$E_v$ + 0.99 to 1.15	~ 10 <sup>-18</sup>	DLTS & HR-ITS (high-resolution isothermal transient spectroscopy)
[53]* [43]*	V	$E_{v} + 0.6$	- ~10 <sup>-22</sup>	Positron Annihilation DLTS & HR-ITS
[76]		$E_{v} + 0.6$	~10 <sup>-17</sup>	ICTS (Isothermal capacitance Tran- sient Spectroscopy)

**Table 2.1** Major trap levels observed in polycrystalline B-doped CVD diamond along with single crystal (\*) and in un-doped CVD diamond films (\*\*).

Reference	Тгар	Energy level (eV)	capture cross- section $\sigma$ (cm <sup>2</sup> )	Experimental Method
[77]**		$E_v$ + 0.6 to 0.8	-	SCLC (Space charge limited currents)
[69]* [72] <b>**</b>	v	$E_{\nu} + 1.25$ $E_{\nu} + 1.14$ 1.23	- ~10 <sup>-13</sup>	DLTS & O-DLTS TSC & PICTS
[53,54]*	V	<i>E<sub>c</sub></i> + 2.5	-	Positron Annihila- tion & Theoretical calculations
[21,43,75]*	B <sub>s</sub> V	$E_{v} + 1.0$	~10 <sup>-18</sup>	DLTS& Theoretical calculations
[78]*	BH	<i>E<sub>c</sub></i> - 1.0	-	Theoretical calcula- tions
[78]*	BH <sub>2</sub>	$E_c$ - 1.84 to 2.88	-	Theoretical calcula- tions
75]*	B <sub>s</sub> VH	Midgap	-	Theoretical calcula- tions
[78]*	Н	$E_c - 1.45$ $E_c - 3.0$	-	Theoretical calcula- tions

## 2.5 Review of defects in *p*-type GaN: beneficial and detrimental

GaN commonly crystallises either in the hexagonal (wurtzite) structure or in the zinc blende structure. From theoretical calculations, the bandgap of wurtzite GaN is found to be approximately 3.45 eV, while for the zinc blende the predicted value is 3.34 eV. This review will focus on the wurtzite GaN, as the GaN samples discussed in this dissertation were grown in this form.

There are a number of essential factors that may cause significant reduction in the room temperature hole concentration achieved in any particular Mg-doped GaN film. These can be summarised as follows:

- The deep nature of the Mg acceptor (i.e. partial ionisation at room temperature)
- The presence of compensating donors (e.g. nitrogen vacancies).
- The incorporation of Mg atoms in electrically inactive sites (i.e. Mg dopants may segregate into planar defects).

The first point, the binding energy of Mg, is a fundamental issue and cannot be readily adjusted. It is therefore worth focusing on the other two effects.

The level of compensation in any Mg-doped GaN film depends strongly on the growth conditions and growth system design. This may explain the variations in p-type conductivity reported by various groups over the last two decades. In the literature [79-82], a compensating donor in Mg-doped GaN has been attributed to an intrinsic defect or a Mg-related defect, as usually experimental results from SIMS (secondary-ion mass spectroscopy) do not show high concentrations of any specific impurity. Calculations have shown that the formation of donor states, such as nitrogen vacancies  $(V_N)$ , is most likely to occur in Mg-doped GaN rather than in *n*-type GaN. The activation energy for nitrogen vacancy diffusion is controlled by the position of the Fermi level [83-84], i.e. when the Fermi position is in the midgap the  $V_N$  charge state is positive and diffusion is unlikely to occur. It has been suggested that a deep donor may be formed as a result of association of a nitrogen vacancy and a substitutional Mg ( $V_N$ -Mg<sub>Ga</sub>). Hautakangas *et al.* have studied defects in metal organic chemical vapour deposited (MOCVD) Mg-doped GaN films using positron annihilation spectroscopy [85]. Their observations indicate that the N vacancies are complexed with the magnesium dopants, forming neutral  $V_{\rm N}$ -Mg<sub>Ga</sub> complexes with a concentration of ~ $10^{17}$  to  $10^{18}$  cm<sup>-3</sup>. Most V<sub>N</sub> should be bound to Mg<sub>Ga</sub> in equilibrium at room temperature, and these pairs dissociated after thermal annealing at (500 -800°C) contributing to both activation and compensation of Mg doping; i.e. Mg activation and  $V_{\rm N}$  migration to the surface. The major compensating centres in p-type materials are  $V_{\rm N}$ -Mg<sub>Ga</sub> complexes. It has been reported that the 2.8 eV emission band observed in photoluminescence (PL) spectrum of MOCVD grown Mgdoped GaN films is due to donor-acceptor pair recombination [86]. This is in good agreement with theoretical calculations [84,87], which assume that the ~2.8 eV emission

band is due to electron transitions from the donor level of the  $V_{\rm N}$ -Mg<sub>Ga</sub> complex (with an ionisation energy of 0.3–0.4 eV below the conduction band minimum) to the acceptor level (~0.2 eV above the valence band maximum), depending on the  $V_{\rm N}$ -Mg<sub>Ga</sub> configuration and charge state.

The gallium vacancy ( $V_{Ga}$ ) defect plays a role in donor compensation in *n*-type GaN; it forms complexes with donor impurities. However, according to theoretical predictions and experimental observations,  $V_{Ga}$  defects are more likely to form in *n*-type than in *p*-type GaN [88]. The  $V_{Ga}$  in *n*-type GaN has a deep level about 1.1 eV above the valence band [89-90]. It has been proposed that the  $V_{Ga}$  is the source of the frequently observed yellow luminescence (YL) in GaN, centred around 2.3 eV. It is suggested that the YL is due to a transition between the conduction band or shallow donors and this deep level (1.1 eV), therefore result in emission around 2.3 eV. An increase in  $V_{Ga}$ concentrations has been observed by Saarinen *et al.* [91] in positron annihilation experiments on oxygen-doped MOCVD-grown GaN samples. The presence of oxygen was found to enhance the concentration of Ga vacancies and hence the YL. On the other hand they found that the YL was suppressed in *p*-type material, consistent with easier formation of  $V_{Ga}$  under *n*-type conditions.

It is known that hydrogen is always present in MOCVD grown films, which can also passivate the Mg in Mg-doped GaN films. It is believed that the high specific resistance of the *p*-GaN layer is due to the reduction of the hole concentration with increasing Mg-doping concentration, which has been attributed to the self-compensation effect in metalorganic vapour phase epitaxy (MOVPE) grown Mg-doped GaN layers [86]. The low *p*-type conductivity gives rise to considerable heating, leading to low performance and degradation of GaN-based devices. The study of device processing issues and the properties of Ohmic contacts to *p*-GaN have also lead to important improvements in device technology. Typically, Ohmic contacts to *p*-GaN are based on high work function metals, such as Pd, Pt, or Ni, with an over-layer of Au. These are annealed at 500-700°C to increase the hole concentration at the surface via the decomposition of Mg-H complexes and the formation of Ga vacancies through interaction with Au.

Van de Walle et al. [88] have found that the formation energy of hydrogen is lower in ptype GaN than in *n*-type GaN, corresponding to a much higher solubility in *p*-type than in *n*-type GaN. In *p*-type GaN, H acts as a donor  $(H^+)$ ; it is electrostatically attracted to negatively charged acceptors and hence it compensates acceptors. Interactions of hydrogen with native point defects in GaN have been studied. Van de Walle et al. performed DFT-LDA calculations for  $V_N$ -H complexes and reported that the  $V_N$ -H complex is the shallow double donor (~20-30 meV) responsible for the frequently observed 3.27 eV emission in Mg-doped GaN and present in sufficient amounts under p-type conditions. Experimental observations by Gelhausen et al. [92] show that the 3.27 eV donor-acceptor-pair (DAP) emission line to be strongly affected by low-energy electron beam irradiation. They have suggested that the acceptor in the 3.27 eV DAP emission is Mg and that the donor (20–30 meV) is a hydrogen related complex ( $V_N$ -H). Another emission line (~2.95 eV) relating to a donor at 350±30 meV was reduced during electron irradiation and attributed to a H-related defect. Their results also indicate that  $V_{\rm N}$ -H complex dissociated during electron irradiation or thermal annealing in N<sub>2</sub> or  $O_2$  atmosphere, generating isolated  $V_N$  and highly mobile H. Isolated  $V_N$  were found to have a binding energy of 180±10 meV according to DLTS and temperature-dependant Hall measurements results [93]. It has been reported [92] that isolated  $V_N$  is a possible candidate to be the donor level (~160 meV below the CB) in the frequently observed 3.14 eV DAP emission.

Carbon is an impurity in GaN acting as a shallow donor when  $C_{Ga}$  (substitutional carbon atoms on Ga site) or as an acceptor when  $C_N$  (substitutional carbon atoms on N site) [94-96]. The presence of the shallow defect  $C_{Ga}$  (~0.2 eV below the conduction band) has been theoretically acknowledged in *p*-type GaN [96] and also via recent experimental observations [94] using cathodoluminescence on nominally undoped semiinsulating GaN layers grown by hot-wall MOCVD. Kakanakova-Georgieva *et al.* [94] have observed a clear evidence of carbon-caused compensation; the blue luminescence at ~415 nm has been strongly correlated with DAP transitions via  $C_{Ga}$ - $C_N$ . Recent theoretical calculations [97] have predicted that the substitutional defect  $C_N$  to be a deep rather than a shallow acceptor in GaN. However, Carbon-related defects in GaN and their involvement in the various radiative recombinations under photon and electron excitation remain a topic of persistent discussions.

The incorporation of Mg dopants in electrically inactive sites or diffusion to dislocation cores is still a subject of ongoing debate [98-104]. Threading dislocations in GaN films arise as a consequence of the lattice parameter mismatch between the GaN and the substrate; this is due to the fact that most of the GaN based devices are grown heteroepitaxially on substrates such as sapphire. Threading dislocation densities in the order of 10<sup>9</sup> cm<sup>-2</sup> are commonly observed in GaN grown on foreign substrates [98], this used to be more than  $10^{10}$  cm<sup>-2</sup> in early devices [100]. In conventional optoelectronic devices (e.g. AlGaAs or AlInGaP based devices), defect densities six orders of magnitude lower would be expected to result in excessive non-radiative recombination, generation of heat and consequently device failure [99]. Despite the high density of defects, GaN based LEDs still can achieve high quantum efficiencies. It has been shown that the concentration of non-radiative recombination centres in GaN is somehow in correlation with the threading dislocation density [105]. However, the concept of whether TDs themselves act as non-radiative recombination centres remains controversial. An explanation for the defect insensitive nature of the near-band-edge emission in indium-containing nitride films (e.g. InGaN or AlInGaN) is due to the extremely short diffusion lengths (<4 nm), short radiative lifetimes of excitonic emissions, fairly long non-radiative lifetime and preferential capture of holes and/or positrons (positrons are the antimatter of electrons, having a positive charge similar to holes) by localised radiative centres (atomic condensates of In-N) which form localised valence states with high positron affinity; the holes form localized excitons to emit the light, although some of the excitons recombine at non-radiative centres [106].

A range of experimental techniques have been used by a number of authors to investigate deep level centres in p-GaN. Temperature-dependent Hall effect experiments have been carried out to deduce the acceptor activation energy and investigate the compensation level [107-110]. Thermal admittance spectroscopy measurements on Mg-doped GaN have also received considerable attention as reliable method for detecting

shallow and deep levels [111,112]. DLTS measurements have been extensively applied to *n*-type GaN [113-115], evidence of various deep centres within the bandgap have been revealed, however, fewer DLTS studies have been conducted on defects in Mgdoped GaN [116,117]. Unfortunately, conclusions from this range of electrical measurements regarding the properties and origin of deep levels in Mg-doped GaN have not been convincing, perhaps the samples employed may have varied in quality, with difficulties in forming metal contacts to *p*-GaN and issues with doping level.

A summary of the defect levels reported in Mg-doped wurtzite GaN, with their estimated activation energies, is tabulated in Table 2.2.

Reference	Trap	Energy Level (eV)	Experimental Technique or Method Used	
[88,92], [118- 120]	Substitutional Mg (Mg <sub>Ga</sub> )	$E_v + 0.124$	DLTS, TAS and Theoretical calculations	
		$E_{v} + 0.135$		
		$E_{v} + 0.16$		
		$E_{v} + 0.18$		
		$E_{v} + 0.20$		
		$E_{v} + 0.25$		
[95,121]	Dislocation-related	<i>E<sub>c</sub></i> - 2.97	O-DLTS and SSPC (Steady- State PhotoCapacitance)	
[118]	Dislocation-related	$E_{\rm u} + 0.40$	TAS, DLTS combined with MCL (Microcathodolumines- cence) and EBIC (Electron beam induced current) imaging	
		$E_{V} + 0.85$		
		<b>D</b> <i>y</i> <b>T0.05</b>		
[88,92-93]	$V_{ m N}$	<i>E<sub>c</sub></i> - 0.16	DLTS, PL and Theoretical calculations	
[94- 96]	C <sub>Ga</sub>	<i>E<sub>c</sub></i> - 0.20	O-DLTS, SSPC and Theoreti- cal calculations	
[86,88], [122-124]	V <sub>N</sub> – Mg <sub>Ga</sub>	<i>E<sub>c</sub></i> - 0.3-0.4	PL, Hall measurements and Theoretical calculations	

Table 2.2 Trap levels observed in the literature for Mg-doped wurtzite GaN films.

### **2.6** Electrical contacts to polycrystalline diamond

Most metals have been found to yield Schottky contacts to polycrystalline diamond; metals such as Au or Al are commonly used to form Schottky contacts [125-128]. It has been always difficult to produce good Ohmic contacts on wide bandgap materials such as diamond due to the large barrier heights that generally form when metals are deposited. Heavy doping near the diamond surface is used to enhance tunnelling through the potential barrier at the metal/diamond interface and improve conduction. Ohmic contact formation depends on several factors such as the doping level, surface treatment prior to metal deposition, annealing temperature or the density of surface states which govern the Fermi level pining and therefore influence the barrier height. The application of different surface treatments has been found to change the surface termination from hydrogen to oxygen terminated and hence change the properties of contacts. For example, low resistivity contacts can be achieved by exposing the diamond film to  $O_2$  plasma, prior to metal deposition, or dipping in a CrO<sub>3</sub> in H<sub>2</sub>SO<sub>4</sub> solution at 200°C followed by a rinse in a 1:1 solution of  $H_2O_2$  and  $NH_4OH$  at 90°C. It has been found that transition metals such as Ti or Ta form low resistivity carbides as they have great affinity with carbon, this would enhance the diffusion of subsequently deposited metals [129]. Ti/Au contacts have been reported [130] to exhibit good Ohmic characteristics. A post deposition anneal at 500°C for 10 minutes yielded a reduction in the specific contact resistivity by three orders of magnitude to  $10^{-6} \Omega \text{ cm}^2$ . However, not much improvement of the resistance of the Ohmic contacts has been achieved by post annealing at higher temperatures (>850°C).

### 2.7 Electrical contacts to *p*-type GaN

The difficulty in forming low resistance Ohmic contacts to *p*-type GaN is due to the fact that GaN is a wide bandgap semiconductor, requiring high work function metals to obtain Ohmic contacts. High work function metals including Au, Pt, Pd or Ni have been investigated, in standard metal contact forms to *p*-GaN [131-135]. Various bilayer and complex metallization schemes have been also investigated. For example, Ni/Au, Pt/Au, Pd/Au, Pd/Pt/Au, Pt/Ni/Au, Ni/Pt/Au, Cr/Au, Ni/Cr/Au, Au/Mg/Au, Ni/Mg/Ni/Si,

Ni/Au-Zn and Cr/Au-Zn [136-143]. These have all exhibited high specific contact resistance (>10<sup>-3</sup>  $\Omega$  cm<sup>2</sup>). Only Ni/Au bilayer when annealed in an oxygen-containing atmosphere (400 - 600°C) resulted in a specific resistance of the order of  $10^{-4} \Omega \text{ cm}^2$ [144]. Reduction in the specific contact resistance  $(10^{-4}-10^{-6} \ \Omega \ cm^2)$  has been achieved by using the Au/Ni structure annealed in  $O_2 + N_2$  ambient [145]. It has been found that the main mechanism responsible for the Ohmic nature is the creation of a thin oxide layer (NiO) on the metal/p-GaN interface. Liday et al. [145] have investigated a NiO<sub>x</sub> based contact scheme (Au/NiO<sub>x</sub>) to p-GaN, with a low content of oxygen in the  $NiO_x$ layer. They have reported that a low contact resistance is assisted by Ga vacancies in the region of the metal/p-GaN interface after diffusion of Ga into the metallic layer, and also suggest that the creation of a metal/NiO/p-GaN contact structure due to annealing in  $O_2 + N_2$  is responsible for the obtained Ohmic properties. Smalc-Koziorowska *et al.* argue that an essential factor leading to high resistance contacts is Ni [146]. They have suggested that in order to obtain low resistance contacts to p-type GaN a thin nonoxidized Ni layer combined with the separated oxidized Ni layer is necessary. They have observed that one of two contact structures may develop during annealing of the simple Ni/Au contact, depending on the GaN surface morphology. These normally result in different properties of the Ni/Au contact under thermal strain. They have concluded that contacts on rough GaN surfaces (covered with hillocks containing dislocations) cause non-uniformity of the Au layer, and result in high resistance, whereas relatively low resistance contact may be obtained on a relatively smooth GaN surface as the Au layer deposited on such surface remains continuous [146].

### 2.8 Effect of plasma etching on contacts to *p*-type GaN

Chemical etching is a useful process for device fabrication. Various wet etching approaches have been applied to *n*-type and *p*-type GaN [147-152]; investigations have shown that selective wet etching of GaN in KOH is still associated with difficulties and does not yield satisfactory results [147,148]. So far, no suitable wet etchant has been found for GaN and related compounds due to their chemical stability against various acids and bases used at  $75^{\circ}$ C. Plasma etching (dry etching) is an important process for

the fabrication of various GaN based devices. Despite the fact that it is well documented that plasma processing of nitride semiconductors may induce significant damage to the near surface region of the film [153-159]. Argon plasmas are commonly used as they do not interact chemically with the GaN. O<sub>2</sub> plasmas are also used in semiconductor device processing to remove hydrocarbon contamination, while fluorine-containing plasmas are used for dielectric etching. There have been some attempts [160] to overcome the plasma damage issue by burying the damage with a *p*-type re-growth; however this has not solved the problem completely. Several authors have investigated the effect of postplasma processes to recover from the induced damage and achieve reliable Ohmic contacts to p-type GaN [154,155,161]. It has been reported that exposure of n-type GaN surfaces to plasma affects the performance of Schottky contacts, with increased leakage currents and reduced barrier heights [162]. This has been postulated to be caused by an increased n-type doping in the near surface region due to preferential loss of nitrogen from these layers [155,163]. In p-GaN, damage-related shallow or deep donor states significantly degrade the properties of contacts, i.e. compensation of the acceptors will take place in the near-surface region. Annealing at very high temperatures (750°C) in N<sub>2</sub>, for 30 seconds, has been shown to have a significant effect on reducing the plasmainduced damage in p-type GaN [164]. It has been reported [165] that ohmic contacts were obtained using a low inductively-coupled plasma (ICP) power (~50 W) combined with high temperature post-etch annealing (1000°C), however, there is no quantitative analysis of the resistance of the contacts, which may have been affected by this high annealing temperatures. Hsuch et al. have investigated the effect of a low reactive ion etching plasma power of 50 W on Schottky barrier height [166]. Low power etching, using RF/ICP powers of 20/40 W, have been found to improve the properties of unannealed Ohmic contacts to p-GaN and without the use of regrowth techniques [167].

#### **2.9** Conclusions

This chapter initially discussed the different types of crystallographic defects in semiconductors and the properties of deep and shallow levels. The issues of impurity incorporation and doping of wide bandgap semiconductors were also discussed. Literature reviews on beneficial and detrimental defects in CVD polycrystalline diamond and Mg doped MOCVD GaN have been provided. Finally, various methods for the fabrication of metal contacts on B doped diamond and p-GaN have also been presented.

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# **3. Growth Techniques Used In This Work**

### **3.1 Introduction**

Chemical vapour deposition (CVD) is a microfabrication chemical process, widely used in the semiconductor industry to produce thin films. The process involves a gas phase chemical reaction occurring above a solid surface. Usually, the CVD process is used to produce solid materials with high-purity and high-performance. The materials of interest, such as silicon, silicon carbide, gallium nitride and synthetic diamonds, can be deposited in various forms including: monocrystalline, polycrystalline, amorphous, and epitaxial films.

According to the process by which chemical reactions are initiated (i.e. activation process) and process conditions, the CVD technique is classified into a number of methods. The activation can involve thermal methods (e.g. a hot filament is used to chemically decompose the source gases), electric discharge (e.g. DC, RF or microwave which allows deposition at lower temperatures, always critical in the manufacture of semiconductors), or a combustion flame (such as an oxyacetylene torch, an open-atmosphere, flame-based technique for depositing high-quality thin films and nanomaterials). Although each method differs in detail, they still share a number of common features. For example, to ensure the formation of diamond rather than amorphous carbon the temperature of the substrate is usually greater than  $700^{\circ}$ C. Also, growth of diamond normally requires that about 1%vol. CH<sub>4</sub> (the precursor gas) is diluted in excess of hydrogen. In addition the desired doping can be incorporated into the film during CVD growth by including the required dopant atoms into the gas mixture. A detailed review of the various CVD methods can be found in [1-4]; only brief explanations about the techniques used in this work are mentioned here.

### **3.2 Hot Filament CVD**

Hot filament CVD (HFCVD) is one of the CVD techniques used for producing diamond films. It uses a vacuum chamber in which the process gases are metered in at carefully controlled rates. The pressure in the chamber is maintained at typically 20–30 Torr. A substrate heater is used to bring the substrate up to a temperature of 700–900°C, the substrate sits on the heater, a few millimetres below a filament, which is electrically heated to temperatures in excess of 2200°C, as illustrated in Figure 3.1.



**Figure 3.1** On the left side: the HFCVD reactors at Bristol University dedicated for Boron doped diamond. On the right a schematic diagram of the vacuum chamber.

The filament is usually made from a metal such as tungsten or tantalum; however, the resistivity of these metals changes due to the fact that they react with the carboncontaining gases and carburize to form the metal carbide and hence they become brittle, reducing their lifetime and the maximum deposition time that can be performed in one run. This issue can be solved by using rhenium for the filament material since Re is able to survive these conditions and does not react significantly with the process gas (e.g. does not act as a sink for carbon or boron species). The HFCVD method is relatively low-cost and easy to operate and produces reasonable quality polycrystalline diamond films at a rate of  $1-10 \mu$ m/h, depending upon exact deposition conditions. However, one of the major disadvantages of this technique is that the hot filament is particularly sensitive to oxidizing or corrosive gases, which limits the variety of gas mixtures which can be used [5]. Recent advances in the HFCVD technique have led to the growth of mono-crystalline diamond under specific conditions; this may be the future of large scale single crystal growth for electronic applications [6].

### 3.3 Microwave Plasma CVD

Plasma is any gas in which a significant percentage of the atoms or molecules is ionized; typically this takes place at low pressure (mTorr to a few Torr). Plasmas with low fractional ionization are of great interest for materials processing because electrons are very light compared to atoms and molecules. Energy exchange between the electrons and neutral gas is very inefficient, therefore electrons can be maintained at very high temperatures, equivalent to several electronvolts of average energy, while the neutral atoms remain at the ambient temperature. These energetic electrons can induce dissociation of precursor molecules and the creation of large quantities of free radicals.

Microwave plasma CVD (MWPCVD) deposition occurs after the creation of plasma of the reacting gases. The plasma is generally created by RF (AC) frequency or DC discharge between two electrodes, the space between which is filled with the reacting gases; microwave power is coupled into the chamber via a dielectric window (usually quartz) in order to create a discharge. The microwaves couple energy into gas phase electrons, which in turn transfer their energy to the gas through collisions. This leads to heating and dissociation of the gas molecules, the formation of active species, and finally film deposition onto a substrate, which is immersed in the plasma.

MWPCVD reactors use very similar conditions to HFCVD reactors, but they use higher power and higher growth rates have been achieved (>10  $\mu$ m/h). Hence MWPCVD is now among the most widely used techniques for diamond growth, despite being significantly more expensive. In addition, a wide variety of gas mixtures can be employed due to the fact that no filaments are required. Recent advances using MWPCVD have been reported [7] for successful growth of single crystal diamond, where the substrate stage design and methane concentration have been optimised. High quality diamond at high growth rates (50-150)  $\mu$ m/h was achieved while varying the gas pressure, concentration and substrate temperature for enhanced growth and crystal purity [8].

Figure 3.2 illustrates an ASTeX (2.5 GHz) MWPCVD reactor [9] in which microwave powers of up to 5 kW can be used achieving growth rates well in excess of 10  $\mu$ m/h.





**Figure 3.2** On the left side: an ASTeX MWPCVD reactor at Bristol University dedicated for B doped diamond. On the right, a schematic diagram of the vacuum chamber.

The substrates to be coated are positioned on a heated stage directly beneath the plasma ball; substrates as large as 10 cm in diameter can be used to grow thin films. In principle, the inner chamber diameter is chosen so that only one microwave radial mode can be sustained in the cavity at 2.45 GHz. Microwaves are coupled into a water-cooled

metal cavity through a quartz window, using a tuning antenna which converts the  $TE_{10}$  microwave mode in the waveguide to the  $TM_{01}$  mode in the cavity.

## 3.4 Metalorganic Vapour Phase Epitaxy

Metalorganic vapour phase epitaxy (MOVPE), is a CVD method of epitaxial growth of materials and is also known as metal organic chemical vapor deposition (MOCVD); it is primarily used for growing II-VI and III-V materials, some metallic oxides and metals.

The MOVPE technique has become more important since nitride based light emitting diodes (LEDs) were first demonstrated in the early 90's [2, 3].



**Figure 3.3** Basic MOVPE schematic diagram, where MFC is the mass flow controller which controls the amount of gas going into the reactor.

The word epitaxy is derived from the Greek term meaning stacked or arranged in thin layers. Basically, to produce thin layers of compound semiconductors, the chemicals have to be vaporized and transported into the MOVPE reactor together with other gases; ultra-pure gases are injected and then finely dosed, as illustrated in Figure 3.3. Formation of the epitaxial layer occurs by final pyrolysis of the constituent chemicals at the substrate surface.

Many materials of interest are difficult to transport via gases because they tend to have very low vapour pressures, unlike organic compounds which often have very high vapour pressure. Therefore, a metal such as Ga, Al or Cu has to be chemically attached to an organic compound that has a very high vapour pressure. However, the organicmetal bond is very weak and can be broken during thermal processing on the wafer, depositing the metal with the high vapour pressure organic component being pumped away.

One of the disadvantages of MOCVD is that care must be taken to ensure that little of the organic byproducts are incorporated. Unintentional hydrogen incorporation and carbon contamination are sometimes detrimental issues. Also there are growing concerns associated with the safe use and the maximum quantities of hazardous materials such as certain gases and metalorganics permissible in device fabrication operations. These have become factors of paramount importance in the MOVPE-based crystal growth of compound semiconductors.

A robust route to uniformity and scalability has been achieved by implementing the Close Coupled Showerhead (CCS) MOVPE technology [11]. Figure 3.4 shows a photo of a CCS Thomas Swan (now Aixtron)  $6\times2$  inch MOCVD growth system, at the University of Cambridge, in which the GaN samples discussed in this work were grown.





In CCS MOCVD, the chemicals are introduced vertically into the reactor chamber, with the gases introduced through a huge number of very small channels designed like a showerhead in the reactor ceiling, located very close to the heated wafers, which assures that the process gases are always distributed uniformly over the whole wafer carrier surface. Further, it is constructed to enable precursors to be separated right up to the point where they are injected onto the substrates through multiple small pipes. The reagents are injected into the reactor chamber through separate orifices in a water-cooled showerhead injector, to create a uniform distribution of reagent gases. Substrates are placed on top of a rotating susceptor, which is resistively heated. The three-zone heater enables modification of the temperature profile to provide temperature uniformity over the susceptor diameter. This technology enables the chemicals to decompose and the targeted atoms diffuse very quickly through the gas phase onto the wafer surface.



Figure 3.5 Aixtron Close Coupled Showerhead 55x2 inch [11].

Figure 3.5 shows an Aixtron multi-wafer CCS system; the reason for using 2 inch diameter wafers is because GaN-based materials typically grown on sapphire, which is cheaper per unit area for 2 inch wafers. The current advances in MOCVD technology have enabled the deposition of large surface areas and therefore MOCVD has become the first and most cost-effective choice for compound semiconductor manufacturers.
## 3.5 Conclusions

This chapter briefly discussed several important CVD techniques used to fabricate electronic materials to meet the industry demands, as well as pointing out the drawbacks associated with CVD such as unintentional hydrogen incorporation and carbon contamination which are sometimes detrimental effect in device fabrication.

In addition, the HFCVD and MWPCVD growth techniques used in this work to grow synthetic diamond thin films were discussed. Detailed information about MOVPE growth using Close Coupled Showerhead technology were given in this chapter, as this was the method used to grow GaN wafers in this thesis.

Finally, some examples were given to show that researchers and industry are currently concentrating upon developing methods to scale up the CVD processes and reduce production costs to the point at which it becomes economically viable to use wide bandgap semiconductors as materials of choice.

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# 4. Theory of Electrical Characterisation Methods

## 4.1 Introduction

Most semiconductor device applications rely on the electrical properties of the semiconductor. It is important to measure the electrical properties of deep level defects within the bandgap as, in some cases, the processes that occur in deep levels which influence device performance are non-radiative and cannot be observed by optical techniques such as Photoluminescence (PL). Different capacitance measurement techniques have been applied to investigate defects within the bandgap of semiconductors. These include Photocapacitance and Thermally Stimulated Capacitance (TSCAP) which either exhibit low sensitivity or they are only suitable for the extraction of optical parameters and therefore did not cover broad application. Other techniques such as Positron Annihilation Spectroscopy (PAS), a contactless method which allows depth-dependent defect characterization, is significantly sensitive to void-like defects such as vacancies but requires elaborate equipment that is not readily available to most researchers. Thermally Stimulated Current (TSC), Deep Level Transient Spectroscopy (DLTS), and Thermal Admittance Spectroscopy (TAS) are amongst the useful electrical characterisation tools that are widely used for studying electrically active defects in semiconductors. However, TAS is only suitable for detecting majority carrier traps and TSC is strongly influenced by leakage currents and the information obtained from TSC is limited and more difficult to interpret comparing to DLTS [1]. DLTS is one of the most common deep-level characterisation techniques today, having replaced TSC. Capacitance-Voltage (C-V) and Current-Voltage (I-V), used in conjunction with other electrical characterisation methods, are helpful tools for extracting useful information and also in assessing the suitability of a specific Schottky or a p-n junction to be used for further measurements such as DLTS or TAS.

The theory of semiconductors is described in many text books [1-3]. Therefore, only a short description of the basic aspects that are relevant to this research is given. The aim

of this chapter is to introduce the reader to the terminology and notation used in this thesis.

## **4.2** Theory of the depletion region

### 4.2.1 An overview of semiconductor junctions

Junctions are the boundary or the interface that occurs between two semiconducting materials of interest. For example, growing a layer of crystal doped with one type of dopant (e.g. a *p*-type semiconductor) on top of a layer of crystal doped with another type of dopant (*n*-type semiconductor) should form a *p*-*n* junction. If these layers were made of the same material but different dopants then it is called a *p*-*n* homojunction, whereas, if they were made out of different semiconductors, they are called *p*-*n* heterojunctions. Heterojunctions can form between two different materials with the same type of doping (isotype), known as *p*-*p* or *n*-*n* heterojunctions.

A different type of junction known as a *metal-semiconductor junction* is created by depositing metal layers on a semiconductor. A metal-semiconductor junction can either form a *Schottky* barrier (as a device by itself it is known as a Schottky diode) or form a non rectifying contact known as *Ohmic* contact. The type of contact formed depends on the bandgap of the semiconductor, doping type and carrier concentrations in the semiconductor, the metal's work function, and other factors such as surface states.

Although a p-n or a Schottky are both junctions of interest for electrical characterisation measurements using capacitance spectroscopy techniques, the analysis or characterisation of defects within a bandgap of a specific material can be made simpler by using a Schottky junction. In the fabrication of a Schottky device only one type of semiconducting material is used, one type of carrier and also there is no need to dope the same material both n and p-type. In a Schottky barrier the space charge region extends only into the semiconductor. Due to Schottky barrier there should be no injection of minority carriers; hence there is only majority carrier conduction, making the analysis easier. However, this depends on factors such as the formed barrier's characteristics.

#### 4.2.2 *p-n* Junctions

A *p*-*n* structure consists of two semiconductor regions with different doping type as shown in Figure 4.1. The *p*-type region has an acceptor density ( $N_A$ ), while the *n*-type region has a donor density ( $N_D$ ). The dopants are considered to be shallow, so that, for example, the electron density in the *n*-type region is approximately equal to the donor density. The same applies to the holes in the *p*-type region.



**Figure 4.1** A p-n junction in thermal equilibrium (zero-bias). The underneath plots illustrate the charge density, the electric field, and the built-in voltage [4].

In thermal equilibrium condition (no external voltage is applied), a potential difference or built-in potential ( $V_{bi}$ ) is formed across the junction. This is due to the fact that the dopants in the regions close to the p-n interface lose their neutrality and become charged, forming a depletion region or space charge region. In the n region nearby the p-n interface, electrons tend to diffuse into the p region leaving behind positively charged ions (donors). Similarly, holes in the p region near the junction tend to diffuse into the n-type region leaving negatively charged ions (acceptors). An electric field formed by the charges on the ionized donors and acceptors, causes a drift of carriers in the opposite direction. The diffusion of carriers continues until the drift current balances the diffusion current. The depletion region extends further on the less doped side, since the depletion region has the same magnitude of charge on both sides of the p-n junction. Equilibrium is reached when the two Fermi levels ( $E_{Fn}$  and  $E_{Fp}$ ) equalise.



Figure 4.2 A reverse-biased silicon p-n diode.

If a *p*-*n* diode is reverse-biased, as shown in Figure 4.2 and Figure 4.3, the potential across the junction increases with increasing reverse-bias voltage and so does the width of the depletion region. The junction barrier becomes greater and charge flow is minimal. When the *p*-*n* junction is forward-biased (opposite polarity) the negative charge applied to the *n*-type semiconductor repels the electrons (i.e. electrons flowing through the *n*-type region toward the junction), while the positive charge applied to the *p*-type

semiconductor repels the holes (i.e. holes flowing through the p-type region in the opposite direction toward the junction). This lowers the potential barrier; the electrons and holes travel in opposite directions, but they also have opposite charges, so the overall current is in the same direction on both sides of the diode. The depletion region decreases with increasing forward-bias voltage and eventually becomes narrow enough that electrons can cross the junction and inject into the p-type semiconductor. Also the two species of carriers are constantly recombining in the vicinity of the narrow junction, which is detrimental for device performance.



Figure 4.3 Energy band diagram of a *p*-*n* junction under reverse and forward bias [5].

#### 4.2.3 Schottky barrier diode

According to the Schottky model, bringing a metal and a semiconductor in intimate contact will result in a potential barrier formed at the metal-semiconductor interface preventing most charge carriers (electrons or holes) from passing from one side to the other. Only carriers that have enough energy to get over the barrier will cross to the other side of the junction via thermionic emission.

In Figure 4.4, a basic Schottky contact on an *n*-type semiconductor is shown. The energy band diagram is constructed with reference to the vacuum level (the energy of a free stationary electron outside the material). However, not all metals form Schottky barriers; a metal is characterised by the work function ( $\Phi_m$ ) which is the energy required to excite an electron from the metal to the vacuum level. The semiconductor is characterised by the electron affinity of the material ( $X_s$ ). In thermal equilibrium, the Fermi energy levels of the semiconductor ( $E_{Fs}$ ) and the metal ( $E_{Fm}$ ) should be aligned, band bending occurs on the semiconductor side, meaning that the depletion region is extending only on the semiconductor side.



**Figure 4.4** Band diagram of a Schottky junction on *n*-type semiconductor, in thermal equilibrium [5].



**Figure 4.5** Energy band diagram of a Schottky junction (a) under forward bias and (b) under reverse bias [5].

Figure 4.5 illustrates that it is possible to vary the depletion width by applying a voltage to the Schottky junction. When the junction is reverse-biased, the negative charge applied to the metal repels the electrons; the dopants electrons will be emitted (i.e. dopants become ionized and give rise to a space charge). If the junction is forward biased, the electrons will be captured. The metal–semiconductor interface and the edge of the depleted region work like two capacitor plates, with the depletion region acting as a dielectric.

Therefore, Schottky devices are commonly used in electrical characterization of semiconductors. It is possible to characterize a semiconductor material by analysing the emission and/or capture of electrons by dopants or by any defects; C-V profiling admittance spectroscopy and DLTS are the most popular electrical characterization techniques that use this type of junction. For a Schottky barrier or a p-n junction diode, capacitance measurements should detect any charge that responds to an applied time varying voltage. However, interface traps and/or deep level defects in the semiconductor bulk can contribute to the capacitance and hence produce errors in capacitance profiles. Although the ac voltage frequency is often considered to be sufficiently high (1 MHz) for the interface traps to be unable to follow, errors can still arise in both time and depth dependent *C*-*V* profile because the dc reverse bias usually varies sufficiently slowly for the traps to be able to respond. For trap concentrations much less than the doping density, e.g. 1% or less, the contribution of traps is usually negligible.

### 4.3 Majority and minority carriers: emission and capture

The semiconductor has *n* electrons/cm<sup>3</sup> in the conduction band and *p* holes/cm<sup>3</sup> in the valence band introduced by shallow-level dopants. There are only four possibilities for the behaviour of a deep level with regard to the conduction and the valence bands, as illustrated in Figure 4.6, where  $n_T$  and  $p_T$  represent the deep traps occupied by electrons and holes respectively.



**Figure 4.6** The probabilities of carrier capture and emission processes for deep-level impurities within the bandgap of a semiconductor [1].

The emission rate  $(e_n)$  represents the electrons emitted per second  $(s^{-1})$  from electronoccupied centres. The capture rate  $(c_n . n)$  represents the density of electrons captured per second  $(cm^3 s^{-1})$  from the conduction band. For example when an electron is captured from the conduction band by a deep centre, this process is called electron capture and it is characterised by the capture coefficient  $(c_n)$ , one of two events will takes place. The deep centre can either emit the electron back to the conduction band (called electron emission) or it can capture a hole  $(c_p)$  from the valence band. Following either of these processes, the deep centre is occupied by a hole and again has two options; either it captures an electron from the conduction band or emits the hole back to the valence band. The latter event is sometimes viewed as electron emission from the valence band to the centre. Generally after an electron has been emitted, the centre finds itself in the  $p_T$  state and subsequently emits a hole, returning it to the  $n_T$  state. Then the cycle repeats.

An impurity can act as a trap or a generation-recombination (*G-R*) centre depending on the Fermi level position, the energy level of the deep centre, the capture cross-section of the centre, and the temperature. For centres nearer to the conduction band edge electron emission dominates  $e_n >> e_p$ , whereas for centres nearer to the valence band edge  $e_p >> e_n$ . Centres with energies near the midgap behave as *G-R* centres, which can exist in one of two states. If occupied by an electron, it is in the  $n_T$  state and if occupied by a hole, it is in the  $p_T$  state. If the *G-R* centre is an acceptor,  $n_T$  is negatively charged and  $p_T$ is neutral. If it is a donor,  $n_T$  is neutral and  $p_T$  is positively charged. The density of centres occupied by electrons  $n_T$  and holes  $p_T$  must equal the total density ( $N_T = n_T + p_T$ ). It should be noted that when majority and minority carriers are generated or recombine, the electron density in the conduction band (n), the hole density in the valence band (p), and the charge state of the centre  $n_T$  or  $p_T$  are all functions of time.

For a Schottky diode, as described in Figure 4.7(a), at zero bias, capture dominates emission, and the steady-state density of deep traps is  $n_T \approx N_T$ . The time dependence of  $n_T$ , during the initial emission period, is given by:



**Figure 4.7** A Schottky diode (a) zero bias, (b) reverse bias at t = 0, (c) reverse bias at t > 0 and (d) The applied voltage as a function of time and the capacitance transient [1].

$$n_T(t) = n_T(0) \exp\left(-\frac{t}{\tau_e}\right) \approx N_T \exp\left(-\frac{t}{\tau_e}\right)$$
(4.1)

where  $\tau_e$  is the electron emission time ( $\tau_e = 1/e_n$ ),  $n_T(0)$  is the initial steady-state density and it is given by:

$$n_T = \frac{e_p}{e_n + e_p} N_T \tag{4.2}$$

When the diode is biased from zero to reverse bias, with most trap levels initially occupied by electrons for  $t \le 0$ , electrons are emitted from the traps for t > 0. During this

period of reverse bias emission dominates because the emitted carriers (electrons) are swept out of the space-charge region (scr) very quickly (i.e. the transit time is shorter than the typical capture times), therefore reducing the probability of being recaptured. When the diode is pulsed from reverse to zero bias, electrons rush in to be captured by traps in the  $p_T$  state. During the capture period, the time dependence of  $n_T$  is:

$$n_T(t) = N_T \cdot \left(N_T - n_T(0)\right) \exp\left(-\frac{t}{\tau_c}\right)$$
(4.3)

where  $\tau_c$  is the electron capture time ( $\tau_c = 1/c_n.n$ )

The capacitance of the Schottky device of Figure 4.7 is best described by [1]:

$$C = A \sqrt{\frac{\varepsilon_0 q N_{scr}}{2(V_{bi} - V_1)}}$$
(4.4)

where, A is the area of the diode, q is the electron charge,  $V_I$  is the applied reverse bias,  $V_{bi}$  is the built-in potential,  $\varepsilon \& \varepsilon_0$  are the permittivities of the semiconductor and free space respectively and  $N_{scr}$  is the density of ionized impurities in the scr. The ionized shallow donors (dopant atoms in the scr) are positively charged  $N_D^+$ , and  $N_{scr}$  depends on the status of deep levels:

- In the case of deep *acceptor* impurities that are occupied by electrons (negatively charged),  $N_{scr} = N_D^+ n_T^-$ .
- For deep *acceptor* centres that are occupied by holes (neutral),  $N_{scr} = N_D^+$ .
- For shallow and deep donor levels occupied by electrons (neutral),  $N_{scr} = N_D^+$ .
- For deep donor level occupied by holes (positively charged),  $N_{scr} = N_D^+ + p_T^+$ .

In Figure 4.7(a) the diode is initially zero biased, allowing traps to capture majority carriers (electrons in *n*-type). In Figure 4.7(b) majority carriers are emitted from the traps as a function of time immediately after a reverse bias pulse is applied to the junction. The majority carriers are emitted at  $t \ge 0$  contributing to the capacitance, i.e.

the depletion region width (*W*) decreases and *C* increases until steady state is attained as illustrated in Figure 4.7(c) & (d), where  $C_0$  is the quiescent capacitance, and  $C_{(V=0)}$  is the capacitance at zero bias. It should be noted that the applied reverse bias has to be long enough so that all majority carriers are emitted. If the time available for electron capture is short, not all the traps will be occupied by electrons when the diode returns to reverse bias. The capture time ( $\tau_c$ ) is given by:

$$\tau_c = (C_n \cdot n)^{-1} \tag{4.5}$$

$$C_n = \sigma_n v_{th} \tag{4.6}$$

where  $\sigma_n$  is the electron capture cross-section,  $v_{th}$  is the electron thermal velocities and n is the electron density.

Unfortunately there are situations when not all traps empty during the emission process; trap levels below the Fermi level remain occupied by electrons during the emission transient and do not capture electrons during the filling process.

For electrical minority carrier injection (e.g. holes in *n*-type), *p*-*n* junctions should be used. It is well known that Schottky diodes do not inject minority carriers efficiently. For example if a  $p^+$ -*n* junction is forward biased, holes are injected into the *n* region and capture dominates emission. In this case it is difficult to predict the occupancy, but the traps are no longer solely occupied by majority carriers (electrons) contrary to the case of zero bias; a certain fraction is occupied by holes.

In Figure 4.8, at t = 0, assume that in an *n*-type diode all deep-level impurities are occupied by electrons (majority carrier emission) or holes (minority carrier emission). The transient is still detected as a time-varying capacitance and it is described by the expression

$$C(t) = C_0 \left[ 1 - \left( \frac{n_T(0)}{2N_D} \right) \exp \left( -\frac{t}{\tau_e} \right) \right]$$
(4.7)



**Figure 4.8** The capacitance-time transients following majority carrier emission and minority carrier emission [1].

where  $n_T(0)$  is the initial steady-state density and  $C_0$  is the quiescent capacitance (i.e. the initial capacitance of a device at reverse bias -V assuming that all deep-level impurities are emitted). The trap concentration can be calculated using a first-order expansion of Equation (4.7).

$$C \approx C_0 \left( 1 - \frac{n_T(0)}{2N_D} \right) \tag{4.8}$$

if it is assumed that most traps are occupied by holes (minority carriers), this would imply for the deep-level acceptor impurities that  $n_T \approx 0$  and  $N_{scr} \approx N_D$ , because deeplevel acceptor centres are neutral when occupied by holes. That is the state just after the junction has been forward biased (at t=0). Immediately after applying a reverse bias pulse, minority carriers (holes) are emitted from the traps, and hence their charge changes from neutral to negative, for  $t \rightarrow \infty$ , the total ionized scr density decreases  $N_{scr} \approx$  $N_D - n_T$ , the width of the scr increases, and the capacitance decreases. The emission time constant ( $\tau_e$ ) is given by:

$$\tau_e = \frac{1}{e_n + e_p} \tag{4.9}$$

Where  $e_p >> e_n$ , (hole emission dominates for centres nearer to the valence band edge).

for electrons 
$$\tau_e = \frac{\exp((E_c - E_T)/kT)}{\sigma_n v_{th} N_c}$$
 (4.10)

for holes 
$$\tau_e = \frac{\exp((E_T - E_v)/kT)}{\sigma_p v_{th} N_v}$$
(4.11)

where  $N_c$  and  $N_v$  are the effective densities of state in the conduction and valence bands respectively, k is the Boltzmann constant and T is the temperature.

For electrons 
$$v_{th} = \sqrt{\frac{3kT}{m_n}}$$
 (4.12)

$$N_c = 2 \left(\frac{2\pi \, m_n kT}{h^2}\right)^{3/2} \tag{4.13}$$

where  $m_n$  is the electron effective mass and h is Planck's constant. Similar expressions apply for holes.

If Equation (4.10) is multiplied by  $T^2$  and the factor  $(v_{th}/T^{1/2})(N_c/T^{3/2})$  is expressed as:

$$\gamma_n = \left( v_{th} / T^{1/2} \right) \left( N_c / T^{3/2} \right) \tag{4.14}$$

The emission time constant can be rewritten as:

$$\tau_e T^2 = \frac{\exp((E_c - E_T)/kT)}{\gamma_n \sigma_n}$$
(4.15)

The trap activation energy can be deduced, using equations (4.10) and (4.15), from the slope of the  $\ln(e_p/T^2)$  versus 1/T plot and the trap capture cross-section can be extrapolated from the intercept on the  $\ln(e_p/T^2)$  axis.

# 4.4 Current-voltage analysis

The current through a p-n junction is characterised by the equation:

$$I = I_0 \left( \exp\left(\frac{q(V - IR_S)}{\eta kT}\right) - 1 \right)$$
(4.16)

where  $I_o$  is the saturation current and  $\eta$  the diode ideality factor.  $V = V_d + IR_s$ , where  $V_d$  is the voltage across an ideal diode, i.e. the voltage across the space-charge region in series with any voltage drops across the p and n quasi-neutral regions (qnr),  $R_s$  is the series resistance and I is the current.



Figure 4.9 I-V curve for a forward biased diode with series resistance [1].

Figure 4.9 shows an example for current in a *p*-*n* junction diode (forward biased junction), plotted using Equation (4.16). At high currents the deviation of the log(I) vs. V curve from linearity is due to series resistance.  $R_s$  can be determined according to:

$$\Delta V = IR_s \tag{4.17}$$

For  $IR_s \gg V \gg \eta kT /q$ , the plot shows linear dependence of current on voltage. For  $V > \eta kT /q$ , at low current, the current is dominated by scr recombination and at higher current it is dominated by qnr (quasi-neutral region) recombination. Therefore, the total current is described by the following equation:

$$I = I_{0,scr}\left(\exp\left(\frac{q(V-IR_S)}{\eta kT}\right) - 1\right) + I_{0,qnr}\left(\exp\left(\frac{q(V-IR_S)}{\eta kT}\right) - 1\right)$$
(4.18)

The reverse saturation currents for any of the two regions  $(I_{o,scr} \text{ and } I_{o,qnr})$  can be determined by linear extrapolation of each region to V = 0. The ideality factor is deduced from the slope  $\left(m = \frac{d \log(I)}{dV}\right)$  as a function of the sample's temperature.

$$\eta = \frac{q}{2.3 \ kT} \frac{1}{\left(\frac{d \log(I)}{dV}\right)} \tag{4.19}$$

The thermionic current of a Schottky barrier diode is characterised by the equation:

$$I = I_{s} \left( \exp \left( \frac{q(V - IR_{s})}{\eta kT} \right) - 1 \right)$$
(4.20)

$$I = AA^*T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \left(\exp\left(\frac{q(V-IR_s)}{\eta kT}\right) - 1\right)$$
(4.21)

where  $I_s$  is the saturation current, A is the area of the diode,  $A^*$  is Richardson's constant,  $A^* = 120 \ (m^*/m)$  A cm<sup>-2</sup> K<sup>-2</sup>,  $\eta$  is the diode ideality factor, and  $\Phi_b$  is the effective barrier height.

$$\Phi_b = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_s}\right) \tag{4.22}$$

The barrier height is commonly calculated from the saturation current  $I_s$ . It can be determined by extrapolating the  $log(I_s)$  versus V curve to V = 0. The effect of series

resistance is not important in this extrapolation because the current  $I_s$  is very low. At higher currents, the value of  $R_s$  can be estimated using the same method as described for a *p*-*n* junction.

For V >> kT/q, at a constant forward bias voltage  $V = V_1$ , Equation (4.21) can be written as:

$$\ln(I/T^{2}) = \ln(AA^{*}) - q\left(\Phi_{b} - \frac{V}{\eta}\right) / kT$$
(4.23)

A plot of  $\ln(I/T^2)$  versus 1/T is called a Richardson plot, the slope of which  $-q(\Phi_b - V_1/\eta)/k$  and the intercept on the vertical axis is  $\ln(AA^*)$ . However, the extraction of  $A^*$  from the intercept is prone to error, as the 1000/T axis usually covers only a narrow range and any uncertainty in the data can produce a large error in the value of  $A^*$ . Fortunately,  $A^*$  appears in the "ln" term and an error of 2 in  $A^*$  gives rise to an error of only 0.7 kT/q in  $\Phi_b$ .

The barrier height is calculated from the slope  $\left[\frac{d(\ln(I/T^2))}{d(I/T)}\right]$ :

$$\Phi_b = \frac{V_1}{\eta} - \frac{k}{q} \frac{d(\ln(I/T^2))}{d(1/T)}$$
(4.24)

In this case *n* must be determined independently.

Accurate extraction of  $\Phi_b$  sometimes becomes impossible when both the barrier height and the ideality factor are temperature dependent and non-linear Richardson plots are observed. Linearity can be restored if  $\eta \ln(I/T^2)$  is plotted against 1/T [6].

For a well-behaved Schottky diode,  $\eta$  value is near unity. However,  $\eta$  can deviate from unity as a result of current flow due to mechanisms other than thermionic emission such as thermionic-field emission and recombination& generation. The presence of high  $R_s$ also increases the value of ideality factor,  $\eta$ .

## 4.5 Capacitance-voltage analysis

The width of a reverse-biased scr of a junction device relies on the applied voltage. The capacitance per unit area of a Schottky diode is given by

$$\frac{C}{A} = \sqrt{\frac{\varepsilon_s \varepsilon_0 q \left(N_A - N_D\right)}{2(V_{bi} - V)}}$$
(4.25)

For *n*-type semiconductors  $N_D >> N_A$ , whereas for *p*-type  $N_D << N_A$ . The built-in potential  $V_{bi}$  is related to the barrier height by the relationship

$$\Phi_b = V_{bi} + V_o \tag{4.26}$$

$$V_o = (kT/q) \ln(N_c/N_D)$$
(4.27)

where  $N_c$  is the effective density of states in the conduction band. Plotting  $1/C^2$  versus V gives a curve with the slope  $2/[q.\varepsilon_s.\varepsilon_o.(N_A - N_D)]$ , and with the intercept on the V-axis gives the intercept voltage  $(V_i)$ , as shown in Figure 4.10 (in this example  $V_i$ =0.53 V).



**Figure 4.10**  $1/C^2$  versus V plot of a diode, exhibiting an intercept voltage of 0.53 V.

$$V_i = -V_{bi} + kT/q \tag{4.28}$$

The barrier height can be determined from the  $1/C^2 - V$  curve for  $1/C^2 \rightarrow 0$  or  $C \rightarrow \infty$ indicating sufficient forward bias to cause flat band conditions in the semiconductor. The flat-band barrier height  $\Phi_{b(C-V)}$  is determined by using Equations (4.26) and (4.28)

$$\Phi_{b(C-V)} = -V_i + V_o + kT/q \tag{4.29}$$

For a Schottky barrier diode with a *p*-type semiconductor that has  $N_A$  doping density, using the *depletion approximation*, i.e. neglecting minority carriers and assuming perfect charge neutrality beyond a depth W and total depletion of majority carriers in the scr to W, the doping profiling can be obtained using the following equations:

$$N_A(W) = \frac{2}{q\varepsilon_s \varepsilon_0 A^2} \frac{d(1/C^2)}{dV}$$
(4.30)

$$W = \frac{\varepsilon_s \varepsilon_0 A}{C} \tag{4.31}$$

This approximation works reasonably well when the scr is reverse biased and when the semiconductor is uniformly doped. Further, it is known that the charges that actually respond to the ac voltage are the mobile carries (i.e. holes in this case, not the ionised acceptor ions). Hence, the differential C-V profiling measures the effective carrier density, not the doping density. That is neither the true carrier density nor the doping density. Fortunately, the effective carrier density is approximately the majority carrier density and therefore Equation (4.30) can be described as:

$$p(W) = \frac{2}{q\varepsilon_s \varepsilon_0 A^2} \frac{d(1/C^2)}{dV}$$
(4.32)

It should be noted that for a Schottky diode the width of the scr only spreads into the semiconductor; the spreading of scr into the metal is negligible. In the case of a p-n junction, Equations (4.31) and (4.32) are applicable only when one side of the junction

is more highly doped than the other side (i.e.  $p^+n$  or  $n^+p$  junction), and hence the scr spreading into the heavily doped region can be ignored. If that is not the case then these equations must be modified. Fortunately, most p-n junctions for doping density profiling, are of the  $p^+n$  or  $n^+p$  type, and therefore corrections due to doping asymmetries are not necessary.

## 4.6 Deep Level Transient Spectroscopy (DLTS)

As discussed in section 4.3, the presence of deep traps in the depletion region of a Schottky diode alter the junction capacitance; it is affected by any variation in the charge state of the deep traps, i.e. change in concentration of carriers trapped by the deep levels [1-2]. The traps that capture or emit carriers can be monitored by observing the corresponding change in the capacitance. DLTS is a powerful technique for investigating the electronic behaviour of deep levels in semiconductors. The trapping process is examined by changing the voltage applied to the junction using biasing pulse techniques. There are two types of biasing pulses, the majority carrier pulse, in which the voltage bias is pulsed from reverse voltage to zero voltage, the momentary reduction in the diode bias introducing only majority carriers into the region of observation. In the second type of biasing pulse, the injection pulse is applied either by forward biasing the device for a very short interval (this is in the case of a *p*-*n* junction) or by an optical pulse which inject both majority and minority carriers into the depletion region, this is known as O-DLTS, where the voltage bias can be pulsed from a reverse voltage to a forward voltage.

In Figure 4.11 firstly assume that a  $p^+n$  junction diode so that the depletion region is expected only to occur in the *n* side of the junction. Secondly, assume that the semiconductor contains a low concentration of defect that forms a deep electron trap with an energy level  $E_T$ . The conduction and valance bands are denoted by  $E_c$  and  $E_v$ .



**Figure 4.11** A schematic diagram describing the origin of the DLTS transient for majority carrier trap. (1) Quiescent state; (2) The filling pulse; (3) reverse bias; (4) exponential decay as carriers are emitted [7].

The unshaded area illustrates the depletion region while the *n* shaded area indicates the bulk of *n*-type semiconductor containing free carriers. At the  $E_T$  level, black dots and spaces between them indicate filled and empty traps respectively. It is assumed in the initial state (step 1) that all the trap level in the depletion region is empty and the traps in the bulk of the *n* region are filled. With the application of a fill pulse, the reverse bias across the diode is reduced. The width of the depletion region *W* is reduced while the capacitance of the diode is drastically increased, as shown in (2). As a result of the reduction in the depletion region the traps are filled up to a distance of approximately the depletion width below the surface of the semiconductor. After filling pulse duration of  $t_p$ , the reverse bias is returned to its quiescent level, as shown in (3). The increase in the reverse bias increases the width of the depletion region; some of the deep level traps in the depletion region are now filled. The filled traps in the depletion region are in this case above the Fermi level; hence, they will emit carriers since they are thermally

excited. This causes the charge density in the depletion region to increase, increasing the junction capacitance. Immediately after each pulse the rf capacitance changes by  $\Delta C$ .

Figure 4.12 illustrates the situation of a minority carrier trap (i.e. hole traps in *n*-type), an injection pulse is used to apply forward bias and hence inject both minority and majority carriers into the depletion region; since the depletion region is forward biased and the junction barrier may have collapsed [8]. The assumed hole traps in this case must have high hole capture coefficient  $c_p >> c_n$  to be filled with holes. After the filling pulse the defect states are filled with holes and the width of scr is smaller, as shown in (2). After filling pulse duration of  $t_p$ , the bias is returned to its quiescent level, as shown in (3), with emission of the trapped holes the capacitance becomes smaller and relaxes at the initial value  $C_R$ .



**Figure 4.12** A schematic diagram describing the origin of the DLTS transient for a hole trap in an n-type semiconductor. (1) Quiescent state; (2) The filling pulse; (3) reverse bias; (4) Exponential decay as carriers are emitted as a function of time [7].

It should be noticed that for majority carrier emission the capacitance increases with time whether the material is n- or p-type and whether the impurities are donors or acceptors [9]. For an n-type semiconductor, traps in the upper half of the band gap are generally observed with majority carrier pulses; those in the lower half are detected with minority carrier pulses. Midgap traps can respond to either minority or majority carrier excitation. Minority carriers can also be injected optically [1].

Basically, DLTS is a signal-processing method based on transient analysis. It is known that the power of capacitance-time transients analysis was only fully realized when automated data acquisition techniques were introduced. The first of these was Lang's dual-gated integrator or double boxcar approach [10]. In DLTS, the dual-gated signal integrator is necessary for the setting of a rate window, extracting the difference in capacitance from the transient, and averaging the signal for noise reduction. The rate window concept can simply explained by assuming the capacitance-time transients in Figure 4.13 are sampled at times  $t = t_1$  and  $t = t_2$  and that  $\Delta C$  is the difference in capacitances at t<sub>1</sub> and t<sub>2</sub>, i.e.  $\Delta C = C(t_1) - C(t_2)$ . The temperature is slowly scanned while the diode is repetitively pulsed between zero and reverse bias. A difference signal is generated, as a change in the capacitance within the preset rate window. The capacitance difference is plotted for each transient as a function of temperature; this is known as the DLTS spectrum, and it passes through a maximum when the emission rate matches the system's time constant. In DLTS plots the position of the peak (a peak for each deep level) on the temperature axis allows one to determine the fundamental parameters governing thermal emission and capture. The height of the peak is related to trap density. The majority carrier trap spectra usually are depicted with an opposite sign of peak amplitude in respect to the minority carrier trap spectra.

The DLTS signal is described by the following equation:

$$\Delta C = C(t_1) - C(t_2) = C_0 \frac{n_T(0)}{2N_D} \left( \exp\left(-\frac{t_2}{\tau_e}\right) - \exp\left(-\frac{t_1}{\tau_e}\right) \right)$$
(4.33)



**Figure 4.13** Illustration of how the DLTS signal is generated from using the double boxcar. The output is the average difference between the capacitance at time  $t_1$  and the capacitance at time  $t_2$  as a function of temperature [10].

The maximum emission time constant ( $\tau_{e,\max}$ ) is in fact the set rate window for the scan that will detect an emission rate *e* from a trap and it is obtained by differentiating Equation (4.33) with respect to  $\tau_e$  and setting the result equal to zero [1].

$$\tau_{e\max} = \frac{t_2 - t_1}{\ln(t_2/t_1)} = e^{-1}$$
(4.34)

It should be noticed that different rate windows can be used for each temperature scan by varying  $t_1$  and  $t_2$ , (i.e. it is possible to record and monitor the emission rate of a trap as function of temperature by setting different rate windows). A suitable way of doing that by varying  $t_1$  and  $t_2$  while  $\ln(t_2/t_1)$  remains constant. In this way the shape and size of the peaks on the  $\Delta C$  versus T plot will not be affected, i.e. the peaks shift with temperature with no curve shape change, making peak location easier. For every  $t_1$  and  $t_2$  gate, one value of  $\tau_e$  corresponding to a particular temperature is generated, giving one point on a  $\ln(\tau_e T^2)$  versus 1/T plot. Trap parameters such as the activation energy and the apparent capture cross-section can be deduced according to Equation (4.10).

The trap concentration  $(N_T)$  can be easily calculated from  $\Delta C_{\text{max}}$  if the hole or electron trap is completely filled due to a saturation injection pulse or a large majority carrier pulse.

$$N_T = 2\frac{\Delta C}{C} \left( N_A - N_D \right) \tag{4.35}$$

where  $N_A - N_D$  is the net ionized impurity concentrations and C is the quiescent capacitance of the junction under reverse bias conditions.

DLTS also offers the extraction of information about the carrier capture cross-section that describes the ability of the trap to capture free charge carriers. Measurements of  $\sigma$ are best achieved by varying the fill pulse duration. The application of a short fill pulse implies that the trap will not have time to fill completely while along fill pulse entails that the trap will be saturated by carriers. The capture cross-section can be determined by measuring the trap occupancy while varying the fill pulse duration. The capacitance change as a function of the fill-pulse length is best described by the following equation [10].

$$\ln\left[\frac{\Delta C_{\infty} - \Delta C_t}{\Delta C_{\infty}}\right] = \sigma_p \ v_{th} \ p \ t_p \tag{4.36}$$

where  $\Delta C_{\infty}$  is the equilibrium capacitance value,  $\Delta C_t$  is the capacitance at time *t*,  $\sigma_p$  is the trap capture cross-section, *p* is the majority carrier population,  $t_p$  is the fill-pulse duration, and  $v_{\text{th}}$  is the thermal velocity.

Equation (4.36) can be used to investigate whether deep electronic states originated from point or extended defects. In these experiments consecutive DLTS scans are performed around the peak temperature of the defect and the fill pulse length is reduced

consistently until a point is reached where the trap fails to fill the DLTS peak maximum. In the case of point defects, the majority carrier capture cross-section should obey a linear dependence on the logarithm of a combination of capacitance terms as function of fill pulse length. Deviation from this relationship provides a sensitive test for the presence of extended defects that exhibit Coulombic repulsion, because the repulsive force reduces subsequent carrier capture at the defect, i.e. this is due to the Coulomb potential that arises around the defect that prevents further carrier capture after a period of time. In this case, non-linear slope is obtained, hence the capture characteristics can not be described by Equation (4.36). Nevertheless, DLTS can still be applied to identify such defects. It has been reported [11,12] that the DLTS signal should exhibit a dependence on the logarithm of the fill pulse time when the carrier capture is into extended defects,

$$\Delta C_m \propto \ln(t_p) \tag{4.37}$$

where  $\Delta C_m$  denotes the amplitude of the DLTS signal.

### 4.7 High resolution Laplace-DLTS

Conventional DLTS has insufficient energy resolution (at best about 50 meV) to reveal information about closely spaced trap levels. A high resolution modification of DLTS, Laplace DLTS (LDLTS) [13] provides substantial increase in energy resolution over conventional DLTS. LDLTS records and digitizes the capacitance transient due to carrier emission at a fixed temperature and extracts the emission rates present in the transient by applying a mathematical algorithm. In fact, several thousand capacitance transients are averaged, which ensures that the signal-to-noise ratio is of the order of 1000, which is enough to separate transients with closely spaced emission rates. LDLTS is capable of distinguishing whether a single DLTS peak is due to emission from a unique defect or several defects closely spaced in energy. The choice of measurement temperature is usually governed by the original DLTS measurement, i.e. an optimum temperature is chosen for each deep state, which is around the maximum of the DLTS peak.

In the LDLTS software used in this work, the capacitance transients are analysed by three different inverse Laplace transform algorithms (i.e. mathematical algorithms that effectively performs an inverse Laplace transform for the recorded transient), and a plot of peak intensity as a function of emission rate produced. In LDLTS the improvement in resolution was possible by changing the filter characteristic. A common approach to the quantitative description of non-exponential behaviour in the capacitance transients is to assume that they are characterised by a spectrum of emission rates. A mathematical representation of the capacitance transients given by the following equation is the Laplace transforms of the true spectral function F(s).

$$f(t) = \int_{0}^{\infty} F(s) e^{-st} ds$$
(4.38)

where f(t) is the recorded capacitance transient.

Therefore, it is necessary to use a mathematical algorithm that effectively performs an inverse Laplace transform for the function f(t) in order to find a real spectrum of the emission rates (time constants) present in the transient. The LDLTS software offers a library of algorithms which either modified for the requirements of LDLTS or were developed specifically for this system. The three different algorithms used (CONTIN, FTIKREG and FLOG) [14-16] are based on the Tikhonov regularization method and they differ only in the way the regularizations parameters are defined. This provides a complete and comparative analysis of emission rate which increases confidence in the accuracy of the generated LDLTS spectra.

LDLTS requires the use of a highly stable cryostat and it is very important to establish accurate communication with the temperature controller, as any instability in temperature before the end of the fill pulse will affect the occupation of the traps, e.g. a stability

of  $\pm$  50 mK is required for the detection of a shallow level ~100 meV from the band edge. Any large degree of instability in temperature will introduce noise which is detrimental for accurate measurement of such a shallow trap. Further details about the specifications of the equipments and software used in this project for DLTS and LDLTS are given in the following chapter.

#### **4.8 Thermal Admittance Spectroscopy (TAS)**

In principle, the presence of a deep level in the measured rectifying junction is determined by a flexion in the capacitance-frequency (*C*-*f*) curves, and a peak in the conductance/frequency (*G*/*f*) curves that occurs at frequency  $f_0$ ; this frequency is related to the emission rate of the deep level [1,17].

$$\omega_0 = 2\pi f_0, \quad \omega_0(T) \propto e_p(T), \qquad \omega_0(T) = v_{th} \sigma_p N_v \exp\left(-\frac{E_a}{kT}\right)$$
(4.39)

where  $e_p(T)$  is the emission rate of a carrier from a deep level in a *p*-type semiconductor as a function of temperature,  $\sigma_p$  is the capture cross section of the deep level,  $N_v$  is the valence band density of states,  $v_{th}$  the thermal velocity and  $E_a$  is the energy level of the acceptors above the valence band edge. However, the response of majority carriers at a measurement frequency is limited by the dielectric relaxation time  $(\tau_{rel})$  [17]. The majority carriers can not respond to the measurement frequency (*f*) when the angular modulation frequency  $\omega=2\pi f$  exceeds  $1/\tau_{rel}$ . The C-*f* and *G*/*f* curves should shift towards higher/lower frequencies by increasing/decreasing the measurement temperature, and hence it is possible to evaluate the dependence of the defect emission rate on temperature. The equivalent circuit of a *p*-*n* junction or a Schottky diode is a junction capacitance (*C*) in parallel with a junction conductance (*G*) (which governs the leakage current) and a series resistance ( $R_s$ ) (which depends on bulk resistivity and on contact resistances), as shown in Figure 4.14.



Figure 4.14 The actual equivalent circuit for a *p*-*n* or Schottky diode.

The complex impedance (Z) of the circuit is given by

$$Z = R_{s} + \frac{G - j\omega C}{G^{2} + (\omega C)^{2}} = Re\{Z\} + Im\{Z\} = \left[R_{s} + \frac{G}{G^{2} + (\omega C)^{2}}\right] - j\left[\frac{\omega C}{G^{2} + (\omega C)^{2}}\right]$$
(4.40)

where  $Re\{Z\}$  and  $Im\{Z\}$  are respectively the real and imaginary components of the complex impedance. The general equation defining the measured complex admittance (Y) is given by [1]:

$$Y = \frac{1}{Z} = \left[\frac{G(1 + R_s G) + R_s(\omega C)^2}{(1 + R_s G)^2 + (\omega R_s C)^2}\right] + j\left[\frac{\omega C}{(1 + R_s G)^2 + (\omega R_s C)^2}\right]$$
(4.41)

and the admittance is also defined as:  $Y = G_m + j\omega C_m$  (4.42)

$$G_{m} = \left[\frac{G(1+R_{s}G)+R_{s}(\omega C)^{2}}{(1+R_{s}G)^{2}+(\omega R_{s}C)^{2}}\right], \quad C_{m} = \left[\frac{C}{(1+R_{s}G)^{2}+(\omega R_{s}C)^{2}}\right]$$
(4.43)

where  $C_m$  and  $G_m$  are the measured capacitance and conductance respectively.

For reasonably good junction devices, the condition  $R_sG \ll 1$  is generally satisfied. Lowering the frequency reduces the second term in the denominator to less than one and the true capacitance is determined. Then the frequency is raised until the second term dominates, and  $R_s$  can be calculated with all other quantities known. Unless the effect of the series resistance is not negligible, the imaginary component of the measured admittance is directly proportional to the depletion capacitance, i.e. if  $(R_sG \ll 1)$  and  $(R_s \ll 1/(\omega C))$ , then  $C_m = C$ . However, for large  $R_s$  and G values ( $R_s > 1 k\Omega$  and  $G \approx$  $10^{-5}$  S), the measured capacitance should be corrected using the above equations. Therefore care must be taken if the directly measured  $C_m$  is used to obtain the built-in voltage  $(V_{bi})$  and impurity concentration. It is reported [18] that analysis of  $C_m$  vs. V data suggests that the extrapolated  $V_{bi}$  value increases with increasing frequency. This implies that extrapolating the  $V_{bi}$  from a plot of  $1/C^2$  vs. V is not always valid; there may not be a unique gradient. It is therefore advisable to investigate the measured capacitance as a function of dc bias, frequency and temperature. The series resistance can be either estimated from the I-V curves [19] for each temperature or by constructing a Nyquist plot from complex impedance measurements [18,20], as function of bias, frequency and temperature, where  $R_s$  equals the saturation value in the measured real part of the impedance.

It is worth mentioning that in the TAS experiments (*G*/ $\omega$  vs. *T*), the conductance data can be recorded using a stable temperature scan rate at a fixed probing frequency for each experiment; this in principle is similar to the DLTS experiments [17].

It is possible to directly use the conductance peaks occurring at each temperature to construct an Arrhenius plot and hence  $E_a$  and the apparent  $\sigma$  of each defect can be deduced according to the standard equation [21]:

$$\frac{2\pi f}{T_{max}^2} \propto exp\left(-\frac{E_a}{kT_{max}}\right)$$
(4.44)

where  $T_{max}$  is the temperature at which the conductance peak is occurring and f is the probing frequency for each experiment. A plot of  $ln(\omega/T^2)$  vs. 1/T should give a straight line the slope of which corresponds to  $E_a$  and the intercept is related to  $\sigma$ .

#### **4.9** Conclusions

This chapter described the necessary theoretical background associated with device physics of junction diodes. An overview of capacitance-voltage and current voltage analysis were provided for both p-n and Schottky barrier junctions. This chapter also discussed the occupancy of the electrically active traps in semiconductors by majority or minority carriers in light of the mentioned junction devices. In addition, the techniques used for studying deep defect levels such as Deep Level Transient Spectroscopy (DLTS), Laplace-DLTS and Thermal Admittance Spectroscopy were briefly described. The theory of these experimental tools was discussed together with the necessary equations for the extraction of significant trap parameters in semiconductors.

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# 5. Experimental Setup

#### 5.1 Introduction

As discussed in chapter 4, it is essential to use sensitive tools for characterising deep level defects in semiconductors. The high frequency (1 MHz) transient capacitance techniques, deep level transient spectroscopy (DLTS) and the high resolution Laplace DLTS (LDLTS), have proved to be useful experimental tools to probe deep and shallow level defects. Thermal admittance spectroscopy (*TAS*), in which the conductance of a Schottky or a p-n junction is monitored as a function of temperature, is also used to verify the existence of electrically active defects (charge carrier traps) within the bandgap of a material. These experimental techniques allow for the calculation of fundamental defect parameters and measure their concentration in the material.

This chapter starts with a description of the DLTS and LDLTS experimental setup used in this study; it also provides information about the LDLTS software used. The second section presents the setup used for carrying out thermal admittance spectroscopy experiments and also for measuring capacitance-voltage (C-V), as a function of temperature. Further, it illustrates the current-voltage (I-V) system and describes how these instruments are connected and also controlled via LabView applications.

Finally, this chapter provides a brief description for the supplementary techniques used in this study namely Raman spectroscopy and scanning electron microscopy (SEM).

### **5.2 DLTS and LDLTS experimental setup**

#### 5.2.1 The Hardware

Figure 5.1 shows a schematic diagram for the DLTS and LDLTS systems used in this study. The setup used for the DLTS and LDLTS measurements consisted of the following hardware elements:


Figure 5.1 Schematic diagram of the DLTS and LDLTS systems used in this study.

#### 5.2.1.1 Acquisition and pulse generator card

This interface card is the most vital hardware element; it is connected to a PC dedicated for Laplace DLTS experiments, and is used for data acquisition and sample biasing and pulsing; as in this system no external pulse generator is used. This card has an internal pulse generator for supplying a filling pulse to the sample followed by a constant quiescent reverse bias during which the capacitance of the sample is observed. Two types of data acquisition and pulse generator card are available within the DLTS facility at Sheffield Hallam University (SHU). The first one is the transient processing card (known as the UMIST card), this was developed at the University of Manchester, with the following specifications: Input voltages:  $\pm 5$  V, resolution: 16-bit, maximum sampling frequency: 200 kHz, output voltages:  $\pm 10$  V and pulse widths from 20 ns. The other card is a National Instruments PCI-6251 together with a NI I/O SCB-68 connector box, with the following specifications: Input voltages:  $\pm$  10 V, resolution: 16-bit, maximum sampling frequency: 2 MHz, output voltages:  $\pm$  10 V and pulse widths from 0.5  $\mu$ s.

#### 5.2.1.2 GPIB interface card

To get the applications up and running fast, a National Instruments (NI) GPIB card for PCI interface is used. GPIB cables and connectors (IEEE 488 Bus) are used to establish fast communication between the system instruments via defined GPIB addresses (individually defined using the I/O software interface).



**Figure 5.2** A photograph of the vacuum systems used for DLTS at SHU. Two heads are available: (10-450) K and (15-800) K.

## 5.2.1.3 Temperature controller

A Lakeshore-340 temperature controller is used for controlling the set point temperature or temperature scans of the measurements. The system uses two different sensors, either a silicon sensor (10-450) K or a platinum sensor (15-800) K, to measure the sample temperature inside the vacuum chamber, and the temperature is also monitored nearer the cold head. The output of the sensors is fed back to the temperature controller in order to maintain the appropriate rate of temperature change during measurements.

## 5.2.1.4 Cryostat and sample holder

An Advanced Research Systems (ARS) 4HW Cryostat connected to an Edwards pump for pumping the system to vacuum is used, as shown in Figure 5.2. The pressure of the sample chamber is monitored using an Edwards ADG high vacuum indicator.



Figure 5.3 Photographs of the sample holder inside the closed-cycle liquid He cryostat.

The sample is mounted on a cold finger in the closed-cycle liquid Helium cryostat which is capable of operating in the selected temperature range. Figure 5.3 shows some photographs of the sample holder inside the vacuum chamber.

#### **5.2.1.5** Capacitance meter

A Boonton 72B capacitance meter (1 MHz) was used for capacitance-voltage (C-V) and DLTS measurements, which monitors thermal emission after excitation by an electrical pulse.

#### 5.2.1.6 Oscilloscope

An Agilent DSO6104A Oscilloscope was used to monitor the filling pulse to be supplied to the sample.

#### 5.2.2 The Laplace DLTS Sofware

The Laplace DLTS software used in this work was first developed in 1993 by L. Dobaczewski, I. D. Hawkins and A. R. Peaker, who were awarded a UK National Physical Laboratory prize for this invention; this was followed by a Royal Academy of Engineering Foresight Award in 1997 [1]. Laplace DLTS has been subsequently developed through several research projects funded by the European Union, the Polish Ministry of Science and Higher Education and by the Engineering and Physical Sciences Research Council, UK.

The graphical user interface (GUI) of the software enables the user to choose the measurement mode and scan parameters, for example, using single temperature scan, simultaneous 9-rate windows measurements, or multiple temperature scans with 2 rate windows each (based on the TrapView software). The software also allows the user to set the biasing conditions for every experiment and to choose the sample pulsing mode, for example, single pulse, double pulse for the electric field dependence and trap profiling, injection pulse for carrier recombination processes analysis, or minority carrier transient spectroscopy. In addition the software controls the hardware, for example, it is easy to set the parameters for the temperature controller and set up the

excitation and acquisition parameters. Further, it performs preliminary analysis of the time constant and creating the noise histogram. The software stores the large amounts of experimental data and all parameters that describe each measurement in a database system, and then readily manipulates the data. The database system runs in the back-ground of the measurement process, records experimental data and when the measurement is done it enables the user to extract, compare and visualise recorded data.



**Figure 5.4 (a)** A capacitance transient **(b)** a spectrum obtained from the capacitance transient using three different algorithms.

It is important to minimize the effect of noise on measurements because the capacitance transient is very small. Therefore, instead of taking a single point, the capacitance measurements are usually averaged over thousands of transients. For numerical calculations, the LDLTS software uses three mathematical algorithms; CONTIN [2], FTIKREG [3] and FLOG [1]. The trap relaxation process is measured as a capacitance transient, as shown in Figure 5.4, then using these algorithms it is converted from the time domain into a spectrum of carrier emission rates in the frequency domain.

Laplace Deep Level Spectroscopy provides an increase in energy resolution over conventional DLTS of an order of magnitude. The use of three different algorithms in parallel substantially increases the level of confidence in the spectra obtained. Additionally, for preliminary data analysis a discrete deconvolution method can be used, this method is based on a simple integration procedure [4].





Figure 5.5 demonstrates the improvement in energy resolution possible with LDLTS. The main plot shows a measurement of a Si:Au sample using Laplace DLTS, whereas the inset shows the DLTS spectrum of the same defect. It is clearly evident in LDLTS there are two distinct defects; one of these has been found to be due to substitutional gold the other to a gold-hydrogen complex [5]. However, these peaks can not be resolved using DLTS.

## 5.3 Thermal Admittance Spectroscopy and *I-V* experimental setup

The vacuum system used in the admittance spectroscopy and I-V setup is similar to the one described above (used for DLTS). Figure 5.6 shows a schematic diagram for the systems used in this study.



Figure 5.6 Schematic diagram of the TAS and I-V systems used in this study.



Figure 5.7 A photograph of the setup used for TAS and *I-V* systems at SHU.

## 5.3.1 Agilent LCR meter E4980A

A precision LCR meter is used for evaluating semiconductor devices over a wide range of frequencies (20 Hz to 2 MHz) and test signal levels 0.1 mV to 20 V, and 50  $\mu$ A to 200 mA.

The E4980A's list sweep function permits entry of up to 201 frequencies, test signal levels, or bias level points to be automatically measured. Such an LCR meter is sometimes needed before performing DLTS measurements when a sample conductance has to be known or to find out whether the measurement has to be performed with a test frequency other than 1MHz. This system is also used to carry out C-V and capacitance-frequency (C-f) measurements.

Labview programs have been developed locally to automate the different measurements and to enable the user to select different parameters using a friendly graphical user interface. Once a single measurement is executed the data are recorded and subsequently saved in a predefined disk location on the system. Hardware drivers have been configured to establish automatic connection between the E4980A, the temperature controller and the PC using the GPIB interface.

#### 5.3.2 Cryostat and sample holder

The cryostat and vacuum system is similar to the one discussed above. The sample is mounted on a finger in the closed-cycle liquid Helium cryostat which is capable of operating in the range 10 - 450 K.

#### 5.3.3 Current-voltage experimental setup

A Keithley 6487 Picoammeter/Voltage Source is used for *I-V* experiments, it provides higher accuracy and fast rise times, as well as a damping function for use with capacitive devices. With eight current measurement ranges and high speed auto-ranging, this instrument can measure currents from 20 fA to 20 mA. It performs measurements at speeds up to 1000 readings per second and provides a voltage source from 200  $\mu$ V to 500 V.

An application program (developed by a former SHU student) based on LabVIEW software was used in this study to carry out the current-voltage-temperature (I-V-T) experiments. This application is provided with a graphical user interface which confirms that the connection with the instruments has been automatically initialised via predefined GPIB addresses. It enables the user to select a voltage sweep, plot the corresponding currents, and store the recorded data on the user's folder.

## 5.4 Supplementary techniques used for this work

#### 5.4.1 Raman Spectroscopy

Raman Spectroscopy is a technique that can be used to study solid, liquid and gaseous samples. The Raman technique is named after the Indian scientist Sir C. V. Raman who was the first to observe in practice the inelastic scattering of light in 1928, he won the Nobel Prize in Physics in 1930 for this discovery [6].

Raman Spectroscopy relies on the inelastic scattering of photons by a substance. Usually the source of light is a laser in the near infrared, visible or UV. This inelastic scattering is observed as a shift in the frequency of the scattered light relative to the excitation wavelength. The Raman shift gives information about the vibrational, rotational modes and other low frequency transitions in the system. Therefore, this technique provides unique spectra (containing information about chemical composition and structure) for each specific compound.



Figure 5.8 Schematic diagram of the Raman spectrometer [7].

The basic setup of a Raman spectrometer is outlined in Figure 5.8. The excitation laser beam is directed into the spectrometer via an array of mirrors; the beam is passed through a set of optics to set the profile of the beam. The power of the laser illuminating the sample is controlled by a set of neutral density filters. The beam is passed through a line filter (with specific wavelength) that removes any plasma lines from the laser to ensure a monochromatic source. The beam is focused onto the sample as it is reflected into a microscope. The scattered light is collected back into the spectrometer and passed though a notch filter to remove the intense Rayleigh-scattered radiation, leaving the weaker Raman-scattered light. Another set of optics is used to focus the Ramanscattered light before diffraction grating separates the different wavelengths. Finally, the different wavelengths are then detected by a CCD camera (charge-coupled device) connected to a PC running the Raman software. The software is also used to set the Raman measurement parameters, such as scanning range, exposure time and number of accumulations.

The Raman Spectroscopy setup used in this study is a Renishaw RM2000, it is a multiwavelength system with three different excitation sources; 785 nm diode laser, the 514.5 nm line of an Ar+ laser, and the 325 nm line of a HeCd laser.

#### 5.4.2 Scanning Electron Microscopy

The scanning electron microscope (SEM) uses a high-energy beam (up to 40 keV) of electrons to produce an image. The beam of electrons is focused by electromagnetic lenses on to the specimen and rastered over the surface to build up an image. The electrons interact with atoms at and near the surface of the specimen producing signals that contain information about the specimen's surface topography, grain structure, grain size, composition, and other properties such as electrical conductivity. The SEM is capable of much higher resolution than conventional optical microscopes due to the short wavelength of the electron beam. Resolutions of less than 1 nm are possible with modern machines. Most SEMs require a high vacuum throughout the chamber and an electrically conductive sample. More recent developments have involved the use of pressure limiting apertures in the column enabling a low pressure of an imaging gas to be maintained in the specimen chamber whilst keeping high vacuum conditions at the gun. This enables the study of non-conducting or vacuum-sensitive materials. Since its development in the early 1950's, SEM has opened up new areas of research in physical and medical sciences.



Figure 5.9 Schematic diagram of a scanning electron microscope [8].

In a typical SEM, as illustrated in Figure 5.9, a beam of electrons is emitted from an electron gun (either thermionic or field emission) [9]. The electron beam, with energy ranging from 50 eV to 30 keV, follows a vertical path through the microscope. The beam passes through electromagnetic fields and lenses which focus the beam down toward the sample. As soon as the beam hits the sample, electrons and X-rays are ejected from the sample; detectors are used to collect the X-rays, secondary or backscattered electrons, and convert them to a signal that is used to produce an image.

The SEM setup used in this study is The FEI Nova<sup>™</sup> Nano SEM. This system offers high resolution (~1 nm) in high vacuum mode with accelerating voltage of 15 kV. Small

and large samples can easily be accommodated inside the large chamber on high precision and high stability stage.

# 5.5 Conclusions

This chapter firstly presented the experimental setups used for electrical characterisation of devices in this work. These included *C-V*, *I-V*, *DLTS*, *LDLTS* and admittance spectroscopy setups. Details of instruments connectivity and used software in each setup were also provided.

Finally, basic description was given for the Raman spectroscopy and SEM techniques that were used in this work to provide supplementary information about the quality of the grown thin films.

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# 6. Materials growth, Characterisation and Device fabrication

## 6.1 Introduction

Two different materials and different sets of samples were investigated in this thesis, using the electrical techniques explained in chapter 5. The first set of data is associated with the electrical characterisation of defects in B-doped polycrystalline diamond films grown on  $p^+$  silicon substrates. In this work, hot-filament Chemical Vapour Deposition (CVD) and Microwave Plasma-Enhanced CVD methods were employed to grow diamond thin films. The diamond films were grown by Prof. P. W. May at the University of Bristol. This chapter provides details of the growth conditions, contact formation and characterisation for semiconducting diamond thin films. It also discusses the deposition of several types of Schottky contacts on polycrystalline diamond.

The second part of this chapter is associated with a description of the growth of Mgdoped GaN films grown by MOVPE on sapphire substrates. Details of the processing of Schottky diodes on these films have also been provided. The aim of forming electrical contacts on GaN was to investigate the effect of threading dislocation density (TDD) on electrically active defects in Mg-doped GaN films using DLTS and/or admittance spectroscopy. The GaN thin films described in this chapter were grown by Dr. M. Kappers at the University of Cambridge.

Finally, details of the sheet resistance, the estimated doping concentrations and the Raman characterisation of the as-grown thin films are also provided in this chapter.

## 6.2 Specifications of the diamond thin films

#### 6.2.1 Substrate and nucleation layer

Silicon is the most commonly used substrate for depositing CVD diamond because of various considerations; it has the same crystal structure as diamond, a high melting point (1683 K), relatively low thermal expansion mismatch coefficient with diamond and the

ability to form a carbide layer on the substrate surface to which the carbon-containing species in the gas phase can bond to and hence form CVD diamond.

The substrate for all the diamond samples reported in this chapter was single crystal (100) Si (B-doped, p+, resistivity  $\approx 0.01$ -0.02  $\Omega$  cm), cleaved into 0.5 or 1 cm<sup>2</sup> squares. Since nucleation on the substrate is necessary for the growth of the diamond film, the silicon substrate was manually abraded prior to deposition using 1–3 µm diamond grit, to facilitate the diamond nucleation, and then cleaned with isopropyl alcohol (IPA). Before diamond film deposition the substrate was positioned on a resistive heating unit inside the vacuum chamber. A current of 4 A was passed through the heater, increasing the temperature of the substrate to ~400°C to remove any adsorbed impurities such as water.

#### 6.2.2 Growth conditions of B-doped Hot Filament CVD diamond films

Ten polycrystalline diamond films were deposited on p-type Si substrates using hot filament CVD (HFCVD). Sample OS-a1, which was not intentionally doped, was grown in a B-free reactor. This is because B is known to diffuse into the sidewalls and components within a reactor, and then diffuse out again during later growth runs, inadvertently introducing B into the gas mixture and causing unwanted doping of any growing film [1].

The gas mixture used was high purity  $H_2$  (200 sccm), CH<sub>4</sub> (2 sccm) with diborane (B<sub>2</sub>H<sub>6</sub>) as a variable source of boron. These gases were metered into the chamber via mass flow controllers with the process pressure maintained at 20 torr. Rhenium was used for the filament material since Re does not act as a sink for carbon or boron species. The filament coil was suspended ~5 mm above the Si substrate and a current of 6.75 A passed through it ( $V_{ac}$  ~20 V) for the duration of the deposition run, usually 6-8 hours, yielding a film thickness of 3-4 µm. The estimated filament temperature was ~2000°C and the estimated Si surface temperature (combined heat from filament and substrate heater) was ~900°C.

#### 6.2.3 Growth conditions of B-doped Microwave Plasma-enhanced CVD films

Three boron-doped polycrystalline diamond films were deposited on heavily borondoped Si substrates using a 1.5 kW ASTeX (2.5 GHz) microwave plasma-enhanced (MWP) CVD reactor with a water-cooled, double-walled chamber containing a Mo substrate holder. The Si substrates were manually abraded prior to the deposition run, cleaned and then placed on an alumina plate and raised ~1 mm into the plasma, with the result that the substrate attained a temperature of ~900°C, as measured by two colour optical pyrometry. The gas mixture used was high purity H<sub>2</sub> (200 sccm), CH<sub>4</sub> (2 sccm) with diborane (B<sub>2</sub>H<sub>6</sub>) as a variable source of boron, using microcrystalline diamond (MCD) conditions [2], and the deposition time was 1.5 h.

Batch	Sample	Growth Method	Deposition run (hour)	<b>4-pt probe -</b> resistance (Ω)	B-concentration (cm <sup>-3</sup> )
	OS-a1		6	50 K	Undoped
A	OS-a2	HF-CVD	6	121	$\sim 2 \times 10^{20}$
	OS-a3		6	38	$\sim 8 \times 10^{20}$
	OS-a4		6	35	~9×10 <sup>20</sup>
	OS-a5		6	42	~6×10 <sup>20</sup>
В	OS-b1	MWP-CVD	1.5	43	$\sim 6 \times 10^{20}$
	OS-b2		1.5	1.8 K	~8×10 <sup>18</sup>
	OS-b3		1.5	Out of range	ge (highly doped)
	OS-c1		8	1.75 K	~8×10 <sup>18</sup>
С	OS-c2	HF-CVD	8	1.35 K	~2×10 <sup>19</sup>
	OS-c3		8	450	~8×10 <sup>19</sup>
D	OS-d1 UE CVD		8	1.5 K	~1.5×10 <sup>19</sup>
	OS-d2	пг-Сур	8	950	~4×10 <sup>19</sup>

Table 6.1	Details of	all as-grown	CVD-diamond films.
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An estimation of the B content was made for each film by comparison with a calibration graph of 4-point probe resistivity measurements against B-content measured by SIMS [2]. This procedure gives the total B content in the film, which may be higher than the concentration of electrically active B due to compensation or segregation, as mentioned earlier. Table 6.1 details the polycrystalline diamond films, as grown in four batches.

## 6.2.4 SEM results of boron doped CVD-diamond films

Figure 6.1 illustrates that in sample OS-b3 nucleation on the substrate did not take place and hence deposition of diamond film was unsuccessful. However this could be due to the silicon substrate not being abraded prior to deposition, to facilitate the diamond nucleation. This film is therefore not discussed further.



Figure 6.1 Electron micrograph of sample OS-b3, scale is shown for 1 µm.

The rest of the polycrystalline films were of thickness  $3\sim4 \mu m$ . Figure 6.2 shows typical scanning electron microscope (SEM) images of the boron-doped CVD diamond films. The film morphology was microcrystalline with facetted crystallites averaging  $\sim1 \mu m$  in size, uniformly deposited with good reproducibility from film to film.



**Figure 6.2** Electron micrographs of different HF-CVD diamond films, scales are shown for (a) 1  $\mu$ m, (b) 5  $\mu$ m and (c) 50  $\mu$ m. The SEM with low magnification is to show the uniformly deposited films.

### 6.2.5 Raman spectroscopy to determine crystal quality

Laser Raman Spectroscopy (LRS) is a widely used technique to identify the characteristic energies of the chemical bonds; it can also distinguish between different phases within the same material.

The Raman spectrum of natural diamond shows a sharp, single peak centred at a wave number of approximately 1332 cm<sup>-1</sup> [3]. This feature also dominates the Raman spectra of high quality, polycrystalline diamond films grown by CVD methods [2-3], see Figure 6.3. CVD diamond films mostly consist of small diamond crystallites surrounded by graphitic/amorphous carbon grain boundaries. These boundaries produce additional peaks in the Raman spectrum that can help identify the crystallite size and overall quality of the diamond sample.



Figure 6.3 Raman spectrum of a microcrystalline diamond, taken at 325 nm [3].

However, peaks may be observed in the spectra which are characteristic of non-diamond contamination, depending on the deposition conditions (such as films grown with high methane concentration in gas phase). The Raman spectrum of graphite shows a broad

feature centred on 1575 cm<sup>-1</sup>, called the G peak [3]. The relative intensity of the diamond peak to the intensity of the G peak is often used as a crude measure of the phase purity of CVD diamond. However, when characterising CVD diamond films, the observation of any broad resonance at higher wave numbers is generally taken to indicate the presence of graphite-like non-diamond phases containing sp<sup>2</sup>-bonded carbon atoms.

In this work, the quality of the diamond films was verified by Raman spectroscopy. The presence of polycrystalline diamond in all films was confirmed. Figure 6.4 and Figure 6.5 show laser Raman spectra for samples OS-a2 to OS-a5, which were obtained at room temperature using a Renishaw 2000 spectrometer and were obtained with a green excitation source of 514 nm wavelength derived from an  $Ar^+$  laser.



Figure 6.4 Raman spectra for samples OS-a2 and OS-a5, taken at 514.5 nm.

Figure 6.4 shows that samples OS-a2 and OS-a5 each present a sharp peak centred at 1332 cm<sup>-1</sup>, corresponding to a  $sp^3$ -bounded structure [2-4]. This diamond peak shifts to lower wavenumber with increasing B content, and the line shape becomes asymmetric, as shown in Figure 6.5. The large Si line at 520 cm<sup>-1</sup> generally decreases in intensity

with B concentration as the film becomes darker and less transparent to the green laser light. The large feature around  $900-1000 \text{ cm}^{-1}$  is the second order from this intense Si line.



Figure 6.5 Raman spectra for samples OS-a3 and OS-a4, taken at 514.5 nm.

The broad feature at 1225 cm<sup>-1</sup> increases with B concentration and dominates the spectrum at high B content [4]. The G band is evident at low B concentrations, but is not very intense, and at higher B concentrations, as the film achieves metallic conductivity (OS-a3 and OS-a4), it disappears. This does not imply that there is less graphite in these films, only that the G band signal is hidden beneath those from the other more dominant nearby features. The peak at ~1150 cm<sup>-1</sup> maybe characteristic of nano-phase diamond or could be due to  $sp^2$  carbon species at grain boundaries [5]. This is weakly present for the undoped film, but it increases with B concentration, suggesting that B promotes the incorporation of  $sp^2$  carbon species, possibly at grain boundaries. At even higher B concentrations, this peak is hidden beneath the 1225 cm<sup>-1</sup> peak.

Figure 6.6 shows a laser Raman spectrum for sample OS-a1, which was obtained at room temperature using a Renishaw 2000 spectrometer and was taken using green

excitation 514 nm wavelength (Ar<sup>+</sup>). The undoped film exhibited a large rising photoluminescent (PL) background. This PL background decreases markedly with trace amounts of B doping, and it almost disappear for B contents >  $8 \times 10^{18}$  cm<sup>-3</sup> giving a flat baseline. The reason for this is attributed to the fact that B is compensating the nitrogen-related defects within the diamond that give rise to the majority of the PL [2].



Figure 6.6 Raman spectrum for sample OS-a1, taken at 514.5 nm.

Figure 6.7 shows laser Raman spectra for samples OS-d1, OS-d2 and an un-doped film, which were obtained at room temperature using a Renishaw 2000 spectrometer and were taken using UV 325 nm excitation (HeCd).

P. May *et al.* [2] have investigated the variations in Raman spectra of B-doped diamond films as a function of B content, publishing a large amount of data for microcrystalline diamond (MCD). In samples OS-d1 to OS-d2, the diamond peak decreases in intensity with increasing B content, as previously reported [2]. The G band is apparent with a peak at about 1585 cm<sup>-1</sup> due to crystalline graphite impurities. Notably, the broad peak

usually seen on the visible Raman spectrum at  $\sim 1225 \text{ cm}^{-1}$  is absent from the spectrum of OS-d2. Wang *et al.* [4] reported that the peak located at  $\sim 1225 \text{ cm}^{-1}$  cannot be detected when it is excited by the UV lasers even in a highly doped sample.



**Figure 6.7** Raman spectra for the different boron-doped MCD films using UV (325 nm) excitation. Features below 700 nm were not visible due to the cut-off filter used to remove the UV laser line.

#### 6.2.6 Fabrication of Schottky diodes on the diamond films

Usually after CVD diamond growth, the surface of the diamond is hydrogen terminated since the surface is an abrupt ending of growth and unsatisfied dangling bonds are present. However, hydrogen causes surface conductivity and as a result reduces the current passing through the bulk semiconductor because the conducting surface presents an alternate conducting path [6]. Therefore, the diamond surface requires oxygen passivation (e.g. oxygen plasma) resulting in the removal of conductive H surface states before electrical contacts are made.

## 6.2.6.1 Batches A, B and C

The process for making Schottky contacts on B-doped films in batches A, B and C was as follows: the films were degreased using trichloroethylene followed by acetone and the samples were then stored in methanol. The films were immersed in a solution of NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (1:1:5) for 10 minutes at 70°C, to remove metallic impurities, and subsequently rinsed in deionised (DI) water. The films were then dipped in a solution of HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (1:1:6) for 10 minutes at 70°C, to remove any organic impurities, and rinsed in DI water. The diamond surface was passivated using a RT Oxygen plasma asher (5 to 10 seconds only). Subsequently, Al dots of 1 mm in diameter were evaporated through a shadow mask on to the diamond surface to produce rectifying Schottky contacts. Before the fabrication of the Ohmic contact on the back of the p-type Si substrate, the diamond surface and sides of the film were protected with hydrofluoric acid (HF)-resistant wax/photo resist to minimise H-contamination during the processing of the back contact. The films were dipped for a few seconds in hydrofluoric acid (buffered HF) solution, to remove the native oxide layer from the silicon, and then rinsed in DI-water and blown dry with N2. It was then stored under methanol (to prevent surface oxidation) prior to the evaporation of an Al layer on the back of the  $p^+$ -Si.





Figure 6.9 shows a micrograph of processed Schottky diodes (1 mm in diameter) on one sample, bonded to gold pads mounted on ceramic.



**Figure 6.9** Schottky diodes (dots of 1 mm in diameter) on one sample, bonded to gold pads mounted on ceramic.

#### 6.2.6.2 Batch D

The diamond films OS-d1 and OS-d2 were degreased using trichloroethylene followed by acetone; the samples were then immersed in a saturated solution of  $H_2SO_4$  and  $HNO_3$  acid at around 200°C for 20 min to remove any graphitic layers and to Oterminate the surface. The films were subsequently annealed in vacuum at 750°C for 30 minutes. Schottky contacts (1-mm-diameter dots) were formed on the oxidized diamond surface with Al deposited by thermal evaporation through a patterned mask; there were about 8 Schottky devices on each  $0.5 \times 0.5$  cm<sup>2</sup> sample. Al Ohmic contacts were evaporated on the Si back surface, as described in section 6.2.6.1.

The diamond samples were mounted on ceramic and then each of the Schottky contacts was bonded to a gold pad on the ceramic. The back contact was also bonded to a contact pad.

## 6.3 Specifications of the Mg-doped GaN films

#### 6.3.1 Substrate and buffer layer

The thin films discussed in this section were grown on (0001) sapphire substrates. Two different buffer layer schemes between the film and the sapphire substrate were used, giving rise to differing threading dislocation densities (TDDs) in the film. Buffer scheme A consisted of a 2  $\mu$ m thick layer of AlN grown at 1130°C on the sapphire, followed by a 1.0  $\mu$ m thick not-intentionally-doped (NID) GaN layer at 1020°C. Buffer scheme B consisted of a 30 nm GaN nucleation layer deposited at low temperature (540°C) on the sapphire, followed by a 1.5  $\mu$ m layer of NID GaN buffer layer grown at 1005°C.



**Figure 6.10** Schematic diagrams of Mg doped GaN thin films: (a) structure A, (b) structure B.

#### 6.3.2 MOVPE growth conditions of the Mg doped GaN wafers

Four Mg doped GaN wafers were grown in a Thomas Swan close-coupled showerhead metal-organic vapour phase epitaxy (MOVPE) reactor using (0001) sapphire substrates. Two buffer layer schemes were used in this study, as discussed above. In all cases a 0.5 µm thick layer of Mg-doped GaN was grown on top of the buffer. The GaN growth

mode was quasi-two-dimensional in order to avoid unintentional n-type doping during early stages of the GaN epilayer growth [7,8]. The reactor pressure was 100 torr, the V-to-III ratio was 1420 and the growth temperature for the Mg-doped GaN was 1020°C. One wafer (C4022B) was subsequently grown using buffer scheme A, and three wafers (C4039B, C4052C and C4041B) were grown using buffer scheme B and different Mg precursor fluxes. These were annealed in the growth reactor for 20 minutes at 780°C in a nitrogen atmosphere to activate the carriers. Details of the Mg precursor flux are given in Table 6.2.

## 6.3.3 Characterisation of the Mg doped GaN thin films

The Mg concentrations in selected films (C4039B and C4022B) were quantified as  $\sim 1 \times 10^{19}$  cm<sup>-3</sup> by secondary ion mass spectrometry (SIMS) performed by Loughborough Surface Analysis Ltd. using O<sub>2</sub><sup>+</sup> primary ion bombardment and positive secondary ion detection to optimise the sensitivity to magnesium. Atomic Force Microscopy (AFM) experiments revealed a TDD of  $(2\pm1)\times10^9$  cm<sup>-2</sup> in film C4022B (structure A), whereas in structure B the TDD was  $(1\pm0.1)\times10^{10}$  cm<sup>-2</sup> using the method described in [9]. The AFM experiments were carried out by Dr. R. A. Oliver at the University of Cambridge. These measurements were performed in intermittent contact (IC) mode using a Veeco Dimension 3100 microscope equipped with a Nanoscope V controller. Veeco RTESP tips with a nominal apex radius of 8 nm were used.

For Hall effect experiments, indium bump contacts were deposited in a Van der Pauw configuration. The Van der Pauw resistances were measured on a home-built set-up involving an HP relay and DVM box (HP3497A), a programmable current source (Keithley 220), a PC and an electromagnet with a magnetic flux density of 0.2 T at the centre of the pole gap. The Hall effect data measured at room temperature are given in Table 6.2, and are the average of four measurements made at different positions for each wafer, as illustrated in Figure 6.11. The above mentioned experiments were carried out at the University of Cambridge in collaboration with Prof. C. Humphreys' group.

Wafer No. / buffer scheme	Mg precursor flux (µmol/min)	TDD (cm <sup>-2</sup> )	Sheet resistance (kΩ/□)	Hall mobility (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	hole concen- tration (cm <sup>-3</sup> )
C4022B Structure A	0.87	(2±1)×10 <sup>9</sup>	144.5	12.5	0.7×10 <sup>17</sup>
C4039B Structure B	0.87	(1±0.1)×10 <sup>10</sup>	144.3	9.3	0.9×10 <sup>17</sup>
C4052C Structure B	0.67	(1±0.1)×10 <sup>10</sup>	118.8	14.5	0.7×10 <sup>17</sup>
C4041B Structure B	0.43	(1±0.1)×10 <sup>10</sup>		Out of range	

Table 6.2 Sample growth details, AFM and room temperature Hall effect results.



Figure 6.11 Hall sample position on wafer.

## 6.3.4 Raman spectroscopy results

Room temperature Raman spectroscopy experiments were performed using 514.5 nm  $Ar^+$  laser excitation and a Renishaw Raman spectrometer prior to annealing. The Raman active phonons for the wurtzite GaN structure have been widely discussed in the literature [10-13].



**Figure 6.12** Raman spectra for the films with different levels of Mg-doping, taken at 514.5 nm.



Figure 6.13 Raman spectra for sample C4022B, taken at 514.5 nm.

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All the samples in this work show spectra typical of high quality material. Figure 6.12 shows Raman spectra taken at room temperature for the three samples with the same TDD and different Mg doping levels, whereas Figure 6.13 shows the Raman spectrum of sample C4022B. The GaN  $E_2$ (high) phonon frequencies were all reasonably close to the generally accepted value in unstressed material (567 cm<sup>-1</sup>).

A common peak ascribed to a phonon mode of GaN,  $A_1(LO)$ , is also observed at 735 cm<sup>-1</sup> in all samples; the local intensity of this is used as a direct measure of the phonon– plasmon interaction. The LO phonons interact strongly with the charge carriers. However, the compressive stress imposed by the substrate may result in the small increase in the GaN  $E_2(high)$  phonon frequencies in the samples with high TDDs. All of the spectra show the usual sapphire signals ( $A_{1g}$  and  $E_g$ ) at 418 and ~750 cm<sup>-1</sup>, respectively, as denoted by arrows in all films. The sapphire signals were visible because the GaN wafers were too thin to absorb the entire incident light.

#### 6.3.5 Fabrication of Schottky diodes on the p-type GaN

The GaN samples were cleaned using n-butyl acetate, acetone and isopropanol, then dried under nitrogen. After cleaning, the *p*-GaN surface was dry etched by exposure for 3 min to an  $Ar_2$  plasma with a RF power of 100 W; the  $Ar_2$  flow rate was 50 sccm and



Figure 6.14 Metal contacts on films (a) structure A, and (b) structure B.

the chamber pressure was 5 mTorr. Subsequently, Ohmic contacts were formed with Ni/Au (20 nm/20 nm) deposited by thermal evaporation, followed by lift-off and annealing at 500°C for 5 minutes in a nitrogen/air mix. Al/Au (20 nm/200 nm) Schottky contacts of varying diameters (50, 100, 200, 300, 400 and 500)  $\mu$ m were deposited by thermal evaporation through a mask.



Figure 6.15 Bonding of Schottky contacts on one sample.

Firstly, bonding was made directly to the thin Schottky contacts, as shown in Figure 6.15. Unfortunately, this has resulted either in devices with poor rectification behaviour, or in some samples bonding to contacts was not possible and the contacts peeled off. This may be due to the pressure applied by the bonding machine.

A second set of samples was processed similarly, as described above, and in order to enable bonding to these thin contacts, a 500 nm silicon nitride layer was deposited over the entire surface. Electrical access to the contacts was achieved by reactive ion etching (RIE) windows in the silicon nitride. The RIE etch parameters were: CHF3 with a gas flow rate of 35 sccm, RF power 70 W and the chamber pressure was 35 mTorr. Ti/Au contact pads (20 nm / 200 nm) were then thermally evaporated on to the samples. The micrograph in Figure 6.16 shows some of the fully processed devices.



**Figure 6.16** Bonding of Schottky contacts (View looking down). The micrograph on the right shows processed diodes on one sample, scale is shown for 1000  $\mu$ m.

All Ni/Au contacts demonstrated Ohmic behaviour, as all samples were annealed under the same conditions. However, the device processing conditions were varied slightly from the above mentioned routine for another set of samples. These were not subjected to argon plasma (surface treatment) prior to Schottky contact deposition; the fabricated diodes exhibited high leakage currents. The effect of surface treatment is further discussed in chapter 8.

All the device processing work was carried out at the EPSRC national centre for III-V technologies in Sheffield under the supervision of Dr. G. Hill and Dr. Robert Airey.

## 6.3.6 Supplementary Raman Spectroscopy Results

The objective of these supplementary Raman spectroscopy experiments was to use the leftover of the GaN wafers in order to investigate the effect of thermal annealing on the activation of Mg dopants.

Local vibrational modes related to the activation of Mg acceptors were observed in the Raman spectra after annealing at 550°C in N<sub>2</sub> ambient for ~5 minutes. Figure 6.17 and Figure 6.18 clearly show that an additional phonon line appears at about 657 cm<sup>-1</sup> after thermal annealing; the intensity of this peak is almost proportional to the Mg content in the films.



**Figure 6.17** Raman spectra for the annealed Mg-doped films (the films were annealed in  $N_2$  for ~5 minutes), taken at 514.5 nm.



**Figure 6.18** Raman spectrum for the annealed C4022B film (the film was annealed in  $N_2$  for ~5 minutes), taken at 514.5 nm.

The 657 cm<sup>-1</sup> peak has been observed by Harima *et al.* [13] in annealed Mg-doped samples prepared by MOCVD and thermally annealed in N<sub>2</sub> atmosphere at temperatures above 500°C. They attributed the 657 cm<sup>-1</sup> peak to a local vibrational mode for Mg–N stretching because the frequency agrees with an estimation from that of the  $E_1$ (TO) mode of GaN (560 cm<sup>-1</sup>) multiplied by the root of the reduced mass ratio between Mg–N and Ga–N pairs. It was concluded that the 657 cm<sup>-1</sup> mode intensity is a good measure of *activated* Mg concentration, as this structure has been observed for Mg-doped GaN samples but not for undoped GaN samples.

The Mg concentrations for the GaN samples in this work were  $\sim 10^{19}$  cm<sup>-3</sup>, as determined by SIMS experiments. The free hole concentrations were  $\sim 10^{17}$  cm<sup>-3</sup> in the annealed films, which were measured at *T*=300 K by Hall effect measurements. This explains why the 657 cm<sup>-1</sup> mode was not detectable in the as-grown samples as only a few percent of the Mg atoms are ionized at room temperature [14].

Figure 6.17 shows a variation in the intensity of the Raman peak  $E_1(TO)$  at 560 cm<sup>-1</sup> with Mg content, i.e. the incorporation of Mg causes disorder. It is noticeable for all samples that a higher Mg content yields a more intense  $E_1(TO)$  mode. The  $E_1(TO)/E_2$  intensity ratio may be used as a measure for the disorder in the sample [15], as the  $E_1(TO)$  mode is caused by a high concentration of defects. Additionally the  $E_2$  mode becomes broader with a higher Mg content, which can be attributed to the lower crystalline quality.

## 6.4 Conclusions

This chapter described the growth conditions and characterisation of the diamond and GaN thin films examined in this project. The polycrystalline diamond thin films were grown on p+ silicon by HF-CVD and MWP-CVD. The boron concentration in the films ranged from approximately  $8 \times 10^{18}$  to  $9 \times 10^{20}$  cm<sup>-3</sup>. The quality of the produced films was verified by Raman spectroscopy.

The Mg:GaN thin films were grown on sapphire by MOVPE using two different buffer layers giving rise to differing TDDs in the GaN as measured by AFM. The Mg concentrations in the GaN films were  $\sim 10^{19}$  cm<sup>-3</sup>, as determined by SIMS experiments, whereas, the free hole concentrations were  $\sim 10^{17}$  cm<sup>-3</sup>, as measured at T = 300 K by Hall effect measurements. Only a few percent of the Mg atoms were ionized at room temperature. Experimental results showed activation of Mg upon annealing at 550°C in N<sub>2</sub> atmosphere. Finally, different contact structures have been carefully fabricated in order to make reliable electrical contacts to wide bandgap semiconductors for subsequent investigations.
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# 7. Experimental results from *p*-type diamond diodes

## 7.1 Introduction

Polycrystalline diamond films always exhibit electrical properties significantly different to those of single-crystal diamond. However, despite many years of research, little is known about the energy distribution and density of native and extrinsic defects in CVD polycrystalline diamond films. These defects can trap carriers or form recombination centres, and therefore detailed information about them is required in order to improve the performance of devices based on CVD diamond.

In this chapter a comparison of electrically active defects in CVD diamond films with different boron levels has been conducted. Table 7.1 details the polycrystalline diamond samples discussed in this chapter.

Batch	Sample	Growth Method	Annealing	Estimated B-doping (cm <sup>-3</sup> )
A	OS-a2	HF-CVD	Un-annealed	~2×10 <sup>20</sup>
	OS-a5			~6×10 <sup>20</sup>
В	OS-b1	MWP-CVD	Un-annealed	~6×10 <sup>20</sup>
	OS-b2			~8×10 <sup>18</sup>
С	OS-c1	HF-CVD	Un-annealed	~8×10 <sup>18</sup>
	OS-c2			~2×10 <sup>19</sup>
	OS-c3			~8×10 <sup>19</sup>
D	OS-d1	HF-CVD	Annealed 750°C for 30 min	~1.5×10 <sup>19</sup>
	OS-d2			~4×10 <sup>19</sup>

**Table 7.1** Details of the CVD-diamond samples.

These samples were grown on *p*-type Si substrates. Schottky diodes were processed on the diamond surface as described in chapter 6; the investigation of Schottky diodes allowed electrical profiling of the region near the surface of the diamond. Consequently useful conclusions were drawn about the nature of defects present in the diamond film and their capture kinetics, also significant information was extracted about the dopant behaviour at different electrical depths.

Deep level transient spectroscopy (DLTS) and admittance spectroscopy (AS) have been applied to investigate the electronic behaviour of deep levels in semiconducting diamond. Prior to DLTS or AS experiments, capacitance-voltage (C-V) and currentvoltage (I-V) measurements, as function of temperature, were performed to check the integrity of all the diodes on each sample. The C-V data were analysed to yield concentration-depth profiles while the I-V data were used to obtain important diode parameters such as the Schottky barrier height. In addition, the high-resolution Laplace DLTS technique has been applied to establish whether the traps detected by DLTS are due to single or multiple carrier emissions, and direct capture cross-section measurements have been taken to demonstrate whether the detected deep electronic states originated from point or extended defects. Finally, results from AS and DLTS have been compared for the semiconducting diamond.

## 7.2 Experimental results from MWP-CVD grown materials

#### 7.2.1 Sample OS-b1

*I-V* and *C-V* measurements were first carried out at room temperature on all the diodes of this sample in order to select the diodes with the lowest leakage current and conventional capacitance-bias dependence.

The *I-V* data in Figure 7.1, for sample OS-b1, revealed that the forward and the reverse currents were high; the diodes exhibited very high leakage currents, possibly due to the combination of low mobility and very high B doping in this sample. This is as expected

Chapter 7: Experimental results from p-type diamond diodes



Figure 7.1 Current-Voltage characteristics for sample OS-b1 at different temperatures.

for a highly doped film. Both the forward and reverse currents rapidly increase with increasing temperature until 350 K and when the temperature rises above 350 K they almost become temperature independent. A possible explanation for this behavior is that the B concentration is very high, near the limit for metallic conduction; above 350 K, a sufficient proportion of the B is ionised and so the carrier concentration appears to be independent of temperature and mobility decreases at temperatures above RT due to phonon scattering [1,2]. Consequently, conductivity slightly reduces resulting in a small decrease in current. The obtained values of reverse current were high and hence further analysis by techniques that scan over a temperature range such as DLTS and LDLTS was not possible for this particular sample.

Figure 7.2 and Figure 7.3 illustrate respectively the obtained C-V and the corresponding carrier concentration-depth (N-x) profiles for this highly doped diode. It is clear that the capacitance of diode OS-b1 at zero bias is quite large and it greatly increases with



**Figure 7.2** *Capacitance-Voltage* characteristics for sample OS-b1, at different temperatures.



Figure 7.3 Carrier concentration-depth (*N*-*x*) profiles for sample OS-b1.

temperature. This indicates that the width of the depletion region is narrow, as can be verified from the N-x profiles (~ 14 nm), which is expected since the carrier concentration is high. It is worth noting that semi-metallic conduction was taking place in this sample, and the B acceptor level may be getting very close to the valence band [3].

#### 7.2.2 Sample OS-b2

#### 7.2.2.1 I-V and C-V Measurements

*I-V* measurements were carried out over a wide temperature range of 200 to 600 K, as shown in Figure 7.4. At temperatures below 500 K the diode exhibited almost zero leakage current (at V= -5 V), however as the temperature reached 500 K an abrupt change in reverse current values was observed, and as the temperature rises further the leakage current of the diode rapidly increases.



Figure 7.4 *I-V* characteristics for sample OS-b2 at different temperatures.



**Figure 7.5** Richardson plot,  $\ln(1/T^2)$  vs. 1/T for sample OS-b2.

The *I-V* data were used to construct a plot of  $ln(I/T^2)$  versus *1/T*, shown in Figure 7.5, at a constant forward bias voltage V = 0.5 V (Richardson plot); the activation energy was calculated from the slope, and the ideality factor was determined independently  $(\eta = 1.56)$  from the V = 0 intercept of  $I_0$  (at T=300 K for V >> kT/q). The obtained  $E_a$ value was 270 ± 10 meV. This value is near that of the acceptor level, and suggests that the increase in current was caused by simple thermal ionisation of the dopant. It could also be due to ionisation of holes trapped at defects.

Figure 7.6 illustrates the *N*-*x* profile for this diode at a high temperature. The carrier concentration value was about two orders of magnitude smaller than the initial doping concentration (see Table 6.1) indicating that only about 2% of the B concentration was activated at T= 450 K.



Figure 7.6 Carrier concentration-depth (*N*-*x*) profile for sample OS-b2.

#### 7.2.2.2 DLTS and LDLTS Measurements

The DLTS experiments for this sample were performed with a reverse bias -4 V, -0.5 V fill pulse and fill pulse length 2 ms. The spectra are shown in Figure 7.7. The substrate temperature was varied over the range 690 to 80 K by using a closed cycle He cryostat and the DLTS data were recorded using a temperature scan rate 4 K/min at a fixed frequency of 1 MHz.

The DLTS spectra revealed two minority carrier (electron) traps; the first trap or peak covers a wide range of temperature from 140 to 290 K for the 200 s<sup>-1</sup> emission rate window (RW). This peak shifts towards higher temperatures for larger rate windows as expected, since the carriers have more energy as the temperature increases. A broad shoulder in the spectra extending to over 280 K is observed. The second feature in the DLTS spectra covers a wider range of temperature (400 - 600) K for the 200 rate window. This peak or minority carrier trap shifts slightly with temperature for smaller rate windows. Variation of the biasing conditions did not detect any other defects.



Figure 7.7 DLTS spectra for sample OS-b2, performed with a reverse bias -4 V.



Figure 7.8 Arrhenius plot derived from the DLTS spectra for sample OS-b2.

The activation energy of each trap was derived by measuring the peak temperature for every particular emission rate on the DLTS spectrum. The slope of the Arrhenius plot of  $\ln(e_p/T^2)$  versus the reciprocal of temperature allowed the trap activation energy to be calculated. The Arrhenius plot in Figure 7.8 shows that the points are virtually on a straight line. The activation energy of the low temperature trap was 0.35 eV and that of the high temperature trap was 1.36 eV, deep in the diamond bandgap.

To illustrate the behaviour observed by DLTS in this particular sample, it is worth mentioning again that hydrogen-related defects are some of the most technological important impurities in diamond. Polycrystalline CVD diamond films are grown in an atmosphere rich in hydrogen and some is incorporated during growth; much of the hydrogen may be located at the grain boundaries or in non-diamond carbon inclusions.



**Figure 7.9** LDLTS spectra for the low temperature peak,  $V_R$ =-4 V and  $t_P$ =2 ms, sample OS-b2.

On the other hand, *p*-type to *n*-type conversion of B-doped homoepitaxially grown diamond films upon deuterium plasma treatment was experimentally observed [4] and the conversion process was related to the presence of defects in the B-doped layer.

Higher resolution measurements provided by LDLTS may be able to provide accurate information on whether there are more closely spaced defects contributing to the observed levels. Therefore, LDLTS experiments were performed on the low temperature DLTS peak, using the same biasing conditions for this diode. Figure 7.9 shows the LDLTS spectra obtained at different temperatures (160 - 240 K) to illustrate the number of emission rate components that are present. Figure 7.9 clearly indicates that the activation energies can not be extracted and these levels are not due to point defects. Rather these two traps may be due to emission from extended defects, as the emission rates did not vary with temperature. Figure 7.10 shows the LDLTS spectra for the high temperature DLTS peak, the experiments were performed using the same biasing conditions as DLTS, at selected temperatures.



**Figure 7.10** LDLTS spectra for the high temperature peak,  $V_{R}$ =-4 V and  $t_{P}$ =2 ms, sample OS-b2.

Three levels were revealed, and the peak emission rates were scattered with temperature and hence did not allow meaningful activation energy calculations.

Unfortunately, the LDLTS can not yield more information other than the fact that a multitude of closely spaced defects exist, which possess complicated emission characteristics. However, it is worth noting that both the *I-V* and *C-V* measurements for this sample show a sudden change at elevated temperatures (above 500 K). However, slight changes in the color of the electrical contacts of this particular sample were observed after testing; it is suggested that the contacts may have degraded due to enhanced diffusion along grain boundaries at very high temperatures (~690 K), hence results for this sample are not discussed further.

## 7.3 Experimental results from the HF-CVD grown materials: Batch A

The film OS-a1 was nominally undoped for reference purposes, as discussed in chapter 6; the remaining HF-CVD diamond thin films were processed for electrical contacts.

While checking the suitability of the contacts it proved difficult to bond to contacts on samples OS-a3 and OS-a4, they also exhibited semi-metallic behaviour. This can simply be explained by the very high doping of those samples. It should be once again mentioned that the boron doping concentration of  $5 \times 10^{20}$  cm<sup>-3</sup> is considered to be the beginning of metallic conduction in single crystal diamond, however this level may be different for the polycrystalline diamond films examined in this work. Hence it was not possible to conduct any electrical measurements on those two samples.

## 7.3.1 Samples OS-a2 and OS-a5

#### 7.3.1.1 *I-V* Measurements

*I-V* measurements were performed at room temperature on all the diodes of samples OS-a2 and OS-a5 in order to select the diodes with the least leakage current.



Figure 7.11 *I-V* characteristics for samples OS-a2 and OS-a5, at 300 K.

The *I-V* plots in Figure 7.11 illustrate that the less highly doped sample OS-a2 exhibited higher series resistance, which was expected. *I-V* measurements were then performed over a wide temperature range, 80 to 400 K, and as the temperature rose the leakage current of the diodes increased rapidly. In order to avoid irreversible diode breakdown the maximum applied reverse bias was set to -1 V. The *I-V* characteristics reveal that, whilst DLTS measurements may be possible at temperatures below 400 K, at high temperatures the diodes become very leaky.

The *I-V* characteristics for both samples were analyzed in order to deduce the ideality factor and the barrier heights from the slope and the intercept of the plot of log *I* vs. *V*. Large ideality factors,  $(2.5 < \eta < 7)$  and  $(2 < \eta < 4)$ , were obtained over the mentioned range of temperatures for sample OS-a2 and sample OS-a5 respectively. These *n* values may suggest that other current transport mechanisms rather than thermionic emission were taking place, possibly due to the fact that, at high doping levels, conduction occurs by nearest-neighbour and variable range hopping of holes between ionised B sites

accompanied by a drop in mobility [5]. At very high doping levels, an impurity band is formed, giving rise to semi-metallic conductivity.

There was also a temperature dependence involved in the Schottky barrier height. The extrapolated barrier heights for diodes on both samples were fairly low ( $\Phi_b \approx 0.8$ ) at 400 K.

## 7.3.1.2 C-V Measurements

C-V experiments on these samples were carried out at different temperatures. They were performed at the same bias as the *I-V* measurements to ensure that there was no large current passing through the device. The capacitance of sample OS-a2 was quite large and it increased greatly with temperature; for temperatures below 200 K the capacitance almost vanished but as the temperature rose beyond this point the capacitance increased continuously.



Figure 7.12 C-V characteristics for sample OS-a2, at different temperatures.



Figure 7.13 C-V characteristics for sample OS-a5, at different temperatures.

The capacitance of sample OS-a5 at zero bias was even higher than that of OS-a2 as the boron doping for this sample is higher. However, the capacitance changed more rapidly as the temperature rose beyond 180 K.

There was a temperature dependence involved in the extrapolated  $V_{bi}$  and the values for  $V_{bi}$  were too large at temperatures below RT to be interpreted as the diode's  $V_{bi}$ , whereas at 400 K the extrapolated  $V_{bi}$  values were 1.12 V and 1.15 V for samples OS-a2 and

OS-a5 respectively. These values of  $V_{bi}$  seem acceptable for both diodes. The temperature dependence of  $V_{bi}$  may be due to interface states present at the interface of the metal and the semiconductor.

The acquired data were analysed to yield the carrier concentrations for each sample. Figure 7.14 shows the N-x profiles obtained at 400 K for both samples. The carrier concentration was larger in sample OS-a5 and depletion region commences at around 40 nm from the surface.



Figure 7.14 Carrier concentrations-depth (*N*-*x*) profiles, at *T*=400 K.

The values determined from C-V profiling represent the majority carrier density and not the doping density. However, in sample OS-a5, there is a decrease of carriers further behind the surface, therefore, the C-V data suggest that the B is passivated further into the sample; this might be consistent with H partially diffusing out from the surface during the heat treatment, but not being completely removed. This phenomenon is regularly observed in many semiconductors where H incorporation and passivation occurs.

#### 7.3.1.3 DLTS and LDLTS Measurements

Figure 7.15 shows the DLTS spectra acquired with five different rate windows, reverse bias of -0.75 V,  $V_p = 0$  V and  $t_p = 5$  ms. The DLTS spectra revealed a broad peak indicating a defect level emitting majority carriers between 150-280 K and another peak starting at ~320 K.



Figure 7.15 DLTS spectra for Sample OS-a2



Figure 7.16 Arrhenius plot, derived from the DLTS spectra of peak A.

The peaks are positive; therefore they are majority carrier traps. However the intensity of the peaks reduced for slower emission rate windows. As it is a broad level, it could consist of defects closely spaced in energy; there was a slight asymmetry in the 200 s<sup>-1</sup> peak which disappears at slower rate windows. This is also suggestive of more than one trap contributing to this peak. In order to verify this, higher resolution measurements (LDLTS) were required.

Unfortunately, it was only possible to deduce the activation energy for the trap contributing to peak A, as shown in Figure 7.16. The DLTS data for peak B were noisy, yielding an inaccurate Arrhenius plot (not shown). Interpretation of the value for peak A follows later.

LDLTS measurements were performed at temperatures around the peak-maximum of the DLTS spectrum.



Figure 7.17 LDLTS spectra for the low temperature peak (A).

Figure 7.17 shows that three emission rate components were revealed at each of the measured temperatures for the DLTS peak at around 220 K for sample OS-a2. In the

case of simple point defects an increase of emission rate is expected when the temperature increases; the peaks should shift towards higher emission rates at every temperature increment in a consistent manner, since the traps have more energy at higher temperatures and therefore emit faster. However, the LDLTS spectra for this defect show that this is not the case.

Furthermore, the LDLTS peaks either moved in a random fashion when the temperature increased or they seemed almost unaffected by the temperature change, which was not expected to occur. Therefore meaningful activation energies could not be calculated from the LDLTS data.

The calculated trap activation energy from DLTS (0.19 eV) may imply that this level is related to hydrogen, as H is known to be a relatively fast diffuser in boron-doped monocrystalline diamond; it has a low migration energy of 0.2 eV. During this diffusion, H is trapped by boron acceptors giving rise to B-H complexes and to a passivation of boron acceptors by hydrogen. However it must be noted that the LDLTS data have implied that the situation is potentially more complicated than this. It may be that those defects that contribute to the DLTS peak (A) are in the strain field of a larger defect, such as a grain boundary, and the DLTS is averaging the whole system.

The DLTS spectra for sample OS-a5, illustrated in Figure 7.18, reveal a trap level emitting between 140 -180 K. The biasing conditions were similar to OS-a2, a reverse bias of -0.75 V, a filling pulse of 0 V and a fill pulse length of 5 ms.

Unfortunately the Arrhenius analysis for this level did not yield an activation energy as the data were extremely noisy, which may be indicative of more than one trap present. This was confirmed by the LDLTS spectra as shown in Figure 7.19 and Figure 7.20. This may be attributed to the presence of strain fields in the sample.



Figure 7.18 DLTS spectra for sample OS-a5



Figure 7.19 LDLTS spectra for the low temperature peak of sample OS-a5.



**Figure 7.20** LDLTS spectra for sample OS-a5 at 160 K taken with varying  $t_p$ .

Two closely spaced traps are apparent in the LDLTS spectra. The LDLTS spectra across a small range of temperature show virtually no change in the peak temperature. This has been observed before in SiGe quantum wells and was attributed to carriers being thermally emitted from a confined state in the quantum well [6]. It is postulated that the carriers being emitted in this sample are trapped in electronic states associated with the grain boundaries; these states are invariant with T over a small range because they are acting as quantum confinement centres on a microscopic scale.

The results revealed that the main DLTS peak (A) in sample OS-a2 consisted of three levels situated in strain fields of extended defects, possibly grain boundaries. Furthermore, as the boron content of the film increases, one of the traps disappears from the spectra. Unfortunately, activation energies could not be deduced from the LDLTS data, since emission rates did not consistently reduce with temperature, yielding an inaccurate Arrhenius plot. This is attributed to the presence of strain fields in the sample. It has not been possible to obtain activation energies for the two closely related levels that contribute to the single peak observed in the DLTS spectra from sample OS-a5.

## 7.4 Experimental results from the HF-CVD grown materials: Batch C

### 7.4.1 Sample OS-c1

## 7.4.1.1 *I-V* and *C-V* Measurements

Prior to DLTS measurements, C-V and I-V measurements were carried out to check the integrity of the diodes. The I-V characteristics of this sample, shown in Figure 7.21, exhibited good rectification behavior, zero leakage current was observed for this diode over the examined temperature range. However, the forward current increased gradually with temperature. The C-V data in Figure 7.22 show that the capacitance is correctly bias dependent and hence it is possible to conduct DLTS experiments.



Figure 7.21 *I-V* characteristics for sample OS-c1, at different temperatures.



Figure 7.22 C-V characteristics for sample OS-c1, at different temperatures.



Figure 7.23 Carrier concentrations-depth profile, at T=550 K.

It is worth mentioning again that it is known, for example, in diamond containing  $10^{18}$  cm<sup>-3</sup> boron acceptors and having a compensation ratio of 10%, 84% of boron acceptors are not ionized at a temperature of 320°C because of their high ionization energy (~0.37 eV) [7,8]. However in this sample the carrier concentration measured by *C-V* was about 1×10<sup>17</sup> cm<sup>-3</sup> (at *T*=550 K), as shown in Figure 7.23, which is much lower than the estimated boron doping density. The carrier concentration was about two orders of magnitude smaller than the initial doping concentration; the B ionization percentage was ~ 1.25%.

In this sample the *I-V* and *C-V* characteristics suggest that there is a thin insulator layer between the Al Schottky contact and the diamond, which may account for the low current in this sample. This could be a thin oxide layer  $(Al_2O_3)$  formed during the processing. This should not significantly affect the ability to carry out the reverse-biased DLTS however.

#### 7.4.1.2 DLTS and LDLTS Measurements

Figure 7.24 shows the DLTS spectra of sample OS-c1, using a Schottky diode, measured at -2 V reverse bias, various rate windows, fill pulse -0.5 V and fill pulse duration of 5 ms.

The DLTS spectrum revealed one minority carrier trap; the reason that the DLTS of this sample is showing minority carrier emission may be connected with the thin oxide layer in this sample as illustrated in the I-V and C-V plots; minority carriers (electrons) may tunnel through the thin oxide, especially at high temperatures.

The DLTS peak covers a wide range of temperature from 450 K to 600 K for the 200 s<sup>-1</sup> rate window. The peaks look well behaved with the variation of rate windows, they shift towards lower temperatures as the rate window reduced; therefore it was possible to calculate the activation energy of this trap, which was found to be 0.54 eV.



Figure 7.24 DLTS spectra for sample OS-c1.



Figure 7.25 Arrhenius plot, derived from the DLTS spectra of OS-c1.

The DLTS results may be interpreted as boron-hydrogen complex defects.  $H^+$  is the diffusing species in B-doped diamond, and subsequently, neutral BH pairs will form in diamond as a result. Theoretical reports by Mehandru and Anderson [9] predict the formation of a deep donor level by hydrogen, above the fundamental level of boron, which traps the electron from neutral hydrogen leaving a mobile  $H^+$  which neutralizes the B<sup>-</sup> state, thus forming a neutral B-H complex. As a result, a compensated semiconductor is generated within the depth of hydrogenation.

LDLTS experiments were performed at temperatures around the peak-maximum of the DLTS spectrum. Figure 7.26 shows that only two emission peaks were detected by LDLTS for the broad peak seen in DLTS. The high emission rate peak did not particularly change in emission as the temperature varied, which may be indicative of an extended defect. The other LDLTS peak present at lower emission rates seemed to vary in emission as the temperature reduced, but not in a consistent manner.



**Figure 7.26** LDLTS spectra for sample OS-c1 for a  $t_p$  of 5 ms. The inset is a magnification for the low emission rate peaks.



**Figure 7.27** LDLTS spectra for sample OS-c1 recorded at 600 K using different fill pulse durations, the reverse bias was set to -4 V.

Figure 7.27 shows the LDLTS recorded at 560 K using different fill pulse durations, the reverse bias was set to -4 V. The emission rate of the lower peak did not vary with fill pulse length behaving as a defined point defect while the LDLTS peak at higher emission rate slightly varied consistently with the increase of the fill pulse length, which implies that the defect being emitted is trapped in electronic states associated with the grain boundaries. However, in polycrystalline diamond, it is not surprising that there is a rich defect structure with many electronic levels.

#### 7.4.2 Sample OS-c2

#### 7.4.2.1 I-V and C-V Measurements

Figure 7.28 shows the I-V data obtained for sample OS-c2 at different temperatures. The I-V characteristics for this sample exhibited better forward currents than OS-c1, but the leakage current was higher and varied with temperature.



Figure 7.28 *I-V* characteristics for sample OS-c2, at different temperatures.



Figure 7.29 C-V characteristics for sample OS-c2, at different temperatures.

*C-V* measurements for sample OS-c2 were performed on the same diode and the data were analysed to yield the carrier concentrations. Figure 7.29 and Figure 7.30 show respectively the *C-V* data as function of temperature and the *N-x* profile obtained at T=550 K. The carrier concentration measured by *C-V* at this temperature was about  $1\times10^{18}$  cm<sup>-3</sup>, which was much lower than the estimated boron doping density. The B ionization percentage is 5%, which is larger than OS-c1 but still only a small fraction of the estimated B doping for this sample.



Figure 7.30 Carrier concentrations-depth profile for sample OS-c2, at T=550 K.

#### 7.4.2.2 DLTS and LDLTS Measurements

Figure 7.31 shows the DLTS spectra of the Schottky diode, measured at -2 V reverse bias, applying a negative fill pulse -0.5 V, and pulse duration of 5 ms.



Figure 7.31 DLTS spectra for sample OS-c2.



Figure 7.32 Arrhenius plot, derived from the DLTS spectra of OS-c2.

Two dominant majority carrier traps were observed in the DLTS spectra at all rate windows. The first peak at about 160 K, is similar to that observed in OS-a5 although it is somewhat narrower in this diode and contains a shoulder that extends slightly towards lower temperatures. The second DLTS peak is broad, emitting over a wide range of temperatures 220-400 K. Both peaks shifted towards lower temperatures as the rate window reduced. Arrhenius plots were constructed using the DLTS data. The points for each level lie perfectly on a straight line, yielding activation energies of about 0.29 eV for the 160 K peak, and 0.49 eV for the broad peak, as shown in Figure 7.32.

In order to verify the nature of these defects, LDLTS experiments were carried out at a range of temperatures contained within each peak. The LDLTS results shown in Figure 7.33 confirms the presence of one single defect emitting at around 160 K, the emission rate of the low temperature defect is almost unaffected by changes in temperature, suggesting this is not a point defect.



Figure 7.33 LDLTS spectra for the low temperature peak of OS-c2.



Figure 7.34 LDLTS spectra for the high temperature peak of OS-c2.

It is obvious from the LDLTS results (shown in Figure 7.34) that in fact two traps give rise to the DLTS peak at around 350 K. The emission rates of the defects emitting between 260 K and 420 K do vary consistently with temperature, but the results of an Arrhenius plot were not convincing and did not indicate the high temperature trap was due to an extended defect or a point defect. Also, efforts to calculate the activation energy of the defects by plotting the LDLTS pairs of peak emission rate against temperature did not yield a straight line.

It is worth noting that above 380 K only one emission rate appears in the LDLTS spectrum, as illustrated in Figure 7.34. This defect was examined again by cooling the sample in the cryostat and repeating the LDLTS measurements. Two emission rates reappeared in the spectrum for temperatures below 400 K which implies that the second defect did not anneal out permanently at 400 K rather that the emission rate is too fast to see at temperatures above 380K.

In order to further characterise the nature of the defect contributing to the low temperature peak, capture cross-section measurements were performed at T=160 K according to Equation (4.36), in order to investigate the evolution of the capture kinetics with time. Figure 7.35 presents the capture cross-section data of the peak capacitance acquired from DLTS measurements by varying the fill pulse duration from 5  $\mu$ s to 5 ms. The reverse bias was -2 V and the fill pulse -0.5 V. Figure 7.35 illustrates that the defect has a capture rate that changes exponentially with time; deviation from linearity provides a sensitive test for the presence of extended defects that exhibit Coulombic repulsion because the trapped carriers repel any further charges resulting to a diminished carrier capture probability with time.



**Figure 7.35** The capacitance change as a function of fill-pulse duration for the defect at 160 K.

The LDLTS measurements are in accordance with this conclusion where it was observed that the emission rate almost unaffected by the change in temperature. It is postulated that the emission detected in DLTS is due to an extended defect, possibly grain boundaries. This is discussed in more detail later in this chapter. Capture cross section data were acquired for the high temperature defect, from DLTS measurements by varying the fill pulse duration at 350 K, as shown in Figure 7.36. It can be seen that the capture characteristics appear to have a combination of linear and exponential dependency with time.

The combination of capacitances should remain below unity as  $C_{\text{max}}$  is the maximum of the DLTS peak for the highest fill pulse length. The observed increase in the capacitance terms with reduced fill pulse length signifies that the term  $dC_t$  becomes smaller which means that the peak of the DLTS spectrum reduces for reduced fill pulse; this behaviour



**Figure 7.36** The capacitance change as a function of fill-pulse duration for the defect at 350 K in sample OS-c2.

is expected for point defects. However, as the fill pulse reaches  $300 \ \mu$ s, the combination of capacitances starts to reduce. The decrease in the logarithm of the capacitances signifies that the peak of the DLTS starts to increase even if the fill pulse length gradually reduces. These observations indicate that there may be two closely spaced levels, as suggested by LDLTS results, one of which has a more point defect-like capture characteristic while the other is an extended defect. The other scenario may be

that the entire capture process is governed by complex defects. In the case of the extended defect the Coulomb potential that has developed after the initial capture may be of opposing strength to the electric field existing in the depletion region during bias application and is hence momentarily reduced enough by longer fill pulses, therefore result in point defect-like capture or emission. However, when applying very short pulse lengths, there is not enough time to reduce the Coulomb potential around the extended defect sufficiently for carrier capture, thus the behaviour of emission deviates from that of a point defect. In fact it is not a typical behaviour even for extended defects to see an increase in emission as  $dC_t$  increases. Therefore, emission from grain boundary sites has to be considered as the capture process is even more complicated.

### 7.4.3 Sample OS-c3

#### 7.4.3.1 *I-V* and *C-V* Measurements

The *I-V* plots in Figure 7.37 for diode OS-c3 show good diode characteristics, in particular below room temperature for reverse bias -2 V. However, as the temperature







Figure 7.38 C-V characteristics for sample OS-c3, at different temperatures.




rises above 300 K the reverse currents continue to increase quickly and at 550 K the I-V becomes virtually temperature independent.

The C-V plots in Figure 7.38 show that the capacitance is very dependent on bias. Below 550 K the capacitance at zero bias consistently increased with increasing temperature. In this sample the carrier concentration measured by C-V at T=550 K was about  $3\times10^{18}$  cm<sup>-3</sup> showing a B ionization percentage of 3.7% for this diode.

### 7.4.3.2 DLTS and LDLTS Measurements

The DLTS results for diode OS-c3 are shown in Figure 7.40 for a reverse bias -2 V, a fill pulse of -0.5 V and fill pulse length 2 ms.



Figure 7.40 DLTS spectra for sample OS-c3.



Figure 7.41 Arrhenius plot, derived from the DLTS spectra of low temperature peak.

The DLTS spectra revealed a broad majority trap level, covering a wide temperature range from 100 to 220 K for the 200 s<sup>-1</sup> emission rate window. This positive peak appears as a single defect level in this spectrum. Use of different biasing conditions in DLTS did not reveal any other levels in the DLTS spectrum; this was further verified using LDLTS. The peak is well behaved and shifts in a consistent manner towards lower temperatures as the rate window reduces. An Arrhenius plot was constructed to yield the activation energy of this trap, as shown in Figure 7.41. The activation energy is 0.2 eV.

It is worth mentioning that this level (0.2 eV) was detected at similar temperature range to that observed in OS-a5 and OS-c2, and has similar characteristics. However, this may contain more defects; one of them may be the B acceptor level which reduces in activation energy for higher doped samples. It may be the reason that the activation energy of this trap is lower than that of OS-c2 (0.29 eV).

At high temperatures, around 550 K, there was a reversal of capacitance (the negative peak) which could be due to a minority carrier trap emitting around that temperature. An

explanation for this may be that electrons were injected at very high temperatures where this diode tends to have high leakage currents, as illustrated in Figure 7.37. However, the peak seems almost unaffected with the variation of rate window, which is not expected to occur, yielding an inaccurate Arrhenius plot (not shown). Application of different fill pulse voltages was performed to examine this DLTS feature but this did not yield any useful information. Therefore this peak can not be discussed further, but as the emission rate of the defect is not affected by temperature it is suggested that the emission detected in DLTS is either from an extended defect or due to levels in the grain boundaries in diamond, exhibiting very complex emission characteristics. A combination of several characterisation techniques would be necessary to investigate such a feature.



Figure 7.42 LDLTS spectra for the low temperature peak.

LDLTS measurements were performed over the entire temperature range that the low temperature DLTS feature spanned, using the same biasing conditions as DLTS. The LDLTS results revealed two emission peaks which randomly shift with temperature; this confirms that these levels are not due to simple point-like defects.

## 7.5 Experimental results from the HF-CVD grown materials: Batch D

### 7.5.1 Samples OS-d1 and OS-d2

As pointed out in section 6.2.6, the device processing of samples OS-d1 and OS-d2 was different from the previously discussed diamond samples. These films were chemically cleaned to remove any graphitic layers and to O-terminate the surface and then subsequently annealed in vacuum at 750°C. As it has been suggested that large population of boron atoms are passivated by association with other impurities such as hydrogen [8], annealing should reduce the concentration of such complexes, and increase the proportion of electrically active B.

Observations of the effect of examining the Al contacts at elevated temperatures were taken in consideration; the diodes were only tested at temperatures below 500 K to prevent thermal degradation of the contacts.

### 7.5.1.1 The *I–V* and *C-V* Measurements

Prior to DLTS experiments, C-V and I-V measurements were performed to check the suitability of the diodes (up to 8 diodes on each film), and also to obtain information about the Schottky barrier heights of these diodes.

Figure 7.43 and Figure 7.44 show the I-V characteristics for diodes on both films obtained at different temperatures. Table 7.2 details the Schottky diode properties for both diodes in the temperature range 300 to 450 K.



Figure 7.43 *I-V* characteristics for sample OS-d1, at different temperatures.



Figure 7.44 *I-V* characteristics for sample OS-d2, at different temperatures.

<i>T</i> [K]	Sample OS-d1			Sample OS-d2		
	η	$\Phi_{b(IV)}$ [eV]	$\Phi_{\mathfrak{b}(CV)}$ [eV]	η	Φ <sub>b (IV)</sub> [eV]	$\Phi_{b(CV)}$ [eV]
200	2.2	0.83	2.36	3.6	0.66	1.95
250	1.94	0.94	2.38	3.2	0.79	2.05
300	1.8	1.17	2.25	2.9	0.95	2.3
350	1.7	1.25	2.18	2.5	1.12	2.24
400	1.4	1.37	2.1	2.3	1.17	2.15
450	1.2	1.48	1.95	2.1	1.26	2.03

**Table 7.2** Schottky diode parameters for diodes OS-d1 and OS-d2 measured by *I-V* and *C-V* plots.

The barrier height decreased with decreasing temperature (~ 1 eV at 300 K). Schottky barrier heights between 0.8 and 2.2 eV have been reported in the literature [10-13], our measured value of barrier height was within this range. Recent theoretical studies [14] have suggested barrier heights of 1.1 eV for Al contacts on H-terminated diamond.



**Figure 7.45** The log (*I*) *vs*.*V* plots for sample OS-d2 at different temperatures. The plot shows a change in the current conduction mechanism above 250 K.

In sample OS-d2 the *I-V* behaviour changes above  $\sim$ 240 K, as illustrated in Figure 7.45, implying that current mechanisms other than thermionic emission were taking place; therefore larger *n* values were obtained.

The *C-V* data are plotted in Figure 7.46, revealing the profile of carrier concentrations within the space-charge region of a Schottky diode on each of the samples. As expected, the doping was found to be uniform in the space-charge region investigated by the applied voltages. The carrier concentration was higher in sample OS-d2 and the depletion region was narrower (~30 nm) than in sample OS-d1 (~50 nm) at 400 K, as expected. However, carrier concentrations were much lower than the estimated boron-doping density in both samples; showing a B ionization percentage of 2.6% for sample OS-d1 while for sample OS-d2 was 3%. It is worth noting that a large population of the boron atoms incorporated into diamond do not act as acceptors [7,8], despite trying to remove B-H complexes from the subsurface region by annealing.





From the *C*-*V* data, the built-in potential  $(V_{bi})$  values were deduced from the extrapolation of  $1/C^2$  to zero and the Schottky barrier heights  $(\Phi_b)_{CV}$  were calculated from these values at 300-450 K. These data are listed in Table 7.2. It is reported by Nebel *et al.* [15] that the barrier height of Al on B-doped diamond, evaluated using *C*-*V* measurements, is 1.95 eV; this agrees well with the value obtained for sample OS-d1.

Variations of the barrier height over the contact area can occur as a result of nonuniformity of the interfacial layer thickness, inhomogeneities in the interfacial layer composition, and/or distributions of interfacial charges. The variations in the ideality factor with temperature are related to barrier inhomogeneities and also to the degree of its deformation under the applied bias. The ideality factor evolution and difference between  $(\Phi_b)_{CV}$  and  $(\Phi_b)_{IV}$  barriers have been widely discussed by other authors [16,17].

### 7.5.1.2 DLTS and LDLTS Measurements

DLTS experiments were performed using the multi emission rate windows and a range of biasing conditions. Figure 7.47 shows the DLTS spectra for samples OS-d1, measured under reverse bias -3 V with a fill pulse of -0.5V applied for 50 ms.

The DLTS spectra for sample OS-d1 revealed two majority carrier traps. The first peak was around 170 K with an activation energy 0.29 eV, with trap density of  $\sim 2.8 \times 10^{16}$  cm<sup>-3</sup>, and the second peak covered a wide range of temperatures from 320 K to 440 K with an activation energy of 0.53 eV and trap density of  $\sim 4.3 \times 10^{16}$  cm<sup>-3</sup>. Both peaks shift towards higher temperatures for higher-rate windows as expected. However, the peaks are asymmetric with a tail on the low-temperature side (as was the case for most rate windows), a feature typical of an extended defect.

The DLTS experiments of sample OS-d2 were performed using two sets of RWs  $(20 \text{ s}^{-1}, 50 \text{ s}^{-1})$  and  $(80 \text{ s}^{-1}, 200 \text{ s}^{-1})$ ; for clarity two RWs are shown in Figure 7.48.



**Figure 7.47** DLTS spectra of sample OS-d1, obtained with multi rate windows (RW), reverse bias –3 V and fill pulse –0.5 V.



**Figure 7.48** DLTS spectra of sample OS-d2, obtained with reverse bias –3 V and a fill pulse of –0.5 V.

Three hole traps E1, E2 and E3 were found in this film; the activation energies of these levels were deduced from the Arrhenius plot in Figure 7.49 and found to be 0.26 eV, 0.49 eV and 0.35 eV respectively. The E1 and E2 levels are found in both films OS-d1 and OS-d2 whereas E3 is only seen in the more highly doped film. E3 is centred around 250 K, with trap density  $\sim 3 \times 10^{16}$  cm<sup>-3</sup> and an apparent capture cross-section of  $\sim 1 \times 10^{-16}$  cm<sup>2</sup>. This  $\sigma$  value is less than expected for the boron acceptor. However, capture cross-sections extrapolated from Arrhenius plots can have uncertainties of several orders of magnitude and need to be treated with caution.



Figure 7.49 Arrhenius plot, derived from the DLTS spectra of OS-d2.

A defect with similar activation energy (0.35 eV) has been reported in B-doped diamond, grown by hot filament CVD, detected by admittance spectroscopy in the 170-270 K temperature range; the origin of this level has not been confirmed [18].

The high-temperature peak (E2) observed may contain multiple emissions as it covers a wide range of temperatures in both samples. Kiyota *et al.* [19] reported a trap level with activation energy of 0.6 eV above the valence band edge in boron-doped polycrystalline diamond films grown on Si substrates using HF-CVD. They argued that the detected

level is either generated by the hot filament technique applied to grow this diamond or is related to grain boundaries in the polycrystalline diamond. Furthermore, Lombardi [20] has calculated the properties of boron and its complexes with hydrogen in diamond using density functional theory; his results show that BH<sub>2</sub> centres are stable with binding energies of 0.23 to 0.71 eV. It can be argued that although these samples were grown in a hydrogen-rich environment but were oxygen-terminated on the diamond surface it is very likely that hydrogen is present in larger volumes near the interface because the annealing has removed H nearer the surface, giving rise to this level. Kumar et al. [21] have theoretically investigated the BH and BH<sub>2</sub> complexes in B-doped diamond. They predicted the associated acceptor levels to be  $E_v$ +4.44 eV and  $E_v$ +1.14 eV, respectively. The associated donor levels were found to be  $E_c$ -4.84 eV and  $E_c$ -2.80 eV, respectively. The BH donor level at  $E_c$ -4.84 eV (corresponding to  $E_v$ +0.6 eV) is found to be at the same energy level as the donor level of the vacancy [22]. These are in good agreement with recent results measured by isothermal transient spectroscopy [23]. The atomic structure of the complex defect BH<sub>3</sub> is less well understood, it is predicted to form a donor level at  $E_v$ +0.20 eV [24]. Recently, Muret et al. [23, 25] have reported that hole traps with ionisation energies between 0.7-1.6 eV are most likely due to hydrogen related defects. Further details about deep donor levels and deep acceptor levels related to boron, hydrogen, or structural defects in B-doped monocrystalline diamond calculated by *ab initio* method and attribution to traps observed by DLTS is given in [23].

In order to verify the nature of the DLTS features, LDLTS measurements were performed under the same biasing conditions as DLTS, over the entire temperature range that the DLTS feature spanned.

At 170 K, LDLTS results revealed one emission in sample OS-d1, whereas in sample OS-d2 two closely spaced electronic levels were revealed, as shown in Figure 7.50, confirming that a second level was introduced in the more highly doped film.



**Figure 7.50** LDLTS of OS-d2 at 160-180 K with  $V_{B}$ =–3 V, fill pulse –0.5 V and fill pulse length 50 ms. The inset shows the LDLTS of OS-d1.

Figure 7.50 also illustrates that changing the temperature does not particularly influence the emission of these traps. The carrier emission rates did not change with temperature and it is likely that this is because we were unable to sample for long enough due to very slow emission rates, particularly at the low temperatures. Therefore, although one could speculate that this might indicate the electronic levels giving rise to the emission are not pure point defects, this data would need considerable further investigation. A detailed capture cross section measurement which also indicates that extended defects are contributing to these spectra is discussed next.





Figure 7.51 LDLTS of OS-d1 at 360 and 380 K with  $V_{\rm B}$ =–3 V, fill pulse length 50 ms.





LDLTS measurements were carried out at temperatures around the peak-maximum of the DLTS feature E2 on samples OS-d1 and OS-d2. The results, shown in Figure 7.51 and Figure 7.52, reveal three distinct emission rates, confirming that this defect possesses three closely spaced electronic levels in the bandgap. The appearance of the same number of emission rates in both samples means these are unlikely to be artefacts of the measurements. These defect levels either behave in a random way or are almost unaffected by increasing the temperature, suggesting these are not due to point defects.



**Figure 7.53** LDLTS of OS-d2 at temperatures 230-270 K with reverse bias –3 V and fill pulse length 50 ms. The spectra have been offset vertically from each other for clarity.

Figure 7.53 shows the LDLTS results for sample OS-d2 at temperatures around the peak-maximum of the DLTS peak E3. These demonstrate the presence of two closely spaced defects, the emission rates of which vary with temperature in a consistent manner throughout the entire range 230–270 K, behaviour typical of point-like defects. Therefore, activation-energy calculations were possible for these levels; the activation

energy of the defect appearing at lower emission rate was found to be 0.35 eV while the activation energy of the higher emission rate defect was 0.37 eV. This is in very good agreement with that of substitutional B.

It is well known that capture cross-sections extrapolated from Arrhenius plots can have uncertainties of several orders of magnitude and need to be treated with caution. There are various reasons for this discrepancy: a small overlapping effect with a neighbouring signal in DLTS and the fact that DLTS analysis relies upon simple relationships between emission and temperature where in fact these are often more complex. Also, there is experimental evidence showing that electric-field-enhanced emission tends to generate errors in cross-sections [26,27]. A more reliable technique for determining the capture properties is by using various pulse widths at a fixed temperature [27,28] where the capture time can be determined by varying  $t_p$  and hence carrier emission does not affect the results.



**Figure 7.54** The capacitance change as a function of the fill-pulse length of the defect at E1 in sample OS-d1 and the defect at E3 in OS-d2, a reverse bias of -3 V was applied. The data were recorded at 170 K For E1, whereas for E3 at 250 K.

Figure 7.54 shows the capacitance change as a function of the fill-pulse length. The data were recorded for the defect at E1 in sample OS-d1 at 170 K, reverse bias of -3 V and a fill pulse of -0.5 V, in accordance with Equation (4.36). The defect at E3 in sample OS-d2 was examined at 250 K under similar biasing conditions. The recorded data show excellent linearity when plotted in accordance with Equation (4.36), as shown in Figure 7.54, and hence it was possible to extract the capture cross-section by calculating the gradient of the graph; it was found to be  $3 \times 10^{-15}$  cm<sup>2</sup>, which is significantly larger than the value extrapolated from Arrhenius plot ( $1 \times 10^{-16}$  cm<sup>2</sup>).

The majority capture cross-section should obey a linear dependence on the logarithm of a combination of capacitance terms as function of pulse length. This provides a sensitive test for the presence of isolated point defects only if the mobile holes concentration is instantaneously provided to a level where holes could be captured by the deep centres. Deviation from this relationship may provide a test for the presence of extended defects. However, the causes of non-linearity in the capture cross section data could be explained by different scenarios. The first scenario could be that, Equation (4.36) is not valid for E1, as the hole emission time for the transition from the ground state to delocalised states in the valence band falls into the fill pulse time range. For example, if one assumes shallow acceptors like in single crystalline diamond, with a capture cross-section of  $4 \times 10^{-13}$  cm<sup>2</sup> and an activation energy of 0.37 eV (at ~170 K), the emission time is estimated to be 3 ms [29]. This reduces the likelihood of the mobile holes concentration to be instantaneously available to the zone where they have to be captured by the deep centres and resulting in a non-linear characteristic. Such a limitation disappears at 200 K and above. Therefore, E1 could be due to point-like defects.

The second scenario could be that the level E1 is grain boundary related states. This is a reasonable suggestion since it has been only reported in polycrystalline diamond [30-32], although this has not been proven here. In this case the trap distribution will be very inhomogeneous and the defects may be sufficiently closely spaced that the presence of a filled trap will reduce the likelihood of a neighbouring empty trap capturing a hole. Therefore, E1 could be due to an extended defect exhibiting

Coulombic repulsion, because the repulsive force reduces subsequent carrier capture at the defect which is slowly charging up.

In the case of E2, the ionisation should be fast enough, as this trap is emitting at T > 200 K. However, nonlinearity is observed in the capture cross section data for samples OS-d1 and OS-d2 (recorded at 360 K), hence Equation (4.36) does not hold. It has been reported in [25], for B-doped monocrystalline diamond that the origin of the majority carrier traps located in energy between the top of the valence band and circa 1.6 eV is related to hydrogen, confirming previous predictions [21, 23]. Based on these findings, one can suggest that E2 may be due to BH donor level.



**Figure 7.55** DLTS signal as a function of the logarithm of the filling time for the defects at E1 and E2 in sample OS-d1, measured at 170 K and 360K, respectively.

Referring to Equation (4.37), the DLTS signal should exhibit a dependence on the logarithm of the fill pulse time when the carrier capture is into extended defects.

Figure 7.55 shows the data for levels E1 and E2 in sample OS-d1plotted in accordance with Equation (4.37). An excellent fit was obtained, thus demonstrating that the defects giving rise to these capture characteristics are extended-defect-like states. Similar analysis of the E3 level in sample OS-d2 confirmed that the defects giving rise to this level are point defects. The data show excellent linearity when plotted in accordance with Equation (4.36).

#### 7.5.1.3 Admittance Spectroscopy (AS) Measurements

Admittance spectroscopy (AS) is a slightly less sensitive technique than DLTS [33] as the deep-level response is probed only by a small region and not by the whole spacecharge region as in the standard DLTS technique. However, electric field effects on the ionization energy are more easily controlled with the admittance method [33]. In addition, accurate capture cross section for traps associated with extended defects can be obtained. Although a mode of DLTS can be employed that ensures field consistency, the method is more difficult to control than TAS, hence the use of the latter technique in this report.

Figure 7.56 and Figure 7.57 show AS spectra recorded at  $f_T = 10$ , 50 and 250 kHz for samples OS-d1 and OS-d2, respectively, taken at reverse bias of -3 V and 100 mV ac signal, where G is the measured conductance and  $f_T$  is the probing frequency. Both samples were cooled down in the 450-100 K temperature range. It is worth mentioning that TAS and DLTS experiments were carried out using two different setups but under similar vacuum conditions ~ 10<sup>-4</sup> Pa. In all experiments, the data were recorded using a temperature scan rate 4 K/min.

A dependence of the G/ $\omega$  peak position (in Figure 7.56 and Figure 7.57) and the corresponding capacitance step (in Figure 7.58 and Figure 7.59), on the probing frequency  $f_T$  and/or sample temperature is observed.



**Figure 7.56** Experimental  $G/\omega$  curves as a function of temperature for sample OS-d1.



Figure 7.57 Experimental  $G/\omega$  curves as a function of temperature for sample OS-d2.



**Figure 7.58** Capacitance-Temperature plots for sample OS-d1, recorded with frequencies 50 kHz and 1 MHz, at reverse bias –3 V.



**Figure 7.59** Capacitance-Temperature plots for sample OS-d2, recorded with frequencies 50 kHz and 1 MHz, at reverse bias –3 V.

The  $G/\omega$  vs. T data qualitatively reproduce the behaviour observed in the DLTS experiments, and the activation energies of the trap levels determined by admittance spectroscopy agree fairly well with those calculated from DLTS. Two hole traps  $E1(0.26 \pm 0.04)$  and  $E2(0.58 \pm 0.03)$  were detected in the  $G/\omega$  vs. T spectra of samples OS-d1 and OS-d2, and an additional level E3 (0.36  $\pm$  0.02) was observed only in sample OS-d2. The peaks shift towards higher temperatures with increasing frequency, indicating an increase in hole-emission. It was possible to directly use the conductance peaks occurring at each temperature to construct an Arrhenius plot, the acceptor activation energy and the apparent capture cross-section ( $\sigma_p$ ) of each defect were deduced according to Equation (4.44).

A least-squares fitting procedure yields a straight line, the slope of which corresponds to the trap activation energy, as shown in Figure 7.60. The capture cross sections of all three traps were deduced from the intercept with the vertical axis.



Figure 7.60 Arrhenius plot, derived from the AS spectra of OS-d2.

As illustrated in Table 7.3, admittance spectroscopy offers capture cross section extrapolation (at zero bias) for traps associated with extended defects (E1 and E2).

Trap	$\frac{N_T}{(\text{cm}^{-3})}$	$E_T$ - $E$	<sub>V</sub> (eV)	$\sigma_p (cm^2)$	
		DLTS	AS	DLTS	AS■
E1	5×10 <sup>16</sup>	$0.29 \pm 0.03$	$0.26 \pm 0.04$	n/a <sup>†</sup>	2×10 <sup>-18</sup>
E2	7×10 <sup>16</sup>	$0.53 \pm 0.07$	$0.58 \pm 0.03$	n/a <sup>†</sup>	8×10 <sup>-19</sup>
E3	3×10 <sup>16</sup>	$0.35\pm0.02$	$0.36 \pm 0.02$	3×10 <sup>-15</sup>	$2 \times 10^{-15}$

Table 7.3 Summary of the deep levels calculated by DLTS and AS.

\* Trap concentration calculated from DLTS.

Measured at 0 V.

<sup>†</sup> Accurate values cannot be determined by DLTS as equation (4.36) does not have a linear fit.

The appearance of point-like-defect states in the more highly doped film may be indicative of isolated B-related centres in bulk diamond, whereas the extended states contributing to E1 and E2 in both films may be due to B trapped at grain boundary sites.

### 7.6 Discussion and Conclusions

The main objective of this work was to investigate electrically active defects in thin polycrystalline diamond films deposited by HF-CVD on conducting *p*-type silicon, containing different amounts of boron. The boron concentration in the diamond film ranged from approximately  $8 \times 10^{18}$  cm<sup>-3</sup> to  $9 \times 10^{20}$  cm<sup>-3</sup>, the quality of the produced HF-CVD diamond films was verified by Raman spectroscopy. Different device processing recipes have been carefully investigated to make reliable electrical contacts; Schottky contacts were fabricated on the diamond film and Ohmic contacts on the Si. Assuming a low ionisation rate of the boron in the diamond, the Si resistivity was chosen such that the majority of the depletion region was contained in the diamond.

In addition, a comparison of defects in polycrystalline diamond films grown by different CVD methods, namely HF-CVD and MWP-CVD, as function of B content was attempted. Unfortunately, due to some technical issues with the MWP-CVD growth system (dedicated for boron doping), it was only possible to conduct two successful growths which were not enough to carry out such a comparison.

In this chapter, *I-V*, *C-V*, DLTS and high-resolution LDLTS characterisation techniques were applied to thin polycrystalline semiconducting diamond films, at temperatures up to 690 K. However, a peculiar behaviour was observed at very high temperatures (> 650 K) as well as change in the contact's color that may be due to enhanced diffusion of the Al contacts along grain boundaries. Therefore, further measurements were performed at lower temperatures.

The *C*-*V* analyses of the unannealed samples mostly imply that the carrier concentrations reduce deeper into the sample behind the surface. This can be attributed to the fact that in polycrystalline diamond the areal density of the grain boundaries decreases towards the surface as the layer gets thicker, as discussed in section 2.4. As it is known that B segregates to the grain boundaries in inactive complexes, a larger fraction of the volume being associated with grain boundaries (which is what is found deeper within the film) is likely to result in less active B within the layer, giving rise to more free holes nearer the surface. *C*-*V* analysis of the annealed samples OS-d1 and OS-d2 revealed more uniform carrier concentration-depth profiles; this is possibly due to dissociation of boron-hydrogen complexes at  $750^{\circ}$ C, as these films were vacuum annealed before processing, or may be due to dissociation of grain boundary complexes. CVD diamond growth is inextricably linked to the presence of hydrogen atoms, which are generated as a result of the gas being activated thermally, and so it is probable that B-H complexes are formed during growth.

LDLTS is capable of distinguishing whether a single DLTS peak is due to emission from a unique defect or several defects closely spaced in energy. Several thousand LDLTS capacitance transients were averaged, which ensured that the signal-to-noise ratio was of the order of 1000, which was enough to separate transients with closely spaced emission rates. The LDLTS transient was analysed by three different inverse Laplace transform algorithms, and a plot of peak intensity as a function of emission rate produced. A combination of LDLTS and direct capture cross-section measurements was used to demonstrate whether the electrically active defects present in the material are due to point or extended defects.

Increasing the B content in CVD diamond films from  $1 \times 10^{19}$  to  $4 \times 10^{19}$  cm<sup>-3</sup> and annealing the films resulted in a number of majority carrier traps appearing in the DLTS spectra. In the more highly doped film, E1 was found to contain two closely spaced extended defects. The E2 level in both films consisted of three closely spaced states, all of which were extended in nature, according to their electrical behaviour. The E3 level found in the more highly doped film consisted of two closely spaced levels, both of which are due to point-like defects. Taken with the fact that these levels were not found in the less heavily doped films, this is consistent with them being associated with a B-related centre in bulk diamond.

Fewer shallow defects were detected in the diamond films at ~170 K than deeper at ~400 K, although they mostly exhibited linear dependence of the DLTS peak on the logarithm of the fill-pulse time, demonstrating that the trapping is in defects in the strain field of an extended defect, possibly B segregated to the grain boundaries.

Finally, it was shown that data recorded by DLTS and admittance spectroscopy yielded identical information about the activation energies of deep levels in CVD-diamond films. Accurate calculation of the defect's capture cross-section, using DLTS or admittance spectroscopy, was discussed. This is the first time that admittance spectroscopy and DLTS have been compared for semiconducting diamond.

# References

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# 8. Experimental results from *p*-type GaN diodes

### 8.1 Introduction

GaN based devices have recently attracted a great deal of attention because of their applications in light-emitting diodes (LEDs) and potential for use in high-power, hightemperature and high-frequency electronic devices. However, one of the key bottlenecks in the development of GaN-based devices is accurate control of *p*-type doping. This is due to factors that include the ready compensation of the most usual p-type dopant, Mg, by hydrogen. Hydrogen is unintentionally incorporated in GaN films during growth and processing. The Mg acceptor state is relatively deep in the band gap, with reported values ranging from 120 to 250 eV [1-4]. Coupled with compensation by H, this means that the ionised acceptor concentration at room temperature is significantly below the total Mg concentration. It has also been suggested that there is a significant degree of self-compensation in Mg-doped GaN [5]. A further problem is thought to be the high level of dislocation density in the material, due to the lack of available lattice matched substrates, as most GaN-based LEDs are grown heteroepitaxially on substrates like sapphire, silicon, or silicon carbide. The lattice mismatch between the substrate and the GaN results in the formation of a high density of threading dislocations, usually more than  $10^9$  cm<sup>-2</sup> [6]. The reason that GaN-based quantum wells emit light so efficiently, even though the TDD is high, is not because these dislocations are electrically inactive, but because the carriers are thought to be localised [7], that prevents them diffusing to the dislocations which would otherwise quench the light emission. The interaction of the dopants with these extended defects is not well understood and the subject of ongoing debate [6-12].

In this chapter the effect of threading dislocation density (TDD) on electrically active defects in Mg-doped GaN films grown by MOVPE on (0001) sapphire has been investigated by admittance spectroscopy (AS). The capacitance and conductance of the films were measured as functions of modulation test frequency for temperatures in the

range 200 - 450 K. The variation in TDD was introduced by using different buffer layer schemes between the sapphire substrate and the *p*-GaN film. The technique of reducing TDDs by these layers was developed at Cambridge University by Dr. R. Oliver who provided the materials for this work.

# 8.2 Electrical characterisation of p-type GaN Schottky diodes

The growth of the GaN layers and the metal contact formation is discussed in detail in section 6.3. Table 8.1 gives a summary of the thin film growth details, TDD in each wafer as measured by AFM at Cambridge, and room temperature Hall effect results (measured at Cambridge).

Table 8.1 summary of the samples growth details,	, TDD in each wafer as measured by
AFM, and room temperature Hall effect results	

Wafer No. / Buffer scheme	Mg precursor flux (µmol/min)	TDD (cm <sup>-2</sup> )	Hole Concentration (cm <sup>-3</sup> )
С4022В / А	0.87	~ 2×10 <sup>9</sup>	0.7×10 <sup>17</sup>
С4039В / В	0.87	~ 1×10 <sup>10</sup>	0.9×10 <sup>17</sup>
С4052С/В	0.67	$\sim 1 \times 10^{10}$	0.7×10 <sup>17</sup>
С4041В / В	0.43	~ 1×10 <sup>10</sup>	Not detectable

The measured C-V (at 1 MHz) of the fabricated GaN Schottky diodes did not vary with bias. Therefore, deep level transient spectroscopy (DLTS) experiments could not be applied to the *p*-type GaN diodes discussed in this chapter, because our DLTS system uses a Boonton capacitance meter that can only operate at 1 MHz.

It is also known that the resistivity of the Mg-doped GaN is extremely high below 200 K [13], therefore the capacitance variations at that DLTS temperature range will result in stray values. Hence, for the GaN samples discussed here, admittance spectroscopy was more reasonable than the conventional DLTS measurement.

The *I-V* characteristics of the diodes were recorded using a Keithley 6487 automated system. Admittance spectroscopy measurements were carried out using an Agilent E4980A LCR meter used in the parallel equivalent circuit mode, at zero to -3 V reverse bias with a 50 mV rms value for the small ac signal. The conductance and capacitance of each diode was monitored over a wide range of frequencies and temperatures. The ac signal frequency was varied in the range 100 Hz – 1 MHz and the substrate temperature was varied in the range (140– 450) K by using a closed cycle He cryostat. Further details about the specifications of the equipments used for *I-V* and thermal admittance spectroscopy experiments are given in chapter 5.

#### 8.2.1 *I-V* Measurements

Figure 8.1 illustrates the *I-V* characteristics of Schottky diodes on all four films after etching. Only diodes on samples C4022B (lower TDD) and C4039B (higher TDD) were suitable for comparison and detailed analysis.



**Figure 8.1** The *I*–*V* characteristics of Schottky diodes fabricated on etched Mg-doped GaN films, at room temperature.



**Figure 8.2** The *I-V* characteristics at room temperature for diodes fabricated on unetched Mg-doped GaN films C4022B and C4039B.

For comparison, unetched diode I-V curves are also presented. As illustrated in Figure 8.2, the *I-V* characteristics of the as-cleaned (unetched) diodes exhibited high reverse leakage currents, The current-voltage characteristics showed that the diode on C4022B is slightly less resistive than the diode on sample C4039B, which could be attributed to the lower TDD in sample C4022B, assuming the dislocations capture carriers and reduce current flow. However, both diodes are poor before etching. As a measure of diode quality and to help explain what the effect of the etching is, it is easiest to choose an arbitrary reverse leakage current value, and test at what reverse voltage this value is exceeded. i.e. if we choose  $5.9 \times 10^{-5}$  A, in the unetched sample C4022B the reverse voltage at which this occurs is -0.95 V, and in the unetched sample C4039B it is -1.15 V. After etching both these reverse voltages increase with sample C4022B showing the biggest increase. This means that Sample C4022B is now showing no reverse leakage current up of the chosen test magnitude until at least -10 V. This is interpreted as meaning that an etched diode on Sample C4022B is a higher quality diode

than an etched diode on Sample C4039B. This is clearly shown in Figure 8.3. This has previously been reported and attributed to a decrease in hole concentration in the near-surface region through the creation of shallow states, possibly nitrogen-vacancy related defects [14].



**Figure 8.3** The I-V characteristics at room temperature for plasma etched diodes with different TDDs. The inset shows the log (I) vs. V plot.

The electrical effects of plasma damage in the surface of *p*-type GaN have been reported in the literature [14-20], and surface type conversion has been observed in *p*-GaN at high ion fluxes and high ion energies ( $\geq$ 750 W). It is believed that this Schottky behaviour is associated with more nitrogen-vacancy related defects formed below the *p*-GaN surface, after plasma etching, which lead to an increased Schottky barrier for the transport of holes. It has also been reported [15,16] that plasma etching plays a very important role in the change of electrical properties in *p*-GaN.



Figure 8.4 The I-V characteristics for sample C4022B at different temperatures.



Figure 8.5 The I-V characteristics for sample C4039B at different temperatures.

### 8.2.2 Capacitance Measurements

It is known that the resistivity of the Mg-doped GaN is extremely high; its capacitance drops dramatically at low temperatures and almost vanishes at 200 K [13,21] due to very low dopant ionisation rates. Therefore, the effect of the series resistance on the measured capacitance should be corrected using an equivalent circuit model.



**Figure 8.6** Schematic view of energy band diagram for p-GaN Schottky diode and the parallel equivalent circuit, where  $C_m$  and  $G_m$  are the measured capacitance and conductance respectively. These measured values contain the series resistance effect.

As illustrated in Figure 8.6, the equivalent circuit of that diode is a junction capacitance C in parallel with a junction conductance G (which governs the leakage current) and a series resistance  $R_s$  (which depends on bulk resistivity and on contact resistances).

The complex impedance (Z) of the actual circuit, shown in Figure 8.6, is given by:

$$Z = R_S + \frac{G - j\omega C}{G^2 + (\omega C)^2}$$
(8.1)

Equation (8.1) can be re-written as:

$$Z = Z' + j Z'' = \left[ R_S + \frac{G}{G^2 + (\omega C)^2} \right] - j \left[ \frac{\omega C}{G^2 + (\omega C)^2} \right]$$
(8.2)

whereas the measured complex impedance  $(Z_m)$  is given as

$$Z_{m} = \frac{G_{m}}{G_{m}^{2} + (\omega C_{m})^{2}} - j \frac{\omega C_{m}}{G_{m}^{2} + (\omega C_{m})^{2}} = Z_{m}^{'} - j Z_{m}^{''}$$
(8.3)

where  $C_m$  and  $G_m$  are the measured capacitance and conductance respectively.

The general equation defining the measured complex *admittance*  $(Y_m)$  is given by [22]

$$Y_m = G_m + j \ \omega \ C_m \tag{8.4}$$

$$G_m = \frac{G(1 + R_s G) + R_s(\omega C)^2}{(1 + R_s G)^2 + (\omega R_s C)^2}, \qquad C_m = \frac{C}{(1 + R_s G)^2 + (\omega R_s C)^2}$$

The imaginary component of the measured admittance is directly proportional to the depletion capacitance if the effect of the series resistance is negligible, i.e. If  $(R_sG \ll 1)$  and  $(R_s \ll 1/(\omega C))$ , then  $C_m = C$ . However, for large  $R_s$  and G values ( $R_s > 1 \text{ k}\Omega$  and  $G \approx 10^{-5}$  S), the measured capacitance should be corrected using the above equations.

The admittance is also defined as:

$$Y = \frac{1}{Z} = \frac{1}{Z' - j \, Z''} \tag{8.5}$$

if Equation (8.5) is multiplied by  $\left[\frac{Z'+jZ''}{Z'+jZ''}\right]$  then it can be written as:

$$Y = \frac{Z'}{(Z')^2 + (Z'')^2} + j \frac{Z''}{(Z')^2 + (Z'')^2}$$
(8.6)

Care must be taken if the directly measured depletion capacitance is used to obtain the built-in potential and impurity concentration, as it has been recently reported [23] that analysis of  $C_m vs$ . V data show that the extrapolated built-in potential value increases with increasing frequency. This implies that extrapolating the built-in voltage from a plot of  $1/C^2 vs$ . V is not always valid; there may not be a unique gradient. It is therefore advisable to investigate the measured capacitance as a function of dc bias, frequency and temperature.



**Figure 8.7** An example of the  $Z_m$  vs.  $Z_m$  plots of the AC impedances of a Schottky junction (sample C4022B) at different AC frequencies and constant temperature.

The series resistance can be either estimated from the *I-V* curves [24] for each temperature or by constructing a Nyquist plot from complex impedance measurements [25] as function of bias, frequency and temperature, where  $R_s$  equals the saturation value in the measured real part of the impedance. Equation (8.3) is used at each measurement temperature to estimate the  $R_s$  values, as illustrated in Figure 8.7. The series resistance is determined from the minimum  $Z'_m$  value at the highest frequency.

In this work it was necessary to correct for the high resistivity of all samples during analysis of the admittance spectroscopy data. Due to carrier freeze-out at temperatures below 200 K and the upper temperature limit of our cryostat, admittance spectroscopy was carried out in the temperature range 200-450 K. This was done using a model proposed by Kavasoglu *et al.* [23] based on the equivalent parallel circuit model, in which the corrected impedance (Z) can be calculated using Equations (8.2) and (8.3) by subtracting the series resistance effect from the measured real component  $(Z'_m)$ , at each measurement temperature:

$$Z' = Z'_m - R_s (8.7)$$

$$Z'' = Z''_m (8.8)$$

by substituting (8.7) and (8.8) in (8.6), the real and imaginary components of the corrected admittance can then be re-written as:

$$G = \frac{(Z'_m - R_s)}{(Z'_m - R_s)^2 + (Z''_m)^2} \quad and \quad C = \frac{Z''_m}{\omega \left[ (Z'_m - R_s)^2 + (Z''_m)^2 \right]}$$
(8.9)

The C-f curves in Figure 8.8 shows the corrected capacitance spectra of samples C4039B, C4052C and C4041B, obtained experimentally at zero bias and 50 mV AC signal over the frequency range 100 Hz to 1 MHz and at room temperature.


**Figure 8.8** *C*– *f* spectra for etched diodes over a wide range of frequencies at zero bias with a 50 mV rms value for a small ac signal and T=300 K.

In principle, the presence of a deep level in the measured rectifying junction is determined by a flexion in the *C*-*f* curve and a peak in the (G/ $\omega$  vs.  $\omega$ ) plot. The peak in the (G/ $\omega$  vs.  $\omega$ ) plot occurs at the transition frequency  $\omega_0$  at which the carriers respond, and is defined as the frequency at which the capacitance is half  $\Delta C$ , where  $\Delta C$  is the difference between  $C_{\text{High}}$  and  $C_{\text{Low}}$ , as illustrated in Figure 8.9.



**Figure 8.9** The transition frequency  $\omega_0$ . It could be determined from the *C*-*F* plot or the conductance (G/ $\omega$  vs.  $\omega$ ) plot

Figure 8.8 illustrates that a single flexion point in the C-f curve occurs in all samples of structure (A), but it is more obvious in the higher doped sample C4039B, as expected.

The C-f curves in Figure 8.10 and Figure 8.11 show the corrected capacitance spectra of samples C4022B and C4039B respectively, obtained experimentally at zero bias and 50 mV AC signal over the frequency range 500 Hz to 1 MHz and with the temperature varied from 200 to 450 K. A temperature dependent step-like variation is observed in the frequency range indicating that the inflection frequency  $\omega_0$  can be deduced.



**Figure 8.10** *C*– *f* spectra for sample C4022B at zero bias with a 50 mV rms value at different temperatures



**Figure 8.11** *C*– *f* spectra for sample C4039B at zero bias with a 50 mV rms value at different temperatures

The temperature dependent *C-f* plots show that at sufficiently low frequency, about  $\sim 1.5$  kHz, both samples exhibited almost constant junction capacitances at all temperatures. This agrees very well with the low frequency value reported by J. kim *et al.* [21]. At about 1.5 kHz the capacitance becomes frequency independent, which implies full response of deep Mg acceptors, and hence a *C-V* depth profile can be constructed [22].

The TDD in C4022B is an order of magnitude lower than in C4039B. The capacitance of C4022B measured at zero bias is lower than that of C4039B, which implies a larger depletion region. This is indicative of a less conducting sample, which one may attribute to the lower dislocation density. There is also a temperature dependence involved in the barrier height, which makes detailed analysis extremely problematic. This temperature dependence can be seen in Figure 8.10 and Figure 8.11.

Table 8.2 details the Schottky diode parameters for samples C4022B and C4039B as calculated by C-V and I-V analysis.

Sample C4022B					Sample C4039B				
T (K)	η	(Φ <sub>b</sub> ) <sub>IV</sub> (eV)	$(R_s)_{IV}$ (k $\Omega$ )	(Φ <sub>b</sub> ) <sub>CV</sub> (eV)	T (K)	η	(Φ <sub>b</sub> ) <sub>IV</sub> (eV)	$(R_s)_{IV}$ (k $\Omega$ )	(Φ <sub>b</sub> ) <sub>CV</sub> (eV)
300	3.7	1.21	8.9	2.32	300	4.9	0.88	12.8	1.78
340	3.2	1.35	4.4	2.33	340	3.9	0.99	6.4	1.79
380	2.7	1.50	2.7	2.33	380	3.2	1.10	3.9	1.81
420	2.6	1.52	1.9	2.31	420	2.9	1.24	2.6	1.80

**Table 8.2** Schottky diode parameters for *etched* samples C4022B and C4039B, measured by *I-V* and *C-V* at different temperatures.

For the *C*–*V* method it is important that  $C^{-2}$  versus *V* plots be linear and independent of frequency; however the barrier height obtained using the *C*-*V* method,  $(\Phi_b)_{CV}$ , is hardly affected by the changes in the temperature. The *I*-*V* characteristics for samples C4022B

and C4039B have been analyzed in order to deduce the ideality factor ( $\eta$ ) and the barrier heights from the slope and the intercept of the plot of log (*I*) vs. V.

As shown in Table 8.2, large ideality factors, ( $\eta > 2$ ), were obtained over the measured range of temperatures. These large  $\eta$  values are attributed to the high specific resistance of the *p*-GaN layer.

Barrier heights obtained using the *I-V* method,  $(\Phi_b)_{IV}$ , shown in Table 8.2 are underestimates of the real potential barrier height present at these interfaces due to large  $\eta$ values. However accurate extraction of  $\Phi_b$  using the current-temperature method was impossible because non-linear Richardson plots [22] were observed, due to temperature dependency of the obtained barrier height and the ideality factor values. Linearity could not be restored using modified Richardson plots. ( $\Phi_b$ )<sub>CV</sub> values are over-estimates due to effects of distributions of interfacial charges on *C*–*V* measurements.

A number of theoretical studies and experiments have been carried out by others [26-28] to compare barrier heights determined by I-V and C-V techniques. It was found that generally  $(\Phi_b)_{CV}$  exhibit larger values than  $(\Phi_b)_{IV}$  and this discrepancy was attributed to the existence of two regions of contact area each having a different barrier height, i.e. when two Schottky diodes of different barrier heights are connected in parallel the lower barrier height dominates the I-V behaviour, but the C-V behaviour is dominated by the one with the largest contact area. Furthermore, variations of the barrier height over the contact area can occur as a result of nonuniformity of the interfacial layer thickness, inhomogeneities in the interfacial layer composition and distributions of interfacial charges. Therefore it is more realistic to represent a distribution for the barrier height rather than only two different barrier height values.

#### 8.2.3 Carrier concentration-depth profiles

Figure 8.12 and Figure 8.13 show the carrier concentration-depth profiles obtained at different temperatures for samples C4022B and C4039B, respectively, measured at 1.5 kHz.



**Figure 8.12** The *C*-*V* concentration-depth profiles obtained for diode on sample C4022B. The inset shows the  $1/C^2$  vs. V plot at 300 K, where V<sub>bi</sub> is the built-in voltage.



**Figure 8.13** The *C*-*V* concentration-depth profiles obtained for diode on sample C4039B. The inset shows the  $1/C^2$  vs. V plot at 300 K.

The carrier concentration is larger at the surface in C4039B; it should be noted that the values determined from C-V profiling represent the majority carrier density and not the doping density. There is a noticeable decrease of carriers further behind the surface. The C-V data suggest that there is a highly doped layer, ~  $6 \times 10^{18}$  cm<sup>-3</sup> (C4039B) and ~  $1.5 \times 10^{18}$  cm<sup>-3</sup> (C4022B), that lies around 50-60 nm below the surface of the doped GaN. This thin layer has been previously seen by others [2,29] and is attributed to post growth annealing; an increase in the hole concentration at the surface could be caused by decomposition of Mg-H complexes with the H escaping from the surface. This explains the observation that, in the case of un-etched samples, the sample with higher TDD was slightly more resistive than the one with lower TDD even though they were very similar in dopant concentration and processed together. Additionally, current transport at the metal/high Mg-doped GaN interface was dominated by a deep level defect band induced by high Mg doping, leading to the formation of a low barrier height and larger leakage currents at the Schottky interface. It is suggested here that after post growth annealing the deep level defect band exists with a large defect density of about 10<sup>19</sup> cm<sup>-3</sup>. However, when these films were exposed to plasma etching just before evaporating the metals, the high hole concentration near the surface of samples, dominated by the acceptor-like deep level defects, was reduced to  $\sim 10^{18}$  cm<sup>-3</sup> through the creation of shallow states by the RIE; hence the etched samples exhibited higher barrier height and smaller leakage current. It has also been reported by others [15,16] that dry etching contributes to a shift of the Fermi level towards the conduction band edge in *p*-GaN.

#### 8.2.4 AC Conductance Measurements

Figure 8.14 and Figure 8.15 show the  $(G/\omega vs. \omega)$  curves for samples C4022B and C4039B, respectively, where  $\omega=2\pi f$  and f is the probing frequency.



**Figure 8.14** The zero bias  $G/\omega$  spectra at different temperatures, zero bias and 50 mV ac signal for etched diode on sample C4022B.





The contribution of traps to device conductance is obvious; the frequency peaks shift towards higher frequencies with the increase of measurement temperature, indicating an increase of hole emission rate.

It is possible to directly use the conductance peaks occurring at each temperature to construct an Arrhenius plot and hence the acceptor activation energy and the apparent capture cross section of each defect can be deduced according to the standard equation [30]:

$$\frac{2\pi f}{T_{max}^2} \propto \exp\left(-\frac{E_a}{k T_{max}}\right) \tag{8.10}$$

where  $T_{\text{max}}$  is the temperature at which the conductance peak is occurring and f is the probing frequency for each experiment. A plot of  $ln(\omega/T^2)$  vs. 1/T should give a straight line, the slope of which corresponds to the trap activation energy and the intercept is related to  $\sigma_p$ .



Figure 8.16 Arrhenius analysis for the *G*-*f* peaks indicated at zero bias.

Figure 8.16 shows the Arrhenius plot for the single defect observed in the  $G/\omega vs. \omega$  spectra of both films. The trap energy calculated for the two samples was almost identical at  $160 \pm 5$  meV.

It is worth mentioning that the  $(G/\omega vs. T)$  and  $(G/\omega vs. f)$  experiments were carried out using two different setups but under similar vacuum conditions  $(10^{-6} \text{ torr})$ . However, in the  $(G/\omega vs. T)$  experiments, the conductance data were recorded using a temperature scan rate 4 K/min at a fixed probing frequency for each experiment; this is in principle, similar to the deep level transient spectroscopy (DLTS) experiments [31].







**Figure 8.18** *G*-*T* spectra (temperature scan) taken with different frequencies and an applied reverse bias of -2 V: for an etched diode on sample C4039B.

Figure 8.17 and Figure 8.18 show the temperature dependence of the AC conductance measured at a reverse bias of -2 V and an AC signal of 50 mV, using probing frequencies of 1, 3, 10 and 50 kHz. Both samples were examined in the (430-140) K temperature range. A single peak is clear in the ( $G/\omega vs. T$ ) curves which occurs around 250 K, at low frequency, for both samples C4022B and C4039B. The peak shifts towards higher temperatures with an increase of probing frequency.

Conventional Arrhenius analysis, shown in Figure 8.19, reveals the activation energy of the level responsible for this behaviour as  $170 \pm 5$  meV. No other deep centres were observed in these admittance spectroscopy experiments. The estimated trap energy levels are most probably associated with the Mg acceptor state as these values are consistent with the values reported in the literature [1-4]. The *G*-*T* results qualitatively

reproduce the behaviour observed in the G- $\omega$  experiments; this demonstrates that conductance methods are powerful tools for obtaining information on defect physics.



**Figure 8.19** Arrhenius analysis for the *G*-*T* peaks indicated at  $V_{B}$ = -2 V.

The temperature dependencies of the thermal velocity contained in the capture coefficient and  $N_v$  were then considered. Equation (4.39) was divided by  $T^2$  and the term  $(v_{th} \times N_v)$  was replaced by (*Constant* x  $T^2$ ) where  $v_{th} = (3k/m_h^*)^{1/2}.T^{1/2}$ , k is the Boltzmann constant and  $N_v = 8.9 \times 10^{15}.T^{3/2}$ . It was assumed that the effective hole mass for wurtzite GaN is  $m_h^* = 0.8 m_0$  and the acceptor degeneracy factor g is 4. From the extrapolated intercept values of  $\ln(\omega/T^2) vs$ . 1/T plots, the apparent  $\sigma_p$  were estimated to be approximately  $\sim 1 \times 10^{-20}$  cm<sup>-2</sup> for all the samples. The very small  $\sigma_p$  values indicate that the ionised acceptor level is very repulsive which, if the situation is very simple, is not logical; however, Ga vacancies are assumed to defects associated with, or in close

proximity to, a negatively charged gallium vacancy. This interpretation should be considered alongside the fact that it is well known that extrapolated capture cross sections can have error bars of several orders of magnitude.

### 8.3 Discussion and Conclusions

In summary, a hole trap with an activation energy of  $160 \pm 10$  meV was found in samples with the same Mg content and different TDDs. The capture cross-section of this defect was estimated to be  $1 \sim 2 \times 10^{-20}$  cm<sup>2</sup>. Both these values lie within the range of previously reported values for Mg in GaN (120 - 250 meV), therefore, the traps that give rise to the signals in the G/ $\omega$  plots are assumed to be associated with the Mg dopant. The very small capture cross-section indicates that the trap is repulsive, which is not what would be expected of an ionised acceptor level. It is postulated that this may be partly an artefact of the extrapolation technique, and partly due to the presence of other defects near to the Mg acceptors which affect the apparent capture cross-section of the Mg acceptor state.

No shallow traps associated with threading dislocations were observed in these samples. Changing the TDD by an order of magnitude had no effect on the admittance spectra recorded from these films. This was an unexpected result, as cathodoluminescence (CL) studies on *p*-GaN films clearly show that most threading dislocations are non-radiative recombination centres [7, 33]. It is known that as dislocation states capture carriers and cause the dislocation to become charged, Coulombic repulsion means that the dislocation is less likely to capture further carriers [34]. As the admittance spectroscopy technique used in this work measures hole emission and is at relatively low measurement frequencies, any electrically active dislocation-related states would have ample time to fill up and influence the admittance spectra. Therefore the result can be correlated with the CL experiments by suggesting that the electrical activity of dislocations in GaN is primarily due to electron capture and emission. These are assumed to be close to zero electrons in these samples.

There have been reports in the literature for n-type GaN that some deep levels are only readily activated by optical excitation techniques, such as deep level optical spectroscopy and photocapacitance spectroscopy [35]. Cathodoluminescence would also be expected to be able to probe these very deep levels.

In conclusion, there was not any influence of the TDD on the relatively shallow traps detected in this work. If there are very deep electrically active levels associated with the dislocations, they are unlikely to be ionised at device operating temperatures such as those probed in this work, and therefore have not influenced our results.

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# 9. Summary and future work

#### 9.1 Conclusions from CVD diamond films

Deep electronic levels in boron-doped polycrystalline diamond films, with different boron levels, have been investigated experimentally using *I-V*, *C-V*, DLTS, high-resolution LDLTS and thermal admittance spectroscopy (TAS). Increasing the B content in CVD diamond films from  $\sim 1 \times 10^{19}$  to  $\sim 4 \times 10^{19}$  cm<sup>-3</sup> and annealing the films at 750°C resulted in a number of hole traps appearing in the DLTS spectra. The films with B concentrations larger than  $\sim 6 \times 10^{20}$  cm<sup>-3</sup> exhibited semi-metallic behaviour.

The data reported in this thesis, recorded by DLTS and TAS, yielded identical information about the deep levels in CVD-diamond films; these were identified by DLTS and TAS as hole traps. To the best of our knowledge, this is the first time that admittance spectroscopy and DLTS have been compared for semiconducting diamond.

Despite the polycrystalline nature of the diamond films and the difficulty of using LDLTS on such a defective material, still there is a very clear and accurate LDLTS result for the B acceptor in the more highly doped film of batch D (sample OS-d2). However, all the other LDLTS results are complex and really only confirm that there are many extended defects contributing to the DLTS signal.

Finally, it was discussed that a combination of LDLTS and direct capture cross section measurements can be applied to semiconducting diamond to understand whether the trapping is at an isolated point defect or an extended defect. It is suggested that the appearance of point-like-defect states in the more highly doped film (in batch D) are indicative of B-related centres in bulk diamond, whereas the extended states may be due to B trapped at grain boundary sites.

## 9.2 Conclusions from Mg doped GaN films

Mg:GaN thin films were grown on sapphire by MOVPE using two different buffer layers giving rise to differing threading dislocation densities (TDDs) in the GaN. TAS was applied to study the effect of different TDDs on the electronic states in the bandgap of the Mg:GaN.

An electrical trap with an activation energy of about  $165\pm10$  meV was observed using TAS. Data were recorded from two different AC conductance experiments ( $G/\omega vs. \omega$  and  $G/\omega vs. T$ ) for each sample. The obtained activation energy values equate well with the range of previous values reported for Mg in GaN. It is demonstrated that the observed energy levels exhibit repulsive capture characteristics which could be due to defects associated with a negatively charged gallium vacancy.

The *I-V* and *C-V* characteristics illustrate that the electrical properties have been slightly affected by the occupancy of interface traps and the various charge polarities which govern the Fermi level pinning and lead to an increased Schottky barrier for the transport of holes in the sample with higher TDD. However after correcting the effects of series resistances, only majority carrier traps (peaks) above 200 K were detectable using AC conductance measurements. No traps associated with TDs were observed in the samples.

This study detected no deep levels that can be ascribed to the TDs. It is shown by two different techniques that the Mg level can be detected, and it is concluded that the presence of different concentrations of TDs do not significantly affect the electronic deep level populations in the materials. This interesting finding has relevance to optical device properties, as it shows that the threading dislocation density may not be a first order effect when considering how to increased optical efficiency. From these studies it can be concluded that the use of different buffer layer schemes appears to have no significant effect on the obtained energy levels or trap concentrations.

### 9.3 Future work

It is shown in this work that it was only possible to examine a temperature range of 100 - 450 K, and this temperature range is not sufficient to probe levels very deep in the band gap. Increasing the temperature much beyond 450 K causes the contacts to degrade in both materials studied, possibly by pipe diffusion down dislocations and grain boundaries intersecting the surface.

Combined electrical and optical techniques such as optical-LDLTS could be used to examine defects in wide bandgap materials. The use of such technique would allow probing of levels very deep in the band gap, by the use of optical and thermal excitation. Cathodoluminescence would also be expected to be able to probe these very deep levels.

Many high work-function metals have been investigated in the literature in order to obtain low-resistance contacts to *p*-type GaN; either in the form of standard contact design or complex metallization schemes. So far, experimental results show that Ni/Au contacts (if annealed at temperatures between 400 and 600°C in nitrogen/air mix) exhibit the lowest resistance on *p*-type GaN. Resistivities in the range of  $10^{-4}$  to  $10^{-6} \Omega$ .cm<sup>-2</sup> have been reported [1-3]. However, there is still an issue with the stability of the Ni/Au contacts; it is suggested [1-2] that the Ni atoms escape from the *p*-type GaN surface and hence the interface between Au and *p*-GaN leads to poor electric performance, resulting in high resistivity contacts. The nature of the resistivity of Ni/Au contacts after annealing in an ambient atmosphere containing oxygen and nitrogen is still not fully understood. The processes taking place during contact formation, e.g. contact transformation during annealing, still need to be investigated.

On the other hand, current research [4- 6] is focusing on finding a more reliable Ohmic contact for improving the performance of LEDs; very recent studies [6] propose that Pt/Ag/Ni/Au could act as a promising metal contact to *p*-type GaN. The properties of this metallization scheme needs to be thoroughly investigated.

In semiconducting diamond, there are a number of issues that still need to be looked at; among these is the polycrystalline nature of the hetroepitaxially-grown diamond films. These films tend to contain large volume of grain boundaries, dislocations and other defects, that reduce the carriers lifetime and mobility by trapping B atoms and rendering them inactive, despite high doping levels. A comparison, by electrical testing, of electrically active defects in CVD diamond grown on either single crystal CVD diamond or HPHT diamond with different boron levels could be very useful to study the electrical properties of point defects in B-doped diamond. In addition, CVD diamond layers could be grown side by side in the hot filament reactor so their B levels will be virtually identical. There is no report in the literature on a comparison of such layers by electrical testing.

Furthermore, the difficulty in producing n-type diamond remains the outstanding problem in the development of diamond optical devices. However, co-doping the diamond with more than one element to produce n-type has not been satisfactory, and also the tight bonding and rigidity of the diamond lattice makes incorporation of doping atoms larger than C really difficult. This opens up another research area to find alternative n-dopants to those routinely used to n-dope Si, such as P or As.

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