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Investigating the electronic properties of multi-junction ZnS/CdS/CdTe graded bandgap solar cells

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Abstract

The fabrication of multi-junction graded bandgap solar cells have been successfully implemented by electroplating three binary compound semiconductors from II-VI family. The three semiconductor materials grown by electroplating techniques are ZnS, CdS and CdTe thin films. The electrical conductivity type and energy bandgap of each of the three semiconductors were determined using photoelectrochemical (PEC) cell measurement and UV-Vis spectrophotometry techniques respectively. The PEC cell results show that all the three semiconductor materials have n-type electrical conductivity. These two material characterisation techniques were considered in this paper in order to establish the relevant energy band diagram for device results, analysis and interpretation. Solar cells with the device structure glass/FTO/n-ZnS/n-CdS/n-CdTe/Au were then fabricated and characterised using current-voltage (I-V) and capacitance-voltage (C-V) techniques. From the I-V characteristics measurement, the fabricated device structures yielded an open circuit voltage (V_{oc}) of 670 mV, short circuit current density (J_{sc}) of 41.5 mAcm^{-2} and fill-factor (*FF*) of 0.46 resulting in ~12.8% efficiency when measured at room temperature under AM1.5 illumination conditions. The device structure showed an excellent rectification factor (*RF*) of $10^{4.3}$ and ideality factor (*n*) of 1.88. The results obtained from the C-V measurement also showed that the device structures have a moderate doping level of 5.2×10^{15} cm^{-3}.

Keywords: Electrodeposition, buffer layer, graded bandgap device structures, n-n-n+Schottky barrier.

1.0 Introduction

Numerous research works have been carried out on CdS and CdTe binary compound semiconductors due to their suitability in photovoltaic applications. CdTe which has a high absorption coefficient of 10^4 cm^{-1} [1] and an optimum bandgap of 1.44 eV [2] for single bandgap p-n junction has proven to be a suitable absorber layer partner to CdS thin films. CdS/CdTe solar cells with efficiencies over 10% have been achieved at laboratory scale level by various research groups [3–8]. Diverse techniques such as sputtering, physical vapour deposition [9], closed space sublimation [2,3], electrodeposition [10–13] and molecular beam epitaxy [14] have been used for the development of CdTe-based solar cells. First Solar Company has recently announced the highest efficiency of 22.1% for this device structure [15].

CdS has been a suitable window layer to CdTe-based solar cells [2] and researchers working on photovoltaic (PV) materials have identified some factors which cause a reduction in the CdS/CdTe solar cell efficiency. One of the identified factors which cause a reduction in the efficiency of CdS/CdTe based solar cell is the formation of pinholes [16]. Non-uniformity of the CdS window layer can lead to the formation of pinholes after annealing. This non-uniformity is mostly experienced when the CdS layer is very thin ~(40-80) nm. Thus, the presence of pinholes will create shunting paths within the device structure.

This unwanted shunting paths cause a reduction in all three solar cell parameters and the overall solar cell efficiency. Therefore, to prevent the formation of pinholes on CdS layer after annealing, a thicker CdS thin film (>200 nm) is needed. One major disadvantage of using thick CdS is that it causes the short circuit current density (J_{sc}) to reduce under illumination [16,17]. To prevent further degradation of solar cell parameters such as the J_{sc}, open circuit voltage (V_{oc}) and fill factor (*FF*) through the use of very thin CdS layer, a buffer layer with higher bandgap than that of CdS is needed as an intermediate layer between the conducting substrate and CdS window layer [18]. With the incorporation of buffer layer, the CdS thickness can still be maintained at thickness <200 nm without necessarily causing a loss in the V_{oc} and *FF*.

In the experimental investigations reported by Ferekides et al. [16], the authors showed that collection of charge carriers is improved with the use of high-resistive buffer layers. The most effective buffer layers according to Ferekides at al. [16] are Cd_2SnO_4/Zn_2SnO_4. Semiconductor materials containing Zn element such as ZnO [19–21], ZnS [22] and Zn_{1-}

$_xSn_xO$ [18] are generally being preferred as buffer layers to CdS/CdTe solar cells due to their large bandgaps and high resistivities. The fabrications of multi-junction solar cells have been demonstrated by researchers in the field. Rios-Flores et al. [21] achieved CdTe solar cell efficiency between 14-14.6% using the structure ITO/ZnO/CdS/CdTe/Cu/Mo. The authors used the CSS technique to deposit CdTe at a substrate temperature of 500^oC. Oladeji et al. [23] also applied the CSS technique to deposit CdTe absorber layer and achieved a 10% efficiency using $Cd_{1-x}Zn_xS$/CdS/CdTe solar cell structure. Using electroplating technique, Echendu et al. [22] was also able to produce ~10.4% efficient solar cells using the device structure glass/FTO/n-ZnS/n-CdS/n-CdTe/Au. The device structures developed by these authors are multi-junction solar cells since the solar cells have more than one junction. The experimental works carried out by these authors showed that the CdS/CdTe solar cell efficiency can be enhanced by the incorporation of buffer layer. These buffer layers therefore help in minimising pinholes formation which causes shunting in two-layer CdS/CdTe solar cells [16].

In this work, we report the fabrication of glass/FTO/n-ZnS/n-CdS/n-CdTe solar cell using combination of two n-n heterojunctions (HJ's) and a large Schottky barrier at the interface between the n-CdTe absorber layer and Au metal contact [24]. The present work is an improvement over the earlier works reported by Echendu et al. [22] in using glass/FTO/n-ZnS/n-CdS/n-CdTe/Au for solar cell fabrication. Improvements have been seen in this work as compared to the previous investigations reported by the earlier mentioned authors after successfully optimising the thickness of the three semiconductor layers and post-growth treatment used for the device structures. The highest efficiency reported by Echendu et al. [22] was ~10.4% while in this present work, we have been able to improve the device efficiency to ~12.8%.

Earlier work carried out by Echendu et al. [22] also showed that the three-layer device structure (glass/FTO/n-ZnS/n-CdS/n-CdTe/Au) is better in terms of solar cell performance than the two-layer device structure (glass/FTO/n-CdS/n-CdTe/Au). Also, in our earlier conference presentations, we reported and compared the electronic parameters obtained from glass/FTO/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures [25]. We also observed experimentally that the three-layer device structures have a higher solar-to-electric conversion efficiency than the two layer device structures. Therefore the focus of this paper is not on comparison but to further investigate the electronic properties of the

glass/FTO/n-ZnS/n-CdS/n-CdTe/Au multi-junction graded bandgap solar cells using current-voltage (I-V) and capacitance-voltage analytical techniques.

2.0 Experimental Details

The three semiconductor materials used in this experimental work were prepared using electroplating technique with a two-electrode set up. The ZnS thin films were cathodically electrodeposited on glass/fluorine-doped tin oxide conducting substrate from an aqueous solution containing 0.15 M $ZnSO_4$ (with a purity of 99.999%) and 0.15 M $(NH_4)_2S_2O_3$ (98% purity) in 400 ml of de-ionised water. Full details of the ZnS material characterisation techniques can be found in the work published by Madugu et al. [26]. The electrodeposition of CdS thin films were also carried out from an acidic aqueous solution containing 0.3 M $CdCl_2$ and 0.03 M $(NH_4)_2S_2O_3$; full details of this work have been reported by Abdul-Manaf et al. [27]. The CdTe layers were electroplated from the electrolyte containing 1 M $CdSO_4$ (99.999% purity) and 2 ml of dissolved TeO_2 (99.995% purity) in an aqueous medium, containing 800 ml of de-ionised water. After taking the cyclic voltammogram of the electrolyte to determine the suitable voltage range to grow nearly stoichiometric CdTe layer, an optimised cathodic potential of 1400 mV was obtained to carry out the CdTe electrodeposition. Full details related to this work have also been published by Fauzi [28]. A ZnS thickness of ~100 nm was electroplated on glass/FTO substrate. CdS thin film of ~150 nm was electroplated on glass/FTO/ZnS substrate while CdTe of ~1.2 µm thickness was electrodeposited on glass/FTO/n-ZnS/n-CdS structure. It should be noted that after the electrodeposition of each of the layers used in the device structure starting from the deposition of n-ZnS on glass/FTO conducting substrates, the samples were cleaned with de-ionised water, blown with nitrogen gas and annealed before the deposition of the next layer. The cleaning process is necessary to remove any surface contaminations which can introduce surface states to the device structure. The annealing process is also essential to improve the material crystallinity since as-deposited semiconductor materials exhibit poor performance when used in solar cell fabrication.

The complete device structure, glass/FTO/n-ZnS/n-CdS/n-CdTe was rinsed using organic solvents like methanol, washed in de-ionised water and blown with nitrogen gas before treating the CdTe top surface with a saturated $CdCl_2$ solution. After the $CdCl_2$ solution was dried up, the device structure was then annealed in a temperature controlled furnace at 400^oC for 10 minutes in air. After the annealing, the device structure was allowed to cool down,

rinsed in de-ionised water and blown with nitrogen gas again before chemical etching. The etching process is important to remove any surface defects such as residual from $CdCl_2$ treatments and other possible oxides that may be formed on the CdTe top surface due to air annealing [8] . The acidic etching was carried out for ~5 seconds in an aqueous solution containing concentrated H_2SO_4 acid and potassium di-chromate ($K_2Cr_2O_7$) while the basic etching was performed for ~120 seconds in an aqueous solution consisting of $Na_2S_2O_3$ and NaOH. Details on the preparation of the acidic and basic etchants have been reported in one of our previous communications [29]. After completing the etching process, the device structure was rinsed in de-ionised water and blown with nitrogen gas before transferring it to a metal coating vacuum system (Edwards Auto 306 vacuum evaporator) where circular Au contacts of 2 mm diameter and ~100 nm thicknesses were evaporated on the device structure. The solar cell active area is ~0.031 cm^2. The deposition of Au contacts on n-CdTe form a large Schottky barrier at the n-CdTe/Au interface [29]. The final device structure now becomes glass/FTO/n-ZnS/n-CdS/n-CdTe/Au which is a combination of two heterojunction device structures namely n-ZnS/n-CdS and n-CdS/n-CdTe with a large Schottky barrier at n-CdTe/Au interface. The metal coating system was maintained at a pressure of 10^{-6} mbar to ensure a high vacuum system during evaporation of Au. The high vacuum system is essential to prevent the top surface of the etched CdTe layer from oxidising. Oxidation of the CdTe top layer if not properly controlled can lead to increase in the material resistivity which may not be helpful to promote device efficiency.

2.1 Energy band diagram of n-n-n+SB device structure

Before using the electroplated layers for solar cell fabrication, the materials were first characterised for their electrical and optical properties. The electrical signals obtained from photoelectrochemical (PEC) cell measurements showed that all the three semiconductor layers used in the graded bandgap structure were n-type in electrical conduction. The PEC cell comprises of a semiconducting electrode with the structure glass/FTO/semiconductor, a counter electrode from a carbon rod, and liquid electrolyte produced from 0.1 M $Na_2S_2O_3$. Both electrodes are inserted in a liquid electrolyte and connected to a digital voltmeter. The differences between voltages across the two electrodes under dark and light conditions give rise to the PEC signal. While the sign of the PEC signal indicates the electrical conductivity type, the magnitude reveals the level of the doping density of the semiconductor material [30].

It is essential to know the electrical conductivity type of these materials so as not to assume the device structure of the final solar cell being fabricated. The results from PEC cell measurements also help to determine the shape of the energy band diagram. Another important material parameters needed to obtain the actual energy band diagram of the device structure is the energy bandgap obtained from optical absorption measurement characterisation technique. Figs. 1 (a), 1 (b) and 1 (c) show the results of optical absorption measurements obtained for electroplated and heat-treated ZnS, CdS and CdTe layers respectively. The energy bandgaps obtained from Figs. 1 (a-c) are 3.70, 2.42 and 1.50 eV respectively. With the higher bandgap of ZnS layer, pinholes can be minimised while bandgap grading is introduced to the device structure during heat treatments. This unique property makes the ZnS thin film suitable for use as a buffer layer to CdS/CdTe solar cells.

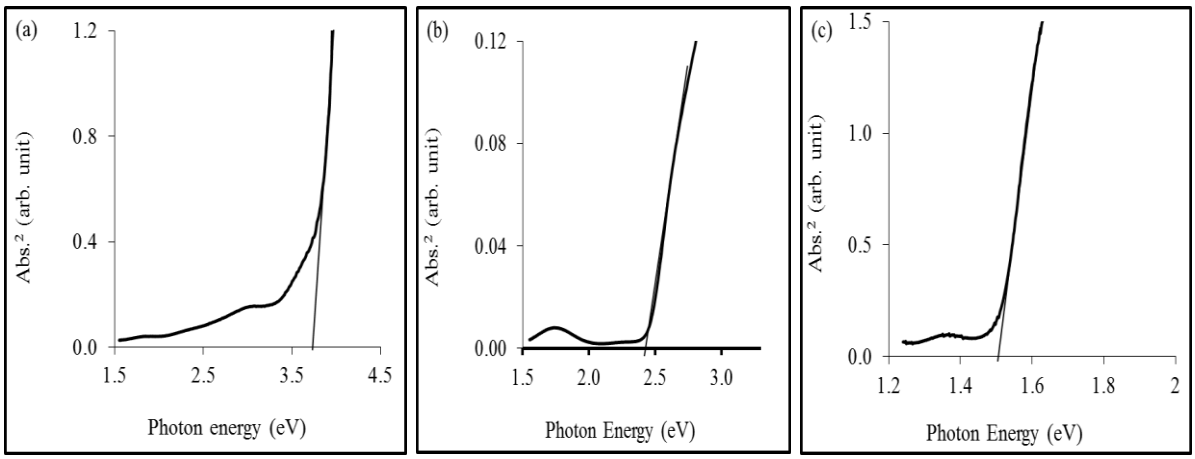

Fig. 1. Optical absorption measurements of (a) ZnS layers heat-treated at 300^{o}C for 10 minutes in air (b) CdS layers annealed at 400^{o}C for 20 minutes in air and (c) CdTe layers annealed with $CdCl_2$ treatment at 400^{o}C for 10 minutes in air.

The energy band diagram for n-n-n+SB device structure is shown in Fig. 2. The formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} ternary compound semiconductors are illustrated in Fig. 2. As explained by Echendu et al. [22], the formation of $Zn_xCd_{1-x}S$ at the interface between the ZnS/CdS HJ is due to the interdiffusion of Zn and Cd during annealing process. The same explanation applies to the formation of CdS_xTe_{1-x} at the CdS/CdTe interface. Due to heat-treatment, S and Te interdiffuse to form CdS_xTe_{1-x}. Chu et al. [31] explained that treating the CdTe surface with $CdCl_2$ solution causes a reaction to take place at the interface between CdS and CdTe thin films thus producing a thin layer of CdS_xTe_{1-x}. According to Potter et al.

[32], the formation of CdS_xTe_{1-x} alloy near the CdS/CdTe interface is being promoted through the $CdCl_2$ annealing process.

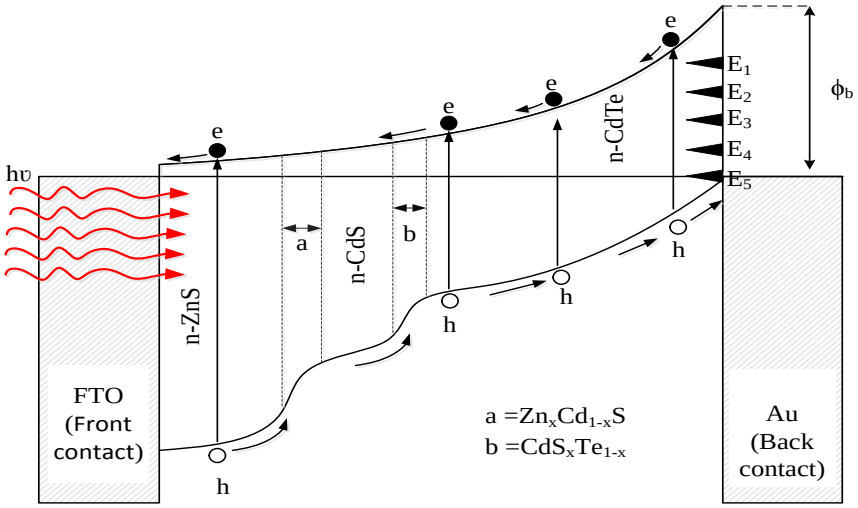

Fig. 2. Energy band diagram of n-n-n+SB device structure showing the formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} as a result of interdiffusion of atoms at two different interfaces during annealing. Note that the above energy band diagram is not drawn to scale.

Apart from ZnS functioning as a buffer layer, the incorporation of ZnS into the CdS/CdTe HJ likewise leads to the formation of graded bandgap device structure as described in Fig. 2. Also, the formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} tend to contribute to the bandgap grading of the device structure. Due to the graded bandgap structure, there is therefore a high tendency for this device structure to start absorbing high energy photons from the blue-end and low energy photons from the infrared region of the solar spectrum. This therefore maximises optical absorption from the solar spectrum, minimises thermalisation and improve collection of photo-generated charge carriers [33]. Since there is no p-layer in this device structure, the depletion region is therefore formed at the band bending created at the metal/semiconductor (n-CdTe/Au) interface. The depletion region provides a strong electric field to separate the photo-generated charge carriers created within the device structure. The fast separation of the photo-generated electrons and holes to the external circuit reduces the recombination of these charge carriers within the device structure. This therefore leads to generation of higher short circuit current density.

Due to the difference in the energy bandgap of these materials, the slope of the energy band diagram which represents the built-in electric field can be improved upon. Therefore, the

formations of n-n HJ at the ZnS/CdS and CdS/CdTe interface also complement the creation of the built-in electric field within the device. The fabrication of rectifying n-n and p-p semiconductors have been well demonstrated by researchers in the field [34]. Due to the presence of defect states, it is difficult to have an ideal interface at the n-CdTe/Au contact. The existence of these states (shown as E_1 to E_5 in Fig. 2) in the bandgap introduce strong pinning of the Fermi level and with an adequate surface processing of the absorber layer, the Fermi level can be pinned at E_5 which is close to the valence band (VB). Due to this Fermi level pinning effect, the potential barrier height is not always a dependant of the metal work function [29]. Existence of experimentally observed defect levels (E_1-E_5) is a real cause for reproducibility; and for high efficiency devices, Fermi level should be pinned at E_5 level closer to the valence band.

3.0 Device characterisation using current-voltage (I-V) technique

It is important to measure the solar cell parameters under dark and illumination conditions so as to fully characterise the diode and photovoltaic parameters. Under the dark condition, the diode parameters are obtained from the log-linear and linear-linear characteristics. The Log I versus V for n-n-n+SB is shown in Fig. 3 (a). The parameters obtained from Log I vs V curve were: rectification factor (*RF*), ideality factor (n), reverse saturation current (I_o), potential barrier height (ϕ_b); from the linear-linear I-V curve, the series resistance (R_s) and shunt resistance (R_{sh}) were obtained from the high forward and reverse regions of the curve respectively. The *RF* obtained for diodes fabricated from n-n-n+SB device structure under dark condition is $10^{4.3}$. As reported by Dharmadasa [30], *RF* of $10^{3.0}$ is sufficient to obtain over 12% efficiency from the CdTe-based solar cells. For the CdTe-based solar cells with lower efficiency, it is therefore possible to have *RF* of lesser orders of magnitude as observed in our previous work [25]. The value of the ideality factor helps to determine the type of current transport mechanism which takes place within the device structure. For the solar cells fabricated and reported in this work, the ideality factor of 1.88 was obtained. This shows that two current transport mechanisms (thermionic emission and recombination and generation (R&G) process) take place in parallel [30]. As reported by Rhoderick, n>1.00 due to carrier recombination [35]. When n>1.00, the ϕ_b is always being underestimated.

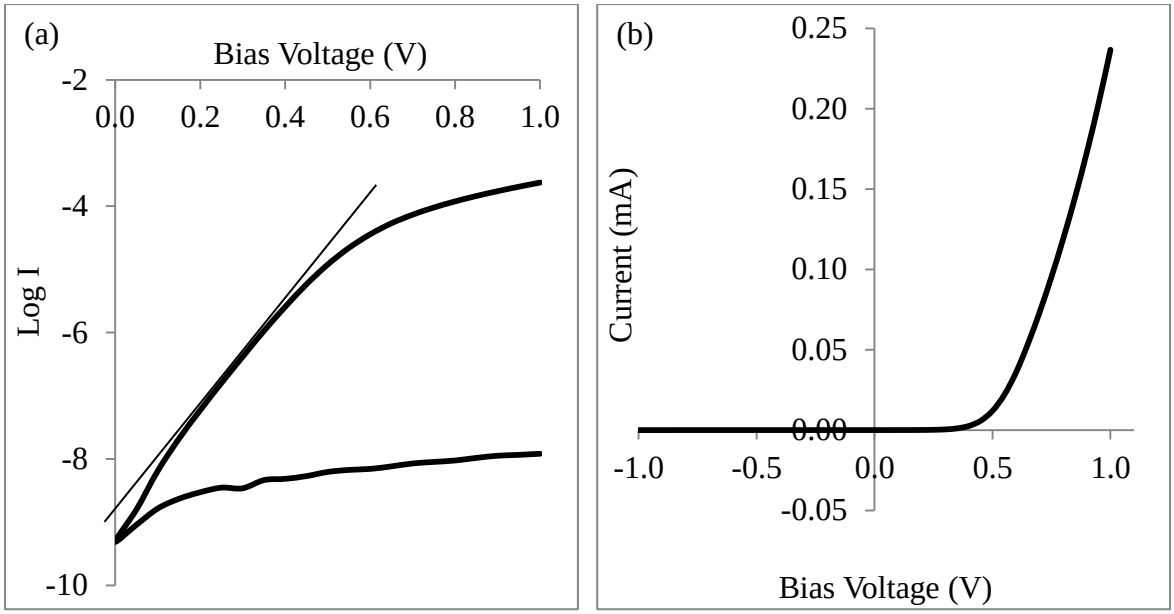

Fig. 3. I-V characteristics of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au (n-n-n+SB) device structure under dark condition plotted in (a) Log-linear and (b) Linear-linear scales.

The I_o is obtained from the intercept of the straight line section of best tangent of the forward current curve on the Log I axis. The obtained I_o value is 0.79 nA. This I_o value was used in estimating the barrier heights. The estimated ϕ_b for n-n-n+SB diode is >0.81 eV. The *n* value <2.00, high *RF* and larger ϕ_b obtained for n-n-n+SB diode illustrate how healthy the depletion width of the device structure is. It also shows the strength of the electric field produced in the depletion region. The healthy depletion region and strong electric fields work together to effectively separate and transfer the photo-generated electrons and holes to the external circuit. This explains the reason for the high J_{sc} observed in the n-n-n+SB device structures.

The linear-linear dark I-V curve for n-n-n+SB device structure is shown in Fig. 3 (b). The R_s and R_{sh} values as estimated from Fig. 3 (b) are ~1351 Ω and 81 MΩ respectively. The shape of the reverse curve of diode in Fig. 3 (b) showed infinite R_{sh}. Our previous conference presentations showed that the incorporation of ZnS as a buffer layer in to the CdS/CdTe device structure leads to a great improvement in the R_{sh} [25]. The presence of large R_{sh} indicates that the leakage paths for the photo-generated charge carriers are minimised; therefore, the amount of current loss through the leakage path is reduced and the current that flows through the external circuit will increase and this eventually leads to an improvement in the cell performance. With reduced leakage current paths, an improvement in the J_{sc} is expected. This improvement was observed in the experimental work with n-n-n+SB device structures.

The J-V characteristics of n-n-n+SB solar cells carried out at room temperature under AM1.5 illumination condition is shown in Fig. 4. The solar cell parameters obtained were V_{oc} = 670 mV, J_{sc} = 41.5 mAcm^{-2}, FF = 0.46 and η = ~12.8%. The estimated R_s and R_{sh} under light are ~134 Ω and ~3819 Ω respectively. The reduction of the R_s from ~1351 Ω under dark condition to ~134 Ω under AM1.5 illumination condition shows that the fabricated solar cell has a good photo conductivity effect. The low R_s value also helps in enhancing the J_{sc} value. Some of the other possible reasons for high J_{sc} value have been summarised in the previous section and in one of the recent review paper [22]. Also the larger bandgap of ZnS (~3.70 eV) in the front of the device structure has assisted in creating a steep slope to ease the transportation of electrons to the front contact. In this device structure, all three layers are active in PV conversion and the thermalisation effects are minimised.

The J_{sc} of 41.5 mAcm^{-2} obtained from the measured cells of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells are higher than the reported J_{sc} limit [36] for single p-n junction CdTe solar cell. This increase can be attributed to the graded bandgap structures used in this work [12]. To ensure the authenticity of the J_{sc} observed in this work, the surrounding CdTe layers were carefully removed to ensure that current is not being collected from the immediate CdTe surrounding layers. It was observed that after carefully removing the surrounding CdTe layers around the gold contact, the J_{sc} still remains. This shows that there was no lateral current collection around the measured solar cell contact in these devices. As suggested by Basol [37], the absence of current collection from the surroundings can be mainly due to the high resistivity and ultra-thin CdTe layers being used as an absorber. Due to the grading of the device structure, it is also possible to have the presence of impurity PV effect and impact ionisation. When either or both phenomena are present in a device structure, there is high tendency for the J_{sc} to rise. Multi-junction graded bandgap solar cells such as the n-n-n+SB or n-n-p provide effective means of harvesting photons from various regions (UV, Vis, and IR regions) of the solar spectrum [38].

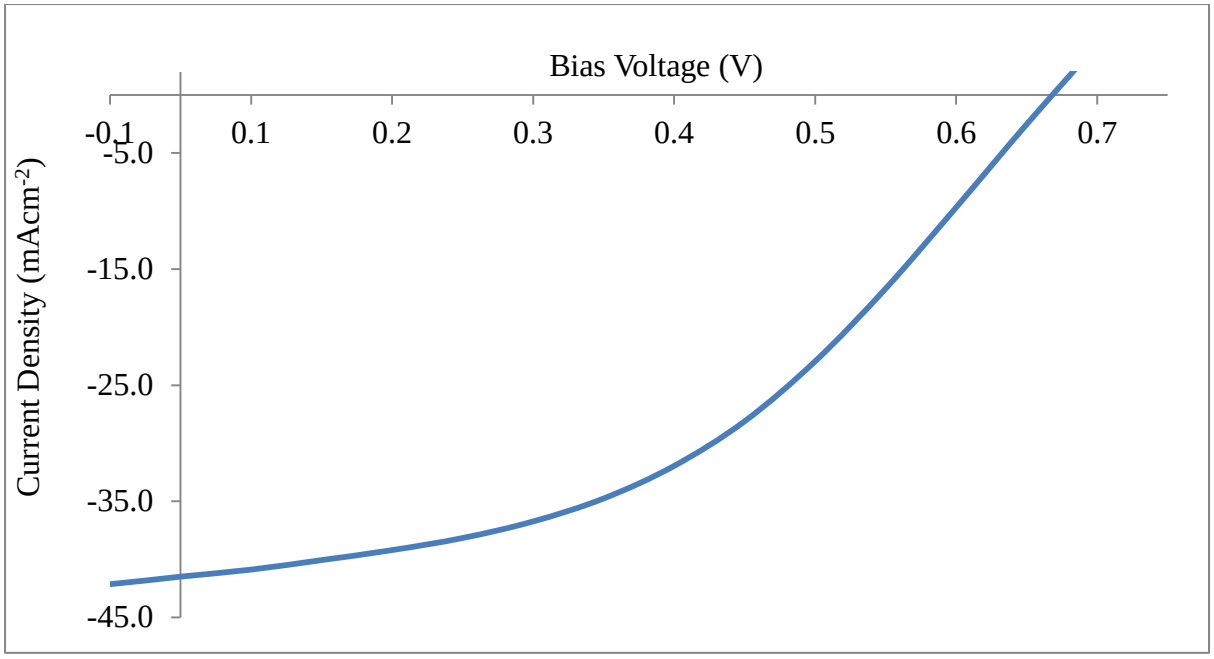

Fig. 4. I-V characteristics of n-n-n+SB device structure under AM1.5 illumination condition.

3.1 Device characterisation using capacitance-voltage (C-V) measurement technique

The depletion capacitance and the doping density of the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structure have been determined using the C-V characterisation technique. The C-V measurements were carried out under dark condition at room temperature using AC frequency of 1 MHz. Figs. 5 (a) and 5 (b) show the C-V characteristics and Mott-Schottky plots of the n-n-n+SB device structures respectively. The depletion capacitance of the n-n-n+SB multi-junction solar cell at zero bias is 264 pF as shown in Fig. 5 (a). This value remains fairly constant with applied bias from the reverse region to the forward bias at V=~0.2 V.

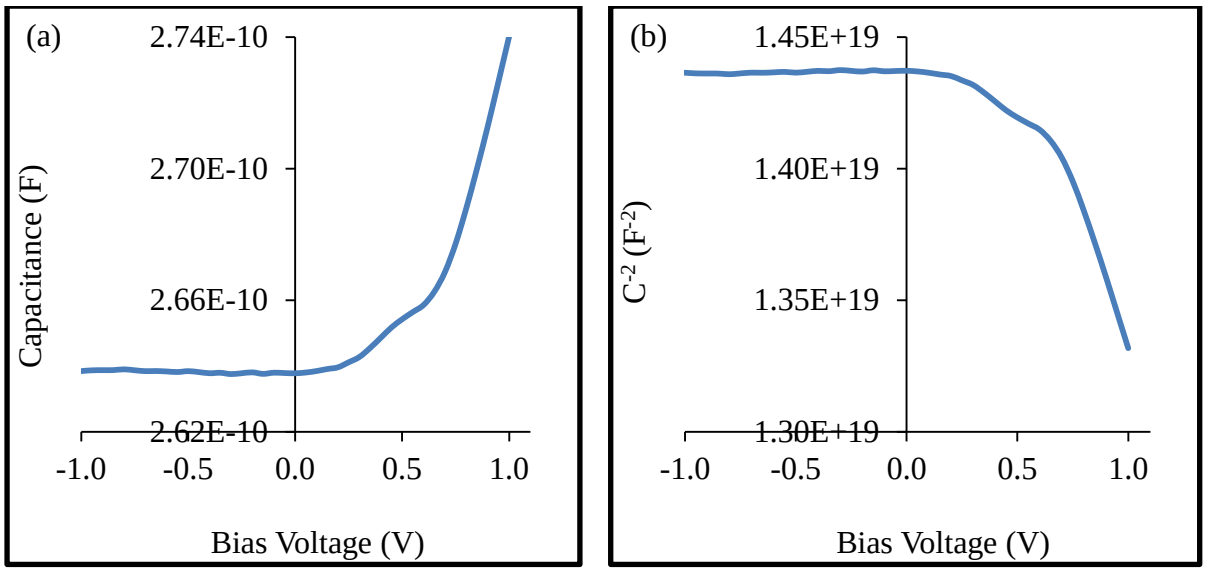

Fig. 5. (a) Capacitance-voltage plot and (b) Mott-Schottky plot of n-n-n+SB device structure under dark conditions.

As the forward bias voltage increases beyond 0.2 V, increase of the depletion capacitance with applied forward bias voltage was observed. The constant depletion capacitance from the reverse bias region is an indication that the solar cell device structure is fully depleted even at bias voltage of ~0.2 V [39]. For an almost or fully depleted device structure, the width of the depletion region is almost equal to the thickness of the electroplated layer. The theoretical thickness obtained for the absorber layer in the device structure is ~1200 nm while the depletion width obtained for the n-n-n+SB using Equation (1) is ~1160 nm. The correlation between the estimated theoretical thickness and measured depletion width further attest to the fully depleted nature of the n-n-n+SB device structure.

The capacitance of the depletion region is given by,

$$C_o = \frac{\varepsilon_r \varepsilon_o A}{W} \qquad (1)$$

Where C_o is the depletion capacitance, ε_r is the relative permittivity of the material (ε_r is 11.0 for CdTe [40]), ε_o is the permittivity of vacuum, A is the diode area and W is the depletion width. For this estimation, the permittivity of CdTe, the main layer of the structure is used.

One other electronic parameter which is also important in obtaining a good solar cell with optimum performance is the doping density. For solar cells to have higher efficiency, it must

have a moderate doping. As reported by various researchers in the literature, doping density between ~10^{14} and ~10^{16} cm^{-3} have been obtained for device structures with efficiency greater than 10% [5,38,41,42]. In this work, the doping density for glass/FTO/n-ZnS/n-CdS/n-CdTe/Au has been estimated to be 5.20×10^{15} cm^{-3}. It should be noted that the straight line segment of Mott-Schottky plot is obtained after ~0.5 V forward bias and the depletion region is mainly within the CdTe layer. Therefore, the value obtained (5.20×10^{15} cm^{-3}) represents the doping concentration of n-type CdTe layers. This value falls in the range of reported values of doping density in the literature. Since the majority carriers are electrons in n-n-n+SB device structure, the obtained doping density (N_D-N_A) from the C^{-2} vs V plot (Mott-Schottky plot) is synonymous to the electron donor density in the solar cells device structure.

By substituting the estimated values of N_D-N_A into Equation (2), the position of Fermi level (Ec-E_F) for the n-CdTe used was estimated. The Ec-E_F was found to be at ~0.13 eV below the conduction band minimum.

$$\Delta E = E_C - E_F = kT \ln\left(\frac{N_C}{N_D - N_A}\right) \tag{2}$$

Where E_C is the lowest energy of the conduction band, E_F is the Fermi level, k is the Boltzmann constant (1.38×10^{-23} $m^2kgs^{-2}K^{-1}$), T is the room temperature measured in Kelvin and N_C is the effective density of states in the conduction band edge of semiconductor. The N_C was calculated to be 7.92×10^{17} cm^{-3} for CdTe thin films using Equation (3).

$$N_C = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2} \tag{3}$$

Where $m_e^* = 0.1m_o$ is the effective electron mass of n-CdTe, $m_o = 9.1 \times 10^{-31}$ kg is the rest mass of electron and $h = 6.626 \times 10^{-30}$ cm^2kgs^{-1} is the Planck's constant.

Conclusion

The fabrication of multi-junction graded bandgap solar cells have been successfully achieved by incorporating wide bandgap ZnS semiconductor as a buffer layer to CdS/CdTe-based solar cells. The summary of the electronic parameters obtained from I-V and C-V measurement techniques for glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells show that the n-n-n+SB device structure is a potential device architecture that can be further developed for high efficiency solar cell fabrication. The large bandgap in the front of the n-n-n+SB device structure has assisted in creating a steep slope to ease the transportation of electrons to the front contact and the production of strong electric field within the depletion region has helped in separating the holes and electrons to the back and front contacts respectively where they are collected for effective current generation. The overall effect of this process can be seen in the improved short-circuit current density of the n-n-n+SB device structure. Work is presently ongoing to improve the efficiency further using graded bandgap device structures based on electroplated materials.

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References

[1] J. L. Boone, T. P. Van Doren, A. K. Berry, Thin Solid Films, **87** (1982) 259–264.

[2] C. Ferekides, J. Britt, Sol. Energy Mater. Sol. Cells, **35** (1994) 255–262.

[3] T. L. Chu, S. S. Chu, C. Ferekides, C. Q. Wu, J. Britt, C. Wang, J. Appl. Phys., **70** (1991) 7608.

[4] S. K. Das, G. C. Morris, Sol. Energy Mater. Sol. Cells, **28** (1993) 305–316.

[5] J. Britt, C. Ferekides, Appl. Phys. Lett., **62** (1993) 2851–2852.

[6] M. Tsuji, T. Aramoto, H. Ohyama, T. Hibino, K. Omura, J. Cryst. Growth, **214** (2000) 1142–1147.

[7] X. Wu, Sol. Energy, **77** (2004) 803–814.

[8] A. Bosio, N. Romeo, S. Mazzamuto, V. Canevari, Prog. Cryst. Growth Charact. Mater., **52** (2006) 247–279.

[9] H. R. Moutinho, J. Vac. Sci. Technol. A Vacuum, Surfaces, Film., **13** (1995) 2877–

2883.

[10] M. P. R. Panicker, M. Knaster, F. A. Kroger, J. Electrochem. Soc., **125** (1978) 566.

[11] C. Sella, P. Boncorps, J. Vedel, J. Electrochem. Soc., **133** (1986) 2043–2047.

[12] N. B. Chaure, A. P. Samantilleke, I. M. Dharmadasa, Sol. Energy Mater. Sol. Cells, **77** (2003) 303–317.

[13] S. Bonilla, E. A. Dalchiele, Thin Solid Films, **204** (1991) 397–403.

[14] I. S. Yahia, F. Yakuphanoglu, S. Chusnutdinow, T. Wojtowicz, G. Karczewski, Curr. Appl. Phys., **13** (2013) 537–543.

[15] R. Martin, MIT Technol. Rev. First Solar's Cells Break Effic. Rec., (2016). https://www.technologyreview.com/s/600922/first-solars-cells-break-efficiency-record/ (accessed June 28, 2016).

[16] C. S. Ferekides, R. Mamazza, U. Balasubramanian, D. L. Morel, Thin Solid Films, **480**–**481** (2005) 224–229.

[17] C. S. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D. L. Morel, Sol. Energy, **77** (2004) 823–830.

[18] J. D. Major, K. Durose, 2013 IEEE 39th Photovolt. Spec. Conf., (2013) 1146–1149.

[19] A. D. Compaan, A. Gupta, S. Lee, S. Wang, J. Drayton, Sol. Energy, **77** (2004) 815–822.

[20] J. A. M. AbuShama, S. Johnston, T. Moriarty, G. Teeter, K. Ramanathan, R. Noufi, Prog. Photovoltaics Res. Appl., **12** (2004) 39–45.

[21] A. Rios-Flores, O. Ares, J. M. Camacho, V. Rejon, J. L. Pena, Sol. Energy, **86** (2012) 780–785.

[22] O. K. Echendu, I. M. Dharmadasa, Energies, **8** (2015) 4416–4435.

[23] I. O. Oladeji, L. Chow, C. S. Ferekides, V. Viswanathan, Z. Zhao, Sol. Energy Mater. Sol. Cells, **61** (2000) 203–211.

[24] I. M. Dharmadasa, A. P. Samantilleke, N. B. Chaure, J. Young, Semicond. Sci. Technol., **17** (2002) 1238–1248. http://iopscience.iop.org/0268-1242/17/12/306.

[25] O. I. Olusola, M. L. Madugu, I. M. Dharmadasa, Improvement of CdS/CdTe Solar Cell Parameters using ZnS Buffer Layer, in: Proc. of PVSAT-12, Liverpool (2016): pp. 107–110. http://www.pvsat.org.uk/proceedings/.

[26] M. L. Madugu, O. I. Olusola, O. K. Echendu, B. Kadem, I. M. Dharmadasa, J. Electron. Mater., **45** (2016) 2710–2717.

[27] N. A. Abdul-Manaf, A. R. Weerasinghe, O. K. Echendu, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., **26** (2015) 2418–2429.

[28] F. Bin Fauzi, PhD Thesis "Research and Development of CdS/CdTe Solar Cells Incorporating ZnTe Layers," Sheffield Hallam University, Sheffield, 2015.

[29] I. M. Dharmadasa, Prog. Cryst. Growth Charact. Mater., **36** (1998) 249–290.

[30] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[31] T. L. Chu, S. S. Chu, Solid State Electron., **38** (1995) 533–549.

[32] M. D. G. Potter, D. P. Halliday, M. Cousins, K. Durose, Thin Solid Films, **361**–**362** (2000) 248–252.

[33] I. M. Dharmadasa, O. Elsherif, G. J. Tolan, J. Phys. Conf. Ser., **286** (2011) 12041.

[34] W. G. Oldham, A. G. Milnes, Solid. State. Electron., **7** (1964) 153–165.

[35] E. H. Rhoderick, IEE Proc. I Solid State Electron Devices, **129** (1982) 1–14.

[36] A. Morales-Acevedo, Sol. Energy Mater. Sol. Cells, **90** (2006) 2213–2220.

[37] B. M. Basol, J. Appl. Phys., **55** (1984) 601–603.

[38] I. M. Dharmadasa, P. A. Bingham, O. K. Echendu, H. I. Salim, T. Druffel, R. Dharmadasa, G. U. Sumanasekera, R. R. Dharmasena, M. B. Dergacheva, K. A. Mit, K. A. Urazov, L. Bowen, M. Walls, A. Abbas, Coatings, **4** (2014) 380–415.

[39] O. K. Echendu, PhD Thesis "Thin film solar cells using all-electrodeposited ZnS, CdS and CdTe materials," Sheffield Hallam University, Sheffield, 2014.

[40] J. R. Pugh, D. Mao, J. G. Zhang, M. J. Heben, A. J. Nelson, A. J. Frank, J. Appl. Phys., **74** (1993) 2619–2625.

[41] J. M. Woodcock, A. K. Turner, M. E. Ozsan, J. G. Summers, Thin film solar cells based on electrodeposited CdTe, in: Conf. Rec. Twenty Second IEEE Photovolt. Spec. Conf., Las Vegas, NV, USA (1991): pp. 842–847.

[42] I. M. Dharmadasa, Coatings, **4** (2014) 282–307.