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PROGRESS IN DEVELOPMENT OF GRADED BANDGAP THIN FILM SOLAR CELLS WITH ELECTROPLATED MATERIALS

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ABSTRACT

Photovoltaic devices are developed mainly based on p-n or p-i-n type device structures, and these devices can utilise only a fraction of the solar spectrum. In order to further improve device parameters and move towards low-cost and high-efficiency next generation solar cells, device architectures capable of harvesting all photons available should be designed and developed. One such architecture is the fully graded bandgap device structure as proposed recently based on both n-type and p-type window layers. These designs have been experimentally tested using well researched GaAs/AlGaAs system producing impressive device parameters of open circuit voltage (V_{oc}) ~1175 mV and fill factor (FF) ~0.85. The devices have also been experimentally tested for the evidence of impurity photovoltaic (PV) effect and impact ionisation taking place within the same device. Since these structures have been experimentally proved with a well-established semiconductor, the effort has been focussed on developing these devices using low-cost and scalable electroplated semiconductors, in order to minimise manufacturing cost. This paper reviews and summarises the work carried out during the past decade on this subject. Graded bandgap devices produced using only two or three electroplated semiconductor layers have been explored and their conversion efficiencies have gradually increased from 10.0%, through 12.8% to 15.3% for different structures. While the work is progressing along this line, the paper summarises the achievements to date.

Keyword: Semiconductors, Graded bandgap, CdS/CdTe, Device configuration, Solar cells.

1 INTRODUCTION

The competitiveness of solar cells lies within its conversion efficiency while its economic viability is determined by its production cost. Semiconductor (SC) deposition techniques such as electrodeposition matches the economic requirements provided efficient solar cells can be fabricated using the technique. Improvements of CdS/CdTe solar cells after about two decades of stagnation has been achieved through better understanding of materials and device issues. In a view of increasing efficiency and/or economic viability, several concepts and innovative technologies proposed include intermediate band solar cell [1], quantum dots and quantum wells solar cell [2], down and up conversion solar cell [3], plasmonic solar cell [4], hot-carrier solar cell [5], tandem solar cell with tunnel junctions [6], dye-sensitised and Perovskite solar cells [7] and graded bandgap solar cell [8-9]. Amongst the proposed concepts only tandem solar cells and graded bandgap solar cells have experimentally shown reasonable efficiency with required stability and the potential of increasing performance. The main difference between these two approaches is that the tandem solar cells efficiency increase is mostly due to increase in open-circuit voltage, V_{oc} while in the graded bandgap solar cells the efficiency is mainly increased due to increase in the short-circuit current density, J_{sc}. The main disadvantage of the tandem solar cell is the series connection of cells resulting into the reduction in charge carrier mobility and increase in the recombination potential of e-h pairs generated within the cell while the graded bandgap solar cell's disadvantage is the technicality of growth required. With major emphasis on graded bandgap architectures, the mechanism as proposed by Dharmadasa et al [8, 10] can be facilitated by incorporating either an n-type or p-type wide bandgap front-layer with a gradual reduction in bandgap towards p-type or n-type back layer respectively. The latter is more advantageous due to higher potential barrier height (ϕ_b) achievable for electron transport is larger than that of a device made on an n-type window layer material [11] as shown in Figure 1.

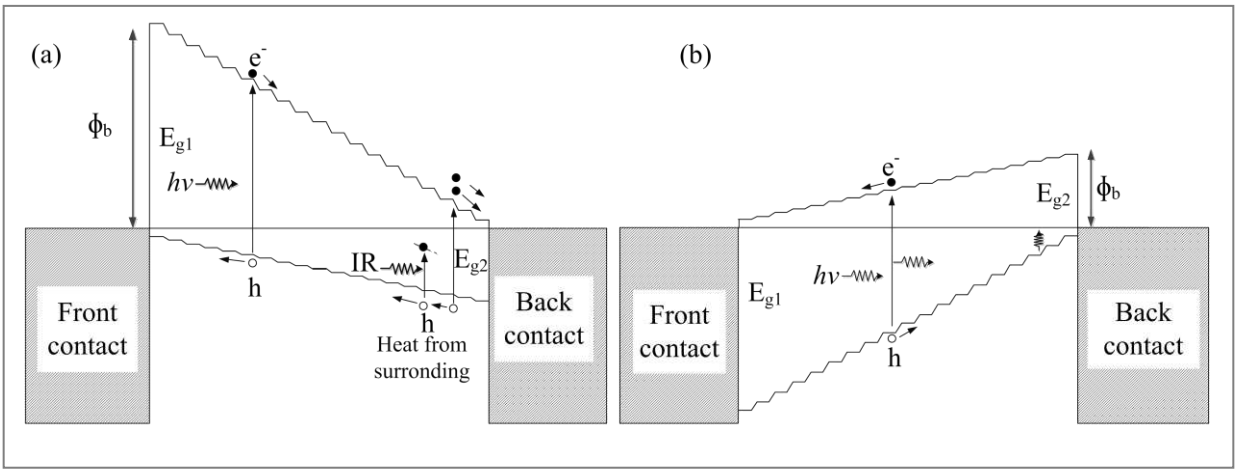

Figure 1: Schematic representation of graded bandgap solar cells based on (a) p-type window layer and (b) n-type window layer.

2 THE CONCEPT AND EXPERIMENTAL VALIDATION

The concept validation was achieved using well-established Metal-Organic Vapour Phase Epitaxy (MOVPE) technique in the deposition of well-researched GaAs/AlGaAs in which 12% efficiency (η) was achieved in the first run and 20% was achieved in just the second run based on improved material engineering [11]. To facilitate the device shown in Figure 1 (a), the bandgap grading was achieved by a gradual increment of Al atomic percentage to increase the bandgap of GaAs from 1.42 eV to 2.20 eV. Furthermore, the GaAs back-layer was doped n-type with Si. The Si atomic concentration was gradually reduced towards the middle of the structure, in a 3 µm thick alloy layer. Also, C concentration was increased towards the front of the device to gradually increase its p-type doping. This way, the doping profiles were changed, to vary the doping of semiconductors from n- to p- from the rear to the front of the device [10-11]. It was reported that the middle of the device shows material intrinsic properties. The hallmarks of the experimental results were the highest reported open circuit voltage (V_{oc}) of 1175 mV and FF of ~0.85 under AM1.5 illumination condition for a single cell and the PV activity of the cell in complete darkness achieving V_{oc} >700 mV due to impurity PV effect under dark condition [12]. Furthermore, the presence of impact ionisation

was validated by the Incident Photon to Charge Carrier Efficiency (IPCE) measurement of 140% [11]. This result shows that a single photon can create more than one e-h pairs. These results confirm the presence of both impurity PV effect and impact ionisation functioning within one device making use of native defects. These results also justify the achievability of higher short-circuit current density J_{sc} above the Shockley–Queisser limit of a single p–n junction [13] for devices fabricated using multilayer graded bandgap configuration coupled with high V_{oc} (1175 mV) and the highest possible FF (0.85) values experimentally observed.

3 MULTILAYER GRADED BANDGAP DEVICE STRUCTURE UTILISING ELECTRODEPOSITION TECHNIQUE

Electrodeposition technique is a process of coating or deposition of metal(s) or semiconductors compounds on electrically conducting substrate. Electrodeposition of semiconductors which was first introduced by Panicker et al [14] can be achieved using either a 3-electrode (3E) or 2- electrode (2E) configuration, suitable electrolyte containing the required precursors, power supply, stirrer and hot plate. It should be noted that the main difference in setup between the 3E and 2E electrodeposition configuration is the incorporation of a reference electrode in the 3E configuration in addition to the counter electrode (CE) and working electrode (WE) as utilised in the 2E configuration. The effect of electroplating configuration on the electrodeposited semiconductor layer properties have been published by the author's group elsewhere [15]. With major advantages such as low setup cost, possibility of depositing n-, i-, and p- type semiconductor from the same electroplating setup by deposition voltage variation, self-purification, bandgap engineering, proven scalability and manufacturability [16], [17], electrodeposition is suitable for the growth of multilayer graded bandgap device structure.

3.1 STAGE 1 – PRELIMINARY WORK ON GLASS/FTO/n-ZnS/n-CdS/n-CdTe/Au

After experimentally testing the new concept of graded bandgap devices, work has begun to produce these devices using low-cost and scalable electroplated materials. For this purpose, over 14 different semiconductor layers have been established using electrodeposition technique within the authors' group [18]–[28]. The main challenge was the incorporation of different layers into glass/FTO/WL/AL/MC, glass/FTO/BL/WL/AL/MC, glass/FTO/BL/WL/AL/PPL/MC in n-n+SB, n-p, n-n-n, n-n-p, n-n-n-p configurations, where FTO is fluorine-doped tin oxide, BL is the buffer layer, WL is the window layer, AL is the absorber layer, PPL is the pinhole plugin layer, MC is the metal contact and SB is the Schottky barrier. Echendu et al [29] demonstrated the possibility of achieving high efficiency graded bandgap solar cell using all-electrodeposited glass/FTO/n-ZnS/n-CdS/n-CdTe/Au in which the n-ZnS layer is the BL, n-CdS is the WL and n-CdTe is the AL. This device structure follows the second type of graded bandgap devices as shown in Figure 1 (b) and its real situation is shown in Figure 4.

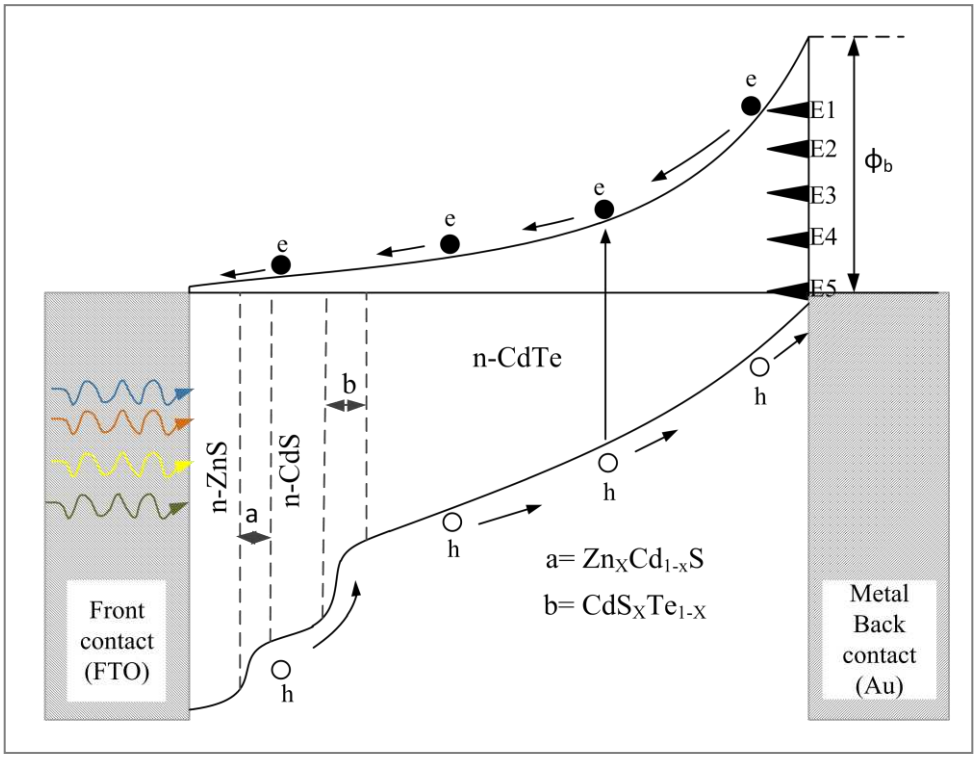

Figure 2: Typical band diagram of the glass/FTO/n-ZnS/n-CdS/n-CdTe /Au thin film solar cell.

The use of Au on n-type CdTe back-layer is to create a large Schottky barrier (SB) at the metal/semiconductor (M/SC) interface. It should be noted that the inclusion of the Schottky barrier structures near the back contact is capable of producing potential barrier heights of (~1.20 eV) greater than or comparable to barrier heights in p-n junction devices based on CdTe [29]. It has been experimentally shown that there are five possible Fermi level pinning positions on n-CdTe/metal interfaces [30] producing different potential barriers. In fact, this does affect the reproducibility of the devices.

The precursors present in the aqueous electrolytic bath in which ZnS was deposited were 0.3 M $ZnCl_2$ and 0.03 M $(NH_4)_2S_2O_3$ [31], the precursors for the CdS layer were 0.3 M $CdCl_2$ and 0.03 M $Na_2S_2O_3$ [32] while CdTe layer was grown from aqueous electrolytic bath containing 1 M $CdSO_4$ and 1 mM TeO_2 [29]. The thicknesses of the electrodeposited layers are g/FTO/n-ZnS (300 nm)/n-CdS (600 nm)/n-CdTe (1700 nm)/Au as calculated using Faraday's equation as shown in eq. (1). The electronic parameters measured for completed devices are tabulated in Table 1.

$$T = \frac{JtM}{nFd} \tag{1}$$

It should be noted that in between subsequently deposited layers, the materials were rinsed, dried in a stream of nitrogen and treated both chemically and thermally to improve the electronic properties of the deposited layers [33]. The glass/FTO/n-ZnS layers were heat treated between (300 and 350) °C for (10 to 15) minutes while both the glass/FTO/n-ZnS/n-CdS and the glass/FTO/n-ZnS/n-CdS/n-CdTe layers were treated between (400 and 450) °C in air for (15 to 20) minutes in the presence of $CdCl_2$ after deposition. After the completion of growth and treatment, the layers were acidically etched using solution containing potassium dichromate ($K_2Cr_2O_7$) and concentrated sulphuric acid (H_2SO_4) and alkalinically etched using solution containing sodium hydroxide (NaOH) and sodium thiosulfate ($Na_2S_2O_3$) for the duration of 2 seconds and 2 minutes respectively to make the CdTe surface Cd-rich and

improve the metal/semiconductor contact [30, 34]. To avoid the back-layer oxidation, immediately after etching, 100 nm Au contacts were evaporated in a high vacuum system with the aid of a 2 mm diameter metal mask. The treatment and etching processes were unique for all the devices fabricated and discussed in this review. Using the same precursors for ZnS and CdTe, Echendu et al [35] fabricated a glass/FTO/n-ZnS/n-CdTe layer with the major consideration of reducing the thickness of ZnS from 300 to 200 nm, while the CdTe thickness remained at 1700 nm. Due to inter-diffusion, the formation of an intermediate material such as $ZnCdS_xTe_{1-x}$ is generated during heat treatment resulting in a graded-bandgap configuration [35]. At AM1.5 illuminated condition, the champion cell conversion efficiency of 10.4% was observed with the measured value of J_{sc} higher than the Shockley–Queisser limit of a single p–n junction [13]. This is due to the multi-layer and multi-junction n–n–n+ SB device configurations theoretically proposed [10, 36] and experimentally tested [8, 11] in the literature, although, FF was low and a comparatively low V_{oc} were observed. The low V_{oc} values as reported in this work indicate the presence of leakage paths which might also be due to low-purity precursors utilised in the deposition of the semiconductor layers. The main challenge for the reported work was the low fill factor (FF) values. Under the dark condition, the series resistance (R_s) was high and the shunt resistance (R_{sh}) was low. The observed doping density (N_D) of 8.1×10^{14} cm^{-3} falls within the doping concentration of reported high-efficiency solar cells (~1.0×10^{14} – 5×10^{15} cm^{-3}) [37-38].

Table 1: Graded bandgap device parameters reported under both AM1.5 illuminated condition and dark conditions.

DEVICE CONFIGURATION	PARAMETERS UNDER AM1.5 ILLUMINATED CONDITION				PARAMETERS UNDER DARK CONDITION			Ref.
	η (%)	J_{sc} ($mAcm^{-2}$)	V_{oc} (mV)	FF	R_s (Ω)	R_{sh} (Ω)	N_D (cm^{-3})	
n-ZnS/n-CdS/n-CdTe/Au	10.4	40.8	640	0.40	175	4.6×10^{3}	8.1×10^{14}	[29]
n-ZnS/$ZnCdS_xTe_{1-x}$/n-CdTe/Au	12.0	47.8	646	0.39	---	---	---	[35]
n-ZnS/n-CdS/n-CdTe/Au	12.8	41.5	670	0.46	1351	8.1×10^{6}	5.2×10^{15}	[39]
n-In_xSe_y/n-CdS/n-CdTe/Au	10.0	38.1	640	0.41	309	4.5×10^{3}	2.0×10^{14}	[50]
n-CdS/n-CdTe/p-CdTe/Au	15.3	33.8	730	0.62	500	7.2×10^{6}	6.6×10^{14}	[49]

3.2 STAGE 2 – OPTIMISATION OF MATERIALS AND DEVICE STRUCTURES

3.2.1 PRECURSOR REPLACEMENT AND THICKNESS OPTIMISATION

Further improvement in material properties in both ZnS and CdS due to changes in deposition precursors as documented by Madugu et al [19] and Abdul-Manaf et al [24] respectively led to the enhancement in the n-ZnS/n-CdS/n-CdTe/Au type solar cell's efficiency as reported by Olusola [39]. The ZnS precursors were replaced with 0.15 M $ZnSO_4$ and 0.15 M $(NH_4)_2S_2O_3$ [19]. The culmination of the concentration and precursor utilised by Madugu et al [19] is the growth of both n- and p- type ZnS from the same aqueous electrolytic bath by intrinsic doping. While the CdS precursors as documented by Echendu et al [29] were replaced with 0.3 M $CdCl_2$ and 0.03 M $(NH_4)_2S_2O_3$ [24]. The replacement of the $Na_2S_2O_3$ with $(NH_4)_2S_2O_3$ was due to the possibility of absorption, adsorption and accumulation of Na in the electrolyte on the grown CdS layer. It is well known that CdS is intrinsically an n-type material due to defects such as Cd interstitials and S vacancies in the crystal lattice [40] while Na is a p-type dopant in CdS. Therefore, the introduction of p-dopant into an n-type layer will increase the resistivity of the deposited layer due to compensation which might have a negative impact on the fabricated PV devices. The CdTe layer was deposited from a similar aqueous electrolyte by Echendu et al containing 1 M $CdSO_4$ and 1 mM TeO_2 [29]. The thicknesses of all the layers incorporated by Olusola [39] were optimised and reduced to 100 nm for the n-ZnS layer and 150 nm for the n-CdS layer to decrease the effect of parasitic absorption [41] on the fabricated solar cell devices. The CdTe layer thickness was also reduced to 1200 nm. As observed in Table 1, a champion conversion efficiency of 12.8% was observed at AM1.5 with improvement in the J_{sc} which might be due to high transmittance of both the BL and WL due to the reduction in thicknesses. A comparative improvement in both the V_{oc} and FF were also observed which might be attributed to improvement in material quality. The increase in

V_{oc} signifies a comparative reduction in the shunt while the improvement in the FF can be attributed to the increase in the R_{sh} although the R_s observed were still high.

3.2.2 BUFFER LAYER ALTERATION (In_xSe_y)

Although CdS proves the best heterojunction partner to CdTe due to the comparatively low lattice mismatch of 10% [42] In_xSe_y was incorporated into the glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au due to its excellent wetting property on FTO surface [20]. The In_xSe_y was deposited from an aqueous electrolytic bath containing 0.10 M $InCl_3$ and 0.025 M SeO_2 [20]. At a low In_xSe_y thickness of ~80 nm incorporated in the device structure, a bandgap of 2.89 eV was achieved through bandgap engineering which is one of the advantages of electrodeposition technique. This could be accomplished through the deposition voltage variation to increase the concentration of one of the constituents [43-44] and/or through thickness optimisation [45], [46] which is not limited to electrodeposition.

The CdS and CdTe thicknesses utilised in this work were 150 nm and 2500 nm respectively. The CdS layers were deposited from an aqueous electrolyte containing 0.075 M $CdCl_2$ and 0.15 M $(NH_4)_2S_2O_3$ [24] while the CdTe layers were deposited from 1 M $CdSO_4$ and 1 mM TeO_2 [29] aqueous electrolyte. The glass/FTO/n-In_xSe_y was treated at 300°C for 10 minutes in air while the subsequent glass/FTO/n-In_xSe_y/n-CdS and glass/FTO/n-In_xSe_y/n-CdS/n-CdTe layers were treated between (400 and 450)°C in air for (15 to 20) minutes in the presence of $CdCl_2$ after deposition. The highest efficiency observed was 10.0% at AM1.5, with a fill factor of 0.41, V_{oc} of 640 mV and J_{sc} of 38.1 $mAcm^{-2}$. Although the doping density of the absorber material falls within the high-efficiency solar cell range of (~1.0×10^{14} – 5×10^{15} cm^{-3}) [37-38], the low R_{sh} which suggest high leakage current was observed in dark condition as shown in Table 1. From observation, an alteration in buffer layer from ZnS to In_xSe_y do not show any significant improvement in the electronic parameters of the fabricated cell. The

highpoint in this work is the possibility of bandgap engineering of In_xSe_y and its incorporation in a glass/FTO/n-In_xSe_y/n-CdS/n-CdTe/Au device structure.

3.2.3 MULTILAYER CONFIGURATION

The glass/FTO/n-CdS/n-CdTe/p-CdTe/Au was initialised to reduce deposition and treatment complexity by eliminating the use of buffer layer and optimising the window layer. In addition, there is a possibility of Na leaching from the glass layer into the semiconductor layer when subjected to subsequent heating of the glass/FTO. Provided the semiconductor layer are p-type, the leaching of Na which is a p-type dopant to both CdS and CdTe is advantageous but it might result into high resistivity of the layer due to compensation if the semiconductor layers are n-type. In this work, the optimisation of CdS layer as presented by Ojo et al [47] took into consideration the electroplating mechanism, effect of CdS thickness and parasitic absorption. Based on these findings, 120 nm thick CdS layer was utilised using 0.3 M $CdCl_2$ and 0.03 M $(NH_4)_2S_2O_3$ [24] while the CdTe layer was electrodeposited from an aqueous electrolyte containing 1 M $Cd(NO_3)_2$ and ~1 mM TeO_2 [28]. The 1200 nm n-CdTe and 30 nm p-CdTe were grown in a continuous deposition process in the same aqueous electrolytic bath by changing only the deposition voltage [28]. The ability to grow both n-type and p-type semiconductor layers in the same bath through intrinsic doping earmarks the advantages of electrodeposition [48].

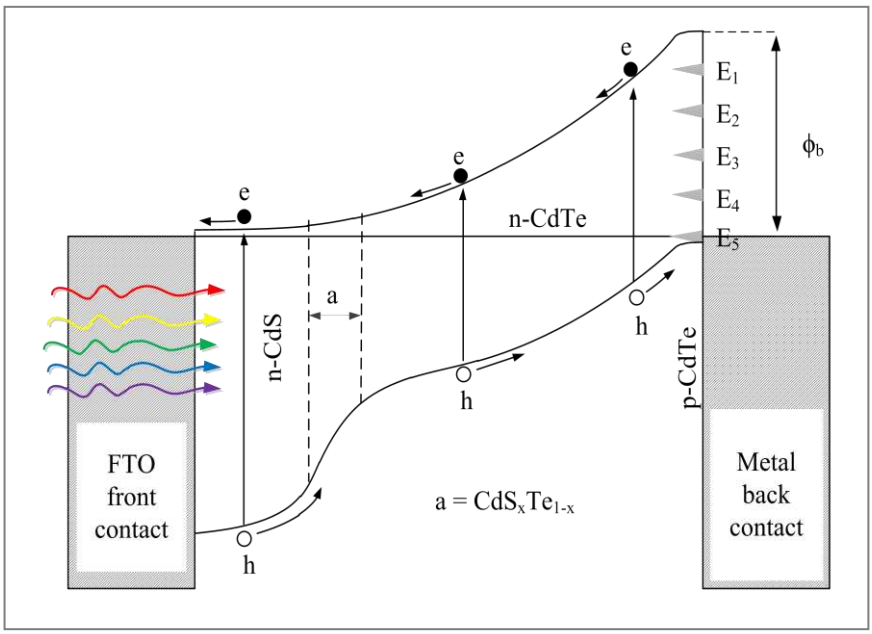

Figure 3: Typical band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe /Au thin film solar cell.

The incorporation of the thin p-CdTe layer was necessitated to set the Fermi level (FL) close to the valence band to achieve high barrier height of ~1.20 eV. This p-CdTe layer was also introduced to remove reproducibility issues due to Fermi level pinning possibilities at one of the five different energy levels [30]. The thickness of the p-CdTe layer has also been optimised to achieve high-performance devices.

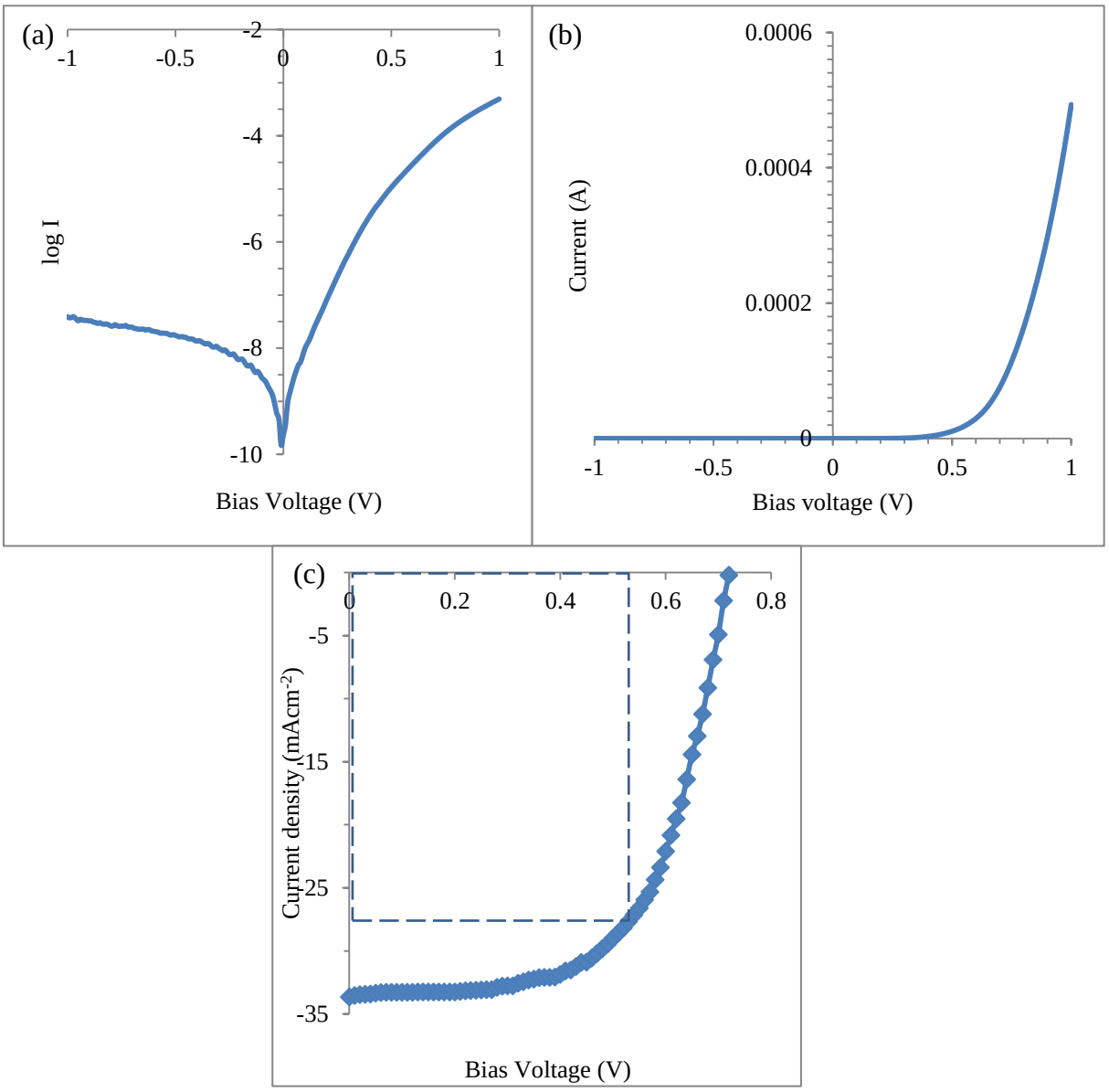

Figure 4: Typical (a) log-linear and (b) linear-linear current–voltage curves of g/FTO/n-CdS/n-CdTe/p-CdTe/Au under dark conditions, while (c) is the I-V curve under A.M1.5 illuminated conditions.

From the fabricated glass/FTO/n-CdS/n-CdTe/p-CdTe/Au structures, champion cell conversion efficiency of 15.3% under AM1.5 illumination was observed. The I-V curves of the devices are shown in Figure 4 and summarised in Table 1. Furthermore, an improved V_{oc} of 730 mV and FF of 0.62 were reported which might be due to improved material processing step as documented by Ojo et al [49]. The yield recorded in this set of experiment was 100% but the variation in device parameters and consistency still requires improvement. The

observed R_s of 500 Ω measured for the champion cells are high and reduction of this should further improve the FF and the J_{sc}. In a view of increasing conversion efficiency and reducing the R_s copper-gold contacts were evaporated on a direct replica of the glass/FTO/n-CdS/n-CdTe/p-CdTe to achieve glass/FTO/n-CdS/n-CdTe/p-CdTe/Cu-Au devices. A champion efficiency of 18.5% was observed under AM1.5 conditions. But due to instability and reproducibility issues, the results have not been published yet until the electronic parameters of the fabricated cells can be stabilised and further experimentation performed.

4 CONCLUSION

The utilisation of electrodeposition technique under both 3-electrode and 2-electrode configuration show promises in the fabrication of high-efficiency solar cell using graded bandgap multilayer device configuration. This review iterates the gradual development in attaining high efficiency using graded bandgap configuration. As expected, these preliminary studies on n-n-n plus large Schottky barrier and n-n-p structures produced PV active devices showing best efficiencies of 12.8% and 15.3% respectively. It is evident that improvement in device properties such as R_s, R_{sh}, FF, and V_{oc} is required. Furthermore, work on the incorporation of the p-type window layer as shown in Figure 1 (a) are continuing as proposed by Dharmadasa et al [10] to achieve even more efficient devices. This structure is more capable of producing high V_{oc} values as demonstrated by GaAs/AlGAs systems.

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