Optoelectronic Devices Based on Graded Bandgap Structures Utilising Electroplated Semiconductors

Olajide Ibukun-Olu Olusola

A thesis submitted in partial fulfilment of the requirements of
Sheffield Hallam University for the degree of
Doctor of Philosophy

August 2016

Declaration

I hereby declare that the work described in this thesis is my own work, done by me and has not been submitted for any other degree anywhere.

_____

OLAJIDE IBUKUN-OLU OLUSOLA

Acknowledgement

To God be the glory, honour and adoration for the great things He has done. My sincere appreciation goes to the immediate past Vice-Chancellor of my home university (the Federal University of Technology, Akure (FUTA)), Professor Adebisi M Balogun for nominating me for the Commonwealth Scholarship award. I also want to appreciate the present Vice-Chancellor of FUTA, Professor A.G. Daramola for approving my study leave to pursue this programme. My gratitude also goes to the immediate past Dean of School of Science, FUTA, Professor I.A. Fuwape for recommending me for this award at the faculty level and also for her motherly roles. Dr. S.S. Oluyamo is greatly appreciated for his mentorship, help and for connecting me with my Director of Studies. Professor B. Adeyemi and Professor A. Adebayo are also thanked for their trust to be my guarantor for this award. I appreciate the contributions made by Professor M.T. Babalola, Professor O.S. Ajayi, Professor M.O. Ajewole, Professor A.M. Arogunjo and Dr. K.D. Adedayo towards the success of my academic career. All the staff, the present and the past Heads of Physics Department are acknowledged and appreciated. I am also grateful to the FUTA Director of Academic Planning, Mrs A.O. Adebayo for her motherly role and advice while processing the award. I sincerely appreciate the Commonwealth Scholarship Commission, UK and Sheffield Hallam University for funding this research programme.

My immense gratitude goes to my supervisor and Director of Studies, Professor I.M. Dharmadasa for the excellent training and professional mentorship that he gave me during this research programme. Being a research student under him has really exposed me to the fundamentals of electronics material and device physics. I appreciate the contributions of my second supervisor, Dr. Faris Al-Naemi towards the completion of my PhD programme.

I sincerely appreciate the useful advice and technical discussions of my colleagues (Dr. A.R. Weerasinghe, Dr. O.K. Echendu, Dr. F. Fauzi, Dr. N.A. Abdul-manaf, Dr. H.I. Salim, M.L. Madugu, and A.A. Ojo) in the Electrodeposition arm of Solar Energy Research Laboratory, Sheffield Hallam University. My dear friend, Abubakar Mohammed is greatly appreciated for the technical support he gave in the use of referencing software and MS-Word applications. Thanks to Burak Kadem and Yaqub

Rahaq for useful academic discussions during this research programme. I appreciate the friendship of A. Ogunsanwo, B. Ayomanor, O. Oluwafemi and O. Ojedokun.

Research collaborators from different research institutes such as Professor T. Druffel, Dr. R. Dharmadasa and their group members from Conn Centre, University of Louisville, USA are acknowledged for performing PL and UPS experiments. Professor M. Dergacheva from Institute of Organic Catalyst & Electrochemistry, Kazakhstan is also thanked for assisting in carrying out AFM measurements. Special thanks to MERI staff; to mention but a few, Professor Doug Cleaver, Professor Nabok Alexei, Professor Chris Sammon, Dr. Paul Bingham, Dr. Aseel Hassan, Dr. Nicholas Farmilo, Gary Robinson, Corrie Houton, Deeba Zahoor, Stuart Creasy, Rachael Toogood, Deborah Durmus, Gillian Hill, Gail Hallewell, Paul Allender, Bob Burton, Dr Tony for their technical and administrative helps during my research programme.

The Pastorate of Mountain of Fire and Miracles Ministries (MFM) Sheffield branch, Pastor and Pastor (Mrs) A. Macgregor, Pastor and Pastor (Mrs) T. Aisida, Pastor and Pastor (Mrs) A. Adewale are greatly thanked for both spiritual and physical support during my sojourn in Sheffield city, UK. I cannot but appreciate the support received from the Prayer and Youth Department of MFM Sheffield headed by Brother Gbenga Odele and Brother Muyiwa Babatunde respectively.

I acknowledge and appreciate the sacrifice of my aged parents, Elder Joshua Olusola Ojo-Eleka and Deaconess Eunice Ademolabi Olusola Ojo-Eleka to give us a befitting education right from our infant days to this present moment. May the good Lord grant you more strength in your old age and may you live long to enjoy the fruits of your labour in Jesus name. I greatly acknowledge the financial support received from my elder brother, Pastor (Dr) K.O. Olusola right from my teenager to this present time. Special thanks also go to all my family members, Mr and Mrs Johnson Oladeji, Pastor (Dr) and Deaconess Kolapo Olusola, Dr (Mrs) and Pastor Abioye Ayorinde, Pastor (Dr) and Dr (Mrs) Joshua Aransiola, Pastor and Mrs Femi Olusola, Mr and Mrs Wole Olusola, Mr and Mrs Seun Olusola and my in-laws. God bless you all.

Mr and Mrs Segun Olusola are also acknowledged for their supports. To my beloved wife, Olanike J. Olusola, I appreciate her support and encouragement throughout my stay in United Kingdom and during the PhD thesis writing stage. God bless you richly in Jesus name. Finally, I thank everyone who has assisted me in one way or the other and contributed positively to my success in life. Thanks and may God bless you all.

Dedication

This research work is dedicated to the Almighty God, the Father of our Lord Jesus Christ for His salvation, protection, guidance and for seeing me through in my research work.

List of Publications

Journal Publications

1. **O.I. Olusola**, O.K. Echendu, I.M. Dharmadasa, Development of CdSe thin films for application in electronic devices, J. Mater. Sci. Mater. Electron. 26 (2015) 1066–1076. doi:10.1007/s10854-014-2506-x.
2. N.A. Abdul-manaf , H.I. Salim, M.L. Madugu, **O.I. Olusola**, I.M. Dharmadasa, Electro-Plating and Characterisation of CdTe Thin Films Using CdCl2 as the Cadmium Source, Energies. 8 (2015) 10883–10903. doi:10.3390/en81010883.
3. **O.I. Olusola**, M.L. Madugu, I.M. Dharmadasa, Growth of n- and p-type ZnTe semiconductors by intrinsic doping, Mater. Res. Innov. 19 (2015) 497–502. doi:10.1080/14328917.2015.1105570.
4. **O.I. Olusola**, M.L. Madugu, N.A. Abdul-Manaf, I.M. Dharmadasa, Growth and characterisation of n- and p-type ZnTe thin films for applications in electronic devices, Curr. Appl. Phys. 16 (2016) 120–130. doi:10.1016/j.cap.2015.11.008.
5. M.L. Madugu, **O.I. Olusola**, O.K. Echendu, B. Kadem, I.M. Dharmadasa, Intrinsic Doping in Electrodeposited ZnS Thin Films for Application in Large-Area Optoelectronic Devices, J. Electron. Mater. (2016). doi:10.1007/s11664-015-4310-7.
6. H.I. Salim, **O.I. Olusola**, A.A. Ojo, K.A. Urasov, M.B. Dergacheva, I.M. Dharmadasa, Electrodeposition and characterisation of CdS thin films using thiourea precursor for application in solar cells, J. Mater. Sci. Mater. Electron. (2016). doi:10.1007/s10854-016-4629-8.
7. D.G. Diso, F. Fauzi, O.K. Echendu, **O.I. Olusola**, I.M. Dharmadasa, Optimisation of CdTe electrodeposition voltage for development of CdS/CdTe solar cells, J. Mater. Sci. Mater. Electron. (2016). doi:10.1007/s10854-016-4844-3.
8. **O.I. Olusola**, H.I. Salim, I.M. Dharmadasa, One-sided rectifying p-n junction diodes fabricated from n-CdS and p-ZnTe:Te semiconductors, Mater. Res. Express. 3 (2016) 95904. doi:doi:10.1088/2053-1591/3/9/095904.
9. I.M. Dharmadasa, O.K. Echendu, F. Fauzi, N.A. Abdul-Manaf, **O.I. Olusola**, H.I. Salim, M.L. Madugu, A.A. Ojo, Improvement of composition of CdTe thin

films during heat treatment in the presence of $CdCl_2$, J. Mater. Sci. Mater. Electron. (2016). doi:10.1007/s10854-016-5802-9.

10. A.A. Ojo, H.I. Salim, **O.I. Olusola**, M.L. Madugu, I.M. Dharmadasa, Effect of thickness: a case study of electrodeposited CdS in CdS/CdTe based photovoltaic devices, J. Mater. Sci. Mater. Electron. (2016). doi:10.1007/s10854-016-5916-0.

Conference Proceedings

1. **O.I. Olusola**, P.A. Bingham, S. Creasey and I.M. Dharmadasa, Schottky Barrier Formation at Au and Electro-plated n-CdSe Interface, in: Proc. of PVSAT-10, Loughborough University, Loughborough, UK, (2014) (Poster).
2. **O.I. Olusola**, H.I. Salim, I.M. Dharmadasa, Fabrication of Rectifying p-n Junction Diodes from Heterogeneous n-CdS and p-ZnTe Semiconductors, UK Semiconductors & UK Nitrides Consortium Summer Meeting, Sheffield, United Kingdom, 9-10 July, 2014, pp. 103 (Oral Presentation).
3. **Olajide I. Olusola**, Vinay Patel and I.M. Dharmadasa, Optimisation of pH for Electrodeposition of n-CdSe Thin Films for Applications in Photovoltaic Devices, in: Proc. of 29th European Photovoltaic Solar Energy Conference and Exhibition, Amsterdam, The Netherlands, (2014) pp. 1852-1856. DOI: 10.4229/EUPVSEC20142014-3DV.2.49 (Poster).
4. M. L. Madugu, P. A. Bingham, H. I. Salim, **O. I Olusola** and I. M. Dharmadasa, Development of In_xSe_y Buffer Layers for Applications in CdTe Based Thin Film Solar Cells, in: Proc. of 29th European Photovoltaic Solar Energy Conference and Exhibition, Amsterdam, The Netherlands, (2014) pp. 1847-1851. DOI: 10.4229/EUPVSEC20142014-3DV.2.48 (Poster).
5. **O.I. Olusola**, M.L. Madugu and I.M. Dharmadasa, Growth of n- and p- type ZnTe Semiconductors by Intrinsic Doping, in: Proc. of PVSAT-11, University of Leeds, Leeds, UK, (2015) pp. 141–144 (Poster).
6. H.I. Salim, **O.I. Olusola** and I.M. Dharmadasa, Cathodic electrodeposition of CdS thin films from thiourea precursor for solar cell applications, in: Proc. of PVSAT-11, University of Leeds, Leeds, UK, (2015) pp. 149–152 (Poster).
7. **O.I. Olusola**, M.L. Madugu, I.M. Dharmadasa, Development of n- and p-type ZnTe Semiconductors for application in Electronic Devices, UK

Semiconductors & UK Nitrides Consortium Summer Meeting, Sheffield, United Kingdom, 1-2 July, 2015, pp. 130 (Poster).

8. **O.I. Olusola**, M.L. Madugu, I.M. Dharmadasa, Improvement of CdS/CdTe Solar Cell Parameters using ZnS Buffer Layer, in: Proc. of PVSAT-12, University of Liverpool, Liverpool, UK, (2016) pp. 107–110 (Oral Presentation). http://www.pvsat.org.uk/proceedings/.

Submitted articles for Publication

1. **O.I. Olusola**, M.L. Madugu, I.M. Dharmadasa, Investigating the electronic properties of multi-junction ZnS/CdS/CdTe graded bandgap solar cells, Submitt. to J. Mater. Chem. and Phys. (2016).
2. **O.I. Olusola**, M.L. Madugu, A.A. Ojo, I.M. Dharmadasa, Investigating the effect of $GaCl_3$ incorporation into the usual $CdCl_2$ treatment on CdTe-based solar cell device structures, Submitt. to J. Curr. Appl. Phys. (2016).
3. I.M. Dharmadasa, M.L. Madugu, **O.I. Olusola**, O.K. Echendu, F. Fauzi, D.G. Diso, A.R. Weerasinghe, T. Druffel, R. Dharmadasa, B. Lavery, J.B. Jasinski, T.A. Krentsel, G. Sumanasekera, Electroplating of CdTe Thin Films from Cadmium Sulphate Precursor and Comparison of layers grown by 3-electrode and 2-electrode systems, Submitt. to Coatings. (2016).
4. A.A. Ojo, **O.I. Olusola**, I.M. Dharmadasa, Effect of the inclusion of gallium in normal cadmium chloride treatment on electrical properties of CdS/CdTe solar cell, Submitt. to J. Mater. Chem. and Phys. (2016).

Abstract

The main aim of the work presented in this thesis is to develop low-cost multi-junction graded bandgap solar cells using electroplated semiconductors. The semiconductor materials explored in this research are CdSe, ZnTe, CdS, CdMnTe and CdTe thin films. These layers were characterised for their structural, compositional, morphological, optical, and electrical features using XRD, Raman spectroscopy, EDX, SEM, UV-Vis spectroscopy, PEC cell, C-V, I-V and UPS measurement techniques respectively. The summary of the results depict that CdSe and CdS semiconductors have hexagonal crystal structures and are mainly n-type in electrical conduction within the explored range of deposition potentials. The crystal structures of ZnTe thin films are hexagonal and the electroplated ZnTe thin films have both n- and p-type electrical conduction. In the literature, the electrical conductivity type of ZnTe thin films has been reported to be p-type. In this work, the developments of n-type ZnTe thin films have been successfully achieved for the first time by using intrinsic doping. Also, the fabrication of p-n homo-junction diodes from intrinsically doped electroplated ZnTe layers have been developed for the first time. Results from analytical techniques showed that CdTe and CdMnTe thin films have cubic crystal structures and can exist as n- and p-type materials. The semiconductor materials investigated in this work have been used for solar cells fabrication. Some of the device structures explored are based on p-n hetero-junction solar cells fabricated from CdS/ZnTe hetero-structure and combination of n-n hetero-junction plus large Schottky barrier (n-n+SB) solar cells fabricated from CdS/CdTe hetero-structure. The highest efficiency obtained for the p-n junction solar cell with device structure glass/FTO/n-CdS/p-ZnTe/Au was ~5.3% while the highest efficiency reported in this work for n-n+SB solar cells with device structure glass/FTO/n-CdS/n-CdTe/Au was ~7.6%. Multi-junction graded bandgap solar cells with different device structures were also fabricated in this research work. The two most important solar cells in this category are n-n-n plus large Schottky barrier (n-n-n+SB) solar cells fabricated from glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures and n-n-p solar cells fabricated from glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device structures. The n-n-p device structure is a combination of one n-n hetero-junction and one n-p homo-junction interface. The experimental investigations carried out on the effect of thickness of p-CdTe on n-n-p device structures showed that thinner p-CdTe layer of ~35 nm is most appropriate to be used in the n-n-p solar cells device configuration. The highest efficiency obtained for the n-n-p solar cell device structures was ~10.9% while the highest efficiency obtained for the n-n-n+SB solar cell device structures was ~12.8% with an active area of ~0.031 cm^2.

Table of Contents

List of Figures

List of Tables

Chapter 1 - Introduction

1.1 Energy and its universal importance

According to the report by British Broadcasting Corporation (BBC) [1], universal demand for energy has risen relentlessly as a result of growth in population and industrial development. According to the report, demand for energy has been predicted to keep on rising by at least 50% by year 2030 as countries like India and China seek to sustain their rapid economic growth. The trend of increase of the listed energy sources with the projected future demand is shown in Figure 1.1. As shown in Figure 1.1, about 80% of the global energy is being supplied by fossil fuels namely coal, oil and gas. Fossil fuels are carbon compounds formed over a long period of time from the remains of dead animal and plants. They have a time frame for them to be used up and are also non-renewable energy sources.

In the recent decades, a great concern has been raised over the negative impact the gases emitted by burning of fossil fuels will have on the environment. These gases are known as greenhouse gases and they include carbon dioxide (CO_2), sulphur dioxide (SO_2) and methane (CH_4). The accumulation of these gases in atmosphere leads to climate change and causes global warming. Since the energy sources from fossil fuels cannot be replenished after usage, there is therefore a cogent need to find an alternative energy sources that is renewable.

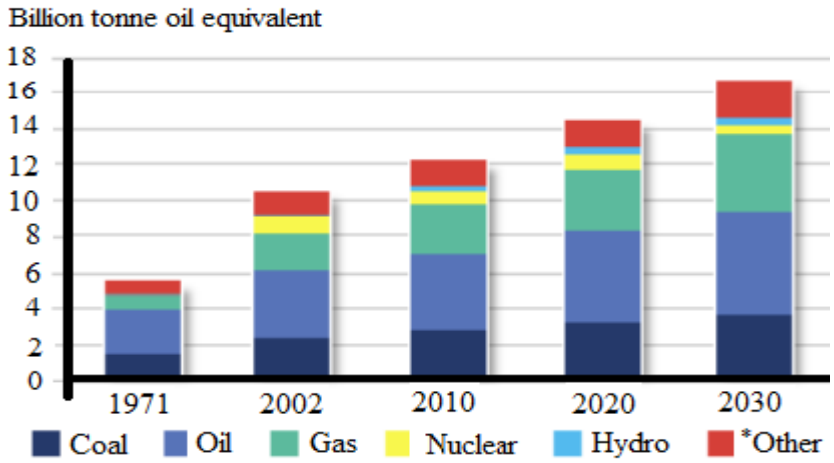


Figure 1.1. Projected future demand for different energy sources. Note that (*Other) includes geothermal, wind, heat, solar and so on [1].

1.2 Energy sources

The sustenance of living things on the face of the Earth depends strongly on the availability of energy sources. These energy sources can be classified as renewable and non-renewable.

1.2.1 Non-renewable energy sources

Non-renewable energy resources cannot be replaced at the rate at which they are being consumed. Fossil fuels such as coal, crude oil and natural gas are the main sources of this non-renewable energy. When burnt, fossil fuels emit greenhouse gases causing environmental pollution. The perpetual use of fossil fuels at the present rate is also believed to contribute to global warming increase and cause severe changes in the climate conditions [2]. Due to the negative impact the emitted gases from fossil fuels are creating on the environment, it is therefore essential to look for a clean source of energy which is environmental friendly, hence the need for solar energy.

1.2.2 Renewable energy sources

Renewable energy sources are abundant in nature, clean, sustainable and environmentally friendly. The environmental friendliness is due to the fact that they do not contribute to environmental pollution that comes as a result of greenhouse gases emission into the atmosphere. Also, they do not contribute to global warming which has been a huge concern to the entire populace. Some of the alternative renewable energy resources are: hydropower, wind, biomass, biofuel, tidal, geothermal and solar energy. Among all these renewable energy resources, solar energy happens to be the best energy source since virtually all other renewable energy resources derive their source from sunlight either directly or indirectly [3].

1.3 Solar energy

Solar energy is the energy emitted by the Sun and its energy is distributed as shown in the electromagnetic spectrum of the Sun. Solar technology can be classified as either active or passive based on the manners they capture and transform energy. While passive solar technology makes use of materials with good thermal characteristics and positioning of buildings in such a way that it will be warmed by the Sun; active solar technologies basically make use of concentrated solar power, solar thermal collectors

and solar photovoltaics [3]. Concentrated solar power generates energy by using lenses, mirrors or reflectors to concentrate sunlight from a large area onto a small area [4]. Once the concentrated or focused light is converted to heat, it drives a steam turbine connected to an electrical generator which generates electricity [5]. Solar thermal collector (STC) absorbs sunlight and uses it to generate heat. The thermal energy produced from the STC can be used for domestic hot water heating or space heating [6]. Solar photovoltaics (SPV) convert light energy from the Sun into electricity using thin layers of semiconductor materials [7]. The SPV are noiseless and produce clean energy.

The Sun's constituents are mainly hydrogen and helium elements. The Sun's composition by mass is ~71.0% H and 27.1% He. Less than 2.0 % of the mass of the Sun belong to other various metals [8]. The Sun whose temperature at the surface is about 5726^{o}C happens to be the main source of solar radiation [9]. The total power produced by the Sun is ~3.85×10^{26} W [10]; however, it is not all the energy from the Sun (solar radiation) that reaches the Earth's surface. The atmosphere affects the amount of solar radiation received. For example, when solar radiation travels through the atmosphere, about 26% is scattered or reflected back to space by atmospheric particles and clouds, ~4% is reflected back to the space by Earth's surface, ~19% is absorbed by clouds, atmospheric gases and particles while only ~51% is available at the Earth's surface of all the sunlight that passes through the atmosphere annually [11]; this analysis is shown in Figure 1.2.

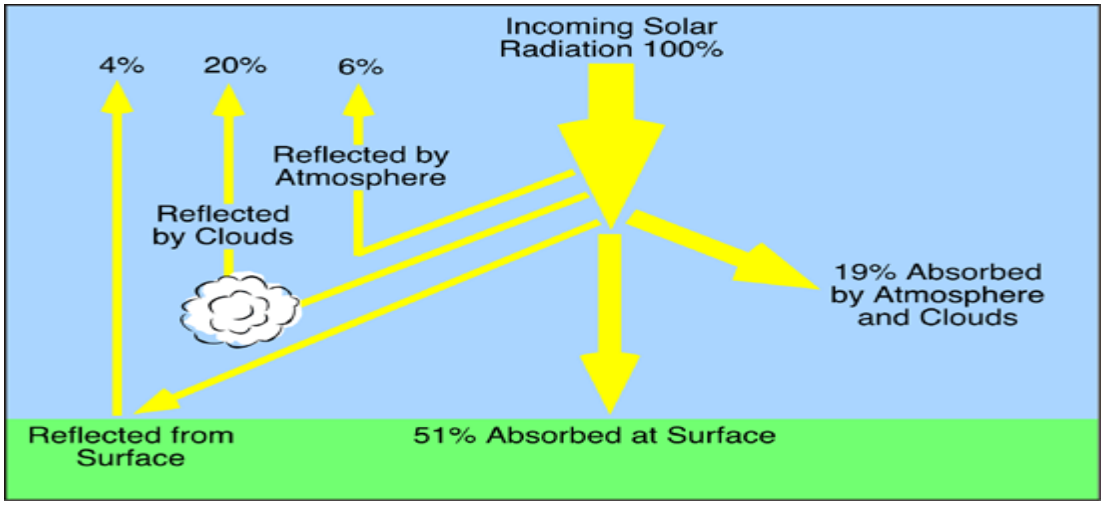


Figure 1.2. Reflected and absorbed solar radiation [11].

1.4 Solar spectrum

As previously discussed, the incoming radiation from the Sun can be harnessed using a wide range of modern technologies such as solar photovoltaics, solar thermal, solar heating and so on [3]. The radiation (light and heat) given out by the Sun to the Earth is in form of electromagnetic waves which have different wavelengths. Radiations such as ultraviolet, X-rays and visible light have short wavelengths while infrared radiations have longer wavelengths. The solar radiation spectrum shown in Figure 1.3 comprises of electromagnetic radiation of various wavelengths. This spectrum can be divided into three main parts namely: (i) Ultraviolet region with λ <400 nm, {this region contains approximately 5% of the irradiance}; (ii) Visible region with wavelength ranging from 400 nm to 700 nm, {this region contains approximately 43% of the irradiance} and (iii) Infrared region (λ >700 nm), {this region contains ~52% of the irradiance} [12,13].

Using the solar thermal and photovoltaic technologies, the spectrum from the ultraviolet region to the infrared end can be used for terrestrial energy applications [14]. The solar thermal technology is used in harnessing the solar energy found at the infrared region of the solar spectrum while photovoltaic (PV) technology is used to harness the solar energy at the UV and visible region of the solar spectrum. With the new PV technology model of multi-layer graded bandgap solar cell structures proposed by Dharmadasa in 2005 [15,16], it is also possible for solar cells to harness the infrared radiation in the solar spectrum via impurity PV effect and impact ionisation. In this report, main emphasis is laid only on semiconductor materials which find useful applications in photovoltaic solar energy conversion.

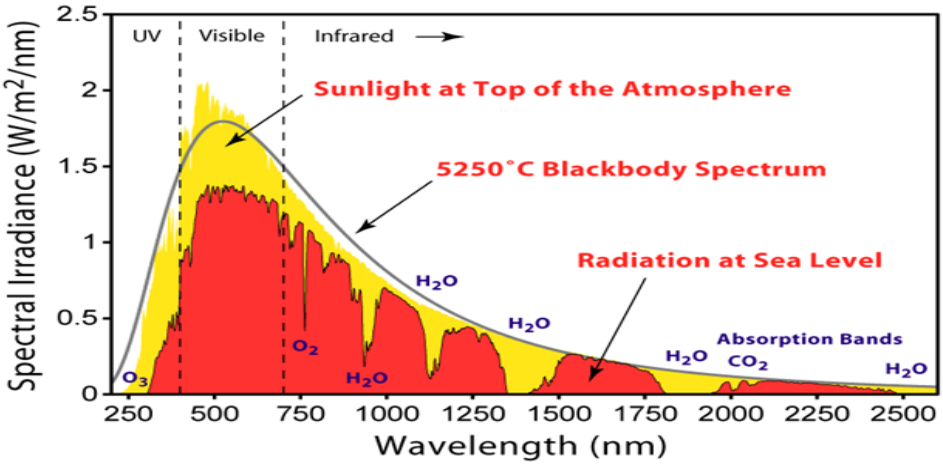


Figure 1.3. The energy spread in the solar spectrum [12,13].

1.5 Air mass

Air mass (AM) is the measure of how light travels through the Earth's atmosphere; it can also be defined as the path lengths through which sunlight takes within atmosphere to reach the Earth's surface. When light passes through the Earth's atmosphere, its intensity will attenuate due to absorption, reflection or scattering of sunlight by air molecules, dust and clouds [12]. The average solar energy falling on the Earth's surface is known as Air-Mass 1.5 (AM1.5) radiation; this is illustrated in Figure 1.4. AM1.5 is the air-mass when the Sun moves at an angle of ~48.2^{o} from the zenith [17]. This radiation is defined as an insolation with corresponding power of about 1000 Wm^{-2} or 100 mWcm^{-2} [18]; this value is used by the PV industry as Standard Test Condition (STC) for terrestrial solar panels. The air mass 1.0 (AM1.0) is when the solar spectrum has travelled through the atmosphere with normal incidence above the point on the Earth or when the Sun is directly at its zenith above the point on the Earth. AM1.0 is used in the tropical regions of the Earth to characterise solar cells; the incident power per unit area corresponds to ~1040 Wm^{-2} [19]. The air mass zero (AM0.0) is the solar irradiance in space that is not affected by the atmosphere and it occurs when the Sun stands on the zenith; this means there is no atmospheric presence between the solar cell and Sun [17]. The AM0.0 is used to characterise solar cells used in space power applications like the ones on communication satellites [19]. The power density of AM0.0 light is about 1,367 Wm^{-2} which is considered to be the solar constant [17,19].

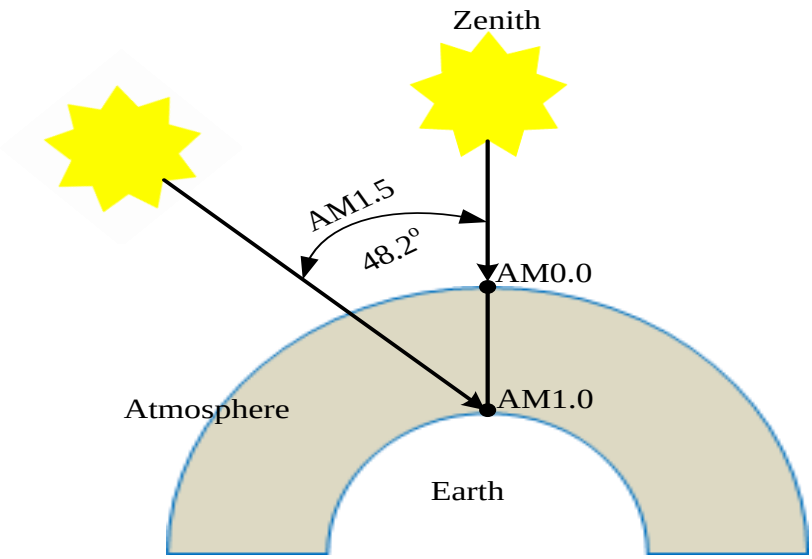


Figure 1.4. Path lengths taken by the solar spectrum through the atmosphere.

1.6 Photovoltaic technology

Photovoltaic (PV) is the technology used in generating electrical power by converting the solar radiation that reaches the Earth's surface into direct current (DC) using suitable semiconductor devices that exhibit the photovoltaic effect. It is not all semiconductor devices that can be used as solar cells; some may function well as good diodes but may not exhibit excellent PV activity when measured under illumination condition. Materials presently used for PV include: monocrystalline silicon, polycrystalline silicon, amorphous silicon, cadmium telluride and copper indium gallium di-selenide (CIGS) [20]. Four standard steps are involved in converting sunlight energy into direct current. The first two steps involve using suitable semiconductor materials that can absorb photons and convert the absorbed photons to electron-hole pairs. The other steps have to do with effective separation of the oppositely charged photo-generated charge carriers and collection of the photo-generated charge carriers via electrical contacts in an external circuit [20].

Photons which come directly from the Sun have different energies which correspond to the various wavelengths of the solar spectrum. It is not all the photons which hit the solar cells that are absorbed; some are transmitted while others are being reflected. The useful photons are the absorbed ones and when these photons fall in the depletion region of the solar cell, they break bonds between the semiconductor atoms to create free charge carriers. It is the quick separation of these photo-generated charge carriers and transference to the external circuit which generates useful electricity.

1.6.1 Energy of photons

The solar radiation comprises of elementary particles called photons. A photon is the quantum of light (electromagnetic radiation) and is characterised by its Energy *E*, which is a function of frequency, *v*. The photon energy is related to frequency by the Equation (1.1) [21].

$$E = h\upsilon \tag{1.1}$$

E is energy in Joules (*J*), *h* is Planck's constant (6.626×10^{-34} JS) and *v* is frequency in Hz.

The photon energy can also be expressed in terms of its wavelength λ, thus Equation (1.1) becomes

$$E = \frac{hc}{\lambda} \quad (1.2)$$

Where c is the speed of light in ms^{-1} and λ is the wavelength in m.

When the wavelength λ is in nm and the values of c and h are substituted using appropriate units, then the photon energy can be obtained in electron volts (eV), which is mostly used in PV solar cell calculations. Under this condition, Equation (1.2) becomes

$$E \cong \frac{1240}{\lambda}(eV) \quad (1.3)$$

To express the photon energy in Joules (J), the wavelength λ is expressed in m as illustrated in Equation (1.4).

$$E \cong \frac{1.99 \times 10^{-25}}{\lambda}(J) \quad (1.4)$$

1.6.2 Brief history of photovoltaic technology

The PV effect was first discovered by Edmund Becquerel, a French scientist in 1839 [22] when the silver chloride he placed in an acidic solution (electrolyte) generated electric power while being connected to platinum electrodes. In the real sense, the photovoltaic effect occurred at the junction formed between the platinum electrode and electrolyte. The first PV activity with a reasonable amount of electromotive force (EMF) was reported by Ohl in 1940 through an experiment he did on silicon based p-n junction device [23]. A major breakthrough happened in 1954 at Bell laboratory with the development of the first 4.5% efficiency silicon solar cell by Daryl Chapin, Calvin Souther Fuller and Gerald Pearson compared to the selenium cells that found it difficult to reach 0.5% [24,25]. Researchers at the Hoffman Electronics Corporation increased this efficiency to about 14% in 1960. The oil crises from 1970-1974 led to the search for PV solar cell technology as an alternative energy resource for terrestrial use. During this period, the main focus was on silicon semiconductor material; this is due to abundance of raw materials for silicon production in the Earth's crust and the knowledge accumulated on silicon. However, the cost of production of a silicon solar panel has been on the high side due to various production processes involved. To therefore reduce the dollars/Watt ($/W) for a solar panel production and improve efficiency, researchers

have focused on other semiconductor compounds such as the binary compound semiconductors [20].

Using the production cost, photovoltaic technologies can be grouped into three main generations. The first generation solar cells are the high efficiencies solar cells with high cost of production. Examples are silicon (Si) and gallium arsenide (GaAs)-based solar cells. The recent reports published by Martin Green et al. [26] showed that monocrystalline Si and thin film GaAs solar cells have efficiencies >25.6% and 28.8% respectively at the laboratory scale level. The high cost of production for this generation of solar cells makes their dollars/Watt to be higher than 1$/W [27]. Thin film solar cells such as copper indium gallium diselenide (CIGS) and cadmium telluride (CdTe) belong to the class of second generation solar cells. They are referred to as thin films because they are products of semiconductor materials of thickness of few microns.

The second generation solar cells are low-cost and with a lower efficiency when compared to the first generation solar cells. The low-cost of production of these solar cells seem to be the major advantage since fewer materials and lesser cost of production processes are involved; the main disadvantage however is their lower efficiency. The US dollar/Watt for the second generation solar cells varies between (0.20-1.00) $/W [27]. The CIGS and CdTe solar cells have efficiencies >21.0% for lab scale devices. Presently, the First Solar Company based in US has achieved the highest efficiency in CdTe thin films both at lab-scale and module level [28]. Both the first and second generation solar cells mentioned above are inorganic materials-based solar cells.

The third generation solar cells are also low-cost low efficiency solar cells. A very good example is the dye-sensitised solar cells (DSSCs). The highest efficiency reported for DSSCs in the solar cell efficiency tables (version 46) for lab scale devices is 11.9±0.4% [26]. Organic photovoltaic (OPV) solar cell is another example of third generation solar cells and it has the advantage of lower cost/m^2 than inorganic thin film solar cells due to their lower processing temperatures and deposition [27]. The highest efficiency reported for organic thin film solar cells at lab scale level is 11.0±0.3% [26]. The US dollar/Watt for the third generation solar cells varies between (0.10-0.50) $/W [27].

1.6.3 Brief history of CdTe-based solar cell

One of the most recognised absorber materials from II-VI binary compound semiconductors that have long been used in the fabrication of thin film solar cells is

cadmium telluride (CdTe). CdTe has a high optical absorption coefficients $>10^4$ cm^{-1} [29] and a near-optimum bandgap of 1.44 eV [30] for simple p-n junction devices. Mathers and Turner in 1928 [31,32] gave the first report on the electrodeposition of CdTe using an aqueous and acidic solution of $CdSO_4$, TeO_2 and H_2SO_4 but the emergence of CdTe as a viable electronic material came into existence in the year 1947 through Frerichs experimental work [33]. In the author's work, CdTe crystals were synthesised in a hydrogen atmosphere through the reaction of Cd and Te vapour. In 1954 [34], Jenny and Bube carried out a research on the electrical conductivity type that can be obtained in CdTe and the authors came to the conclusion that p- and n-type electrical conduction are obtainable by extrinsically doping the CdTe with foreign impurities. Not long after the discovery made by Jenny and Bube [34], Kruger and de Nobel [35] showed that achieving n- and p-type electrical conduction is not only limited to extrinsic means of doping; they showed that by intrinsically varying the Cd-Te stoichiometry, n- and p-type electrical conduction could equally be obtained. The authors obtained n-type with higher Cd ratio and p-type with higher Te ratio. In 1956, the proposal to use CdTe as a semiconductor material for photovoltaic solar energy conversion was made by Loferski [36]. In 1959, the first homojunction solar cell from single crystal CdTe was made by Rappaport [37]; the reported conversion efficiency was ~2% and this was made by diffusing In into p-type CdTe crystals. Subsequent works after this yielded efficiency >7% [38] and 10.5% [39] for p-n single crystal CdTe homojunction cells.

Shortly after this in the early 1960s, the solar cell device structures shifted from homojunction to heterojunction based devices. The first work relating to CdTe-based heterojunction solar cell was carried out by Cusano [40] and made available to the public domain in the year 1963. Cusano [40] achieved an efficiency of ~6% using the device structure n-CdTe/p-Cu_2Te. This fabricated device suffered from stability with time due to the diffusion of Cu into the n-CdTe layer and this eventually lowered the cell efficiency [41,42]. The instability observed in the n-CdTe/p-Cu_2Te device structure and lack of transparent p-type semiconductor as window layer for the n-CdTe absorber thin films prompted the PV researchers to explore other device configurations utilising p-CdTe as an absorber layer. The main task was to now find an appropriate n-type semiconductor as a suitable window layer to p-CdTe absorber layer. In 1964, Muller et al. [43] reported the fabrication of solar cell from n-CdS/p-CdTe with a conversion efficiency <5%. In their work, the authors evaporated n-CdS thin films on a single

crystal p-CdTe layer. Yamaguchi et al. [44] in the year 1977 reported the highest solar cell efficiency of ~11.7% from a p-CdTe single crystal and n-CdS thin film.

The earlier research works carried out on CdTe-based solar cells mainly came from single crystal p-CdTe layer. The first polycrystalline CdS/CdTe heterojunction based solar cells were demonstrated by Adirovich et al. [45] in the year 1969 using the superstrate configuration while in 1972, Bonnet and Rabenhorst [46] reported the fabrication of CdS/CdTe heterojunction based solar cells with a conversion efficiency of ~6% using the substrate configuration. The techniques used by Bonnet and Rabenhorst [46] in developing CdTe and CdS thin films were chemical vapour deposition and vacuum evaporation respectively. Since then, researchers working on thin film solar cells have been using these two configurations in solar cells fabrication. However, superstrate polycrystalline thin film CdS/CdTe heterojunction device structures have received a notable research and development (R&D) awareness and the highest solar cell efficiency among the CdTe-based solar cell configurations have been achieved using the superstrate configuration [28,47].

Different techniques have also been used by various research groups and companies to produce CdTe-based solar cells since inception. Among these many techniques, screen printing [48], closed-space sublimation [49] and electrodeposition [50] have been used to successively achieve solar cell efficiency of over 8%. Closed space sublimation (CSS) was used by the research group at Kodak to achieve ~10% efficiency for CdTe-based solar cells. The group was able to successfully optimise the temperature used in CdTe deposition and the amount of Oxygen in the deposition chamber. The authors grew the CdTe layers in a reactor which permitted controlled oxygen contents to be incorporated into the deposition atmosphere during film growth [49].

In 1984, Basol [51] reported the fabrication of electroplated n-CdS/p-CdTe heterojunction solar cells with an efficiency of ~9.4%. The solar cell parameters obtained by the author for an active cell area of 0.02 cm^2 are: V_{oc} = 0.73 V, J_{sc} = 20 $mAcm^{-2}$ and FF = 0.64. In the subsequent investigations carried out by Basol on CdTe-based solar cell fabrication [52], the author was able to achieve ~10.3% and 10.6% efficiency for CdS/CdTe and CdS/HgCdTe-based solar cells respectively. The energy band diagram for a typical n-CdS/p-CdTe is shown in Figure 1.5

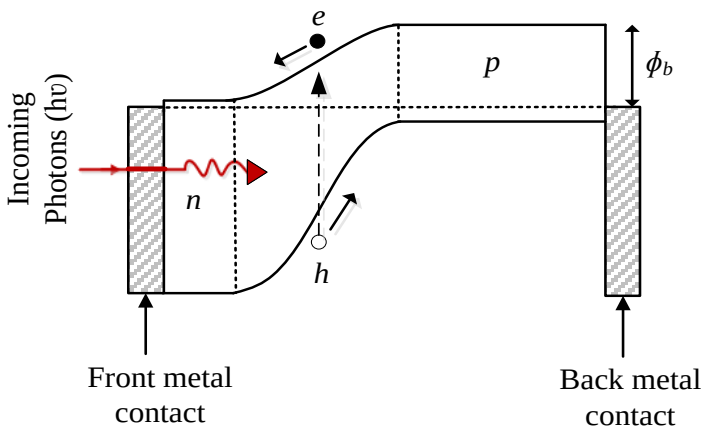


Figure 1.5. Energy band diagram of a typical p-n junction solar cell based on n-CdS and p-CdTe.

In the actualisation of these high efficiency cells, researchers have also shown that the device structures and processing steps are other important factors to achieve high efficiency solar cells [47,53,54]. The incorporation of $CdCl_2$ treatment as part of post-deposition processing step for CdTe-based device structures has significantly improved the solar cell device performance. In the year 1991, Ringel et al. [55] reported the influence of $CdCl_2$ treatment on solar cell fabricated from the device structure glass/SnO_2/CdS/CdTe/ZnTe/Ni. The authors observed a tremendous increase from 1.3% to 8.6% for device structures treated without and with $CdCl_2$ respectively. The subsequent works carried out by Britt and Ferekides in the year 1993 in using $CdCl_2$ treatment on their solar cell device structures yielded an efficiency of 15.8% [56]. The progress in the CdS/CdTe-based solar cell was stagnated for ~8 years until Wu et al. [57] broke the existing record by Britt and Ferekides in 2001. An efficiency of 16.5% was achieved by Wu et al. [57,58] after using a high quality cadmium stannate (Cd_2SnO_4) as the new transparent conducting oxide (TCO) to replace the conventional fluorine-doped tin oxide (FTO) and a modified device structure for the solar cell fabrication. However, this increase after nearly a decade of research is marginal; and increased only by ~0.7% which is within the fluctuation of measurements.

In 2002, a new model for CdTe-based solar cell fabrication was proposed by Dharmadasa et al. [59] as a means of further improving CdS/CdTe based solar cells. The present PhD research is based on this new model. This new model consists of two rectifying junctions connected in parallel; these are n-n heterojunction and a large Schottky barrier interface at the semiconductor/metal contact. The n-n heterojunction is

basically from n-CdS/n-CdTe interface while the Schottky barrier is formed at the n-CdTe/metal interface. The new model originated from the comprehensive works carried out by the author on metal contacts to some selected semiconductors from II-VI binary compound family [60]. The energy band diagram of the proposed new model is illustrated in Figure 1.6. Using this new model, the authors were able to fabricate solar cell devices with an open circuit voltage (V_{oc}) >600 mV, short-circuit current density (J_{sc}) >60 mA cm^{-2} and fill factor (FF) values of ~0.60. These parameters under illumination condition yielded an overall efficiency of ~18%. The result of the solar cell efficiency fabricated by Dharmadasa et al. [59] showed that the proposed new model has a great prospect over the single p-n junction model.

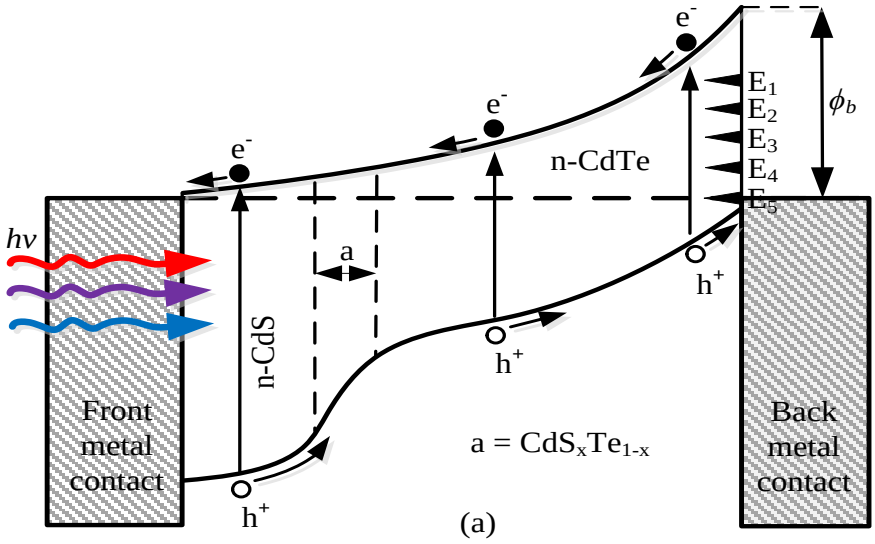


Figure 1.6. Energy band diagram of the proposed n-CdS/n-CdTe (n-n) heterojunction device structure with a large Schottky barrier at the metal back contact. Note that the defect levels responsible for Fermi-level pinning are shown as E_1 to E_5.

One remarkable feature in this proposed model is the observed high J_{sc} value. This value was far greater than the reported J_{sc} limit [61] for a single p-n junction CdTe solar cell. This huge difference can however be attributed to the tandem nature of the device configuration used by Dharmadasa et al. [59]. Other important factors discussed by Dharmadasa et al. [59] in the new model are the presence of defect levels in n-CdTe thin films. The defect levels were earlier observed in the authors' previous works on metal/n-CdTe interface [60] and later applied to device fabrication. Due to the presence of these defects, strong Fermi level pinning can take place without depending on the

metal work function. The 5 defect levels experimentally identified are located in the band gap at E_1=0.40±0.04, E_2=0.65±0.02, E_3=0.73±0.02, E_4=0.96±0.04 and E_5=1.18±0.02 eV below the conduction band minimum [59,60]. According to Dharmadasa [60], the position for Fermi level pinning depends on the material history and methods used in fabricating the metal contact. The material history may also have to do with steps taken to process the semiconductor material most especially before metallisation process. One of these processing steps is the chemical treatments followed by heating of the semiconductor material. The application of chemical treatments to the top surface of the CdTe layer and heat-treatment in air lead to: improvement in the material crystallinity, reduction of series resistance, removal of unwanted defects, formation of larger grains and passivation of grain boundaries [55,62,63].

Another processing step is the etching process which is normally carried out after annealing. In this process, the oxides on the top surface of the CdTe layer are removed. The types of etchants used can also determine where the Fermi level pinning actually takes place. Dharmadasa [60] explained that when the top surface of n-CdTe is treated with an acidic etchant, the acid attacks the Cd element preferentially thereby leaving the surface as Te-rich while a basic etchant attacks the Te element preferentially and leave a Cd-rich surface. Cd-rich CdTe surfaces are associated with defect levels at 0.96 eV and 1.18 eV while Te-rich CdTe surfaces are associated with defect levels at 0.65 eV and 0.73 eV below the conduction band minimum [64,65]. The experimental work carried out by Schulmeyer et al. [66] showed that CdTe with n-type electrical conduction is needed to produce high efficiency solar cell devices. With Cd-rich surface, CdTe becomes n-type and the Fermi level pinning can be at defect levels 0.96 eV and 1.18 eV. With this pinning, a larger Schottky barrier height is produced at the interface and this increases the slope of the band diagram and creates the required high internal electric field across the device structure. Due to this band bending, a healthy depletion region is formed across the device.

1.6.3.1 Principle of operation of substrate and superstrate device configurations

Typical schematic diagrams of CdS/CdTe-based solar cells fabricated using superstrate and substrate configurations are shown in Figures 1.8 (a) and 1.8 (b) respectively. In the superstrate configuration, the initial deposition is always done on the glass superstrate which acts as a support for the deposited layers. The first deposited layer is the TCO and this serves as the front contact. This is followed by sequential deposition of other

semiconductor materials such as CdS window layer and CdTe absorber layer. The metal contact (such as Au) is now evaporated on the CdTe absorber layer to serve the purpose of a back contact; Figure 1.7 (a) illustrates CdTe-based solar cells using the superstrate configuration. In the substrate configuration, the deposition starts from the back contact. In this case, the CdTe layer is first deposited onto a conducting substrate (for example, Molybdenum foil) which acts as the back contact and this is successively followed by CdS and TCO deposition. The TCO in this case acts as the front contact; this is illustrated in Figure 1.7 (b). In both cases, light enters the solar cell devices via the TCO and CdS thin films. In the superstrate configuration, light has to pass through the glass before getting to the CdS/CdTe interface unlike the substrate configuration where light enters directly the CdS/CdTe junction without any obvious/major obstruction.

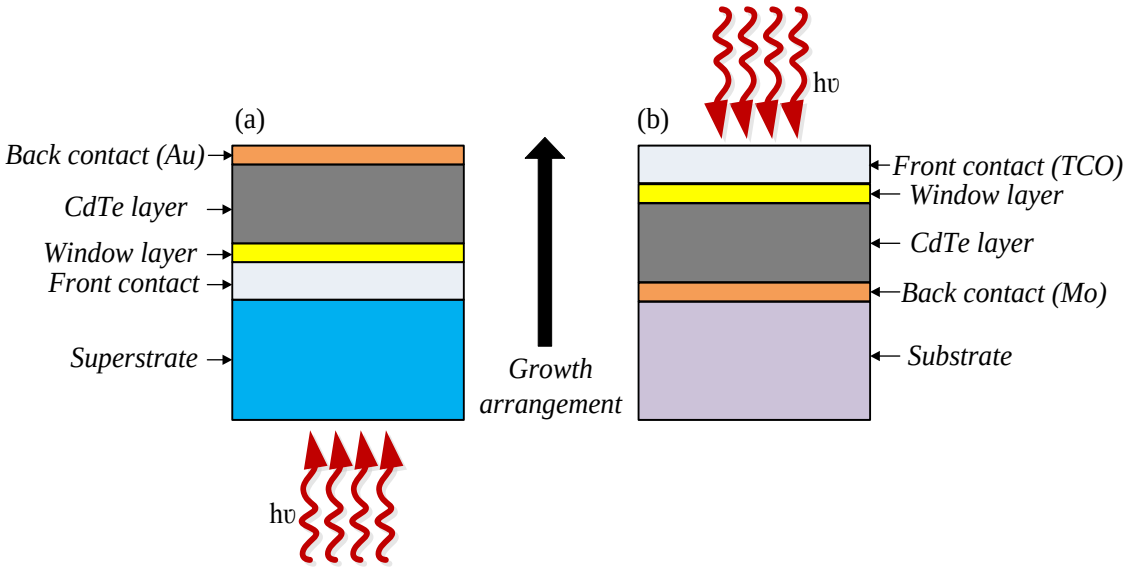


Figure 1.7. Solar cell configurations used for CdTe thin film solar cells, (a) superstrate and (b) substrate configurations.

1.7 Present challenges in CdTe-based solar cell device structures

The efficiency of most solar cells fabricated from heterojunction materials for example, when using thin layers of CdS as window materials and CdTe as absorber materials have been reported in numerous articles in the literatures to be adversely affected by pinholes formation. To therefore minimise and stop these pinholes formation, wide bandgap and high resistive buffer semiconductor layers have been suggested as some of the means for preventing pinholes formation [67]. The presence of pinholes in the thin

film materials leads to creation of leakage paths and short-circuiting between the back and front metal contacts and this adversely affect the solar cell performance. Zn-related compounds such as ZnO [68–71], ZnS [72] and $Zn_{1-x}Sn_xO$ [73] have been suggested by many researchers in the PV field as suitable buffer layers to stop the pinhole formation. In this present work, ZnS with larger bandgap of ~3.70 eV and a thin layer of ZnTe with modified bandgap of 2.60 eV have been used to serve the purpose of pinholes minimisation and bandgap grading.

Some of the other present challenges involved in thin film solar cells fabrication have to do with improving all the solar cell parameters which are short-circuit current density (J_{sc}), open circuit voltage (V_{oc}) and fill factor (FF). The idea of using $CdCl_2$ for treatment in CdTe thin films can be dated back to 1976 [74,75] to improve device parameters without full understanding. Since one of the main aims of this work is to understand the $CdCl_2$ treatment and further improve the device parameters, other chemical treatments such as $GaCl_3$ have been introduced. The incorporation of $GaCl_3$ into the usual $CdCl_2$ treatment emerged as a result of the experimental results reported in $X-\text{ray}$ and $\gamma-\text{ray}$ community by Sochinskii et al. [76] in dissolving Te precipitates with Ga. Since the midgap defects known as killer centres in CdTe originate from Te-richness [77], finding a possible means of reducing these defects would cause the efficiency of the CdTe-based solar cell device structures to improve. Therefore, since Ga has the potential of removing these Te precipitates, the incorporation of $GaCl_3$ into the universal $CdCl_2$ treatment has been proposed in this work to be used as means of surface treatment to improve the efficiency of CdTe-based solar cells. In addition to the chemical treatments, new device structures based on glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p device structure) have also been proposed as a means of improving the solar cell device parameters by moving towards multi-layer graded bandgap devices.

1.8 Research Aim and Objectives

The main aim of this research work is to implement the existing CdTe-based solar cell structures proposed by Dharmadasa et al. [59] in 2002 using low-cost electroplating technique with simplified fabrication process and to develop new device architectures based on graded bandgap devices for CdTe-based solar cell in order to enhance the efficiency. The semiconductor materials used in this research for device fabrication are CdSe, ZnTe, ZnS, CdS, CdTe and CdMnTe.

Some of the works carried out in this research programme and reported in this thesis are based on the device architectures reported by Echendu [14] to test the reproducibility. The work involved the use of multi-junction graded bandgap solar cells employing glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structure. By optimising the thickness of the CdTe layer and incorporating $GaCl_3$ into the universal $CdCl_2$ chemical treatment, improvement in the efficiency of the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au have been recorded compared to the previous work carried out by Echendu [14].

Some of the new device structures developed are glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au and glass/FTO/n-CdS/n-CdTe/p-CdTe/Au. The ZnTe work reported here follows the comprehensive works carried out by Diso [78] and Fauzi [79] on electroplated ZnTe layers. In both authors work, they were able to report only the fabrication of p-ZnTe layers. In this present work, both n- and p-type ZnTe layers have been successfully fabricated using intrinsic doping and these electroplated layers have been applied to solar cell device making; this can be seen as an improvement over the earlier works reported by the duo. A detailed work on the fabricated n- and p-type ZnTe layers have been reported by Olusola et al. [80].

This research work involves the use of electrodeposition technique to grow the selected semiconductor materials. The following procedures are to be followed to actualise the aim of the project:

(i) Obtaining suitable ranges for the deposition potential from the I-V curve of the electrolyte by using cyclic voltammetry technique.

(ii) The use of two electrode electrodeposition method for the growth of semiconductor materials.

(iii) The growth of some selected semiconductor materials by low-cost electrodeposition technique. The materials electroplated in this research work are: CdSe, ZnTe, CdS, CdTe and CdMnTe.

(iv) Full material characterisation by employing a wide range of advanced analytical techniques available at Materials and Engineering Research Institute, Sheffield Hallam University. The analytical techniques used are: Photoelectrochemical {PEC} cell, UV-Vis spectroscopy, X-ray diffraction {XRD}, Raman spectroscopy, Scanning electron microscopy (SEM), Atomic force microscopy {AFM}, energy-dispersive X-ray analysis (EDX), optical profilometry and ultra-violet photoemission spectroscopy (UPS).

(v) Hybrid device fabrication using the semiconductor materials listed above. The thin film solar cell device structures fabricated are: (a) glass/FTO/n-CdS/n-CdTe/back contact, (b) glass/FTO/n-ZnS/n-CdS/n-CdTe/back contact, (c) glass/FTO/n-ZnTe/n-CdS/n-CdTe/back contact, (d) glass/FTO/n-CdS/n-CdTe/p-CdTe/back contact, (e) glass/FTO/n-CdS/n-CdTe/p-ZnTe/back contact and (f) glass/FTO/n-CdS/n-CdTe/p-CdMnTe/back contact.

(vi) Development of the solar cell device structures to achieve highest possible efficiency for terrestrial solar energy conversion by optimising the processing steps.

(vii) Assessment and efficiency evaluation of the final device structures using current-voltage (I-V) and capacitance voltage (C-V) techniques.

1.9 Summary

The universal importance of energy and the need to explore an alternative energy source that is clean, abundant in supply and renewable have been briefly presented. Solar energy seems to be the best source of renewable energy for terrestrial applications since most of the other renewable energy resources either have a direct or indirect dependence on sunlight. A brief history of photovoltaic technology and CdTe thin films was also presented. The current challenges in CdTe thin films with the research aims and objectives have also been discussed in this chapter.

References

[1] http://news.bbc.co.uk/1/shared/spl/hi/sci_nat/06/global_energy/html/introduction.stm (accessed April 12, 2016).

[2] http://en.wikipedia.org/wiki/Non-renewable_resource (accessed April 12, 2016).

[3] https://en.wikipedia.org/wiki/Solar_energy (accessed April 12, 2016).

[4] L. L. Kazmerski, J. Electron Spectros. Relat. Phenomena, **150** (2006) 105–135.

[5] https://en.wikipedia.org/wiki/Concentrated_solar_power (accessed April 13, 2016).

[6] https://en.wikipedia.org/wiki/Solar_thermal_collector (accessed April 13, 2016).

[7] M. A. Green, Energy Policy, **28** (2000) 989–998.

[8] http://hyperphysics.phy-astr.gsu.edu/hbase/tables/suncomp.html (accessed April 13, 2016).

[9] http://www.space.com/14745-sun-composition.html (accessed April 13, 2016).

[10] R. B. Larson, B. Volker, Sci. Am., **70** (2001).

[11] M. Pidwirny, Atmospheric Effects on Incoming Solar Radiation, in: Fundam. Phys. Geogr., 2nd Ed., (2006).

[12] http://www.eyesolarlux.com/Solar-simulation-energy.htm (accessed August 21, 2013).

[13] https://en.wikipedia.org/wiki/Solar_irradiance (accessed April 13, 2016).

[14] O. K. Echendu, PhD Thesis "Thin film solar cells using all-electrodeposited ZnS, CdS and CdTe materials," Sheffield Hallam University, Sheffield, 2014.

[15] I. M. Dharmadasa, J. S. Roberts, G. Hill, Sol. Energy Mater. Sol. Cells, **88** (2005) 413–422.

[16] I. M. Dharmadasa, N. D. P. S. R. Kalyanaratne, R. Dharmadasa, J. Natl. Sci. Found. Sri Lanka, **41** (2013) 73–80.

[17] L. L. Kazmerski, Renew. Sustain. Energy Rev., **1** (1997) 71–170.

[18] T. Markvart, L. Castaner,eds., Practical Handbook of Photovoltaics: Fundamentals and Applications, Elsevier Ltd, (2003).

[19] https://en.wikipedia.org/wiki/Air_mass_(solar_energy) (accessed April 13, 2016).

[20] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[21] D. A. Neamen, Semiconductor physics and devices:basic principles, third ed., McGraw-Hill, New York (2003).

[22] E. Becquerel, Comptes Rendus, **9** (1839) 561–567.

[23] R. S. Ohl, Light-Sensitive Electric Device, U.S. Patent 2,402,662. Filed May 27, 1941. Granted June 25, 1946.

[24] J. Perlin, The Silicon Solar Cell Turns 50, (2004). http://www.nrel.gov/education/pdfs/educational_resources/high_school/solar_cell_history.pdf.

[25] D. M. Chapin, C. S. Fuller, G. L. Pearson, J. Appl. Phys., **25** (1954) 676–677.

[26] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, E. D. Dunlop, Prog. Photovolt Res. Appl., **23** (2015) 805–812.

[27] S. J. C. Irvine, C. Candelise, Introduction and Techno-economic Background, in: Materials Challenges: Inorganic Photovoltaic Solar Energy, The Royal Society of Chemistry, United Kingdom (2014): pp. 1–26.

[28] R. Martin, MIT Technol. Rev. First Solar's Cells Break Effic. Rec., (2016). https://www.technologyreview.com/s/600922/first-solars-cells-break-efficiency-record/ (accessed June 28, 2016).

[29] J. L. Boone, T. P. Van Doren, A. K. Berry, Thin Solid Films, **87** (1982) 259–264.

[30] C. Ferekides, J. Britt, Sol. Energy Mater. Sol. Cells, **35** (1994) 255–262.

[31] F. C. Mathers, H. L. Turner, Trans. Am. Electrochem. Soc., **54** (1928) 293.

[32] R. K. Pandey, S. N. Sahu, S. Chandra, Handbook of semiconductor electrodeposition, first ed., Marcel Dekker Inc., New York (1996).

[33] R. Frerichs, Phys. Rev., **72** (1947) 594–601.

[34] D. Jenny, R. Bube, Phys. Rev., **96** (1954) 1190–1191.

[35] F. Kruger, D. de Nobel, J. Electron., **1** (1955) 190–202.

[36] J. J. Loferski, J. Appl. Phys., **27** (1956) 777–784.

[37] P. Rappaport, RCA Rev., **20** (1959) 373–397.

[38] J. Mimilya-Arroyo, Y. Marfaing, G. Cohen-Solal, R. Triboulet, Sol. Energy Mater., **171** (1979).

[39] G. Cohen-Solal, D. Lincot, M. Barbe, in: Conf. Rec. 4th ECPVSC, (1982): pp. 621–626.

[40] D. A. Cusano, Solid. State. Electron., **6** (1963) 217–218.

[41] D. Bonnet, Int. J. Sol. Energy, **12** (1992) 1–14.

[42] K. D. Dobson, I. Visoly-Fisher, G. Hodes, D. Cahen, Sol. Energy Mater. Sol. Cells, **62** (2000) 295–325.

[43] R. Muller, R. J. Zuleeg, J. Appl. Phys., **35** (1964) 1550–1556.

[44] K. Yamaguchi, H. Matsumoto, N. Nakayama, S. Ikegami, Jpn. J. Appl. Phys., **16** (1977) 1203–1211.

[45] E. I. Adirovich, Y. M. Yuabov, G. R. Yugadaev, Sov. Phys. Semicond., **3** (1969) 61–65.

[46] D. Bonnet, H. Rabenhorst, in: 9th IEEE Photovolt. Spec. Conf., New York (1972): pp. 129–132.

[47] B. E. Mccandless, J. R. Sites, Cadmium Telluride Solar Cells, in: Handb. Photovolt. Sci. Eng., first ed., John Wiley & Sons, Ltd, Chichester, West Sussex, England (2003): pp. 617–662.

[48] H. Uda, H. Matsumoto, Y. Komatsu, A. Nakano, S. Ikegami, in: Proc. 16th IEEE Photovo1taic Spec. Conf., San Diego, California (1982): p. 801.

[49] Y. S. Tyan, E. A. Perez-A1buerne, Y. Tyan and E. A. Peres-A1buerne, in: Proc. 16th IEEE Photo-Voltaic Spec. Conf., San Diego, California (1982): pp. 794–

800.

[50] B. M. Basol, E. S. Tseng, R. L. Rod, S. Ou, O. M. Stafsudd, B. M. Baso, E. S. Tseng, R. L. Rod, S. Ou, and O. M. Stafsudd, in: Proc. 16th IEEE Photovo1taic Spec. Conf., San Diego, California (1982): p. 805.

[51] B. M. Basol, J. Appl. Phys., **55** (1984) 601–603.

[52] B. M. Basol, Sol. Cells, **23** (1988) 69–88.

[53] B. M. Başol, Int. J. Sol. Energy, **12** (1992) 25–35.

[54] I. M. Dharmadasa, Coatings, **4** (2014) 282–307.

[55] S. A. Ringel, A. W. Smith, M. H. MacDougal, A. Rohatgi, J. Appl. Phys., **70** (1991) 881–889.

[56] J. Britt, C. Ferekides, Appl. Phys. Lett., **62** (1993) 2851–2852.

[57] X. Wu, J. C. Keane, R. G. Dhere, C. DeHart, D. S. Albin, A. Duda, T. A. Gessert, S. Asher, D. H. Levi, P. Sheldon, 16.5% efficient CdS/CdTe polycrystalline thin-film solar cells, in: Proc. 17th Eur. PVSEC, Munich, Germany (2001): pp. 995–1000.

[58] X. Wu, Sol. Energy, **77** (2004) 803–814.

[59] I. M. Dharmadasa, A. P. Samantilleke, N. B. Chaure, J. Young, Semicond. Sci. Technol., **17** (2002) 1238–1248. http://iopscience.iop.org/0268-1242/17/12/306.

[60] I. M. Dharmadasa, Prog. Cryst. Growth Charact. Mater., **36** (1998) 249–290.

[61] A. Morales-Acevedo, Sol. Energy Mater. Sol. Cells, **90** (2006) 2213–2220.

[62] A. Rohatgi, R. Sudharsanan, S. A. Ringel, M. H. MacDougal, Sol. Cells, **30** (1991) 109–122.

[63] A. Romeo, S. Buecheler, M. Giarola, G. Mariotto, A. N. Tiwari, N. Romeo, A. Bosio, S. Mazzamuto, Thin Solid Films, **517** (2009) 2132–2135.

[64] Z. Sobiesierski, I. M. Dharmadasa, R. H. Williams, Appl. Phys. Lett., **53** (1988) 2623–2625.

[65] I. M. Dharmadasa, J. D. Bunning, A. P. Samantilleke, T. Shen, Sol. Energy Mater. Sol. Cells, **86** (2005) 373–384.

[66] T. Schulmeyer, J. Fritsche, A. Thißen, A. Klein, W. Jaegermann, M. Campo, J.

Beier, Thin Solid Films, **431**–**432** (2003) 84–89.

[67] C. S. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D. L. Morel, Sol. Energy, **77** (2004) 823–830.

[68] A. D. Compaan, A. Gupta, S. Lee, S. Wang, J. Drayton, Sol. Energy, **77** (2004) 815–822.

[69] J. A. M. AbuShama, S. Johnston, T. Moriarty, G. Teeter, K. Ramanathan, R. Noufi, Prog. Photovoltaics Res. Appl., **12** (2004) 39–45.

[70] A. Rios-Flores, O. Ares, J. M. Camacho, V. Rejon, J. L. Pena, Sol. Energy, **86** (2012) 780–785.

[71] J. Elias, R. Tena-Zaera, C. Lévy-Clément, Thin Solid Films, **515** (2007) 8553–8557.

[72] O. K. Echendu, I. M. Dharmadasa, Energies, **8** (2015) 4416–4435.

[73] J. D. Major, K. Durose, 2013 IEEE 39th Photovolt. Spec. Conf., (2013) 1146–1149.

[74] N. Nakayama, H. Matsumoto, K. Yamaguchi, S. Ikegami, Y. Hioki, Jpn. J. Appl. Phys., **15** (1976) 2281–2282.

[75] K. Zanio, Semiconductors and Semimetals (Volume 13, Cadmium Telluride), Academic Press, New York, USA (1978).

[76] N. V. Sochinskii, M. D. Serrano, E. Dieguez, F. Agullo-Rueda, U. Pal, J. Piqueras, P. Fernandez, J. Appl. Phys., **77** (1995) 2806–2808.

[77] I. M. Dharmadasa, O. K. Echendu, F. Fauzi, N. A. Abdul-Manaf, H. I. Salim, T. Druffel, R. Dharmadasa, B. Lavery, J. Mater. Sci. Mater. Electron., **26** (2015) 4571–4583.

[78] D. G. Diso, PhD Thesis, "Research and development of CdTe based thin film PV solar cells," 2011. http://shura.shu.ac.uk/4941/.

[79] F. Bin Fauzi, PhD Thesis "Research and Development of CdS/CdTe Solar Cells Incorporating ZnTe Layers," Sheffield Hallam University, Sheffield, 2015.

[80] O. I. Olusola, M. L. Madugu, N. A. Abdul-Manaf, I. M. Dharmadasa, Curr. Appl. Phys., **16** (2016) 120–130.

Chapter 2 - Semiconductor materials, solar cell interfaces and types of solar cells

2.1 Introduction

The emphasis of this chapter is on semiconductor materials, their properties and classifications based on external dopants addition and grouping using valence electrons as seen in the periodic table. Various interfaces which exist in solar cell devices and the physics behind them are also explored. A brief study of different types of solar cells presently fabricated at large scale level and the ones currently being researched on are also discussed.

2.2 Solid materials

Solid materials can be generally grouped into three categories namely: conductors, semiconductors and insulators. Energy bands also exist in these solid materials in the form of valence band (VB) and conduction band (CB). The VB is the allowed energy band that is filled with electrons while the CB is the empty energy band. In conductors like metals, the valence band is partially filled with electrons and they overlap with the conduction band [1]. This attribute makes the electron to freely move from the VB to the CB even at zero Kelvin and without necessarily applying excitation energy either from heat or light source. Conductors generally have low electrical resistivity due to the presence of conduction electrons which contribute to the current flow. In conductors, there exists very minute or no energy gap between the VB and the CB.

The valence band of semiconductors is filled with electrons, and with thermal agitations even at room temperature [1,2] or excitation by light [3], some of these electrons can be excited to the conduction band. A small energy gap exists between the VB and CB of semiconductor materials. For an insulating material, there exists a wider energy gap between the VB and CB and this makes it difficult for electrons to be excited from the VB to CB at room temperature [1]. Thus insulators have very high resistance because most of the electrons only occupy the available states in the VB and they are not available for conduction. This therefore makes the VB to remain completely full and CB to be totally empty.

The classifications of these solid materials can also be made based on the materials resistivity and energy bandgap. The possible ranges for the resistivity and energy bandgap of these three solid materials are indicated in Table 2.1.

Table 2.1. Classification of solid materials based on their electrical resistivities and energy bandgap.

Solid materials	Electrical resistivities (Ωcm)	Energy bandgap (eV)
Metals/semi metals	$\sim 10^{-8}$-10^{-1}	≤0.30
Semiconductors	$\sim 10^{-1}$-10^{8}	~0.30-4.00
Insulators	$\sim 10^{8}$-10^{20}	≥4.00

2.3 Semiconductor materials

The range of resistivities of semiconductor materials lie in-between that of conductors and insulators as shown in Table 2.1 and these values can be modified accordingly by subjecting it to some external conditions. One of these conditions is temperature; this can be in form of annealing temperature or measurement temperature. The resistivity of most semiconductor materials decreases with increase in temperature. These materials behave in opposite way to conductors whose resistivity increases as temperature increases [3]. As explained by Sharma [3], bombarding the semiconductor materials by a beam of light also causes a rapid decrease in its resistivity. Also, the resistivity of semiconductor materials can be modified by systematically introducing very small amount of impurities known as dopants into the semiconductor. Due to the flexible nature of the semiconductor materials, they find useful application in the fabrication of solid state electronic devices.

2.3.1 Classification of semiconductor materials based on dopants addition

Semiconductor materials can be grouped into two categories based on dopants addition. The ones made without the addition of any external dopants are called intrinsic semiconductor materials while the others fabricated through the use of external impurity atoms called dopants are called extrinsic semiconductor materials.

2.3.1.1 Intrinsic and extrinsic semiconductor materials

A pure semiconductor formed without the incorporation of any external dopant elements known as impurities are referred to as intrinsic materials. The semiconductors formed by controlling the amounts of added impurity atoms are called extrinsic materials. This addition changes the electrical properties of the material. The type of external impurity atoms added will determine the electrical conductivity type and the charge carrier that will be dominant in the semiconductor; this can either be holes in the VB or electrons in the CB [1]. In addition to the above, defects are also one of the prevailing factors which determine the pinning position of the Fermi level in a semiconductor material. It should be noted that while electrons are thermally excited from the valence band to the conduction band to improve conductivity in intrinsic semiconductors, the conductivity of extrinsic semiconductors is improved with the dopants addition [4].

Taking for example silicon (Si) which is an elemental semiconductor with four valence electrons; when each of the Si atoms share its four outermost electrons with other four nearby Si atoms leading to formation of four covalent bonds, an intrinsic material is formed as shown in Figure 2.1 (a). There are no free electrons available for conduction in an intrinsic material because the atoms are tightly bonded to one another as illustrated in Figure 2.1 (a). For the intrinsic Si semiconductor material, the Fermi level is located halfway between the conduction band minimum (E_{Cmin}) and valence band maximum (E_{Vmax}) as shown in the energy band diagram of Figure 2.1 (b).

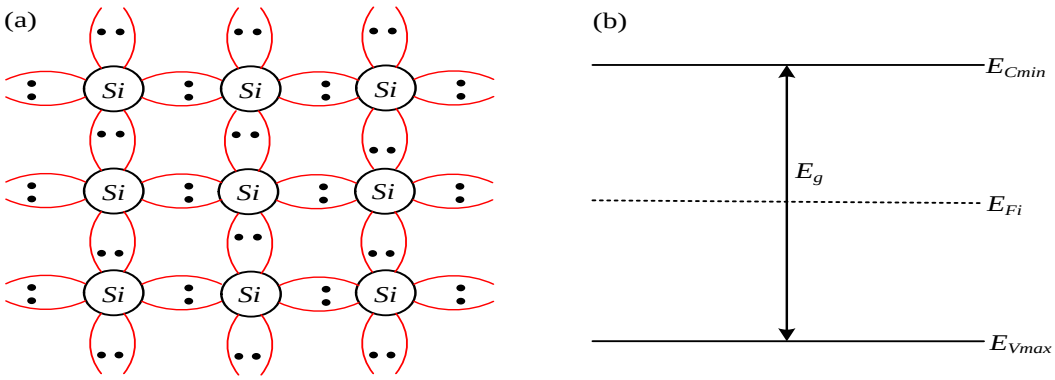


Figure 2.1. Typical diagrams illustrating (a) covalent bond formation in intrinsic silicon crystal lattice and (b) energy band diagram of an intrinsic semiconductor material with emphasis on Fermi level position.

The conduction band represents the energy levels that are not occupied by electrons while the valence band is the energy levels occupied by electrons. The energy gap between the E_{Cmin} and E_{Vmax} is referred to as the bandgap. The bandgap signifies the minimum energy (in eV) that must be overcome for electrons to be thermally excited from the VB to the CB. The valence electrons located beneath the E_{Vmax} are represented by closed circle in Figure 2.2. The opened circle below the E_{Vmax} represent the vacancies (holes) created after electrons have been excited from the VB to the CB. The closed circles above the E_{Cmin} represent the excited electrons from the VB.

If one of the valence electrons of an intrinsic semiconductor material receives adequate energy as shown in Figure 2.2 (a), for instance, by bombarding it with light; it can be released from the covalent bond and migrate inside the crystal. This loose electron can then add to the electrical current flow through the material when an electric field is applied. A continuous bombardment of the semiconductor with more light gives rise to excitation of more electrons from the VB to the CB. The more the free electrons available for conduction, the greater will be the magnitude of electrical current generated provided the conduction electrons and holes recombine at the external circuit and not within the semiconductor. If all the electrons in the valence band of an intrinsic material are now excited as illustrated in Figure 2.2 (b), the total number of electrons excited into the CB will leave an equal number of holes in the VB thereby making the concentration of holes in the VB (p) to be equal to the concentration of electrons (n) in the CB. This means $n = p = n_i$, where n_i is the intrinsic carrier concentration [2].

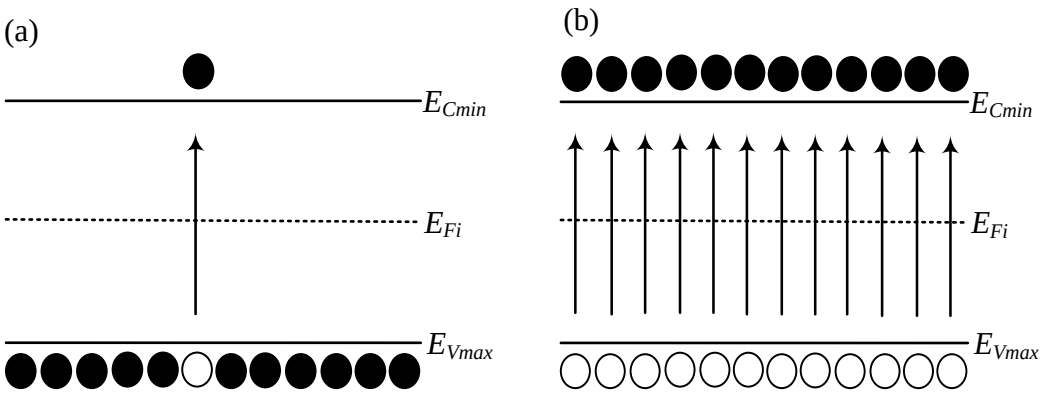


Figure 2.2. Typical energy band diagrams of an intrinsic semiconductor material illustrating the excitation of (a) one electron and (b) all electrons from valence band to conduction band after bombardment of the atoms with light.

The addition of external impurity atoms to the intrinsic material is known as doping. If the intrinsic Si material is doped with pentavalent atoms such as antimony (Sb) as shown in Figure 2.3 (a), four out of the five valence electrons in the Sb atoms are involved in forming covalent bonds with the four neighbouring Si atoms. The remaining one negatively-charged electron which does not take part in covalent bond formation becomes free and available for conduction; this conduction electron is now donated to the lattice and available for electrical conduction [2]. The antimony atom is therefore called a donor atom due to its ability to donate a free electron for conduction. The introduction of donor atoms (impurities) into the Si material changes its properties to an extrinsic material. Therefore, this type of extrinsic material is n-type in electrical conduction. The Fermi level for n-type materials is positioned towards the E_{Cmin} as shown in Figure 2.3 (b). Other pentavalent atoms which can act as donor atoms to Si are nitrogen (N), phosphorus (P) and arsenic (As).

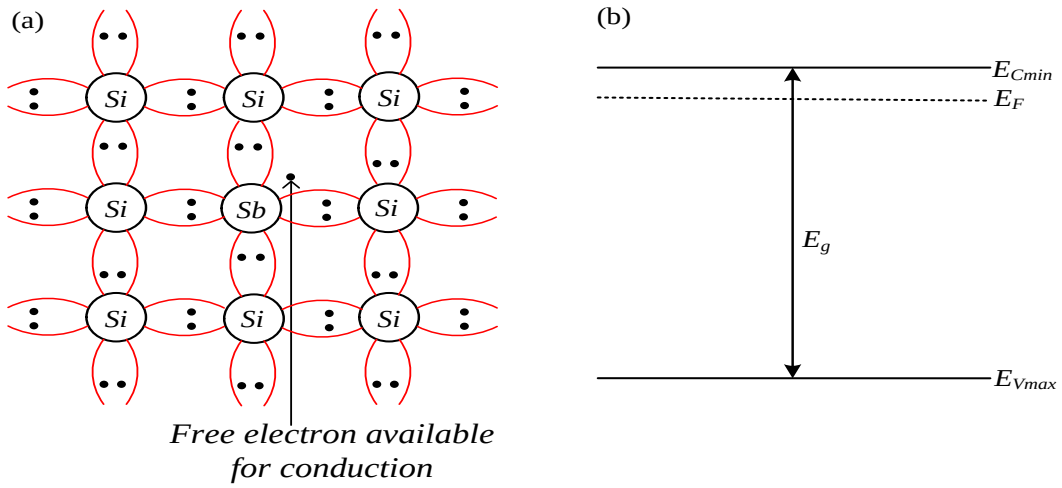


Figure 2.3. Typical diagrams illustrating (a) covalent bond formation between silicon (Si) and antimony (Sb) atoms, and (b) energy band diagram of n-type semiconductor material with emphasis on Fermi level position.

On the other hand, doping the intrinsic Si material with trivalent atoms such as gallium (Ga) creates a vacancy which needs to be filled up with an extra electron as illustrated in Figure 2.4 (a). Thus additional one electron is needed from an external atom to complete the covalent bond formation. This feature makes Ga and other trivalent atoms such as boron (B), aluminium (Al) and indium (In) to become an acceptor atom to Si. This type of extrinsic material is p-type in electrical conduction. The Fermi level position for p-type material is located towards the E_{Vmax} as shown in Figure 2.4 (b).

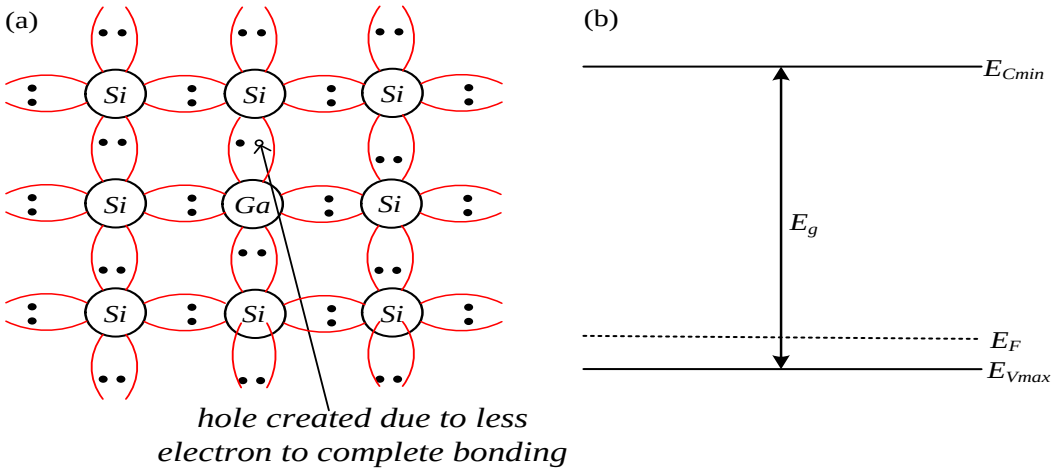


Figure 2.4. Typical diagrams illustrating (a) covalent bond formation between silicon (Si) and gallium (Ga) atoms, and (b) energy band diagram of p-type semiconductor material with emphasis on Fermi level position.

2.3.2 Classification of semiconductor materials based on elemental composition

It is imperative to fabricate the right semiconductor materials that can be used for solar-to-electric energy conversion. The development of these materials can be achieved by selecting the right elements that can be used for this purpose from the periodic table. Based on the elements that constitute semiconductor materials, they be can classified as elemental, binary, ternary and quaternary compound semiconductors. The elements used in the production of these semiconductor materials can be obtained from group I to group VII of the periodic table [5]. Elemental semiconductors are crystals formed by single element materials. Common examples of elemental semiconductors are obtained from group IV of the periodic table and these include: carbon (C), silicon (Si) and germanium (Ge). Binary compound semiconductors are formed from the chemical reactions which take place between two elements. Binary compound semiconductors can be further classified as II-VI and III-V depending on the group of the element in the periodic table. For example, the chemical reactions between one element such as Cd from group II and another element such as Te from group VI produce II-VI semiconductor known as cadmium telluride (CdTe). Likewise, the chemical reactions between gallium elements from group III and arsenic from group V produce III-V semiconductor known as gallium arsenide (GaAs). Other examples of II-VI and III-V binary compound semiconductors can be found in Table 2.2. The productions of ternary and quaternary compound semiconductors take place when three and four elements chemically react with one another respectively. Table 2.2 also shows some common

examples of these types of semiconductors. The semiconductor materials used in this research work belong to the II-VI and ternary compound family.

Table 2.2. A brief summary of semiconductor groups based on elemental composition.

Semiconductor group	Common examples of semiconductors
Elemental semiconductor from group IV	C, Si, Ge
II-VI binary compound semiconductors	CdSe, CdS, CdTe, ZnTe, ZnS, ZnO,
III-V binary compound semiconductors	GaAs, GaP, GaN, InAs, InP, AlAs, AlP
Ternary compound semiconductors	$Cd_xMn_{(1-x)}Te$, $Cd_xHg_{(1-x)}Te$, $Al_xGa_{(1-x)}As$
Quaternary compound semiconductors	$Cu_2ZnSnSe$, $CuInGaSe_2$ (CIGS)

2.4 Types of junctions/interfaces in solar cell devices

In electronic devices such as solar cells, junctions are created when two or more semiconductor materials are brought together in such a way that there is an intimate contact between them. This interface is essential because it determines the electric field strength and how the charge carriers created within the semiconductor materials are effectively separated and transferred to the external circuit for current generation. The formation of this interface can also happen if a direct contact is made between the semiconductor and metal or insulator. This section will be focused on the different interfaces that exist in electronic devices, especially in solar cells.

2.4.1 Homo-junction and Hetero-junction

In forming hetero-junction device structures, two different semiconductor materials having different energy bandgaps are joined together. The interface formed between the two different materials is referred to as hetero-junction interface. A good example of hetero-junction interface is when a p-CdTe thin film is deposited on n-CdS layer [6,7]. One of the advantages of using two or more different semiconductors in the device structure is the absorption of different regions of the solar spectrum. In homo-junction device structures, two similar materials are joined together and homo-junction interface is formed between them. A typical example of homo-junction interface is when a p-type Si layer is formed on an n-type Si wafer [8]. In both cases, materials with same or different electrical conductivity types may be used. For instance, the hetero-junction and homo-junction interface may be p-n, p-i-n, p-p and n-n interface. Also, the interface at

the hetero-junction and homo-junction structures can also be one-sided by varying the doping concentration of any of the semiconductor partners forming the interface [1].

2.4.2 p-n junction

The theory of p-n junction form the basic foundation to understand the principle of operation of semiconductor devices [2]. A p-n junction device is a 2-terminal device formed when an n-type semiconductor comes into intimate contact with a p-type semiconductor. As shown in Figure 2.5 (a), diffusion of holes from the p-type material to the n-type material and electron diffusion from the n-type to p-type material take place simultaneously due to the difference in holes and electrons concentrations between the two semiconductors [9]. The diffusion of electrons from the n-side to the p-side leads to creation of negatively charged ions at the p region. In a similar way, the diffusion of holes from p-side to n-side leads to creation of positively charged ions at the n-region of the semiconductor. The creations of positive and negative charge ions which are opposite to each other produce an electric field at the p-n interface. As these positive and negative ions build up on n- and p-sides respectively as illustrated in Figure 2.5 (b), they form a barrier which prevents further diffusion of holes and electrons from p- and n- materials respectively. The created barrier is what forms the p-n interface.

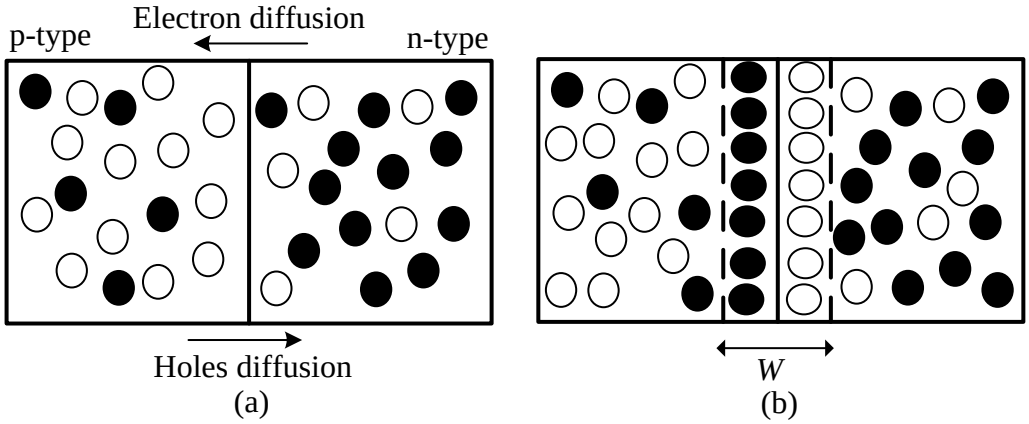


Figure 2.5. Typical schematic diagrams illustrating (a) electrons and holes diffusion and (b) the formation of barrier which prevents further diffusion of holes and electrons. The region between the created barriers is the depletion region with width, *W*.

The region between the built-up positive and negative ions is called the space-charge or depletion region (*W)* as indicated in Figure 2.5 (b). The name depletion region arises from the fact that the region is depleted of both electrons and holes. The electric field

produced within this region prevents the holes and electrons from further diffusion [9]. The energy band diagram of a typical p-n junction device is described in Figure 2.6. The depletion width (*W*) here represents the region where the band bending takes place. X_p and X_n are the distances by which the depletion region extends into p- and n-type semiconductors respectively. Homogeneous p-n junction will be produced if one material is used in fabricating the p- and n- layers while heterogeneous p-n junction will be produced if different semiconductor materials are used in fabricating the p- and n-layers.

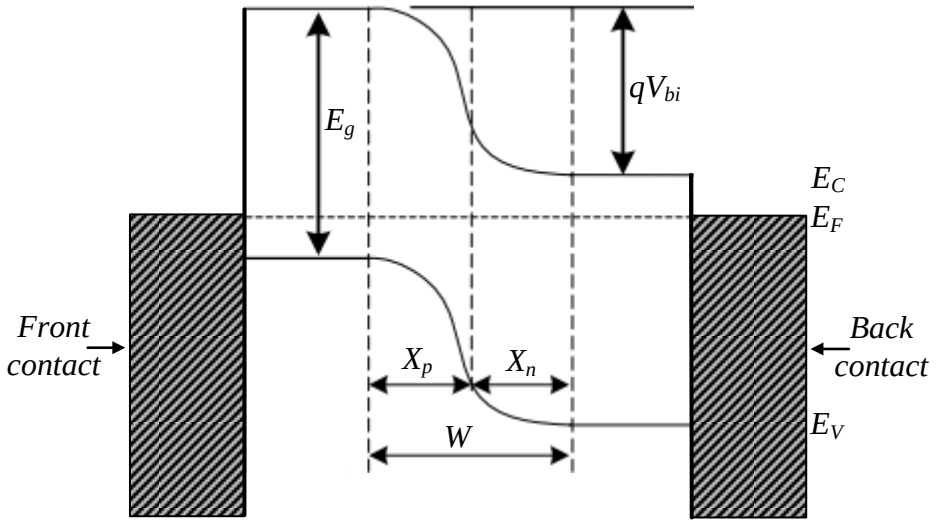


Figure 2.6. Energy band diagram of a typical p-n junction device structure. Note that the band bending between the p- and n-semiconductor material is the depletion region, $W=X_p+X_n$.

2.4.3 One-sided p-n junction

One-sided p-n junction may be fabricated by heavily doping one layer and moderately doping the other hetero-junction or homo-junction partner. Kabra et al. [10] demonstrated the fabrication of one-sided rectifying n^+p junction diode fabricated from n-Si and p-ZnO heterogeneous materials. Several articles in the literature have reported investigations relating to abrupt junctions [1,2,11,12]. Examples of hetero-junction and homo-junction one-sided interface are n^+p, p^+n, n^+n and p^+p. Figure 2.7 (a) illustrates the energy band diagram of a diode with one-sided abrupt n^+p junction fabricated from n-CdS and p-ZnTe semiconductors while Figure 2.7 (b) shows the energy band diagram of abrupt n^+p junction diode fabricated from n-ZnTe and p-ZnTe materials.

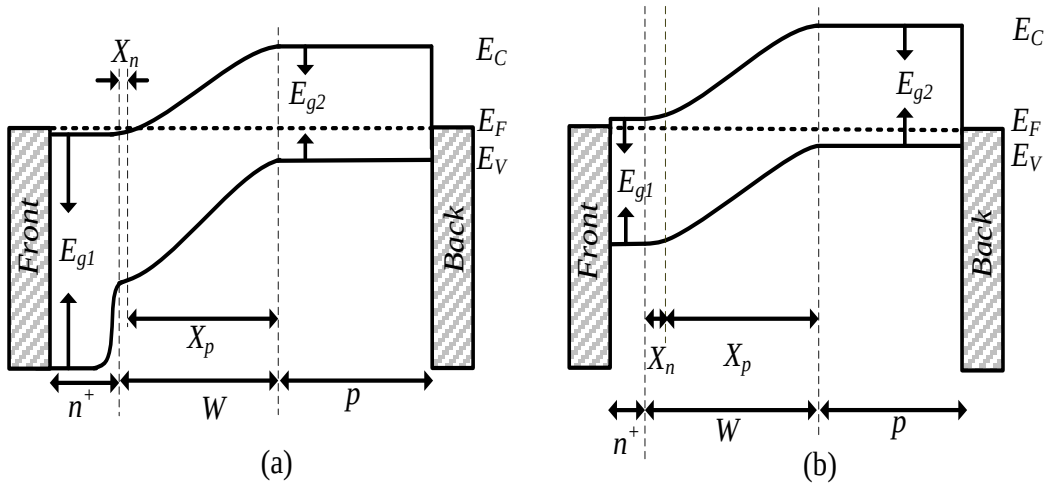


Figure 2.7. Energy band diagrams of abrupt p-n junction (a) one-sided n^+p hetero-junction diode fabricated from n-CdS and p-ZnTe semiconductors and (b) one-sided n^+p homo-junction diode fabricated from n-ZnTe and p-ZnTe semiconductors.

2.4.4 p-i-n interface

p-i-n junction is produced when an insulating or intrinsic semiconductor thin film is inserted between a p- and n- semiconductor material. In practical situations, it is difficult to fabricate i-type layer; however p- and n-semiconductor materials with high resistivity can serve the purpose of i-layer sandwiched between the p and n semiconductors. The principle of operation of p-i-n interface is similar to that of p-n junction. Figure 2.8 shows the energy band diagram of a p-i-n device structure. The Fermi levels of the p- and n- layers are aligned through the i-layer to produce a strong and healthy electric field throughout the intrinsic material [5]. The main merit of having this type of structure is its ability to produce a high potential barrier (ϕ_b) which approaches the energy bandgap of the semiconductor materials used in the p-i-n structure [5]. With high ϕ_b, the probability of obtaining a large open circuit voltage (V_{oc}) is possible. Meyers [13] successfully demonstrated the fabrication of this n-i-p junction in solar cell fabrication by using n-CdS, i-CdTe and p-ZnTe layers.

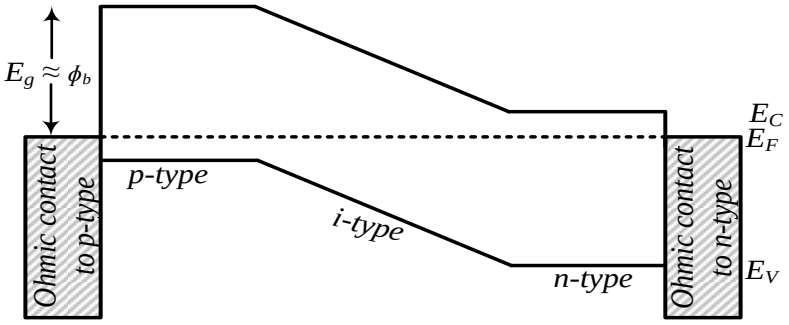


Figure 2.8. Energy band diagram of p-i-n diode illustrating the possibility of obtaining high potential barrier height (ϕ_b) almost equal to the semiconductor bandgap (E_g).

2.4.5 n-n and p-p interfaces

The fabrication of n-n and p-p hetero-junctions fabricated from Ge/Si was reported by Oldham [14]. Figures 2.9 (a) and 2.9 (b) demonstrate typical energy band diagrams of n-n and p-p semiconductors fabricated from two different materials of same thicknesses respectively while Figures 2.10 (a) and 2.10 (b) illustrate typical energy band diagrams of n-n and p-p semiconductors fabricated from same semiconductor materials having equal thicknesses respectively. Two or more n-n interfaces can be combined together to produce multi-junction graded bandgap solar cells as discussed in Section 9.14.

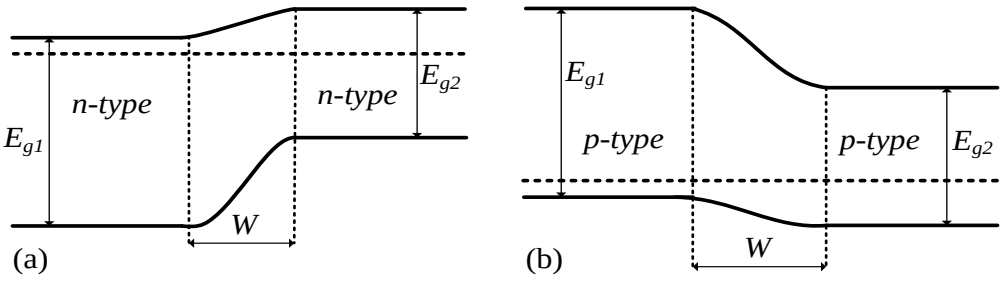


Figure 2.9. Typical energy band diagrams of (a) n-n and (b) p-p hetero-junctions.

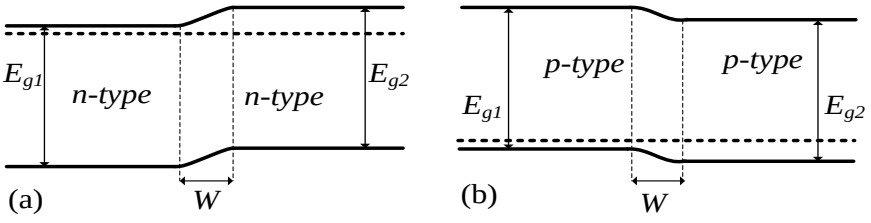


Figure 2.10. Typical energy band diagrams of (a) n-n and (b) p-p homo-junctions.

2.4.6 Metal-Semiconductor (MS) interface

The MS interface is formed when a metal and a semiconductor are brought into direct contact with each other. One of the usefulness of the MS interface is the formation of electrical contacts which are used to collect the photo-generated charge carriers and transport them through an external circuit [5]. Two MS interfaces namely ohmic and rectifying contacts are needed in an electronic device most especially, in a solar cell depending on their design.

2.4.6.1 Ohmic contacts formation

Ohmic contact is a non-rectifying interface with linear current-voltage (I-V) characteristics behaving according to Ohms law. There are two ways of making ohmic contacts to the semiconductor material. The first method involves the formation of no potential barrier between the semiconductor and the metal while in the second method, a barrier formation can take place. In the first method, a metal with a lower (or higher) work function (ϕ_m)than the electron affinity $(\chi_s)$of n-type (or p-type) semiconductor is being used. In this situation, there would be no formation of built-in potential barrier height, ϕ_b (that is, $V_{bi} \leq 0$ V) and this would enable current to easily flow between the metal and the semiconductor.

For instance, when an ohmic contact is made between a n-type semiconductor and metal ($\phi_m < \phi_{ns}$) as shown in Figure 2.11, an alignment of Fermi level takes place at equilibrium by the transfer of electrons from the metal to n-type semiconductor [15].

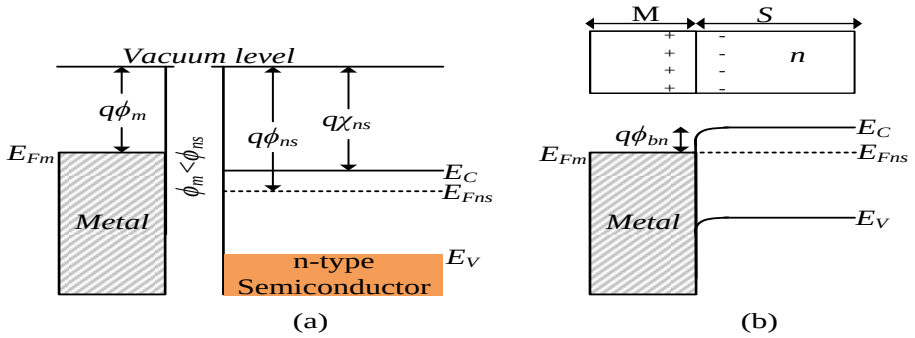


Figure 2.11. Energy band diagrams illustrating the ohmic contact formation between metal and n-type semiconductor (a) before joining the metal and semiconductor and (b) at equilibrium position after making contact. Note that ϕ_{ns} is the work function of the n-type semiconductor while χ_{ns} is the electron affinity of the n-type semiconductor.

Figures 2.11 (a) and 2.11(b) show the energy levels before and after making metal contacts to the n-type material respectively. This transfer makes the surface of the n-semiconductor to become more n in electrical conduction [1] and this lifts up the electron energies of the semiconductor relative to the metal at thermal equilibrium [15]. If the M/S interface is forward biased, electrons flowing from the semiconductor to the metal do not encounter barrier. Likewise, if the M/S interface is reverse biased, a small barrier height of $\phi_{bn} = E_C - E_{Fns}$ exists for electrons flowing from the metal into the semiconductor. Since the created barrier is small under the reverse bias condition, electrons can still flow through from the metal into the semiconductor.

The energy level before making ohmic contact for p-type material $(\phi_m > \phi_{ps})$ is illustrated in Figure 2.12 (a). After contact making (Figure 2.12 (b)), electrons flow from the conduction band of the p-semiconductor into the metal so as to attain thermal equilibrium and this produces more holes in the semiconductor. The large densities of holes at the surface therefore make the semiconductor surface to be more p in electrical conduction. When forward biased, holes produced in the p-type semiconductor can easily tunnel through into the metal from the semiconductor. Since no depletion region is formed in the M/S interface when $\phi_m > \phi_{ps}$, the movement of holes can take place from semiconductor to metal and vice versa. The above description is for ideal case when there are no surface states at the M/S interface. This ideal situation was also observed when making ohmic contacts on p-CdTe as described in Section 8.5.5.

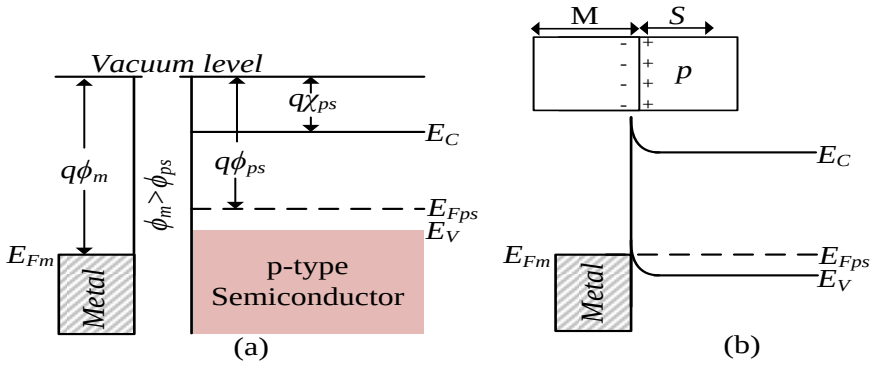


Figure 2.12. Energy band diagrams illustrating the ohmic contact formation between metal and p-type semiconductor (a) before joining the metal and semiconductor and (b) at equilibrium position after making contact. Note that ϕ_{ps} is the work function of the p-type semiconductor while χ_{ps} is the electron affinity of the p-type semiconductor.

However in practical situations, the presence of surface states at the semiconductor can cause Fermi level pinning to take place thereby making V_{bi} >0 V and independent of the metal work function. When this happens, the ohmic response becomes non-linear in one or both bias regions.

The second alternative method is to heavily dope the semiconductor that is directly adjacent to the metal [15]. In this type of situation even if a potential barrier is created as a result of the metal being used {for example, using a metal of higher (or lower) work function to the n-type (or p-type) semiconductor}, the heavy doping creates a very narrow depletion width. With this narrow width, tunnelling becomes the main means of transporting current across the Schottky barrier and this allows flow of current in both directions with linear response to the applied bias [16]. A practical example of this was also observed in the degenerate n-CdS thin film described in Chapter 7.

2.4.6.2 Rectifying contacts formation

The formation of rectifying contacts also known as Schottky contacts occur when a metal with higher work function, ϕ_m is brought into intimate contact with n-type semiconductor materials having a lower work function, ϕ_{ns}. To form rectifying contacts on p-type semiconductor, metal with lower work function is coated on p-type semiconductor materials having higher work function, ϕ_{ps}. In both cases of n- and p-type, charge transfer takes place until there is an alignment of Fermi level at equilibrium [15].

In n-type material where, $\phi_m > \phi_{ns}$; the Fermi level of the semiconductor is higher than the Fermi level of the metal before evaporating the metal contact on the semiconductor as shown in Figure 2.13 (a). This means that the electron energy of the semiconductor is higher. To equalise the two Fermi levels, the electron energy of the semiconductor must be lowered relative to the metal [15]. To achieve this, electrons have to flow from the CB of the semiconductor to the metal. Figure 2.13 (b) illustrates the energy band diagram after the FL of both semiconductor and metal have been aligned.

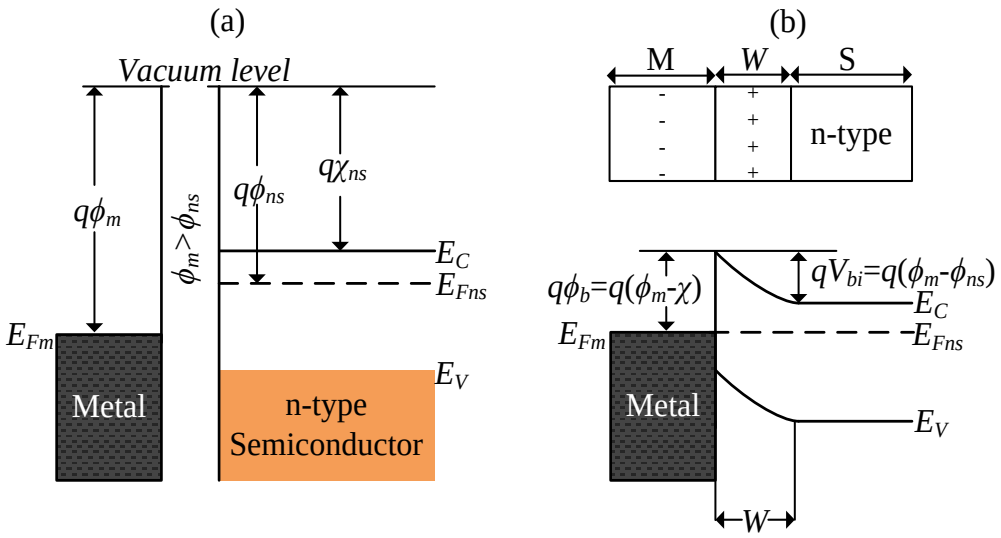


Figure 2.13. Energy band diagrams illustrating the Schottky contact formation between metal and n-type semiconductor (a) before joining the metal and semiconductor and (b) at equilibrium position after making contact.

The flow of electrons from the semiconductor to the metal leads to a decrease in the electron concentration. This decrease lowers the Fermi level and bends the edge of the conduction band near the interface up. The flow of electrons to the metal will induce a negative charge on the metal and a positive charge of ionised donors on the semiconductor near the interface. For this cause, the region of semiconductor near the metal interface where band bending takes place becomes depleted of mobile electrons. The presence of negative charges at the surface of the metal and positive charges at the semiconductor region near the metal interface create an electric field at the interface. The built-in potential in eV (qV_{bi}) which prevents further diffusion of electrons from conduction band of n-semiconductor to metal is given as,

$$qV_{bi} = q(\phi_m - \phi_{ns}) \tag{2.1}$$

The potential barrier height ($q\phi_b$) which prevents electron in metal from diffusing into the semiconductor conduction band is

$$q\phi_b = q(\phi_m - \chi) \tag{2.2}$$

Where $q\chi$ is the electron affinity of the semiconductor measured from the vacuum level to the conduction band edge of the semiconductor.

The Schottky barrier formation on p-type material where $\phi_m < \phi_{ps}$ is shown in Figure 2.14. The energy band diagrams before and after metal coating on the p-type semiconductor are summarised in Figures 2.14 (a) and 2.14 (b) respectively.

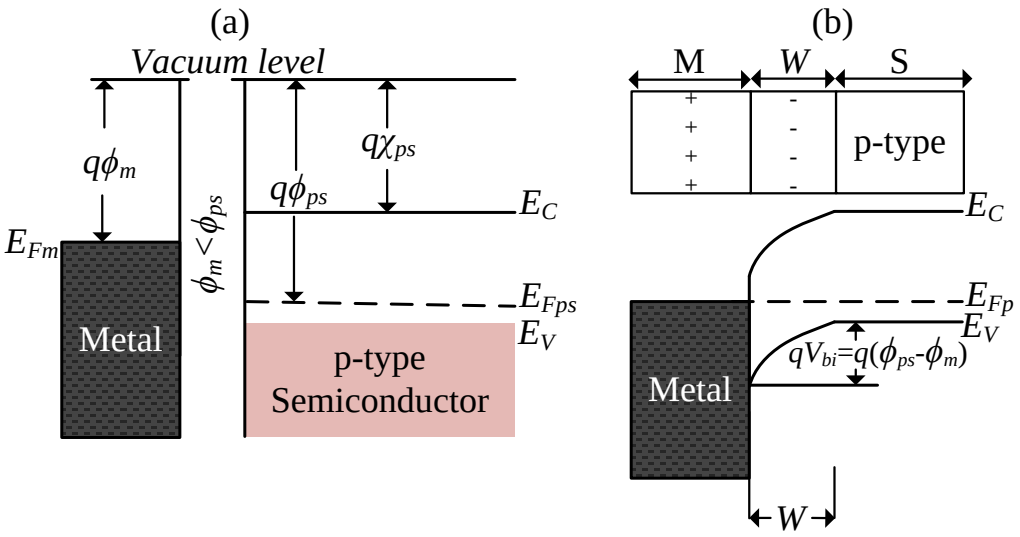


Figure 2.14. Energy band diagrams illustrating the Schottky contact formation between metal and p-type semiconductor (a) before joining the metal and semiconductor and (b) at equilibrium position after making contact.

The above descriptions are applicable for Schottky diodes that are free of surface and interface states. Equation (2.1) is therefore valid for ideal Schottky diodes. In practical applications, the Schottky diodes do not obey this ideal equation due to presence of defects at the surface/interface. This is why potential barrier is most of the times not dependent on the metal work function. In the ideal case, band bending takes place when metal contact is made on the semiconductor but in practical applications, it is possible to have band bending prior to metallisation. This band bending can be explained in terms of surface states which may arise from formation of thin layer of oxide films or dangling bonds at the semiconductor surface [16]. The surface states can be donor states which release an electron to become positive; this donor state pins the Fermi level close to the conduction band. It can also be acceptor states which obtain an electron to become negative and pins Fermi level close to valence band. Mostly, the dangling bonds which arise from incomplete bonding [15] always dominate and for an n-type semiconductor material, the surface will attain positive charge; this makes the band to bend upwards near the semiconductor surface before metallisation.

As explained by Streetman and Banerjee [15], surface states are common in compound semiconductors due to the presence of interfacial layer. The effect of these states are mostly felt when two different compound semiconductors are grown on each other. Due to the lattice mismatch between the two compound semiconductor materials at the interface, defects also known as surface states may be introduced. The introduction of these defects if not properly controlled may bring about a poor performance in solar cell efficiency since they actively determine the position at which the Fermi level pins. Details of these defects as described by Dharmadasa et al. [17] have been discussed in Section 1.6.3. Thus, the interfacial layer introduces defect states into the energy bandgap of semiconductor which pins the Fermi level at a particular position [15]. For instance, a group of interface states sited at ~0.35 eV below the conduction band minimum of n-CdTe will pin the FL at the surface of n-CdTe and the potential barrier height of the Schottky will depend on the surface states pinning effect instead of the metal work function.

In this situation, the Schottky potential barrier becomes:

$$q\phi_b = E_g - q\phi_o \tag{2.3}$$

E_g is the bandgap of the semiconductor and $q\phi_o$ (shown in Figure 2.15) is a neutral level which exists between the surface Fermi level and the surface valence band energy.

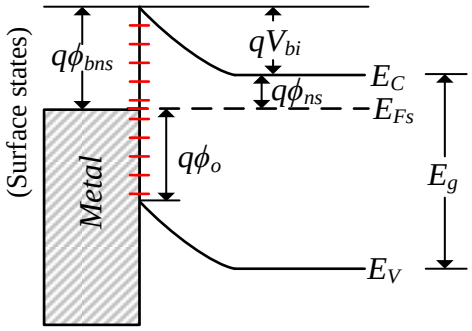


Figure 2.15. Energy band diagram of Schottky interface with surface states. The surface states denoted by red lines at the M/S interface helps in pinning the FL at the M/S interface giving rise to a Schottky barrier.

From Equations (2.2) and (2.3), it can be deduced that ϕ_b of the M/S interface can be determined using the work function of the metal and interface or surface states present at the semiconductor bandgap [1]. In the same way, the V_{bi} solely depends on the

semiconductor properties and not on metal work function when there is presence of interface states. From Figure 2.15, the following equations can be deduced for n-type semiconductors.

$$q\phi_{bns} = qV_{bi} + q\phi_{ns} \tag{2.4}$$

$$q\phi_{bns} = E_g - q\phi_o \tag{2.5}$$

where $q\phi_{ns} = E_C - E_{Fs}$ (2.6)

$$E_g = E_C - E_V \tag{2.7}$$

Putting Equations (2.5), (2.6) and (2.7) into Equation (2.4)

$$qV_{bi} = E_C - E_V - q\phi_o - (E_C - E_{Fs}) \tag{2.8}$$

$$qV_{bi} = E_{Fs} - (E_V + q\phi_o) \tag{2.9}$$

Equation (2.9) shows that qV_{bi} equally depends on the semiconductor properties and independent on metal work function.

2.4.6.3 Current transport mechanisms in Schottky diodes

As explained by Dharmadasa et al. [17], when a solar cell is exposed to sunlight, it is synonymous to forward biasing while solar cells being kept in the dark are equivalent to zero biasing of the diode. For this reason, the direction of electron flow under dark and light conditions differs and they are illustrated in Figure 2.16. In the same way, when a metal/semiconductor junction is reverse biased, the flow of electrons differs from when it is forward biased. The various current transport mechanisms that take place in metal-semiconductor contact when forward biased under dark are highlighted below and described diagrammatically in Figure 2.16 (a) [11,18]. Figure 2.16 (b) also describes the direction of electron flow when M/S junction is forward biased under illumination. Brief details of some of the current transport mechanisms are discussed in Chapter 3.

(i) Thermionic emission of electrons (majority carrier) from the semiconductor over the barrier into the metal contact.

(ii) Electron tunnelling from the semiconductor into the metal through the barrier.

(iii) Recombination of electrons and holes within the depletion region.

(iv) Thermionic emission of holes (minority carrier) from the metal into the semiconductor.

Transport mechanism (i) is dominant for Schottky diodes with moderately doped semiconductor while transport mechanism (ii) is dominant for M/S interface with an heavily doped semiconductor [11]. The basic processes (i-iv) discussed above for current transport mechanism equally holds for metal to semiconductor current flow when reverse biased under dark condition.

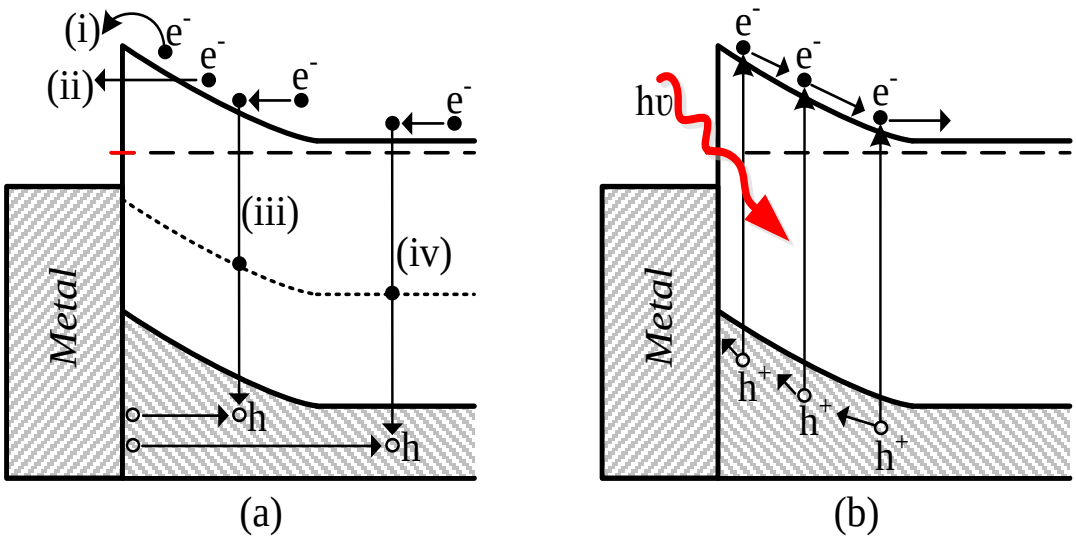


Figure 2.16. (a) Basic current transport mechanisms for flow of electrons in metal-semiconductor junction when forward biased under dark condition. (b) Direction of electron flow when the Schottky junction is illuminated with light. Note that this is the same direction in which electrons also flow when reverse biased under dark condition.

2.4.7 Metal-insulator-semiconductor interfaces

The potential barrier height (ϕ_b) obtained at p-n interface is larger than those of M/S interface. Therefore, the built-in potential (V_{bi}) and open-circuit voltage (V_{oc}) are higher in p-n junction than in M/S junction. One way of increasing the ϕ_b to values close to the energy bandgap value is by incorporating a thin, insulating layer of ~10 nm at the semiconductor surface before depositing the metal contact [2]. Figure 2.17 (a) shows the formation of ϕ_b at the interface between metal and semiconductor. The insertion of the insulating layer (*I*-layer) between the metal contact and semiconductor give rise to metal-insulator-semiconductor (MIS) structure as shown in Figure 2.17 (b). The *I*-layer can be intentionally introduced by growing a very thin insulating layer. Organic

materials can be deposited as *I*-layer between the metal and semiconductor to form MIS structure. This was demonstrated by Mabrook et al. [19] when the authors used organic thin films as insulating layers to fabricate MIS organic memory devices. The *I*-layer can also be obtained by oxidising the top surface of the semiconductor layer [20]. The presence of the *I*-layer between the metal and the semiconductor eliminate interaction at the interface thus leading to removal of ageing effects at the back metal contact [5]. This phenomenon guarantees an increase in the lifetime of the solar cell structure. Another advantage of the MIS structure is the extension of electric field into the semiconductor surface as a result of band bending increase which occurs at the MIS interface [2,5]. The incorporation of a thin insulating layer between the metal and semiconductor have been used in enhancing the illuminating characteristics of metal contacts to semiconductors like GaP and CdS [21].

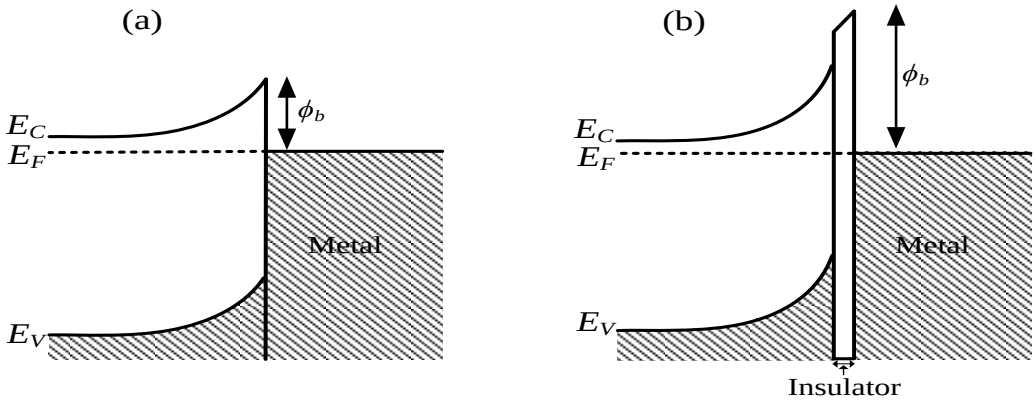


Figure 2.17. Typical energy band diagrams of n-type semiconductor illustrating (a) the formation of potential barrier height at metal/semiconductor (MS) interface and (b) the improvement of the potential barrier height as a result of insertion of an insulating layer (I-layer) in-between the metal and semiconductor.

2.5 Types of solar cells

Solar cells can be made from organic materials (for example polymer) or inorganic materials (for example, Si, GaAs, CdTe, CZTS). Solar cells fabricated from organic materials are called organic solar cells while the ones produced from inorganic materials are called inorganic solar cells. When both organic and inorganic materials are used in solar cell production, the result is a hybrid solar cell. A good example of hybrid solar cell is perovskite. The focus of this section will be on some solar cells that are presently

in use on a large scale basis and the ones that are currently being researched into for future industrial commercialisation.

2.5.1 Inorganic solar cells

Inorganic solar cells (IOSCs) are classes of PV devices which make use of inorganic materials to absorb photons which break bonds between atoms and create electron-hole pairs that are useful for electricity generation. Examples of inorganic solar cells are Si-based solar cells, III-V based solar cells such as GaAs and chalcogenide-based solar cells. Chalcogenide-based solar cells are solar cells which contain a minimum of one group VI element. Group VI elements are called chalcogens and they are: oxygen (O), sulphur (S), selenium (Se) and tellurium (Te). Examples of these solar cells are copper indium diselenide (CIS), copper indium gallium diselenide (CIGS), copper zinc tin sulphide (CZTS) and cadmium telluride (CdTe). The research presented in this thesis is focused on inorganic solar cells primarily CdTe-based solar cells. A brief history of CdTe-based solar cells was given in Chapter 1.

2.5.2 Organic solar cells

Organic solar cell (OSC) is a group of photovoltaic device which uses organic molecules to absorb photons and transport charge to produce electric current using the photovoltaic principle. Kearns and Calvin [22] first observed the PV behaviour of organic compounds in the 1950s. A good example of OSC is polymer based solar cells. Based on types of junctions available in organic solar cells (OSCs), they can be categorised as single layer, bilayer, discrete heterojunction, bulk heterojunction, graded heterojunction and continuous junction. The simplest form of OSC is the single layer and they are fabricated by sandwiching a layer of organic materials in-between two different electrodes [23]. The metallic conductors used for the electrodes are ITO which serves as the anode and Al or Mg which serves as the cathode. For the bilayer OSC, two layers namely electron acceptor and electron donor are sandwiched between the two different conducting electrodes. Examples of donor and acceptor materials are poly (2-methoxy-(5- ethylhexyloxy)-1,4-phenylene-vinylene) (MEH-PPV) and Phenyl-C61-butyric acid methyl ester (PCBM) respectively. The schematic diagrams showing the basic structure of a single layer and bilayer OSC are shown in Figures 2.18 (a) and 2.18 (b) respectively.

The OSC differ from inorganic solar cell in some regards. For instance in OSC, the electric field is created as a result of the differences in the work function between the two electrodes while in inorganic solar cells for example a p-n junction solar cell, the electric field is created as a result of the barrier created between the diffused holes and electrons at the interface. The terms valence and conduction bands used in inorganic electronics are referred to as HOMO (highest occupied molecular orbital) and LUMO (lowest unoccupied molecular orbital) respectively in organic electronics [24]. The bandgap is the energy separation between the HOMO and LUMO energy levels. OSCs are cost effective when used in PV applications, their main demerits lie in low stability and efficiency when compared to inorganic PV cells.

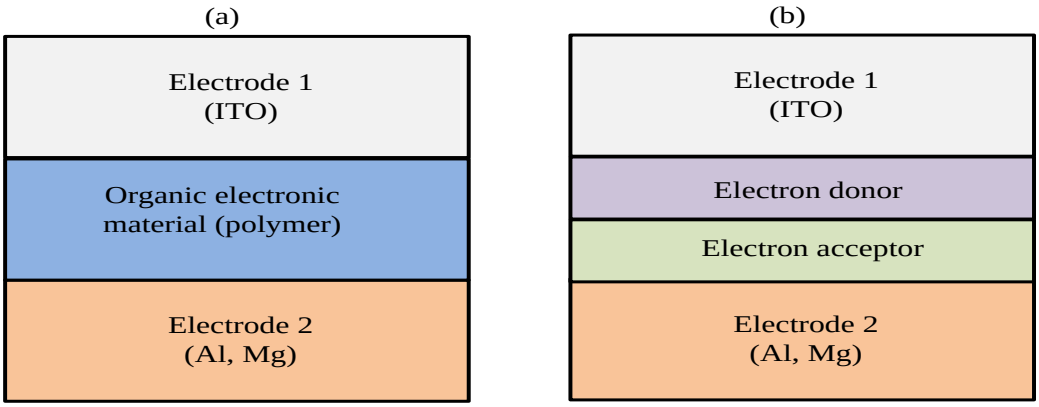


Figure 2.18. Schematic diagrams of organic solar cell (a) single layer organic solar cell and (b) bilayer organic solar cell.

2.5.3 Hybrid solar cell (Perovskite solar cell)

A perovskite solar cell is a hybrid solar cell fabricated from organic-inorganic halide-based material. This solar cell derives its name from the Russian mineralogist known as L.A. Perovski. The perovskite technology originates from the solid state dye sensitised solar cell (ssDSSC) [25]. Both ssDSSC and perovskite have the same device structure, the main difference is in the light absorber layer. In ssDSSC, the light absorber is photoactive mesoporous oxide with coated dye molecules (TiO_2 and dye) while in perovskite, the light absorber layer is perovskite. With the incorporation of a new light absorber material in the solid state sensitised solar cell, the power conversion efficiency (PCE) has increased from 11.9% in ssDSSC to 22.1% in perovskite-based solar cell [26]. The schematic diagrams of ssDSSC and perovskite are illustrated in Figures 2.19 (a) and 2.19 (b) respectively.

The perovskite solar cells are processed from solution and they have crystal structure of the form ABX_3 where A and B are larger and smaller cations respectively [27]. The larger cation is an organic-based material while the smaller cations are inorganic-based materials such as tin (Sn) and lead (Pb). X is the anion mainly from oxygen, nitrogen, carbon, or halogens [25]. An example of absorber material used in perovskite is methylammonium lead trihalide ($CH_3NH_3PbX_3$) where A is (CH_3NH_3), B is Pb and X is halogen such as Cl or Br atom. The contents of halides used determine the optical bandgap and this value can range between 1.50 and 2.30 eV.

Perovskites have the advantage of very low cost of production and rapid improvements have been seen in the solar cell efficiency of perovskites from 2009, to date [28]; the world record efficiency of this solar cell as reported by researchers from KRICT/UNIST group in South Korea is 22.1% [26,29]. The current issue that needs to be addressed with the perovskite technology is the instability of the device fabricated from perovskites at high relative humidity. It is highly believed that once the instability issue is resolved, the material has the potential of being commercialised on a large scale production for PV application.

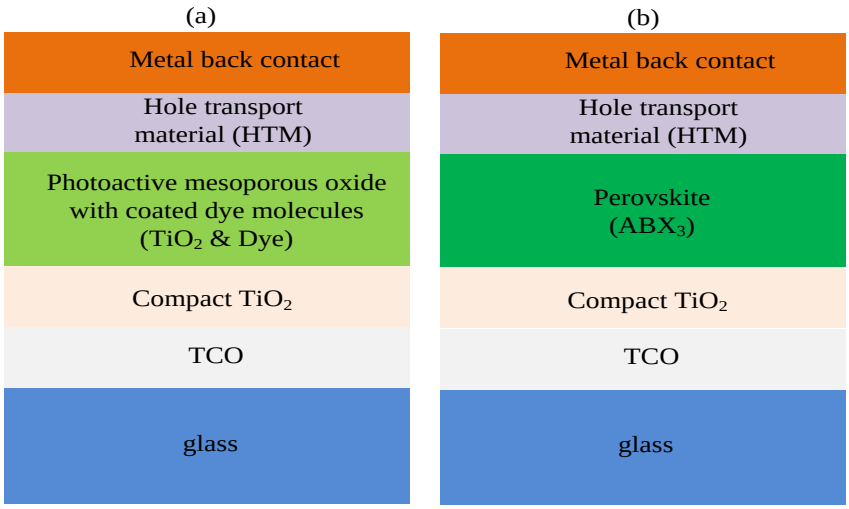


Figure 2.19. Schematic diagrams of (a) solid state dye sensitised solar cell (ssDSSC) and (b) perovskite-based solar cell.

2.5.4 Multi-junction graded bandgap solar cells

The use of multi-junction graded bandgap (MJGB) device structures for solar cell application is important in harvesting photons from various parts of the solar spectrum. Some of the experimental works reported on solar cell device structures in Chapter 9 of

this thesis are based on this type of device structure. These device structures are made up of different semiconductors having various energy bandgaps and arranged in a way that photons from different parts of the spectrum can be effectively absorbed to enhance the output short-circuit current density. The full MJGB solar cell structure was proposed by Dharmadasa et al. [30] in 2005 and it was experimentally tested with GaAs/AlGaAs using MOVPE growth technique and the obtained results showed a working model [31]. One of the focuses of this present research work is to develop the MJGB structures using low-cost electroplated semiconductors most especially from II-VI family.

Figures 2.20 (a) and 2.20 (b) demonstrate the two possible ways of designing the MJGB device structures as proposed by Dharmadasa et al. [30,31] . In Figure 2.20 (a), the starting window layer is a wide bandgap p-type semiconductor material while in Figure 2.20 (b), the starting window material is a wide bandgap n-type layer. In both cases, the last layer is a narrow bandgap layer. Starting from the front contact towards the back contact, both device structures show a gradual reduction in bandgap from E_{g1} to E_{gn}. The device structure in Figure 2.20 (a) has the advantage of a higher potential barrier height over the one in Figure 2.20 (b). With higher ϕ_b, it is possible to obtain higher V_{oc} value. However, the device structure in Figure 2.20 (b) has been used in this work for solar cell fabrication due to the availability of electroplated materials.

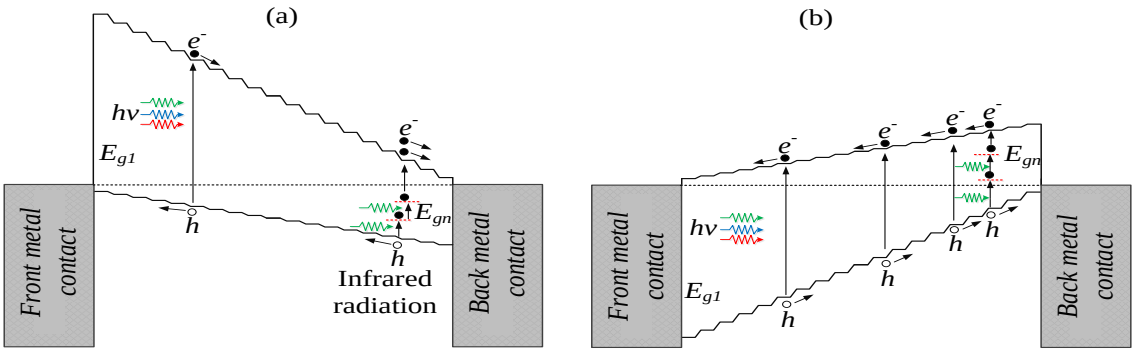


Figure 2.20. Energy band diagrams of new designs for graded bandgap solar cells proposed by Dharmadasa [30] with (a) a p-type window material and (b) an n-type window material. Redrawn from [30,31].

As light moves through the device structure, absorption of photons takes place starting from the ultra-violet (UV) region through the visible (Vis) and then finally to the infrared (IR) end of the solar spectrum. MJGB solar cells are designed in such a way that the high energy photons (UV and Vis) are absorbed by the wide bandgap semiconductor deposited first on the conducting substrate. The narrow bandgap thin

films deposited afterwards absorb the low energy photons at the infrared end of the spectrum. This absorption process is essential so as to reduce thermalisation effect [32]. Thermalisation effects do occur when high energy photons are absorbed by low energy bandgap semiconductors; when this occurs, heat is produced within the device structure and this eventually lowers the solar cell parameters and the life span. Thermalisation effect in PV solar system is like an overload effect in induction motors of an electrical system.

The MJGB also make use of impact ionisation and impurity PV effect to reduce R&G process, increase photo-generated charge carriers, separate and transport the generated carriers to external circuit before they recombine in the device structure [5]. Considering Figure 2.20 (a), when high energy photons are absorbed at the front of the solar cell, they break bonds between the atoms and excite electrons from the VB to the CB. When this happens, they create electron and hole pairs which are separated to the back and front contacts respectively. The quick separation is initiated by the presence of strong internal electric field in the solar cell structure. The strong built-in electric field is represented by the steep slope produced as a result of the device structure design. High kinetic energy (KE) is gained by the electrons accelerating towards the back contact. The electrons moving with high KE transfers its momentum to the atoms located at the rear end of the device and break the bonds between these atoms. This makes a photon which produce electrons with initial high KE to create two electron-hole pairs. This mechanism is referred to as band-to-band impact ionisation.

As explained by Dharmadasa et al. [32], the transmission of infrared photons towards the rear of the solar cell take place as a result of their low photon energy. These photons can equally break bonds between atoms and excite electrons from CB to VB due to low bandgap materials towards the back. In the same vein, heat from the surroundings or infrared radiation can break bonds between atoms and create electron-hole pairs. However, most of the far infrared photons do not possess sufficient energy to directly promote the excited electrons to the CB but the energy is adequate to promote the excited electrons to one of the defect levels located below the CB. As earlier explained, there is presence of defects at the M/S interface and these defects can be very useful if well controlled. Some of these defects may be introduced during post deposition treatment process like etching or during growth while others may be introduced during growth. The ones introduced during growth are mainly native defects.

The holes created are quickly transported to the front ohmic contact and this does not therefore permit the trapped electrons at the defect levels to fall back and recombine with the hole. Further absorption of infrared radiation can create another electron-hole pair (EHP) and the newly excited electron can push the initial excited electrons at one of the defect levels to the CB. Aside these, the high KE electrons accelerating down the slope can also promote the trapped electrons in defect levels to the CB. This mechanism of operation is referred to as impurity PV effect. The combination of impact ionisation and impurity PV effect can improve the device parameters of the fabricated solar cell showing avalanche of electrons created during this process.

2.6 Summary

In this chapter, solid materials and the different categories in which they exist have been briefly presented. Semiconductor materials have been classified into two major groups based on dopants addition and elemental composition. Brief discussions have also been made on the various interfaces which exist in an electronic device. Some of the current transport mechanisms taking place in metal/semiconductor interfaces were discussed, and highlights of some types of solar cells were also given. Since the thesis work was focused on development of graded bandgap devices, the new designs were presented to show their advantages over two-layer solar cell device structures.

References

[1] D. A. Neamen, Semiconductor physics and devices:basic principles, third ed., McGraw-Hill, New York (2003).

[2] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New Jersey (2007).

[3] A. K. Sharma, Semiconductor Electronics, second ed., New Age International Publishers Ltd., New Delhi, India (2001).

[4] J. Koryta, J. Dvorak, L. Kavan, Priciples of Electrochemistry, Second Edi, John Wiley & Sons, Ltd., Chichester, West Sussex, England (1993).

[5] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[6] B. M. Basol, J. Appl. Phys., **55** (1984) 601–603.

[7] B. E. Mccandless, J. R. Sites, Cadmium Telluride Solar Cells, in: Handb. Photovolt. Sci. Eng., first ed., John Wiley & Sons, Ltd, Chichester, West Sussex, England (2003): pp. 617–662.

[8] D. M. Chapin, C. S. Fuller, G. L. Pearson, J. Appl. Phys., **25** (1954) 676–677.

[9] J. L. Gray, The Physics of the Solar Cell, in: Handb. Photovolt. Sci. Eng., first ed., John Wiley & Sons, Ltd, Chichester, West Sussex, England (2003): pp. 61–112.

[10] V. Kabra, L. Aamir, M. M. Malik, Beilstein J. Nanotechnol., **5** (2014) 2216–2221.

[11] T. Soga, Nanostructured Materials for Solar Energy Conversion, in: Nanostructured Mater. Sol. Energy Convers., first ed., Elsevier, (2006).

[12] H. Gómez, R. Henríquez, R. Schrebler, R. Córdova, D. Ramírez, G. Riveros, E. A. Dalchiele, Electrochim. Acta, **50** (2005) 1299–1305.

[13] P. V. Meyers, Sol. Cells, **23** (1988) 59–67.

[14] W. G. Oldham, A. G. Milnes, Solid. State. Electron., **7** (1964) 153–165.

[15] B. G. Streetman, S. K. Banerjee, Solid State Electronic Devices, Sixth Edit, Pearson Prentice Hall, New Jersey (2010).

[16] J. Singh, Semiconductor Devices: Basic Principles, first ed., John Wiley & Sons, Inc., United States of America (2001).

[17] I. M. Dharmadasa, J. D. Bunning, A. P. Samantilleke, T. Shen, Sol. Energy Mater. Sol. Cells, **86** (2005) 373–384.

[18] E. H. Rhoderick, IEE Proc. I Solid State Electron Devices, **129** (1982) 1–14.

[19] M. F. Mabrook, D. Kolb, C. Pearson, D. A. Zeze, M. C. Petty, Adv. Sci. Technol., **54** (2008) 474–479.

[20] J. R. Pugh, D. Mao, J. G. Zhang, M. J. Heben, A. J. Nelson, A. J. Frank, J. Appl. Phys., **74** (1993) 2619–2625.

[21] H. Card, Solid. State. Electron., **16** (1973) 365–374.

[22] D. Kearns, M. Calvin, J. Chem. Phys., **29** (1958) 950–951.

[23] H. Spanggaard, F. C. Krebs, Sol. Energy Mater. Sol. Cells, **83** (2004) 125–146.

[24] P. N. Rivers, Leading Edge Research in Solar Energy, Nova Science Publishers, (2007).

[25] N. G. Park, Mater. Today, **18** (2014) 65–72.

[26] NREL, Best Res. Cell Effic., (2016). http://www.nrel.gov/ncpv/images/efficiency_chart.jpg (accessed April 22, 2016).

[27] P. P. Boix, K. Nonomura, N. Mathews, S. G. Mhaisalkar, Mater. Today, **17** (2014) 16–23.

[28] A. Kojima, K. Teshima, Y. Shirai, T. Miyasaka, J. Am. Chem. Soc., **131** (2009) 6050–6051.

[29] Y. Zhou, K. Zhu, ACS Energy Lett., (2016) 64–67.

[30] I. M. Dharmadasa, Sol. Energy Mater. Sol. Cells, **85** (2005) 293–300.

[31] I. M. Dharmadasa, J. S. Roberts, G. Hill, Sol. Energy Mater. Sol. Cells, **88** (2005) 413–422.

[32] I. M. Dharmadasa, N. D. P. S. R. Kalyanaratne, R. Dharmadasa, J. Natl. Sci. Found. Sri Lanka, **41** (2013) 73–80.

Chapter 3 - Techniques for materials growth, materials and device characterisation

3.1 Introduction

The development of thin films can be achieved using physical methods such as sputtering, evaporation, epitaxial growth, thermal or chemical methods such as chemical vapour deposition (CVD), metal organic chemical vapour deposition (MOCVD), chemical bath deposition (CBD), electrodeposition (ED) and polymer assisted deposition (PAD). Before the thin film deposition, it is of utmost importance to prepare the substrate on which the thin films would be grown. After the thin films development, it is essential to study their material and electronic properties. This chapter focuses on electrodeposition technique as the main growth technique used in this research work and some of the analytical techniques used in material and device characterisation.

3.2 Substrate selection and preparation

The deposition technique used in this work requires the usage of conducting substrates to grow the thin film material. For this reason, the substrate needs to be well prepared before being used in the electrolytic bath. Failure to thoroughly clean the substrate may introduce impurities to the bath in ppm level and this may eventually affect the overall efficiency of the solar cell. Apart from impurity introduction into the bath, uniform deposition of thin film may not be obtained on the substrate. This non-uniformity is a problem in thin film deposition because it causes the doping concentration of the deposited layers to vary from one point to another on the thin film. Some of the properties of the conducting substrates are that it must have low resistance and be transparent. Due to their transparent nature, they are often referred to as transparent conducting oxide (TCO). The most widely used TCO are fluorine-doped tin oxide (FTO) and indium-doped tin oxide (ITO). ITO-coated glasses have low thermal stability when used as a TCO substrate [1] and they are more expensive than FTO-coated glass.

In this work, FTO-coated glasses have been used as conducting substrates due to their numerous advantages over ITO. Some of the merits offered by FTO are its stability under atmospheric conditions and high temperature, mechanical hardness, high tolerance to physical abrasion and chemical inertness [2]. TCOs generally have low

resistivities. The resistivities of the FTO substrates are selected based on their sheet resistance. In this work, FTO-coated glasses with sheet resistances of 7 Ω/□ and 13 Ω/□ purchased from Sigma-Aldrich have been used. The substrates were cut into the desired dimension before cleaning. The cleaning was first done in ultrasonic medium containing soap solution for 15 minutes. A further rinsing action using de-ionised water was carried out on the glass/FTO substrates after completing the ultrasonic cleaning. The surfaces were finally rinsed in organic solvents (methanol and acetone), washed in de-ionised water and dried with nitrogen gas flow before being applied as the working electrode in the ED set-up.

3.3 Electrodeposition growth technique

Electrodeposition is a non-vacuum growth technique used in depositing metallic and semiconducting coatings on top of an electrically conductive substrate such as metal [3]. This growth technique offers a lot of advantages among which are: reduction of material waste during and after growth, providing an enabling environment to grow thin films with small and large areas (scalability), low-cost, ease of intrinsic and extrinsic doping, self-purification of electrolytic bath, bandgap tunability and manufacturability, low temperature growth and the ability to control the film thickness by varying the deposition time and potential [4,5]. The scalability of this technique was proven by BP Solar when they manufactured 0.94 m^2 solar panels with efficiency of ~10.6% [6].

Electrodeposition can be categorised into different groups based on the power supply source and the working electrode being used. With respect to the power supply source, electrodeposition can be potentiostatic or galvanostatic. In potentiostatic deposition, direct current at fixed voltage is used while in galvanostatic deposition, the power source is a direct current at constant current [7]. Potentiostatic electrodeposition has been used in this work to carry out electroplating work. Depending on which electrode is used as the working electrode (WE) in electroplating technique, the growth of thin films can be achieved using cathodic and anodic means of deposition. In cathodic electrodeposition, the cathode electrode serves as the working electrode while in anodic electrodeposition; the anode serves as the working electrode. The electrodeposition of thin films take place on the working electrode and for this reason, the conducting substrate which function as the WE must not react chemically with the electrolyte [2].

As explained by Pandey [7], the cathodic deposition has gained a wide popularity in electrodeposition growth technique because it produces stoichiometric thin films with good adherence to the substrate and most of the metal ions are cations (positive ions); while in anodic deposition, the thin films formed have poor adhesion and stoichiometry. In this research work, cathodic electrodeposition has been used to carry out the growth of thin films. The components making up the electrodeposition system are: electrolytes, electrodes (anode which is a counter electrode, cathode which functions as the working electrode and reference electrode), power supply, electric heater with a magnetic stirrer. The electrodeposition system can be set-up as a two-electrode or three-electrode system. In this work, two-electrode system was used to carry out the electroplating of semiconductor thin films. The main difference between these two is that in two-electrode set-up, two electrodes namely anode and cathode are used while in three-electrode set-up, a third electrode known as a reference electrode is introduced. The use of the third reference electrode has been avoided in this research to prevent possible leakage of unwanted group 1A and 1B ions like Ag^{+} and K^{+} from Ag/AgCl and saturated calomel electrode (SCE) into the electrolytic bath most especially CdTe electrolyte which is used in electroplating the main solar cell absorber layer being studied in this work. The Ag^{+} and K^{+} are classified as p-type dopants to CdTe thin films and since the main research interest is focused on electroplating n-CdTe thin films as absorber layer, the leakage of these ions into the bath can cause compensation to take place thus leading to a high resistive material which can adversely affect the solar cell device efficiency. The deterioration in efficiency of CdTe-based solar cells after being contaminated with Ag^{1+} and Cu^{2+} ions have been reported by Dennison [8].

Figure 3.1 shows the schematic diagram of the two-electrode set-up in electrodeposition technique. The bath contains an electrolyte comprising of metal ions (for instance, $ZnSO_4$ for the deposition of Zn). The conducting surface (cathode) is usually immersed in an electrolyte solution containing salt of the metal ions. As illustrated in Figure 3.1, the cathode and anode electrodes are connected to negative and positive terminals of the power source respectively. When a direct current maintained at constant voltage from the power supply flows through the electrolyte, the anions and cations of metal salts move toward the anode and cathode respectively and may be coated on the electrodes after charge transfer reaction has taken place [7]. This type of electrodeposition is referred to as cathodic electrodeposition.

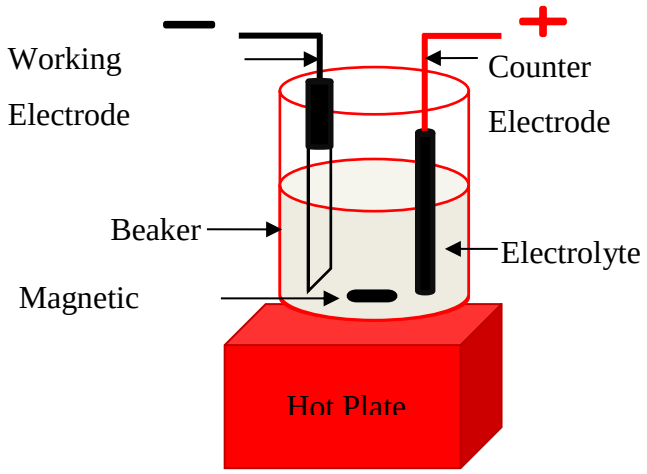


Figure 3.1. Electrodeposition set-up for a simplified 2-electrode system.

In the cathodic electrodeposition, the salts of metal ions which carry positive charges (cations) are attracted towards the cathode. In this process, the positive metallic ions will gain electrons from the cathode and will reduce to the metallic form as a solid thin film on the glass/FTO substrate which is used as the working electrode [9]. In the anodic electrodeposition, the anions are attracted towards the anode, donate one or more electrons to the anode and finally form a deposit in the form of a solid thin film on the FTO substrate attached to the anode. This process in which the anions donate electrons to the working anode electrode is referred to as oxidation.

The electrodeposition technique works on the principle of electrolysis which was discovered by Michael Faraday in 1834 [10]. The two laws postulated by Faraday relate the mass of the electrodeposited material to the deposition current density and atomic weight of the material. The first law states that "the mass of a substance deposited or liberated at any electrode is directly proportional to the quantity of electrical charge passing through the electrolyte". The second law explains that when the same amount of charge is passed through the electrolytes, the mass of the substances deposited or liberated is proportional to its respective chemical equivalent weight. The chemical equivalent weight is the ratio of molecular weight to the valence number of ions (electrons transferred per ion).

The first law can be expressed mathematically as

$$m = ZQ \tag{3.1}$$

Where Z is a constant known as chemical equivalent weight.

The chemical equivalent weight from the second law can be expressed mathematically as shown in Equation (3.2)

$$Z = \left(\frac{M}{z}\right) = \left(\frac{M}{nF}\right) \tag{3.2}$$

Combining Equations (3.1) and (3.2) together

$$m = \left(\frac{Q}{F}\right)\left(\frac{M}{n}\right) \tag{3.3}$$

where m is the mass of material in gram formed on an electrode, Q is the effective electric charge in Coulomb that passes through the cell, F is the Faraday's constant with value 96,485 $Cmol^{-1}$, M is the molecular weight of the material in $gmol^{-1}$, z is valence number of ions and n is the number of electrons transferred in the chemical reaction for the formation of 1 mol of substance in gcm^{-3}.

Faraday's equation can further be modified to calculate the thickness of the electrodeposited material as shown in Equation (3.4).

$$T = \left(\frac{1}{nF}\right)\left(\frac{itM}{\rho A}\right) = \left(\frac{JtM}{nF\rho}\right) \tag{3.4}$$

Where T is the thickness of the material in cm, i is the average deposition current in Ampere, A is the surface area of the coated material, J is current density in Acm^{-2}, t is the deposition time in seconds and ρ is the density of the deposited material in gcm^{-3}.

3.4 Cyclic Voltammetry

Before electroplating the various semiconductor materials and studying their individual properties, it is essential to determine the range of cathodic potential suitable for their deposition. The tool used for this purpose is known as cyclic voltammetry [11]. In this process, a range of cathodic potentials are scanned, for instance from 0 to 2,000 mV between the electrodes immersed inside the electrolyte, using a computerised potentiostat at a constant sweep rate. The currents through the electrolyte are monitored as the voltages between electrodes are changed. The currents corresponding to each scanned potential are plotted and the results give a cyclic voltammogram. Cyclic voltammogram can therefore be described as the current-voltage characteristics that describes the conduction of electrical current through the electrolyte as a function of applied potential [12]. The potential is usually scanned in both forward and reverse direction so as to determine the approximate voltage in which the deposition and

dissolution of the electroplated layers take place. This technique has been used in this work to investigate suitable regions of deposition potential to electroplate thin films that are near stoichiometric. The power source used in this work is GillAC computerised potentiostat (ACM instrument) and the scanning was carried out at a sweep rate of 180 $mVmin^{-1}$.

3.5 Techniques used for material characterisation

The material properties of the semiconductors developed in this work have been studied using some basic analytical techniques such as photoelectrochemical (PEC) cell measurement for investigating the electrical conductivity type of the semiconductor material, optical absorption technique for studying the optical properties of the material, X-ray diffraction (XRD) and Raman spectroscopy for evaluating the material structural properties, scanning electron microscopy (SEM) technique for determining the material morphological properties, energy dispersive X-ray analytical (EDX) technique for analysing the compositional properties of the material, Ultra-violet photoelectron spectroscopy (UPS) for studying the position of the Fermi level in semiconductor materials and direct current (DC) conductivity measurement technique for resistivity determination. This section will be focused on the analytical techniques used in this research work.

3.5.1 Photoelectrochemical cell measurement

Photoelectrochemical (PEC) cell measurement is a quick and easy technique used in the determination of electrical conductivity type of semiconductors. The technique involves a semiconductor and electrolyte with interface creation between them. The interface formed between the semiconductor and electrolyte is very similar to the junction formation between semiconductors and metal, that is M/S interface also known as Schottky barrier. As explained in sub-section 2.4.6.2 of Chapter 2, both semiconductors and metals have different Fermi energy levels in their energy bandgap before making contacts with each other. In the same manner, electrolytes also have an energy level known as $E_{o\ REDOX}$ while the Fermi level position (*FLP*) of the semiconductor remains E_F. This E_F can be E_{Fn} or E_{Fp} depending on whether the semiconductor material is n, or p-type respectively.

By immersing the semiconductor inside the electrolyte, electron transfer takes place between the two until equilibrium is achieved. At equilibrium, there is an alignment of the Fermi level of the semiconductor with the redox energy level of electrolyte according to Equation (3.5); this alignment do take place under dark condition as shown in Figure 3.2 (b) for both n- and p-type materials.

$$E_{Fn} \text{ or } E_{Fp} = E_{REDOX} \tag{3.5}$$

As illustrated in Figure 3.2 (b), band bending takes place at the region of the semiconductor which is near the semiconductor/electrolyte (S/E) interface [13]. The band bending direction can either be upward or downward depending on the initial Fermi (E^I_F) level position of the semiconductor [14]. If the semiconductor material under investigation is n-type, band bends upwards. For a p-type semiconductor material, band bends downwards as illustrated in Figure 3.2 (b).

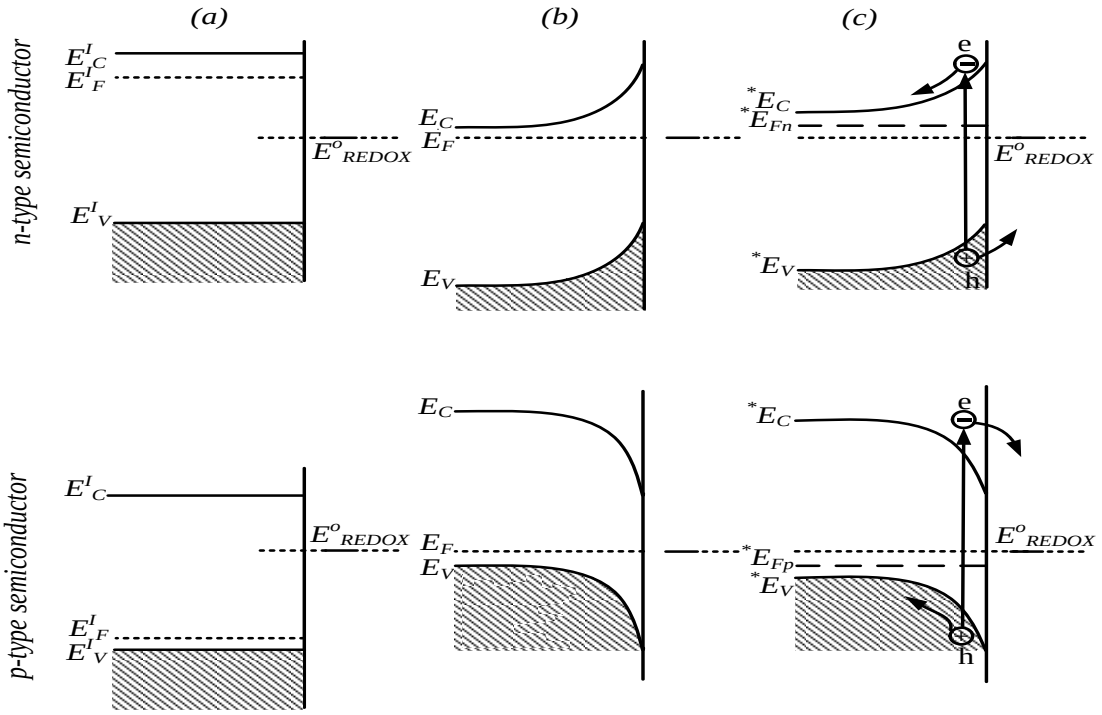


Figure 3.2. Band diagram formation between semiconductor and electrolyte (a) before the semiconductor makes contact with the electrolyte, (b) after the semiconductor makes contact with the electrolyte under dark condition and (c) after the semiconductor makes contact with the electrolyte under illumination condition.

Under illumination condition, photons with energy greater than the bandgap are absorbed in the semiconductor region and this leads to generation of electron-hole pairs.

Once created, the electrons and holes no longer maintain equilibrium and this shifts the Fermi level towards the initial Fermi level of the semiconductor to create a new Fermi level under illumination denoted as $^{*}E_F$ (this can either be $^{*}E_{Fn}$ or $^{*}E_{Fp}$) as shown in Figure 3.2 (c). When this shift occurs, there is a decrease in the band bending. The potential change (ΔE) expressed in Equation (3.6) [13] therefore corresponds to the difference in the shift of the Fermi energy level measured under dark and light conditions per unit charge, *e*.

$$\Delta E = \left(\frac{1}{e}\right) \left| {}^{*}E_F - E_F \right| = E_{light} - E_{dark} \tag{3.6}$$

As illustrated in Figure 3.3, the set-up for the PEC cell measurement consists of glass/FTO/semiconductor (of unknown conductivity type) which serves as the semiconducting electrode, a graphite electrode which is used as the counter electrode and electrolyte prepared from 0.10 M $Na_2S_2O_3$ in 20 ml of de-ionised water. The two electrodes are immersed in the prepared electrolyte and connected to a DC voltmeter. The potential between the two electrodes are measured under both dark and illuminated conditions. The PEC signal or open circuit voltage produced by the solid/liquid junction is obtained by taking the difference between the potential measured under dark and illumination conditions. Before using the PEC cell set-up to carry out further measurement, it is usually first calibrated with a known semiconductor like n-CdS before measuring un-known semiconductors. The sign of the PEC signal helps in determining the electrical conduction type of the electrodeposited materials while the magnitude of the PEC signal is a factor of the doping concentration of the semiconductor material under test [15]. When the PEC signal produces zero PEC signal, it signifies that the material can be insulating, intrinsic or metallic.

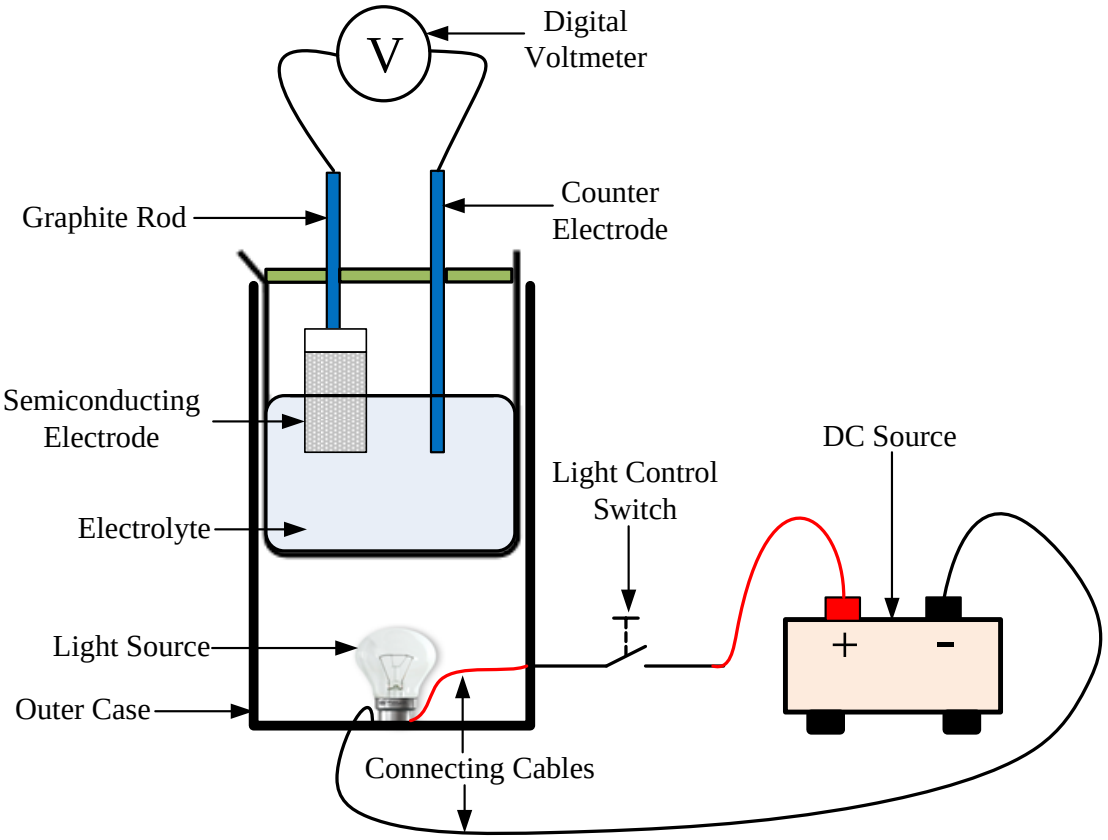


Figure 3.3. Typical schematic diagram of the experimental set-up for PEC cell measurement.

3.5.2 UV-Vis Spectrophotometry

The bandgap of semiconductor materials and other optical properties such as % transmittance can be obtained using optical absorption technique. The basic equipment used in this technique is known as Ultraviolet-Visible spectrophotometer commonly known as UV-Vis spectrophotometer. The UV-Vis spectrophotometer measures the absorption, % transmittance and reflectance in the near UV and visible region of the electromagnetic spectrum. The range of the wavelengths for the near UV and visible region are ~(200-400) nm and ~(400-700) nm respectively. Cary 50 scan UV/Vis spectrophotometer has been used in this research work to carry out all the optical absorption measurements.

The basic components which make up the UV-Vis spectrophotometer as illustrated in Figure 3.4 are: light sources (UV and Vis.), monochromator also known as wavelength selector, sample container, detector and signal processor with readout [16]. Light

sources such as deuterium and hydrogen lamps which emit radiation within the range (160-375) nm can be used as light source for UV radiation. For visible and near infrared radiation, tungsten filament or halogen lamps can be used since it can emit radiation within the range (350-2500) nm wavelength. The radiations emitted by these light sources also extend into the UV region; for this reason, they are mostly used in spectrophotometers.

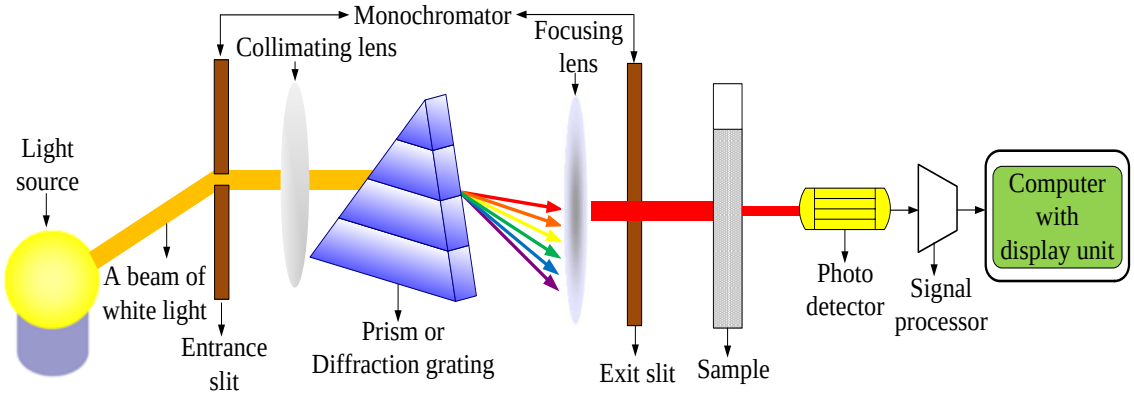


Figure 3.4. A typical schematic diagram showing the basic components of a UV-Vis spectrophotometer.

A monochromator consists of an entrance slit, a collimating lens, a dispersing device such as a prism, a focusing lens and an exit slit. The emitted light which consists of radiation having more than one single wavelength (that is, polychromatic radiation) passes through an entrance slit into a monochromator. In a spectrophotometer, a beam of monochromatic radiation is provided to illuminate a material and the ratio of intensity of incoming photons to the outgoing ones is measured. The beam is assembled together via a collimating lens and then strikes the reflection prism (dispersing device) at an angle. The prism eventually splits the beam into its wavelengths. By rotating the prism, the output radiation which has a specified wavelength leaves the monochromator through the exit slit and is directed towards the material under test. Depending on the thickness of solid materials under test, some of the intensity of a beam of monochromatic light is absorbed while others are transmitted as shown in Figure 3.5. The intensity of transmitted light (I) is related to the intensity of incident light (I_o) by Equation (3.7).

$$I(x) = I_o \exp(-\alpha x) \tag{3.7}$$

Where *x* is the thickness of the semiconductor and it represents the distance into which light travels through in the semiconductor material. α is a constant and it is the material's absorption coefficient; it determines the rate at which the material absorbs light as light passes through it.

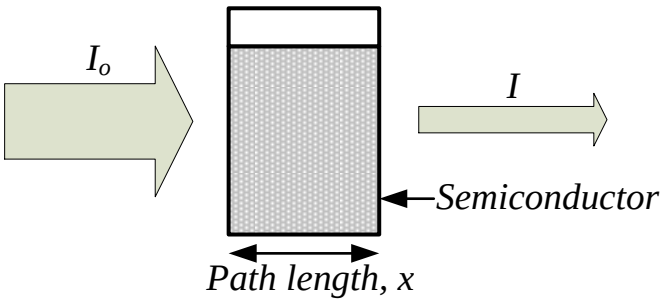


Figure 3.5. Typical schematic diagram illustrating the light intensity before (I_o) and after absorption (I).

The transmittance (T) of the material is defined by the ratio of the transmitted light intensity to the intensity of the incident monochromatic light as expressed in Equation (3.8)

$$T = \frac{I}{I_o} \tag{3.8}$$

Equation (3.9) relates the absorbance (A) and transmittance with each other [17]

$$A = \log_{10}\left(\frac{I_o}{I}\right) = \log_{10}\left(\frac{1}{T}\right) = \log_{10}\left(\frac{100}{\%T}\right) = 2 - \log_{10}\%T \tag{3.9}$$

$A = 2 - \log_{10}\%T$ permits easy calculation of absorbance from the data of % transmittance.

The transmitted light is detected by photodiode which functions as a detector in this case. The detector converts monochromatic light radiation into electrical signal which is sent as input to the signal processor. The signal processor amplifies the signal, processes it and passes the processed signal to a display unit such as computer. The spectrophotometer measures the absorbance and other optical properties as a function of wavelength. By plotting the square of absorbance (A^2) against the energy of photon ($h\nu$), the bandgap can be estimated by extrapolating the straight line portion of the absorption curve to the photon energy axis. Also, the bandgap can be obtained by plotting $(\alpha h\nu)^2$

versus $h\nu$ and extrapolating the straight line portion of the $(\alpha h\nu)^2$ versus $h\nu$ absorption curve to the photon energy axis.

The relationship between the absorption coefficient (α) of a direct bandgap semiconductor material, the incident photon frequency (ν) and the optical bandgap (E_g) is expressed by Tauc relation in Equation (3.10) [18].

$$\alpha h\nu = k(h\nu - E_g)^{1/2} \tag{3.10}$$

Where *h* is Planck's constant and *k* is the constant of proportionality which depends on the refractive index of the sample.

3.5.3 X-ray diffraction (XRD)

X-ray diffraction (XRD) technique is a non-destructive and non-contact method used in identifying the crystal structures and phases present in crystalline materials. It also gives information on the materials crystallite sizes, atomic planes, lattice spacing, preferred orientation and intensity of the individual peaks obtained from the XRD measurement. This technique was discovered in 1912 by Max von Laue when he observed that crystalline materials behave as 3-dimensional diffraction gratings for X-ray wavelength in a similar manner to that of plane spacing in a crystal lattice [19]. As shown in Figure 3.6, the samples to be tested are put inside the sample holder stationed between the X-ray tube and X-ray detector. The X-ray tube generates the X-rays which are filtered to yield monochromatic radiation. These rays are assembled together through a collimator and made to pass through a slit. These slits have different dimensions based on the opening created in them. The slit dimension may range from (1/32 to 2) mm. The interaction between the monochromatic rays after passing through the slits and the sample is known as interference. The X-ray tube gradually moves so as to focus the rays on the sample under investigation and this movement leads to changes in the incident angles.

The operational principle of XRD is established on the constructive interference of monochromatic X-rays and a crystalline sample. X-ray is an electromagnetic radiation having wavelength ranging between (0.1-100) Å while a crystal is a regular array of atoms. The wavelength range of the X-ray is similar to the distances between atoms in a crystal and this is why it is easy for X-rays to be diffracted by the crystal structures [20]. When the X-rays strike the crystal atoms, they are scattered by the electrons in the

atoms and this results in the production of secondary spherical waves that emanate from the electron. This type of scattering is known as elastic scattering and the electron which causes the scattering is referred to as the scatterer.

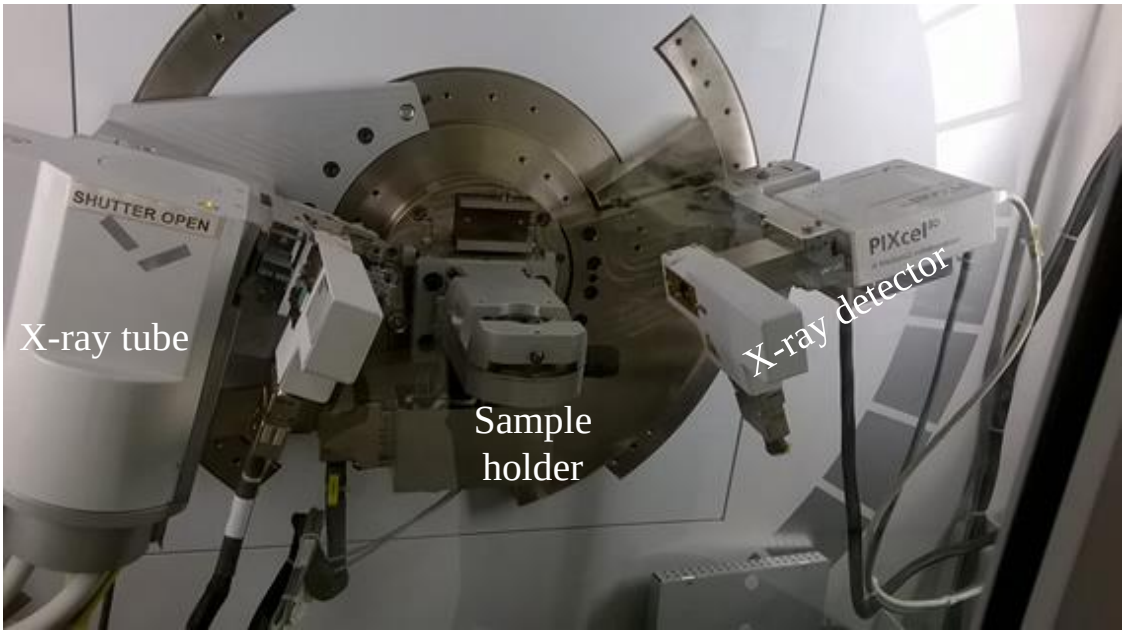


Figure 3.6. Typical XRD equipment illustrating the three main sub-compartments.

The reflection of incoming rays by electron in the atom gives rise to diffracted rays. In some instances, the scattered rays cancel one another (destructive interference) or support one another (constructive interference). The interaction between the incident X-rays having wavelength, λ measured in Angstrom (Å) and the sample under investigation produces constructive interference and diffracted rays when conditions of interaction fulfil Braggs law stated in Equation (3.11).

$$n\lambda = 2d\sin\theta \tag{3.11}$$

Where d is the inter-atomic spacing, n is a positive integer and θ is the angle between the incident or diffracted X-rays beam and the atomic plane.

The Braggs law is derived from Figure 3.7. The occurrence of constructive interference produces a peak in intensity. The diffracted X-rays are then detected and processed by the X-ray detector. The detector finally converts the processed X-ray signal to a count rate before sending it as an input signal to a computerised device from where XRD spectrum (the output) is obtained.

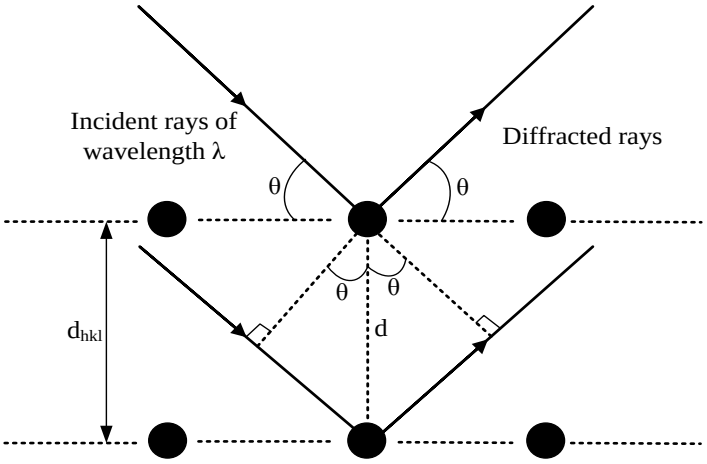


Figure 3.7. Schematic of Bragg's analysis showing the production of diffracted rays as incident rays interact with atoms inside the solid crystals.

The XRD patterns in this work were obtained by plotting the XRD count rate versus the position of angles. Information about the crystallite size of the samples being measured can be obtained from the data extracted from XRD instrument after measurement by using the Scherrer formula stated in Equation (3.12). However, the Scherrer equation has limitation since it cannot be used to estimate crystallite sizes more than 100 nm [21].

$$D = \frac{0.94\lambda}{\beta \cos\theta} \tag{3.12}$$

Where λ is the X-ray wavelength measured in Å, β is FWHM measured in radians and θ is the Bragg's angle measured in degree. The d-spacing permits easy identification of sample since each material has a distinct d-spacing value which can be compared with the standard d-spacing value reported in the JCPDS reference file. One other important parameter obtained from the XRD measurement is the full width at half maximum (FWHM). This parameter alongside other parameters stated in Equation (3.12) is used in getting the crystallite size (D) of the measured sample. The XRD spectra in this work were obtained using Philips PW 3710 X'pert Pro diffractometer with Cu-K_α monochromator of wavelength, λ=1.542 Å in the range of $2\theta=(20\text{-}70)^o$. The current and tension of the X-ray generator were set to 40 mA and 40 kV respectively.

3.5.4 Raman spectroscopy technique

The Raman spectroscopy technique is a quick and non-destructive method to analyse semiconductor material qualities such as homogeneity, surface conditions and microcrystallinity [22]. This technique can be used for quantitative and qualitative analysis of samples. Quantitative and qualitative analysis are carried out by measuring intensity and frequency of scattered radiations respectively [23]. The technique is used as fingerprint for quick identification of unknown materials by comparing the material under test with standard reference spectra.

It is a scattering technique which is based on Raman Effect. The principle of operation is based on inelastic scattering of monochromatic light most especially laser beam. The monochromatic light acts as the incident radiation to the sample under investigation. When samples are illuminated with monochromatic laser light at a certain frequency, the molecules in the sample interact with the laser light and begin to vibrate which eventually leads to emission of scattered light with different frequency. The shift in the frequency between incident and scattered light is known as Raman shift or Raman Effect. This shift provides information about the rotational, vibrational, frequency levels and other low-frequency modes in the material. The inelastic scattering is a phenomenon generally used when the frequency of monochromatic incident photons differs in value from the frequency of scattered radiation upon interaction with the sample. The emitted scattered light is detected by photon detector in computerised Raman set-up equipment, analysed and displayed as Raman spectrum on the computer visual display unit. The Raman spectra reported in this thesis were obtained using a Renishaw Raman microscope with 514 nm argon ion laser source and a charge-coupled device (CCD) detector.

3.5.5 Scanning electron microscopy technique

Scanning electron microscopy (SEM) is an analytical technique used in studying the morphology of thin film materials. It is an electron microscope which scans sample under investigation with focused beam of electrons to produce images in a vacuum system using high accelerating voltage. The first microscope with high magnification was invented in 1937 by Manfred von Ardenne [24]. Figure 3.8 shows a typical schematic diagram of SEM equipment [25]. The SEM instrument consists of five basic components namely: electron source, column containing electromagnetic lenses via

which electrons travel down, sample chamber, electron detector and computer with visual display unit (VDU) to view the scanned images.

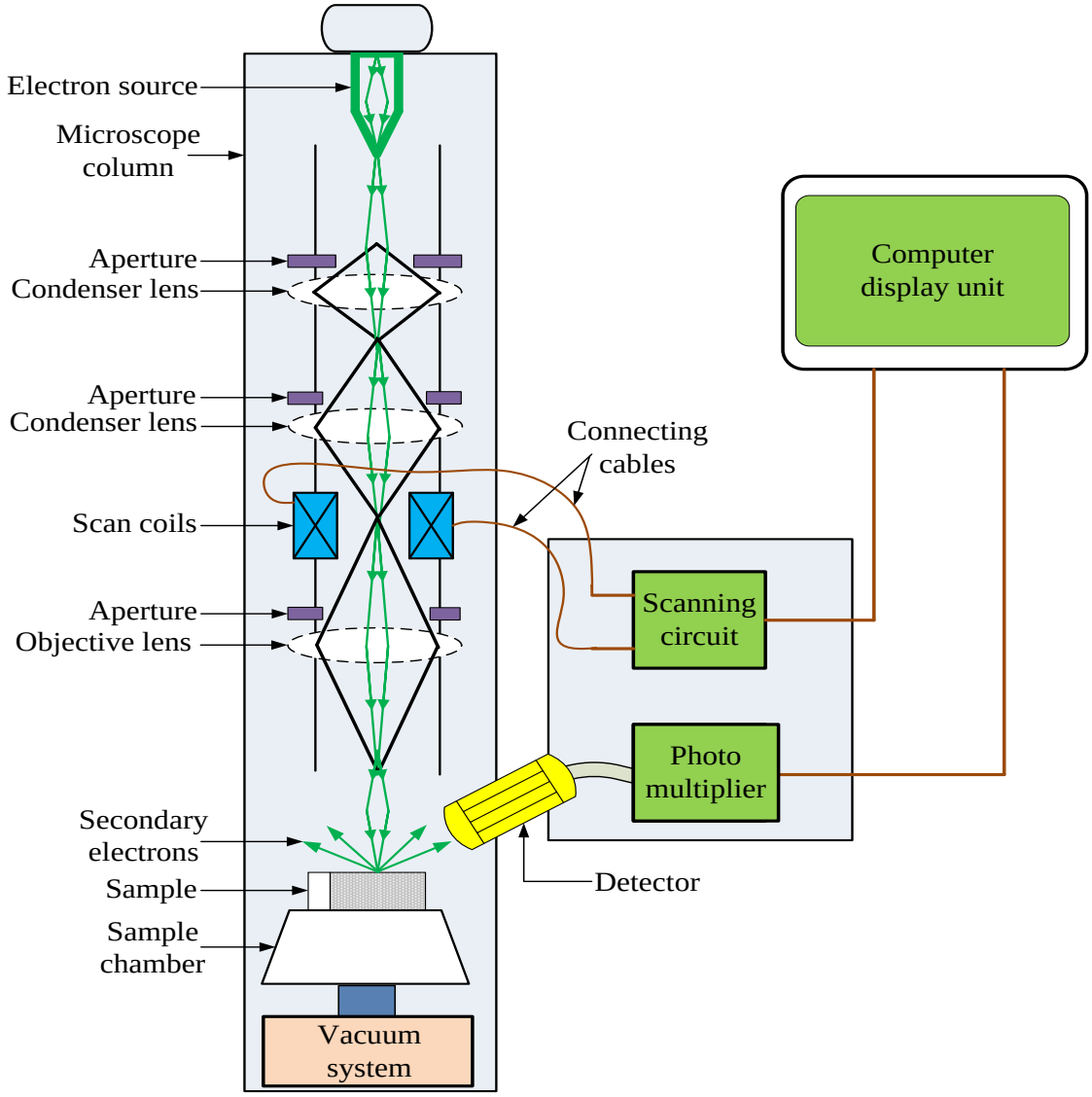


Figure 3.8. Typical schematic diagram of scanning electron microscope. Redrawn from [25].

Tungsten filament, Lanthanum hexaboride (LaB_6) or Cerium hexaboride (CeB_6) solid state crystal and field emission gun (FEG) are the three main types of electron sources used in SEM instrument [26]. Electrons are produced at the source (for instance, the electron gun shown in Figure 3.8) sited at the upper part of the column by thermionic heating at very high voltage ranging from ~5 kV to ~30 kV. The voltage range may vary from one instrument to the other. The produced electrons accelerate through the column and passes through the set of condenser lenses and apertures to generate a focused ray of electrons which strike the surface of sample mounted on a stage in the sample

chamber. The main function of these lenses is to focus the beam of electrons as it travels from the electron source to the sample chamber down the column. The scan coils which are located above the objective lens controls the position at which the electron beam hits the sample and it also allows the beam to be scanned across the area of the sample surface in a raster way [25]. An interaction therefore takes place between the electrons and atoms in the sample to produce numerous signals in the form of secondary electrons, backscattered electrons, auger electrons and characteristic X-rays [27]. These signals which comprise of information about the surface topography and composition of the material being tested are collected by detector to produce images which can be viewed on a computer VDU.

The basic signals being used for image production are the secondary electrons (SE) and backscattered electrons (BSE). The secondary electrons are usually low-energy electrons generated via ejection of electrons from the surface of sample atoms and they are detected by the secondary electron detector (SED) [28]. The SED can be used to detect the surface morphology of the sample since secondary electrons are low energy electrons created near the surface and not at the in-depth of the sample [25]. One disadvantage of the SE is that it can be affected by noise which can lower the quality of the SE images [28].

On the other hand, the backscattered electrons are higher energy electrons which originate from a notable depth within the material (sample) and are resiliently backscattered by the sample atoms. The backscattered electrons are generated when there is an interaction between the incident beams of electron and the nucleus of an atom in a sample. When this interaction takes place, the primary electron may scatter in any direction with minimal energy loss. Some of the scattered electrons are then directed back out of the sample to produce back scattered electrons which are then detected by backscattered electron detectors (BSED). The BSE does not give valuable facts about the sample topography; rather, they give compositional information on samples with higher atomic numbers; this is because atoms having higher atomic numbers easily backscatter. The greater the atomic number of an atom, the higher will be the positive charge of the atom's nucleus and the greater the tendency for an interaction producing BSE to occur [28]. Three types of signals produced by the primary electron beam are illustrated in Figure 3.9 with respect to their depth of generation from within the sample.

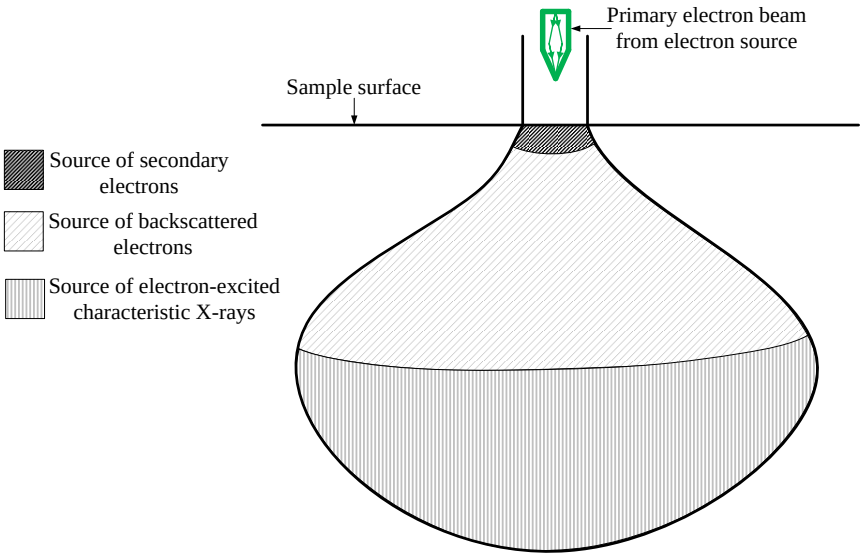


Figure 3.9. Typical diagram illustrating the production of three different signals within the specimen volume as a result of sample-electron interaction. Note the different sections of the specimen volume where characteristic X-rays, secondary and backscattered electrons emerge from.

Some other important factors which should be taken note of when carrying out the morphological measurement using SEM technique are accelerating voltage and the electron spot size. The accelerating voltage alongside with sample thickness determines the depth to which electron beam will penetrate through when it strikes the sample. The electron spot size coupled with the volume of interaction between the sample and electron beam determine the maximum resolution obtainable in SEM measurement. Some SEM instruments have a resolution in the range (1-20) nm [26].

The SEM micrographs reported in this work were obtained using the FEI Nova NanoSEM 200 at the Materials and Engineering Research Institute (MERI) of Sheffield Hallam University, Sheffield, United Kingdom. This instrument has an accelerating voltage of up to 30 kV and resolution of up to 1 nm. No special preparation was made for the samples used in the SEM analysis except that the samples were thoroughly washed with methanol, rinsed in de-ionised water and dried in a nitrogen gas flow before being transferred to the SEM vacuum system. Also, silver paint has been used to electrically connect the metallic sample holder and glass/FTO on which the thin film is deposited on. The essence of this connection is to prevent charging effects which take place between the sample holder and thin films grown on FTO/glass since the glass is a non-conductive material. Charging effects do take place on non-conductive materials

during scanning in a vacuum system and this may introduce error during image scanning.

3.5.6 Energy Dispersive Spectroscopy (EDS)

Energy dispersive spectroscopy (EDS) or energy dispersive X-ray analysis (EDX) is a technique used to analyse the composition of atoms present in a sample both qualitatively and quantitatively. It can be used to detect the elements present in the periodic table. EDS instrument can be found in most SEM equipment as a sub-part or as an attachment to the main SEM instrument. One of the limitations of this equipment is that it gives information mainly on the atomic composition and not molecular composition of the samples [27]. As earlier explained in SEM technique, the interaction of high energy electron beam with samples generate signals such as secondary electrons (SE), backscattered electrons (BSE), auger electrons and characteristic X-rays [27]. While the SEM makes use of SE and BSE, the EDX uses characteristic X-rays.

The characteristic X-rays are produced when high energy electron beam knocks out of the atom an inner shell electron and the vacant site being generated as a result of ejection of inner shell electron is being occupied with outer shell electron; this is illustrated in Figure 3.10. The ejected electron becomes ionised and the atom becomes unstable due to the electron vacancy generation. To stabilise this atom, electron from outer shell has to move into the inner shell to fill the vacancy. When this transition happens, there is a release of excess energy which corresponds to the difference in energy between the two shells. The excess energy is therefore emitted as an X-ray photon. The emitted X-rays have wavelength which depends on the characteristics of atoms inside the sample, hence the name characteristics X-rays [29]. The emitted X-rays are named based on the shell where the first vacancy occurs and the shell where electrons transit from to occupy the vacancy. As shown in Figure 3.10, if the first vacancy takes place in the K-shell and electrons transit from L shell to fill the vacancy in K shell, the X-ray emitted is referred to as K_α X-ray. On the other way round, if electrons transit from M shell to occupy the vacancy in K shell, the emitted X-ray will be referred to as K_β X-ray [28].

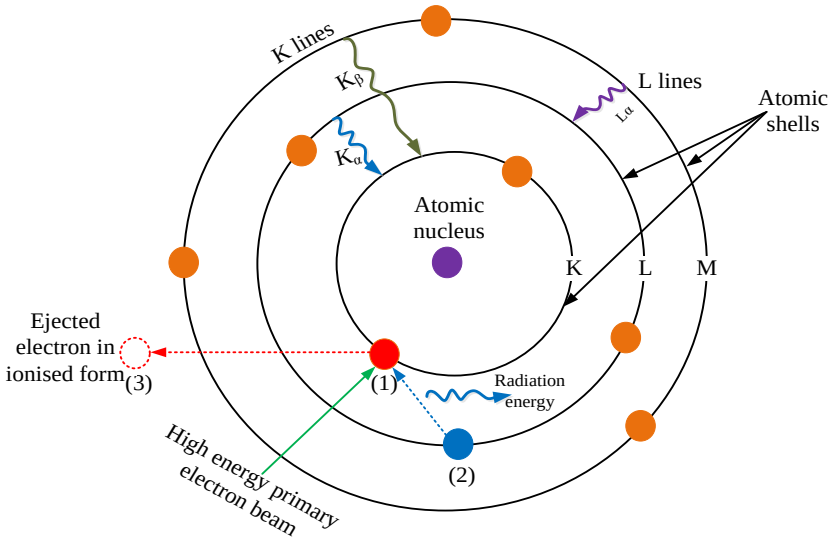


Figure 3.10. Illustration of three atomic shells (K, L, M) with emphasis on ejection of electron from inner shell leading to vacancy generation and filling of the vacancy from an outer shell. Note that the X-ray nomenclature are named based on the shell where the first vacancy occurs and the shell where electrons move from to occupy the vacancy.

Since EDX detection system is part of SEM equipment, the principle of operation is similar. Figure 3.11 shows the schematic diagram of an EDX instrument. For EDX, the detector used is made up of semiconducting silicon crystal with diffused lithium atoms, Si(Li) which has to be placed in line of sight of the sample since X-rays cannot be deflected. The distance of the detector to the sample should be as small as possible, say 20 mm or less from the sample [29]. Both SEM and EDX use the same electron source but in EDX, the characteristic X-ray being emitted from the sample is fed into the X-ray detector. The detector is usually kept in a cryostat so as to cool it with liquid nitrogen to enable it attain cryogenic temperature [30]. The detector converts the X-ray signal to voltage signals. The voltage signal is passed to a pulse processor which amplifies and measure the signal before sending it to multi-channel analyser (MCA). The MCA converts the amplified/measured voltage signal into a digital form suitable for display as a plot of histogram of intensity versus energy in keV on computer system. In this work, EDX detector attached to a FEI Nova NanoSEM 200 has been used to carry out the compositional analysis. Aztec software was used in performing the EDX analysis.

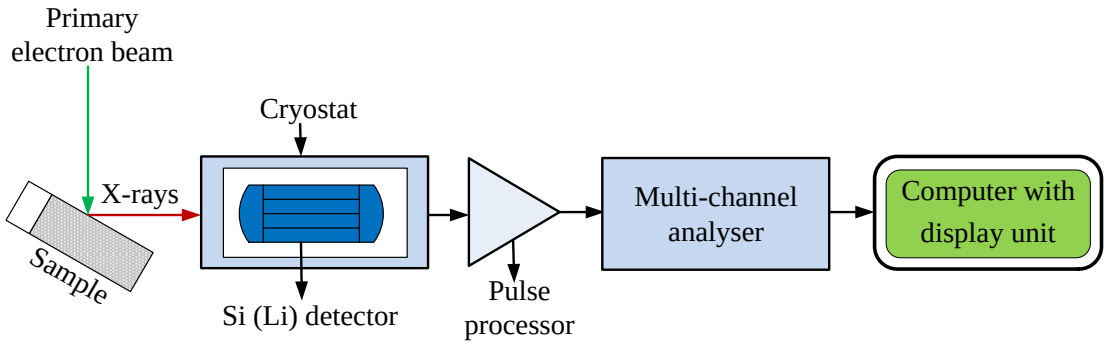


Figure 3.11. Experimental set-up of the EDX spectrometer.

3.5.7 Ultra-violet photoelectron spectroscopy (UPS)

The UPS is an analytical technique that can be used in studying the electronic band structure of solid materials [31]. The work function of a material, Fermi level of thin film semiconductor surfaces and position of valence band maximum (E_{Vmax}) can also be determined using this technique [32]. In this research work, UPS technique has been used to investigate the *FLP* of some of the electroplated semiconductor materials. By knowing the *FLP* of the material, the electrical conductivity type can thus be determined. This technique is to further complement the PEC cell measurement technique being used in this work to determine the electrical conductivity type. The UPS operation is based on the fundamental principle of photoelectric effect proposed by Albert Einstein in 1905. Photoelectric effect is a phenomenon which explains how electrons are ejected from a material surface when photons (light) shine on it. The ejected electrons are usually referred to as photoelectrons. When the energy of the incident photon ($h\nu$) is greater than the material workfunction (W), the ejected photoelectron will then have kinetic energy (E_k) given by Equation (3.13) [33].

$$E_k = h\nu - W \tag{3.13}$$

The kinetic energy of photoelectrons produced by samples after absorbing UV photons can therefore be measured by UPS technique. The basic components making up a UV system are: UV photon source, electron detector, an ultrahigh vacuum system and a computer display system. An ultrahigh vacuum system (~10^{-9} Torr) is required in UPS experiment to prevent attenuation of emitted electrons. A helium discharge lamp with two energies of He-I photon at ~21.2 eV and He-II photon at ~40.4 eV can serve the purpose of the UV photon source. Generally, the UV radiation has energy ranging

between 10-45 eV [34] to excite photoelectrons in the valence band to vacuum level. The interactions of the UV photons are however restricted to the valence band due to their low energy. In UPS, when the incident photons interact with atoms in the sample, the atoms are ionised leading to the emission of low energy photoelectrons. This low energy creates a platform to study surface properties and band structure of the material. Hence, The UPS is a highly surface sensitive technique because the path length for the ejected electrons from the sample is of few angstroms. The interference between energy of the emitted electrons and valence electrons is however a major disadvantage in this technique [31].

The UPS measurements in this work were carried out by our collaborator at the Conn Centre for Renewable Energy Research at University of Louisville, USA. The equipment used for this work was VG Scientific MultiLab 3000 ultra-high surface analysis system. This system was supported with differentially-pumped He cold cathode capillary discharge UV lamp and CLAM4 hemispherical electron energy analyser. A resonance line He-1 with photon energy of ~21.22 eV and base chamber pressure of $\sim 10^{-9}$ Torr was used for the samples excitation. Due to the possibility of having noise interference in the system at low kinetic energy, the UPS measurements were carried out using a negative bias voltage of 18 V to prevent any form of distortions in the instrument. Gold films were sputtered onto half of the samples used in this experiment while the other half of the sample was not sputtered with gold. This method allows the Fermi level of the Au and CdTe film to be aligned. The measurement of the *FLP* was done from the He-1 FL edge of the samples coated with Au. The Au sputtered area was connected to the sample stage using Ag paste for proper biasing and to prevent charging effect.

3.5.8 Direct current (DC) conductivity measurement

The concept of Ohms law has been used in the DC conductivity measurement to determine the electrical resistivity and conductivity of the semiconductor materials. To carry out this measurement, metals which form two ohmic contacts to the semiconductor have to be carefully selected. In this technique, varying DC voltages are applied across the two semiconductor terminals and the corresponding DC current that flows through the semiconductor material are measured using an ammeter. A Keithley 2401 sourcemeter has been used in this work to carry out the DC conductivity

measurements. A basic schematic diagram illustrating current flow as the voltage is being varied is illustrated in Figure 3.12.

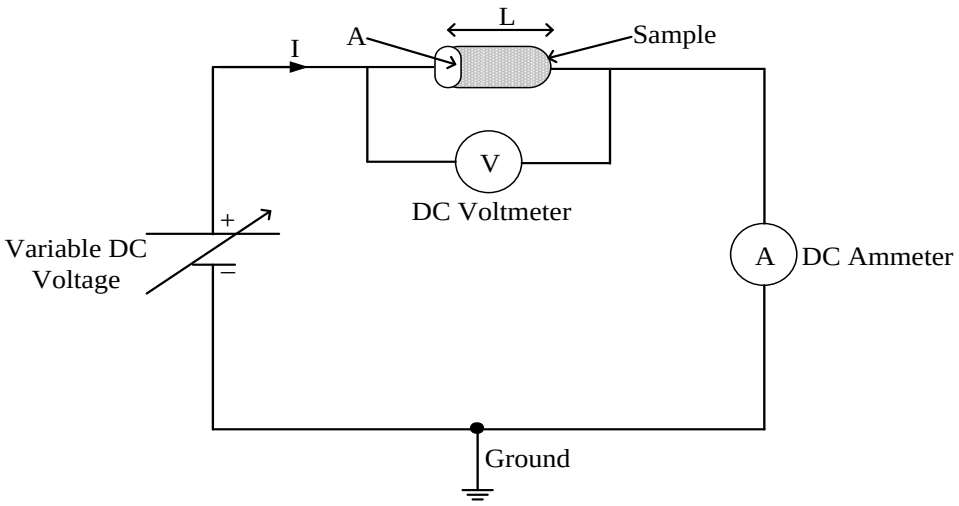


Figure 3.12. A basic schematic circuit diagram illustrating current flow in semiconductor as the voltage is being varied.

When the set of measured currents and their corresponding voltages are plotted as shown in Figure 3.13, a linear graph which obeys Ohms law by passing through the origin is obtained.

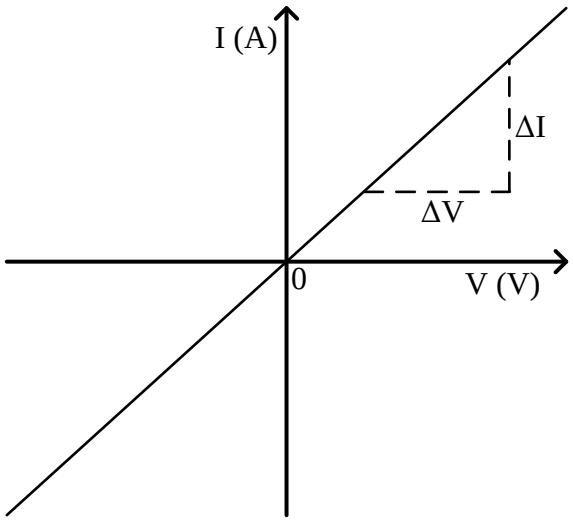


Figure 3.13. Typical I-V characteristics illustrating the linear relationship between direct current and voltage in accordance to Ohms law. Note that the slope gives the conductance of the semiconductor materials.

The inverse of the slope of I-V characteristics in Figure 3.13 gives the resistance, R of the semiconductor as shown in Equation (3.14).

$$R = \left(\frac{\Delta I}{\Delta V}\right)^{-1} = \frac{\Delta V}{\Delta I} = \rho\left(\frac{L}{A}\right) \tag{3.14}$$

where L, A and ρ are the thickness (cm), cross-sectional area (cm^2) and resistivity (Ωcm) of the semiconductor material respectively.

The material resistivity can then be obtained by re-arranging Equation (3.14) as

$$\rho = \left(\frac{RA}{L}\right) \tag{3.15}$$

The conductivity, σ of the semiconductor material measured in $(\Omega \cdot cm)^{-1}$ or $(S \cdot cm^{-1})$ is determined by finding the inverse of ρ in Equation (3.15).

3.6 Analytical techniques for device characterisation

After materials growth and characterisation, the next stage is to use the developed semiconductor materials for electronic device fabrication. Diode is the basic building block of any electronic device and solar cells are basically diodes when measured under dark condition. The basic techniques used for the diode and solar cell characterisation are current–voltage (I-V) and capacitance-voltage (C-V) techniques. With the application of external bias say from -1.0 V to +1.0 V, the current and capacitance signals can be measured. This section discusses the two basic techniques used in this research work for device characterisation; they are: current-voltage (I-V) and capacitance-voltage (C-V) analytical techniques.

3.6.1 I-V characteristics of a typical thin film solar cell

The main characteristic of the solar cell is called the I-V curve. Figure 3.14 (a) shows the equivalent circuit of solar cell using a single diode model. An ideal diode is expected to have a zero series resistance ($R_s=0$) and infinite shunt resistance ($R_{sh}\rightarrow\infty$) [35]. The solar cell in Figure 3.14 is represented by diode symbol *D*. For these types of diodes with infinite R_{sh}, the R_{sh} behaves like an open circuit as shown in Figure 3.14 (b) and this makes virtually all the currents coming from the light source to flow mainly

through the diode (solar cell) instead of going through both the solar cell and shunt resistor. In this case, an alternative path for current flow is avoided with the presence of infinite R_{sh}. For this reason, the total current at the output will be maximum. At low R_{sh} (Figure 3.14 (a)), current is lost to the shunt which ultimately leads to reduction in open-circuit voltage and fill factor. Low R_{sh} are due to defects that arise in the material during growth and they cause power losses [36]. The low R_{sh} provides alternative path for the current generated from photons to flow. According to Kirchhoff's law, the total generated current from photons divides into two, I_1 and I_2. I_1 goes through the solar cell represented by diode, D while I_2 goes through the shunt path.

The series resistance on the other hand reduces the FF, although high values of R_s can also lead to reduction in the short-circuit current density [37,38]. Low R_{sh} and high R_s leads to a gradual reduction in FF (shape of the IV curve) which ultimately affects the power output of the solar cell. If $R_s = 0$, there would be no voltage drop before the load. Figure 3.14 (c) indicates an ideal diode situation where the R_{sh} tends towards infinity and R_s tends to zero.

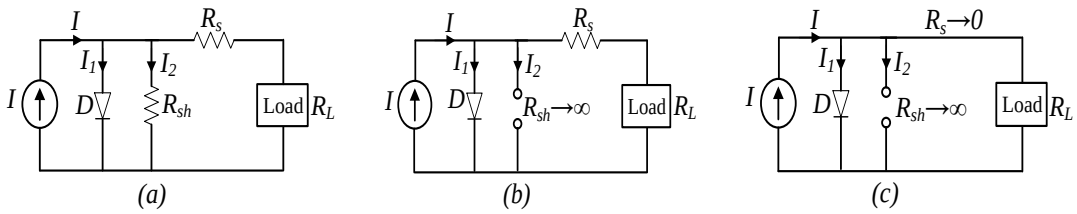


Figure 3.14. Typical schematic diagram showing the equivalent circuit of a solar cell using a single diode model.

It is important to measure the solar cell parameters under dark and illumination conditions so as to fully characterise the diode and photo-voltaic parameters. Under the dark condition, the diode parameters are obtained from the log-linear and linear-linear characteristics. The parameters obtained from Log I vs V curve are: rectification factor (RF), ideality factor (n), reverse saturation current (I_s), potential barrier height (ϕ_b); from the linear-linear I-V curve, the series resistance (R_s) and shunt resistance (R_{sh}) are obtained. Under illumination condition, the electronic parameters obtained are: open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF), conversion efficiency (η), series resistance and shunt resistance. The device parameters were obtained using Keithley 2401 sourcemeter with an embedded DC voltage source and AM1.5 solar simulator.

3.6.1.1 I-V characteristics of solar cell under dark condition

Under dark condition, the solar cell behaves like a diode either because of a rectifying Schottky junction formed between an n-type semiconducting material and a metal contact or because of junction formation between the n- and p-type semiconducting materials. The I-V characteristic of a Schottky type diode under dark condition is described by Equation (3.16) [35,39].

$$I_D = SA^*T^2.\exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \tag{3.16}$$

Or

$$I_D = I_S\left(\exp\left(\frac{qV}{nkT}\right)-1\right) \tag{3.17}$$

where $I_s = SA^*T^2.\exp\left(\frac{-q\phi_b}{kT}\right)$ (3.18)

Where I_D is the forward current in dark, I_s is the reverse saturation current derived from the extrapolation of the intercept of Log I at V = 0. V is the forward bias voltage, n is the ideality or junction quality factor, S is the surface area of the cell, A^* is the Richardson constant, q is the electronic charge ($1.6\text{x}10^{-19}$ C), T is the room temperature measured in Kelvin = 300 K and k is the Boltzmann constant = $1.38\text{x}10^{-23}$ JK^{-1}.

ϕ_b is the barrier height at the device interface and can be deduced from Equation (3.19) once I_s is determined from the intercept of the log-linear I-V curve.

$$\phi_b = \frac{kT}{q}\ln\left(\frac{SA^*T^2}{I_s}\right) \tag{3.19}$$

The Richardson constant for the semiconductor having effective mass m^* is given by Equation (3.20) [40].

$$A^* = \frac{4\pi m^* k^2 q}{h^3} \tag{3.20}$$

m^* is the effective mass of charge carriers and it varies from one semiconductor material to the other. For a p-type semiconductor, m^* is denoted as m_p^*; while for an n-

type semiconductor, m^* is represented as m_e^*. For instance, the effective electron mass of CdTe, m_e^* is $0.1m_o$ [41], $m_e^* = 0.21m_o$ is the effective electron mass for n-CdS, $m_p^* = 0.20m_o$ is the effective hole mass for p-ZnTe, m_o = 9.1 × 10^{-31} kg is the rest mass of electron and h = 6.626 × 10^{-30} cm^2kgs^{-1} is the Planck's constant. The Richardson constant for free electrons in n-CdTe using $m_e^* = 0.1m_o$ has been estimated from Equation (3.20) to be 12.0 $Acm^{-2}K^{-2}$.

$\exp\left(\frac{qV}{nkT}\right) \rangle\rangle 1$ when voltages applied externally across the diode is greater than or equal to 75 mV (V ≥ 75 *mV*) [42]. Therefore Equation (3.17) can be reduced to

$$I_D = I_S.\exp\left(\frac{qV}{nkT}\right) \tag{3.21}$$

Taking the ln of Equation (3.21)

$$\ln I_D = \ln I_S + \frac{qV}{nkT}$$

$$2.303\log_{10} I_D = 2.303\log_{10} I_S + \frac{qV}{nkT}$$

$$\log_{10} I_D = \log_{10} I_S + \frac{q}{2.303\times nkT}.V \tag{3.22}$$

Rearranging Equation (3.22) to resemble a straight line equation $Y = mx + C$

$$\log_{10} I_D = \frac{q}{2.303\times nkT}.V + \log_{10} I_S \tag{3.23}$$

From Equation (3.23), a plot of $\log_{10} I_D$ against V gives a slope, m of $\frac{q}{2.303\times nkT}$ and intercept of $\log_{10} I_S$ as shown in Figure 3.15. Equation (3.23) is thus very useful in analysing the I-V data measured under dark condition for a PV device. The ideality factor (n) of the diode can be calculated from the slope of the forward curve while I_s is found from the intercept on the $\log_{10} I$ axis.

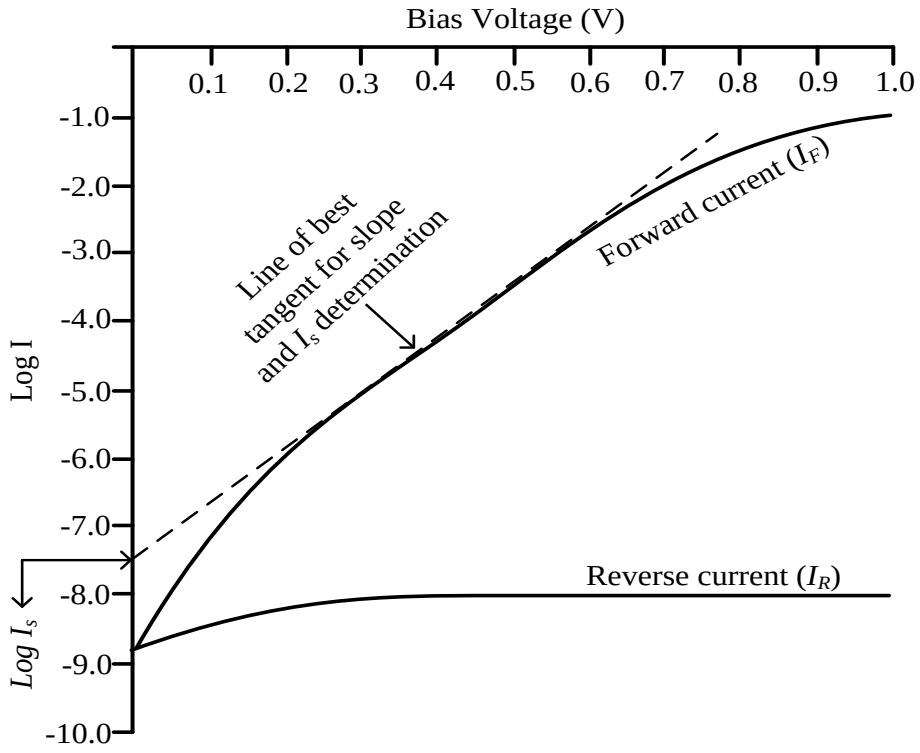


Figure 3.15. Typical log-linear I-V characteristic of diode under dark condition. The curves representing the forward current and reverse current have been indicated. Also, the intercept of the line of best tangent on the Log I axis is useful to determine the saturation current.

From Figure 3.15, slope = $\frac{\delta Log_{10} I}{\delta V} = \frac{q}{2.303 \times nkT}$ (3.24)

$$q = slope \times 2.303 nkT$$

$$n = \left(\frac{q}{kT}\right)\left(\frac{1}{slope \times 2.303}\right)$$

where $\frac{q}{kT} = \frac{1.6 \times 10^{-19}}{1.3806488 \times 10^{-23} \times 300} = \frac{1.6 \times 10^{-19+23}}{1.38 \times 300} = 38.647 \approx 38.65 \ \ CJ^{-1}$

$$n = 38.65 \ \times \left(\frac{1}{slope \times 2.303}\right) = 16.78 \ \times \left(\frac{1}{slope}\right)$$

$$n = 16.78\left(\frac{\delta V}{\delta(\log_{10} I)}\right) \quad (3.25)$$

From Equation (3.24)

$$q\delta V = 2.303nkT \times \delta \log_{10} I$$

$$q\delta V = \delta(\ln I)nkT$$

$$n = \frac{q}{kT}\left(\frac{\delta V}{\delta(\ln I)}\right)$$

$$n \cong 38.65\left(\frac{\delta V}{\delta(\ln I)}\right) \tag{3.26}$$

Equation (3.25) is used to calculate n when $\log_{10}(I)$ is plotted against V while Equation (3.26) is applicable in finding n value when ln (I) is plotted against V. The ideality factor (n) helps in determining the type of current transport that takes place over the potential barrier height. For example, in an ideal diode, current is transported mainly through thermionic emission of electrons over the potential barrier and this makes n to become 1.00 [40,43]. If n = 2.00, it means the current flow through Schottky junction takes place through recombination and generation (R&G) mechanisms within the device. Under this situation, the depletion region and the junction are full of R&G centres [35]. In real situation when working with practical electronic devices, the value of n can vary between 1.00 and 2.00 [44]; this implies that both thermionic emission with R&G process do take place in parallel.

The rectification factor (RF) is an important diode parameter that helps in determining the quality of a rectifying diode. It is the ratio of forward current to reverse current at a specified voltage. A RF of ~10^3 is adequate for application in some electronic devices such as diodes and solar cells [35]. The linear-linear I-V characteristics of diode illustrated in Figure 3.16 can be used to determine the R_s, R_{sh}, threshold voltage (V_T), breakdown voltage (V_{BD}). As earlier explained, an ideal diode must have zero R_s; while for a solar cell to be efficient, the value of the R_s must be kept to the barest minimum value. High value of R_s may be due to resistance contribution from the oxide layer formed at the interface between the metal and semiconductor [45], bulk resistance of the back-metal contact [44,46] and usage of a highly resistive semiconductor. The value of R_{sh} in a diode denotes the presence of current leakage paths in the diode. As shown in

Figure 3.16, R_s is determined by taking the slope of the I-V curve at the high end of the forward I-V curve while the slope taken at the high reverse end of the I-V curve gives the R_{sh}.

The threshold voltage or the turn-on voltage is the minimum voltage required to turn on a diode [39] and the value varies from one semiconductor material to the other [47–49]. The V_T must be overcome for diodes to be able to conduct in forward direction. Breakdown voltage occurs in the reverse bias region of the diode and it happens when a large reverse current flows through the diode. Under ideal situation, large currents are supposed to flow through the diode when forward biased because diode is a unidirectional device which allows currents to pass through it in only one direction. Due to this unique feature, currents are not allowed to flow through an ideal diode when reverse biased. However, since most fabricated diodes are not ideal in their electronic behaviour, they can permit negligible or small amount of currents called reverse saturation current to flow through. But when high voltage which results to high field is applied to the diode, a large reverse current flows through the p-n junction thereby causing the diodes to breakdown [39].

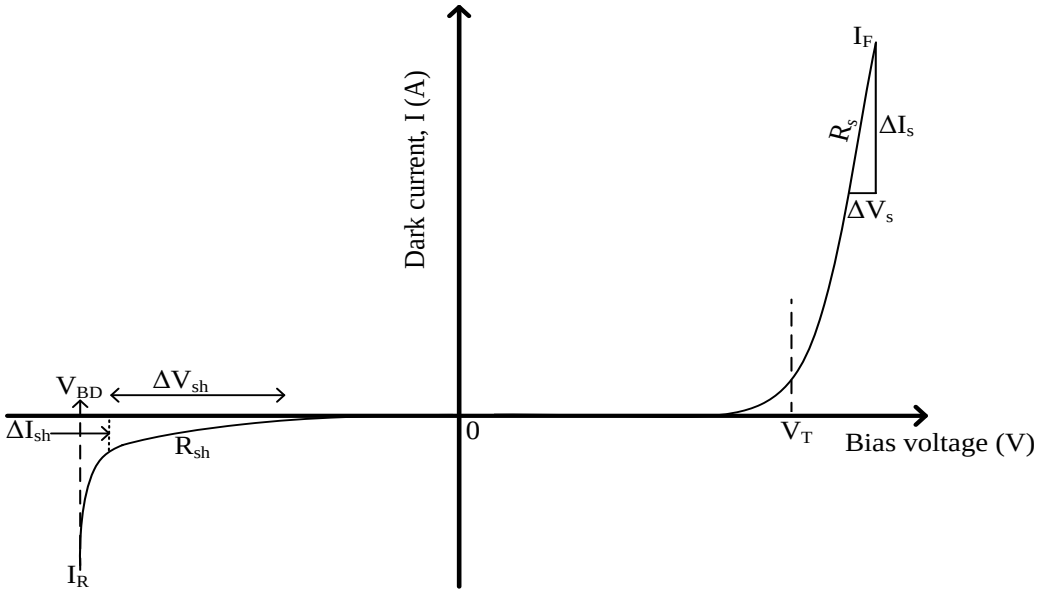


Figure 3.16. Determination of breakdown voltage, threshold voltage, series and shunt resistance from typical linear-linear I-V characteristics of a diode under dark condition.

3.6.1.2 I-V characteristics of solar cell under illumination condition

It is important to be acquainted with what happens to solar cells under illumination condition. When a solar cell is illuminated as shown in Figure 3.17 (a), it behaves as a diode with current source parallel to the diode junction as illustrated in Figure 3.17 (b) [39]. The current generated from the solar cell after shining light on it is known as photo-generated currents. Under illumination condition, the equivalent circuit of an ideal solar cell has zero R_s and infinite R_{sh}.

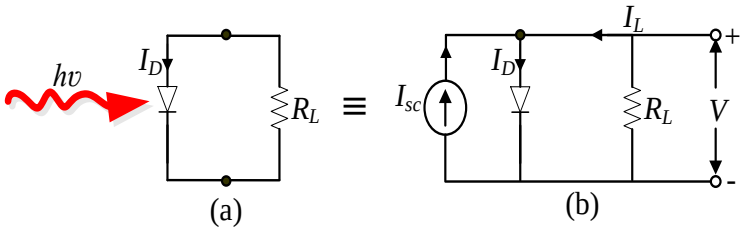


Figure 3.17. (a) Ideal solar cell under illumination and (b) Equivalent circuit of ideal solar cell under illumination after representing the effect of photons with current source.

The resultant current (I_L) of the ideal solar cell under illumination as deduced from Figure 3.17 (b) is given by Equation (3.27) [39].

$$I_L = I_D - I_{SC} \tag{3.27}$$

The direction of the photo-generated current (I_{SC}) is opposite to the direction of diode forward current in dark as indicated by the negative sign in Equation (3.27). Substituting Equation (3.17) into Equation (3.27) yields Equation (3.28).

$$I_L = I_D - I_{SC} = I_S\left(\exp\left(\frac{qV}{nkT}\right)-1\right) - I_{SC} \tag{3.28}$$

The three important parameters that determine the efficiency (η) of solar cell are open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}) and fill factor (FF). The V_{oc} is the potential measured when current does not flow in the external circuit; that is when the current, I_L in Equation (3.28) becomes zero. This can be obtained directly from Figure 3.18 at I_L=0 where the I-V curve intercept the X-axis. The short-circuit current (I_{sc}) is photo-generated current that flows through the cell when the voltage across the two electrical contacts is zero or when the two contacts are short-circuited. I_{sc} can be obtained directly from Figure 3.18 at V=0 where the I-V curve intercept the Y-axis.

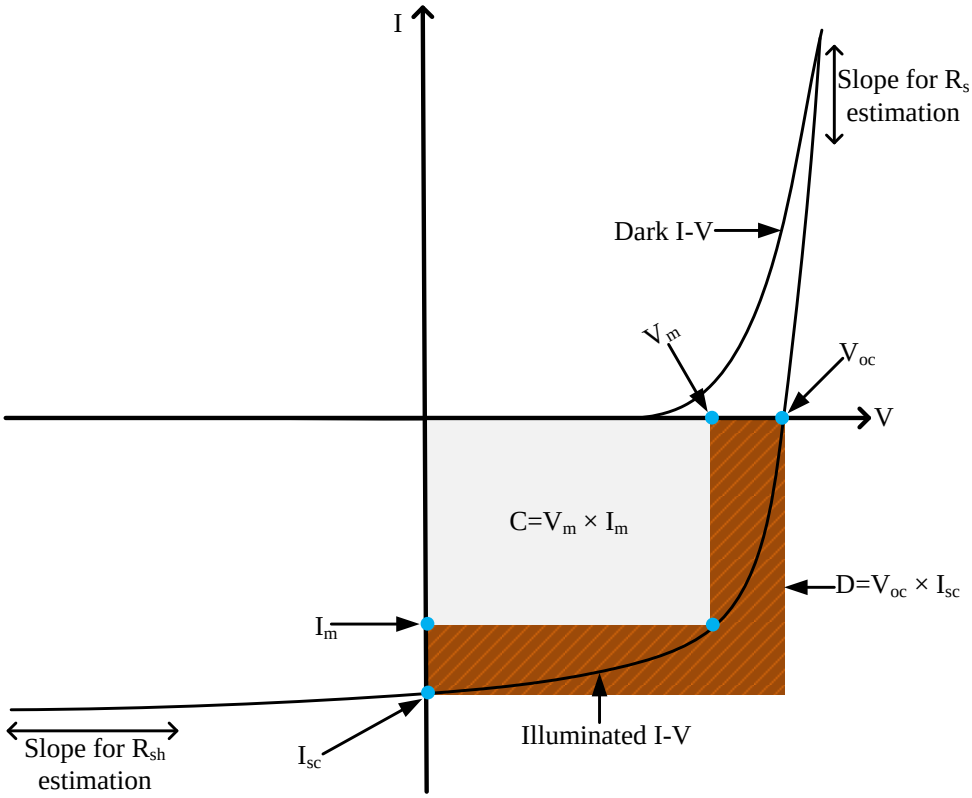


Figure 3.18. A typical I-V characteristic of solar cell measured under dark and illuminated conditions.

The third parameter of a solar cell is the fill factor (*FF*) and it is the fraction of electrical power that can be extracted from the solar cell. *FF* also gives the squareness of the I-V curve of the solar cell as shown in Figure 3.18 and it is defined as the ratio of the maximum power output, P_{max} to the product of I_{sc} and V_{oc} as expressed in Equation (3.29).

$$FF = \frac{P_{\max}}{V_{oc} I_{sc}} = \frac{V_m I_m}{V_{oc} I_{sc}} = \frac{area\ \ C}{area\ \ D} \tag{3.29}$$

The conversion efficiency (η) of the solar cell which explains the overall performance of the solar cell is defined as the ratio of the maximum power output ($P_{\max}$) to the total incident power (P_{in}) according to Equation (3.30) [39].

$$\eta = \frac{P_{\max}}{P_{in}} = \frac{V_m I_m}{P_{in}} \tag{3.30}$$

The conversion efficiency in terms of V_{oc}, I_{sc} and *FF* can be obtained by combining Equations (3.29) and (3.30).

$$\eta = \frac{FF \times V_{oc} \times I_{sc}}{P_{in}} \tag{3.31}$$

where $P_{in} = 100 \ \ mWcm^{-2}$ is the solar power incident on a unit area under the standard AM1.5 illumination condition.

For a unit area of the solar cell, the short circuit current, I_{sc} is replaced by the short circuit current density J_{sc} as stated in Equation (3.32). Conventionally, the unit of J_{sc} is expressed in $mAcm^{-2}$.

$$J_{sc} = \frac{I_{sc}}{A} \tag{3.32}$$

Thus, Equation (3.31) becomes

$$\eta = \frac{FF \times V_{oc} \times J_{sc}}{P_{in}} \tag{3.33}$$

3.6.2 Capacitance-voltage (C-V) technique

Electronic parameters of thin film semiconductor devices such as depletion capacitance at zero bias (C_o), the doping concentration of the acceptors (N_A) and donors (N_D) can be found using C-V technique. Other quantities which can be deduced from the initially obtained parameters of C-V plot are: the diffusion potential (V_{bi}), energy difference between the Fermi level (E_F) and the bottom of the conduction band edge (E_C) ($\Delta E = E_C - E_F$), the energy difference between the Fermi level (E_F) and the top of the valence band edge (E_V) ($\Delta E = E_F - E_V$) and the depletion width (W). The C-V measurements can be carried out at room temperature or temperatures either below or above it. For all the experimental results discussed in this thesis, CV measurements were carried out at room temperature and bias voltage of -1.0 to +1.0 V. CV measurements are also better carried out at a higher frequency (say 1 MHz) to reduce defect interference. This is because at low frequency, presence of defects in the material does affect the measured capacitance due to contribution from defects.

Equation (3.34) [50] is applicable for a p-n junction diode where we have both the acceptors and donors. The doping density (N) of the n-type semiconductor and p-type semiconductor can be estimated from the junction capacitance shown in Equation (3.35). While applying Equation (3.35) to device structures fabricated from n-type

semiconductor, the doping density (N) becomes a donor concentration (N_D-N_A) while N also becomes acceptor concentration (N_A-N_D) for device structures fabricated from p-type semiconductor [7].

For a one-sided p-n junction diode, Equation 3.34 can be further modified to resemble Equation (3.36) and (3.37) depending on the application. For a p^+n junction diode where $N_A \gg N_D$, the doping density N becomes N_D; in this case, Equation (3.34) can be simplified to Equation (3.36). Likewise N becomes N_A if $N_D \gg N_A$ (n^+p) as shown in Equation (3.37). These various applications thus allow Equation (3.34) to be modified accordingly. Using Equation (3.35), a graph of C^{-2} versus V is plotted to estimate the value of N, and the built-in potential (V_{bi}) can be obtained from the intersection of C^{-2} versus V curve on bias voltage axis. A graph of C^{-2} versus V is called Mott-Schottky plot, which finds application in metal semiconductor (MS) devices and one-sided p-n junction diodes [50].

Under an ideal situation, a plot of C^{-2} versus V is supposed to give a linear graph as shown in Figure 3.19 (a). However, the presence of surface states, traps, and non-uniformity of doping in the semiconductor material makes the Mott-Schottky plots to deviate from linearity as illustrated in Figure 3.19 (b) [7,51]. The Mott-Schottky plots presented in Chapters 4, 5, 7, 8 and 9 of this thesis deviate from linearity and these could be attributed to factors such as surface states and non-uniformity of doping in the electroplated semiconductors used in this research. The deviation from linearity thus implies that the theory developed for a simple depletion region is not fully applicable for more complex systems.

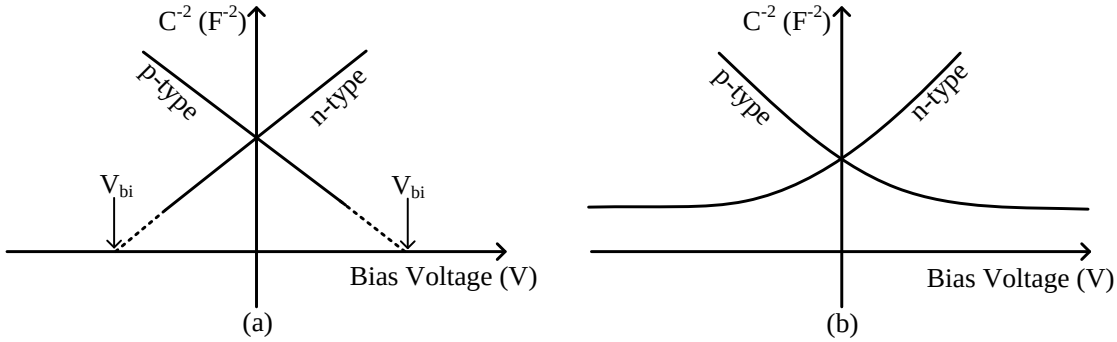


Figure 3.19. Mott-Schottky plots of n- and p-type semiconductors (a) for an ideal diode and (b) non-ideal diode due to presence of surface states and defects.

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R) \times (N_A + N_D)}{e\varepsilon_s NA^2 \times (N_A N_D)} \tag{3.34}$$

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\varepsilon_s N A^2} \tag{3.35}$$

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\varepsilon_s N_D A^2} \quad \text{if } N_A \gg N_D \quad \{p^+n\} \tag{3.36}$$

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\varepsilon_s N_A A^2} \quad \text{if } N_D \gg N_A \quad \{n^+p\} \tag{3.37}$$

In the above equations, V_R is the reverse bias voltage, V_{bi} is the built-in potential, e is the charge on electron, C is the measured capacitance in Farad (F), ε_s is the permittivity of semiconductor and A is the area of the p-n junction diode, N_A is the acceptor density (or the concentration of free holes at room temperature) and N_D is the donor density (or the concentration of free electrons at room temperature).

The effective width (W) of the depletion region of fabricated Schottky diodes or p-n junction diodes can be estimated from Equation (3.38).

$$W = \frac{\varepsilon_r \varepsilon_o A}{C} \tag{3.38}$$

Where ε_r is the relative permittivity of the material (ε_r is 10.2 for CdSe, 8.9 for CdS, 8.9 for ZnS [52], 10.4 for ZnTe [53] and 11.0 for CdTe [41]), ε_o is the permittivity of vacuum, A is the diode area, C is the measured capacitance at zero bias and W is the depletion width. For a fully depleted device, the depletion width is almost equal to thickness of the thin film. The depletion region forms the heart of a basic electronic device; this is where electric field is being created as a result of separation of positive and negative space charges.

The depletion width, W can also be expressed as shown in Equation (3.39) [44].

$$W = X_p + X_n = \left(\left(\frac{2\varepsilon_s V_{bi}}{e} \right) \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \right)^{0.5} \tag{3.39}$$

$$X_p = \left(\frac{2\varepsilon_s V_{bi}}{e N_A} \right)^{0.5} \tag{3.40}$$

$$X_n = \left(\frac{2\varepsilon_s V_{bi}}{e N_D} \right)^{0.5} \tag{3.41}$$

Where X_p and X_n are the distances by which the depletion region extends into the p- and n-type semiconductors respectively.

Equation (3.40) is applicable to n^+p junction diodes where the doping concentration in the n-region is much greater than that of the p-region ($N_D >> N_A$). In n^+p junction diodes, $X_n << X_p$; therefore the total depletion width, $W \approx X_p$. In the same way, Equation (3.41) can be used to determine the depletion width in a p^+n junction diodes where the doping concentration in the p-region is much greater than that of the n-region ($N_A >> N_D$) [43]. In p^+n junction diodes, $X_p << X_n$; therefore the total depletion width, $W \approx X_n$.

Having determined W and X_p from Equation (3.38) and (3.40) respectively, X_n can then be found by using Equation (3.39). For n^+p junction diodes where the concentration of holes in the valence band (acceptor density) is determined from the Mott-Schottky plots, the donor density (N_D) can then be estimated by substituting known values of X_n and V_{bi} into Equation (3.41). As earlier discussed, Equation (3.38) can be used in calculating the total depletion width for the p-n junction diode by using the depletion capacitance obtained from C-V plot. The estimated result from Equation (3.38) can only correspond to that obtainable from Equation (3.39) if the right V_{bi} value is used. The V_{bi} is found by extrapolating the Mott-Schottky curve to the bias voltage axis at C^{-2}=0. [39]. The V_{bi} can therefore be accurately determined if the C^{-2} (F^{-2}) axis of the Mott-Schottky plot starts from the origin. Alternatively, the V_{bi} can be theoretically determined by applying Eqn. (3.51).

The effective density of states depends on temperature and the nature of semiconductor material and this makes the value to vary from one semiconductor material to the other. The concept of effective mass is useful in modelling the temperature dependence of N_C; this allows Equations (3.42) and (3.43) to be used over a range of temperatures [39].

The effective density of states in the conduction band edge of semiconductor is given by

$$N_C = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2} \tag{3.42}$$

Where m_e^* is the effective electron mass of n-type semiconductor, $m_o = 9.1 \times 10^{-31}$ kg is the rest mass of electron and $h = 6.626 \times 10^{-30}$ cm^2kgs^{-1} is the Planck's constant.

The effective density of states in the valence band edge of semiconductor is given by

$$N_V = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \tag{3.43}$$

Where m_p^* is the effective hole mass of p-type semiconductor.

The Fermi-Dirac probability function of electrons occupying the donor state is given by [50]

$$n = \frac{N_C}{1+\frac{1}{g}\exp\left(\frac{E_C - E_F}{kT}\right)} \tag{3.44}$$

Where E_C is the lowest energy of the conduction band, E_F is the Fermi level and g is called a degeneracy factor ~2.00 for donor atoms and ~4.00 for acceptor atoms [44,54].

From Equation (3.44), $\Delta E = E_C - E_F = 0.693kT\ln\left(\frac{N_C}{n}\right)$ (3.45)

Equation (3.45) is therefore a very useful relationship to determine the position of Fermi level in a degenerate n-type semiconductor. For non-degenerate semiconductors where the doping density is less than the effective density of states, the degeneracy factor, g in the Fermi-Dirac function is not being considered. Therefore Equation (3.44) reduces to,

$$\Delta E = E_C - E_F = kT\ln\left(\frac{N_C}{n}\right) \tag{3.46}$$

Equation (3.46) is an approximation of the Fermi-Dirac function and is mostly applied to determine the Fermi level position of a non-degenerate n-type semiconductor. It should be noted that $n = N_D$ if all impurity atoms are ionised. For a non-degenerate p-type semiconductor, Equation (3.46) can be re-written as,

$$\Delta E = E_F - E_V = kT\ln\left(\frac{N_V}{p}\right) \tag{3.47}$$

E_F - E_V is the difference in energy (ΔE) between the Fermi level and the top of the valence band and p is the hole concentration.

For a p-n junction diode, the electric field, *E* in the semiconductor at the interface is given by,

$$\mathrm{E}(x=0)=\frac{eW}{\varepsilon_s}\quad\left(\frac{N_A\times N_D}{N_A+N_D}\right) \tag{3.48}$$

For Schottky diodes fabricated from n-type and p-type semiconductors, the electric fields in the semiconductor at the M/S interface are given by Equations (3.49) and (3.50) respectively. Equations (3.49) and (3.50) are also applicable to p^+n and n^+p junction diodes respectively [39].

$$\mathrm{E}(x=0)=\frac{eX_nN_D}{\varepsilon_s} \tag{3.49}$$

$$\mathrm{E}(x=0)=\frac{eX_pN_A}{\varepsilon_s} \tag{3.50}$$

As explained by Sze and Ng [39], most of the built-in potential and depletion region are inside the lightly doped region of the one-sided p-n junction diode. Therefore, the magnitude of the built-in potential for one-sided junction diode can be estimated using Equation (3.51) [39,49].

$$|V_{bi}|=\frac{|E_{\max}|}{2}(W) \tag{3.51}$$

3.7 Summary

Substrates selection and preparation, and the basic electrodeposition growth technique used in this work have been discussed. Also, some of the analytical techniques for material characterisation have been briefly explained. The end result of every material being investigated and analysed with the characterisation techniques is to employ them in device fabrication. For this reason, brief explanations have been given on the two basic techniques used in this work for device characterisation; the two analytical techniques are I-V and C-V measurement techniques.

References

[1] D. J. Kwak, B. H. Moon, D. K. Lee, C. S. Park, Y. M. Sung, J. Electr. Eng. Technol., **6** (2011) 684–687.

[2] http://www.sigmaaldrich.com/materials-science/material-science-products.html?TablePage=106837645 (accessed May 7, 2016).

[3] K. Osborne, VIII-Metals-G-Electroplating, (2011) 1–8. http://nzic.org.nz/ChemProcesses/metals/8G.pdf (accessed May 9, 2016).

[4] I. M. Dharmadasa, J. Haigh, J. Electrochem. Soc., **153** (2006) G47–G52.

[5] S. Bonilla, E. A. Dalchiele, Thin Solid Films, **204** (1991) 397–403.

[6] D. Cunningham, M. Rubcich, D. Skinner, Prog. Photovoltaics Res. Appl., **10** (2002) 159–168.

[7] R. K. Pandey, S. N. Sahu, S. Chandra, Handbook of Semiconductor Electrodeposition, first ed., Marcel Dekker Inc., New York (1996).

[8] S. Dennison, J. Mater. Chem., **4** (1994) 41–46.

[9] M. Paunovic, M. Schlesinger, Fundamentals of Electrochemical Deposition, second ed., John Wiley & Sons, Inc., Hoboken, New Jersey (2006).

[10] R. G. Ehl, A. J. Ihde, J. Chem. Educ., **31** (1954) 226–232.

[11] Y. G. Gudage, N. G. Deshpande, R. Sharma, J. Phys. Chem. Solids, **70** (2009) 907–915.

[12] D. G. Diso, G. E. a. Muftah, V. Patel, I. M. Dharmadasa, J. Electrochem. Soc., **157** (2010) 647–651.

[13] J. Koryta, J. Dvorak, L. Kavan, Priciples of Electrochemistry, second ed., John Wiley & Sons, Ltd., Chichester, West Sussex, England (1993).

[14] M. Grätzel, Nature, **414** (2001) 338–344.

[15] D. G. Diso, F. Fauzi, O. K. Echendu, A. R. Weerasinghe, I. M. Dharmadasa, J. Phys. Conf. Ser., **286** (2011) 12040.

[16] http://teaching.shu.ac.uk/hwb/chemistry/tutorials/molspec/uvvisab3.htm (accessed April 30, 2016).

[17] http://teaching.shu.ac.uk/hwb/chemistry/tutorials/molspec/beers1.htm (accessed April 30, 2016).

[18] J. Tauc, Amorphous and Liquid Semiconductors, Plenum Press, London (1974).

[19] http://serc.carleton.edu/research_education/geochemsheets/techniques/XRD.html (accessed April 24, 2016).

[20] http://www.doitpoms.ac.uk/tlplib/xray-diffraction/intro.php (accessed April 24, 2016).

[21] A. Monshi, World J. Nano Sci. Eng., **2** (2012) 154–160.

[22] P. Nandakumar, C. Vijayan, M. Rajalakshmi, A. K. Arora, Y. V. G. S. Murti, Phys. E, **11** (2001) 377–383.

[23] G. S. Bumbrah, R. M. Sharma, Egypt. J. Forensic Sci., **6** (2016) 209–215.

[24] M. von Ardenne, Improvements in electron microscopes, Germany (1937). https://en.wikipedia.org/wiki/Scanning_electron_microscope.

[25] I. Guwahati, Microsc. Tech., http://nptel.ac.in/courses/102103044/18 (accessed May 1, 2016).

[26] http://www.nanoscience.com/products/sem/technology-overview/ (accessed May 1, 2016).

[27] P. D. Ngo, Energy Dispersive Spectroscopy, in: Fail. Anal. Integr. Circuits, Kluwer Academic Publishers, (1999).

[28] D. Vaughan,ed., An Introduction to Energy-Dispersive X-ray Microanalysis, Noran Instruments, Middleton, Wisconsin (1999).

[29] I. Guwahati, Energy Dispersive Spectrom., http://nptel.ac.in/courses/103103026/18 (accessed May 5, 2016).

[30] https://en.wikipedia.org/wiki/Energy-dispersive_X-ray_spectroscopy (accessed May 6, 2016).

[31] D. P. Woodruff, T. Delchar, Modern Techniques of Surface Science, Cambridge University Press, (1994). https://www2.warwick.ac.uk/fac/sci/physics/current/postgraduate/regs/mpags/ex5/techniques/electronic/ups/ (accessed May 6, 2016).

[32] I. M. Dharmadasa, O. K. Echendu, F. Fauzi, H. I. Salim, N. A. Abdul-Manaf, J. B. Jasinski, A. Sherehiy, G. Sumanasekera, J. Mater. Sci. Mater. Electron., **27** (2016) 5039–5046.

[33] R. S. Quimby, An Introduction to Photonics and Lasers, John Wiley & Sons, Inc., Hoboken, New Jersey (2006).

[34] http://www.chem.qmul.ac.uk/surfaces/scc/scat5_3.htm (accessed May 6, 2016).

[35] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[36] C. Honsberg, S. Bowden, http://www.pveducation.org/pvcdrom/solar-cell-operation/shunt-resistance (accessed January 13, 2016).

[37] C. Honsberg, S. Bowden, http://www.pveducation.org/pvcdrom/solar-cell-operation/series-resistance (accessed January 13, 2016).

[38] M. A. Green, Solid State Electron., **20** (1977) 265–266.

[39] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New Jersey (2007).

[40] E. H. Rhoderick, IEE Proc. I Solid State Electron Devices, **129** (1982) 1–14.

[41] J. R. Pugh, D. Mao, J. G. Zhang, M. J. Heben, A. J. Nelson, A. J. Frank, J. Appl. Phys., **74** (1993) 2619–2625.

[42] E. H. Rhoderick, R. H. Williams, Metal-Semiconductor Contacts, 2nd ed., Oxford Science Publications, Oxford, United Kingdom (1988).

[43] T. Soga, Nanostructured Materials for Solar Energy Conversion, in: Nanostructured Mater. Sol. Energy Convers., first ed., Elsevier, (2006).

[44] J. L. Gray, The Physics of the Solar Cell, in: Handb. Photovolt. Sci. Eng., first ed., John Wiley & Sons, Ltd., Chichester, West Sussex, England (2003): pp. 61–

112.

[45] A. Keffous, M. Siad, S. Mamma, Y. Belkacem, C. Lakhdar Chaouch, H. Menari, A. Dahmani, W. Chergui, Appl. Surf. Sci., **218** (2003) 337–343.

[46] A. Rohatgi, S. A. Ringel, R. Sudharsanan, P. V Meyers, C. H. Liu, V. Ramanathan, Sol. Cells, **27** (1989) 219–230.

[47] O. I. Olusola, M. L. Madugu, I. M. Dharmadasa, Mater. Res. Innov., **19** (2015) 497–502.

[48] O. I. Olusola, O. K. Echendu, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., **26** (2014) 1066–1076.

[49] V. Kabra, L. Aamir, M. M. Malik, Beilstein J. Nanotechnol., **5** (2014) 2216–2221.

[50] D. A. Neamen, Semiconductor Physics and Devices: Basic Principles, third ed., McGraw-Hill, New York (2003).

[51] I. M. Dharmadasa, N. B. Chaure, A. P. Samantilleke, A. Hassan, Sol. Energy Mater. Sol. Cells, **92** (2008) 923–928.

[52] A. Rockett, The Materials Science of Semiconductors, Springer Science and Business Media, LLC, New York, USA (2008).

[53] J. C. Irwin, J. Lacombe, J. Appl. Phys., **41** (1970) 1444–1450.

[54] Y. Masumoto, H. Umino, J. Sun, E. Suzumura, Phys. Chem. Chem. Phys., **17** (2015) 25278–25282.

Chapter 4 - Growth and characterisation of CdSe thin films

4.1 Introduction

CdSe is a well-known II-VI semiconductor that can crystallise in either wurtzite (hexagonal) or the zinc blende (cubic) structure. It is a direct bandgap semiconductor material which is used in opto-electronic devices, light-emitting diodes (LEDs), field-effect transistors (FETs), biosensors, biomedical imaging and solar cells fabrication [1]. CdSe is an n-type semiconductor with a bandgap of ~1.80 eV in the wurtzite crystal phase and ~1.71 eV in the zinc blende phase [2,3]. According to Böhmler et al. [3], the energy bandgap values are dependent on the crystal phase of the thin films. The deposition of CdSe thin film has been achieved using different growth methods such as pulsed laser deposition [4], thermal vacuum evaporation [5], chemical bath deposition (CBD) [4,6], spray pyrolysis [7] and electrodeposition [8–10].

This chapter describes the cathodic electrodeposition of CdSe thin films on FTO-coated glass substrates using two-electrode system and aqueous acidic electrolyte. The material properties of ED-CdSe layers were studied using some of the analytical techniques discussed in Chapter 3. The effects of pH variation of the CdSe electrolyte on its optoelectronic properties have also been explored. The electronic qualities of the electrodeposited CdSe layers were tested using the device structure glass/FTO/n-CdSe/metal contact and the results are reported in this thesis. Overall, the aim of this work is to study the material and electronic properties of CdSe thin films under different deposition conditions so as to know the areas where it can best be applied in terms of electronic device fabrication.

4.2 Preparation of CdSe electrolytic bath

The precursors used for the growth of CdSe thin films were 0.3M $CdCl_2$ as Cd^{2+} source and 0.003M SeO_2 as Se^{2-} source in 400 ml of de-ionised water. All chemicals used for electrodeposition were analytical reagent grade of purity 5N (99.999%) from Sigma Aldrich. The growth temperature and pH of the bath used for the optimisation of the growth voltage were approximately 80^{o}C and 2.20±0.02 respectively. The pH of the bath was adjusted accordingly by adding ammonia or HCl solution. The 2.20±0.02 pH

was the initial pH used for CdSe characterisation before optimising the pH to grow a nearly stoichiometric CdSe layer for electronic device application. The glass/FTO used in this work was TEC-15 with a sheet resistance of ~13 Ω/□ and the electroplating of CdSe was carried out in potentiostatic mode using a 2-electrode system set-up.

4.3 Voltage optimisation and growth of CdSe thin films

In this section, some analytical techniques used in determining suitable cathodic deposition potentials range for the growth of nearly stoichiometric CdSe layers and for material characterisations have been explored. To obtain a suitable deposition potential for the CdSe layers, other preparative parameters such as the growth temperature, pH and growth time (t_g) were kept constant at 80^oC, 2.20±0.02 and five minutes respectively.

4.3.1 Cyclic voltammogram

A suitable voltage range to grow nearly stoichiometric CdSe thin films was obtained using cyclic voltammogram. A range of cathodic potentials from 0 to 2000 mV was applied through the electrodes immersed in the electrolyte at a sweep rate of 3 $mVsec^{-1}$. The initial pH of the solution and deposition temperature was maintained at 2.20±0.02 and ~80^oC respectively. Cyclic voltammograms were obtained for the electrochemical reactions in solutions of 0.3M $CdCl_2$, 0.003M SeO_2 and mixture of 0.3M $CdCl_2$ + 0.003M SeO_2 each in 400 ml of de-ionised water to determine the approximate deposition voltages for Cd, Se and CdSe respectively.

4.3.1.1 Cyclic voltammogram of 0.3M $CdCl_2$

0.3M $CdCl_2$ was prepared using 400 ml of de-ionised water and the pH of the first solution was measured to be 3.79±0.02 at room temperature; this pH was adjusted to 2.20±0.02 by the addition of HCl solution. The first voltammogram of the $CdCl_2$ solution as shown in Figure 4.1 was taken to help in determining the potential at which the Cd deposition and dissolution take place. From Figure 4.1, the first hump appears at a cathodic potential of ~910 mV; this shows that Cd begins to deposit at this potential. In the reverse direction of the curve, the transition point from the positive current density axis to the negative is ~1440 mV; this voltage is an indication of the potential at which Cd dissolution begins to dominate. In fact, at ~1440 mV, equal amounts of Cd deposition and dissolution take place and hence the resultant current becomes zero. The

reduction of Cd^{2+} to Cd on the surface of FTO electrode takes place according to Equation (4.1), and the current flow is in the forward direction. However, the dissolution of Cd takes place according to Equation (4.2) and the current produced is in the opposite direction.

$$Cd^{2+} + 2e^{-} \rightarrow Cd \quad (4.1)$$

$$Cd \rightarrow Cd^{2+} + 2e^{-} \quad (4.2)$$

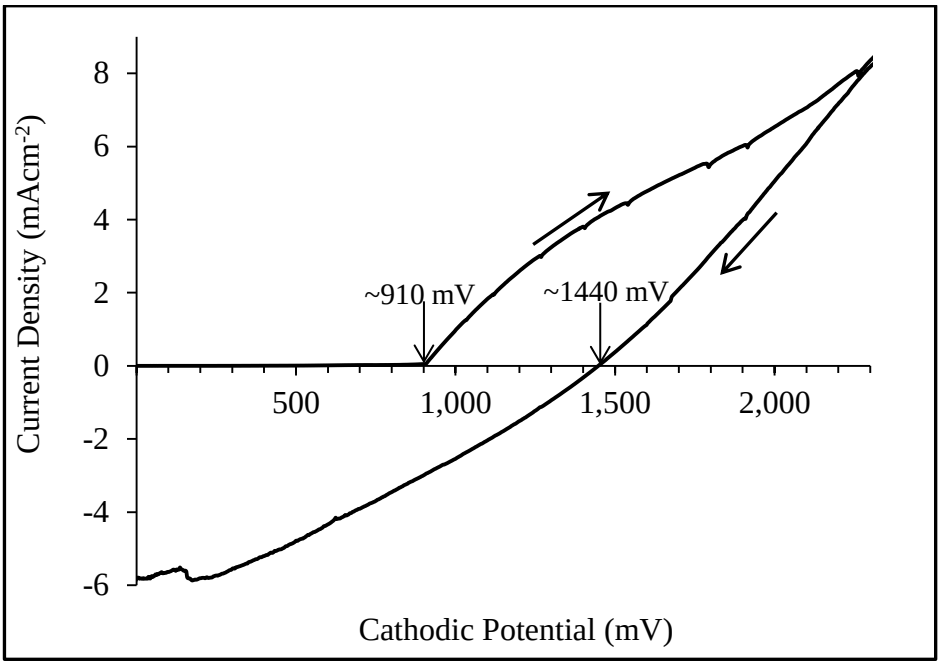


Figure 4.1. A typical cyclic voltammogram of electrolyte containing 0.3M of $CdCl_2$ aqueous solution (pH = 2.20±0.02, T = 80^{o}C).

4.3.1.2 Cyclic voltammogram of 0.003M SeO_2

A cyclic voltammogram of 0.003M SeO_2 of aqueous solution is shown in Figure 4.2 and the corresponding chemical reaction is described in Equation (4.3). In the forward curve (Figure (a) at the inset of Figure 4.2), the first hump appears at a cathodic potential ~178 mV; this voltage is an indication of the potential at which Se deposition begins. According to Pawar et al. [11], this reduction peak is as a result of the irreversible reaction shown in Equation (4.4). Se dissolution begins to dominate at ~589 mV (this is shown in Figure (b) at the inset of Figure 4.2).

$$SeO_2 + H_2O \rightarrow H_2SeO_3 \quad (4.3)$$

$$H_2SeO_3 + 4H^{+} + 4e^{-} \rightarrow Se + 3H_2O \quad (4.4)$$

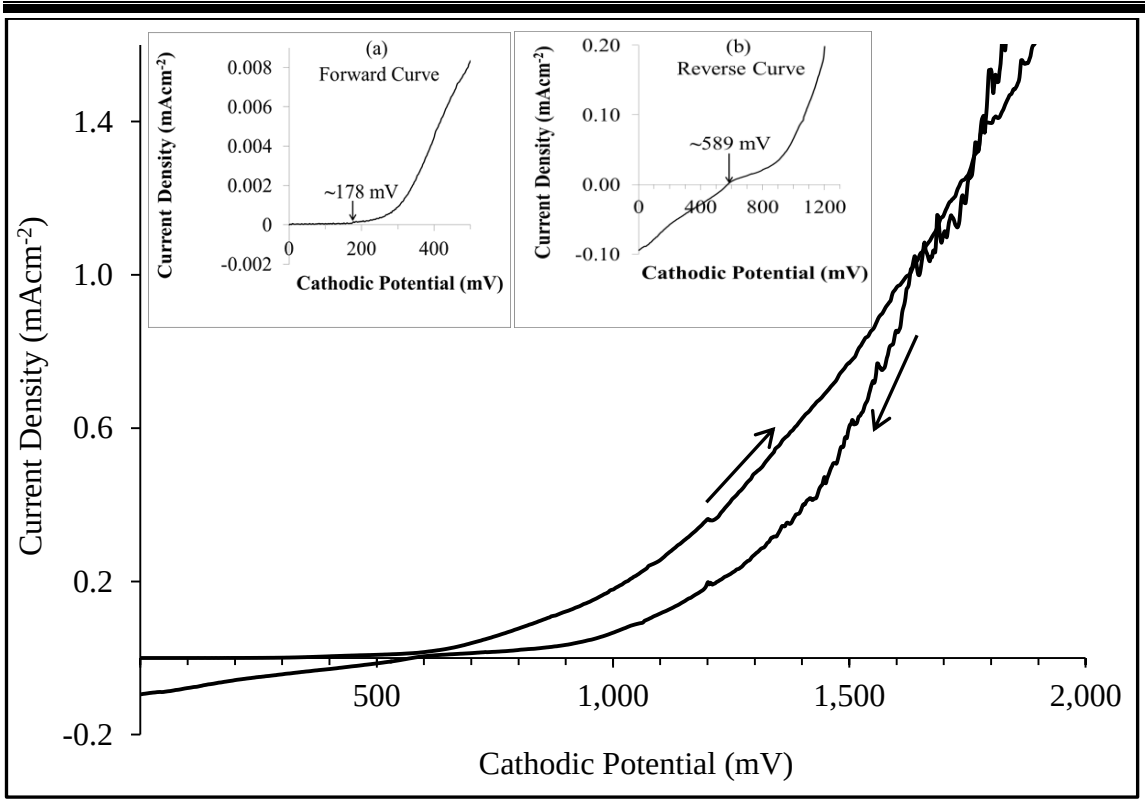


Figure 4.2. A typical cyclic voltammogram of electrolyte containing 0.003M of SeO_2 aqueous solution (pH = 2.20±0.02 and T = 80^oC).

4.3.1.3 Cyclic voltammogram of mixture of 0.3M $CdCl_2$ + 0.003M SeO_2

Figure 4.3 shows the cyclic voltammogram measured for glass/FTO electrode in an aqueous solution containing a mixture of 0.3M $CdCl_2$ and 0.003M SeO_2. It is also worth noting that the minimum standard reduction potential for electrolysis of water molecules is about 1230 mV [12]. The discharging of most active H atoms at the cathode while CdSe is forming is an excellent built-in method to passivate defects in the CdSe layer. However, if H_2 bubbles are formed at the cathode, it could have a detrimental effect of delamination of the semiconducting layer. The redox potential (E^o) of Se and Cd are +0.74 and -0.40 V respectively [13]. From the redox potential values, Se shows a more positive redox potential than Cd; for this reason, Se is therefore expected to deposit before Cd.

The forward curve illustrated at the inset of Figure 4.3 (Figure (a)) shows that Se begins to deposit at ~440 mV while Figure (b) at the inset of Figure 4.3 shows that Cd begins to deposit at ~1080 mV. The sudden rise in deposition current at 1080 mV to 1800 mV shows the beginning of reaction between Cd and Se to form CdSe. In this region, the layer formed is a mixture of CdSe and elemental Se thus giving rise to a Se-rich CdSe

layer. Beyond 1800 mV, a sharp rise is noticed in the deposition current. This leads to a gradual decrease in the amount of elemental Se because more Cd is incorporated into the CdSe layer. As the growth voltage further increases, the amount of elemental Se in the CdSe layer gradually reduces thus giving rise to stoichiometric formation of CdSe layer in the voltage range between 1900 to 2000 mV. Beyond 2000 mV, formation of Cd dendrites was observed. The Cd dendrites formation shows that at voltages ≥2000 mV, the CdSe layer formed is a Cd-rich material.

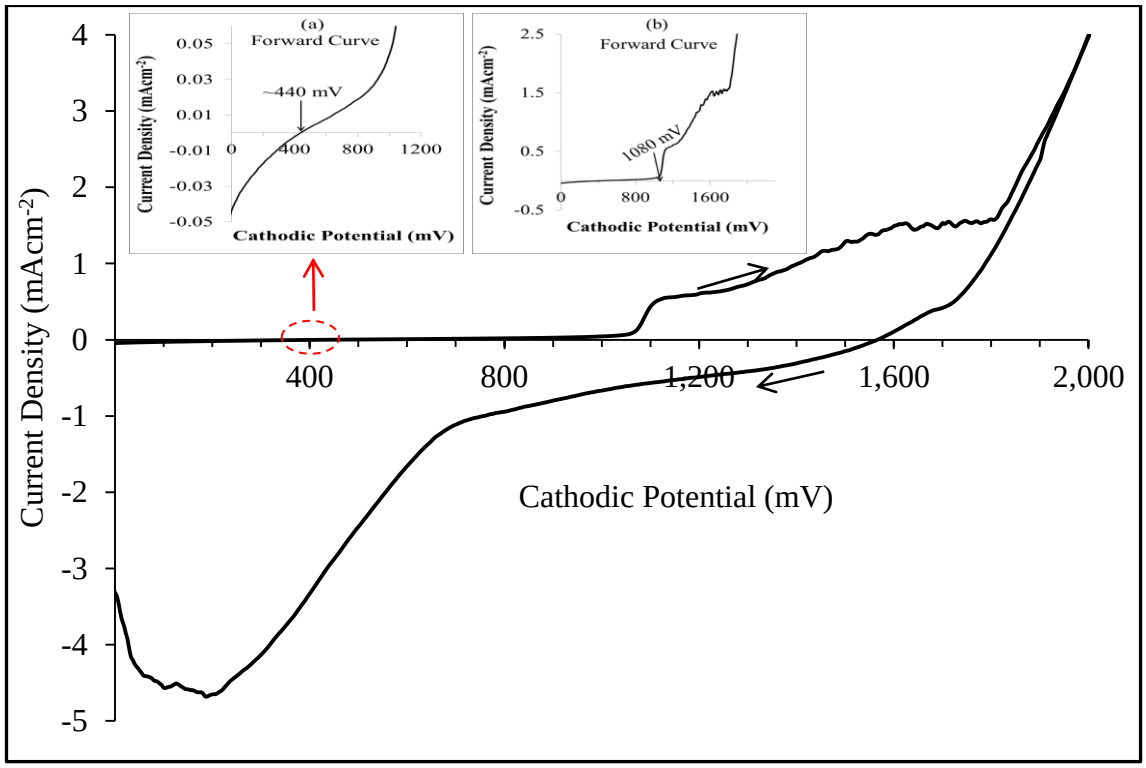


Figure 4.3. Cyclic voltammogram of electrolyte containing a mixture of 0.3 M of $CdCl_2$+0.003 M of SeO_2 aqueous solutions (pH =2.20±0.02 and T=80^oC). (Insets show the transition voltages).

The formation of CdSe thin film is according to the following overall reactions:

$$CdCl_2.H_2O \rightarrow Cd^{2+} + 2Cl^- + H_2O \quad (4.5)$$

$$SeO_2 + H_2O \rightarrow H_2SeO_3 \quad (4.6)$$

$$H_2SeO_3 + 4H^+ + 6e^- \rightarrow Se^{2-} + 3H_2O \quad (4.7)$$

Reaction for the formation of CdSe on FTO substrate may be due to Equation (4.8).

$$Cd^{2+} + Se^{2-} \rightarrow CdSe \quad (4.8)$$

As seen from Figures 4.1 and 4.2, Cd begins to deposit at around 910 mV while Se begins to deposit at around 178 mV under the experimental conditions used in this work. The shift in the reduction potential of both Cd and Se from ~910 mV and 178 mV (Figures 4.1 and 4.2) to ~1080 mV and 440 mV (Figures (b) and (a) at the inset of Figure 4.3) respectively may be due to the chemical reaction that takes place to form CdSe. Comparing the potential at which both Cd and Se begin to deposit, it can be seen that Se deposits first before Cd as seen from the cyclic voltammogram. The theoretical redox potential value can be used to determine which of the elements deposit first; however, its shortcoming is that it cannot be used to determine the approximate potential at which the compound is formed. This is why cyclic voltammetry was used to determine which of the elements deposit first and the suitable potential range to grow CdSe compound.

4.3.2 Structural characterisation

X-ray diffraction (XRD) and Raman spectroscopy techniques were used to study the structural behaviour of electroplated CdSe thin films in both as-deposited and heat-treated states.

4.3.2.1 X-ray diffraction (XRD) studies

Samples of CdSe layers were grown in the voltage range between 1900 mV and 2000 mV in order to examine their structural properties and to identify material phases. This allows preliminary optimisation of growth voltage, V_g to produce near stoichiometric CdSe. Typical XRD patterns for as-deposited (AD) CdSe as a function of V_g are shown in Figure 4.4 (a) while Figure 4.4 (b) shows the XRD patterns of heat-treated (HT) CdSe in air at 350^{o}C for 15 minutes. The XRD peaks show that the as-grown and annealed CdSe films are polycrystalline in nature having hexagonal structure with the preferred orientation along (002) plane. Other peaks that correspond to (103) and (112) planes were also observed with lower peak intensities. The XRD results show that CdSe layers grow best in the cathodic voltage range between 1966 and 1974 mV. A continuous increase in peak intensity was observed as the cathodic deposition voltage increases from 1960 to 1972 mV. A further increase in the voltage led to a decrease in the peak intensity indicating decrease in crystallinity in this V_g region. The XRD results also show that the highest intensity of the (002) peak occurs at a cathodic potential of 1972 mV for both AD- and HT-CdSe samples (see Figure 4.5). Therefore, in this work,

V_g of 1972 mV was selected as the optimum potential for electrodeposition of CdSe thin films.

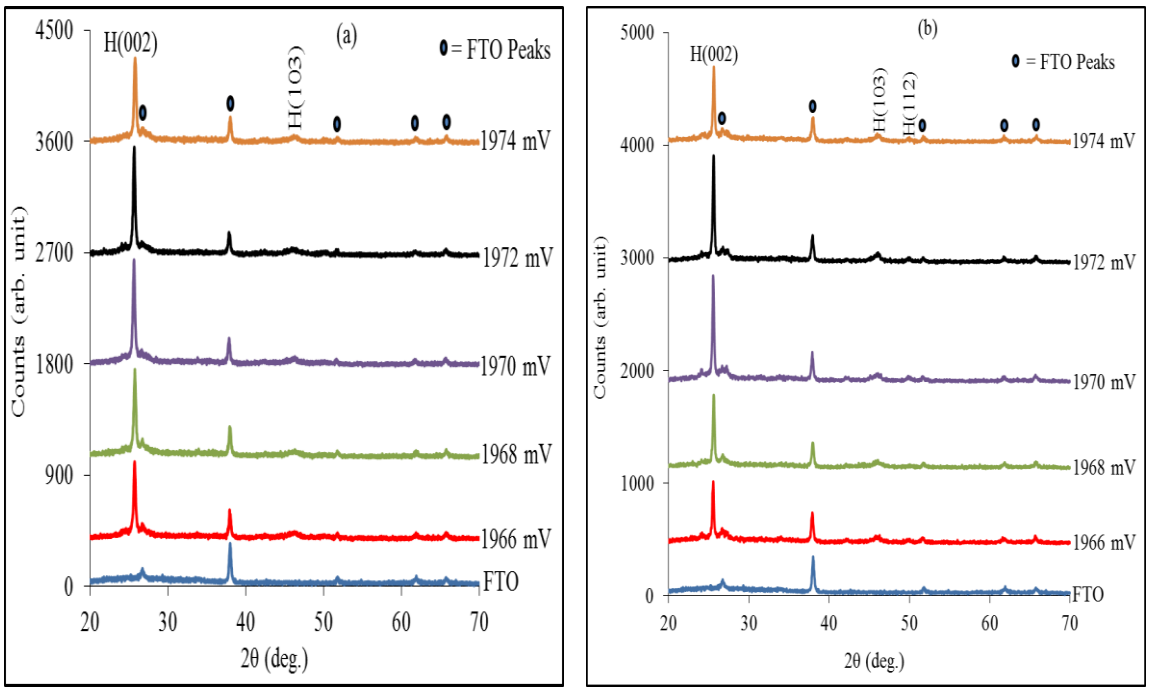


Figure 4.4. XRD spectra of electroplated CdSe layers grown at the cathodic potentials ranging from 1966 mV to 1974 mV for (a) as-deposited CdSe layers, and (b) heat-treated CdSe layers at 350^{o}C for 15 minutes in air.

Figure 4.5 shows how the intensity of the (002) peak varies with the cathodic potential for both AD- and HT-CdSe. This result also explains how the crystallinity of the CdSe layers is improved when subjected to heat treatment. The peak intensities of the HT-CdSe are generally higher than those of the AD-CdSe. This is because, increase in temperature also increases the grain size of the CdSe layers thereby leading to a corresponding improvement in crystallinity.

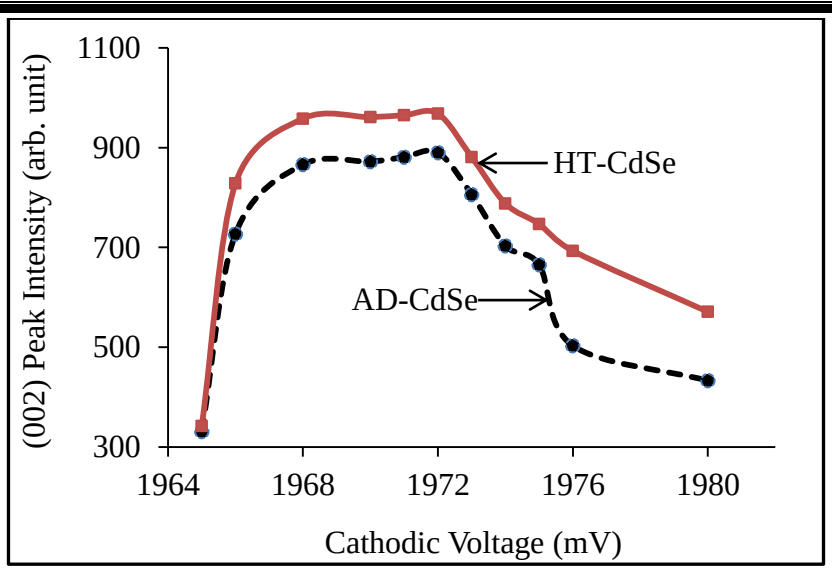


Figure 4.5. Variation of (002) peak intensity as a function of growth voltage for AD- and HT-CdSe layers.

The observed d-spacing values (Table 4.1) from XRD results are compared with the standard values reported in JCPDS data, reference code '01-077-2307' and both are found to be in good agreement. The crystallite sizes of the AD- and HT-CdSe grown at 1972 mV for 20 minutes were determined using Scherrer's equation stated in Equation (3.12) of Chapter 3. The Scherrer's relation is useful in calculating the crystallite size (D) of a poly-crystalline thin film material by using the results obtained from XRD analysis [10]. The calculated crystallite sizes for AD- and HT-CdSe thin films using (002) peak were ~33 and 63 nm respectively. Table 4.1 shows the comparison between the peak intensity and FWHM of AD- and HT-CdSe layers obtained from XRD measurements. After annealing, the intensity increases and the FWHM values decrease indicating the improvement of crystallinity of the material. According to the Scherrer's equation, a reduction in FWHM (β) leads to an increase in the crystallite size and hence, a corresponding increase in grain size. Thus, the higher the crystallite sizes of a thin film material, the better its crystallinity.

Table 4.1. Summary of XRD measurement results for AD- and HT-CdSe layers.

Sample	Peak Intensity	2 theta (degrees)	d-spacing (Å)	FWHM, β (degrees)	FWHM, β (Rad.)	D (nm)
AD-CdSe	1626	~26.00	~3.44	0.260	0.0045	33.3
HT-CdSe	2944	~26.00	~3.45	0.130	0.0023	63.0

4.3.2.2 Raman spectroscopy measurements

An alternative technique that can be used to determine the extent to which a thin film material is crystallised is Raman spectroscopy. Using the Raman instrument, an extended spectrum for the AD- and HT-CdSe layers was collected at room temperature using a 50% laser power (~15 mW) and 100x objectives in the Raman microscope for 10 seconds. Initially, a 100% laser power (~30 mW) was used in the experiment but after switching to white light, it was observed that a section of the sample exposed to the beam was already damaged. For this reason, the laser power was reduced to 50%. Thus, the 50% laser power was able to reduce the heating effect of the laser beam thereby preventing any change on the layer which could lead to loss or reduction of crystallinity. Curve fitting was also performed on the spectra using a combination of Lorentzian/Gaussain mathematical function to obtain parameters such as peak position, peak intensity and peak width also known as full width at half maximum (FWHM). Figure 4.6 shows two visible Raman peaks for AD- and HT- CdSe layers at 200^{o}C for 10 minutes in air. These peaks are Raman longitudinal optical (LO) vibration mode at wave numbers 206 cm^{-1} and 414 cm^{-1} for 1LO and 2LO peaks respectively.

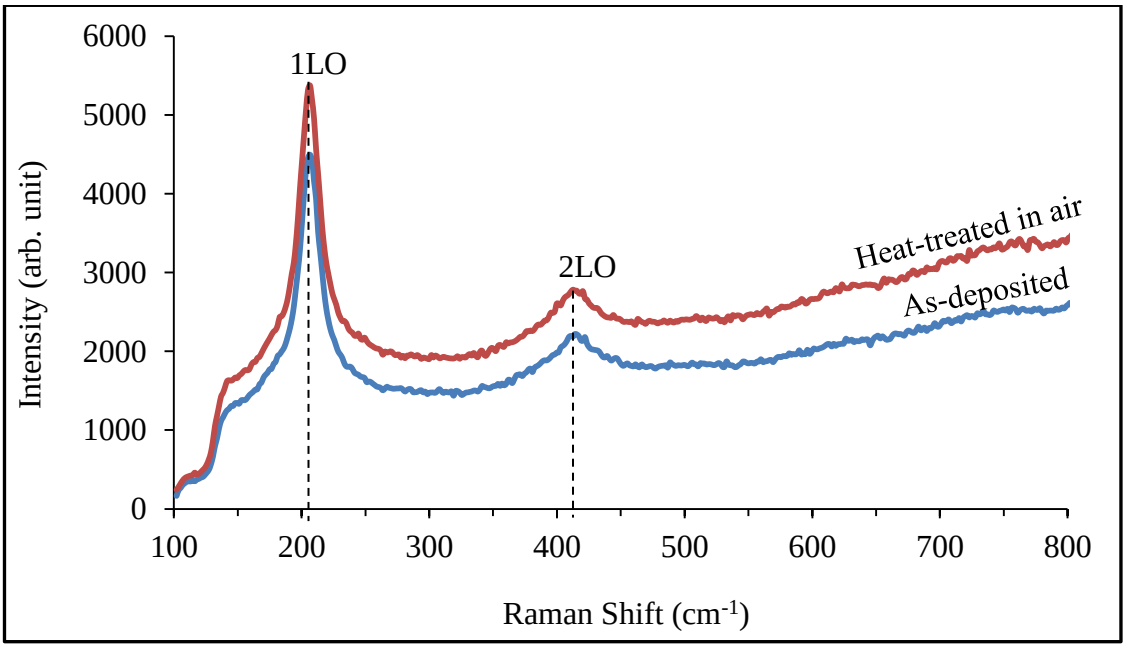


Figure 4.6. Raman spectra of as-deposited and heat-treated CdSe thin films at 200^{o}C for 10 minutes in air.

The wave numbers obtained in this experiment are almost similar to that obtained by Brioude et al. [14] after using an excitation wavelength of 514.5 nm from an argon-krypton laser power. Both AD- and HT- CdSe thin films reveal clear peaks at 1LO and 2LO with no shift in the peak positions. Table 4.2 shows the parameters obtained after performing curve fitting on the spectra. The result shows that HT-CdSe layers possess a better crystallinity than the AD- CdSe layers due to reduced FWHM and higher peak intensity as observed in both 1LO and 2LO Raman peaks.

Table 4.2. Raman parameters obtained by curve fitting of the CdSe spectra.

Raman parameters	As- deposited		Heat-treated	
	1LO	2LO	1LO	2LO
Raman peak position (cm^{-1})	206	414	206	414
Peak intensity (arb. unit)	3002	428	3171	450
FWHM (cm^{-1})	18.7	30.6	17.7	30.5

4.3.3 Optical absorption studies

The optical absorption measurements of the ED-CdSe layers were carried out in order to estimate the optical energy bandgap (E_g). Typical optical absorption graphs for estimation of energy bandgap of both AD- and HT-CdSe layers grown at 1972 mV are shown in Figure 4.7(a); the graph was obtained by plotting the square of absorbance (A^2) as a function of the photon energy ($h\nu$). The bandgaps were estimated by extrapolating the straight line portion to the photon energy axis (at absorbance^2 = 0). As illustrated in Figure 4.7 (a), a reduction took place in the E_g after annealing in air. The decrease in E_g after heat-treatment in air shows that the material crystallinity improved after heat-treatment [15]. The spectrum of absorption curve for HT-CdSe layer also exhibits a sharper absorption edge than AD-CdSe. This is an indication that the concentration of defects in the HT-CdSe layers have been reduced [16]. The E_g values were also obtained for both AD- and HT-CdSe layers deposited between 1966 mV and 1976 mV. The obtained energy bandgap values are plotted in Figure 4.7(b) as a function of cathodic potentials. In general, the E_g values for AD-CdSe layers are higher than HT-CdSe layers with respect to each growth voltage. The higher E_g values suggest the formation of smaller grains in AD-CdSe while the lower E_g values observed in HT-CdSe layers signify the development of smaller grains into larger grains after annealing [17]. A further explanation of the transformation of smaller grains to larger ones is

given in section 4.3.5 of this chapter. In summary, the results shown in Figure 4.7 denote that the energy bandgap of the annealed CdSe at a cathodic voltage of 1972 mV tends to be closer to the bandgap of bulk CdSe in the wurtzite crystal phase. This value was reported by Böhmler et al. to be ~1.80 eV [3].

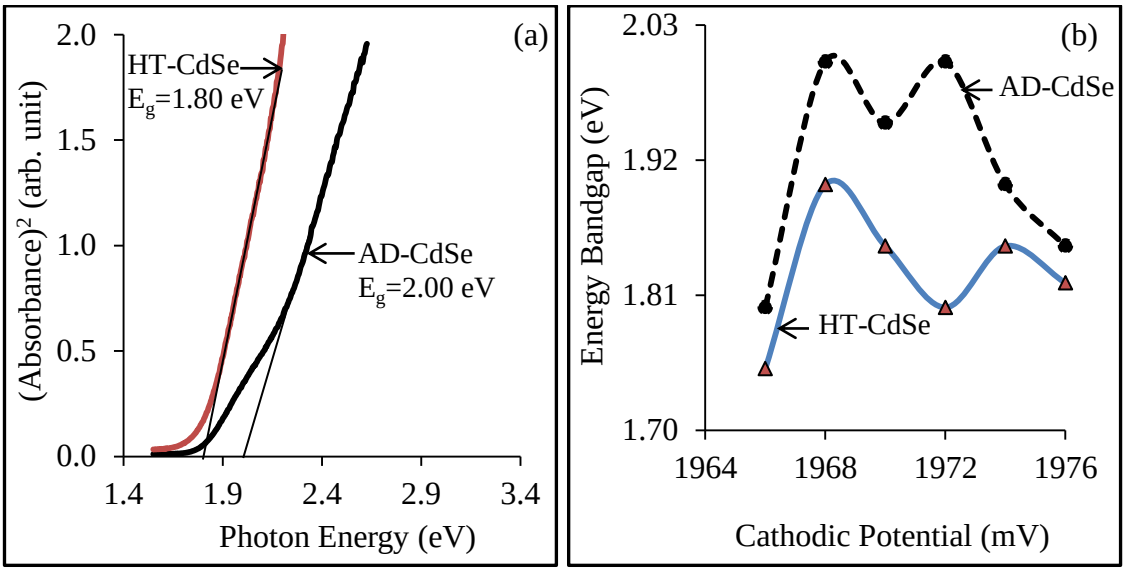


Figure 4.7. (a) Typical optical absorption graphs for CdSe layers grown at -1972 mV and (b) Variation of the typical energy bandgaps as a function of cathodic deposition potentials.

4.3.4 Photoelectrochemical (PEC) cell measurements study

Figure 4.8 illustrates the PEC signals for both AD- and HT-CdSe layers grown at different growth voltages (V_g).

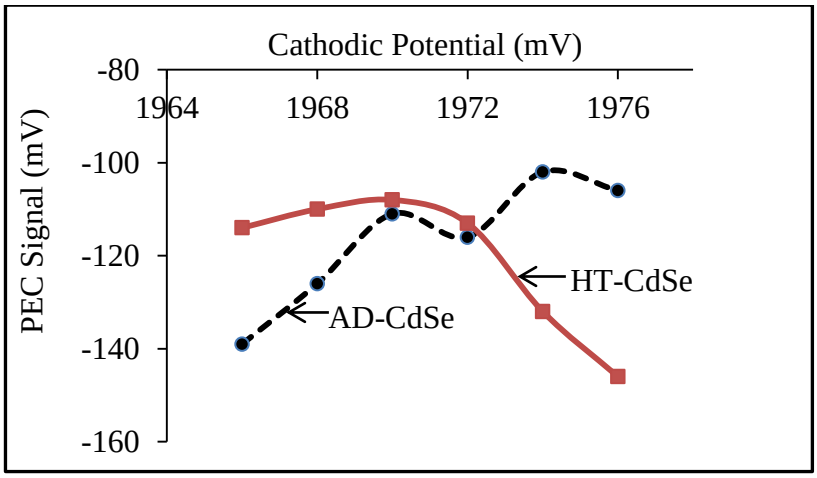


Figure 4.8. Typical PEC signals for CdSe/electrolytic junctions as a function of growth voltage, indicating n-type electrical conduction.

The PEC signals show that both AD and HT samples of CdSe layers grown in the voltage range of 1966 mV to 1976 mV are n-type in electrical conduction. The results also show a crossing / overlapping of the PEC signals for both AD- and HT-CdSe layers at a cathodic potential of 1972 mV. This may be an indication of V_g for growing stoichiometric CdSe layers.

4.3.5 Morphological analysis of CdSe

Scanning electron microscopy (SEM) was used to investigate the surface morphology, the range of the grain sizes and the average thickness of CdSe layers grown on FTO substrates. SEM is a useful tool to study morphology of thin films [11]. Figure 4.9 (a) shows that the surface of AD-CdSe film is uniformly covered by large numbers of grains without pinholes. The obtained micrographs of AD-CdSe layers reveal compact films of regular morphology.

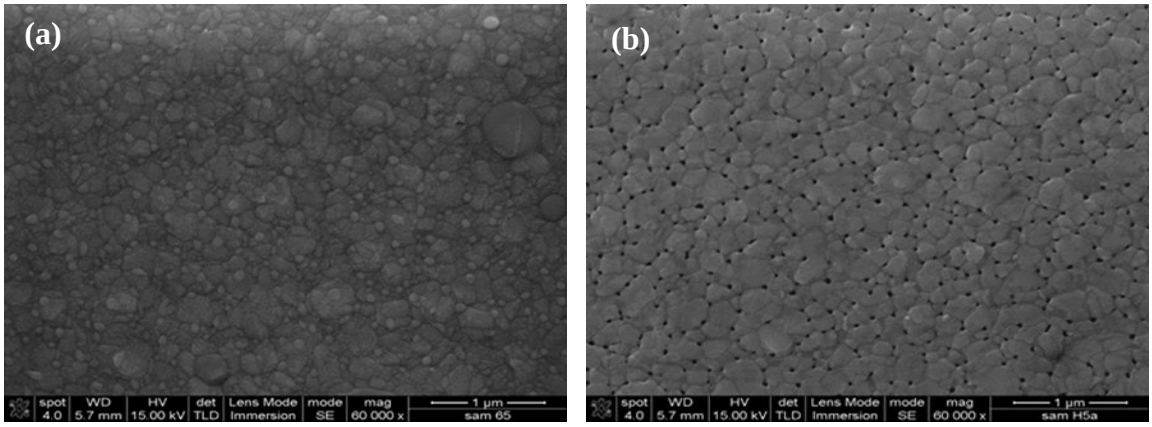


Figure 4.9. SEM images of CdSe thin films grown on FTO substrates at V_g = -1972 mV and t_g = 30 mins. Surface morphology of (a) AD-CdSe and (b) CdSe heat-treated at 380^{o}C for 30 minutes in air.

Figure 4.9 (b) shows the presence of pinholes on the surface of the HT-CdSe films; these pinholes are due to sublimation of excess Se element in the CdSe layer that arises as a result of the high annealing temperature of 380^{o}C for longer duration of 30 minutes. This pinhole formation may also provide an indication of Se precipitation during growth of CdSe layers. Figures 4.10 (a) and 4.10 (b) show the SEM images of AD- and HT-CdSe grown at a shorter duration of five minutes. In Figure 4.10 (a), the grain size of the AD-CdSe layer ranges from 27 to 320 nm while in Figure 4.10 (b), the grain size of HT-CdSe layer ranges from 72 to 360 nm. The minimum and maximum grain sizes of HT-CdSe are greater than those of the AD-CdSe. This increase in grain size may be

attributed to the annealing parameters (temperature and time) used. Both images show that the whole surface of the substrate is more compact together with absence of pinholes. The SEM cross-section illustrated in Figure 4.11 gives the average film thickness of CdSe layer as 156 nm comparable with the theoretical value of 154 nm which was calculated using Faraday's laws of electrodeposition stated by Equation (3.4) in Chapter 3. The thickness of SiO_2 and FTO from Figure 4.11 are ~18 nm and ~196 nm respectively.

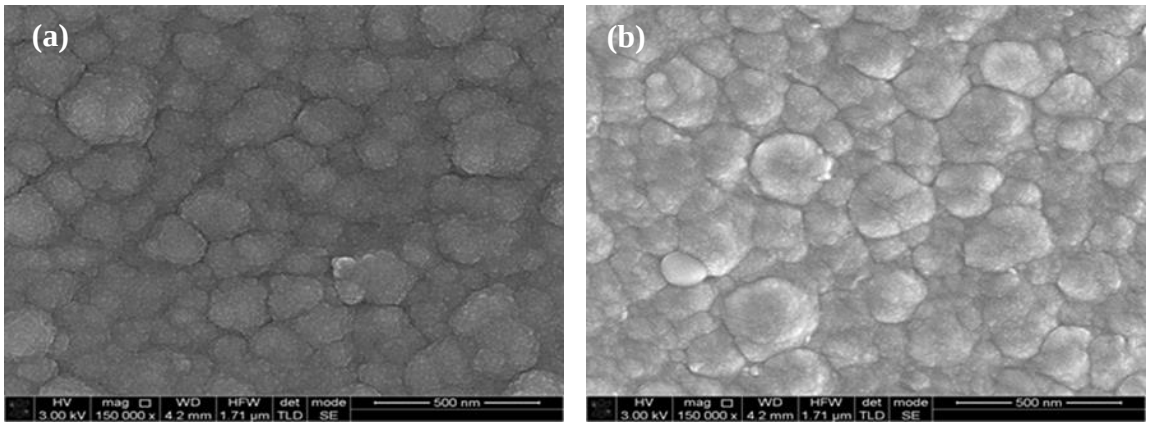


Figure 4.10. SEM images of CdSe thin films grown on FTO substrate at V_g = -1972 mV for t_g = 5 mins. (a) Surface morphology of AD-CdSe with grain size ranging from 27 to 320 nm and (b) Surface morphology of HT-CdSe at 250^{o}C for 10 minutes in air with grain size ranging from 72 to 360 nm.

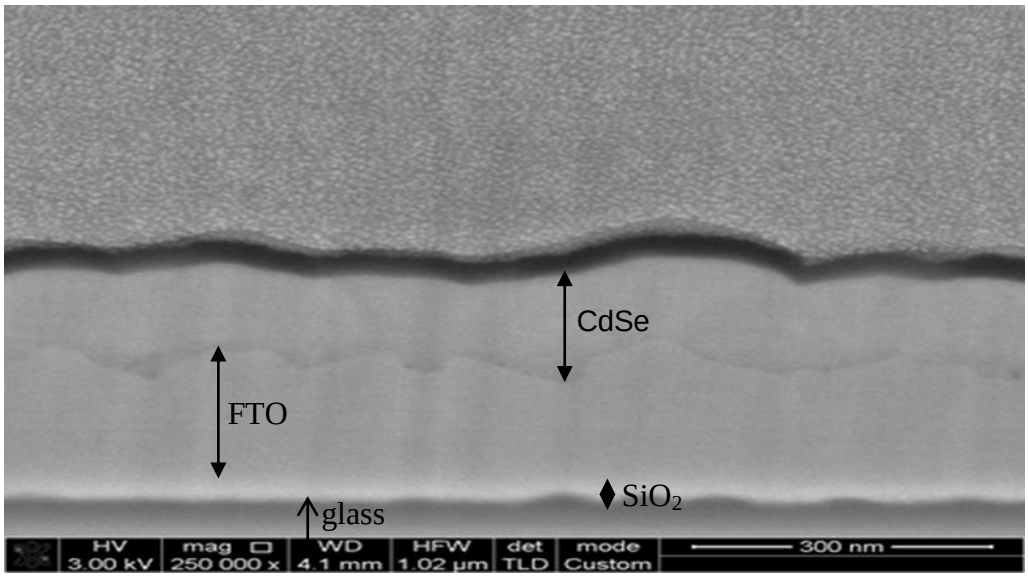


Figure 4.11. Typical cross-section of CdSe thin films grown on FTO substrate and heat-treated at 250 ^{o}C for 10 minutes in air (V_g = -1972 mV and t_g = 5 mins.) (Courtesy: G.J. Russel microscopy center at University of Durham, UK).

4.3.6 Atomic force microscopy (AFM)

Figure 4.12 shows AFM pictures of annealed CdSe deposited at cathodic potential of 1972 mV on glass/FTO substrates. The AFM images reveal the presence of large and dense agglomeration of small grains with good cementing effect. The layers produce pinholes free material suitable for buffer, window and absorber materials in thin film solar cells.

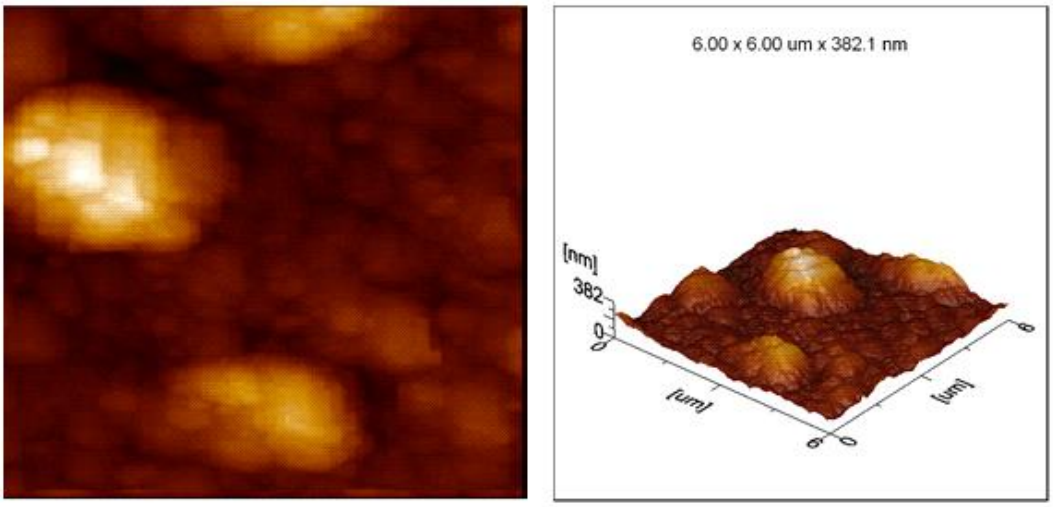


Figure 4.12. Typical AFM images of annealed ED-CdSe grown at -1972 mV on glass/FTO substrate (Courtesy: Institute of Organic Catalysis and Electrochemistry, Almaty, Kazakhstan).

4.3.7 Thickness of ED-CdSe layers

A fore knowledge of thickness of thin film materials is important before device fabrication. This is essential because thickness affects device performance most especially in thin film solar cells. CdSe can be used as an n-type buffer, window or absorber layer in thin film solar cells by selecting its thickness appropriately. In this study, different thicknesses of cadmium selenide were obtained by using deposition times in the range (5 – 30) minutes at a constant deposition potential of 1972 mV. The measured thicknesses obtained by using Microfocus Optical Thickness Profilometer measurement system was compared with the theoretical estimate obtained using Faraday's laws of electrodeposition as illustrated in Figure 4.13. Faraday's law used in the theoretical thickness estimation is given by Equation (4.9) [18].

$$T = \frac{JtM}{nF\rho} \tag{4.9}$$

where T is the thickness of the CdSe film in cm, *J* is average deposition current density in Acm^{-2}, F is Faraday's constant (96485 C/mol), t is the deposition time in seconds, M is the molecular weight of CdSe (191.37 $gmol^{-1}$), n is the number of electrons transferred in the reaction for the formation of 1 mole of CdSe (n = 6 as given by Equations (4.5), (4.6), (4.7) and (4.8) and ρ is the density of CdSe (5.82 gcm^{-3}).

Figure 4.13 shows that the thickness of AD-CdSe increases as the deposition time increases. The results show an approximate linear variation of thickness with deposition time for the experimental graph while in the theoretical curve, a non-linear response is observed. This non-linear behaviour may be due to variation of current density with deposition time during growth period. As shown in Figure 4.13, the thickness of ED-CdSe layer grown for 15 minutes shows a value of approximately 0.80 µm (800 nm) when measured using the thickness profilometer while the theoretical estimate using Faraday's equation gave an approximate value of 0.95 µm (950 nm). The discrepancy between the theoretical estimate and measured value may be due to the fact that not all the electronic charges used in the theoretical estimate are actually involved in the deposition of CdSe. Part of these electronic charges flow through the electrolyte to take part in the electrolysis of water; hence, the observed thicknesses from experimental results are lower than the theoretical values [18]. One of the main advantages of CdSe is the growth of 2.0 µm layer in a short period of ~30 minutes. This is a very important factor for lowering the manufacturing cost of solar cells using CdSe, when compared to CdTe.

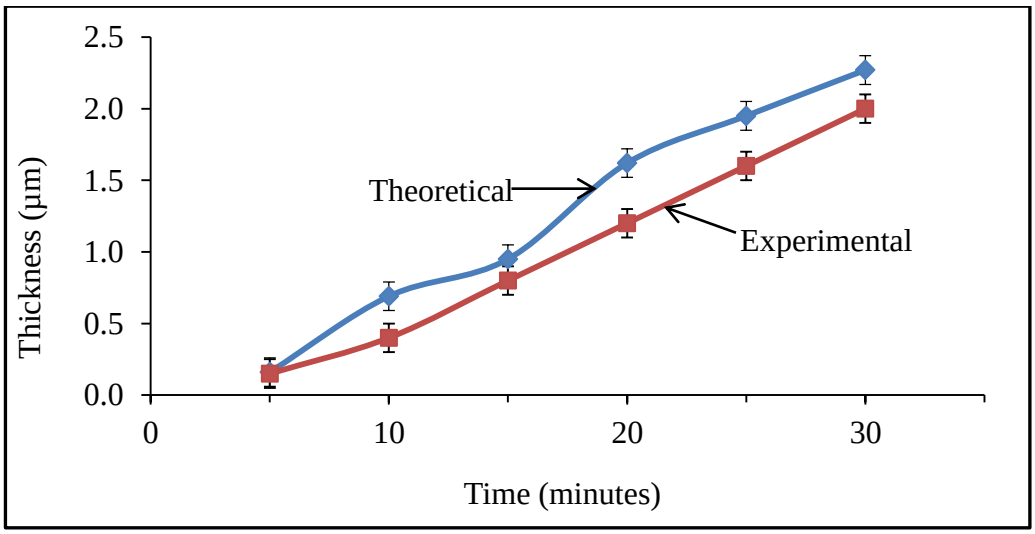


Figure 4.13. Estimated experimental and theoretical values of thickness of CdSe layers as a function of growth period.

4.4 pH optimisation of CdSe thin films

The research work reported thus far show that the pH of the electrolytic solution has a significant effect on the growth of thin film materials [19–21]. Athanassopoulou et al. [22] used a pH of 2.20 for the electrolytic bath and reported the colour of CdSe as glossy black after 20 minutes of deposition using cathodic electrodeposition technique. Shyju et al. [23] prepared CdSe thin films using chemical bath deposition (CBD) technique in an alkaline medium with pH ranging from 10-11 and the authors reported the CdSe appearance as reddish in colour. The compositional analysis carried out by Shyju et al. [23] on the CBD-prepared CdSe showed that the atomic % of Se is greater than that of Cd. Gudage et al. [24] also studied the influence of pH on microstructural and optical properties of electrosynthesised CdSe thin films at different pH of the bath ranging from 2.40 to 3.00 at the interval of 0.15±0.02 using a 3-electrode system. Gudage et al. [24] observed that the atomic percentage of Se is higher than Cd at pH ≥ 2.70. All these reports by different researchers explain the tendency of obtaining different electronic parameters for CdSe thin films at different pH.

In this work, CdSe thin films were electrodeposited using a 2-electrode system at different pH of the electrolytic bath ranging from 1.50 to 3.00±0.02. This experiment was carried out to investigate the pH effect on: the deposition current density, the colour of the CdSe layers, the magnitude of its PEC signals, the optical and compositional properties. This study thus helps in determining the optimum pH of the electrolytic bath where the photovoltaic activity of CdSe layers can be achieved for development in thin film solar cells. The preparative parameters for the pH optimisation of the electrolytic bath used for CdSe growth are: deposition time of 5 minutes, electrolytic bath temperature of 80^{o}C and a cathodic growth voltage of 1972 mV.

4.4.1 Effect of pH variation on deposition current density

Preparative parameters such as stirring, growth temperature and pH of the electrolyte do have effect on the deposition current density (J_d). The experimental results observed while keeping constant the stirring, growth temperature and sample area showed that the lowest average deposition current density (J_d) occured at pH = 2.50. A decrease in J_d was observed as pH increases from 1.50 to 2.50 while an increase in J_d value was further observed as the pH increases from 2.50 to 3.00 thus making pH = 2.50 to have the least J_d value as shown in Figure 4.14. The pH where the J_d is minimal indicates where more resistive semiconductor materials can be grown. This low J_d suggests the

reason for the photovoltaic behaviour of glass/FTO/n-CdSe/Au structure under illumination condition as described in sub-section 4.5.2.

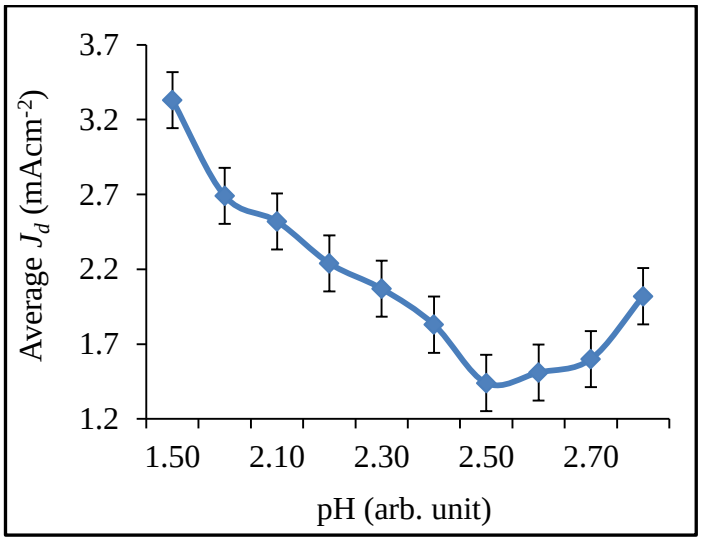


Figure 4.14. The variation of deposition current density (J_d) as a function of pH. The growth voltage (V_g) was kept at constant value of V_g = -1972 mV.

4.4.2 Effect of pH on the visual appearance of electrodeposited CdSe layers

The experiments carried out to study the effect of pH on the growth of CdSe showed that ED-CdSe semiconductors grow within a pH window of 2.00 to 3.00. The experimental observations revealed that the colour changes from black to reddish by gradual changing of the pH from more acidic to less acidic medium. At a pH range of 2.00 to 2.30, the colour appears black while at a pH of 2.40 to 2.50, the colour appears dark red. The CdSe appearance becomes reddish at a pH range of 2.60 to 3.00. The reddish appearance of CdSe within this pH range is an indication of deposition of more Se than Cd since elemental Se layer are known to be reddish in colour [20]. The experimental results show that uniform CdSe layers can be grown in an acidic solution (lower pH) when using an electrodeposition technique. The poor deposition of thin films observed at a pH $\geq$ 3.00 is likely to be an indication that a less acidic aqueous solution may not be ideal for electrodepositing CdSe thin films. This is unlike CdSe thin films grown from CBD technique using a basic solution (very high pH from 10.00 to 11.00) as reported by Shyju et al [23]. As shown in Figure 4.15, a non-uniform deposition occurred at a pH of 1.50. Between 2.00 and 2.10, peelings of the layers were observed. Uniform deposition was observed between 2.20 and 2.70 while non-uniform deposition and peelings were observed at pH beyond 3.00. Thus, the suitable pH range

to grow a uniform non-peeling CdSe layer is 2.20 to 2.70 ± 0.02 at a growth time (t_g) ≤ 5 minutes. The deposition time can be increased to more than five minutes by adjusting other preparative parameters for growth such as lowering the bath temperature, reducing the stirring rate or the voltage of deposition.

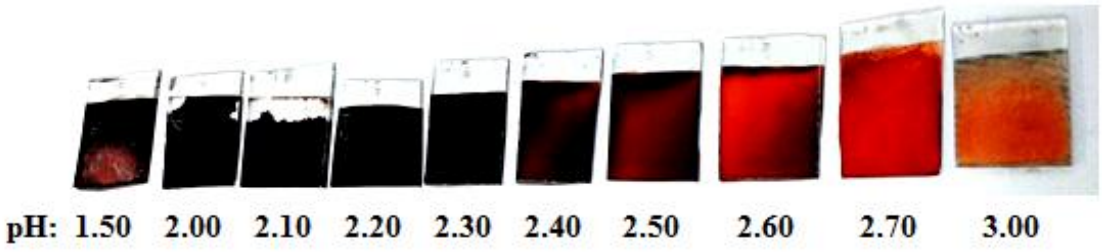


Figure 4.15. The appearance of as-deposited ED-CdSe layers grown at different pH (t_g = 5 minutes, T = 80^{o}C and V_g = -1972 mV).

The explanation given by Athanassopoulou et al. [22] that CdSe is glossy black at pH of 2.20 agrees with the results obtained in this work. Likewise, the investigations carried out by Shyju et al. [23] which showed that CdSe can be reddish in appearance was observed in this work between the pH of 2.60 to 3.00. The different colours exhibited by CdSe signify that it can serve various purposes in thin film solar cells. For instance, with the reddish appearance, CdSe can be used as an n-type window material in thin film solar cells [23], while with the dark appearance, it can find a useful application as an absorber layer in thin film solar cells [22,25,26].

4.4.3 Effect of pH variation on the electrical conductivity type of ED-CdSe

A photoelectrochemical study was carried out on ten samples of CdSe grown at different pH with other preparative parameters being constant to help in the determination of a suitable pH for the growth of stoichiometric CdSe thin films. The sign of the PEC signals as shown in Table 4.3 reveal that CdSe has n-type electrical conductivity within the explored pH range. Figure 4.16 shows only the magnitude of the PEC signal (the PEC signal sign is not considered in this figure) of the AD- and HT-CdSe versus pH. The heat-treatment of the CdSe layers was carried out at 200^{o}C for 10 minutes in air. The results further show that the magnitude of the PEC signal of the AD- and HT-CdSe increases as the pH increases from 1.50 to 2.50. At a pH above 2.50, the PEC signals begin to decrease. Thus, the highest peak occurs at a pH of 2.50 where the CdSe layer appears as dark red. The pH with the highest peak was chosen as the suitable pH for growing a near stoichiometric CdSe layer. Since the magnitude of the PEC signal depends on the width of the depletion region formed at the CdSe/electrolyte

interface, it thus shows that a wider depletion region can be formed for CdSe layers grown at pH = 2.50. A wide depletion region indicates a strong built-in electric field which is required for the separation of photo-generated charge carriers which are created when photons fall on the depletion region [27]. The strong built-in electric field reduces the recombination of the charge carriers before they get to the two electrical contacts; these contacts can be FTO and electrolyte in the PEC system or FTO and Au in a solid state device, glass/FTO/n-CdSe/Au.

Table 4.3. PEC signals with pH.

	PEC Signal (mV)	
pH	AD-CdSe	HT-CdSe
1.50	-77	-70
2.00	-123	-110
2.10	-132	-120
2.20	-151	-135
2.30	-182	-150
2.40	-189	-160
.50	-212	-170
2.60	-204	-160
2.70	-196	-147
3.00	-131	-110

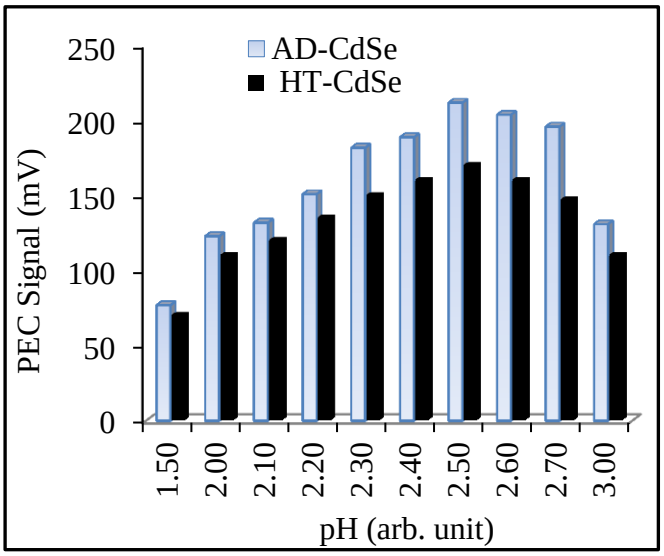


Figure 4.16. Variation of the magnitude of PEC signals with pH.

4.4.4 Effect of pH variation on the optical properties of CdSe thin films

The optical absorption measurements of the ED-CdSe layers were carried out in order to estimate the optical energy bandgap. The studies revealed that the pH of the electrolytic solution has a significant effect on the bandgap of the CdSe thin films. The plot of $(\text{absorbance})^2$ versus photon energy for HT-CdSe layers at pH of 2.20 and 2.50 of the electrolytic bath is shown in Figure 4.17 (a) while Figure 4.17 (b) presents the optical absorption spectra at pH of 2.60 and 2.70. The straight line portion of the graph is extrapolated to the photon energy axis; the intercept on the energy axis gives the E_g value when $(\text{absorbance})^2$ is zero. The energy bandgaps for the HT samples were found to be in the range 1.74 to 2.45 eV depending on the pH of the electrolytes in the bath, this variation is shown in Table 4.4. Table 4.4 also gives the summary of energy bandgaps for pH between 1.50 and 3.00 for AD-CdSe layers. The optical absorption results in Table 4.4 further show that the E_g of the annealed CdSe at a pH of 2.50 tends

to be closer to the bandgap of stoichiometric and bulk CdSe in the wurtzite crystal phase [3].

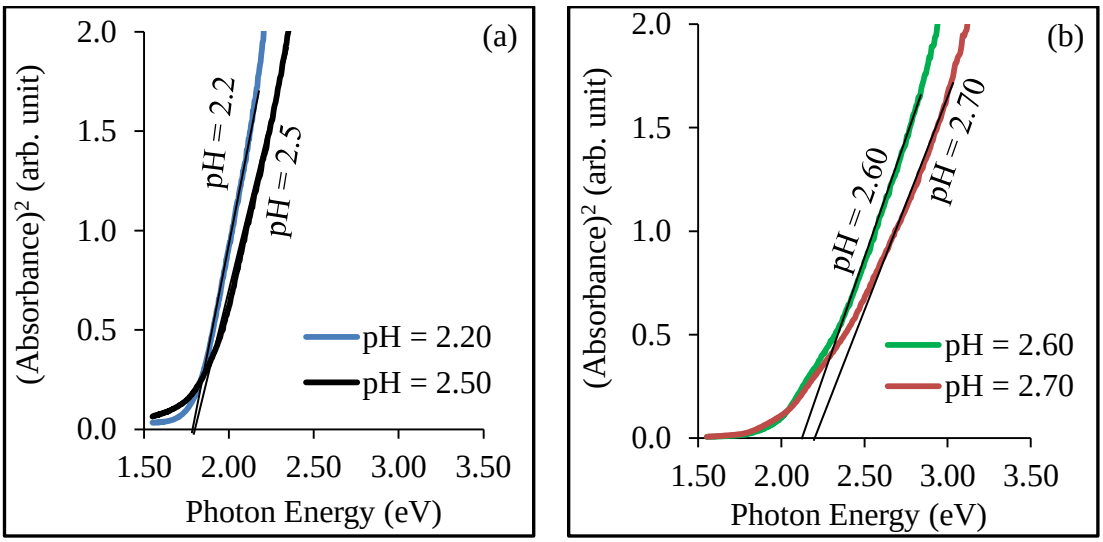


Figure 4.17. Optical absorption spectra for HT-CdSe samples grown at: (a) pH of 2.20 and 2.50 and (b) pH of 2.60 and 2.70.

Figure 4.18 represents the variation of E_g as a function of pH for samples grown within the pH range of 2.00 to 3.00 of the electrolytic bath for both AD- and HT-CdSe layers. The optical results in Table 4.4 and the appearance of the ED-CdSe (Figure 4.15) show that the electroplated CdSe semiconductor materials can be used as a window layer at a pH of 2.70 and above due to its higher energy bandgap and its transparency. Likewise, dark layers of CdSe can be used as an absorber layer in a solar cell application; these dark layers can be obtained by using lower pH region (2.20-2.50) where uniform and non-peeling CdSe layers were observed. One interesting fact to note is that within this pH region, the energy bandgaps of both AD- and HT-CdSe layers tend to be equal; with energy bandgaps of HT-CdSe layers approaching the bulk value for CdSe films in the hexagonal crystal phase.

Table 4.4. Energy bandgap for AD- and HT-CdSe at different pH values ranging from 1.50 to 3.00.

	Bandgap (eV)	
pH	HT-CdSe	AD-CdSe
1.50	1.74	1.88
2.00	1.96	2.00
2.10	2.00	2.05
2.20	1.80	1.90
2.30	1.80	1.90
2.40	1.80	1.90
2.50	1.80	1.90
2.60	2.10	2.10
2.70	2.20	2.42
3.00	2.45	2.50

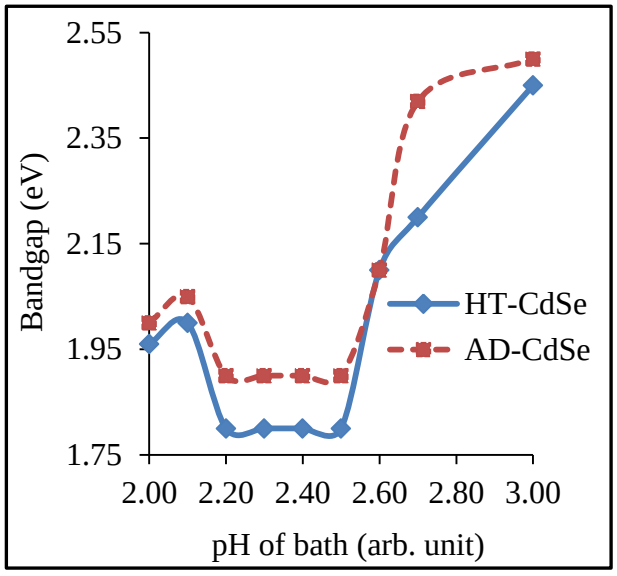


Figure 4.18. Variation of energy bandgaps with pH (t_g = 5 minutes, T = 80°C and V_g = -1972 mV).

4.4.5 Effect of pH variation on the compositional properties CdSe thin films

EDX technique was used to carry out the quantitative analysis of the ED-CdSe thin films deposited on FTO substrate to study the percentage (%) composition of the Cd and Se atoms present in the CdSe thin films at different pH values ranging between 2.30 and 3.00. This technique also helps in determining the film stoichiometry. Table 4.5 summarises the percentage composition of Cd and Se atoms present in the CdSe thin films at different pH values while Figure 4.19 illustrates the diagrammatic representation of Cd and Se atoms within the explored pH values. As seen in Figure 4.19, the percentage of Cd and Se atoms present in the CdSe thin film changes with pH values. At lower pH of 2.30, average atomic % of Cd:Se for ED-CdSe was 53.6:46.4 showing that the film is more rich in Cd than Se while at a pH of 3.00, the atomic % of Cd:Se for ED-CdSe was 84.2:15.8 signifying that the film is more rich in Se than Cd.

The compositional analysis also revealed that the Cd:Se ratio was close to 1:1 at the pH of 2.50. This is an indication that pH of 2.50 may be suitable for growing nearly stoichiometric CdSe layers. The EDX analysis showed that lower pH favours deposition of more metallic atoms like Cd than Se. As the pH increases from 2.30 towards 3.00, the % of Cd atoms decrease while the % of Se atoms increase. It could therefore be seen that by changing the pH of the electrolytic bath, the stoichiometry and properties of electroplated CdSe layers can be changed. The experimental results obtained in this

work also agrees with the report given by Gudage et al. [24] that the atomic percentage of Se is higher than Cd at pH ≥2.70.

Table 4.5. Composition of CdSe thin films versus pH values.

Bath pH	Elements	Atomic %
2.30	Cd	53.6
	Se	46.4
2.50	Cd	49.6
	Se	50.4
2.70	Cd	34.8
	Se	65.2
3.00	Cd	15.8
	Se	84.2

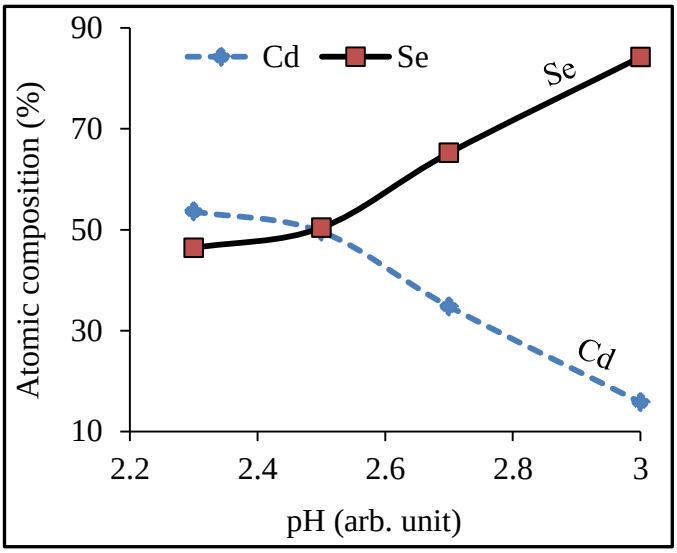


Figure 4.19. Plot of percentage composition of Cd and Se atoms in CdSe thin films versus pH values.

4.5 Testing the electronic quality of CdSe thin films

The electronic qualities of ED-CdSe layers were tested using current-voltage (I-V) and capacitance-voltage (C-V) techniques. The I-V technique was used in studying the ohmic behaviour of glass/FTO/n-CdSe/metal contacts while the rectifying behaviour of glass/FTO/n-CdSe/metal contacts was investigated using both I-V and C-V techniques.

4.5.1 Ohmic behaviour of electrodeposited n-CdSe layers

In order to study the ohmic behaviour of ED-CdSe layer, a metal whose work function is lower than the electron affinity of CdSe is needed as a metal contact for the ED-CdSe layers. In this study, Al with work functions of ~4.20 eV [28] has been chosen as a metal contact to CdSe with electron affinity of ~4.95 eV [29]. Al was evaporated on ED-CdSe layer of ~1.6 µm in a metal evaporator maintained at a high pressure of 10^{-7} mbar. This high pressure was used to prevent oxidation of the Al metal contact. The resistances of AD- and HT-CdSe layers were estimated from the device structure glass/FTO/n-CdSe/Al using I-V measurement technique. The I-V curves obtained for AD- and HT-CdSe thin films are given in Figures 4.20 (a) and 4.20 (b) respectively.

The results show that both AD- and HT-CdSe layers obey Ohm's law when Al was used as a back metal contact.

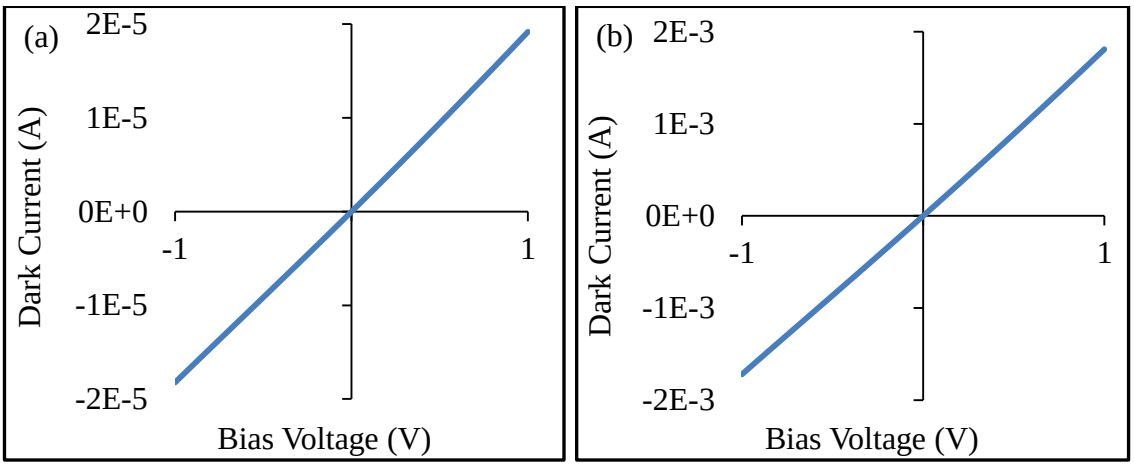


Figure 4.20. I-V curves illustrating the ohmic behaviour of glass/FTO/n-CdSe/Al device structure for (a) as-deposited CdSe layer and (b) heat-treated CdSe layer at 200^{o}C, for 10 minutes in air.

The electrical resistivity was calculated from the estimated resistances using Equation (3.15) stated in Chapter 3 while the electrical conductivity was estimated by finding the inverse function of resistivity. Table 4.6 shows the summary of measured and calculated electronic parameters of AD- and HT-CdSe thin films at 200^{o}C for 10 minutes in air. As seen in Table 4.6, the AD-CdSe layer possesses very high series resistance (R_s) of ~52 kΩ but after annealing, the R_s was reduced to ~0.55 kΩ.

Table 4.6. Summary of ohmic parameters obtained for as-deposited and heat-treated CdSe layers at 200^{o}C for 10 minutes in air.

Ohmic parameters	AD-CdSe	HT-CdSe at 200^{o}C for 10 minutes in air
Series resistance, R_s (kΩ)	52.00	0.55
Resistivity, ρ (Ω.cm)	8.95×10^{6}	9.47×10^{4}
Conductivity, σ $(\Omega.cm)^{-1}$	1.12×10^{-7}	1.06×10^{-5}

A very high resistivity of the order of 10^6 Ωcm was obtained for AD-CdSe layer. The high series resistance exhibited by CdSe can lead to low J_{sc} and FF when used in solar cell fabrication. After heat-treatment, the resistivity of the CdSe layer reduces to the order of 10^4 Ωcm. This shows that annealing can help to reduce the R_s and ultimately

lead to a better fill factor. The overall result thus shows that annealing helps to improve the electronic quality of ED-CdSe layers.

4.5.2 Rectifying behaviour of electrodeposited n-CdSe layers

The rectifying behaviour of CdSe thin films was studied by developing glass/FTO/n-CdSe/Au device structure. Au was chosen for this experiment because a metal with work function (ϕ_m) higher than the electron affinity (χ) of CdSe is needed to make a Schottky contact on n-CdSe (ϕ_m of Au is 5.10 eV while the χ of CdSe is 4.95 eV). The rectifying contacts were made by evaporating 3 mm diameter Au contacts on n-CdSe layers.

Figures 4.21 (a) and 4.21 (b) show the log-linear and linear-linear I-V characteristics of the Schottky diodes fabricated from n-CdSe layers. The semi-log graph was used in estimating the values of the rectification factor (*RF*), ideality factor (*n*), the reverse saturation current (I_s), and the potential barrier height (ϕ_b) while the linear-linear graphs are useful in estimating the series resistance (R_s) and shunt resistance (R_{sh}) from the forward and reverse current portions of the I-V curve respectively.

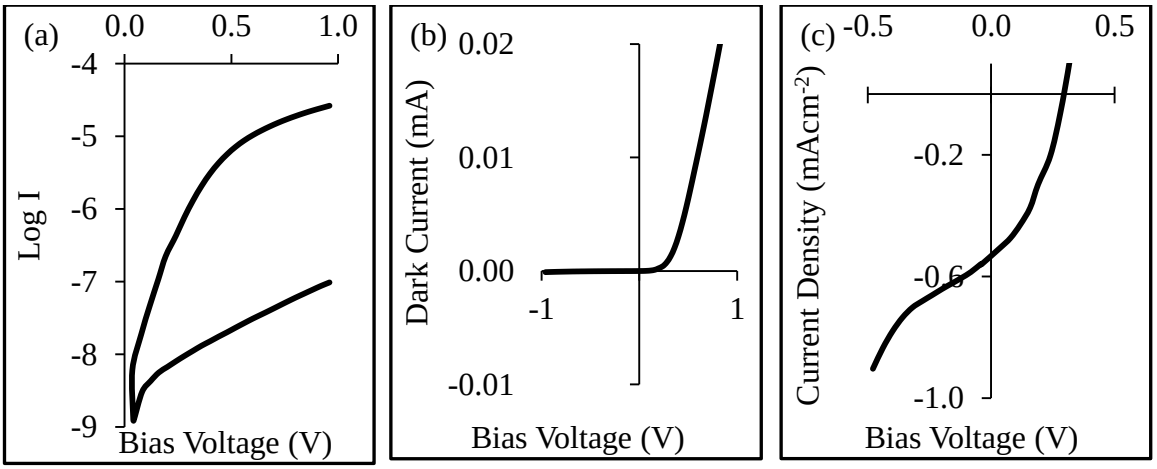


Figure 4.21. Typical I-V characteristics of the n-CdSe/Au Schottky diodes (a) Log-linear, (b) Linear-linear under dark conditions, and (c) under AM1.5 illumination condition at room temperature.

Table 4.7 gives the summary of I-V parameters of the Schottky diodes under dark and illumination conditions. A RF of $10^{2.5}$ was obtained for this particular diode, however RF > $10^{2.5}$ was observed for some other measured diodes reported in one of our previous communications [30]. The RF helps in assessing the quality of a rectifying diode. A large RF of approximately 10^2 is sufficient for a good rectifying diode [31].

Table 4.7. Summary of I-V parameters of g/FTO/n-CdSe/Au measured under dark and illumination conditions.

	I-V measurement under dark condition							I-V measurement under illumination condition			
Device Structure	*RF*	*n*	I_s (nA)	ϕ_b (eV)	R_s (kΩ)	R_{sh} (MΩ)	V_t *(V)*	V_{oc} *(V)*	J_{sc} $mAcm^{-2}$	*FF*	η *(%)*
glass/FTO/n-CdSe/Au	$10^{2.5}$	1.5	6.31	>0.79	24.0	4.1	0.24	0.300	0.55	0.35	0.06

The ideality factor estimated using Equation (3.25) of Chapter 3 lies between 1.00 and 2.00. The *n* value of 1.50 signifies that both thermionic emission and R&G process contribute to current transport in parallel. Details of the importance of ideality factor have been discussed in Chapter 3. The fabricated Schottky diodes also have a leakage current of 6.31 nA and barrier height >0.79 eV. The I_s was estimated by finding the antilog of the intercept on the Log I axis of Figure 4.21 (a) while ϕ_b was estimated using Equation (3.19) of Chapter 3. The barrier height obtained for the Schottky diode is extremely high when compared to the expected {$\phi_b = \phi_m - \chi \approx (5.10 - 4.95)$ eV = 0.15 eV} theoretical value from Schottky theory. Therefore, the high potential barrier height experimentally measured seems to be due to Fermi level pinning at Au/n-CdSe interfaces due to defect levels. This is not surprising for practical thin films with high concentration of defects. R_s and R_{sh} of ~24 kΩ and ~4.1 MΩ were obtained from the linear-linear I-V characteristics in Figure 4.21 (b). The R_{sh} value is very large; this large value is a typical feature of diodes whose behaviour is close to an ideal one. However, due to the presence of high R_s, the fabricated diodes reported in this work deviate from diodes with ideal characteristics. Schottky diodes are known to have lesser forward voltage drop (or threshold voltage) than normal p-n junction diodes [32]; the forward voltage drop of Schottky diode is in the range 0.15 V to 0.45 V [33]. This low threshold voltage makes them to have fast switching speeds and with this feature, they can find useful application at the output stages of switching power supplies [34]. The estimated threshold voltage (V_t) in this work is ~0.24 V; this value falls in the range of reported values of V_t for Schottky diodes. The results of the I-V measurement under AM1.5 illumination showed that the device structure glass/FTO/n-CdSe/Au is photo-voltaic active as shown in Figure 4.21 (c). The initial device parameters are V_{oc}=0.300 V,

J_{sc}=0.55 mAcm^{-2} and *FF*=0.35. All these measured device parameters show that ED-CdSe layers are device quality materials.

4.5.3 Capacitance-voltage measurement of n-CdSe Schottky diodes

Capacitance-voltage (C-V) measurements were carried out on glass/FTO/n-CdSe/Au rectifying structures. The measurements were carried out with a detection signal at 1 MHz in order to reduce contributions from defects towards the junction capacitance. The C-V and Mott-Schottky plots are illustrated in Figures 4.22 (a) and 4.22 (b) respectively. As presented in Figure 4.22 (a), the depletion layer capacitance obtained at zero bias for the glass/FTO/n-CdSe/Au device structure is 6.90 nF. By incorporating the values of the depletion layer capacitance into Equation (3.38), the width of the depletion region, *W* was estimated to be ~41.1 nm. As earlier explained in section 3.5.2 of Chapter 3, Equation (3.39) can also be used in estimating the depletion width if the correct V_{bi} value is used. Using Equation (3.39), the width was calculated to be 41.0 nm. The two values of *W* obtained from Equation (3.38) and Equation (3.39) correspond to each other when approximated to the nearest whole number.

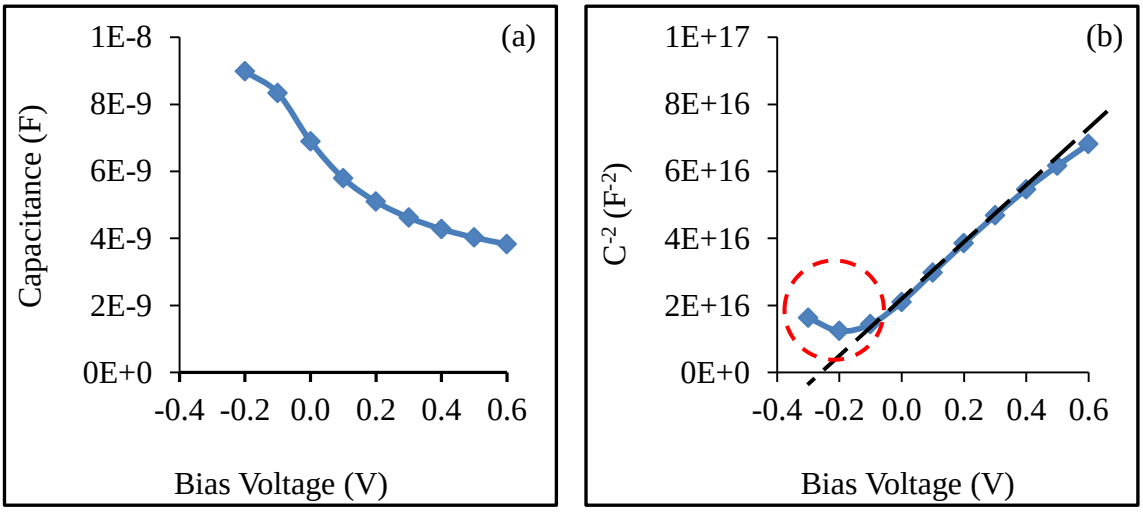


Figure 4.22. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/n-CdSe/Au. Note: The red dotted circle in Figure 4.22 (b) signify the non-linear portion of the Mott-Schottky plot caused by surface states.

The Mott-Schottky plot in Figure 4.22 (b) was used in finding the doping density of the CdSe thin film. The slope (8.70×10^{16} $F^{-2}V^{-1}$) obtained by taking the straight line of linear portion of Mott-Schottky plot in Figure 4.22 (b) was substituted into Equation (3.35) to obtain donor density of 1.61×10^{17} cm^{-3}. As explained by Bhattacharya et al.

[35], when the slope of the Mott-Schottky plot is positive, it indicates that the semiconductor is negative. This is another way of confirming the electrical conductivity type of deposited semiconductor materials. As seen in Figure 4.22 (b), the slope is positive, hence it shows that the electroplated CdSe thin film is n-type in electrical conduction. This result further confirms the PEC cell results given in section 4.3.4 of this chapter that revealed the n-type electrical conduction of ED-CdSe thin films. A linear graph is expected to be obtained for Mott-Schottky plots when the doping concentration of the material used for diode fabrication is uniform [36]. However as seen in Figure 4.22 (b), a section of the plot {the circled section} is not linear. The non-linearity has been explained to be caused by presence of surface states, roughness and traps [35,37]. By substituting the effective electron mass of CdSe ($m_e^* = 0.13m_o$ [38]) into Equation (3.42), the value of effective density of states in the conduction band minimum (N_C) was found to be 1.17×10^{18} cm^{-3} at 300 K room temperature. The experimental results obtained in this work show that the doping density of the CdSe semiconductor is less than the effective density of states in the conduction band of the CdSe thin films. This property makes the Fermi energy level of the CdSe semiconductor to lie below the conduction band minimum thus classifying the CdSe thin films used for the Schottky diodes fabrication as a non-degenerate semiconductor material. Details of the C-V measurement results for Au/n-CdSe Schottky diodes are shown in Table 4.8.

Table 4.8. Summary of electronic parameters obtained from glass/FTO/n-CdSe/Au device structures using C-V technique under dark condition.

C_o (nF)	N_D (cm^{-3})	Built-in potential, V_{bi} (V)		Depletion width, W (nm)		E_C-E_F (eV)	E_{max} (Vcm^{-1})
		Measured	Calculated	Using C_o	Using V_{bi}		
6.90	1.61×10^{17}	0.240	0.241	41.1	41.0	0.05	1.17×10^{5}

As given in Table 4.8, E_C - E_F for the CdSe thin film shows a positive value of 0.05 eV and this also signifies that the Fermi level position lies just below the E_{Cmin}. Equation (3.46) of Chapter 3 was used to calculate the position of the Fermi level for the n-type CdSe layer. The electric field at the M/S interface of the Schottky diode was estimated to be 1.17×10^{5} Vcm^{-1} using Equation (3.49). Using Equation (3.51), the theoretical value of built-in potential was calculated as 0.241 V; by practical measurement using the Mott-Schottky plot in Figure 4.22 (b), the intercept on the voltage axis gives an estimate of the V_{bi} as 0.24 V. By approximating both theoretical and measured values to

2 d.p, the V_{bi} = 0.24 eV. This result shows that there is a correlation between the measured and calculated value of V_{bi}. The agreement between the measured and calculated value of V_{bi} is an indication that the defect level in the Schottky diode is minimal. From Figure 4.21 (b), the I-V measurement also shows the V_{bi} to be ~0.24 V. In terms of V_{bi} measurement, both I-V and C-V techniques show the same value. The V_{bi} is a function of the barrier height. It should be noted that the similarity between the V_{bi} measured from both I-V and C-V techniques does not guarantee the uniformity of the barrier. In most cases, the V_{bi} obtained in C-V is > V_{bi} obtained in I-V. This difference is due to the variation in barrier height (ϕ_b) obtained using these two techniques. In most semiconductor materials, the ϕ_b from C-V is always greater than the ϕ_b from I-V measurement technique [39]. The variation in barrier height is usually caused by sensitivity of C-V technique to the defects in the diode [17] and by inhomogeneities that take place at the M/S interface [40]. Examples of some of these inhomogeneities include: distribution of interfacial charges and lack of uniformity of the interfacial layer thickness [40]. Nonetheless, if the defect levels in the diode are reduced, the sensitivity of C-V technique to defects in the diode will also be minimised and this can influence the results of the measurements being carried out. Under this situation, it is therefore possible for the ϕ_b measured in C-V to be equal to or much less than ϕ_b measured in I-V. In these measurements, since the C-V measurements have been carried out at high frequencies, the effects of defects on measured capacitance have been minimised.

4.6 Summary

CdSe thin films have been successfully grown using electrodeposition technique with a 2-electrode system on glass/FTO substrates. The effect of growing CdSe thin films at different cathodic potentials was explored and optimum V_g of 1972 mV was obtained from the various analytical techniques carried out on the CdSe thin films. The XRD results have shown that the layers are hexagonal and polycrystalline with preferential orientation along the (002) plane. PEC study revealed that the CdSe films have n-type electrical conductivity. The results obtained from the optical absorption measurement showed that ED-CdSe layers have direct band gaps in the range (1.80–2.00) eV for AD and (1.75–1.90) eV for HT-CdSe thin films. The effect of pH variation between 1.50 and 3.00 of the CdSe electrolyte was also investigated on the optoelectronic properties of CdSe layers. The results from PEC study revealed that the CdSe layers are still n-

type in electrical conduction despite variation in pH; the variation in pH only influences the magnitude of the PEC signals and not the electrical conductivity type. Different colours (dark, dark-red and reddish) of the CdSe thin films were also observed under different pH conditions. The minimum and maximum energy bandgaps were observed at the lowest pH of 1.50 and highest pH of 3.00 explored in this work respectively. Depending on the thickness and pH of the layer, CdSe can be applied in thin film PV development for use as a buffer, window or absorber material. The experimental results showed that suitable pH range to grow a uniform non-peeling CdSe layer is 2.20 to 2.70±0.02. Experimental results also indicated that pH of 2.50 is suitable for growing a near stoichiometric CdSe layers which can be used in photovoltaic devices. The electronic quality of the ED-CdSe layers was also tested by making ohmic and rectifying contacts to CdSe thin films. The results from ohmic contacts made to CdSe showed that the thin films obey Ohm's law both for as-deposited and heat-treated materials. CdSe exhibited good rectifying diodes behaviour when measured under dark conditions. The results from C-V analysis equally revealed the non-degenerate nature of the CdSe thin films.

References

[1] L. Zhao, L. Hu, X. Fang, Adv. Funct. Mater., **22** (2012) 1551–1566.

[2] S. M. Pawar, A. V. Moholkar, K. Y. Rajpure, C. H. Bhosale, Sol. Energy Mater. Sol. Cells, **92** (2008) 45–49.

[3] M. Böhmler, Z. Wang, A. Myalitsin, A. Mews, A. Hartschuh, Angew. Chemie - Int. Ed., **50** (2011) 11536–11538.

[4] M. A. Hernandez-Perez, J. Aguilar-Hernandez, G. Contreras-Puente, J. R. Vargas-García, E. Rangel-Salinas, Phys. E Low-Dimensional Syst. Nanostructures, **40** (2008) 2535–2539.

[5] Z. Aneva, D. Nesheva, C. Main, S. Reynolds, A. G. Fitzgerald, E. Vateva, Semicond. Sci. Technol., **23** (2008) 095002.

[6] M. Dhanam, R. R. Prabhu, P. K. Manoj, Mater. Chem. Phys., **107** (2008) 289–296.

[7] A. A. Yadav, M. A. Barote, E. U. Masumdar, Sol. Energy, **84** (2010) 763–770.

[8] C. Bhattacharya, J. Datta, Mater. Chem. Phys., **89** (2005) 170–175.

[9] A. V. Kokate, U. B. Suryavanshi, C. H. Bhosale, Sol. Energy, **80** (2006) 156–160.

[10] S. Thanikaikarasan, K. Sundaram, T. Mahalingam, S. Velumani, J. K. Rhee, Mater. Sci. Eng. B Solid-State Mater. Adv. Technol., **174** (2010) 242–248.

[11] S. M. Pawar, A. V. Moholkar, K. Y. Rajpure, C. H. Bhosale, J. Phys. Chem. Solids, **67** (2006) 2386–2391.

[12] J. Sun, D. K. Zhong, D. R. Gamelin, Energy Environ. Sci., **3** (2010) 1252.

[13] P. Vanýsek, CRC Handbook of Chemistry and Physics, 91th ed., CRC Press, Boca Raton, Florida (2000).

[14] A. Brioude, J. Bellessa, S. Rabaste, B. Champagnon, L. Sphanel, J. Mugnier, J. C. Plenet, J. Appl. Phys., **95** (2004) 2744–2748.

[15] M. A. Redwan, E. H. Aly, L. I. Soliman, A. A. El-Shazely, H. A. Zayed,

Vacuum, **69** (2003) 545–555.

[16] J. Han, C. Spanheimer, G. Haindl, G. Fu, V. Krishnakumar, J. Schaffner, C. Fan, K. Zhao, A. Klein, W. Jaegermann, Sol. Energy Mater. Sol. Cells, **95** (2011) 816–820.

[17] N. B. Chaure, S. Bordas, A. P. Samantilleke, S. N. Chaure, J. Haigh, I. M. Dharmadasa, Thin Solid Films, **437** (2003) 10–17.

[18] F. Fauzi, D. G. Diso, O. K. Echendu, V. Patel, Y. Purandare, R. Burton, I. M. Dharmadasa, Semicond. Sci. Technol., **28** (2013) 045005.

[19] Y. G. Gudage, R. Sharma, Curr. Appl. Phys., **10** (2010) 1062–1070.

[20] C. M. Shen, X. gang Zhang, H. L. Li, Mater. Sci. Eng. B Solid-State Mater. Adv. Technol., **84** (2001) 265–270.

[21] S. M. Pawar, A. V. Moholkar, C. H. Bhosale, Mater. Lett., **61** (2007) 1034–1038.

[22] M. D. Athanassopoulou, J. A. Mergos, M. D. Palaiologopoulou, T. G. Argyropoulos, C. T. Dervos, Thin Solid Films, **520** (2012) 6515–6520.

[23] T. S. Shyju, S. Anandhi, R. Indirajith, R. Gopalakrishnan, J. Alloys Compd., **506** (2010) 892–897.

[24] Y. G. Gudage, N. G. Deshpande, R. Sharma, J. Phys. Chem. Solids, **70** (2009) 907–915.

[25] H. Majidi, J. B. Baxter, Electrochim. Acta, **56** (2011) 2703–2711.

[26] Y. P. Gnatenko, P. M. Bukivskij, I. O. Faryna, A. S. Opanasyuk, M. M. Ivashchenko, J. Lumin., **146** (2014) 174–177.

[27] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[28] G. A. Chamberlain, Sol. Cells, **8** (1983) 47–83.

[29] T. L. Chu, S. S. Chu, Solid State Electron., **38** (1995) 533–549.

[30] O. I. Olusola, O. K. Echendu, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., **26** (2015) 1066–1076.

[31] O. I. Olusola, M. L. Madugu, I. M. Dharmadasa, Mater. Res. Innov., **19** (2015) 497–502.

[32] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New Jersey (2007).

[33] https://en.wikipedia.org/wiki/Schottky_diode (accessed August 21, 2013).

[34] K. Walters, B. Werner, Introduction to Schottky Rectifiers, MicroNote Series 401, (2016).

[35] C. Bhattacharya, J. Datta, J. Solid State Electrochem., **11** (2007) 215–222.

[36] I. M. Dharmadasa, N. B. Chaure, A. P. Samantilleke, A. Hassan, Sol. Energy Mater. Sol. Cells, **92** (2008) 923–928.

[37] R. K. Pandey, S. N. Sahu, S. Chandra, Handbook of Semiconductor Electrodeposition, first ed., Marcel Dekker Inc., New York (1996).

[38] A. E. Raevskaya, A. L. Stroyuk, S. Y. Kuchmiy, J. Colloid Interface Sci., **302** (2006) 133–141.

[39] C. J. Panchal, M. S. Desai, V. a Kheraj, K. J. Patel, N. Padha, Semicond. Sci. Technol., **23** (2007) 015003.

[40] W. G. Osiris, A. A. M. Farag, I. S. Yahia, Synth. Met., **161** (2011) 1079–1087.

Chapter 5 - Growth and characterisation of ZnTe thin films

5.1 Introduction

Group II-VI compound semiconductor materials have found a wide application in a variety of solid-state electronic devices such as electroluminescence devices (for example, light emitting diodes), photosensors, thin-film transistors and solar cells. Zinc Telluride (ZnTe) is one of the II-VI binary compound semiconductors which find numerous applications in optoelectronic devices, switching devices and macro-electronic devices such as solar panels [1–4]. It is also a direct bandgap semiconductor with energy bandgap of 2.20–2.26 eV [5,6]. Over the years, ZnTe semiconductors have found a useful application as a p-type window material in hetero-junction solar cells fabricated from chalcogenide semiconductors such as CdS [3], CdSe [4] and CdTe. p-ZnTe is also a promising candidate for ZnTe/CdTe heterojunction device structures [6] and for development of graded bandgap solar cells. Apart from being used as a window material, thin film ZnTe semiconductors have also found a useful application as a back contact material to CdTe-based solar cells [7]. Due to the resistive nature of ZnTe thin films, researchers have doped ZnTe with Cu in order to achieve low resistivity electrical contacts thus making it more useful as a back contact to thin film solar cells [8].

The electrical conductivity type of ZnTe materials grown by conventional methods has been reported to be p-type. According to Mandel [9], n-type electrical conduction is difficult to achieve due to self-compensation. However, some researchers have been able to achieve n-type electrical conduction in ZnTe by extrinsic doping. Extrinsic dopants such as Al, Sn and Cl have been used to achieve n-type ZnTe [10–15]. Fischer et al. [10] and Chang et al. [11] have been able to prepare n-type ZnTe thin films by using Al as the dopant. Ogawa et al. [12] also obtained n-type ZnTe layers by doping with Al using triethylaluminium. DiNezza et al. [13] likewise reported the growth of n-type ZnTe films on GaSb substrates. These authors achieved the n-type electrical conductivity by thermally diffusing Al into the ZnTe film. Also, the authors reported the fabrication of ZnTe p-n homo-junction diodes with rectifying J-V characteristics and photo-voltaic (PV) behaviour to further confirm the successful growth of n-type ZnTe film. The uses of Cl and Sn as dopants to achieve n-ZnTe have also been demonstrated by Tao et al. [14] and Makhny et al. [15] respectively.

Several techniques have been used for the deposition of ZnTe thin films. Some of these methods are: closed space sublimation (CSS) [16], hydrothermal [17], molecular beam epitaxy [11], rf-magnetron sputtering [18], metallo-organic chemical vapour deposition (MOCVD) [19], metallo-organic vapour phase epitaxy (MOVPE) [20], thermal evaporation [21] and electrodeposition [22–25]. According to Mahalingam et al. [24], electrodeposition (ED) technique provides a suitable method to prepare continuous and thin semiconductor films. This work uses electrodeposition technique with a two-electrode set-up to develop thin films of ZnTe semiconductor.

The aims of this work as described in this chapter are to investigate and establish optimum growth parameters to electrodeposit both p-type and n-type ZnTe layers for applications in electronic devices. To achieve this, the material and optoelectronic properties of ED-ZnTe layers were examined using some of the analytical techniques discussed in Chapter 3. The effects of thickness variation of the ED-ZnTe thin films on their electrical and morphological properties have also been explored. The electronic qualities of the electroplated ZnTe layers were tested using the device structures, glass/FTO/n-ZnTe/metal contact and glass/FTO/p-ZnTe/metal contact. Also, p-n homo-junction diodes were fabricated purely from intrinsically doped electroplated ZnTe layers using the device structure glass/FTO/n-ZnTe/p-ZnTe/metal contact as a way of further confirming the authenticity of the electroplated n-type ZnTe layers.

5.2 Preparation of ZnTe electrolytic bath

The ZnTe thin films were deposited from electrolyte containing 0.015 M $ZnSO_4.7H_20$ (99.999% purity) and 2 ml of dissolved TeO_2 (99.995% purity) solution in 800 ml of de-ionised water. The dissolved TeO_2 solution was separately prepared by adding 30 ml of concentrated H_2SO_4 to 2 g of TeO_2 powder inside a 500 ml glass beaker. The reason for using concentrated acid is due to the inability of TeO_2 powder to dissolve completely in water. The solution was continuously stirred and 200 ml of de-ionised water was gradually added to the concentrated TeO_2 solution. As the gradual addition of water takes place, a clear solution was observed. The prepared TeO_2 solution was later subjected to continuous stirring and heating for ~40 minutes so as to aid complete dissolution of the TeO_2 powder. The pH value of the deposition electrolyte was maintained at 3.50±0.02 by using either NH_4OH or H_2SO_4. The growth temperature of

the electrolytic bath was ~80^{o}C and the solution was moderately stirred using a magnetic stirrer.

5.3 Voltage optimisation and growth of ZnTe thin films

Some analytical techniques such as cyclic voltammogram which gives valuable information about the suitable range of deposition potentials have been discussed in this section alongside other techniques used for general material characterisation.

5.3.1 Cyclic voltammogram

Cyclic voltammetry studies were performed in an aqueous solution that contains 0.015 M $ZnSO_4.7H_2O$ and 2 ml of dissolved TeO_2 solution at a pH of 3.50±0.02. A FTO coated glass substrate was used as the working electrode to study the mechanism of deposition of ZnTe thin films. A computerised GillAC potentiostat was used to carry out this voltammetric study at a sweep rate of 180 $mVmin^{-1}$. In this technique, a range of cathodic potentials from 0 to 2000 mV was applied across the electrolyte through the electrodes. The potentiostat was used in monitoring the current through the electrolyte as the voltages between electrodes were varied [26].

A typical cyclic voltammogram for FTO-coated glass substrate in the prepared electrolyte is shown in Figure 5.1. The forward curve illustrated at the inset of Figure 5.1 shows that tellurium (Te) begins to deposit at ~200 mV. It has been shown that Te being a nobler element deposits first [24,25] according to Equation (5.1).

$$HTeO_2^+ + 4e^- + 3H^+ = Te + 2H_2O \quad (5.1)$$

The redox potential (E^o) of Te and Zn with respect to the standard hydrogen electrode are ~+0.593 and -0.762 V respectively [27]. Since Te shows a more positive redox potential than Zn, it is therefore expected to deposit first. As shown in Figure 5.1, a rise observed in the forward current from point P reaches its first peak at point Q, and then starts to reduce due to deposition of Zn at ~930 mV and initial co-deposition of ZnTe on the cathode according to the chemical reaction shown in Equation (5.22).

$$Zn^{2+} + Te + 2e^- = ZnTe \quad (5.2)$$

The rise in deposition current density after ~930 mV shows rapid discharge of Zn and reaction between Zn and Te to form ZnTe. At low cathodic deposition potential, a Te-rich ZnTe layer is expected to be formed [25]. As the deposition potential increases, the

amount of Zn in the ZnTe layer gradually increases thus allowing a near stoichiometric ZnTe layer to be deposited. Thus, a voltage range between ~1350 to ~1750 mV has been identified to grow near stoichiometric ZnTe layers according to the experimental results.

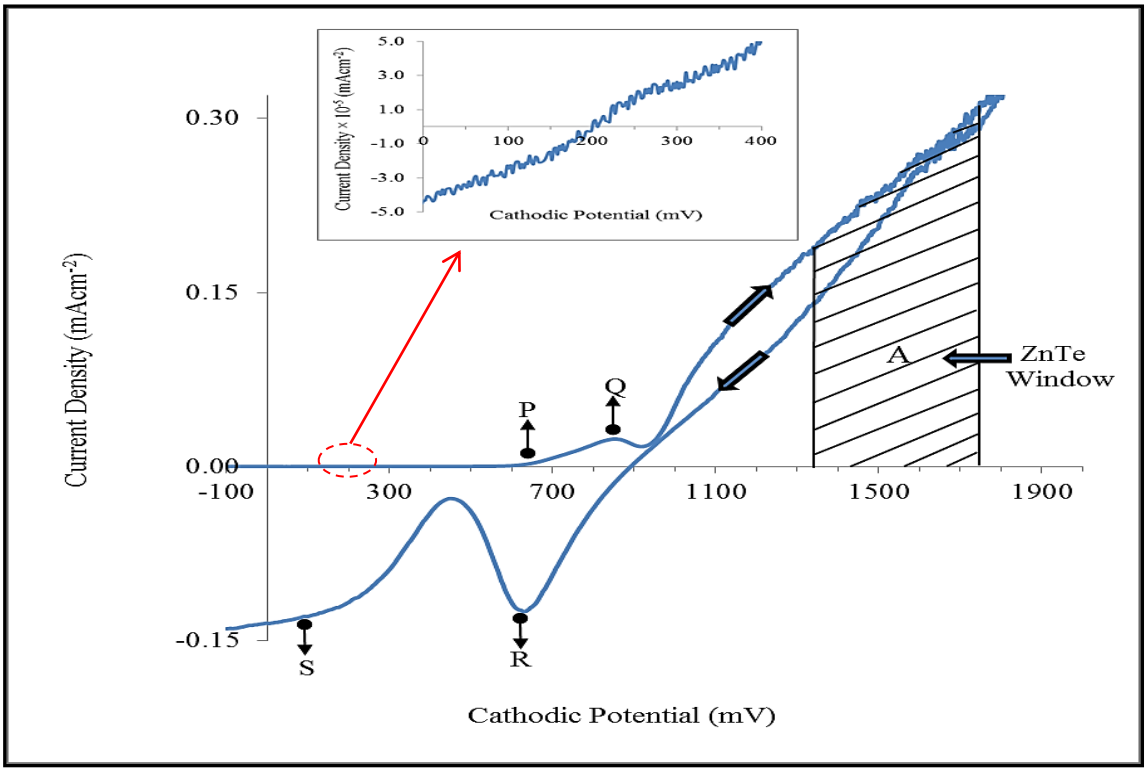


Figure 5.1. Cyclic voltammogram of electrolyte containing 0.015 M $ZnSO_4.7H_2O$ and 2 ml of dissolved TeO_2 in 800 ml of de-ionised water (pH=3.50±0.02, T=80^oC). Inset shows the transition voltage at which Te starts to deposit.

At very high cathodic potential (≥1750 mV), more Zn is deposited on the cathode thus leading to a Zn-rich ZnTe layer. The Zn-richness at high cathodic potential was observed by the change in colour of ZnTe thin film from red brick to dark colour and also by the deviation of the energy bandgap of ZnTe layers grown at V_g≥1750 mV from the bulk value of stoichiometric ZnTe material. Also at V_g≥1750 mV, more Zn which is metallic is deposited and this gradually leads to a reduction in the bandgap of ZnTe layer. In addition, electrolysis of water is also possible at these voltages. Liberation of atomic hydrogen on the cathode is an advantage in defect passivation in ZnTe films but formation of hydrogen bubbles can be a disadvantage in causing peeling of the deposited layer. Therefore, application of higher voltages should be avoided in order to grow ZnTe films avoiding metallic Zn and formation of H_2 bubbles on the cathode.

From the reverse cycle of the current-voltage (I-V) curve shown in Figure 5.1, the current flow transits from the positive to the negative at ~900 mV and peaks at point R. Point R indicates the dissolution of elemental Zn and removal of Zn from ZnTe layer formed on the cathode. The dissolution of Te from the surface of the cathode occurs at the broad peak point S. It has thus been shown that voltammogram is helpful in determining the approximate deposition potential range to grow ZnTe thin films. It is therefore essential to carry out cyclic voltammetry study to determine the approximate deposition potential range to grow ZnTe thin films before optimising the deposition voltage required to grow a near stoichiometric material.

5.3.2 Structural Analysis

Two techniques namely X-ray diffraction and Raman spectroscopy were used in investigating the structural properties of electroplated ZnTe layers.

5.3.2.1 X-ray diffraction studies

The structural properties of ED-ZnTe layers were studied at different growth potential using XRD analytical technique. Samples of ZnTe layers were electrodeposited on glass/FTO substrates at different cathodic potential ranging from 1350 to 1750 mV; this was done in order to determine their crystal structure and phases and to identify the optimum growth potential to achieve highest crystalline and stoichiometric ZnTe layers. Figures 5.2 (a) and 5.2 (b) show the XRD spectra obtained for as-deposited (AD) and heat-treated (HT) ZnTe layers respectively. The heat-treatment of the layers was carried out at 300^{o}C for 10 minutes in air. The XRD spectra revealed the formation of polycrystalline ZnTe thin films and the crystal structure was observed to be hexagonal. For the samples grown between deposition potential (V_g) of 1500–1700 mV, the crystal plane of preferred orientation was found to be along (002) hexagonal plane for the most prominent peak; this peak was observed at different position of angle 2θ as illustrated in Table 5.1. Apart from the most prominent peak which occurred along the (002) plane, other peaks with lower intensities were also observed for both AD- and HT-ZnTe layers. For the AD-ZnTe layers, the peaks occurred along (100), (102), (110) and (112) planes; while for the HT-ZnTe layers, the peaks were observed at (100), (102) and (112) planes.

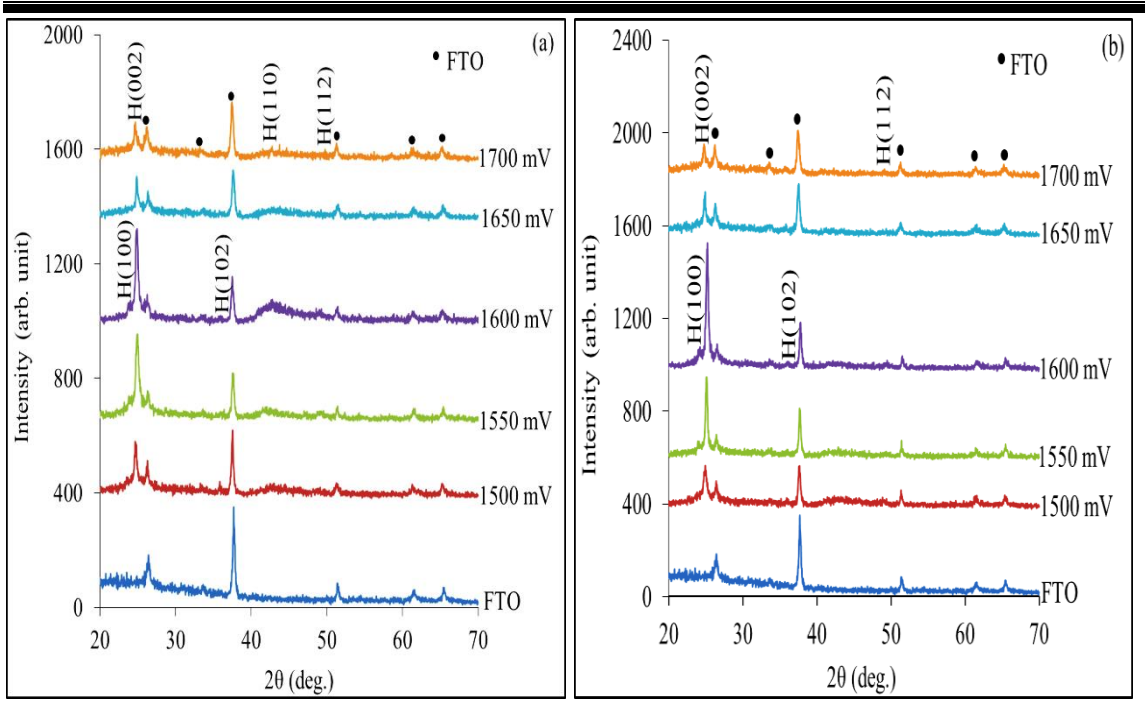


Figure 5.2. XRD spectra of: (a) as-deposited and (b) heat-treated (at 300^{o}C for 10 minutes in air) ZnTe layers grown at different cathodic potentials.

In order to identify the crystal structures of the electroplated thin films, the observed d-spacing values of the most prominent peak of ED-ZnTe thin films grown at different cathodic potentials from 1500–1700 mV were compared with the reported values in JCPDS Reference data as illustrated in Table 5.1. Table 5.1 shows that the observed data from the results of the XRD peak analysis correlates with the reported values from JCPDS with reference code: 00-019-1482 for ZnTe with hexagonal crystal phase. As observed from these experimental results, the position of angle 2θ for the preferred orientation varies from one cathodic potential to the other. Figure 5.3 (a) shows the variation of the preferred orientation peak position versus the cathodic potential. As shown in Figure 5.3 (a), the position of angle 2θ increases from 1500 mV to 1600 mV; beyond this voltage, a decrease was observed in the position. The shift in the position at which the preferred orientation occurs may be as a result of variation in the grain sizes of the thin film material.

Table 5.1. XRD analysis of as-deposited and heat-treated ZnTe layers grown at different cathodic potentials. Note that the analysis illustrates the contrast between the experimentally observed parameters and reported JCPDS reference code values for the peak along the preferred plane of orientation.

Sample	V_g (mV)	2θ (deg.)		Lattice Spacing D (Å)		Plane of Orientation (hkl)	Chemical Formular/Phase
		Observed	Reference	Observed	Reference		
As-deposited ZnTe thin films	1500	24.79	25.06	3.59	3.55	002	ZnTe (Hex)
	1550	24.92	25.06	3.57	3.55	002	ZnTe (Hex)
	1600	24.96	25.06	3.57	3.55	002	ZnTe (Hex)
	1650	24.87	25.06	3.58	3.55	002	ZnTe (Hex)
	1700	24.70	25.06	3.61	3.55	002	ZnTe (Hex)
Heat-treated ZnTe thin films	1500	24.93	25.06	3.57	3.55	002	ZnTe (Hex)
	1550	25.01	25.06	3.56	3.55	002	ZnTe (Hex)
	1600	25.06	25.06	3.55	3.55	002	ZnTe (Hex)
	1650	24.88	25.06	3.58	3.55	002	ZnTe (Hex)
	1700	24.75	25.06	3.60	3.55	002	ZnTe (Hex)

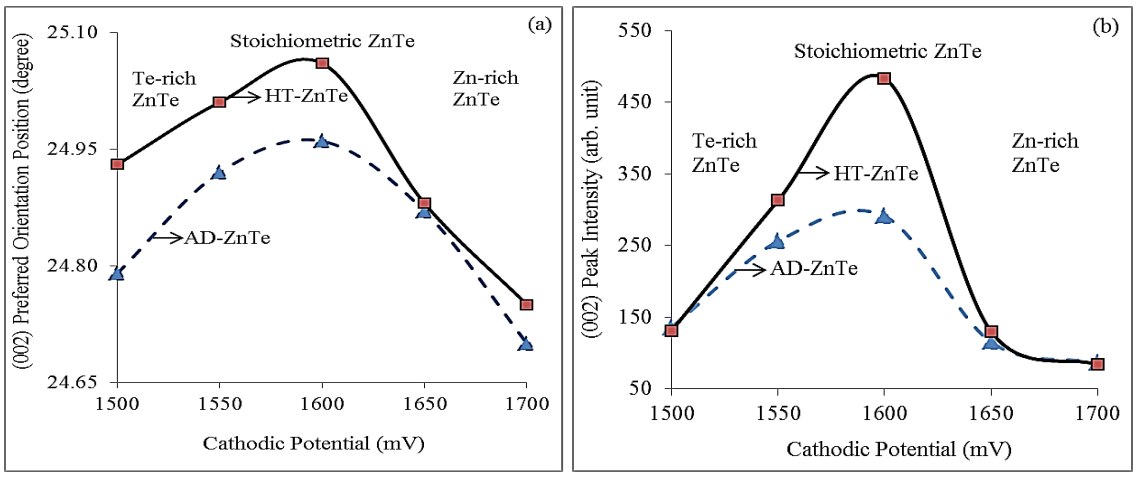


Figure 5.3. Variation of (a) preferred orientation position along (002) plane versus cathodic potential and (b) XRD peak intensity of (002) ZnTe versus cathodic potential for AD- and HT-ZnTe layers.

As explained in section 5.3.5, cathodic potential at which the material is grown has effect on the surface morphology of the thin films and size of its grains. At V_g=1600 mV, the position of the preferred orientation along (002) plane for the HT-ZnTe layer coincide with the reported standard values as indicated in Table 5.1. A trend similar to Figure 5.3 (a) was also observed in Figure 5.3 (b) when the XRD peak intensity of (002)

ZnTe was plotted as a function of cathodic potential. Figure 5.3 (b) shows that the highest peak intensity for the (002) preferred orientation occurred at a cathodic potential of 1600 mV. At this V_g, an increase in peak intensity was observed after annealing in air as also shown in Figure 5.2 (a) and 5.2 (b). This indicates that annealing helps in improving the crystallinity of as-deposited layers. The high peak intensity reveals the crystalline and stoichiometric nature of the material. This result shows that stoichiometric layer of ZnTe thin films can be grown at the cathodic growth potential of 1600 mV.

To further identify and compare all the peaks for AD- and HT-ZnTe layers grown at a V_g of 1600 mV, the two spectra were plotted on the same scale for easy comparison; this is shown in Figure 5.4. The presence of low peak intensity along the (002) plane and the broad peak along (110) plane for AD-ZnTe layer grown at 1600 mV make the material to be less crystalline. It was observed that after annealing the thin film material in air, the material crystallinity was improved as a result of increase in peak intensity along the (002) plane and removal of the broad peak along (110) plane. The summary of XRD data for the ZnTe thin films grown at V_g=1600 mV is shown in Table 5.2. The crystallite size (*D*) obtained from the full width at half maximum (FWHM, β) was estimated using the Scherrer's formula in Equation (3.12) of Chapter 3.

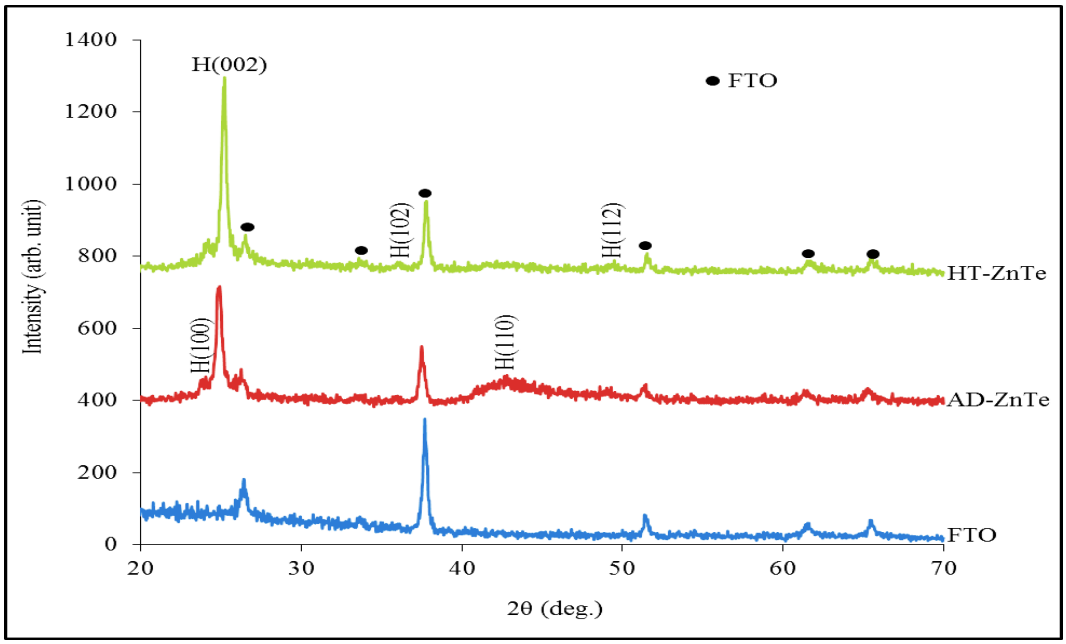


Figure 5.4. XRD spectra of AD- and HT-ZnTe layers grown at optimum cathodic potential of 1600 mV.

Table 5.2. Summary of XRD data for AD- and HT-ZnTe layers grown at optimum voltage of 1600 mV.

Sample	Angle (2θ) (Deg.)	Peak Intensity (%)	d-Spacing (Å)	FWHM (Deg.)	Crystallite size, D (nm)	Plane of orientation (h k l)	Hex-Reference Code Matching
AD-ZnTe at 1600 mV	23.85	35.5	3.73	0.369	23.0	(100)	00-019-1482
	24.96	289.7	3.57	0.260	32.8	(002)	00-019-1482
	35.79	13.7	2.56	0.370	23.6	(102)	00-019-1482
	42.82	38.9	2.11	0.660	13.5	(110)	01-080-0009
	49.02	17.6	1.86	0.990	9.2	(200)	01-080-0009
HT-ZnTe at 1600 mV	24.09	51.9	3.69	0.350	24.3	(100)	01-080-0009
	25.06	483.7	3.55	0.227	34.5	(002)	00-019-1482
	36.05	16.2	2.49	0.390	22.4	(102)	01-080-0009
	49.45	19.6	1.84	0.779	11.7	(112)	00-019-1482

5.3.2.2 Raman spectroscopy

The structural quality of thin film materials can also be determined using a non-destructive Raman scattering technique. The laser power and wavelength used are 15 mW and 514 nm respectively. The laser power was reduced from 100% (30 mW) to 50% (15 mW) to avoid damage to the surface of the layer exposed to the beam. A 100x objective lens was used in the Raman microscope. The Raman instrument was calibrated by using the 520 cm^{-1} Raman shift of the reference silicon wafer. The Raman spectra of ZnTe thin films can exist in both longitudinal and transverse optical modes. According to Irwin et al. [28], the first-order Raman spectrum consists of two peaks namely longitudinal optical (LO) mode and transverse optical (TO) mode. The higher frequency is described as the LO mode while the lower frequency is the degenerate TO mode. Figure 5.5 shows a typical Raman spectra of AD- and HT-ZnTe thin films grown at a cathodic potential of 1600 mV for 30 minutes. The observed peaks in both LO and TO modes are higher in HT-ZnTe layers than AD-ZnTe layers.

The 1TO Raman peak for ZnTe was observed at 165 cm^{-1} and the 1LO phonon mode was observed at 197 cm^{-1}. The second order LO (2LO) phonon mode was also observed for both AD- and HT- ZnTe layers with less peak intensity at the phonon frequency of 397 cm^{-1}. The 1LO and 2LO peaks of ZnTe nanorods reported by Zhang et al. [29] occurred at 205 cm^{-1} and 410 cm^{-1}. When compared with the experimental results

reported by Zhang et al., a small redshift was observed in the 1LO peak and 2LO peaks from 205 cm^{-1} to 197 cm^{-1} and 410 cm^{-1} to 397 cm^{-1} respectively. This shift can be due to reasons such as different thickness of the thin film used for the experimental purpose, composition of Zn to Te in the ZnTe layer [30,31], defects and stresses in ZnTe thin films. Two other peaks at ~120 cm^{-1} and ~142 cm^{-1} were also observed below the 1TO Raman phonon peak. These peaks arise as a result of elemental Te or presence of Te-rich phases in the material [29]. Raman peaks at low frequency of 121.5 cm^{-1} and 141.2 cm^{-1} have also been reported in other II-VI binary compounds containing Te such as CdTe [32]. Precipitates of elemental Te is a common feature during growth of Te containing semiconductors; this is well documented by the research based on CdTe thin films [32,33].

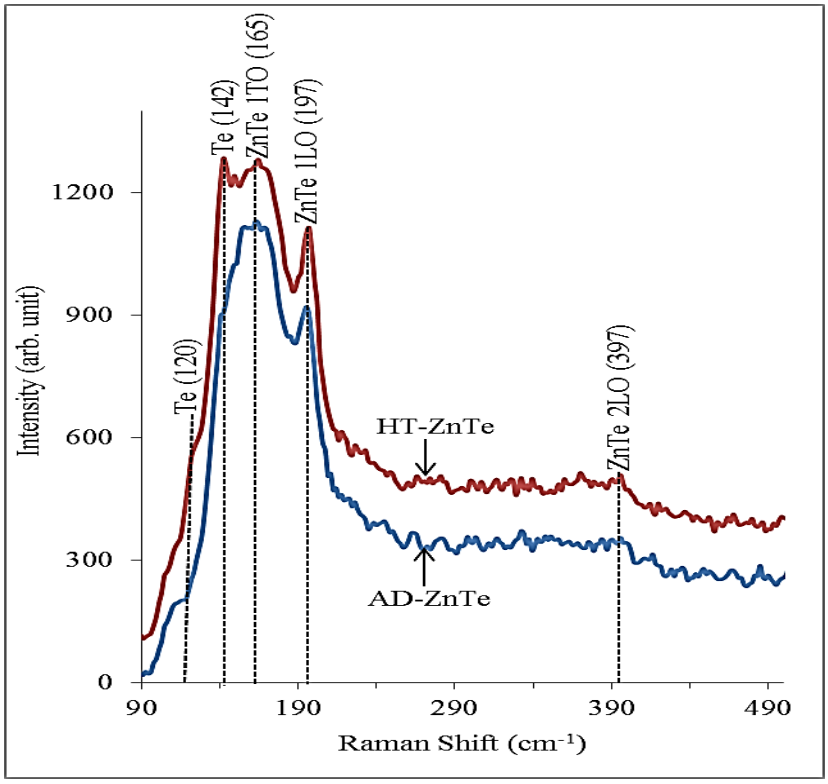


Figure 5.5. Typical Raman spectra for AD- and HT-ZnTe layers grown at 1600 mV for 30 minutes. The spectra shows both transverse optical (TO) and longitudinal optical (LO) phonon modes.

5.3.3 Optical absorption studies

The optical absorption measurements were carried out at room temperature in order to obtain the energy bandgap (E_g) of the ED-ZnTe thin films. The measurements were carried out on ZnTe layers grown between 1350–1750 mV in the wavelength range

350–800 nm. Figures 5.6 (a) and 5.6 (b) show the optical absorption graphs that are used in estimating the energy bandgaps of both AD- and HT-ZnTe layers. The bandgap estimation was done by extrapolating the curve tangent line to the photon energy axis when A^2=0. Figure 5.7 illustrates how the estimated energy bandgaps from optical absorption measurements vary with the cathodic potential for both AD- and HT-ZnTe layers. The AD-ZnTe layers have energy bandgaps in the range (1.70–2.60) eV while the energy bandgaps of HT-ZnTe layers range from (1.90–2.60) eV. At 1600 mV, the E_g of both AD- and HT-ZnTe layers is ~2.20 eV; this value happens to fall in the vicinity of the bandgap of bulk value of stoichiometric ZnTe layers. This signifies that the cathodic potential of 1600 mV can be used in growing near stoichiometric ZnTe layers. The high intensity of XRD peaks, formation of large grains (from SEM and AFM measurements) and accurate bandgap of 2.20 eV (from optical absorption measurements) for materials grown at 1600 mV show strong evidence for growing near stoichiometric and more crystalline ZnTe layers at this voltage.

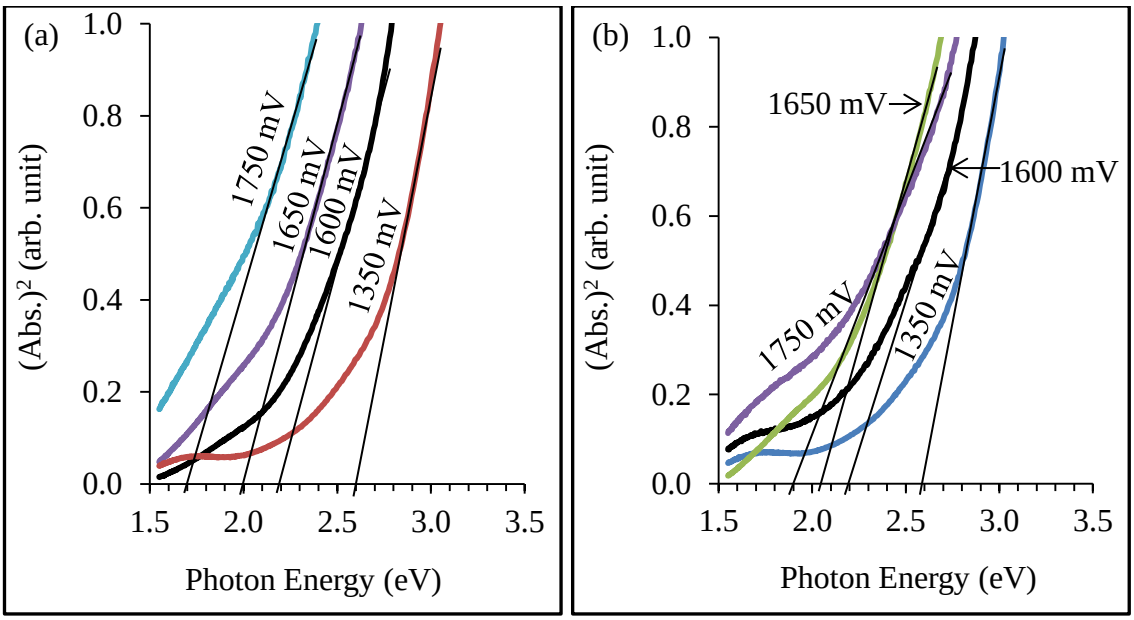


Figure 5.6. Optical absorption graphs for ZnTe layers grown between 1350–1750 mV, (a) AD-ZnTe layers and (b) HT-ZnTe layers.

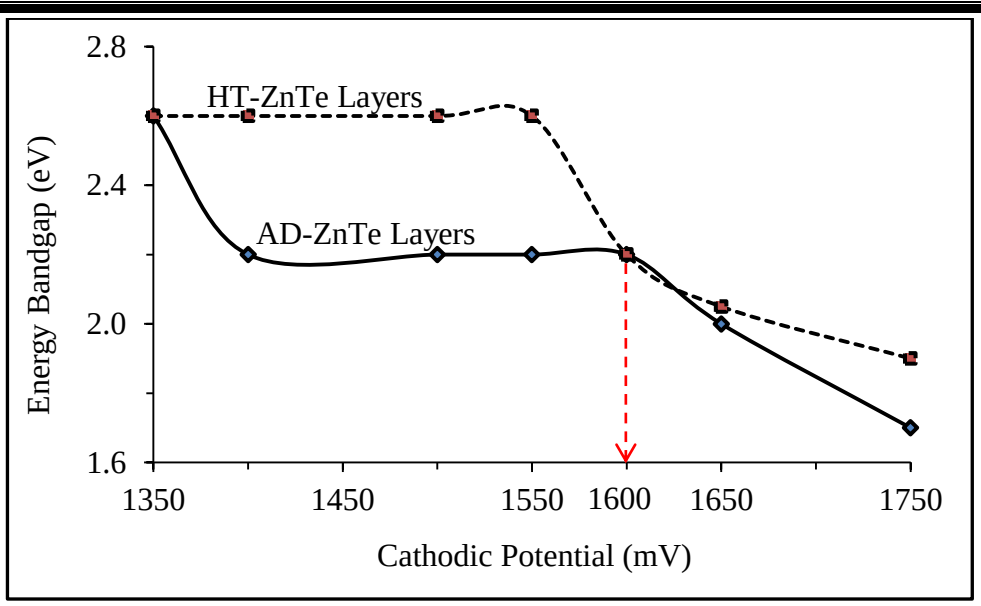


Figure 5.7. Variation of the energy bandgaps of ZnTe layers as a function of cathodic deposition potential, for both AD- and HT-ZnTe layers.

5.3.4 Photoelectrochemical cell measurements

PEC cell measurements were carried out so as to determine the electrical conductivity type of the ED-ZnTe layers. Figure 5.8 shows the results of the PEC signals observed for AD- and HT-ZnTe layers. The results of the PEC signals observed for AD- and HT-ZnTe layers deposited between 1350 and 1800 mV show both p- and n-type electrical conduction. p-type electrical conduction was observed between deposition potential (V_g) of 1350–1600 mV while at $V_g \geq 1620$ mV, negative PEC signals were obtained thus indicating n-type ZnTe layers. The p-type ZnTe was achieved at low potential due to Te-richness in the ZnTe layers. The n-type electrical conductivity was achieved at higher cathodic potential due to Zn-richness. Fauzi et al. [25] reported only p-type ZnTe even at higher cathodic potentials. This can be due to presence of higher concentrations of Te in the electrolyte. The authors attributed this to the likely domination of native defects related to Te-richness in ZnTe material thus making it to be p-type under all growth conditions. Mandel [9] and John et al. [8] attributed the difficulty in achieving n-type ZnTe thin films to self-compensation in the material. However, in this work, n-ZnTe layers have been successfully electrodeposited at higher cathodic potentials thus eliminating the possibility of native defect domination and self-compensation in ZnTe layers. The possibility of growing n-ZnTe could also arise as a result of fine control of Te by using dissolved TeO_2 solution in the ZnTe electrolytic bath. The n- and p- type

ZnTe layers were further tested by fabricating a p-n homo-junction device structure with rectifying ability as explained in section 5.5.2.

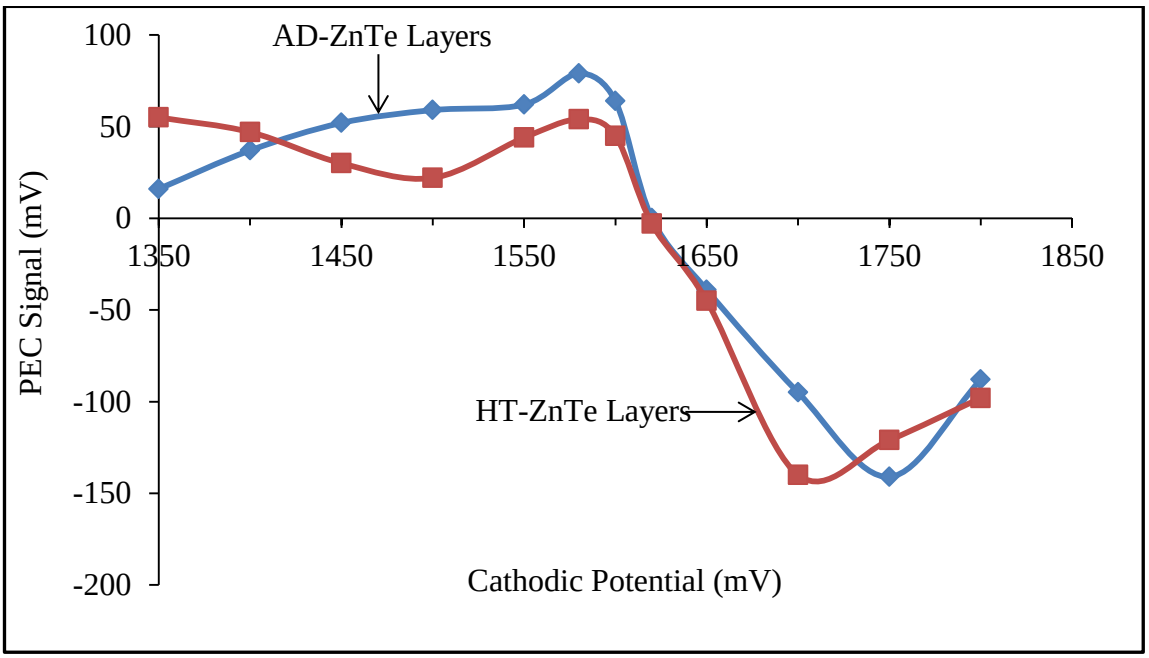


Figure 5.8. Typical PEC signals as a function of deposition potential for AD- and HT-ZnTe layers, showing n- and p-type electrical conduction. Te-richness at voltages less than 1620 mV shows p-type electrical conduction while Zn-richness at voltages greater than 1620 mV shows n-type electrical conduction.

5.3.5 Morphological Analysis

Two techniques namely scanning electron microscopy and atomic force microscopy as discussed in this section were used to investigate the morphological properties of electroplated ZnTe layers.

5.3.5.1 Scanning electron microscopy

Scanning electron microscopy (SEM) technique was used to study the surface morphology of heat-treated ZnTe thin films grown at the stoichiometric potential of 1600 mV and voltages on both sides of this potential. The three SEM images illustrated in Figures 5.9 (a-c) with magnification of 120,000 are for heat-treated ZnTe layers grown for 30 minutes at three different cathodic potentials namely 1550, 1600 and 1650 mV respectively. The heat-treatment was done in air at 300^{o}C for 10 minutes. The SEM images in Figures 5.9 (a-c) show that the films are uniformly covered with grains of varying sizes. Large grains or agglomerations observed are collection of small crystallites. In Figure 5.9 (a), the grain size of the HT-ZnTe layer ranges from ~91–309

nm while in Figure 5.9 (b), the grain size ranges from ~127–509 nm. In Figure 5.9 (c), the grain size ranges from ~73–291 nm. The largest grain size was observed in the ZnTe layer grown at 1600 mV (Figure 5.9 (b)). This result also confirms the XRD results where V_g of 1600 mV show the highest peak intensity in both as-deposited and heat-treated layers.

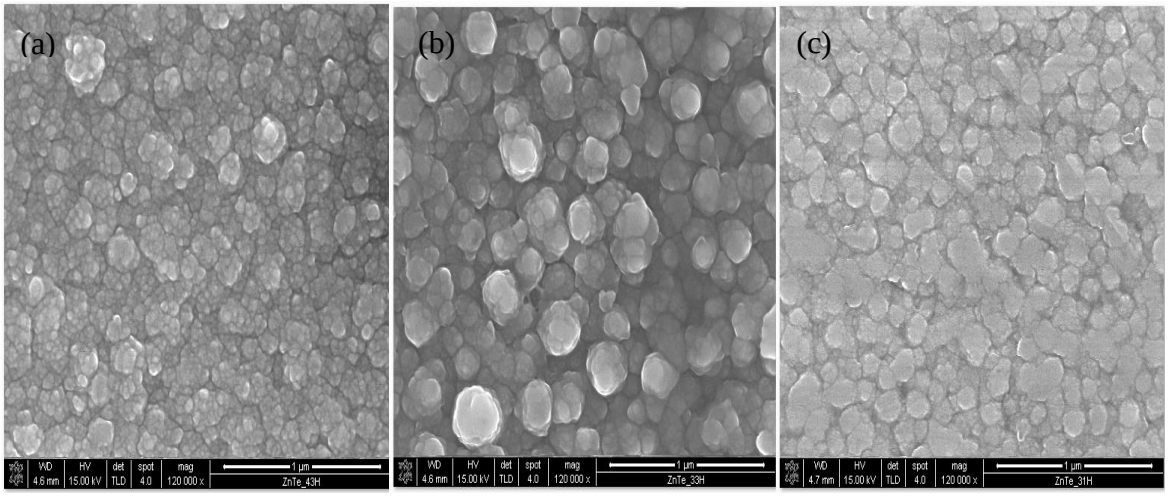


Figure 5.9. SEM images of HT-ZnTe thin films grown on FTO substrates deposited at a pH of 3.50±0.02, growth time (t_g)=30 minutes. (a) For V_g=1550 mV, (b) V_g=1600 mV and (c) V_g=1650 mV.

5.3.5.2 Atomic force microscopy

Atomic force microscopy (AFM) technique was performed using Nanoscope IIIa multimode atomic force microscope. The measurements were carried out to study the surface morphology, growth pattern and to also measure the grain sizes and surface roughness of ED-ZnTe layers. The AFM images showing the surface morphology of AD- and HT-ZnTe layers deposited at 1600 mV for 30 minutes on glass/FTO substrates are shown in Figure 5.10 (a) and 5.10 (b) respectively. The measured grain sizes for AD- and HT-ZnTe layers lie in-between ~(46–323) and ~(139-520) nm respectively. These results do agree with the ones obtained from SEM images of HT-ZnTe layers deposited at 1600 mV. As seen from the AFM results, a reduction was seen in the surface roughness of ZnTe layers after annealing. The average surface roughness measured for AD-ZnTe layer is ~45 nm; after annealing, the surface roughness reduced to ~35 nm. The 3D–AFM images of AD- and HT- ZnTe layers are shown in Figure 5.10 (c) and 5.10 (d) respectively. The 3D–AFM images reveal the growth pattern; both figures show that the ZnTe layers have a columnar growth with varying sizes. According to Fauzi et al. [25], the varying sizes of the columnar shaped thin film

material leaves unwanted gaps in-between the columnar materials. These undesirable gaps cause shorting of devices thus leading to a poor performance when used in solar cells fabrication.

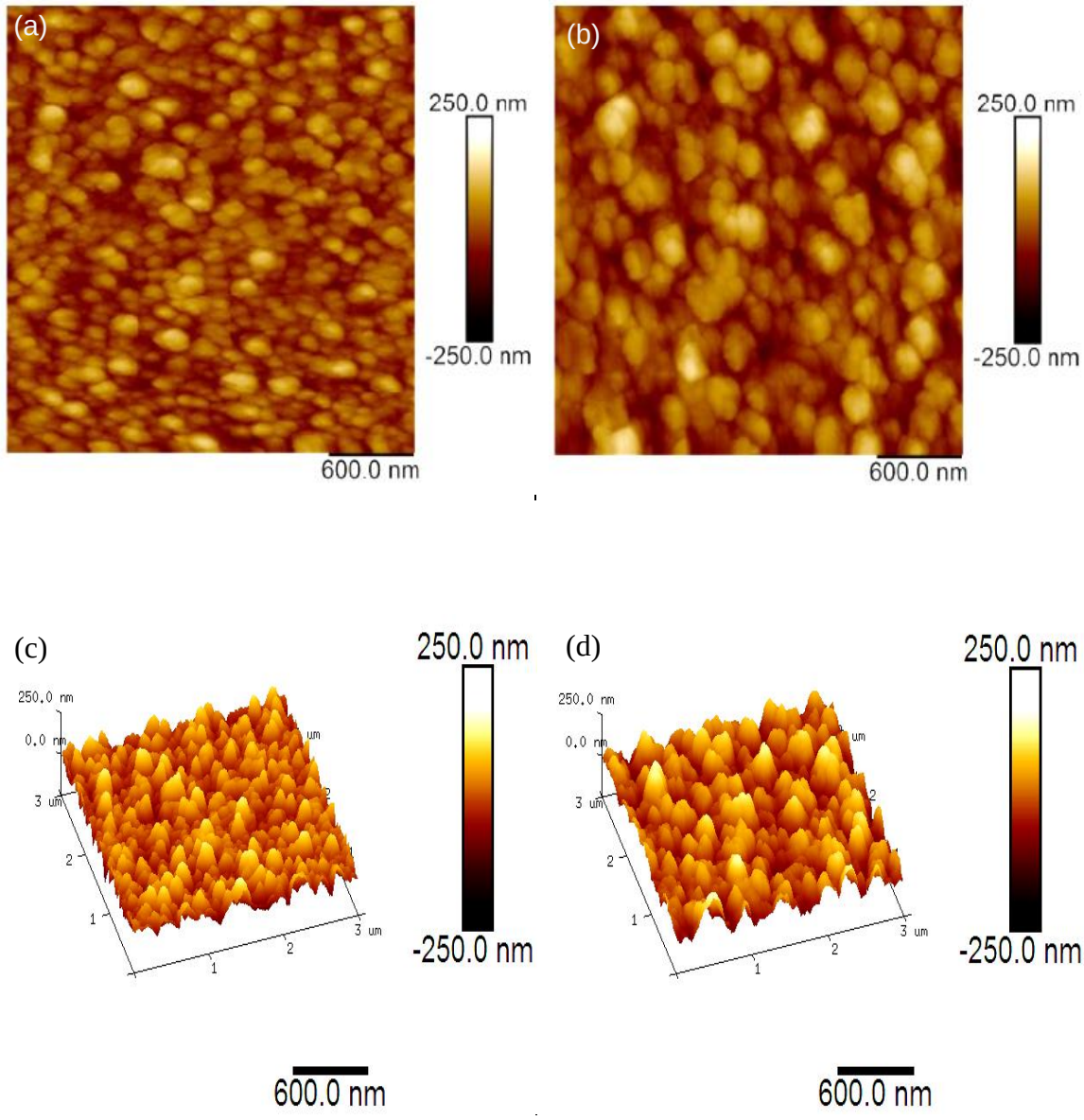


Figure 5.10. AFM images of ZnTe layers grown at 1600 mV for 30 minutes (a,c) AD-ZnTe layers and (b,d) HT-ZnTe layers at 300^{o}C for 10 minutes in air.

5.3.6 Compositional study of electroplated ZnTe layers

The percentage of Zn and Te atoms present in the as-deposited ZnTe thin films were determined using EDX technique. Five samples grown at different cathodic potentials in the range 1500-1700 mV at 50 mV intervals were used for the analysis. Figure 5.11 (a) and 5.11 (b) show the EDX spectra of AD-ZnTe layers grown at 1500 and 1700 mV respectively; while Figure 5.12 summarises how the atomic percentage of Zn and Te

elements present in the ZnTe thin film changes with deposition potential. As illustrated in Figure 5.11 (a), the atomic percentage of Zn:Te at V_g=1500 mV was 38.1:61.9 showing that the AD-ZnTe layer is more rich in Te than in Zn. In Figure 5.11 (b), the composition of Zn:Te atoms at V_g=1700 mV was found to be 68.6:31.4 illustrating that the ZnTe thin film is more rich in Zn than in Te. The results obtained from the EDX analysis further confirmed our earlier statement in section 5.3.4 that p-type ZnTe was achieved at low cathodic potential due to Te-richness while the n-type electrical conductivity was achieved at higher cathodic potential due to Zn-richness.

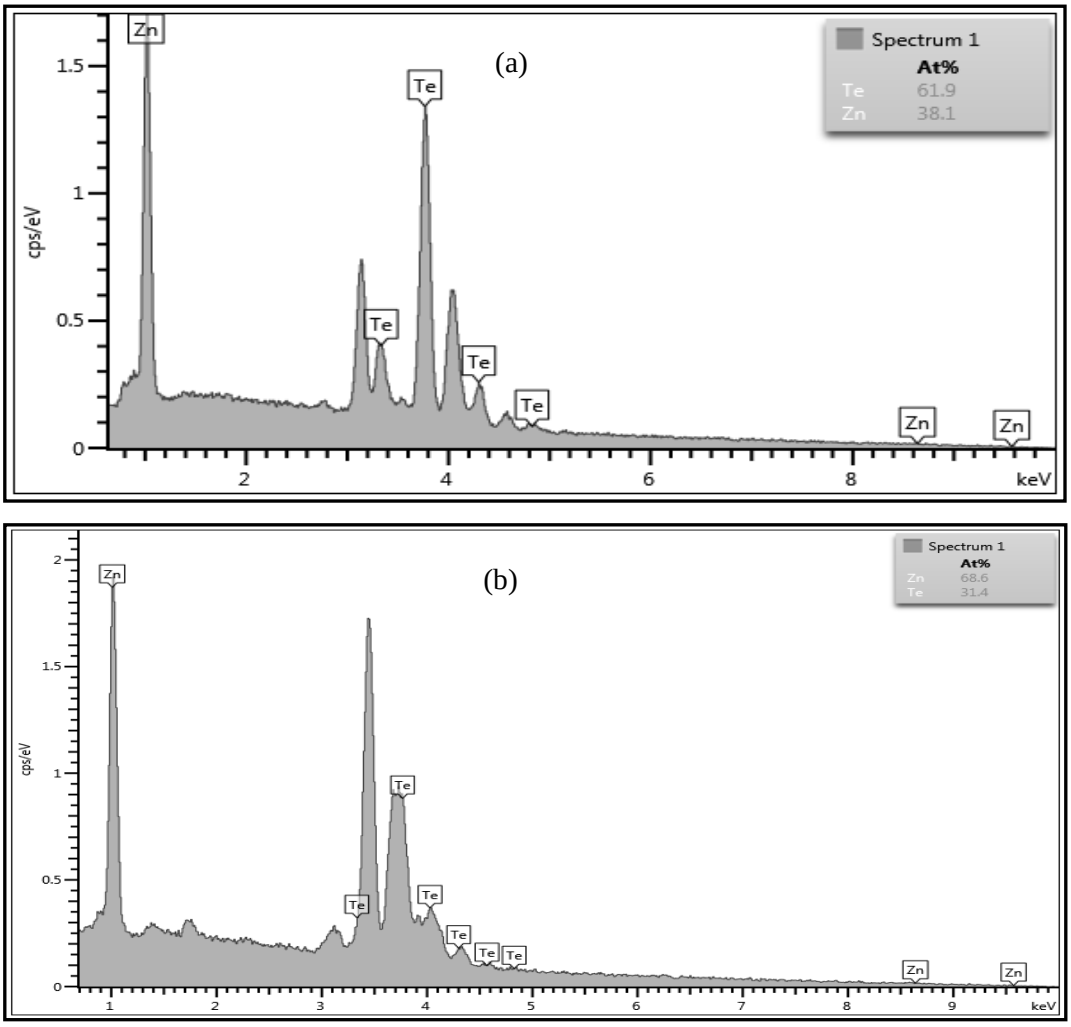


Figure 5.11. EDX spectra of AD-ZnTe layers on FTO substrates grown for 30 minutes at (a) V_g=1500 mV and (b) V_g=1700 mV.

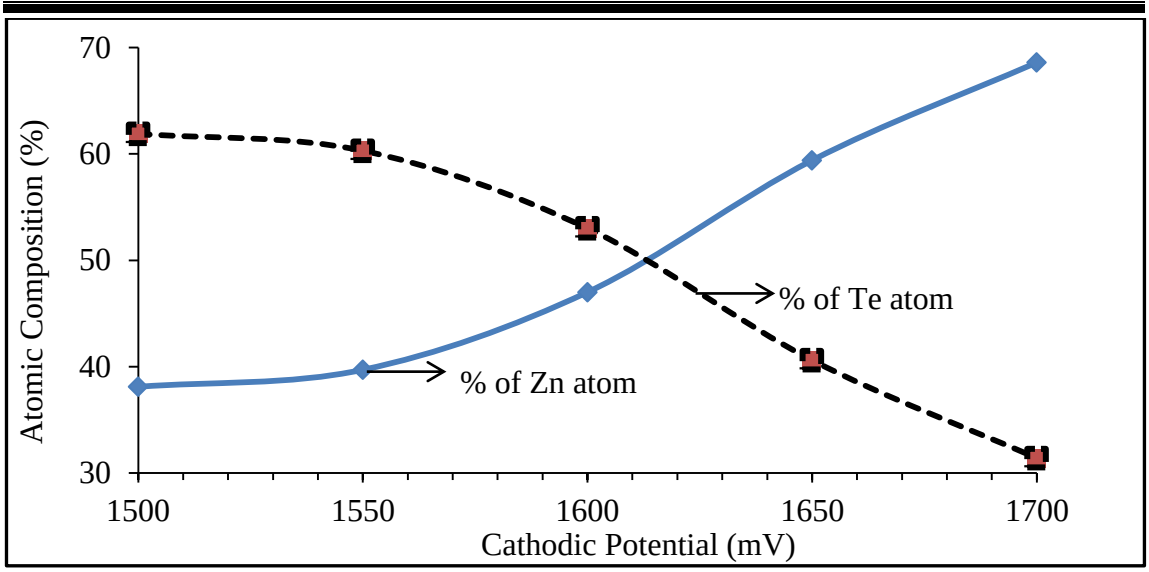


Figure 5.12. Graphical representation of percentage compositions of Zn and Te atoms in AD-ZnTe thin films at different deposition cathodic potential. Note the richness of Te at low cathodic voltages and richness of Zn at high cathodic voltages.

The PEC results (Figure 5.8) of ZnTe layers grown below ~1620 mV show that p-type materials are grown due to Te-richness. Similarly from Figure 5.8, n-type ZnTe layers are grown at voltages above ~1620 mV due to Zn-richness. The EDX result explains the possibility of growing Zn-rich ZnTe thin films at higher cathodic potentials and Te-rich ZnTe thin films at lower cathodic potentials thus confirming the likelihood of having n- and p-type ZnTe layers at higher and lower cathodic potentials respectively. Figure 5.12 shows that as the growth voltage changes, the ratio of Zn:Te atoms in the ED-ZnTe layers likewise varies. As the growth voltage increases from 1500-1700 mV, the % of Te atoms decrease while the % of Zn atoms increase. This result shows that by changing the deposition potential, the stoichiometry and the material properties (such as electrical, morphological, structural and optical) do change. These very results can be used in explaining the probable reason while a reduction was observed in the bandgap of ZnTe layers (Figure 5.6) grown at higher cathodic potentials. At higher cathodic growth voltage, more Zn is electrodeposited than Te thus leading to a gradual reduction in the bandgap of ZnTe layers due to the metallic nature of Zn.

5.4 Thickness measurement of ZnTe layers

The experimental thicknesses of AD-ZnTe layers were obtained by using Microfocus Optical Thickness Profilometer measurement system while the theoretical thicknesses

were estimated using Faraday's law of electrolysis. Thickness (T) of the layer in cm is given by Equation (5.3).

$$T = \frac{JtM}{nF\rho} \tag{5.3}$$

where M is the molecular weight of ZnTe thin film (193.01 $gmol^{-1}$), t is the growth time in seconds, J is the average current density observed during deposition in Acm^{-2}, F is Faraday's constant (96485 $Cmol^{-1}$), ρ is the density of ZnTe (6.34 gcm^{-3}) and n is the total number of electrons required in the deposition of 1 mole of ZnTe (n=6 as given by Equations (5.1) and (5.2)).

The samples used for this measurement were grown at 1600 mV for different duration (0.5–4.0 hours). This experiment was carried out in a ZnTe electrolyte containing excess Te. The composition of the ZnTe bath contains 0.015 M $ZnSO_4.7H_2O$ and 10 ml of dissolved TeO_2 in 800 ml of de-ionised water. The experimentally measured values and theoretically estimated values are shown in Figure 5.13. As expected, the thickness of AD-ZnTe layers increase with increase in deposition time. As illustrated in Figure 5.13, an approximate linear variation of thickness with growth time was observed in both theoretical and experimental curves. The theoretically estimated thickness is generally higher than the experimentally measured thickness because not all the electronic charges used in the theoretical estimation are actually utilised in the deposition of ZnTe thin films. Some of these charges flow through the electrolyte and are used for electrolysis of water thus making the experimentally measured thicknesses to be less than the theoretically estimated values.

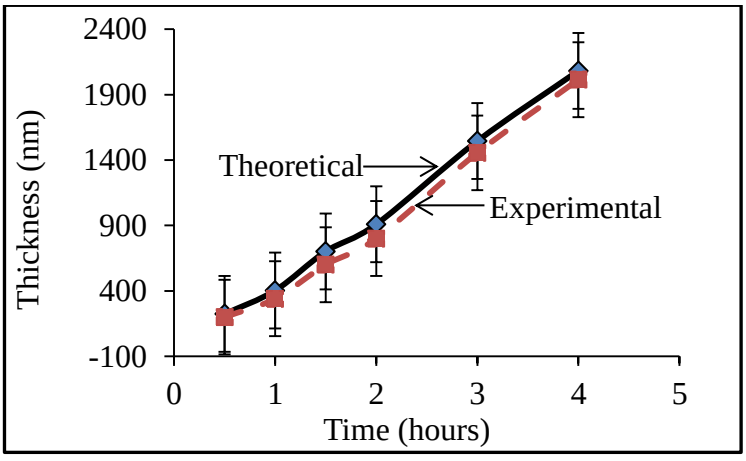


Figure 5.13. Experimental and theoretical estimation of thickness of as-deposited ZnTe layers as a function of deposition time.

5.4.1 Effect of thickness on electrical properties of ZnTe layers

The electrical properties of ZnTe layers grown at 1600 mV was studied at different thicknesses using techniques such as PEC cell measurement, I-V and C-V.

5.4.1.1 Thickness effect on PEC signals

PEC cell measurements were carried out so as to determine the effect of thickness variation on the magnitude of PEC cell signals of AD- and HT-ZnTe layers grown at 1600 mV. It should be recalled that at this V_g, a positive PEC signal was obtained as earlier explained in section 5.3.4. Table 5.3 shows the PEC signals obtained for AD- and HT-ZnTe layers at different growth durations ranging from 0.50 to 4.00 hours while Figure 5.14 is the diagrammatic illustration of PEC signals given in Table 5.3. As seen in Figure 5.14, the highest and lowest PEC signals were observed at the growth time of 2.00 and 4.00 hours respectively. For the HT-ZnTe layers, a progressive increase was observed from 0.50 to 2.00 hours. Beyond 2.00 hours of thin films deposition, a drastic reduction took place in the magnitude of the PEC signals.

Table 5.3. PEC signals of AD- and HT-ZnTe at different growth duration ranging from 0.50 to 4.00 hours.

	PEC Signals (mV)	
Growth Time (hours)	AD-ZnTe	HT-ZnTe
0.50	+68	+64
1.00	+62	+66
1.50	+61	+70
2.00	+79	+85
3.00	+42	+30
4.00	+33	+09

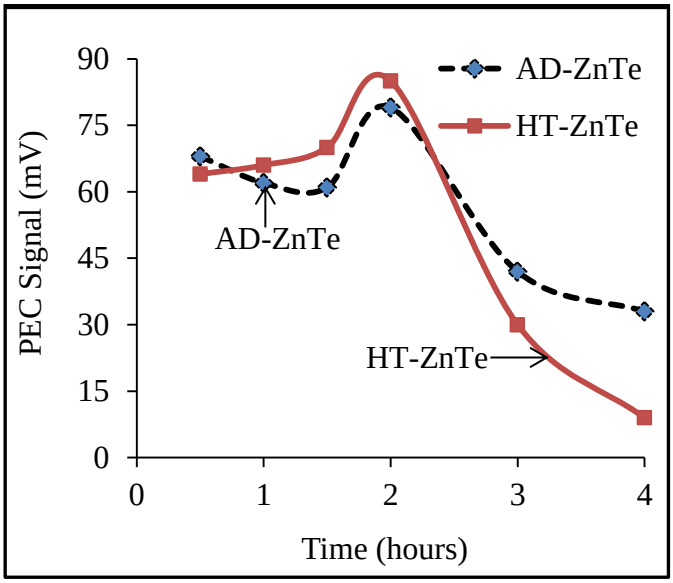


Figure 5.14. Typical PEC signals as a function of deposition time for AD- and HT-ZnTe layers grown at a cathodic potential of 1600 mV.

5.4.1.2 Thickness effect on mobility and Fermi level position

I-V and C-V techniques were both used to investigate how thickness variation affects the resistivity, acceptor density, mobility and position of Fermi level in p-ZnTe layers.

The device structures glass/FTO/p-ZnTe/Au were fabricated to investigate the material resistivity using I-V technique while C-V technique was used to investigate the acceptor density and Fermi level position of glass/FTO/p-ZnTe/Al device structures. Approximately same thicknesses of ZnTe layers were used for both I-V and C-V experiments. Table 5.4 gives the summary of results obtained from I-V and C-V measurement analyses. It was noticed that as the thickness of the ZnTe layer increases, the depletion width (W) increases while the acceptor density (N_A) decreases. The highest conductivity and mobility occurred at growth time of 2.00 hours. It was also observed that as the material thickness increases, the Fermi level position moves away from the valence band maximum towards the mid-gap position. These experimental results show that the thickness of the semiconductor material influences the Fermi level position of electroplated ZnTe layers.

Table 5.4. Effect of thickness of ZnTe layers on electrical parameters obtained from I-V and C-V techniques.

Time *(hours)*	Thickness (nm)	C_o (pF)	W (nm)	N_A (cm^{-3})	σ $(\Omega cm)^{-1}$	$\mu = \sigma/eN$ ($cm^2V^{-1}s^{-1}$)	E_F-E_v (eV)
0.5	223.4	2060	140	1.56×10^{18}	2.22×10^{-5}	0.0001	0.01
1.0	403.2	1090	265	1.21×10^{17}	3.05×10^{-5}	0.0016	0.08
1.5	701.4	608	476	5.66×10^{16}	4.96×10^{-5}	0.0055	0.10
2.0	908.7	591	490	5.16×10^{15}	6.08×10^{-5}	0.0736	0.16
3.0	1544.8	346	836	1.92×10^{15}	1.40×10^{-5}	0.0456	0.18
4.0	2082.5	179	1620	1.47×10^{15}	9.76×10^{-6}	0.0415	0.19

The experimental results summarised in Table 5.4 explain the possibility of having both degenerate and non-degenerate p-type ZnTe semiconductors. For a p-type semiconductor to be termed degenerate, one or both of the following conditions must be met; the first condition is that the acceptor density (N_A) must be greater than the effective density of states in the valence band edge (N_V) while the second condition is that (E_F-E_V) is $\ll$ kT [34]. By substituting $m_p^* = 0.20m_o$ which is the effective hole mass of ZnTe into Equation 3.43 of Chapter 3, the effective density of states in the valence band edge of ZnTe thin film was calculated to be 2.24×10^{18} cm^{-3}. As revealed in Table 5.4, the ZnTe layer grown for 30 minutes duration belong to the degenerate p-type semiconductor since (E_F-E_V) is $\ll$ kT while the ZnTe layers deposited within the range

1.00 to 4.00 hours belong to the non- degenerate p-type semiconductor since N_A is $<$ N_V and (E_F-E_V) is $\gg$ kT.

5.4.2 Effect of thickness on morphological properties of ZnTe layers

SEM technique was used to study how variation in growth duration affects the morphology of ED-ZnTe layers. Figures 5.15 (a-g) show the obtained micrographs of ED-ZnTe layers deposited within the explored growth duration. The SEM images revealed that the grain size increases as the deposition time increases. These results agree with the experimental results reported by Shaaban et al. that the crystallites size of ZnTe thin films increase with the thickness of thin film [35].

The summary of range of grain sizes obtained for ED-ZnTe layers deposited between the growth times of 0.25 to 4.00 hours is given in Table 5.5. The value of theoretical thicknesses obtained from Faraday's equation is also shown in Table 5.5 for easy comparison. As seen from Table 5.5, the smallest grain size is denoted as $G.S_{minimum}$ while the largest grain size is depicted as $G.S_{maximum}$. The average grain size ($G.S_{average}$) was obtained by finding the mean of $G.S_{minimum}$ and $G.S_{maximum}$. The smallest range of grain sizes (21.6-101.5) nm occurred at deposition time of 15 minutes while the largest range of grain sizes (725.5-3091.5) nm was obtained at growth time of 4.00 hours. The graphical relationship between the measured average grain sizes ($G.S_{average}$) and growth time is described in Figure 5.15 (h). Figure 5.15 (h) also includes the plot of theoretical thickness obtained from Faraday's equation for easy comparison. A good correlation exists between Figure 5.15 (h) and Figure 5.13.

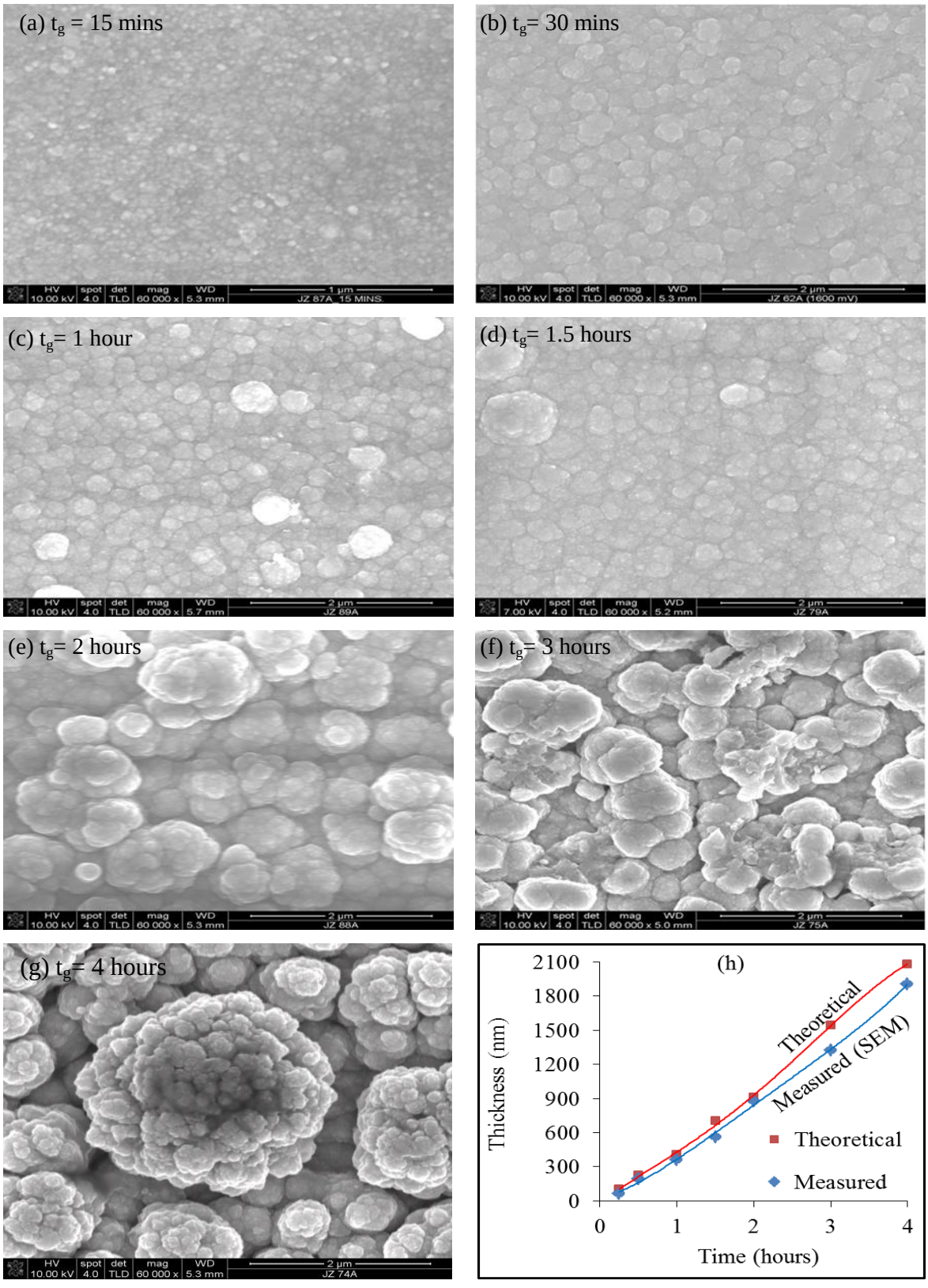


Figure 5.15. (a-g) Typical SEM micrographs of ED-ZnTe layers grown within duration of 0.25 to 4.00 hours and (h) Thickness of ED-ZnTe layers measured from SEM technique and theoretically estimated from Faraday's equation.

Table 5.5. Summary of thickness results obtained from SEM technique and Faraday's law of electroplating.

Time (hours)	$G.S_{minimum}$ (nm)	$G.S_{maximum}$ (nm)	$G.S_{average}$ (nm)	Theoretical thickness (nm)
0.25	21.6	101.5	61.6	100.8
0.50	63.2	326.1	194.7	223.4
1.00	166.4	555.7	361.1	403.2
1.50	226.3	901.8	564.1	701.4
2.00	386.0	1367.7	876.9	908.7
3.00	452.6	2196.3	1324.5	1544.8
4.00	725.5	3091.5	1908.5	2082.5

5.4.3 Effect of thickness on optical absorption

The optical absorption spectra of AD- and HT-ZnTe layers for selected growth duration are illustrated in Figure 5.16. The results of optical absorption measurements carried out at different growth time are presented in Table 5.6. The optical results showed that by increasing the thickness of the ZnTe layers grown in a Te-rich ZnTe electrolyte, the bandgap of the ZnTe layer can be modified. It was observed that the energy bandgaps of the thin films decrease with increase in growth time and film thickness. Researchers working on thin films have also described and explained how variation in thickness of thin films affects the energy bandgap of semiconductor materials [36,37].

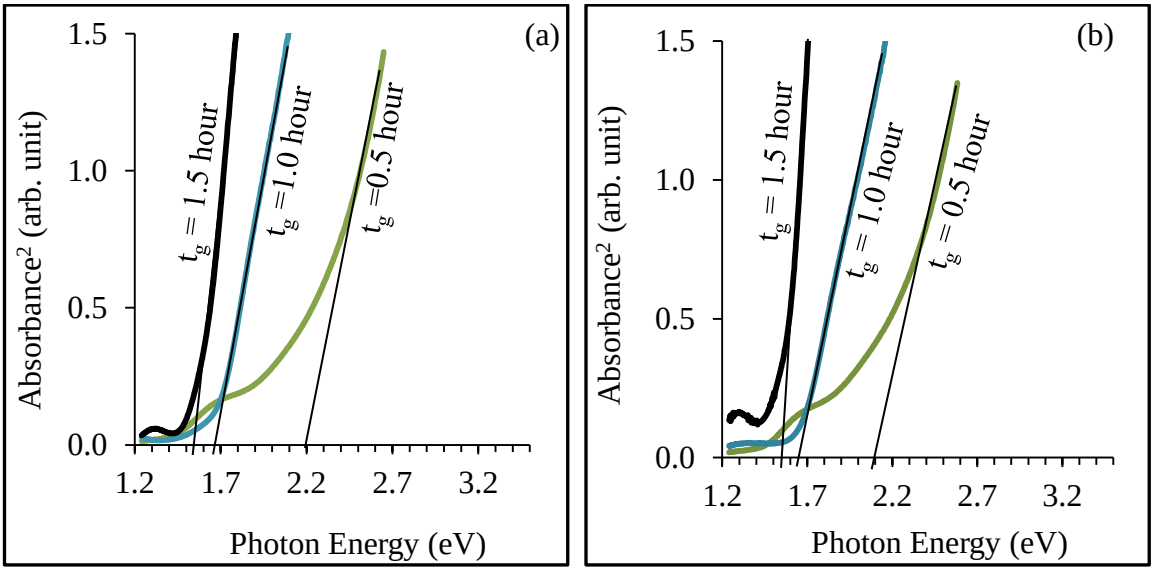


Figure 5.16. Optical absorption spectra showing the effect of thickness variation on energy bandgap of (a) As-deposited ZnTe layers and (b) Heat-treated ZnTe layers.

Table 5.6. Energy bandgaps for AD- and HT-ZnTe layers at different growth duration.

	Growth time (hours)	0.25	0.50	1.00	1.50	2.00	3.00
Bandgap (eV) ± 0.02	AD-ZnTe	2.60	2.20	1.68	1.55	1.30	0.55
	HT-ZnTe	2.35	2.10	1.65	1.55	1.20	0.55

As shown in Figure 5.17, the visual appearance of ZnTe layers differ from each other due to the variation in growth duration. Figure 5.17 (a) and 5.17 (b) show the visual appearance of ZnTe layers grown for 0.50 and 2.00 hours respectively. The energy bandgap of as-deposited Te-rich p-ZnTe (ZnTe:Te) layer grown for 0.50 hours as stated in Table 5.6 falls in the range of bandgap for bulk ZnTe thin films while the energy bandgap of as-deposited Te-rich p-ZnTe (ZnTe:Te) layer grown for 2 hours is ~1.30 eV; this value deviates from the bandgap of stoichiometric ZnTe which is reported to be in the range (2.10–2.26) eV [25]. In Figure 5.17 (b), the Te-rich ZnTe layer appears very dark in appearance thus making it to be highly light absorbing. Te being a semi-metal has a very low bandgap of 0.37 eV [38] and since the ZnTe layers were grown in a Te-rich ZnTe electrolyte for longer duration, more Te easily comes to the surface of the ZnTe layer due to the redox potential of Te atom. This phenomena causes a reduction in the bandgap from ~2.20 to ~1.30 eV providing a suitable method for bandgap grading. The optical absorption curves in Figure 5.16 thus show that the bandgap of ZnTe is tunable by controlling the deposition time, the amount of Te in the ZnTe electrolyte or simply by changing the deposition voltage. It must be noted that the deposition time also determines how much Te and Zn is deposited on the cathode.

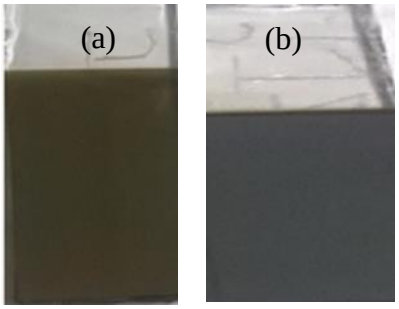


Figure 5.17. Visual appearance of electroplated ZnTe layers grown at same cathodic potential of 1600 mV for different duration of (a) 30 minutes and (b) 2 hours.

5.5 Testing the electronic quality of ZnTe thin films

The I-V and C-V techniques were both used in investigating the electronic qualities of ED-ZnTe layers. The ohmic behaviour of n- and p- ZnTe layers were studied using the device structures glass/FTO/n-ZnTe/Al and glass/FTO/p-ZnTe/Au contacts respectively. Homo-junction diodes were also fabricated from the n- and p-ZnTe layers using glass/FTO/p-ZnTe/n-ZnTe/Al and glass/FTO/n-ZnTe/p-ZnTe/Au device structures. The initial results obtained from glass/FTO/p-ZnTe/n-ZnTe/Al device structures did not yield satisfactory results in terms of rectifying behaviour while homo-junction diodes fabricated from glass/FTO/n-ZnTe/p-ZnTe/Au device structures produced good rectifying property. The electronic properties of glass/FTO/n-ZnTe/p-ZnTe/Au device structures were further assessed using I-V and C-V analytical techniques.

5.5.1 DC conductivity measurements of ED-ZnTe layers

The DC conductivity measurements were carried out on ZnTe layers grown in the p- and n- regions at V_g of ~1600 and 1650 mV respectively. For the purpose of this study, the ohmic contacts to p- and n-ZnTe layers were achieved by using Au and Al metal contacts respectively. Au and Al contact areas of 0.0314 cm^2 and ~100 nm thicknesses were evaporated on electroplated p- and n-ZnTe layers of ~1000 nm in a metal evaporator maintained at a high pressure of 10^{-6} mbar. Using I-V measurement technique, the resistances of p- and n-ZnTe layers were obtained from the device structures glass/FTO/p-ZnTe/Au and glass/FTO/n-ZnTe/Al respectively. The electrical resistivity (ρ) was calculated from the estimated resistances using $\rho = RA/L$ with the known values of contact area (*A*) and the layer thickness of *(L)*.

Table 5.7 shows the summary of electrical properties of p- and n-ZnTe thin films heat-treated at 300^{o}C for 10 minutes in air. As revealed in Table 5.7, the magnitude of the resistivity of p-ZnTe layers is higher than those of n-ZnTe layers. Researchers have shown that for two n- and p-type semiconductors with the same concentration, p-types have a higher resistivity than n-types semiconductor [39]. The majority carriers in n-type semiconductors are the electrons while holes are the majority carriers in p-type semiconductors. Since electrons are known to have higher mobility than holes, it thus shows that electrons must possess lesser resistance to the flow of mobile charge carriers than holes thereby making the n-type ZnTe to have lower resistivity than p-type ZnTe.

Likewise, mobility of charge carriers is a function of the resistivity of semiconductor material; the more resistive a semiconductor material is, the less mobile will be its charge carriers. The measured resistivities in this work fall in the range of values reported by Ishizaki et al. [40], Farooq et al. [41], Ghandhi et al. [42] and John et al. [8]. Rectifying diodes fabricated from high resistive semiconductors such as binary compound semiconductors (for example, CdTe, ZnTe) and Ternary compound semiconductors (for example, CdZnTe, CdMnTe) have found useful applications as X-ray and γ- ray detectors [43–46].

Table 5.7. Summary of electrical properties obtained for p- and n-ZnTe layers electroplated and heat-treated at 300^{o}C for 10 minutes in air (contact area = 0.031 cm^{-2}).

Electrical parameter	p-ZnTe	n-ZnTe
Resistance, R (Ω)	166.7	47.5
Resistivity, ρ (Ω.cm)	5.18×10^{4}	1.48×10^{4}
Conductivity, σ (Ω.cm)$^{-1}$	1.93×10^{-5}	6.77×10^{-5}

5.5.2 Development of p-n homo-junction diodes from electroplated ZnTe thin films

To further test the electronic device quality of electrodeposited n- and p-ZnTe layers, a simple p-n junction diode was fabricated using the device structure glass/FTO/n-ZnTe/p-ZnTe/Au. The fabricated device structure was analysed using I-V technique. An n-ZnTe of ~290 nm was grown at 1650 mV and annealed at 300^{o}C for 10 minutes in air. A p-ZnTe layer of ~1.00 µm was electroplated on annealed n-ZnTe layer at a cathodic potential of 1600 mV. The structure glass/FTO/n-ZnTe/p-ZnTe was then annealed again at 300^{o}C for 10 minutes in air. Gold (Au) metal contacts of ~100 nm thickness and 2 mm diameter (0.031 cm^{-2}) were evaporated on p-ZnTe to form ohmic contacts on p-ZnTe. Figure 5.18 (a) and 5.18 (b) show typical linear-linear and log-linear I-V graphs under dark condition for the fabricated p-n junction diodes. The reverse curve of I-V in Figure 5.18 (a) was used in determining the shunt resistance (R_{sh}) while the series resistance (R_s) was determined using the high forward bias region of the I-V curves. The calculated R_s and R_{sh} from the forward and reverse curves of Figure 5.18 (a) are 13 kΩ and 1.7 MΩ respectively. Other electronic parameters such as rectification factor (*RF*), ideality factor (n), reverse saturation current (I_s) and potential barrier height (ϕ_b) were determined from the log-linear I-V curve shown in Figure 5.18 (b). Under the

deposition parameters used in this initial work, the fabricated homo-junction p-n diodes showed *RF* of ~$10^{2.0}$, *n* value of 2.58, I_s of ~10.0 nA, ϕ_b>0.77 eV and threshold voltage (V_t) of ~0.25 V.

The measured parameters of the p-n homo-junction diodes showed the non-ideal nature of the fabricated diodes, however the result still showed that n- and p- type ZnTe layers have been successfully electroplated due to the rectifying nature exhibited by the diode as shown in Figure 5.18 (a). For a diode which behaves in a nearly ideal way, the current transport takes place via the emission of electrons from one side to the other through the top of the potential barrier at the interface [47]. The high ideality factor obtained in this work showed that there are defects in the material. The value of ideality factor is equal to unity for an ideal diode but deviates from 1.00 due to presence of recombination current [47]. As explained by Sze and Ng [39], the presence of recombination and generation (R&G) centres at the depletion region and interface can also make the ideality factor to increase to 2.00. Presence of high series resistance, tunnelling through the device and presence of R&G centres in the depletion area of the device structures are other possible reasons for ideality factor to exceed 2.00.

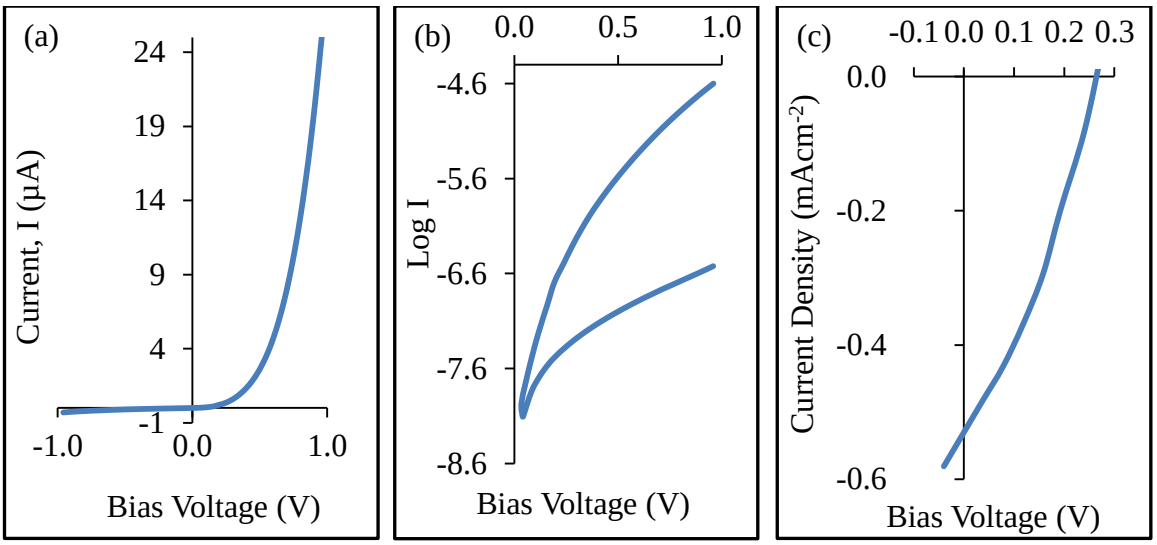


Figure 5.18. I-V characteristics of ZnTe p-n homo-junction diodes under dark condition (a) Linear-linear, (b) Log-linear and (c) I-V characteristics of glass/FTO/n-ZnTe/p-ZnTe/Au under AM1.5 illumination condition at room temperature.

The results of the I-V measurement under AM1.5 illumination showed that the device structure glass/FTO/n-ZnTe/p-ZnTe/Au is photo-voltaic active as described in Figure 5.18 (c). The initial device parameters are V_{oc}=0.260 V, J_{sc}=0.53 mAcm^{-2} and FF=0.34. These measurements were simply carried out to test the electronic properties of the p-n

interface, but not to develop as a solar cell. Both initial I-V measurements under dark and illuminated conditions show that the p-n interfaces have right electronic properties.

5.5.3 Capacitance-voltage measurements of p-n homo-junction diodes

C-V measurements were carried out on glass/FTO/n-ZnTe/p-ZnTe/Au rectifying p-n homo-junction diodes. The C-V and Mott-Schottky plots are illustrated in Figure 5.19 (a) and 5.19 (b) respectively. As illustrated in Figure 5.19 (a), the depletion layer capacitance obtained at zero bias for the p-n homo-junction diodes is 2.43 nF. By inserting the values of the depletion layer capacitance into Equation (3.38) of Chapter 3, the width of the depletion region, *W* was estimated to be ~119 nm. The slope of Mott-Schottky plots in Figure 5.19 (b) was used in finding the doping density of the p-n homo-junction diodes by substituting the obtained slope values (1.60×10^{17} $F^{-2}V^{-1}$) into Equation (3.35) earlier given in Chapter 3. A doping density of 8.58×10^{16} cm^{-3} was obtained; this value signifies that the level of doping in the p-n homo-junction diode device structure is moderate. Using Equation (3.50) presented in Chapter 3, the electric field at the p-n junction of the diode was estimated to be 1.77×10^{5} Vcm^{-1}. The theoretical value of V_{bi} was calculated as 1.06 V by using Equation (3.51). The V_{bi} as indicated in Figure 5.19 (b) is ~1.06 V, this value corresponds with the theoretical value of V_{bi} obtained from Equation (3.51).

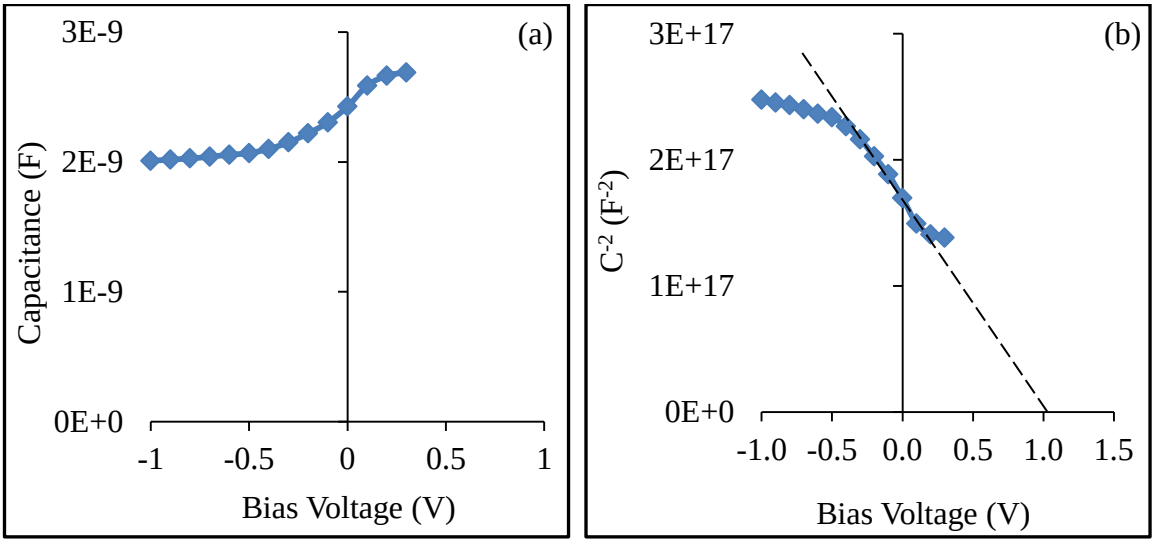


Figure 5.19. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the rectifying p-n homo-junction diodes with device structure, glass/FTO/n-ZnTe/p-ZnTe/Au.

5.6 Summary

The growth of ZnTe thin films was successfully achieved by electrodeposition technique using two-electrode system. The electroplated ZnTe layers are polycrystalline with hexagonal crystal structures and preferred orientation along the (002) plane. The electrical conductivity types show both n- and p-type and electroplating provides a convenient intrinsic doping simply by changing the composition. As seen from the results of EDX analysis, variation in the atomic composition of Zn:Te was observed in the electroplated ZnTe layers as the growth voltage changes. As the cathodic growth voltage increases, the percentage of Zn atoms in the ZnTe layers increase while the percentage of Te atoms in the ZnTe layer decrease as observed in this work. These variations in the atomic composition thus tend to change the material stoichiometry and hence the electrical conductivity type of the layers. The bandgap of ZnTe layers range from (1.90–2.60) eV after annealing in air, but the near stoichiometric material grown at 1600 mV produce 2.20 eV bandgap identical to that of bulk ZnTe. The effect of varying the thickness of deposited p-ZnTe thin films was also investigated on the optoelectronic properties of ZnTe layers. Experimental investigations revealed that ZnTe thin films grown for ~2.00 hours have the largest PEC signals and highest mobility. It was observed that the grain sizes of the thin films increase with thickness, with the largest range of grains obtained at the highest thickness and lowest range of grains obtained at the minimum thickness. Tuneable bandgaps were also obtained for ZnTe layers grown in a Te-rich ZnTe electrolyte by varying the thin film thickness. The electronic qualities of the ED-ZnTe layers were also tested by making ohmic contacts to n- and p-ZnTe thin films of approximately same thickness. The results from DC conductivity measurements showed that p-ZnTe layers have higher resistivity than n-ZnTe layers and both materials show semi-insulating semiconductor properties. The fabrication of p-n homo-junction diodes, the basic building block of electronic devices, was carried out to further investigate the electronic device quality of the electrodeposited ZnTe layers. Initial results obtained from I-V measurements of the device structure glass/FTO/n-ZnTe/p-ZnTe/Au under both dark and illuminated conditions also confirmed the rectifying ability of the n-ZnTe/p-ZnTe interface. The C-V results demonstrate moderate level of doping for the p-n homo-junction diodes.

References

[1] T. Ota, K. Kobayashi, K. Takahashi, J. Appl. Phys., **45** (1974) 1750–1755.

[2] S. M. Patel, N. G. Patel, Thin Solid Films, **113** (1984) 185–188.

[3] F. Pfisterer, H. W. Schock, J. Cryst. Growth, **59** (1982) 432–439.

[4] N. G. Patel, C. J. Panchal, K. K. Makhija, P. G. Patel, S. S. Patel, Cryst. Res. Technol., **29** (1994) 247–252.

[5] R. K. Pandey, S. N. Sahu, S. Chandra, Handbook of Semiconductor Electrodeposition, first ed., Marcel Dekker Inc., New York (1996).

[6] A. Sweyllam, K. Alfaramawi, S. Abboudy, N. G. Imam, H. A. Motaweh, Thin Solid Films, **519** (2010) 681–685.

[7] X. Feng, K. Singh, S. Bhavanam, V. Palekis, D. L. Morel, C. Ferekides, Thin Solid Films, **535** (2013) 202–205.

[8] V. S. John, T. Mahalingam, J. P. Chu, Solid. State. Electron., **49** (2005) 3–7.

[9] G. Mandel, Phys. Rev., **134** (1964) A1073–A1079.

[10] A. G. Fischer, J. N. Carides, J. Dresner, Solid State Commun., **2** (1964) 157–159.

[11] J. H. Chang, T. Takai, B. H. Koo, J. S. Song, T. Handa, T. Yao, Appl. Phys. Lett., **79** (2001) 785–787.

[12] H. Ogawa, G. S. Irfan, H. Nakayama, M. Nishio, A. Yoshida, Jpn. J. Appl. Phys., **33** (1994) 980–982.

[13] M. J. Dinezza, Q. Zhang, D. Ding, J. Fan, X. Liu, J. K. Furdyna, Y. H. Zhang, Phys. Status Solidi C, **9** (2012) 1720–1723.

[14] I. W. Tao, M. Jurkovic, W. I. Wang, Appl. Phys. Lett., **64** (1994) 1848–1849.

[15] V. P. Makhny, V. I. Grivul, Semiconductors, **40** (2006) 774–775.

[16] K. C. Park, E. S. Cha, B. T. Ahn, Curr. Appl. Phys., **11** (2011) S109–S112.

[17] B. B. Wang, M. K. Zhu, H. Wang, G. B. Dong, Opt. Mater. (Amst)., **34** (2011) 42–47.

[18] T. A. Gessert, A. R. Mason, R. C. Reedy, R. Matson, T. J. Coutts, P. Sheldon, J. Electron. Mater., **24** (1995) 1443–1449.

[19] H. Shtrikman, A. Raizman, M. Oron, D. Eger, J. Cryst. Growth, **88** (1988) 522–526.

[20] W. Kuhn, H. P. Wagner, H. Stanzl, K. Wolf, K. Worle, S. Lankes, J. Betz, M. Worz, D. Lichtenberger, H. Leiderer, W. Gebhardt, R. Triboulet, Semicond. Sci. Technol., **6** (1991) A105–A108.

[21] E. Bacaksiz, S. Aksu, N. Ozer, M. Tomakin, A. Özçelik, Appl. Surf. Sci., **256** (2009) 1566–1572.

[22] B. Bozzini, M. A. Baker, P. L. Cavallotti, E. Cerri, C. Lenardi, Thin Solid Films, **361** (2000) 388–395.

[23] M. Bouroushian, T. Kosanovic, D. Karoussos, N. Spyrellis, Electrochim. Acta, **54** (2009) 2522–2528.

[24] T. Mahalingam, V. S. John, S. Rajendran, P. J. Sebastian, Semicond. Sci. Technol., **17** (2002) 465–470.

[25] F. Fauzi, D. G. Diso, O. K. Echendu, V. Patel, Y. Purandare, R. Burton, I. M. Dharmadasa, Semicond. Sci. Technol., **28** (2013) 045005.

[26] O. I. Olusola, O. K. Echendu, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., **26** (2015) 1066–1076.

[27] P. Vanýsek, CRC Handbook of Chemistry and Physics, 91th ed., CRC Press, Boca Raton, Florida (2000).

[28] J. C. Irwin, J. Lacombe, J. Appl. Phys., **41** (1970) 1444–1450.

[29] Q. Zhang, J. Zhang, M. I. B. Utama, B. Peng, M. De La Mata, J. Arbiol, Q. Xiong, Phys. Rev. B, **85** (2012) 085418.

[30] G. Zhang, B. Li, J. Phys. Chem. B, **109** (2005) 23823–23826.

[31] L. Z. Cao, B. L. Cheng, S. Y. Wang, W. Y. Fu, S. Ding, Z. H. Sun, H. T. Yuan, Y. L. Zhou, Z. H. Chen, G. Z. Yang, J. Phys. D. Appl. Phys., **39** (2006) 2819–2823.

[32] P. M. Amirtharaj, F. H. Pollak, Appl. Phys. Lett., **45** (1984) 789–791.

[33] D. N. Bose, M. Holtz, Mater. Lett., **5** (1987) 291–295.

[34] D. A. Neamen, Semiconductor Physics and Devices: Basic Principles, third ed., McGraw-Hill, New York (2003).

[35] E. R. Shaaban, I. Kansal, S. H. Mohamed, J. M. F. Ferreira, Phys. B Condens. Matter, **404** (2009) 3571–3576.

[36] E. S. M. Goh, T. P. Chen, C. Q. Sun, Y. C. Liu, J. Appl. Phys., **107** (2010) 1–5.

[37] V. P. Vani, M. V. Reddy, K. T. Reddy, ISRN Condens. Matter Phys., **2013** (2013) 142029.

[38] M. J. Peterson, F. H. Cocks, Mater. Sci. Eng., **41** (1979) 143–147.

[39] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New Jersey (2007).

[40] T. Ishizaki, T. Ohtomo, A. Fuwa, J. Phys. D. Appl. Phys., **37** (2004) 255–260.

[41] M. U. Farooq, M. Khan, A. Faraz, A. Maqsood, W. Ahmad, L. Li, Mater. Technol. Adv. Perform. Mater., **29** (2014) 29–35.

[42] T. Gandhi, K. S. Raja, M. Misra, Thin Solid Films, **517** (2009) 4527–4533.

[43] L. A. Kosyachenko, R. Yatskiv, N. S. Yurtsenyuk, O. L. Maslyanchuk, J. Grym, Semicond. Sci. Technol., **29** (2014) 015006.

[44] A. E. Bolotnikov, S. E. Boggs, C. M. Hubert Chen, W. R. Cook, F. A. Harrison, S. M. Schindler, Nucl. Instruments Methods Phys. Res. A, **482** (2002) 395–407.

[45] K. Kim, S. Cho, J. Suh, J. Won, J. Hong, S. Kim, Curr. Appl. Phys., **9** (2009) 306–310.

[46] S. del Sordo, L. Abbene, E. Caroli, A. M. Mancini, A. Zappettini, P. Ubertini, Sensors, **9** (2009) 3491–3526.

[47] E. H. Rhoderick, IEE Proc. I Solid State Electron Devices, **129** (1982) 1–14.

Chapter 6 - Growth and characterisation of CdS thin films

6.1 Introduction

Cadmium sulphide (CdS) is a member of group II-VI binary compound semiconductors which has found wide applications in the world of electronic devices. It is a direct bandgap semiconductor having energy of 2.42 eV for single crystalline material at room temperature [1,2]. It is n-type in electrical conduction and is widely used in the fabrication of electronic devices due to its unique optoelectronic features. Some of the applicable areas where CdS semiconductors have found optimum usefulness are: gas sensors [3–5], thin film field effect transistors [6], photoresistors [7], photosensors [8–10], light emitting diodes [11,12], Schottky diodes [13] and solar cells [14–16]. CdS thin films have been found to be a suitable window material to some low-bandgap absorber semiconductor layers. Typical examples of semiconductors using CdS as hetero-junction partner for solar cell applications are CdS/CIS [17], CdS/CIGS [18], CdS/Cu_2S [19] and CdS/CdTe [20–22]. In this work, CdS has been used as an hetero-partner to CdTe thin films to develop glass/FTO/n-CdS/n-CdTe/Au solar cell device structures.

Numerous deposition techniques have been used to-date for the deposition of CdS thin films. Some of these techniques include: chemical bath deposition (CBD) [23], spray pyrolysis [24], vacuum deposition [25], close spaced sublimation (CSS) [26], screen printing [3], sputtering [27], metal-organic chemical vapour deposition (MOCVD) [28] and electrodeposition [29–31]. Polycrystalline CdS thin films with good quality can be obtained using the aforementioned growth techniques. However, the initial cost of setting up instrument for techiques like CSS and MOCVD is very high. In growth technique like CBD, generation of large toxic waste containing Cd is a great disadvantage and disposing these wastes often introduce additional expenses into the overall production cost. In a production line, it is therefore advantageous to use a continuous deposition process like electrodeposition to develop CdS and its other solar cell hetero-partner. This will ensure a reduction in the production cost. In this research, the growth of CdS thin films was achieved using electrodeposition technique with a two-electrode set up. The main aim of this work is to establish the right cathodic

deposition potential for growing CdS thin films for applications in optoelectronic devices most especially solar cells.

6.2 Preparation of CdS electrolytic bath

Two chemicals namely $CdCl_2.xH_2O$ (99.999% purity) and $(NH_4)_2S_2O_3$ (98% purity) were used in preparing the electrolyte for the electrodeposition of CdS thin films. The two chemicals were purchased from Sigma Aldrich, United Kingdom. The precursors $CdCl_2.xH_2O$ serve as the cation source while $(NH_4)_2S_2O_3$ serve as the anion source. The electrolytic bath contains 0.3 M $CdCl_2.xH_2O$ and 0.03 M $(NH_4)_2S_2O_3$ in 400 ml of de-ionised water. After mixing the two chemicals together, the initial pH was measured to be 1.44±0.02. The pH of the bath was adjusted to 2.50±0.02 using diluted NH_4OH and HCl. The solution was allowed to stir continuously for ~6 hours to ensure full dissolution of the chemicals in the de-ionised water. The electroplating of CdS thin films were carried out at ~80^oC using a heater with an embedded magnetic unit which controls the magnetric stirrer during deposition.

6.3 Voltage optimisation and growth of CdS thin films

This section discusses some analytical techniques used for estimating the range of cathodic potentials that would be suitable for the growth of nearly stoichiometric CdS layers and for material characterisation.

6.3.1 Cyclic voltammogram

The suitable voltage range to grow nearly stoichiometric CdS thin films was obtained using a cyclic voltammogram. A range of cathodic potentials from 0 to 1600 mV was applied through the electrodes inside the electrolyte at a sweep rate of 180 $mVmin^{-1}$. The pH of the solution and deposition temperature were maintained at 2.50±0.02 and ~80^oC respectively. The I-V curve of the electrolyte containing aqueous solutions of 0.3 M $CdCl_2$ and 0.03 M $(NH_4)_2S_2O_3$ in both forward and reverse directions is shown in Figure 6.1. The two main atoms making up the CdS thin films are cadmium (Cd) and sulphur (S) from $CdCl_2$ and $(NH_4)_2S_2O_3$ precursors respectively. Out of these two atoms, sulphur has the tendency to deposit first before cadmium because S has a more positive redox potential $\left(E^o\right)$ than Cd. The E^o of sulphur and cadmium with respect to the standard hydrogen electrode (SHE) are +0.449 and -0.403 V respectively [32].

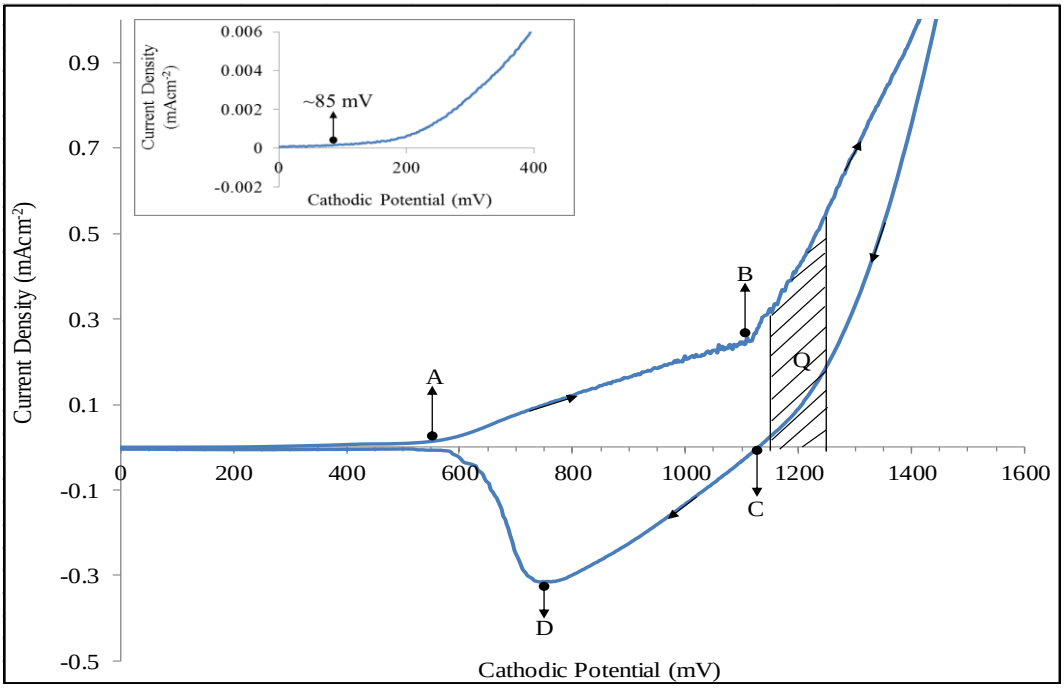


Figure 6.1. Cyclic voltammogram of electrolyte containing 0.30 M $CdCl_2$ and 0.03 M $(NH_4)_2S_2O_3$ in 400 ml of de-ionised water (pH = 2.50±0.02, T = 80^{o}C). Inset shows the transition voltage at which sulphur starts to deposit.

The diagram shown at the inset of Figure 6.1 illustrates the potential at which S begins to deposit while the point labelled A in Figure 6.1 descibes the potential at which Cd deposition starts to take place. The deposition of S starts to take place at ~85 mV while that of Cd begins at ~550 mV. This result further illustrates the initial explanation given about S depositing first before Cd due to its E^o value.

A steady rise was observed in the forward current from point ***A*** to point ***B*** as the cathodic voltage increases from ~550 to 1118 mV. This steady increase shows that more S and Cd are being deposited to form a mixture of sulphur and CdS thin films. The slight reduction observed at point ***B*** before the sudden rise again is due to the deposition of elemental Cd and co-deposition of CdS on the working electrode. The rise in deposition current density after ~1118 mV shows rapid discharge of Cd and reaction between Cd and S to form CdS. The point C indicated on the reverse cycle of the I-V curve shows that the transition point of current flow from the positive to the negative takes place at ~1138 mV. Point ***C*** indicates the dissolution of elemental Cd and removal of Cd from CdS layer deposited on the cathode. At this point, the deposition current density is zero because the dissolution rate of materials is equal to its deposition rate. The dissolution of S from the surface of the working electrode occurs at the broad peak

labelled ***D***. At low cathodic growth potential (≤1118 mV), a S-rich CdS layer is expected to be formed. As the deposition potential increases, the amount of Cd in the CdS layers gradually increases thus allowing near stoichiometric CdS layers to be deposited. Thus, a voltage range (~1150 mV to 1250 mV) labelled ***Q*** in Figure 6.1 has been identified as being suitable to grow near stoichiometric CdS layers according to this experimental result. The overall chemical reaction for the deposition of CdS thin films on the cathode is stated in Equation (6.1) [30].

$$Cd^{2} + S_2O_3^{2-} + 2e^{-} \rightarrow CdS + SO_3^{2-} \qquad (6.1)$$

6.3.2 Visual appearance

The visual appearance of 11 samples of electroplated CdS layers grown between cathodic voltages of 1150 to 1250 mV is shown in Figure 6.2. As earlier discussed, the range of voltages used in this work was determined from the result of the I-V curve of the glass/FTO inside the CdS electrolyte. All the CdS layers shown in Figure 6.2 were deposited at a temperature of ~80^{o}C for 30 minutes duration and the pH of the bath was maintained at 2.50±0.02 at the start of deposition.

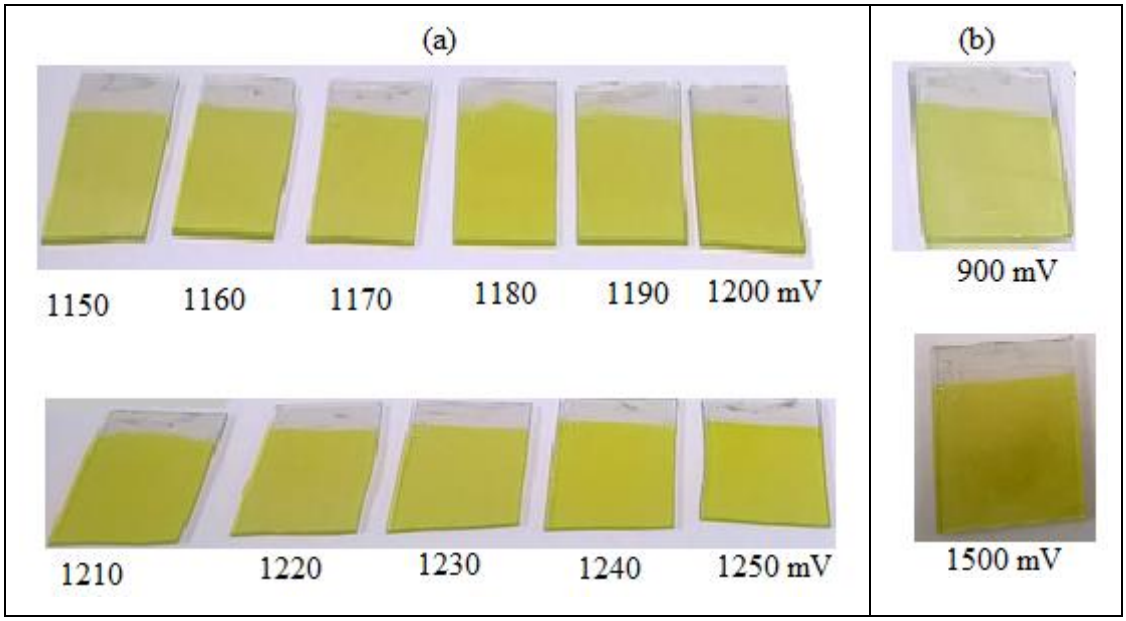


Figure 6.2. Typical images showing the visual appearance of as-deposited CdS thin films grown at different cathodic potentials.

As observed from Figure 6.2, all the ED-CdS layers exhibited uniform yellowish colour in appearance. Visual appearance is one way in which qualitative information can be obtained about electroplated semiconductors as previously explained in Chapter 4 when

the colour of CdSe layers changes with pH. None of the CdS layers appear dark in colour despite the variation in deposition potential. As reported by Diso et al. [33], CdS layers deposited at higher cathodic potential (for example, at 1500 mV) appears dark in colour due to Cd-richness. Attempts made to grow at very high cathodic potential of 1500 mV in this work resulted in formation of Cd dendrytes on the top surface of the CdS thin films as a result of high deposition current density. However, as illustrated in Figure 6.2 (b), the CdS layers grown at this V_g did not become dark as suggested by Diso et al. [33]. This may be due to a lot of factors such as the concentration of Cd salts in the bath and the pH of the electrolyte. The colour of CdS samples grown at low cathodic potential of 900 mV differ from the rest of the samples explored between 1150 to 1250 mV. The colour appears light yellowish; this is due to deposition of more sulphur at this low cathodic potential [34]. As earlier discussed, sulphur has the tendency to deposit easily and faster than Cd because its redox potential is more positive than that of Cd. The energy bandgap obtained for as-deposited CdS layers grown at 900 mV is ~2.28 eV. This value is lower than the E_g of bulk CdS and is closer to the E_g of CdO which has been reported to be in the range 2.20 to 2.30 eV [5,35] . CdO thin films have also been classified as a potential window layer as a result of their E_g value [36].

6.3.3 X-ray diffraction

The XRD spectra of as-deposited CdS layers grown between cathodic potentials of 1170 to 1230 mV is illustrated in Figure 6.3 (a). This voltage range was studied so as to determine the optimum deposition potential to grow nearly stoichiometric CdS layers. The CdS layers used in this investigation were grown for ~30 minutes. As shown in Figure 6.3 (a), two main peaks were observed at the position $2\theta=25.05^{o}$ and 26.66^{o} along the (100) and (002) planes respectively. The presence of these peaks makes the as-deposited (AD) CdS layers to be polycrystalline. The crystal structures of the AD-CdS layers were found to be hexagonal by comparing the observed XRD measured data with the reported data from JCPDS file with reference codes 01-080-0006 and 01-077-2306. Hexagonal crystal phase has been reported to be the stable phase for CdS thin films [37]. Several reports in the literature also show that the cubic phase of CdS thin films convert to hexagonal after annealing [30,38,39].

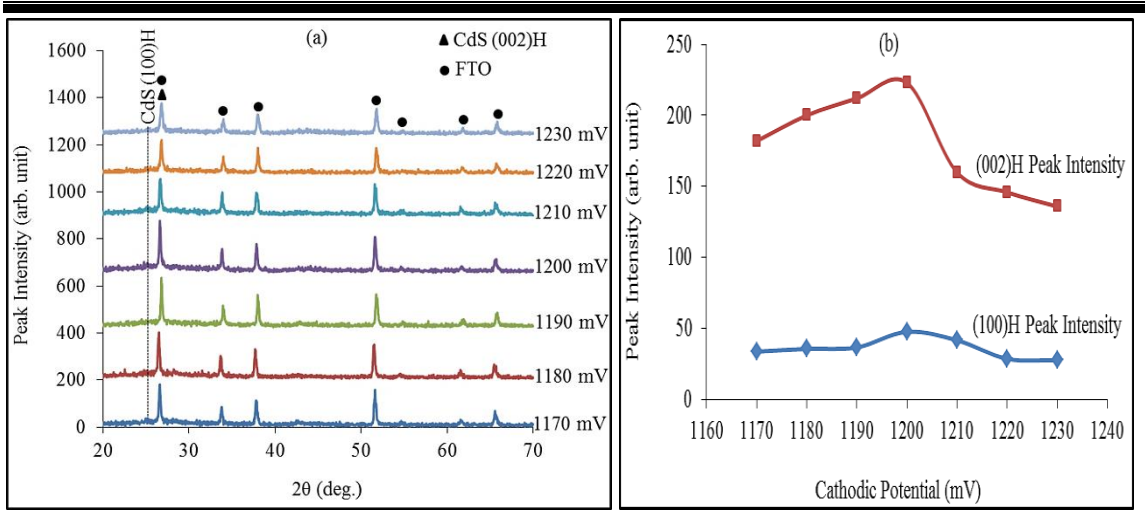


Figure 6.3. (a) XRD spectra of as-deposited CdS layers grown at the cathodic potentials ranging from 1170 mV to 1230 mV, and (b) the (100)H and (002)H peak intensity versus cathodic potentials ranging from 1170 mV to 1230 mV for as-deposited CdS layers.

The peak at 2θ in the range (26.60-26.69)^{o} represents the preferred orientation peak since it has the highest intensity. However, this peak coincides with the underlying FTO peak at 2θ= 26.65^{o}. For this reason, the most intense diffraction peak along (002) plane was not used for the CdS analysis and crystallites size estimation. The second peak observed from the XRD spectra of AD-CdS thin films at 2θ=25.05^{o} along (100) plane was utilised to calculate the crystallite sizes and to determine the optimum potential to electrodeposit nearly stoichiometric CdS thin films. Figure 6.3 (b) shows the plot of peak intensity versus cathodic potentials for diffraction peaks along (002) and (100) plane.

The results presented in Figure 6.3 (b) indicate a similar trend in the peak intensities for both planes as the cathodic potential is increased from 1170 mV to 1230 mV. However, the intensities of peaks along (002) plane are generally higher than those of (100) plane. As observed from Figure 6.3 (b), the peak intensity gradually increases from 1170 mV to 1200 mV along both (002) and (100) planes. As the cathodic deposition potential increases beyond 1200 mV to 1230 mV, a drop was observed in the peak intensity. It is however interesting to see that despite the overlapping which occurs between CdS peak along (002) plane and underlying FTO peak at 2θ= 26.65^{o}, both planes show similar trends at cathodic deposition potentials between 1170 to 1230 mV.

Figure 6.4 (a) shows the XRD spectra obtained for CdS thin films annealed at 400^{o}C for 20 minutes in air. This post deposition heat-treatment is essential to improve the structural and other material properties of CdS thin films so as to make it a suitable semiconductor material for electronic device fabrication [31]. After annealing, another CdS peak with hexagonal crystal structure corresponding to (101) crystal plane was observed at 2θ in the range (28.06-28.33^{o}). The emergence of this peak within the explored deposition potentials after annealing is an indication of improvement in the CdS crystallinity. A reflection of the peak along (101) plane with lower intensity was also observed between 1170 and 1180 mV for AD-CdS layers shown in Figure 6.3 (a).

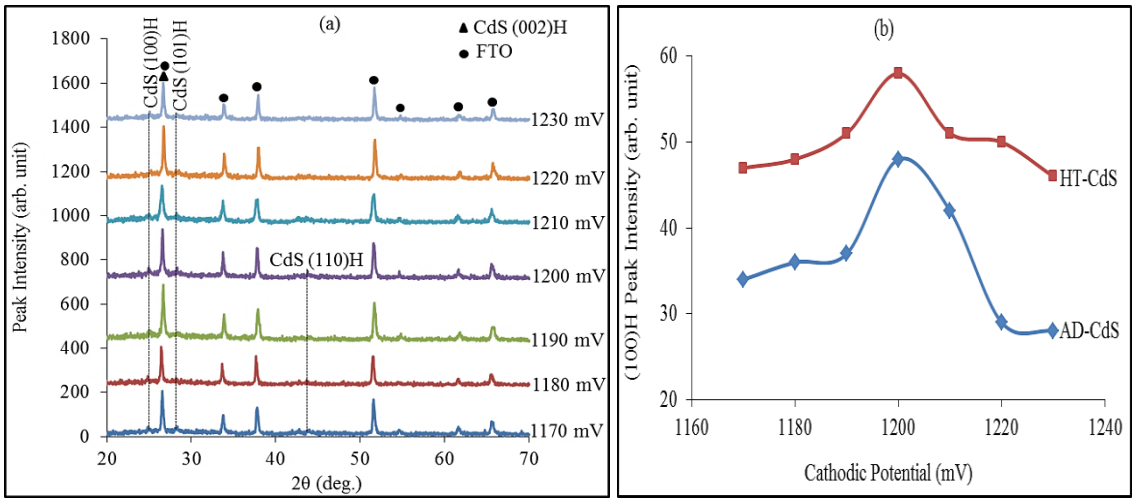


Figure 6.4. (a) XRD spectra of heat-treated CdS layers grown at the cathodic potentials ranging from 1170 mV to 1230 mV and (b) the (100)H peak intensity versus cathodic potentials ranging from 1170 mV to 1230 mV for both as-deposited and heat-treated CdS layers.

Overall, four peaks with hexagonal crystal structures were observed for heat-treated (HT) CdS layers along (100), (002), (101) and (110) planes. The peaks along (100), (002) and (101) planes are common to all HT-CdS layers grown between 1170 and 1230 mV while the peak at (110) plane was only observed for HT-CdS layers grown within the region of 1170-1200 mV. To further show the improvement in crystallinity after heat-treatment in air, the peak intensity along (100) planes of AD- and HT-CdS layers are plotted on the same scale as a function of cathodic potentials for easy comparison; this is illustrated in Figure 6.4 (b). Both AD- and HT-CdS plots follow the same trend with the highest peak intensity observed at 1200 mV in both cases. This investigation therefore shows that cathodic potential of 1200 mV can be used to electroplate near stoichiometric and highest crystalline CdS thin films for further

material characterisation and device fabrication. This growth voltage was used to deposit CdS thin films of ~150 nm as hetero-partner to CdTe layers for solar cells device fabrication as discussed in Chapter 9.

For further analysis of peaks for AD- and HT-CdS layers deposited at 1200 mV, both AD- and HT-CdS spectra with FTO baseline spectrum were drawn on the same scale for straightforward comparison and quick identification of peaks; this is illustrated in Figure 6.5. It could be seen from Figure 6.5 that the CdS peak along (100) plane has increased in intensity after heat-treatment in air. A critical observation shows that the peak along (101) plane was not present in AD-CdS layers grown at V_g=1200 mV; after heat-treatment in air, the (101) peak appeared at $2\theta=28.33^o$ with peak intensity slightly higher than the peak along (100) plane. Despite the slightly higher peak intensity observed at $2\theta=28.33^o$, the peak along (101) plane could not be used as a yardstick for comparing the intensity of peaks observed in AD- and HT-CdS layers due to its absence in most of the as-deposited CdS layers.

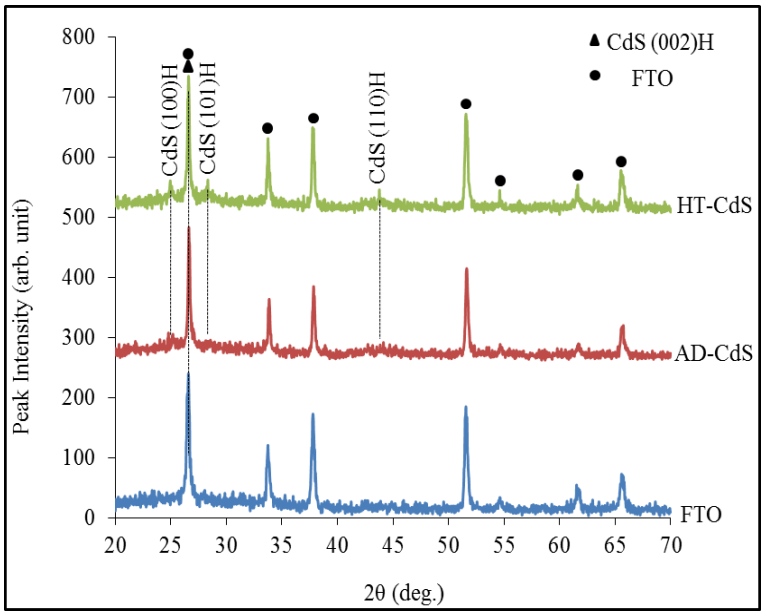


Figure 6.5. Comparative study of XRD peaks of AD- and HT-CdS spectra grown at optimum cathodic potential of 1200 mV.

Another peak along (110) plane absent in AD-CdS layers also emerged in HT-CdS layers after annealing in air. It could therefore be inferred that improvement in peak intensity along (100) plane, emergence of two peaks along (101) and (110) planes all contribute to improvement in the CdS material crystallinity after heat-treatment in air. These results demonstrate the importance of annealing of CdS layers for optoelectronic

device application. Table 6.1 gives the summary of extracted data from XRD measurements and estimated crystallite sizes using Scherrer's equation stated in Equation (3.12) of Chapter 3. The extracted data matches the JCPDS file with reference code 01-080-0006 and 01-077-2306 as stated in Table 6.1.

Table 6.1. Summary of XRD analysis of CdS thin films deposited at cathodic potential of 1200 mV for as-deposited and heat-treated CdS layers at 400^{o}C for 20 minutes in air.

Sample	Angle (2θ) (degrees)	Peak Intensity (arb. unit)	d-spacing (Å)	FWHM (degrees)	Crystallite size, D (nm)	Orientation plane (hkl)	Hex-ref code matching
AD-CdS	25.05	48	3.55	0.422	20.2	(100)	01-080-0006
	26.66	223	3.34	0.195	**43.8**	(002)	01-080-0006
HT-CdS	25.02	58	3.56	0.390	21.8	(100)	01-080-0006
	26.66	231	3.34	0.162	**52.7**	(002)	01-080-0006
	28.33	59	3.15	0.325	26.4	(101)	01-080-0006
	43.77	42	2.07	0.317	28.2	(110)	01-077-2306

The crystallite sizes of CdS layers summarised in Table 6.1 range from 20.2 to 28.2 nm. The crystallite sizes with values 43.8 nm and 52.7 nm are not applicable to the ED-CdS layers due to FTO overlap.

6.3.4 Raman spectroscopy measurements

Typical Raman spectra for AD- and HT-CdS layers are shown in Figure 6.6. In both spectra, the highest Raman intensities were observed at the first longitudinal optical phonons (1LO) vibration mode. In the AD-CdS layers, three Raman peaks corresponding to the transverse optical (TO), 1LO and second longitudinal optical (2LO) phonon modes were observed at 231.7 cm^{-1}, 304.1 cm^{-1} and 606.9 cm^{-1} respectively. The most intense peak was observed at 1LO while the Raman peaks observed at TO and 2LO phonon modes were found to be broad with low intensity. After heat-treatment in air, the peak at TO mode disappears while the intensity of the 1LO peak drastically increases as compared to the 1LO peak of the AD-CdS layers. In a similar manner, an improvement was also seen in the 2LO phonon peak. Litran et al. [40] explained that the increase in peak intensity after annealing can arise as a result of fusing together of the crystallite particles during annealing process.

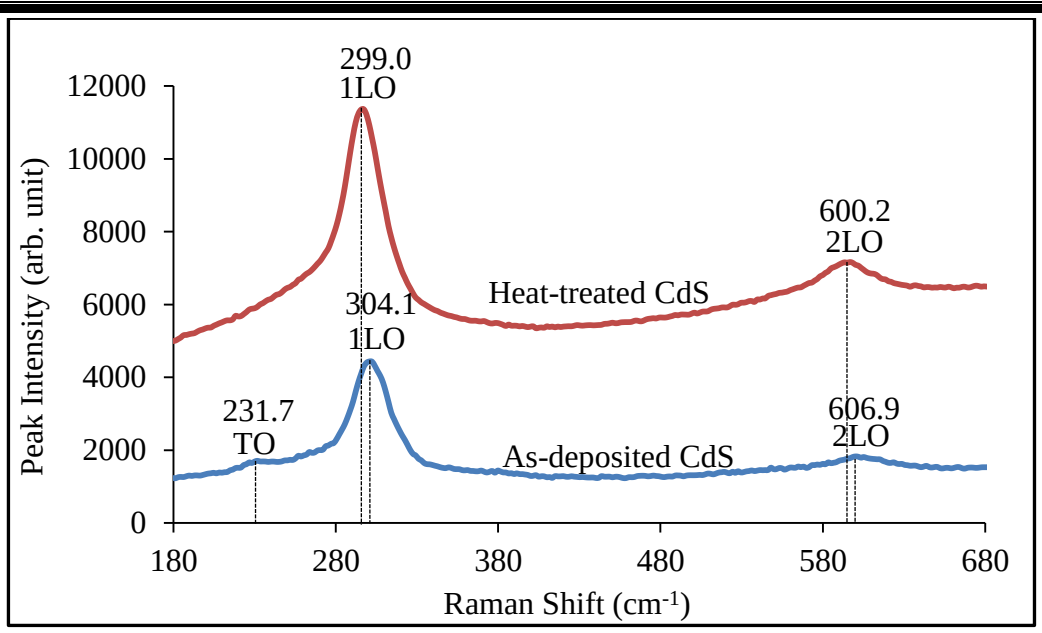


Figure 6.6. Raman spectra of as-deposited and heat-treated CdS thin films at 400^{o}C for 20 minutes in air.

The 1LO and 2LO phonon peaks of the heat-treated CdS layers were seen at 299.0 cm^{-1} and 600.2 cm^{-1} respectively. An increase in the peak intensity of 1LO and 2LO phonon peaks of heat-treated CdS layers is an indication of improvement in the material crystallinity. The Raman shift position of the 1LO and 2LO phonon peaks for bulk CdS material occurred at 305 cm^{-1} and 610 cm^{-1} respectively [40]. As noticed in this work, red shift was observed in the 1LO and 2LO phonon peaks of AD-CdS and HT-CdS when compared with the bulk value of CdS crystal. This red shift change in the phonon peak position can be due to factors such as tensile stress in the CdS semiconductor [31,41], lattice strain which arises as a result of extrinsic defects and internal dislocations in the material [42].

6.3.5 Optical absorption study

Optical absorption measurements were carried out using UV-Vis spectrophotometer so as to determine the energy bandgap of the AD- and HT-CdS semiconductor materials within the explored cathodic deposition potentials. Figures 6.7 (a to d) show the optical absorption spectra for AD- and HT-CdS layers for some selected voltages. The energy bandgaps were determined by extrapolating the line of best tangent of the absorption curve to the photon energy axis at A^2=0.

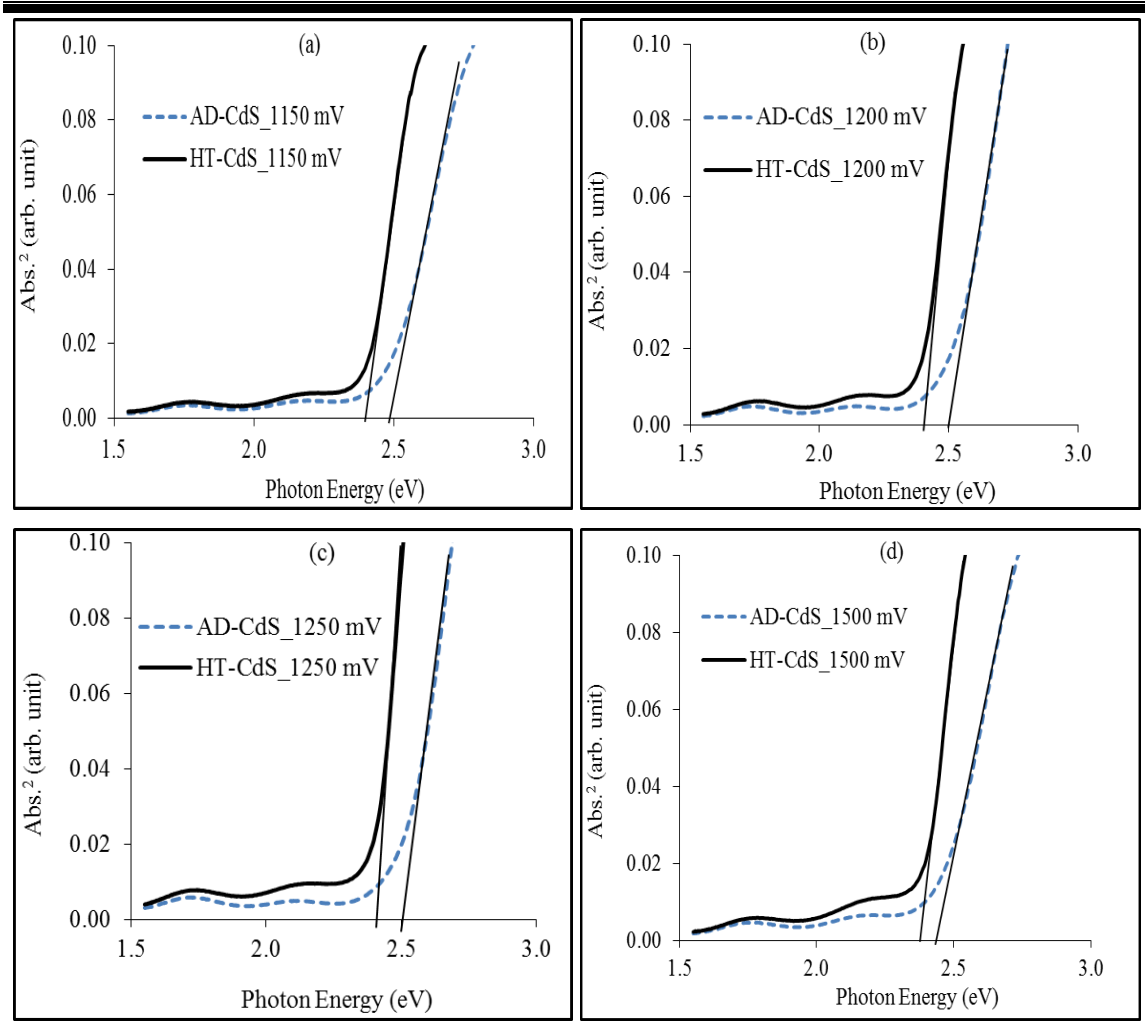


Figure 6.7. Optical absorption spectra for AD- and HT-CdS layers at cathodic potentials of (a) 1150 mV, (b) 1200 mV, (c) 1250 mV and (d) 1500 mV.

In Figure 6.7 (a), the E_g of AD-CdS grown at V_g=1150 mV is ~2.48 eV; after annealing in air, the E_g decreased to 2.40 eV. In Figures 6.7 (b) and 6.7 (c), the energy bandgaps of AD-CdS samples grown at 1200 and 1250 mV decrease from 2.50 to 2.42 eV after annealing in air. For CdS layers grown at 1500 mV (Figure 6.7 (d)), the E_g decreased from 2.44 to 2.38 eV after heat-treatment in air. Overall, the E_g of AD-CdS layers are higher in value than the E_g of HT-CdS layers as observed in Figure 6.7 (a) to 6.7 (d). The larger bandgap of AD-CdS layers can be explained in terms of their smaller or nano particles. One of the properties of semiconductor nanoparticles is that they have quantum confinement effects in their opto-electronic properties and due to their quantum confinement nature, they have a large bandgap [43]. Nanoparticles are therefore known to possess larger bandgaps [43,44] with large surface to volume ratio [45]. Semiconductor materials with large surface to volume ratio have been reported to have reduced crystallite sizes [46]. However, quantum effects are observed only for

crystallites smaller than ~10 nm. Another reason for higher bandgap is that the substrates on which the thin layers are grown may not be 100% covered by the deposited films. The presence of gaps between crystallites allows passage of all wavelengths, producing larger E_g values.

In the 16.5% efficiency reported by Wu in 2004 [44], the author explained that the CdS used as hetero-partner to CdTe thin films have a nanostructure instead of the usual poly-crystalline nature. The nanostructure CdS films reported by Wu have a higher optical bandgap ranging between 2.50 to 3.10 eV. The author explained that as the CdS bandgap increases as a result of incorporation of more oxygen content, the grain size equally decreases. Wu's experimental work thus shows that the higher the energy bandgap of a semiconductor material, the smaller would be its particle size.

Generally, semiconductor materials grown with low temperature technique like electroplating do have smaller crystallites and the tendency for these as-deposited layers to have larger bandgap than heat-treated ones are usually very high. After heat-treatment, the material crystallinity improves with the particle or grain size becoming bigger and obviously, the surface to volume ratio decreases [45]. Chaure et al. [13] also reported a decrease in the bandgap of chemical bath deposited CdS thin films after annealing in air. The authors' reported 2.42 eV for AD-CdS layers and 2.25 eV for annealed CdS layers. Chaure et al. [13] explained the difference in bandgap between AD-CdS and HT-CdS in terms of smaller particles present in as-grown materials coalescing or fusing together into bigger grains after annealing. It should however be noted that due to the flexible nature of semiconductor materials, their optical and electrical behaviour can differ from one another. The detailed energy bandgaps estimated from the absorption spectra of CdS layers grown at cathodic potentials ranging from 1150 to 1250 mV are described in Table 6.2. The energy bandgaps obtained for CdS layers grown at 900 mV and 1500 mV are also included in Table 6.2. As seen in Table 6.2, the bandgaps of HT-CdS layers are generally lower than the AD-CdS layers.

Table 6.2 also shows that as the growth voltage increases from 900 mV to 1250 mV for AD-CdS layers, the energy bandgap increases from 2.28 eV to 2.50 eV. At higher cathodic potential of 1500 mV, the bandgap decreases in both AD- and HT-CdS layers. As explained by researchers in the PV field, this decrease can be caused by incorporation of more elemental Cd at higher deposition potentials [30,31]. Since Cd is

a metallic element, growing at higher cathodic potential of 1500 mV favours the deposition of more Cd and this tends to lower the E_g value of ED-CdS layers. The results in Table 6.2 show that after heat-treatment, the bandgap of CdS layers grown between 1180 and 1250 mV shifted to 2.42 eV which is equal to the energy bandgap of bulk CdS thin films. The optical results further explain that the cathodic potentials ranging between 1180 and 1250 mV are suitable for electroplating near stoichiometric CdS layers. This is a good trend since larger window of cathodic potentials favour the CdS deposition. Energy bandgaps ≤2.40 eV obtained after annealing the CdS samples grown at V_g ≤1170 mV is due to the presence of elemental sulphur and CdS in the material. The presence of elemental sulphur in CdS thin films mostly occurs at lower cathodic potential; this has been reported to increase photo-absorption and reduce optical transmittance thereby leading to a decrease in the energy bandgap [47]. Figure 6.8 shows the diagrammatical representation of energy bandgaps versus cathodic potentials for AD-and HT-CdS layers grown between 1150 and 1250 mV.

Table 6.2. Energy bandgaps of AD- and HT-CdS layers at different cathodic potentials ranging between 1150 and 1250 mV.

Growth potential (mV)	Energy bandgap (E_g) ± 0.01 (eV)	
	AD_CdS	HT_CdS
900	2.28	2.23
1150	2.48	2.40
1160	2.48	2.40
1170	2.48	2.40
1180	2.50	2.42
1190	2.50	2.42
1200	2.50	2.42
1210	2.50	2.42
1220	2.50	2.42
1230	2.50	2.42
1240	2.50	2.42
1250	2.50	2.42
1500	2.44	2.38

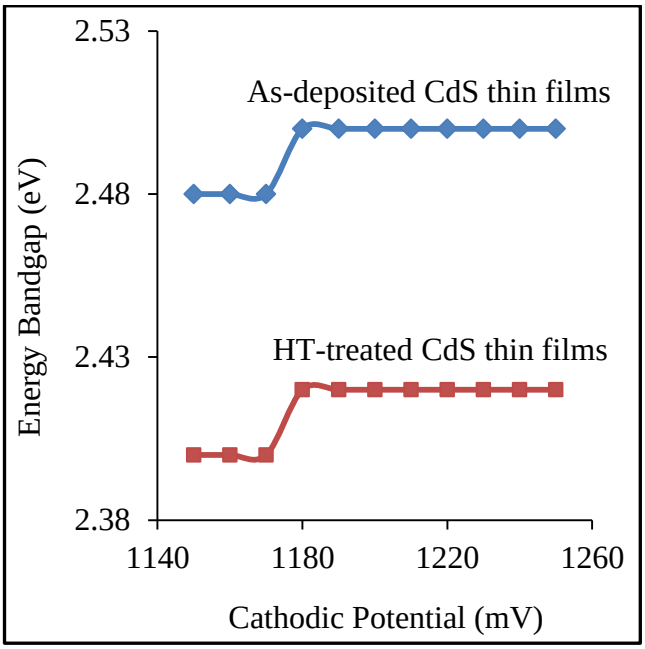


Figure 6.8. Variation of typical energy bandgaps of CdS layers as a function of cathodic deposition potentials for AD- and HT-CdS layers.

The step rise in the energy bandgaps between the cathodic potential of 1170 and 1180 mV is therefore an indication of the reduction of elemental sulphur in the CdS thin

films. The formation of stoichiometric CdS layers with an optimum E_g of 2.42 eV was observed at V_g between 1180 and 1250 mV after heat-treatment in air.

6.3.6 Photo-electrochemical (PEC) cell measurements study

The electrical conductivity type of ED-CdS layers grown within the range 1150-1250 mV were determined using PEC cell measurement technique. The electroplated CdS layers were divided into two; one part was left in the as-deposited state while the other part was annealed ordinarily in air at 400^{o}C for 20 minutes. The PEC signals of AD-CdS and HT-CdS layers as a function of cathodic deposition potentials are plotted on the same graph as shown in Figure 6.9 for easy comparison. Both AD-CdS and HT-CdS layers show n-type in electrical conduction. In terms of magnitude, the highest PEC signal was observed at cathodic potential of 1200 mV for both AD- and HT-CdS layers. CdS is a well-known n-type II-VI binary compound semiconductor and researchers have attributed the n-type electrical conductivity of un-doped CdS layers to the presence of intrinsic defects namely S vacancies and Cd interstitials in the crystal lattice structure of the CdS thin films [2,48].

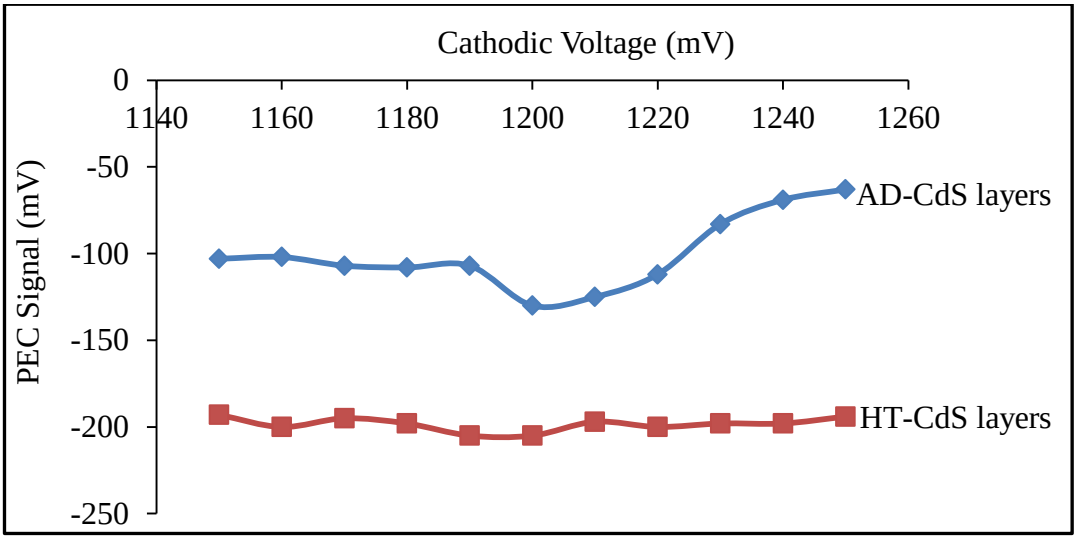


Figure 6.9. Typical PEC signals of as-deposited and heat-treated CdS thin films grown at cathodic potential range of 1150 to 1250 mV. The heat treatment of CdS thin films were carried out at 400^{o}C for 20 minutes duration in atmospheric condition.

6.3.7 Morphological study

The SEM images of as-deposited and heat-treated CdS layers grown for 30 minutes at a cathodic deposition potential of 1200 mV are shown in Figures 6.10 (a) and 6.10 (b) respectively. Both images reveal a fairly uniform coverage of the FTO substrates with

CdS grains. As estimated from the SEM image of AD-CdS layer illustrated in Figure 6.10 (a), the grain size ranges from ~60 to 326 nm. After annealing the CdS layers at 400^{o}C for 20 minutes in air, a slight increase was observed in the grain sizes of the annealed CdS layer shown in Figure 6.10 (b). The grain size of the CdS thin film after annealing ranges from ~68 to 369 nm.

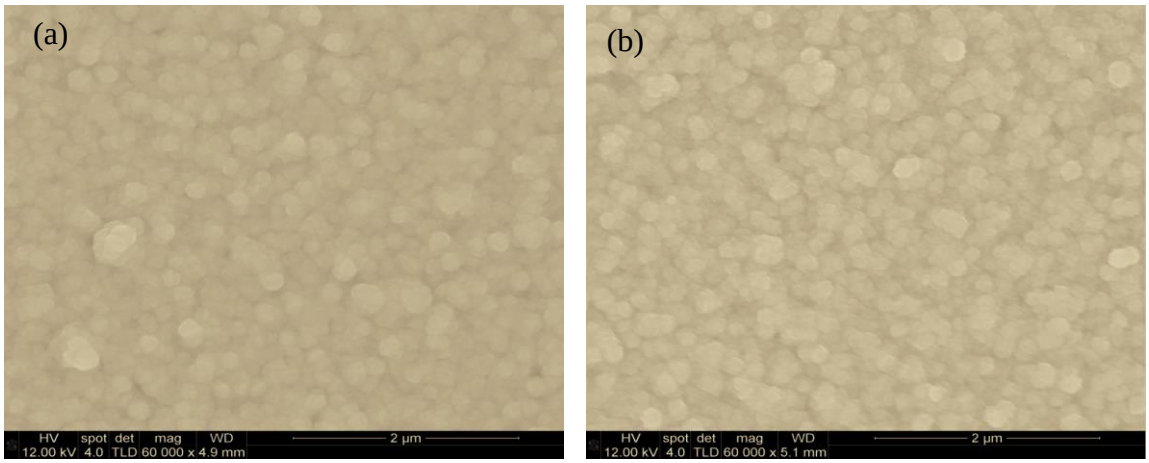


Figure 6.10. SEM images of CdS thin films for (a) as-deposited and (b) heat-treated in air at 400^{o}C, 20 minutes.

6.4 Summary

CdS thin films were successfully electroplated on glass/FTO substrates. The effect of growing CdS thin films at different cathodic potentials ranging from 1150 to 1250 mV was explored and optimum V_g of 1200 mV was obtained from the various analytical techniques carried out on the CdS thin films. The visual appearance of CdS thin films electroplated between 1150 and 1250 mV growth voltage is very similar. The XRD results revealed that the layers are hexagonal and polycrystalline with preferential orientation along the (100) plane. PEC study revealed that the films have n-type electrical conductivity. The magnitude of PEC signals obtained for CdS thin films annealed at 400^{o}C for 20 minutes in air were found to be generally higher than those of the AD-CdS thin films. The results obtained from the optical absorption measurements of annealed CdS thin films showed that a large window of cathodic potentials ranging between 1180 and 1250 mV favours the deposition of nearly stoichiometric CdS layers with an energy bandgap of 2.42 eV. The SEM images of AD- and HT-CdS layers revealed that the FTO substrates are covered with CdS grains of varying sizes.

References

[1] T. L. Chu, J. Electrochem. Soc., **139** (1992) 2443.

[2] C. Wu, J. Jie, L. Wang, Y. Yu, Q. Peng, X. Zhang, J. Cai, H. Guo, D. Wu, Y. Jiang, Nanotechnology, **21** (2010) 505203.

[3] A. Giberti, D. Casotti, G. Cruciani, B. Fabbri, A. Gaiardo, V. Guidi, C. Malagu, G. Zonta, S. Gherardi, Sensors Actuators, B Chem., **207** (2015) 504–510.

[4] X. Jiao, L. Zhang, Y. Lv, Y. Su, Sensors Actuators, B Chem., **186** (2013) 750–754.

[5] W. Kim, M. Baek, K. Yong, Sensors Actuators, B Chem., **223** (2016) 599–605.

[6] B. Mereu, G. Sarau, E. Pentia, V. Draghici, M. Lisca, T. Botila, L. Pintilie, Mater. Sci. Eng. B, **109** (2004) 260–263.

[7] H. Sezen, A. A. Rockett, S. Suzer, Anal. Chem., **84** (2012) 2990–2994.

[8] B. G. An, H. R. Kim, M. J. Kang, J. G. Park, Y. W. Chang, J. C. Pyun, Anal. Chim. Acta, **927** (2016) 99–106.

[9] X. Li, C. Hu, Z. Zhao, K. Zhang, H. Liu, Sensors Actuators, B Chem., **182** (2013) 461–466.

[10] X. Li, Q. Yang, H. Hua, L. Chen, X. He, C. Hu, Y. Xi, J. Alloys Compd., **630** (2015) 94–99.

[11] T. Ota, K. Kobayashi, K. Takahashi, Solid. State. Electron., **15** (1972) 1387–1388.

[12] T. Ota, K. Kobayashi, K. Takahashi, J. Appl. Phys., **45** (1974) 1750–1755.

[13] N. B. Chaure, S. Bordas, A. P. Samantilleke, S. N. Chaure, J. Haigh, I. M. Dharmadasa, Thin Solid Films, **437** (2003) 10–17.

[14] B. M. Basol, J. Appl. Phys., **55** (1984) 601–603.

[15] N. Romeo, A. Bosio, R. Tedeschi, V. Canevari, Mater. Chem. Phys., **66** (2000) 201–206.

[16] S. K. Das, G. C. Morris, Sol. Energy Mater. Sol. Cells, **28** (1993) 305–316.

[17] N. B. Chaure, J. Young, A. P. Samantilleke, I. M. Dharmadasa, Sol. Energy Mater. Sol. Cells, **81** (2004) 125–133.

[18] N. B. Chaure, A. P. Samantilleke, R. P. Burton, J. Young, I. M. Dharmadasa, Thin Solid Films, **472** (2005) 212–216.

[19] V. S. Taur, R. A. Joshi, A. V. Ghule, R. Sharma, Renew. Energy, **38** (2012) 219–223.

[20] I. M. Dharmadasa, A. P. Samantilleke, N. B. Chaure, J. Young, Semicond. Sci. Technol., **17** (2002) 1238–1248. http://iopscience.iop.org/0268-1242/17/12/306.

[21] R. N. Bhattacharya, K. Rajeshwar, J. Appl. Phys., **58** (1985) 3590–3593.

[22] J. Britt, C. Ferekides, Appl. Phys. Lett., **62** (1993) 2851–2852.

[23] S. Prabahar, M. Dhanam, J. Cryst. Growth, **285** (2005) 41–48.

[24] Y. Y. Ma, A. L. Fahrenbruch, R. H. Bube, Appl. Phys. Lett., **30** (1977) 423–424.

[25] F. Pfisterer, H. W. Schock, J. Cryst. Growth, **59** (1982) 432–439.

[26] J. Schaffner, M. Motzko, A. Tueschen, A. Swirschuk, H.-J. Schimper, A. Klein, T. Modes, O. Zywitzki, W. Jaegermann, J. Appl. Phys., **110** (2011) 064508.

[27] A. Rios-Flores, O. Ares, J. M. Camacho, V. Rejon, J. L. Pena, Sol. Energy, **86** (2012) 780–785.

[28] A. Hartley, S. J. C. Irvine, D. P. Halliday, M. D. G. Potter, Thin Solid Films, **387** (2001) 89–91.

[29] B. M. Basol, Sol. Cells, **23** (1988) 69–88.

[30] N. A. Abdul-Manaf, A. R. Weerasinghe, O. K. Echendu, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., **26** (2015) 2418–2429.

[31] H. I. Salim, O. I. Olusola, A. A. Ojo, K. A. Urasov, M. B. Dergacheva, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., (2016).

[32] P. Vanýsek, CRC Handbook of Chemistry and Physics, 91th ed., CRC Press, Boca Raton, Florida (2000).

[33] D. G. Diso, G. E. a. Muftah, V. Patel, I. M. Dharmadasa, J. Electrochem. Soc., **157** (2010) 647–651.

[34] H. I. Salim, PhD Thesis "Multilayer Solar Cells Based on CdTe Grown From Nitrate Precursor," Sheffield Hallam University, Sheffield, 2016.

[35] S. K. Vasheghani Farahani, V. Muñoz-Sanjosé, J. Zúñiga-Pérez, C. F. McConville, T. D. Veal, Appl. Phys. Lett., **102** (2013) 1–5.

[36] T. L. Chu, S. S. Chu, Solid. State. Electron., **38** (1995) 533–549.

[37] R. Lozada-Morales, O. Zelaya-Angel, Thin Solid Films, **281-282** (1996) 386–389.

[38] O. Zelaya-Angel, L. Hernandez, O. Melo, J. Alvarado-Gil, R. Lozada-Morales, C. Falcony, H. Vargas, R. Ramirez-Bon, Vacuum, **46** (1995) 1083–1085.

[39] O. Zelaya-Angel, F. L. Castillo-Alvarado, J. Avendaño-López, A. Escamilla-Esquivel, G. Contreras-Puente, R. Lozada-Morales, G. Torres-Delgado, Solid State Commun., **104** (1997) 161–166.

[40] R. Litran, R. Alcantara, E. Blanco, M. Ramirez-Del-Solar, J. Sol-Gel Sci. Technol., **8** (1997) 275–283.

[41] P. Nandakumar, C. Vijayan, M. Rajalakshmi, A. K. Arora, Y. V. G. S. Murti, Phys. E, **11** (2001) 377–383.

[42] A. Chandran, K. C. George, J. Appl. Phys., **115** (2014).

[43] T. R. Ravindran, A. K. Arora, B. Balamurugan, B. R. Mehta, Nanostructured Mater., **11** (1999) 603–609.

[44] X. Wu, Sol. Energy, **77** (2004) 803–814.

[45] S. J. Fonash, Material Properties and Device Physics Basic to Photovoltaics, in: Sol. Cell Device Phys., second ed., Academic Press, Elsevier Inc., Oxford, UK (2010): pp. 9–65.

[46] K. K. Nanda, S. N. Sarangi, S. N. Sahu, S. K. Deb, S. N. Behera, Phys. B Condens. Matter, **262** (1999) 31–39.

[47] F. Bin Fauzi, PhD Thesis "Research and Development of CdS/CdTe Solar Cells

Incorporating ZnTe Layers," Sheffield Hallam University, Sheffield, 2015.

[48] S. Yılmaz, Y. Atasoy, M. Tomakin, E. Bacaksız, Superlattices Microstruct., **88** (2015) 299–307.

Chapter 7 - Development of n-CdS/p-ZnTe heterostructures

7.1 Introduction

CdS and ZnTe thin films are II-VI binary compound semiconductors with wide bandgap of 2.42 and 2.26 eV respectively. CdS and ZnTe semiconductors are known and widely accepted to be n- and p-type in electrical conduction respectively. Researchers who reported p-type CdS thin films achieved this by extrinsic doping [1,2]. Likewise, the electrical conductivity of ZnTe layers has been generally accepted to be p-type. The problem of obtaining ZnTe layers with n-type electrical conduction without the help of external dopants like Al have been mainly attributed to native defects in the ZnTe materials [3] and self-compensation [4,5]. During this PhD research work at Sheffield Hallam University, the hurdle of achieving n-ZnTe thin films have been successfully overcome via intrinsic doping and this has been reported in the literature [6].

The combination of CdS and ZnTe to form hetero-structures have found useful applications in electroluminescence devices like light emitting diodes [7,8]. Aven and Cook [9] have also been able to obtain diodes of good electronic qualities from the CdS/ZnTe hetero-junction (HJ). The pattern in which CdS thin films grow on ZnTe layers have also been studied [10]. Several works have been done on the CdS/ZnTe HJ but only very few have investigated the CdS/ZnTe HJ for photovoltaic applications. The research work carried out by Pfisterer and Shock was the first work that reported ZnTe/CdS HJ as a viable material for solar cells fabrication [11]. However since then, not much work have been done on the suitability of ZnTe thin films to be used as an absorber material or hetero-junction partner to CdS for solar cells device fabrication. One possible reason could be due to the large bandgap of ZnTe layers which make it un-suitable as an absorber material.

As previously explained in section 5.4.3 of Chapter 5, the bandgap of electrodeposited ZnTe layers can be graded by incorporating excess Te in the layer. Ota et al. [8] observed that diodes (measured under dark condition) fabricated from CdS/Te-rich ZnTe single crystals exhibited good rectifying diode qualities. The observations made by Ota et al. [8] necessitated the reasons why the first set of diodes used for fabrication of one-sided rectifying p-n hetero-junction diodes were grown with a p-type Te-rich ZnTe as hetero-partner to CdS. The ZnTe layers were grown in an acidic bath

containing 0.015 M $ZnSO_4.7H_20$ and 10 ml of dissolved TeO_2 in an aqueous medium. When the Te-rich ZnTe was used as HJ partner to CdS and employed in device fabrication, good diodes were obtained. However, under illumination, the diodes showed very poor PV activity. For this reason, the concentration of Zn in the bath was increased to 0.045 M while still keeping the Te concentration fixed. This is in line with the experimental report given by Major et al. [12] that better solar cell devices are obtained with the Zn-rich buffer layers.

This chapter describes the material properties of n-CdS/p-ZnTe hetero-structure, the effects of usual $CdCl_2$ treatment on ZnTe mono-structure (glass/FTO/ZnTe) and devices fabricated from n-CdS/p-ZnTe hetero-structure (glass/FTO/CdS/ZnTe/Au). The applications of n-CdS/p-ZnTe hetero-structure to electronic devices such as one-sided rectifying n^+p junction diodes and solar cells have also been explored.

7.2 Characterisation of n-CdS/p-ZnTe hetero-structures

The material properties of n-CdS/p-ZnTe device architectures were studied in terms of their structures, morphologies and compositions using XRD, SEM and EDX techniques respectively. Te-rich ZnTe layers and Zn-rich ZnTe layers grown at cathodic potential of 1600 mV were used as hetero-partners to n-CdS to investigate the material properties of the n-CdS/p-ZnTe hetero-structures. In this report, the Te-rich ZnTe refers to ZnTe layers grown from electrolytic bath containing 0.015 M $ZnSO_4.7H_20$ and 10 ml of dissolved TeO_2 in an aqueous medium. The Zn-rich ZnTe refers to ZnTe layers grown from electrolytic bath containing 0.045 M $ZnSO_4.7H_20$ and 10 ml of dissolved TeO_2 in an aqueous medium. The ZnTe layers used in this study are p-type in electrical conduction.

7.2.1 Structural characterisation of n-CdS/p-ZnTe hetero-structure

Figure 7.1 shows the XRD patterns of heat-treated glass/FTO/n-CdS/p-ZnTe hetero-structures in both Te-rich and Zn-rich ZnTe electrolytic bath. The annealing was carried out in air at a temperature of 400^oC for 10 minutes. The diffraction patterns reveal polycrystalline thin films with both CdS and ZnTe peaks. Both CdS and ZnTe films have hexagonal crystal structures. The preferred orientation of CdS thin films was found to be along (101) plane for both spectra illustrated in Figure 7.1. The preferred orientation of ZnTe thin films in Te-rich and Zn-rich electrolytes were found to be along

(002) and (100) planes respectively. Other ZnTe peaks can be identified as (110), (103) and (200) planes with hexagonal crystal structures for both Te-rich and Zn-rich ZnTe layers. For the Te-rich ZnTe thin films, several Te peaks arise as a result of low concentration of Zn ions or excess Te in the ZnTe bath. These Te peaks are hexagonal in structure and correspond to (100), (101), (102) and (110) planes. In the Zn-rich ZnTe diffractogram, a peak appeared at $2\theta = 39.43^{o}$ with a d-spacing of 2.28 Å. This experimentally observed d-spacing value nearly corresponds to the reported d-spacing value of elemental Zn which is 2.29 Å. The reported value was confirmed by JCPDS reference code 00-001-1244 for elemental Zn. By critically comparing the Te-rich and Zn-rich X-ray spectra together, it was observed that the elemental Zn also tends to emerge in the Te-rich ZnTe but the effect was not as obvious as seen in Zn-rich ZnTe bath.

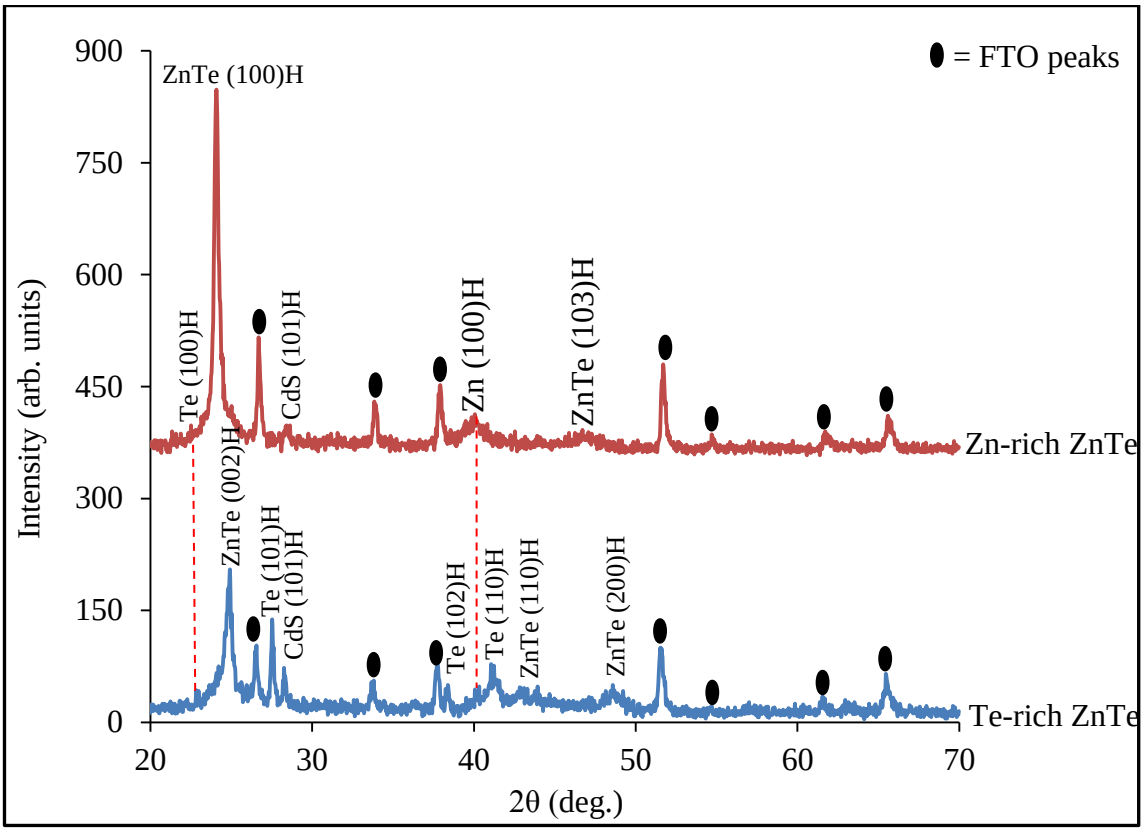


Figure 7.1. XRD patterns for glass/FTO/n-CdS/p-ZnTe structures with emphasis on ZnTe layers grown in Te-rich and Zn-rich ZnTe electrolytic bath.

The presence of a single peak corresponding to elemental Zn does not necessarily mean that the deposited layer is an n-type material. This peak can emerge when ZnTe layers are grown inside a Zn-rich ZnTe electrolytic bath at the p-region side close to inversion

point for longer duration. It may also arise when grown in the n-region for longer duration. As illustrated in Figure 7.1, the XRD spectra showed that the Zn-rich ZnTe diffractogram is a nearly stoichiometric spectrum with minimal number of Te peak. The only Te peak occurred along (100) plane with very low intensity. Figure 7.1 also shows that the XRD peak intensity of Zn-rich ZnTe spectrum is higher than the Te-rich ZnTe spectrum along the preferred plane of orientation; this shows that the Zn-rich ZnTe thin film has a higher crystallinity than the Te-rich ZnTe spectrum.

7.2.2 Morphological characterisation of n-CdS/p-ZnTe hetero-structure

Figure 7.2 shows the surface morphology of annealed glass/FTO/n-CdS/p-ZnTe layers. The heat-treatment was done at 400^{o}C for 10 minutes in air. Figure 7.2 (a) and 7.2 (b) represent the micrographs obtained for ZnTe layers grown from Te-rich and Zn-rich ZnTe electrolytes. It was observed that the grains of the CdS/ZnTe hetero-structure obtained from Zn-rich ZnTe electrolyte are larger and more compact than grains from Te-rich ZnTe electrolyte.

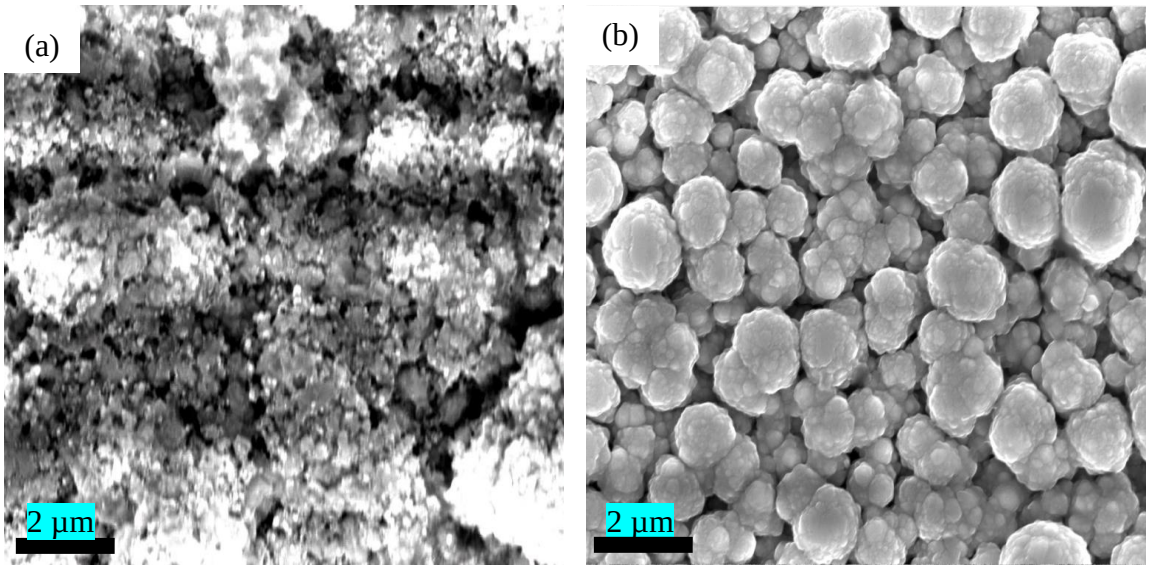


Figure 7.2. SEM micrographs of glass/FTO/n-CdS/p-ZnTe hetero-structures for (a) ZnTe layers grown in Te-rich ZnTe electrolyte and (b) ZnTe layers grown in Zn-rich ZnTe electrolyte.

7.2.3 Compositional characterisation of n-CdS/p-ZnTe hetero-structure

The atomic composition of annealed glass/FTO/n-CdS/p-ZnTe layers is depicted in Figure 7.3. Figure 7.3 (a) and 7.3 (b) represent the EDX spectra obtained for ZnTe layers grown from Te-rich and Zn-rich ZnTe electrolyte respectively. It was noticed that

the percentage atomic composition of Te (45.8%) is higher than Zn (27.5%) as illustrated in Figure 7.3 (a). From Figure 7.3 (b), it was seen that the percentage atomic composition of Zn (45.3%) is higher than Te (27.4%). A summary of the % atomic composition of Zn and Te from Te-rich and Zn-rich electrolyte is presented in Table 7.1. This result shows that the concentration of precursors containing the cations and anions is one of the factors which determine how much Zn and Te is deposited. The ratio of % composition of Cd to S in Te-rich and Zn-rich electrolyte is 26.4:0.3 and 26.3:1.0 respectively.

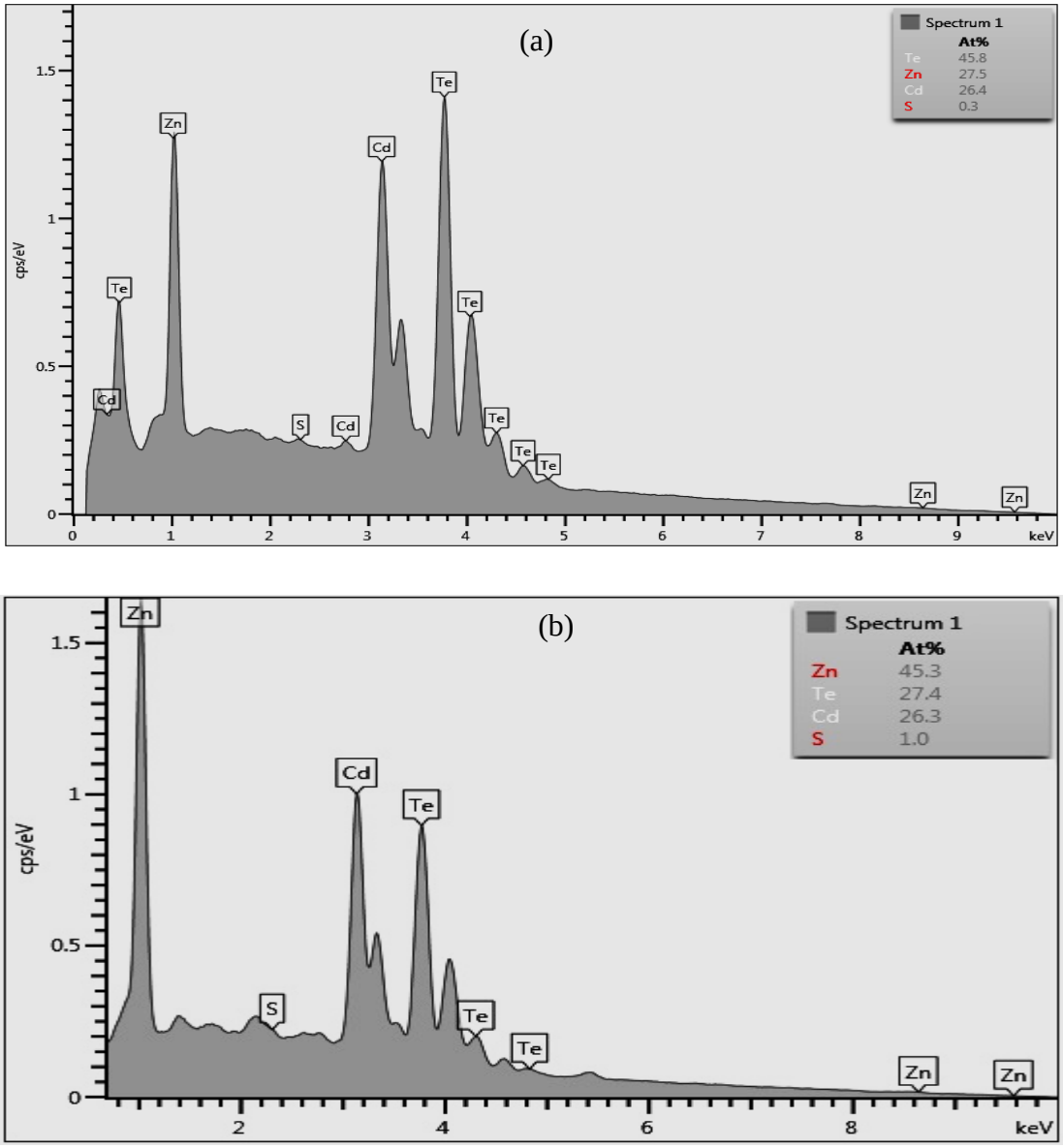


Figure 7.3. EDX spectra showing the percentage of atoms present in the glass/FTO/n-CdS/p-ZnTe hetero-structures for (a) ZnTe layers grown in Te-rich ZnTe electrolyte and (b) ZnTe layers grown in Zn-rich ZnTe electrolyte.

Table 7.1. Comparison of the % atomic composition of Zn and Te from Te-rich and Zn-rich electrolyte.

ZnTe layer	Zn%	Te%
(a) From Te-rich electrolyte	27.5	45.8
(b) From Zn-rich electrolyte	45.3	27.4

This experimental investigation clearly shows that the percentage composition of atoms present in a given semiconductor material is not only influenced by growth voltage as discussed in section 5.3.6, Chapter 5, but can also vary based on the concentration of ions in the electrolytic bath as seen in Figure 7.3 (a) and 7.3 (b). By varying the precursor molarity; the structural, morphological and compositional properties of the material likewise changes. This work agrees with the experimental investigations carried out by Ishizaki et al. [13] and Gromboni et al. [14]. Ishizaki et al. [13] performed an experiment by varying the Zn concentration from 5 mM to 50 mM while keeping the molarity of Te constant at 0.16 mM. The authors observed that a change in the concentration of Zn in the ZnTe electrolytic solution affects the electrical and optical properties of the ZnTe thin films [13]. As explained by the same authors in another communication, there is a likelihood for the amount of Zn in the deposited ZnTe thin films to increase as the Zn concentration in the ZnTe electrolyte increases [15]. The experimental work reported by Gromboni et al. [14] further demonstrated how photo-current increases with the Zn contents in ZnTe thin films. From the investigation reported by Gromboni et al. [14], it is therefore possible for ZnTe thin films produced from Zn-rich ZnTe electrolyte to possess better photo-activity than the ones produced from Te-rich ZnTe electrolyte. The structural properties of CdS/ZnTe hetero-structures discussed in section 7.2.1 of this chapter further attests to this since better crystallinity was obtained in ZnTe thin films (prepared from Zn-rich ZnTe electrolyte) grown on CdS substrate.

7.3 Effects of $CdCl_2$ surface treatment on ZnTe mono-layers

One of the major objectives of growing ZnTe semiconductor materials is to investigate its suitability as a window and absorber material. Various researches have been conducted on the usage of ZnTe as a p-type window layer to other binary and ternary compound semiconductors [16,17]. However, not much work has been done on its

suitability as an absorber material say to CdS [11]. This is because its bulk bandgap enables it to be more useful as window layers rather than as absorber layers [18]. However, the energy bandgap of ZnTe layers can be engineered to make it suitable as an absorber layer. The electroplating technique used in this work is one of the available techniques which allow the bandgap of a semiconductor material to be easily tuned. The bandgap tuning can be achieved by controlling parameters such as the time of growth, the pH of the electrolyte [19], temperature of the electrolytic bath, stirring rate, the concentration of salts used in the electrolytes and growth voltage. In this work, the energy bandgap of ZnTe layers have been successfully tuned as explained in section 5.4.3 of Chapter 5. There are several reports in the literature which support the growth of ZnTe layers in a Te-rich medium [7,8,13].

Due to the proposed usage of ZnTe as an absorber layer to CdS window material, it is therefore essential just like in CdTe to study the effect of surface treatment using chemicals containing Cl [20,21] on the structural and electrical properties of glass/FTO/p-ZnTe before applying the chemical treatments in the hetero-structure. For this reason, ZnTe layer of ~1200 nm was electroplated and used in this experiment. This section discusses XRD and PEC cell measurement techniques to examine what happens to the structural and electrical properties of ZnTe thin films when the top surface of the layer is treated with chemicals containing Cl before annealing in air.

7.3.1 Effect of $CdCl_2$ treatment on structural properties of p-ZnTe as hetero-partner to n-CdS

The first set of Cl treatments used for the ZnTe absorber layers was done using $ZnCl_2$ aqueous solution. Unfortunately, this treatment did not work out well because of the in-ability of the $ZnCl_2$ solution on the ZnTe surface to dry up with time. Instead of the $ZnCl_2$ solution on top of the ZnTe layer to dry up, it was producing more of oily substance on the surface of the ZnTe thin films; the cause of this reaction is however not known as at the time this research was carried out. For this reason, the experiment was discontinued and another Cl source which is $CdCl_2$ was made use of. The application of $CdCl_2$ treatment on top of the ZnTe absorber layers proved successful as the solution dries up quickly without forming oily substance on top of the material. Also, the ZnTe absorber layer survived heat-treatment after annealing with $CdCl_2$ treatment in air.

Figure 7.4 (a) shows the XRD spectra of as-deposited (AD), heat-treated (HT) and cadmium chloride (CC) treated ZnTe layers. The heat-treatment was carried out at 400^{o}C for 10 minutes in air. The result shows that the preferred orientation occurs along the (100) plane for the ZnTe layers; other ZnTe peaks observed are summarised in Table 7.2. The XRD spectra shows that by applying $CdCl_2$ treatment to the ZnTe layer, no additional phase was introduced into the ZnTe thin films as a result of this treatment. All the peaks observed in the AD-ZnTe layers were equally observed in the HT- and CC-treated layers. This shows the possibility of applying the usual $CdCl_2$ treatment to ZnTe layer without changing the material structure or introducing additional/ unwanted/detrimental phase to the semiconductor material. This result contradicts the reports given by Mohanty et al. [22] that ZnTe converts to CdTe and ZnO after treating the top surface of ZnTe thin film of ~140 nm with $CdCl_2$ treatment. The results and explanations given by Mohanty et al. cannot therefore be generalised. The reason for ZnTe reducing to CdTe and ZnO after $CdCl_2$ treatment may be due to several factors such as concentration of $CdCl_2$ solution used for surface treatment, growth conditions, heat-treatment temperature with duration and thickness of the ZnTe layers being used for their experimental investigations [22]. Even though the XRD peaks described in Figure 7.4 show that the ZnTe phase still remains after $CdCl_2$ treatment, there is the possibility of having elemental Cd which was not detected by the XRD probably due to the presence of elemental Cd in minute form. The effect of using $CdCl_2$ treatment on solar cell structures with ZnTe as an absorber layer to CdS is discussed in section 7.4.2.

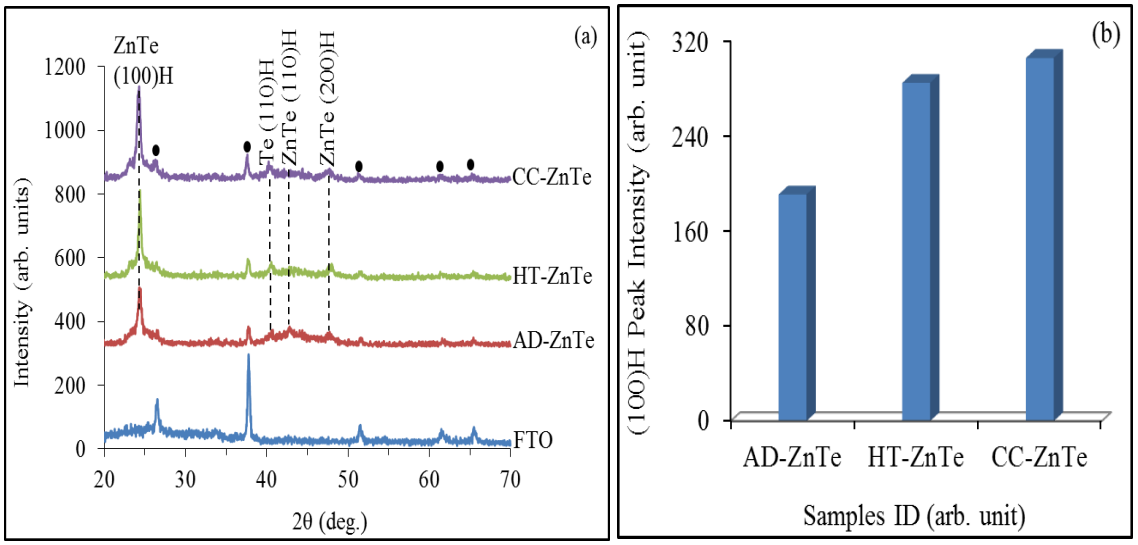


Figure 7.4. (a) XRD spectra of as-deposited ZnTe layer, heat-treated and $CdCl_2$ treated ZnTe layers at 400^{o}C, 10 minutes in air. (b) (100) peak intensity of AD, HT and CC-ZnTe layers.

Table 7.2. Summary of XRD data for as-deposited ZnTe layer, heat-treated and $CdCl_2$ heat-treated ZnTe layers at 400^{o}C, 10 minutes in air.

Sample ID	Angle (2θ)^o	d-Spacing (Å)	Crystal Structure	Chemical Formular	Plane of orientation (h k l)	Reference Code Matching
JZ 88A	24.45	3.64	Hexagonal	ZnTe	(100)	01-080-0009
	40.35	2.24	Hexagonal	Te	(110)	00-001-0727
	42.83	2.11	Hexagonal	ZnTe	(110)	01-080-0009
	47.78	1.90	Hexagonal	ZnTe	(200)	01-080-0009
JZ 88B	24.39	3.65	Hexagonal	ZnTe	(100)	01-080-0009
	40.53	2.22	Hexagonal	Te	(110)	00-001-0727
	47.98	1.89	Hexagonal	ZnTe	(200)	01-080-0009
JZ 88C	24.14	3.69	Hexagonal	ZnTe	(100)	01-080-0009
	40.32	2.23	Hexagonal	Te	(110)	00-001-0727
	47.57	1.91	Hexagonal	ZnTe	(200)	01-080-0009

As shown in Figure 7.4 (b), there was a further improvement in the crystallinity of CC-ZnTe layers after annealing as a result of increase in the peak intensity. For the p-type ZnTe layers of ~1.2 μm, a peak was also observed whose d-spacing value matches that of elemental Te. This peak occurred at 40.35^o, 40.53^o and 40.32^o for AD-, HT-, and CC-ZnTe layers respectively. As shown in Table 7.2, this peak has hexagonal crystal structure and occurred along (110) plane. The d-spacing values range from 2.22-2.24 for AD-, HT-, and CC-ZnTe layers and it closely matches with that of elemental Te with reference code 00-001-0727. The XRD results elucidate the possibility of having p-ZnTe thin films due to the presence of elemental Te. It is worthwhile to know that the inclusion of extra 0.030 M to the initial 0.015 M concentration of Zn precursor did not eliminate the presence of elemental Te peak when the ZnTe layer is grown in the p-region.

7.3.2 Effect of $CdCl_2$ treatment on PEC cell measurements of p-ZnTe as hetero-partner to CdS

PEC cell measurements were equally done for p-type ZnTe layers of ~1200 nm. The result shows that the material remains p-type after $CdCl_2$ treatment. As illustrated in Figure 7.5, an increase was observed in the PEC signal of as-deposited p-ZnTe layers after heating without and with $CdCl_2$ treatment in air. This experimental results show that there is no type conversion after treating p-ZnTe layers with $CdCl_2$; hence the material tends to be more stable even after $CdCl_2$ treatment.

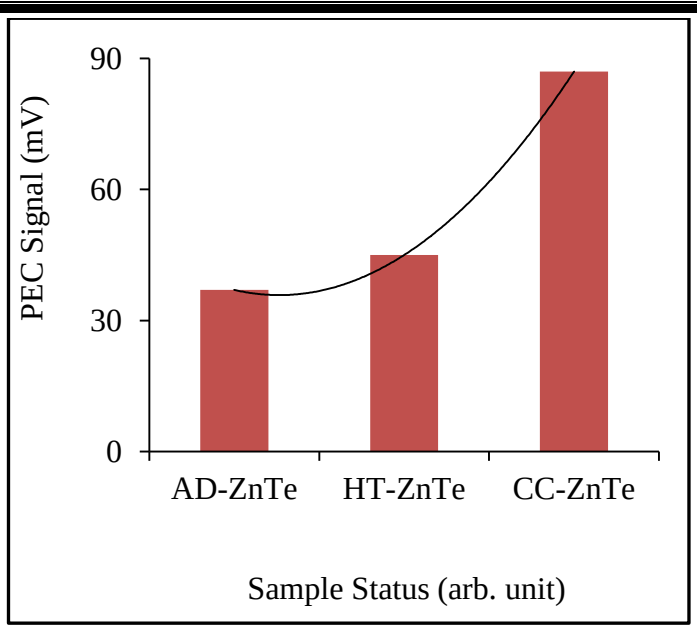


Figure 7.5. Effect of $CdCl_2$ treatment on the electrical conductivity type of p-ZnTe layers.

7.4 Application of n-CdS/p-ZnTe heterostructures

This section is focused on the application of ZnTe thin films as absorber materials to CdS. The two main application areas explored are: (i) fabrication of one-sided rectifying n^+p junction diodes from n-CdS and p-ZnTe thin films all from II-VI binary compound semiconductors and (ii) solar cells fabrication.

7.4.1 One-sided p-n junction diodes fabricated from n-CdS/p-ZnTe

The p-ZnTe used in the fabrication of the initial one-sided n-p junction (n-CdS/p-ZnTe) device structure was grown from 0.015 M of Zn precursor and 10 ml of TeO_2. As previously discussed, the ZnTe electroplated from this electrolyte is referred to as Te-rich ZnTe.

7.4.1.1 I-V characteristics of n-CdS/p-ZnTe hetero-junction diodes under dark condition.

I-V measurements provide a valuable way to test the electronic quality of a semiconductor material. These measurements were carried out using the device structure glass/FTO/n-CdS/p-ZnTe/Au. Since the device structure under consideration has a junction between the n- and p- region, it is therefore of utmost necessity to form ohmic contacts to the window layer which is n-CdS and p-ZnTe which is the absorber

layer. The electron affinity of n-CdS layer has been reported to be 4.80 eV [23] while the work function of FTO is 4.40 eV [24]. The underlying FTO subtrate to n-CdS already creates an ohmic contact to n-CdS since the work function of FTO metal contact is lower than the electron affinity of n-CdS. With regards to the p-ZnTe, its electron affinity has been reported to be 3.53 eV [25] while the work function of Au metal contact is 5.25 eV [23]. Therefore, to create an ohmic contact to p-ZnTe, a metal such as Au with higher workfunction is needed. Figure 7.6 (a) shows the log-linear I-V characteristics of glass/FTO/n-CdS/p-ZnTe/Au device structure. From Figure 7.6 (a), the *RF*, I_s, ϕ_{bo} and *n* values were determined. The *RF* obtained at a bias voltage of ~1.0 V is $10^{2.7}$. I_s of 2.82 µA was obtained from the intercept of the Log I axis. By inserting the value of I_s into Equation 3.19, Chapter 3, ϕ_{bo}>0.64 eV was estimated. *n* value of 2.89 was obtained by substituting the slope of Log-linear I-V in Figure 7.6 (a) into Equation 3.25, Chapter 3. A series resistance (R_s) of ~35.0 Ω and shunt resistance (R_{sh}) of ~30.0 kΩ were obtained from the linear-linear I-V characteristics shown in Figure 7.6 (b). When the Te-rich ZnTe was used as hetero-partner to n-CdS thin films and employed in device fabrication, good rectifying diodes with low R_s values were obtained under dark condition. However, under illumination (Figure 7.6 (c)), the diodes showed very poor PV activity with parameters V_{oc} = 0.058 mV, J_{sc} = 0.56 mAcm^{-2} and *FF*=0.31.

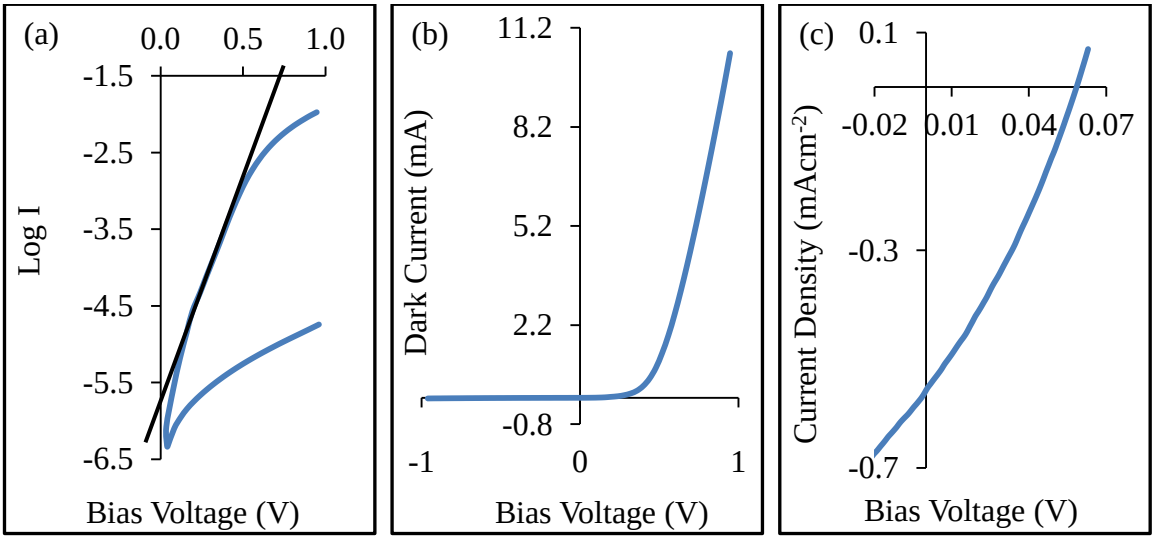


Figure 7.6. I-V characteristics of glass/FTO/n-CdS/p-ZnTe/Au diode under dark condition (a) Log-linear, (b) Linear-linear and (c) I-V characteristics of glass/FTO/n-ZnTe/p-ZnTe/Au under AM 1.5 illumination condition at room temperature.

The I-V results show that the fabricated diodes possess good *RF* of ~$10^{2.7}$ to make them suitable for application as electronic devices. I_s is an important diode electronic parameter which distinguish one diode from the other and it is a small current which flows as a result of the minority carriers in the reverse direction when bias voltage is zero. The magnitude of the reverse saturation current varies from one semiconductor diode to the other and it is a determinant of the quality of a rectifying diode [26]. For instance, I_s for a Si diode varies between ~10^{-10} and ~10^{-12} A and ~10^{-4} A for Ge diode. For the p-n homo-junction diodes fabricated from glass/FTO/n-ZnTe/p-ZnTe/Au device structure by Olusola et al.[6], the I_s value was given to be in the order of 10^{-9}A. For the p-n hetero-junction diodes fabricated in this work from n-CdS/p-ZnTe, I_s is of the order of 10^{-6} A. For a diode to possess good electronic quality, the level of recombination of holes and electrons at the interface and within the bulk of the device (material) must be reduced. To achieve this, I_s which is a measure of the recombination in a device must be kept to a minimum value.

As explained by Rao et al. [27], the increase in I_s may arise as a result of defects in the crystal lattice which act as recombination centres that reduce the lifetime of charge carriers. The high I_s obtained in this work may therefore arise as a result of these defects which act as trapping centres. The large *n* value of 2.89 shows the presence of interfacial impurities and high concentration of recombination and generation (R&G) centres in the depletion region [28,29]. Since the obtained *n* value is >2.00, it thus shows that tunnelling is an important current transport mechanism in the device structure [30].

7.4.1.2 Discussion of results from C-V measurements for CdS thin films

In order to carry out C-V measurements, rectifying contacts were made by evaporating 2 mm diameter Au contacts on n-CdS layers. The C-V and Mott-Schottky plots of glass/FTO/n-CdS/Au device structure are shown in Figure 7.7 (a) and 7.7 (b) respectively. As shown in Figure 7.7 (a), the depletion layer capacitance obtained at zero bias for the glass/FTO/n-CdS/Au device structure is 5.583 nF. By incorporating the values of the depletion layer capacitance into Equation 3.38 of Chapter 3, the width of the depletion region, *W* was estimated to be ~44.3 nm.

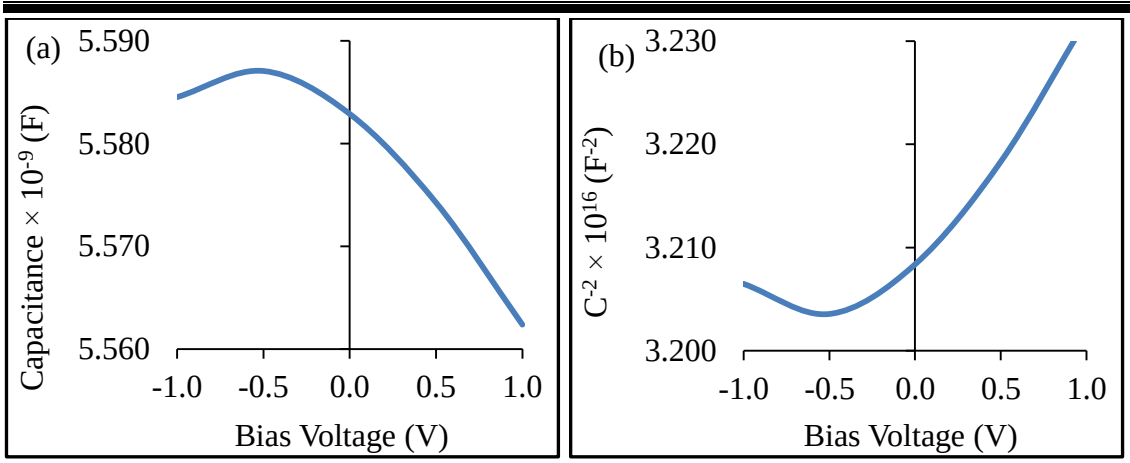


Figure 7.7. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/n-CdS/Au.

Using the slope (1.79×10^{14} $F^{-2}V^{-1}$) obtained from Mott-Schottky plots in Figure 7.7 (b), the donor density of the CdS thin film was estimated to be 9.00×10^{19} cm^{-3}. By taking the effective electron mass of CdS to be $m_e^* = 0.21m_o$ and substituting into Equation 3.42 of Chapter 3, the value of effective density of states in the conduction band minimum (N_C) was calculated to be 2.41×10^{18} cm^{-3}. The experimental results obtained in this work show that the doping density of the CdS semiconductor is greater than the effective density of states in the conduction band of the CdS thin films. This property makes the Fermi energy level to lie within the conduction band thus making the CdS thin films used in this work to become degenerate n-type semiconductor. The details of the C-V measurement results for Au/n-CdS Schottky diodes are shown in Table 7.3.

Table 7.3. The summary of electronic parameters obtained from n-CdS and p-ZnTe layers using C-V technique.

Electronic parameters from CV	CdS thin films	ZnTe thin films
Measured C at zero bias (F)	5.583×10^{-9}	2.620×10^{-10}
W (nm)	44.3	1100.0
E (Vcm^{-1})	8.10×10^{7}	6.81×10^{4}
N_A (cm^{-3})	------	3.55×10^{15}
N_D (cm^{-3})	9.00×10^{19}	------
N_V (cm^{-3})	------	2.24×10^{18}
N_C (cm^{-3})	2.41×10^{18}	------
$E_F - E_V$ (eV)	------	0.17
$E_C - E_F$ (eV)	-0.07	------

As explained by Neamen [31], for a semiconductor to be degenerate, the concentration of electrons (for n-type materials) or hole density (for p-type materials) should be higher than the effective density of states in the conduction band (for n-type materials) and valence band (for p-type materials). This unique property thus makes the Fermi level to be above the conduction band minimum (for n-type) or below the valence band maximum (for p-type). Also in a degenerate semiconductor, $E_C - E_F$ is $\ll kT$; that is, the Fermi level is less than kT below E_C.

To determine the Fermi level position in a degenerate semiconductor, it is important to put into consideration the degeneracy or spin factor of the degenerate semiconductor. The electron spin rotation in CdS quantum dots (QDs) was studied by Masumoto et al. and the spin factor of the electrons was found to be ~1.965±0.006 [32]. The spin factor also called degeneracy factor has been generally reported as 2.00 for donor atoms [31]. Approximating the g-factor obtained for CdS QDs by Masumoto et al. [32] to the nearest one decimal place, the value also tends to be equal to 2.0. Therefore in this work, g-factor of ~2.0 was used to determine the Fermi level position in the CdS degenerate semiconductor.

As seen in Table 7.3, the Fermi level position ($E_C - E_F$) shows a negative value for the CdS thin films. This negative value indicates that the Fermi level position lies within the conduction band thus making E_F to be above the conduction band minimum. Equation (3.45) of Chapter 3 was used to determine the position of the Fermi level for the degenerate n-type CdS layers. The graphical representation of the Fermi level position of CdS shown in Figure 7.8 further illustrates that $E_C - E_F$ lies within the conduction band.

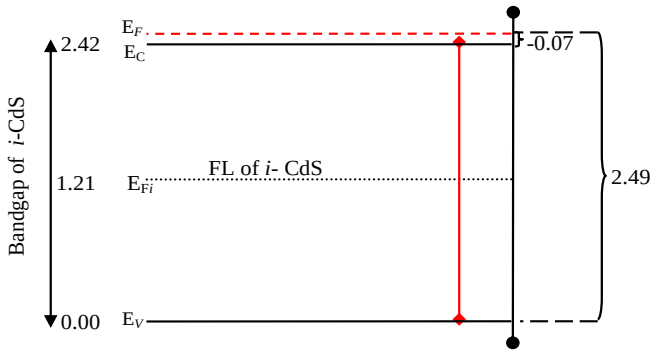


Figure 7.8. Graphical representation of the Fermi level positioning for glass/FTO/CdS/Au device structure.

Thus, the fabricated CdS thin films used in this current investigation fall in the family of the degenerate semiconductors and this explains the possible reason for heavy doping of CdS thin films as given in Table 7.3. The high doping of the CdS thin films was caused by the large concentration of donor atoms in the material. This large electron concentration arises from the fact that below E_F, the energy states are always occupied with electrons while above E_F, the energy states are mostly vacant. Therefore, since E_F is above the E_C minimum (E_{Cmin}) in the n-CdS semiconductor, the energy states below E_F are mainly occupied with donor electrons; this property makes it to behave in a similar manner to metals. Thus, it is expected that in degenerate semiconductors, the electric field at the metal/semiconductor (*M/S*) interface should be higher. As stated in Table 7.3, the electric field in the CdS at the *M/S* junction is higher than that of ZnTe; this is because of the huge concentration of mobile electrons in the CdS conduction band. Using Equations (3.49) and (3.50) of Chapter 3, the electric field for CdS and ZnTe semiconductor materials were calculated to be 8.10×10^{7} and 6.81×10^{4} Vcm^{-1} respectively.

The width of the depletion region is equally a function of the depletion capacitance and doping concentration in the semiconductor. The higher the depletion capacitance, the greater will be the doping density in a semiconductor and the smaller will be the depletion width [31]. Table 7.3 shows that the CdS thin films have a large depletion capacitance of 5.583 nF at zero bias, higher N_D of 9.00×10^{19} cm^{-3} and a small depletion width of 44.3 nm. This is unlike ZnTe semiconductor with moderate doping (3.55×10^{15} cm^{-3}), lesser C_o of 262 pF and higher *W* (1100 nm).

Since the CdS layers grown in this work have a smaller *W,* there is a very high tendency for electron tunnelling through the barrier to increase in the glass/FTO/n-CdS/Au *M/S* structure. Figure 7.9 (a) and 7.9 (b) show the interface where the Au metal is in direct contact with the heavily doped n-CdS layers. In this situation, tunnelling may likely become the prevailing means for current transportation. Figure 7.9 (a) illustrates the degenerate situation where $E_C - E_F$ is $\ll kT$ while Figure 7.9 (b) illustrates the degenerate situation where $E_C - E_F$ is $\ll 0$ (that is negative). Figure 7.9 (b) is the most applicable band diagram for the degenerate n-CdS semiconductor fabricated in this work.

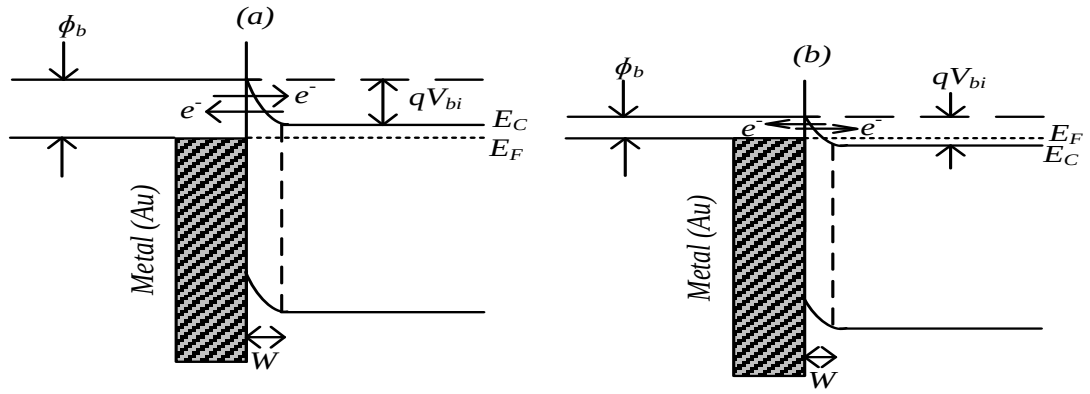


Figure 7.9. Band diagram for metal/semiconductor interface with a degenerate semiconductor (a) E_C-E_F is $\ll kT$, (b) E_C-E_F is $\ll 0$.

7.4.1.3 Discussion of results from C-V Measurements for ZnTe thin films

In order to perform C-V measurements, rectifying contacts were made by evaporating 2 mm diameter Al contacts on p-ZnTe layers. Figure 7.10 (a) and 7.10 (b) show the capacitance-voltage and Mott-Schottky plots of glass/FTO/p-ZnTe/Al device structure respectively. For the glass/FTO/p-ZnTe/Al device structure, the depletion capacitance (C_o) as measured from the C-V plot in Figure 7.10 (a) is 262 pF. By inserting the values of the depletion layer capacitance into Equation 3.38 of Chapter 3, the width of the depletion region, W was calculated to be ~1.10 μm.

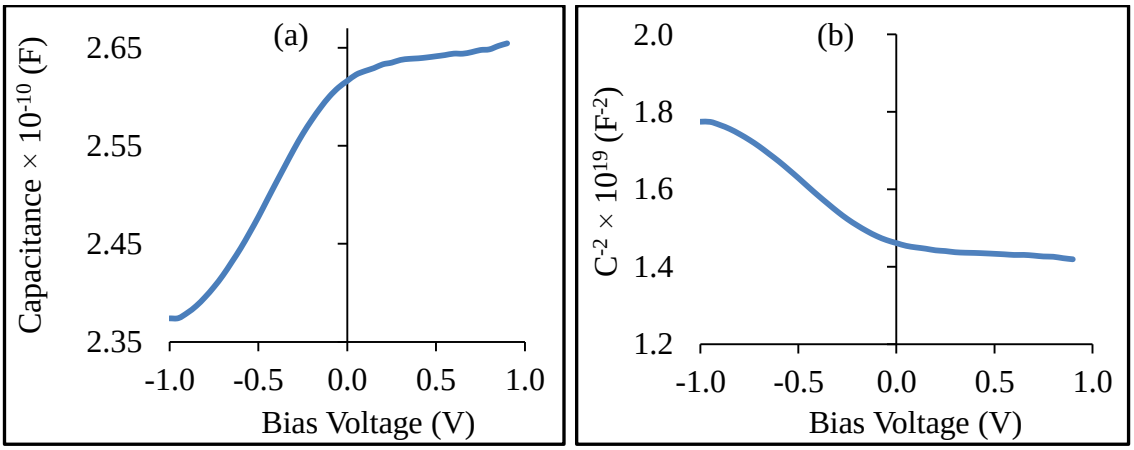


Figure 7.10. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/p-ZnTe/Al.

A slope of 3.88×10^{18} $F^{-2}V^{-1}$ was obtained from the Mott-Schottky plots shown in Figure 7.10 (b) and with this value, the acceptor density of ZnTe layer was calculated to be

3.55×10^{15} cm^{-3}. Using $m_p^* = 0.20m_o$ as the effective hole mass of ZnTe and substituting it into Equation 3.43 of Chapter 3, the effective density of states in the valence band edge of ZnTe thin films was calculated to be 2.24×10^{18} cm^{-3}. The results obtained from this work signify that the concentration of holes in the ZnTe semiconductor is less than the effective density of states in the valence band edge of the ZnTe thin films. Thus the fabricated ZnTe layers used in these experiments belong to the non-degenerate p-type semiconductor with moderate doping and the position of the Fermi level lies above the valence band maximum. As also shown in Table 7.3, E_F - E_V for the ZnTe thin film shows a positive value which is an indication that the Fermi level position lies above the valence band maximum. Equation 3.47 presented in Chapter 3 was applied to determine the position of the Fermi level for the p-type ZnTe layers.

Since the ZnTe semiconductors used in this work have a moderately doped density of 3.55×10^{15} cm^{-3}, low C_o of 262 pF and large depletion width of 1100 nm, the possibility of hole tunnelling from the semiconductor into the metal will decrease in the glass/FTO/p-ZnTe/Al *M/S* structure. Other current transportation mechanisms such as emission of holes from the ZnTe semiconductor into the metal or recombination in the space-charge region may likely dominate. Figure 7.11 shows the energy band diagram of the Schottky barrier formed on moderately doped ZnTe layers.

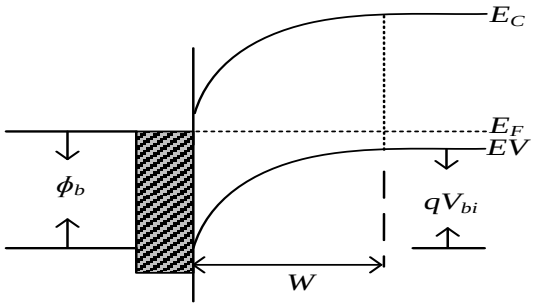


Figure 7.11. Band diagram for Al/p-ZnTe Schottky diodes formed in glass/FTO/p-ZnTe/Al. Note that E_F - $E_V \gg$ kT.

Comparing Figure 7.9 (b) and Figure 7.11 with each other, it is clear that the doping density affects the depletion width of the junction. Heavily doped material like n-CdS illustrated in Figure 7.9 (b) has a narrow depletion width compared to that of moderately doped p-ZnTe layers shown in Figure 7.11. This in turn also affects the effective built-in potential barrier height as illustrated in both figures.

7.4.1.4 Discussion of results from C-V measurements for CdS/ZnTe hetero-junction

The C-V and Mott-Schottky plots of glass/FTO/n-CdS/p-ZnTe/Au HJ device structure with 3 mm diameter active areas are shown in Figure 7.12 (a) and 7.12 (b) respectively. The depletion capacitance obtained at zero bias for the glass/FTO/n-CdS/p-ZnTe/Au device structure is 1.26 nF as illustrated in Figure 7.12 (a).

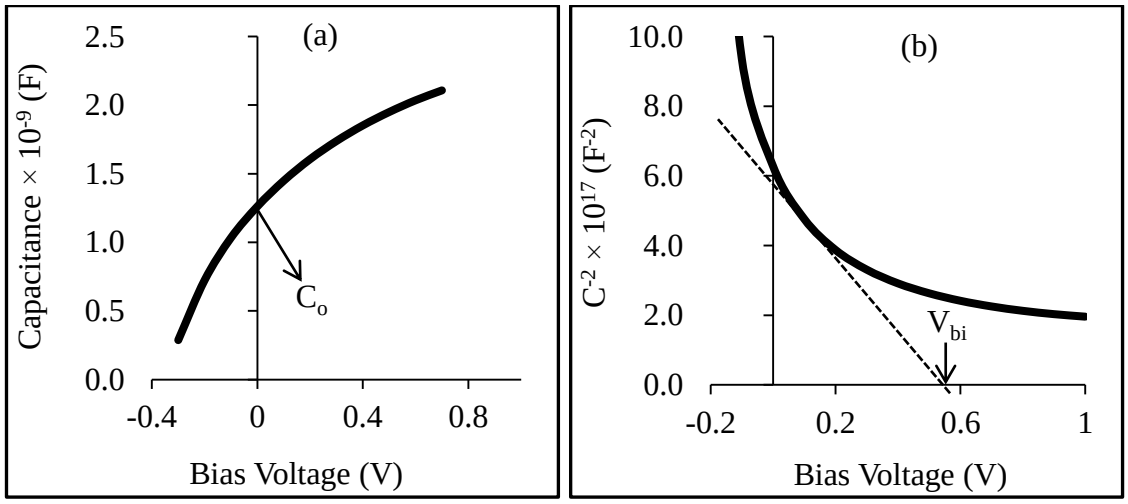


Figure 7.12. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/n-CdS/p-ZnTe/Au.

By substituting the value of the depletion layer capacitance into Equation (3.38) given in Chapter 3, the width of the depletion region, *W* was calculated to be 519 nm. As earlier discussed in section 3.6.2 of Chapter 3, the total depletion width for the one-sided p-n junction diodes can likewise be determined using Equation (3.39) presented in Chapter 3 if the right V_{bi} value is used. The V_{bi} obtained from the Mott-Schottky plot in Figure 7.12 (b) is ~0.55 V; this value nearly corresponds with the theoretical value of ~0.58 V estimated from Equation (3.51) of Chapter 3. Also, Equation (3.40) given in Chapter 3 was used to find the distance by which the depletion region extends into the p-type semiconductor (that is X_p), while X_n was determined by substituting the known value of X_p into Equation (3.39) (that is, X_n=W-X_p).

The acceptor density of the glass/FTO/n-CdS/p-ZnTe/Au HJ device structure was estimated to be 2.47×10^{15} cm^{-3} by using the slope (1.09×10^{18} $F^{-2}V^{-1}$) obtained from Mott-Schottky plot in Figure 7.12 (b). The donor density was estimated to be 3.75×10^{18} cm^{-3} by substituting known values of V_{bi} and X_n into Equation (3.41) of Chapter 3. The experimental results observed in this work show that the p-ZnTe has a moderate

doping while the n-CdS is heavily doped. Since the $N_D \gg N_A$, it thus shows that the fabricated hetero-junction is a one-sided n^+p junction diode. The results obtained in the n^+p HJ device structure are in good agreement with what was earlier obtained in the glass/FTO/p-ZnTe/Al and glass/FTO/n-CdS/Au device structures. Due to the high doping concentration in the n-region, the depletion width (X_n=13.0 nm) becomes very small, almost negligible. This is unlike the p-region which is moderately-doped; the moderate-doping in the p-region thus enhances an increase in the depletion width (X_p=506.0 nm). The fabricated diodes are therefore one-sided n^+p junction diodes since $N_D >> N_A$ and $X_n \ll X_p$.

The summary of electronic parameters of the fabricated n^+p junction diodes obtained by C-V measurement at room temperature is shown in Table 7.4.

Table 7.4. Summary of electronic parameters obtained from glass/FTO/n-CdS/p-ZnTe/Au HJ device structures using C-V technique.

N_A	V_{bi}	N_D	E_F-E_V	E_C-E_F	X_n	X_p	$W = X_n+X_p$	E
(cm^{-3})	(V)	(cm^{-3})	(eV)	(eV)	(nm)	(nm)	(nm)	(Vcm^{-1})
2.47×10^{15}	0.55	3.75×10^{18}	0.18	-0.01	13.0	506.0	519.0	2.22×10^4

The Fermi level positions of the donor atoms and acceptor atoms were determined using Equations (3.45) and (3.47) respectively. The result of the Fermi level position for donor atoms show that the CdS semiconductor in the hetero-structure is degenerate since E_C-E_F is negative. For the ZnTe semiconductor, the Fermi level position for acceptor atoms is positive and this indicates that the E_F is situated above the E_{Vmax}. The knowledge of the Fermi level position is important in drawing the energy band diagram of the device structure; this has been further explained in sub-section 7.4.1.5. For the abrupt n^+p junction diodes fabricated from the glass/FTO/n-CdS/p-ZnTe/Au HJ device structure, the electric field at the junction was estimated to be 2.22×10^4 Vcm^{-1} using Equation (3.48) of Chapter 3. The electric field obtained for the n^+p HJ diode in this work is similar to that reported by Kabra et al. [33] for rectifying p-n junction diodes fabricated from p-ZnO/n-Si hetero-structure.

7.4.1.5 Proposed space charge density and energy band-diagram for CdS/ZnTe hetero-junction devices

By combining the n^+-CdS and p-ZnTe into a single device structure, a one-sided CdS/ZnTe n^+p junction was fabricated since $N_D >> N_A$. The knowledge of the electronic parameters in Table 7.4 have been used to propose the space charge density and energy band diagram of the n^+p hetero-junction device structure. Figure 7.13 (a) shows the probable space-charge density of n^+p junction that can be obtained after putting the two semiconductor materials together to form a device structure.

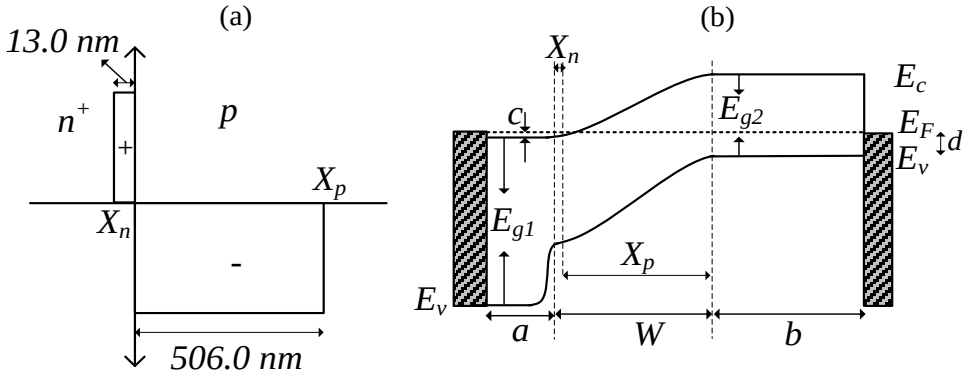


Figure 7.13. (a) Proposed space charge density of one-sided CdS/ZnTe n^+p junction. (b) Proposed energy band diagram of n^+p hetero-junction device structure. E_{g1} is the CdS bandgap, E_{g2} is the ZnTe bandgap used in this work, $W = X_n + X_p$, $a+X_n$ = total thickness of CdS layer = ~45 nm, X_p+b = total thickness of ZnTe layer = ~1200 nm, $c = E_C-E_F$, $d = E_F-E_V$. Note that the above bandgap diagram is not drawn to scale.

Figure 7.13 (a) thus shows that the whole space charge layer stretches into the low-doped region of the junction. This is so because the depletion width is an inverse function of the doping concentration. From Figure 7.13 (a), depletion width, $W= X_p + X_n$ where X_p and X_n are the distances by which the depletion region extends into the p- and n-type semiconductor respectively. Since $N_D >> N_A$, then $X_n << X_p$; thus, the total depletion width, $W \approx X_p$. The proposed energy band diagram for the n^+p hetero-junction device structure is shown in Figure 7.13 (b).

7.4.2 The n-CdS/p-ZnTe hetero-junction as a PV solar cell

The p-ZnTe layers used in the fabrication of solar cells with device structure glass/FTO/n-CdS/p-ZnTe/Au were grown from 0.045 M of Zn precursor and 10 ml of

TeO_2. As previously explained, the ZnTe electroplated from this electrolyte is referred to as Zn-rich ZnTe. Due to the poor solar cell activities produced from p-ZnTe grown from Te-rich ZnTe electrolyte, the concentration of Zn in the bath was increased to 0.045 M while still keeping the Te concentration fixed.

7.4.2.1 Analysis of electronic parameters obtained from n-CdS/p-ZnTe device structures using I-V and C-V techniques

The measurement of solar cells under dark and illumination conditions is important so as to obtain electronic parameters which can be used to describe the cell behaviour. The CdS/ZnTe device structures discussed in this section were treated with and without $CdCl_2$ before making Au contacts on them. Six cells were measured from each set of device structures and their solar cell parameters obtained from I-V under AM1.5 illumination and corresponding doping density obtained from C-V measurements under dark condition at room temperature are summarised in Table 7.5 and Table 7.6. Table 7.5 and Table 7.6 give the summary of results obtained for device structures without and with $CdCl_2$ treatment prior to annealing and metallisation respectively. For the purpose of critical analysis and comparison, the best cell in each set was selected for further discussion. In Table 7.5, sample P105B_14 was selected while from Table 7.6, sample P105C_46 was chosen; both are plotted on same graph for comparison purpose.

The I-V curves of the best cells are shown in Figure 7.14. Figure 7.14 (a) illustrates the log-linear I-V characteristics while Figure 7.14 (b) shows the linear-linear I-V characteristics. Electronic parameters such as *RF*, *n*, I_s and ϕ_b were obtained from Figure 7.14 (a). The R_s and R_{sh} were obtained from Figure 7.14 (b).

Table 7.5. Summary of device parameters obtained for CdS/ZnTe device structures annealed without any chemical treatment at 400^{o}C for 10 minutes in air prior to metal contact formation.

Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF (%)	η (%)	N_A-N_D (cm^{-3})
P105B_35	350	2.83	0.26	0.26	1.25×10^{16}
P105B_33	400	4.10	0.25	0.41	1.47×10^{16}
P105B_25	400	4.77	0.27	0.52	1.50×10^{16}
P105B_16	450	6.45	0.32	0.93	1.56×10^{16}
P105B_13	450	7.40	0.30	0.99	2.36×10^{16}
P105B_14	450	7.26	0.31	1.01	2.48×10^{16}

Table 7.6. Summary of device parameters obtained for CdS/ZnTe device structures annealed with $CdCl_2$ treatment at 400°C for 10 minutes in air prior to metal contact formation.

Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF (%)	η (%)	N_A-N_D (cm^{-3})
P105C_24	380	24.0	0.36	3.28	2.22×10^{17}
P105C_37	440	17.6	0.43	3.33	1.12×10^{17}
P105C_16	400	23.1	0.45	4.16	1.02×10^{17}
P105C_13	400	25.0	0.45	4.50	6.02×10^{16}
P105C_03	520	20.5	0.48	5.12	5.74×10^{16}
P105C_46	480	24.0	0.46	5.30	5.58×10^{16}

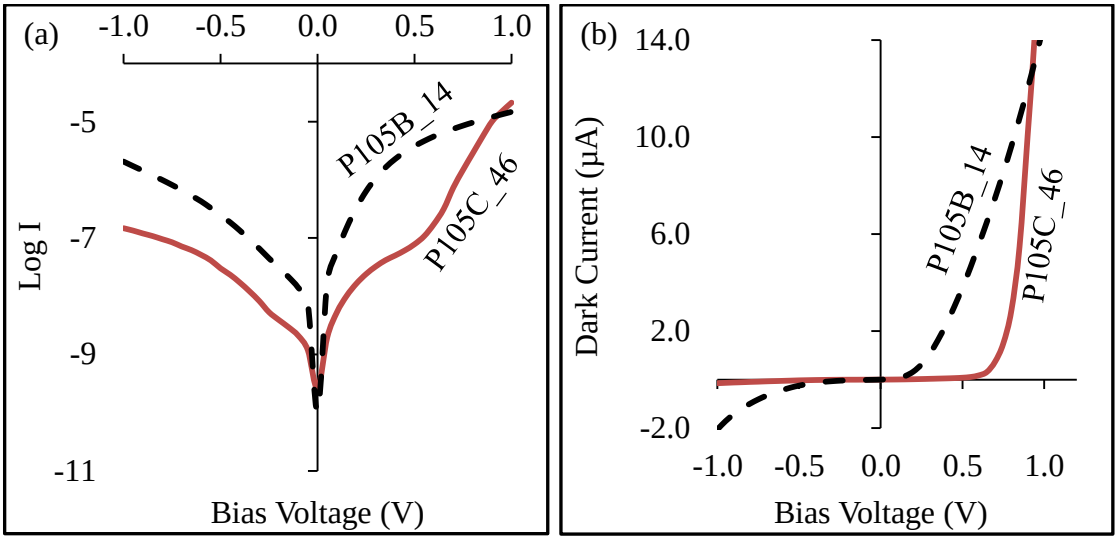


Figure 7.14. I-V characteristics of n-CdS/p-ZnTe device structures under dark condition (a) Log-linear I-V and (b) Linear-linear I-V. Note that P105B_14 and P105C_46 represent the n-CdS/p-ZnTe device structures treated without and with $CdCl_2$ respectively.

Table 7.7 gives the summary of I-V parameters measured under dark and light conditions. As shown in Table 7.7, the quality of rectifying diode also known as *RF* is better in sample P105C_46 than sample P105B_14. One of the main challenges encountered in the p-n junction diodes fabricated from n-CdS/p-ZnTe is the high R_s values in both heat-treated (HT) and $CdCl_2$ (CC) - treated samples. After CC-treatment, the R_s reduced from 40 kΩ to ~6.6 kΩ under dark condition. It should be noted that in order to produce solar cells with better performance, the R_s should be as low as possible and R_{sh} should be as high as possible (for an ideal solar cells, the $R_s = 0$ and $R_{sh} \rightarrow \infty$).

Generally, R_s is caused by the bulk resistance of the semiconductor material, the resistance of the electrical contacts and the interconnections. The main impact of the large R_s is to reduce the V_{oc}, *FF* and the gradient of the log-linear curve at the high forward-bias region, hence, increasing the *n* value and reducing the cell efficiency [34]. However, if the R_s is extremely large as seen in sample P105B_14 under dark, it can significantly reduce the J_{sc}.

Table 7.7. Summary of device parameters of best cells obtained from n-CdS/p-ZnTe device structures treated without and with $CdCl_2$ under dark and illumination conditions.

Treatment Condition	Dark I-V Parameters								Light I-V Parameters		
	Sample ID	*RF*	*n*	I_s (nA)	ϕ_b (eV)	R_s (kΩ)	R_{sh} (MΩ)	V_t (V)	η (%)	R_s (Ω)	R_{sh} (Ω)
HT-treated	P105B_14	$10^{1.0}$	3.13	56.20	>0.72	40.0	0.16	0.20	1.01	1592	4053
CC-treated	P105C_46	$10^{2.2}$	2.36	0.10	>0.89	~6.6	3.70	0.70	5.30	255	4246

The experimental work carried out by Rohatgi et al. [35] revealed that annealed CdZnTe thin films with highest R_s showed lower Te contents compared to the (Cd+Zn) contents. The presence of high R_s under dark conditions as seen in the fabricated diodes in this work can therefore be attributed to the presence of excess concentration of Zn elements present in the electrolyte. Nonetheless, it is good to have a reasonable concentration of Zn source in the bath so as to achieve a good PV effect under illumination. To overcome this limitation, researchers have used external dopants like Cu [36] and Na [37] to reduce the resistivity of ZnTe thin films so as to achieve better solar cell devices. Though in this study, external dopants have not been used. This could therefore be the reason why high R_s values were observed in the fabricated diodes despite its PV activity. For the initial p-ZnTe layers grown from Te-rich ZnTe electrolyte and used as hetero-partner to n-CdS thin films, good diodes with low R_s were obtained but the PV activity under illumination was very poor. Therefore, to produce solar cell devices with good PV effect using ZnTe as an absorber material or as a back contact to CdTe absorber material, it is proper to use higher concentration of Zn (~0.045M of Zn precursor) as compared to the 0.015M and incorporate external dopants like Cu to reduce its R_s.

The value of R_{sh} obtained in diodes fabricated from CC-treated layer is ~23 times larger than the R_{sh} values obtained in the diodes fabricated from heat-treated device structures only. Low values of R_{sh} observed in sample P105B_14 signify existence of leakage paths for the photo-generated charge carriers; this means that the amount of current flow through the external circuit reduces and this eventually leads to a reduction in the cell performance [38]. When a diode is having low R_{sh}, instead of the photo-generated current to pass through external circuit to produce useful electricity, it leaks away within the device structure. This leakage thereby gives rise to the diode leakage current which is also referred to as the reverse saturation current. For this reason, diodes with low R_{sh} tend to have very high leakage current since the low R_{sh} provides an alternative path for the generated current to flow. As shown in Table 7.7, sample P105B_14 with low R_{sh} of 0.16 MΩ has a high I_s of 56.2 nA while sample P105C_46 with high R_{sh} of 3.70 MΩ has a low I_s of 0.1 nA. This result shows that $CdCl_2$ treatment plays a major role in reducing the leakage path for the photo-generated charge carriers.

Another useful parameter which is also of electronic importance is the ϕ_b. The ϕ_b depends on I_s and it determines the threshold voltage (V_t) of the diode when measured under dark or the open circuit voltage (V_{oc}) when measured under AM1.5 illumination. As seen in Table **7.7**, a massive improvement was observed in V_t of the p-n junction diodes from 0.20 V to 0.70 V after $CdCl_2$ treatment. Under illumination condition, the V_{oc} slightly increased from 0.450 V to 0.480 V after $CdCl_2$ treatment. This improvement in V_t and V_{oc} after $CdCl_2$ treatment is due to the reduced I_s and higher ϕ_b obtained in sample P105C_46 as compared to sample P105B_14. Researchers have shown that increase in I_s can lead to decrease in the V_{oc} [39,40]. The breakdown voltage (V_{bd}) is equally important when dealing with electronic devices. As seen in Figure 7.14 (b), the V_{bd} of the p-n junction diode was improved after $CdCl_2$ treatment. The p-n device structure treated without $CdCl_2$ treatment breaks down easily when the reverse voltage slightly exceeds 0.5 V. Due to this breakdown, large reverse saturation current of ~56.2 nA flows through the device while in the case of diodes fabricated from $CdCl_2$ treated device structure, no obvious breakdown occurs even at higher reverse voltage of 1.0 V. Due to the non-breaking nature of this diode, tiny currents of ~0.1 nA flow through the diode when reverse biased. The negligible reverse currents which flow through the diode P105C_46 make it suitable for application in electronic devices. The value of ideality factor (n) for an ideal diode which can produce excellent solar to electric conversion efficiency should be equal to unity. However in practice, this is not always

obtainable due to the native defects in the semiconductor materials. The *n* values obtained in both devices are high and this indicates the presence of defects, interfacial charges, recombination and generation centres in the fabricated device structures [41].

Figure 7.15 shows the I-V characteristics under illumination obtained for n-CdS/p-ZnTe solar cells. The summary of the obtained I-V parameters under illumination condition for the two solar cells discussed in this section are highlighted in Table 7.5 and Table 7.6. The highlighted parameters in Table 7.5 and Table 7.6 represent solar cells fabricated from n-CdS/p-ZnTe device structures treated without and with $CdCl_2$ solution respectively. The drastic reduction of R_s under illumination condition (that is, from 40 kΩ under dark to ~1.6 kΩ under illumination for sample P105B_14 and from 6.6 kΩ under dark to ~255 Ω under illumination for sample P105C_46) shows that the materials exhibit photo-conductivity and devices show improved photo-voltaic activity.

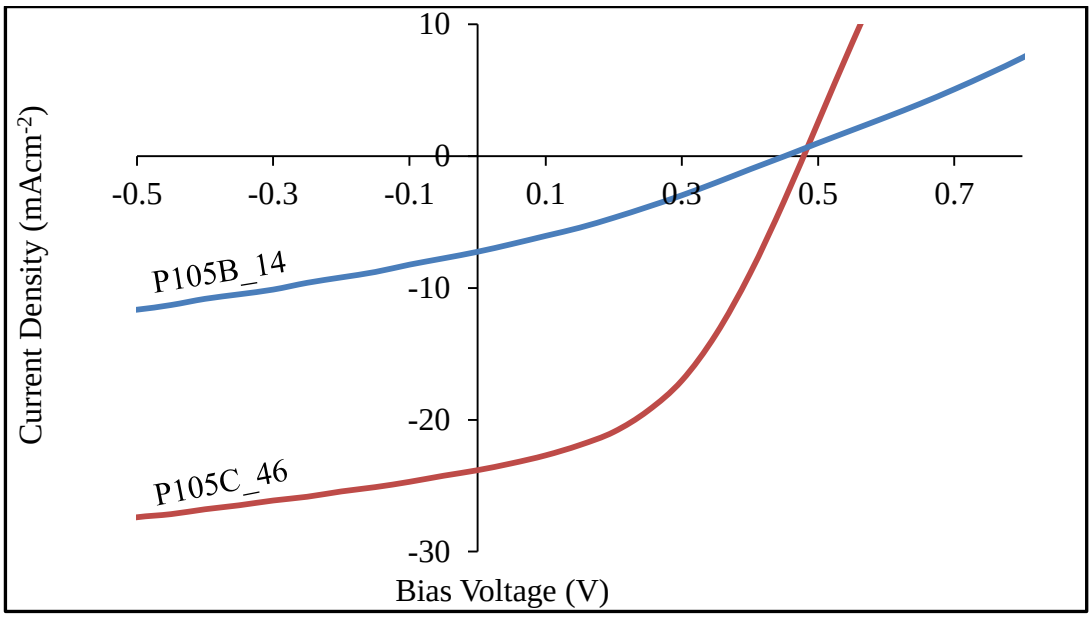


Figure 7.15. I-V characteristics of device parameters obtained for n-CdS/p-ZnTe device structures treated without and with $CdCl_2$ under AM 1.5 illumination condition. Note that P105B_14 and P105C_46 represent the n-CdS/p-ZnTe device structures treated without and with $CdCl_2$ respectively.

Overall, all the parameters of CdS/ZnTe device structures treated with $CdCl_2$ before annealing in air improved when compared to the ones annealed without any chemical treatment. This is seen in the summarised results of Table 7.7. The final solar cell efficiency obtained for devices labelled P105B_14 and P105C_46 are ~1.01% and 5.30% respectively. One possible reason for the high efficiency observed in CC-treated

ZnTe layer may be the removal of some defects at the back contact area as a result of $CdCl_2$ treatment. At the same time, the diffusion of Cl from the $CdCl_2$ treatment to the ZnTe layer could help in grain growth and grain boundary passivation [42]; this is very similar to what happens in CdTe films.

7.4.2.2 C-V analysis of best cells selected from n-CdS/p-ZnTe device structures treated without and with $CdCl_2$ treatment

The C-V and Mott-Schottky plots of ordinary heat-treated glass/FTO/n-CdS/p-ZnTe/Au HJ device structure with 2 mm diameter active areas are shown in Figure 7.16 (a) and 7.16 (b) respectively while the C-V and Mott-Schottky plots of CC-treated glass/FTO/n-CdS/p-ZnTe/Au solar cells are represented in Figure 7.16 (c) and 7.16 (d) respectively.

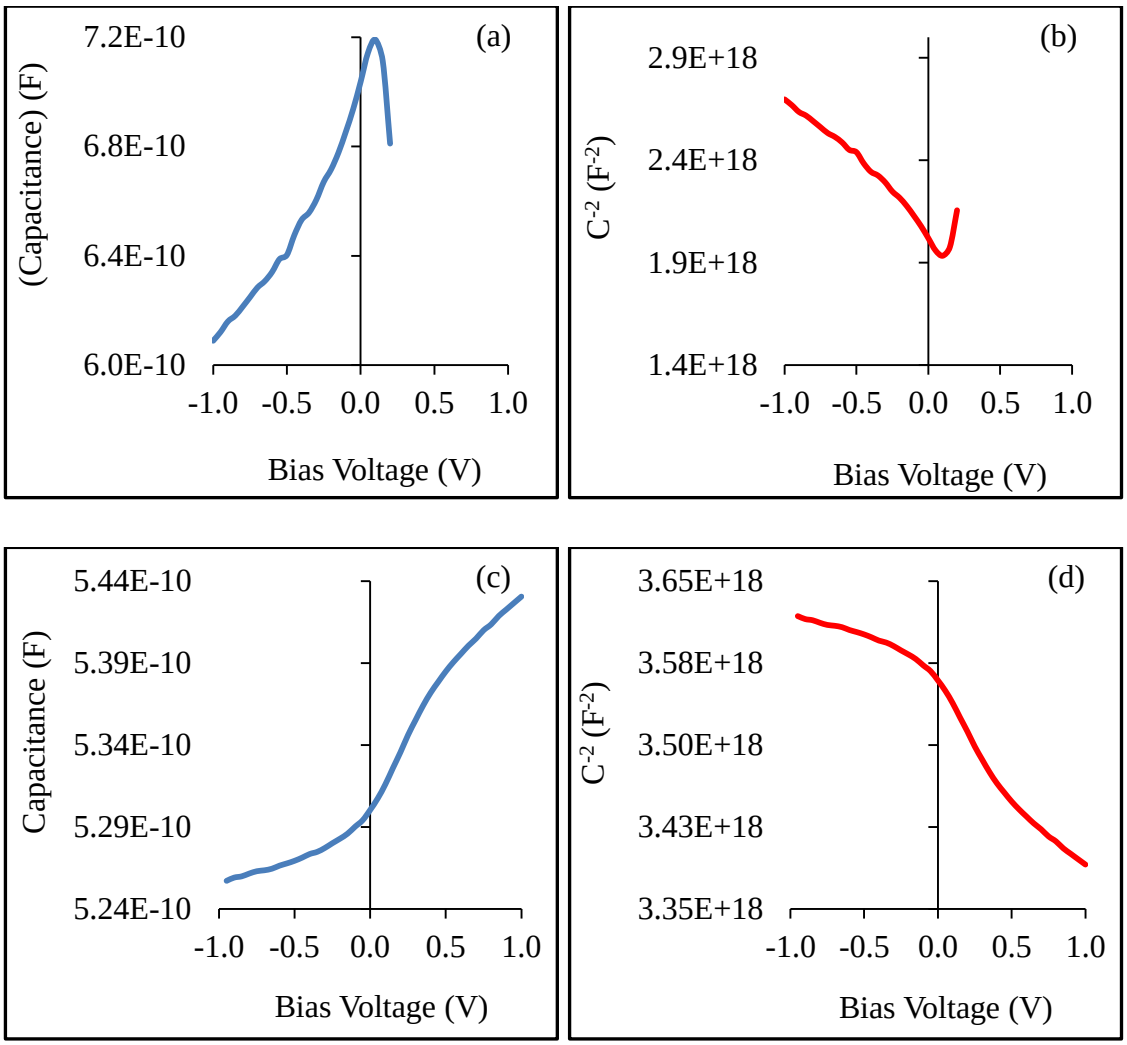


Figure 7.16. Typical C-V characteristics of heat-treated glass/FTO/n-CdS/p-ZnTe/Au device structure (a) capacitance vs bias voltage, (b) C^{-2} vs V graphs and typical C-V characteristics of $CdCl_2$-treated glass/FTO/n-CdS/p-ZnTe/Au device structure (c) capacitance vs bias voltage, (d) C^{-2} vs V graphs.

As shown in Figure 7.16 (a) and 7.16 (c), the observed depletion capacitances at zero bias (C_o) for the HT and CC-treated samples are ~704 pF and ~530 pF respectively. The depletion width of the samples were calculated using Equation (3.38) and the results are given in Table 7.8. It can be seen that the depletion width of the HT sample has increased from 411 nm to 546 nm after CC-treatment. The wider depletion width of the CC-treated sample shows that stronger built-in electric field is available in the depletion region of the device to separate the photo-generated charge carriers. Equation (3.50) was used in estimating the value of electric field at the interface of the p-n junction device. The results as given in Table 7.8 show that CC-treated samples have higher electric field at the p-n junction than HT samples.

Table 7.8. Summary of C-V results obtained for HT- and CC-treated glass/FTO/n-CdS/p-ZnTe/Au solar cell device structures.

Treatment Condition	Dark C-V Parameters					
	Sample ID	C_o (pF)	W (nm)	N_A-N_D (cm^{-3})	E_F-E_V (eV)	E_{max} (Vcm^{-1})
HT-treated	P105B_14	704	411	2.48×10^{16}	~0.12	1.77×10^{5}
CC-treated	P105C_46	530	546	5.58×10^{16}	~0.10	5.29×10^{5}

Figure 7.16 (b) and 7.16 (d) show the Mott-Schottky plots of the HT- and CC-treated glass/FTO/n-CdS/p-ZnTe/Au solar cells. The non-linear shape of the Mott-Schottky plots indicate that the doping levels are non-uniformly distributed in the n-CdS/p-ZnTe layers [43]. Also the non-linearity of the Mott-Schottky plots represents the presence of trap levels in the forbidden band of ZnTe layers [44]. The doping concentration (N_A-N_D) for holes calculated from Figure 7.16 (b) and 7.16 (d) are 2.48×10^{16} and 5.58×10^{16} cm^{-3} for HT and CC-treated samples respectively. The Fermi level positions (E_F-E_V) stated in Table 7.8 shows that the CC-treated sample is closer to the E_{vmax} than the HT-sample. This closeness enhances an increase in the barrier height as seen in Table 7.7. The graph of efficiency obtained from solar cells fabricated from CC-treated glass/FTO/n-CdS/p-ZnTe device structures versus the doping density of holes in the p-n hetero-structure is shown in Figure 7.17. The result in Figure 7.17 shows that efficiency increases as the doping density decreases.

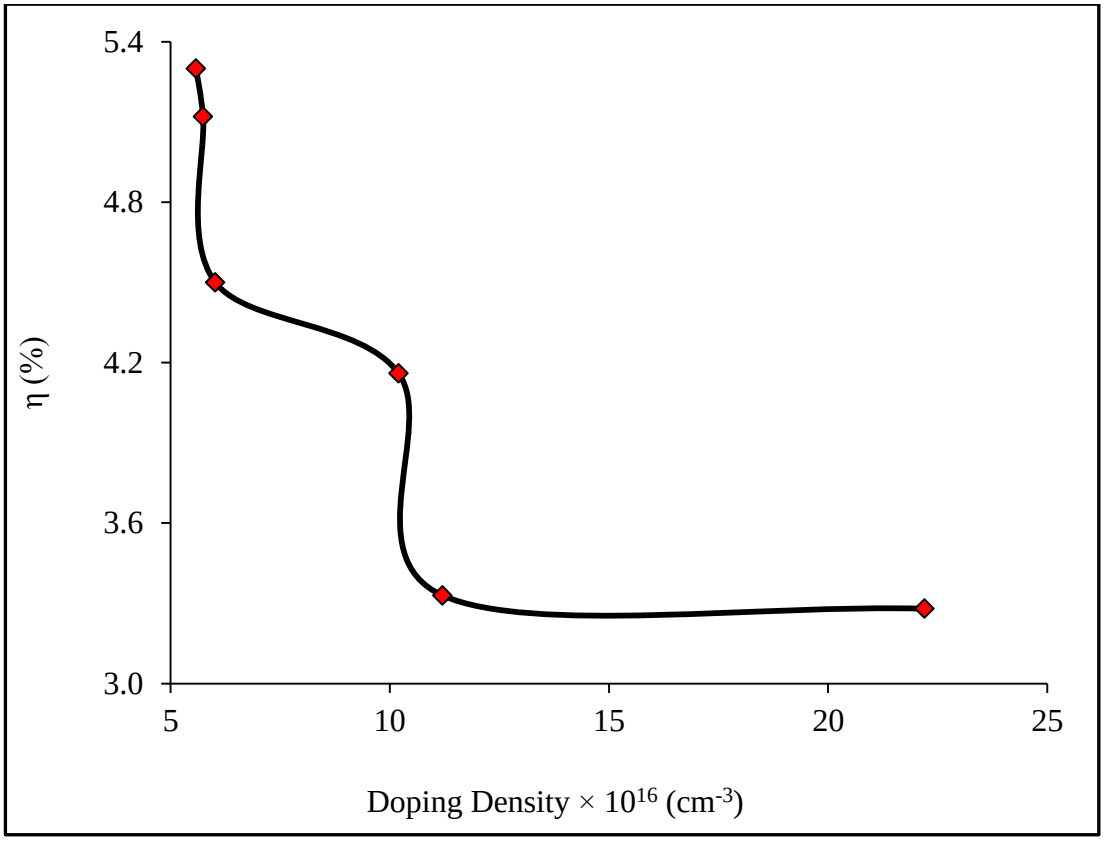


Figure 7.17. Efficiency versus doping density for n-CdS/p-ZnTe solar cell devices fabricated from CC-treated glass/FTO/n-CdS/p-ZnTe device structures.

Comparative study of p-n junction diodes fabricated from Te-rich ZnTe and Zn-rich ZnTe electrolyte indicate that the electric fields at the p-n interface of diodes fabricated from Zn-rich ZnTe electrolyte are generally higher than those of Te-rich ZnTe electrolyte. The presence of stronger electric field obtained at the interface of p-n junction diode from Zn-rich ZnTe electrolyte may therefore be one of the reasons why the fabricated solar cells from Zn-rich ZnTe electrolyte are better than the Te-rich ZnTe electrolyte. Also, diodes fabricated from Zn-rich ZnTe bath has lower capacitance than the ones made from Te-rich ZnTe bath as observed from this work. This result agrees with the experimental investigations reported by Naby et al. [41] that capacitance decreases with increase in Zn concentration.

7.5 Summary

The results presented in this chapter showed that due to the bandgap modification of ZnTe thin films, it can be employed as an absorber layer to n-CdS thin films. ZnTe layers grown from Zn-rich ZnTe electrolyte possess better crystallinity and material quality than the ones grown from Te-rich ZnTe electrolyte. Both categories of ZnTe layers were grown on n-CdS thin films to make electronic devices. The effect of treating the top surface of ZnTe monolayer with $CdCl_2$ solution was investigated before applying it to CdS/ZnTe-based device structures. The results from structural analysis revealed that the $CdCl_2$ treatment does not add additional phase to the ZnTe thin films or convert the film to another compound. p-n junction diodes were made using n-CdS and p-ZnTe grown from Te-rich and Zn-rich electrolyte. The C-V results of diodes fabricated using p-ZnTe grown from a Te-rich ZnTe electrolyte confirmed the successful fabrication of one-sided rectifying p-n junction diodes. A comparative study of fabricated diodes and solar cells showed that ZnTe absorber layers electroplated from Zn-rich ZnTe electrolyte is a better hetero-partner to CdS thin films than ZnTe absorber layers electroplated from Te-rich ZnTe electrolyte. Future work should focus on developing multi-junction graded bandgap solar cells incorporating ZnTe and CdS thin films into the structure.

References

[1] F. Chernow, Appl. Phys. Lett., **12** (1968) 339.

[2] P. J. Sebastian, Appl. Phys. Lett., **62** (1993) 2956.

[3] F. Fauzi, D. G. Diso, O. K. Echendu, V. Patel, Y. Purandare, R. Burton, I. M. Dharmadasa, Semicond. Sci. Technol., **28** (2013) 045005.

[4] G. Mandel, Phys. Rev., **134** (1964) A1073–A1079.

[5] K. Sato, M. Hanafusa, A. Noda, A. Arakawa, IECE Trans. Electron., **E83** (2000) 579–584.

[6] O. I. Olusola, M. L. Madugu, N. A. Abdul-Manaf, I. M. Dharmadasa, Curr. Appl. Phys., **16** (2016) 120–130.

[7] T. Ota, K. Kobayashi, K. Takahashi, Solid. State. Electron., **15** (1972) 1387–1388.

[8] T. Ota, K. Kobayashi, K. Takahashi, J. Appl. Phys., **45** (1974) 1750–1755.

[9] M. Aven, D. M. Cook, J. Appl. Phys., **32** (1961) 960.

[10] M. Aven, W. Garwacki, J. Electrochem. Soc., **110** (1963) 401.

[11] F. Pfisterer, H. W. Schock, J. Cryst. Growth, **59** (1982) 432–439.

[12] J. D. Major, K. Durose, 2013 IEEE 39th Photovolt. Spec. Conf., (2013) 1146–1149.

[13] T. Ishizaki, T. Ohtomo, A. Fuwa, J. Phys. D. Appl. Phys., **37** (2004) 255–260.

[14] M. F. Gromboni, F. W. S. Lucas, L. H. Mascaro, J. Braz. Chem. Soc., **25** (2014) 526–531.

[15] T. Ishizaki, T. Ohtomo, Y. Sakamoto, A. Fuwa, Mater. Trans., **45** (2004) 277–280.

[16] G. B. Sakr, I. S. Yahia, J. Alloys Compd., **503** (2010) 213–219.

[17] G. K. Rao, K. V. Bangera, G. K. Shivakumar, Solid. State. Electron., **56** (2011) 100–103.

[18] A. B. M. O. Islam, N. B. Chaure, J. Wellings, G. Tolan, I. M. Dharmadasa, Mater. Charact., **60** (2009) 160–163.

[19] O. I. Olusola, V. Patel, I. M. Dharmadasa, Optimisation of pH for Electrodeposition of n-CdSe Thin Films for Applications in Photovoltaic Devices, in: EUPVSEC 2014 Conf. Proc., (2014): pp. 1852–1856.

[20] U. Jahn, T. Okamoto, A. Yamada, M. Konagai, J. Appl. Phys., **90** (2001) 2553–2558.

[21] J. D. Major, L. Bowen, R. E. Treharne, L. J. Phillips, K. Durose, IEEE J. PHOTOVOLTAICS, **5** (2015) 386–389.

[22] D. Mohanty, P. Y. Su, G. C. Wang, T. M. Lu, I. B. Bhat, Sol. Energy, **135** (2016) 209–214.

[23] Y. F. Lin, J. Song, Y. Ding, S. Y. Lu, Z. L. Wang, Adv. Mater., **20** (2008) 3127–3130.

[24] M. G. Helander, M. T. Greiner, Z. B. Wang, W. M. Tang, Z. H. Lu, J. Vac. Sci. Technol. A Vacuum, Surfaces, Film., **29** (2011) 011019.

[25] R. Amutha, Adv. Mater. Lett., **4** (2013) 225–229.

[26] C. J. Chen, Physics of Solar Energy, John Wiley & Sons, Hoboken, New Jersey (2011).

[27] A. Rao, S. Krishnan, G. Sanjeev, K. Siddappa, Int. J. Pure Appl. Phys., **5** (2009) 55–62.

[28] O. K. Echendu, I. M. Dharmadasa, Energies, **8** (2015) 4416–4435.

[29] I. S. Yahia, G. B. Sakr, T. Wojtowicz, G. Karczewski, Semicond. Sci. Technol., **25** (2010) 095001.

[30] V. P. Singh, H. Brafman, J. Makwana, J. C. McClure, Sol. Cells, **31** (1991) 23–38.

[31] D. A. Neamen, Semiconductor Physics and Devices: Basic Principles, third ed., McGraw-Hill, New York (2003).

[32] Y. Masumoto, H. Umino, J. Sun, E. Suzumura, Phys. Chem. Chem. Phys., **17**

(2015) 25278–25282.

[33] V. Kabra, L. Aamir, M. M. Malik, Beilstein J. Nanotechnol., **5** (2014) 2216–2221.

[34] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[35] A. Rohatgi, S. A. Ringel, R. Sudharsanan, P. V Meyers, C. H. Liu, V. Ramanathan, Sol. Cells, **27** (1989) 219–230.

[36] V. S. John, T. Mahalingam, J. P. Chu, Solid. State. Electron., **49** (2005) 3–7.

[37] K. C. Park, E. S. Cha, B. T. Ahn, Curr. Appl. Phys., **11** (2011) S109–S112.

[38] O. I. Olusola, M. L. Madugu, I. M. Dharmadasa, Improvement of CdS/CdTe Solar Cell Parameters using ZnS Buffer Layer, in: Proc. of PVSAT-12, Liverpool (2016): pp. 107–110. http://www.pvsat.org.uk/proceedings/.

[39] S. Messina, M. T. S. Nair, P. K. Nair, J. Phys. D. Appl. Phys., **41** (2008) 095112.

[40] E. W. Jones, V. Barrioz, S. J. C. Irvine, D. Lamb, Thin Solid Films, **517** (2009) 2226–2230.

[41] M. A. Naby, A. Zekry, F. E. Akkad, H. F. Ragaie, Sol. Energy Mater. Sol. Cells, **29** (1993) 97–108.

[42] I. M. Dharmadasa, Coatings, **4** (2014) 282–307.

[43] C. Bhattacharya, J. Datta, J. Solid State Electrochem., **11** (2007) 215–222.

[44] O. Almora-Rodriguez, L. Vaillant, A. Bosio, Rev. Cub. Fis., **66** (2014) 1–4.

Chapter 8 - Electrodeposition and characterisation of CdTe thin films

8.1 Introduction

This chapter describes the cathodic electrodeposition of CdTe thin films on FTO-coated glass substrates using two-electrode system and aqueous acidic electrolyte. The material properties of electrodeposited (ED) CdTe layers were studied using some of the analytical techniques discussed in Chapter 3. The effects of annealing temperatures on electrical properties of n- and p-CdTe thin films have been explored. The influence of different chemical treatments on the material and electronic properties of CdTe thin films have also been investigated. The pH variation of chemical solutions used for CdTe surface treatments have also been studied with respect to device fabrication. The Fermi level position of as-deposited and $CdCl_2$ treated CdTe thin films have also been studied.

8.2 Electrolyte preparation for CdTe thin films deposition

Before taking the cyclic voltammogram of electrolyte used in electroplating CdTe thin films, 1 M $CdSO_4$ (99% purity) was first electro-purified. The 1 M $CdSO_4$ was dissolved in a plastic beaker containing 800 ml of de-ionised water. The beaker was put inside an external glass beaker of 2000 ml for heating purpose. Before adding the dissolved TeO_2 solution, the 1 M $CdSO_4$ was electro-purified at cathodic potential of ~900 mV for ~80 hours so as to bring the impurity in the electrolyte to a minimal level. After performing the electro-purification, 5 ml of dissolved TeO_2 was added to the electro-purified bath; the electrolyte was allowed to stir continuously for ~12 hours before the commencement of CdTe thin films deposition. The procedures followed to dissolve TeO_2 powder have been explained in section 5.2 of Chapter 5. The pH value of the prepared electrolyte was maintained at 2.00±0.02 by using either NH_4OH or H_2SO_4. Acidic pH was used in this research work due to the instability of Te at pH >7.0, this alkaline pH leads to very poor adhesion of CdTe on the TCO substrate [1]. The growth temperature of the electrolytic bath was ~85^oC and the solution was moderately stirred using a magnetic stirrer.

In this research work, the concentration of $CdSO_4$ is always kept higher than the Te concentration; this is in accordance with the explanation given by Panicker et al. [2] that to deposit approximately equal amounts of Te and Cd, it is essential to prepare the

electrolyte using high concentration of Cd precursor which is a less noble element and low concentration of Te which happens to be a more noble element. The $CdSO_4$ and TeO_2 used as precursors for the CdTe electroplating work were purchased from Sigma Aldrich. The glass/FTO substrates used for this purpose was TEC 7 with a sheet resistance of 7 Ω/square. Before electrodeposition, the glass/FTO substrates were cut into small pieces with dimensions of 2×4 cm^2 and washed for ~15 minutes in an ultrasonic bath containing soap solution. The substrates were later washed using acetone and methanol solution to remove any form of grease and other surface contaminants. Finally, the substrates were rinsed with de-ionised water before being applied in the ED set-up.

8.3 Voltage optimisation and growth of CdTe thin films

This section discusses some of the techniques used in characterising CdTe thin films so as to select optimum voltage for growing nearly stoichiometric CdTe thin films. To achieve this, other preparative parameters such as the growth temperature, pH and growth time (t_g) were kept constant at 85^oC, 2.00±0.02 and one hour respectively.

8.3.1 Cyclic voltammetry

Cyclic voltammogram gives the details of how electric current flows in the electrolyte when the potentials between electrodes are varied. Cyclic voltammetry studies were carried out in an aqueous solution that contains 1 M $CdSO_4$ and 5 ml of dissolved TeO_2 solution at a pH of 2.00 ± 0.02. A FTO coated glass substrate was used as the working electrode to study the mechanism of deposition of CdTe thin films. A computerised GillAC potentiostat was used to carry out this voltammetric study at a sweep rate of 180 $mVmin^{-1}$. In this technique, a range of cathodic potentials from 0 to 2000 mV was applied across the electrolyte through the electrodes. The potentiostat was used in monitoring the current through the electrolyte as the voltages between electrodes are varied [3]. A typical cyclic voltammogram for FTO-coated glass substrate in the prepared electrolyte is shown in Figure 8.1. The forward curve at the inset of Figure 8.1 shows that Tellurium (Te) begins to deposit at ~145 mV. The redox potential (E^o) of Te and Cd are ~+593 and -403 mV respectively with respect to standard hydrogen electrode [4]. Te is expected to deposit first before Cd because it has a more positive redox potential than Cd. Also, Te deposits first being a nobler element [24,25] according to Equation (8.1).

$$HTeO_2^+ + 4e^- + 3H^+ = Te + 2H_2O \quad (8.1)$$

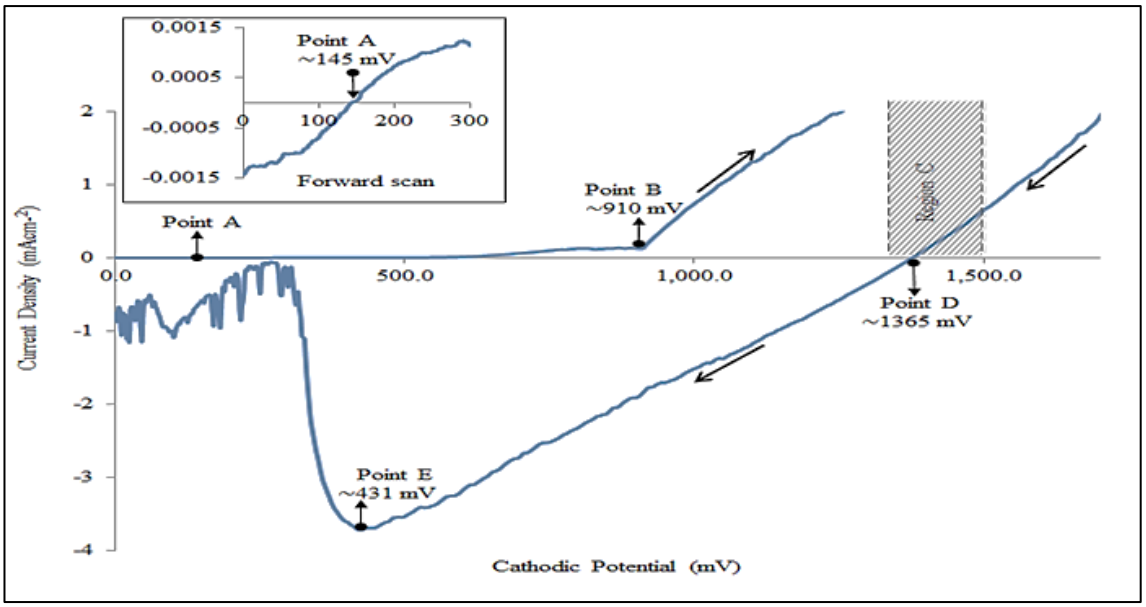


Figure 8.1. A typical cyclic voltammogram of electrolyte containing 1 M $CdSO_4$ and 5 ml of dissolved TeO_2 aqueous solution (pH = 2.00±0.02, T=85^{o}C).

The part labelled point B in Figure 8.1 indicates the voltage (~910 mV) at which Cd deposition starts to take place. The electrochemical reaction of Cd deposition is given by:

$$Cd^{2+} + 2e^- \rightarrow Cd \quad (8.2)$$

Beyond point B, an increase in current density was observed as the cathodic voltage increases. The rise in deposition current density after ~910 mV shows rapid discharge of Cd and reaction between Cd and Te to form CdTe. This rise indicates the initial co-deposition of CdTe on the working electrode (cathode) according to the chemical reaction in Equation (8.3)

$$Cd^{2+} + Te + 2e^- = CdTe \quad (8.3)$$

At low cathodic deposition voltage, a CdTe layer rich in Te is expected to be formed [25]. The amount of elemental Cd in the CdTe layer gradually increases as the deposition voltage increases; this allows a near stoichiometric CdTe layer to be formed. The part labelled region C shows the suitable voltage range for growing CdTe thin films. This voltage ranges between ~1350 to ~1500 mV and it has been identified as being suitable for growing CdTe layers according to this experimental result. By

combining Equations (8.1) and (8.2) together, the total chemical reaction required for the reduction of CdTe thin films on the cathode can be obtained as shown in Equation (8.4).

$$HTeO_2^+ + Cd^{2+} + 3H^+ + 6e^- \rightarrow CdTe + 2H_2O \quad (8.4)$$

From the reverse cycle of the I-V curve shown in Figure 8.1, the current flow transits from the positive to the negative at ~1365 mV. This voltage represents the potential at which the current produced due to material deposition is equal to current produced due to dissolution of material. As the current flow transits further in the negative reverse direction before reaching point E, removal of any elemental Cd and Cd from CdTe layer formed on the cathode takes place. The dissolution of Te from the surface of the cathode occurs at the broad peak point E which is ~431 mV. The essence of the reverse cycle is that below the transition point, the layer formed is Te-rich. The cyclic voltammetry is useful to find approximate voltage range to deposit CdTe layers after which the voltage range is optimised to find a suitable potential to grow nearly stoichiometric CdTe thin films.

8.3.2 Structural analysis using XRD technique

The structural properties of as-deposited (AD) and $CdCl_2$ (CC) treated CdTe layers were studied using X-ray diffraction technique. The CdTe layers were electroplated on glass/FTO substrates at different cathodic potentials from (1350-1440) mV; this task was carried out in order to obtain the optimum deposition voltage to grow nearly stoichiometric CdTe thin films. The XRD also helps in the identification of the crystal structure. The XRD spectra obtained for AD-CdTe layers are shown in Figure 8.2 (a) while Figure 8.2 (b) represents the graph of intensity of (111) peak for AD-CdTe layers as a function of cathodic potentials ranging between 1350 and 1440 mV. For the CC-treated CdTe layers, the XRD spectra are shown in Figure 8.3 (a) while Figure 8.3 (b) signifies the plot of (111) peak intensity as a function of cathodic potentials ranging between 1370 and 1420 mV for AD-CdTe layers, CdTe layers heat-treated (HT) ordinarily in air and CdTe layers treated with $CdCl_2$ (CC) solution before annealing in air. The heat-treatment was carried out in air at 400^{o}C for 10 minutes. For the CC-CdTe layers, the top surface of the CdTe layers were first treated with $CdCl_2$ solution, allowed to dry and then annealed.

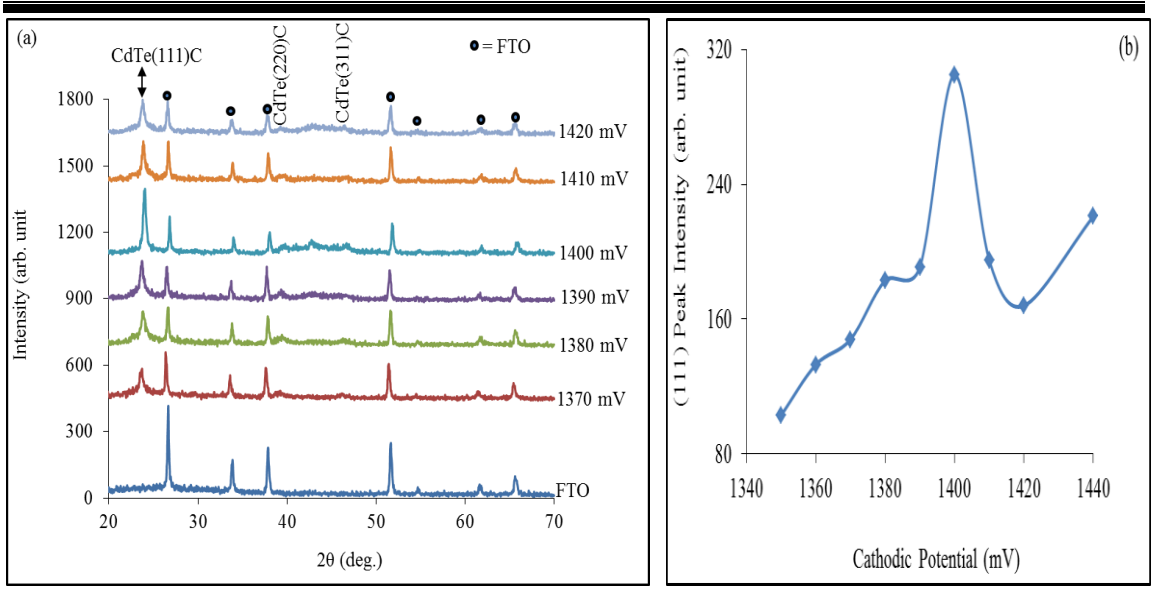


Figure 8.2. (a) The XRD spectra of as-deposited CdTe layers grown at cathodic deposition potentials ranging from 1370 to 1420 mV and (b) A plot of (111) peak intensity of as-deposited CdTe layers versus cathodic potentials ranging between 1350 and 1440 mV.

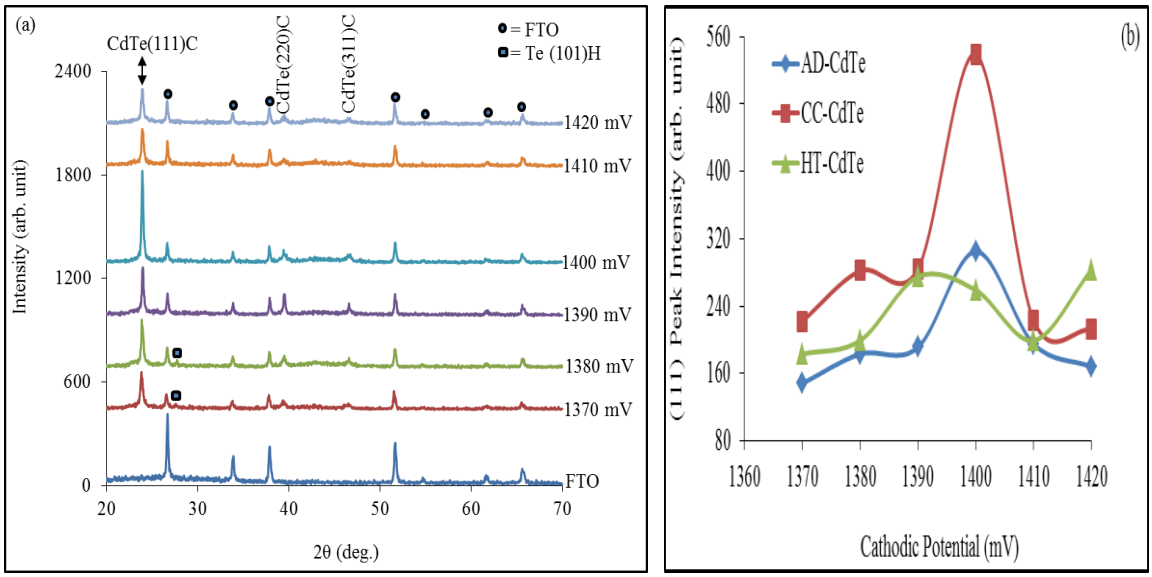


Figure 8.3. (a) The XRD spectra of $CdCl_2$ heat-treated CdTe layers grown at cathodic deposition potentials ranging from 1370 to 1420 mV and (b) A plot of (111) peak intensity of AD-, HT- and CC-CdTe layers versus cathodic potentials ranging between 1370 and 1420 mV.

The XRD spectra of AD- and CC- CdTe layers illustrated in Figure 8.2 (a) and Figure 8.3 (a) respectively showed that the CdTe thin films are polycrystalline and in all cases, the preferred orientation was found to be along the (111) plane. Aside the CdTe peak which showed the highest crystallinity along the (111) plane, other peaks of Cubic

CdTe were also found along the (220) and (311) planes at the peak positions $2\theta=39.43^{o}$ and 46.55^{o} respectively. These peaks have a much lower intensity when compared to the preferred orientation peaks. When the observed data from XRD measurements were compared with the JCPDS reference code: 00-015-0770 for CdTe, it was found out that the crystal structures were cubic. Figure 8.2 (a) and Figure 8.3 (a) show that the CdTe thin films grown at a cathodic potential of 1400 mV have the highest crystallinity peak for both AD- and CC-CdTe layers. For both AD- and CC-CdTe, the peak position for the preferred plane of orientation varied between $(23.61\text{-}24.15)^{o}$.

Figure 8.3 (b) illustrates the graph of intensity of (111) peak for AD-, HT and CC-CdTe layers as a function of cathodic deposition potentials ranging between 1370 and 1420 mV. As seen in Figure 8.3 (b), all the (111) peak intensities increased after $CdCl_2$ treatment for the CdTe layers grown between (1370-1420) mV when compared with AD-CdTe layers. This illustrates that $CdCl_2$ treatment assists in increasing the material crystallinity thus leading to improvement in the material stoichiometry. A gradual increase was observed in the peak intensity from 1370 to 1400 mV. Beyond 1400 mV, the (111) peak intensity starts to reduce. This experimental result shows that a cathodic potential (V_g) of 1400 mV may be ideal for growing nearly stoichiometric CdTe layers. The spectrum of (111) peaks for HT-CdTe layers shown in Figure 8.3 (b) deviates from the trend followed by AD- and CC-CdTe layers. The crystallite sizes for the CdTe samples were calculated for both AD- and CC-CdTe layers at different cathodic potentials using Scherrer's equation given in Equation (3.12) of Chapter 3; the details are shown in Table 8.1. The calculated crystallite sizes is a function of the full width at half maximum (FWHM) extracted from XRD measurement.

Table 8.1. Crystallite sizes estimation based on (111) peak of AD- and CC-CdTe at different cathodic deposition potentials.

	Extracted XRD parameters for AD-CdTe along (111) plane			Extracted XRD parameters for CC-CdTe along (111) plane		
Growth Voltage (mV)	Peak Position (^{o})	FWHM (^{o})	Crystallite Size (nm)	Peak Position (^{o})	FWHM (^{o})	Crystallite Size (nm)
1350	24.15	0.779	10.9	23.94	0.325	26.2
1360	23.87	0.519	16.3	23.84	0.292	29.1
1370	23.61	0.389	21.8	23.85	0.260	32.7
1380	23.82	0.324	26.1	23.92	0.195	43.6
1390	23.68	0.259	32.7	23.89	0.162	52.3
1400	23.88	0.259	32.7	23.89	0.162	52.3
1410	23.77	0.454	18.7	23.85	0.162	52.3
1420	23.96	0.520	16.3	23.92	0.162	52.3

Figure 8.4 shows the estimated crystallite sizes as a function of cathodic potentials. For the AD-CdTe, the crystallite sizes increase as the V_g increases from 1350 to 1390 mV. The same crystallite values were obtained for CdTe layers grown at 1390 and 1400 mV. Beyond this voltage, the size of the crystallites starts to decrease. For the CC-CdTe layers, the crystallite sizes also increase from 1350-1390 mV. The values obtained for the crystallites at 1390 mV and above remain the same. The saturation point reached here is an indication of the limitation of Scherrer's equation. This equation can only be used for poly-crystalline layers with certain size. As reported by Monshi et al. [7], Scherrer's equation mainly predicts the thickness of the crystallites if crystals are <100 nm. The grain sizes can best be estimated by techniques such as SEM and AFM.

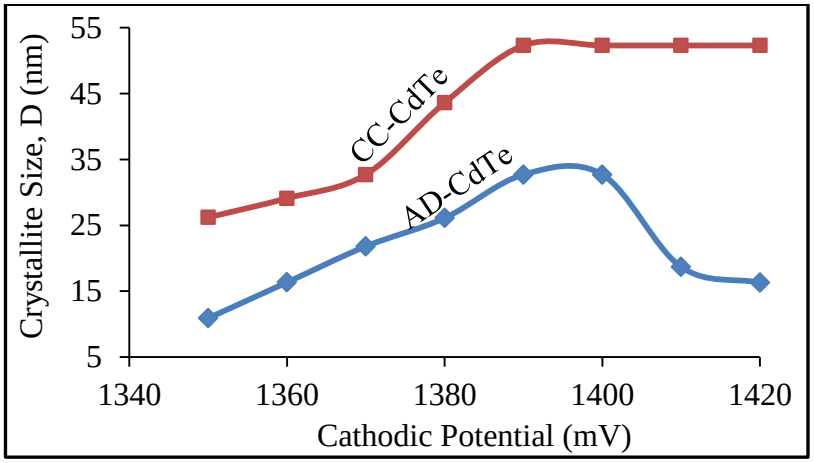


Figure 8.4. Estimated crystallite sizes of AD- and CC-CdTe thin films as a function of cathodic potential.

8.3.3 Optical Absorption

Using the UV-Vis spectrophotometer, the optical absorption measurements of electroplated CdTe layers were successfully carried out using the wavelength in the range 560-1000 nm. As illustrated in Figure 8.5, the energy bandgap was determined by extrapolating the tangent of the absorption curve to the photon energy axis. The optical absorption curves of AD- and CC-CdTe layers deposited at various cathodic voltages from 1350-1420 mV are shown in Figure 8.5 (a) and 8.5 (b) respectively. The bandgap of the as-deposited CdTe layers are in the range 1.25-1.55 eV while those of the CC-treated CdTe layers are in the range 1.10-1.54 eV. As seen in Figure 8.5 (a), lesser E_g values were observed at lower cathodic potentials. The reduction in bandgap as the deposition potential decreases is due to the deposition of semi-metallic Te with a

bandgap of ~0.37 eV [8]. It was observed that some of the CdTe thin films grown at lower V_g also exhibit Te peaks as seen from the XRD spectra in Figure 8.3 (a).

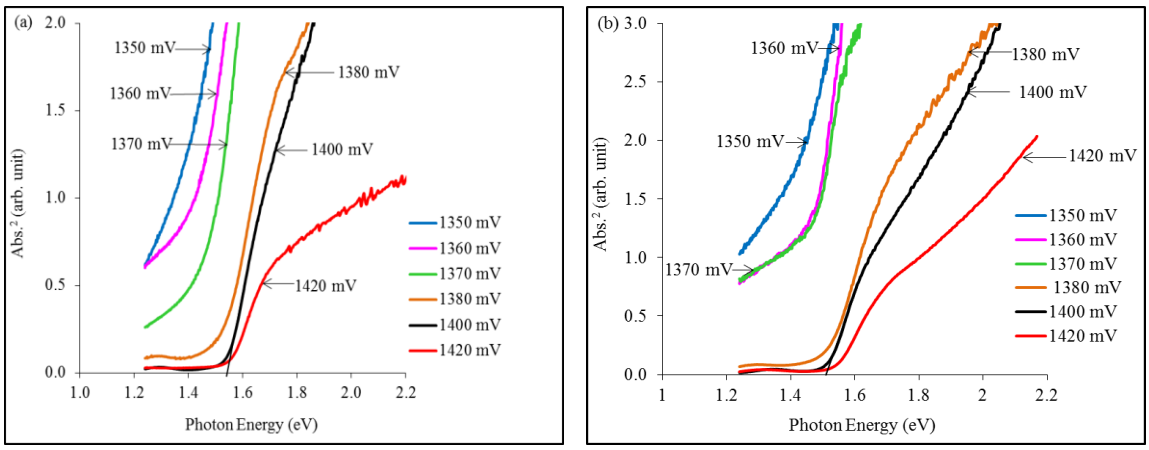


Figure 8.5. Optical absorption graphs of CdTe layers grown between 1350–1420 mV for (a) As-deposited CdTe layers and (b) CdTe layers heat-treated with $CdCl_2$ at 400°C for 10 minutes in air.

Figure 8.6 shows the trend at which the energy bandgaps of AD-CdTe and cadmium chloride heat-treated CdTe layers vary with the cathodic deposition potentials. For most of the CdTe thin films except the ones grown at 1360 mV, a reduction was observed in the energy bandgap after cadmium chloride treatment. The reduction in the bandgap after annealing was explained by Chaure et al. [9] with respect to the small grains present in AD-materials coalescing together to form larger grains after heat-treatment. Likewise, the reduction in the bandgap could also arise as a result of changes in the atomic composition of the electrodeposited semiconductor materials.

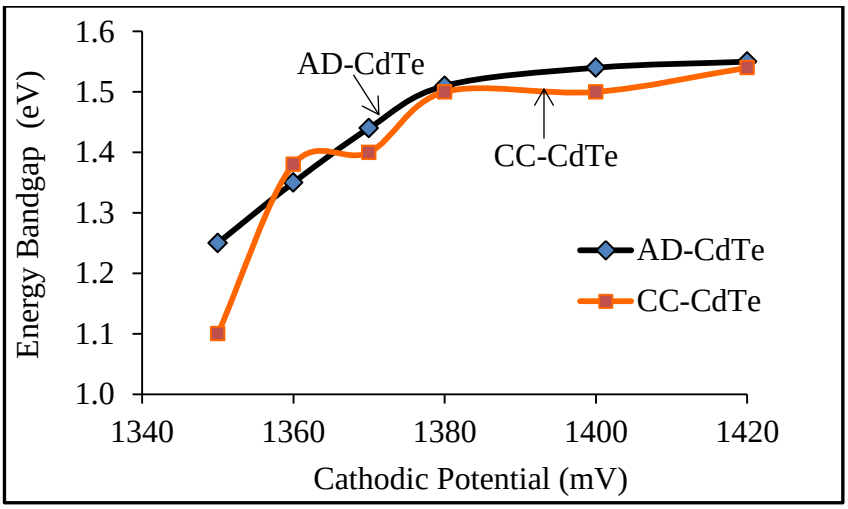


Figure 8.6. Variation of the energy bandgaps of CdTe layers as a function of cathodic deposition potentials for both AD- and CC-CdTe layers.

8.3.4 Photoelectrochemical (PEC) cell measurement

The electrical conductivity type of the CdTe thin films were tested using PEC cell measurements technique. These measurements could not be carried out with the conventional Hall Effect measurement due to the underlying FTO conducting substrate [10]. The experimental set-up to carry out this measurement had earlier been explained in section 3.5.1 of Chapter 3. The types of electrical conduction obtained in the CdTe layers are mainly determined by the polarity of the PEC signal. Figure 8.7 shows the PEC signals as a function of cathodic potentials for AD-, HT- and CC-CdTe layers. After annealing without and with $CdCl_2$ treatment, the PEC signals of n-type CdTe layers beyond 1370 mV reduce and tend towards p-region. As seen in Figure 8.7, the CdTe layers deposited at growth voltages (V_g) <1370 mV show p-type electrical conduction while the CdTe layers grown at V_g >1370 mV are n-type. Panicker et al. [2] explained that deposition at lower cathodic potential favours Te-deposition and produce Te-rich CdTe while deposition at higher cathodic potential gives rise to Cd-rich CdTe layers. Therefore, to obtain n-CdTe layers, a more negative deposition potential is required. As reported by Takahashi et al. [11], more Te is deposited when the deposition potential is more positive (that is, low cathodic potential) while more Cd is deposited when the deposition potential is more negative (that is, higher cathodic potential).

The ability of p-CdTe to convert totally or move towards n-CdTe and n-CdTe to move towards or convert totally to p-CdTe is as a result of complexities in this semiconductor material. The conversion of p-CdTe to n-CdTe may be as a result of Te vacancy (Cd-richness). The Te vacancy may arise when the CdTe layers are deposited very close to V_i point in the p-region with very low level of Te in the bath. Annealing these type of layers with $CdCl_2$ treatment can easily convert the p-CdTe to n-CdTe due to re-distribution of defects which take place during annealing [12]. Researchers have given many reasons for the type conversion of n-CdTe to p-CdTe. One of these reasons may be as a result of Cd vacancy [13–15]. In most cases, Cd vacancies are generated due to evaporation of Cd during heat-treatment. Since Cd has higher vapour pressure than Te, it sublimes first thereby leaving a Te-rich CdTe layer [16]. Aside Cd vacancy, Basol et al. [15] also showed other possibilities of n-CdTe converting to p-type. Some of the explanations given by Basol et al. [15] are: (i) activation of residual p-type dopants in the CdTe thin films (ii) diffusion of p-type dopants from the conducting substrate and annealing environment into the CdTe thin films and (iii) acceptors diffusing into the CdTe thin films from grain boundaries.

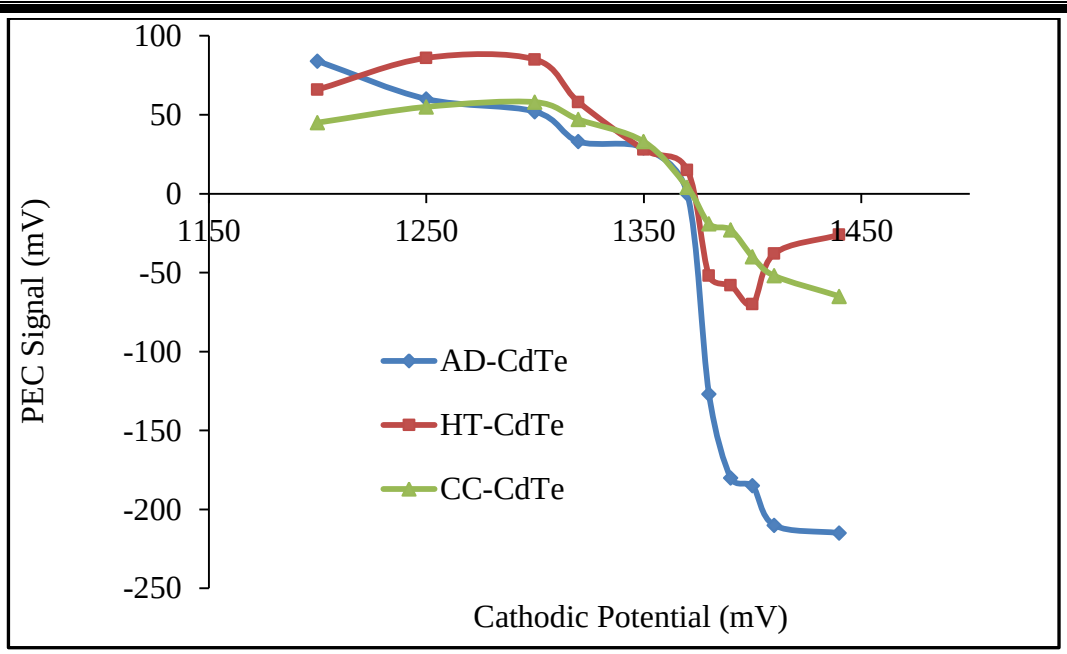


Figure 8.7. Typical variation of PEC signals with cathodic potentials for as-deposited, heat-treated and $CdCl_2$ treated CdTe layers grown from sulphate precursors.

CdMnTe, a ternary compound semiconductor was also investigated. One of the main reasons of exploring CdMnTe in this work is due to the fact that the energy bandgaps are tuneable and wider bandgaps than CdTe thin films can be obtained [17]. With the wide bandgap, it can serve the purpose of a back contact layer to CdTe thin films for barrier height enhancement. p-type CdMnTe layers can also be used as a p-type window material in graded bandgap solar cells. The effect of alloying CdTe with Mn on electrical conduction type is illustrated in Figure 8.8. After annealing ordinarily in air without $CdCl_2$ treatment, the PEC signals of all CdMnTe layers in the n-region beyond 1370 mV convert to p-type. However, since AD- and HT-materials do not have the required crystallinity for inclusion in thin film solar cells, it is therefore proper to treat the surface of the CdMnTe semiconductor materials with $CdCl_2$ before annealing so as to achieve a more crystalline material. The PEC cell results of the CC-treated CdMnTe layers show that the CdMnTe thin films grown at the Cd-rich region (for example, 1450 mV and above) still remain n-type immediately after $CdCl_2$ treatment while the PEC signals of CdMnTe layers grown very close to the inversion voltage of ~1370 mV all convert to p-type CdMnTe. This result agrees with the reports in the literature that CdMnTe layers can have both n- and p-type electrical conduction [18,19]. Based on this experimental investigation; to get p-type CdMnTe, it is proper to anneal ordinarily in air

without any chemical treatments or to grow near the inversion voltage and anneal in the presence of $CdCl_2$ atmosphere.

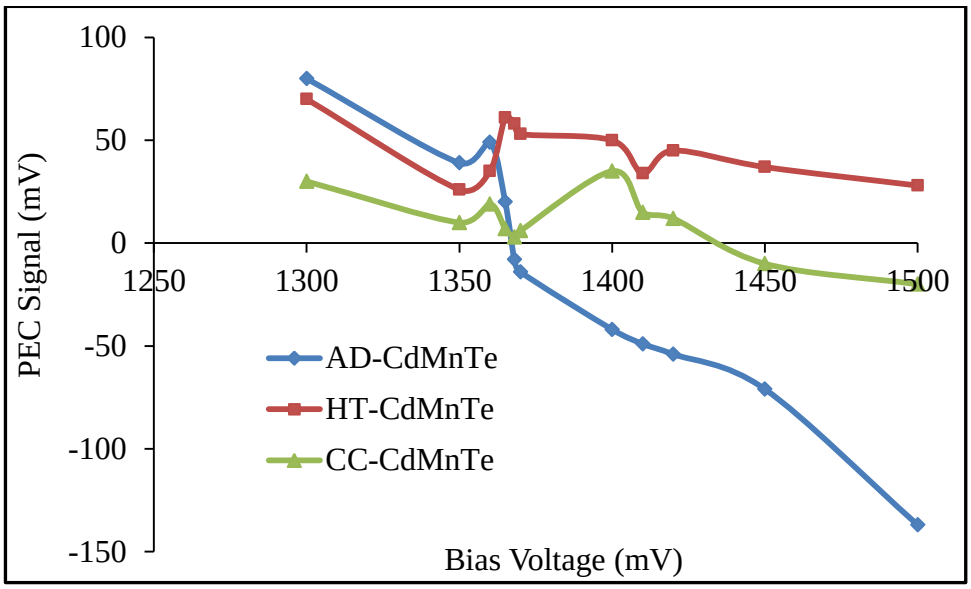


Figure 8.8. Typical variation of PEC signals with cathodic potentials for as-deposited, heat-treated and $CdCl_2$ treated CdMnTe layers.

8.3.5 Thickness Measurement

The thicknesses of CdTe layers grown at different durations were estimated theoretically using Faraday's law of electrolysis,

$$T = \frac{ItM}{nA\rho F} \tag{8.5}$$

where M is the molar mass of CdTe thin films (240.01 $gmol^{-1}$), t is the growth time in seconds, I is the average current observed during deposition in Ampere, A is the area of the electroplated layers in cm^{-2}, F is Faraday's constant (96485 $Cmol^{-1}$), ρ is the density of CdTe (5.85 gcm^{-3}) and n is the total number of electrons required in the deposition of 1 mol of CdTe (n = 6 as given by Equations (8.1), (8.2) and (8.4)).

Figure 8.9 shows how the thickness of CdTe layers grown at a V_g of 1400 mV varies with deposition time. The thickness of ED-CdTe layers increases with deposition time as seen in Figure 8.9. The theoretical estimate of the thickness does not show a perfect linear response due to the variation of deposition current density with growth time. As shown in Figure 8.9, the thickness obtained at ~4 hours of deposition time is ~1.55 μm.

The thickness of the CdTe thin films can be increased beyond 2 µm simply by increasing the deposition time.

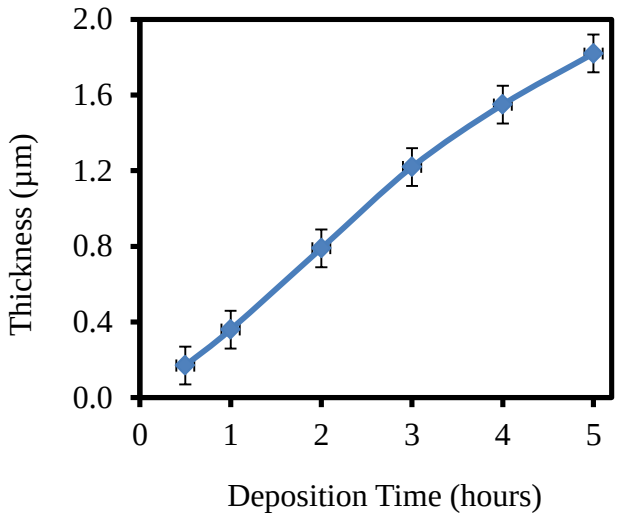


Figure 8.9. Typical theoretical thicknesses of CdTe thin films at different growth duration ranging from (0.5-5.0) hours.

8.4 Effect of annealing temperatures on electronic properties of n- and p-CdTe layers

The knowledge of electronic parameters of semiconductor materials such as the material's resistivity, conductivity, doping density and mobility are very important to help in developing electronic devices of high grade. The effects of different annealing temperatures on these electronic parameters have been investigated during this research work. The temperatures used range from (350-450)^{o}C while the annealing time was fixed for 10 minutes in air. The electrical parameters discussed in this section were obtained for p- and n-type CdTe thin films grown at different cathodic potentials of 1350 mV and 1400 mV respectively. To obtain good ohmic characteristics, the back metal contacts were carefully selected to form ohmic behaviour to the CdTe layer. Since the substrate used in this work is glass/FTO, the FTO already formed an ohmic behaviour with the CdTe because it is a conducting oxide with work function (4.40 eV) [20] higher than the CdTe electron affinity (~4.28 eV) [21]. Au and *In* metal contacts were used in making ohmic contacts to p- and n-CdTe respectively. The work function of Au and *In* metals have been reported to be ~5.25 eV [22] and ~4.09 eV respectively.

In carrying out the DC conductivity measurements, circular ohmic contacts of ~0.031 cm^2 active area were made by coating the p- and n- CdTe layer with Au and *In* metals respectively. The circular contacts of ~0.031 cm^2 active area were obtained from a metallic mask having up to 50 circular dots of 2 mm diameter. I-V characteristics of the glass/FTO/CdTe/ohmic contact structures were carried out by applying a bias voltage from -1.0 to +1.0 V. The I-V results (not shown here for brevity) show a very good linear response that passes through the origin. This signifies nearly ideal ohmic characteristics. The resistances of the metal-coated layers were estimated from the Ohm's law relationship. For each experimental set, the average resistances were determined from the measured cells. Equation (3.15) given in Chapter 3 was used in calculating the electrical resistivity while the conductivity was estimated from the inverse of resistivity values.

8.4.1 Resistivity measurements of p- and n-CdTe thin films

The resistivity values of p- and n-CdTe layers were estimated from the I-V characteristics of the linear resistors fabricated from glass/FTO/p-CdTe/Au and glass/FTO/n-CdTe/In device structures respectively. The doping densities on the other hand were obtained from the C-V characteristics of the fabricated Schottky diodes (glass/FTO/p-CdTe/Al for p-CdTe and glass/FTO/n-CdTe/Au for n-CdTe). The values of resistivities of p-CdTe and n-CdTe thin films obtained at different annealing temperatures are given in Table 8.2. The values for AD-CdTe are given as the heat temperature of 0^oC. As seen from Table 8.2, the as-deposited p-CdTe layers have the highest resistivity when compared to the HT- and CC-CdTe layers. A little decrease was observed in the resistivity of HT-CdTe layers annealed at 350 and 380^oC for 10 minutes in air. With this high resistivity, the AD p-CdTe layers and p-CdTe thin films heat-treated ordinarily in air at temperatures below 380^oC may not be suitable for direct application in thin film solar cells fabrication [16]. The high resistivity makes the p-CdTe layer to be semi-insulating. The semi-insulating property makes it suitable for use in applications such as X- ray and gamma ray detectors [23].

From Figure 8.10 (a), when compared to the initial annealing temperature of 350^oC; drastic reduction was observed in the resistivity of HT p-CdTe layers from annealing temperature of $(400\text{-}450)^oC$. This temperature range is therefore a suitable range for annealing CdTe-based device structures when used in solar cells fabrication and for achieving more crystalline CdTe layers. As revealed in Figure 8.10 (a), the effect of

$CdCl_2$ treatment on the p-CdTe layers are clearly obvious. There was a tremendous reduction in the CdTe resistivity of CC p-CdTe when compared to HT p-CdTe layers even at lower annealing temperatures. This result clearly demonstrates one of the advantages of $CdCl_2$ treatment when used in device fabrication. The reduction in CdTe series resistance was also one of the advantages highlighted by Rohatgi et al. [24] when CdTe layers are treated with $CdCl_2$ solution. Figure 8.10 (a) and 8.10 (b) show the plots of resistivity of p-CdTe and n-CdTe thin films versus annealing temperatures respectively.

Table 8.2. Room temperature (RT) resistance and resistivity values of heat-treated and $CdCl_2$-treated p- and n-CdTe layers at different annealing temperatures of (350-450) ^oC.

		RT resistance and resistivity values after heat treatment at different temperatures						
CdTe Layers		Temp., (^oC)	0	350	380	400	420	450
p-CdTe	HT p-CdTe	*R*, (Ω)	2750	2585	2491	179	133	85
		ρ,(Ω.cm)	8.64×10^5	8.12×10^5	7.83×10^5	5.62×10^4	4.19×10^4	2.67×10^4
	CC p-CdTe	*R*, (Ω)	2750	1260	700	53	33	28
		ρ,(Ω.cm)	8.64×10^5	3.96×10^5	2.20×10^5	1.65×10^4	1.05×10^4	8.71×10^3
n-CdTe	HT n-CdTe	*R*, (Ω)	67.0	38.4	36.9	26.4	33.1	103.0
		ρ,(Ω.cm)	2.11×10^4	1.21×10^4	1.16×10^4	8.29×10^3	1.04×10^4	3.24×10^4
	CC n-CdTe	*R*, (Ω)	67.0	35.9	33.5	24.3	29.9	97.3
		ρ,(Ω.cm)	2.11×10^4	1.13×10^4	1.05×10^4	7.65×10^3	9.41×10^3	3.06×10^4

One other interesting thing to observe in this result is that when the annealing temperature is ≥400^{o}C, there is a very close match between the resistivity of HT and CC p-CdTe layers. However, in all cases, the $CdCl_2$ treated p-CdTe layers showed the least resistivity. In both heat treatment conditions (HT and CC), the least resistivity for p-CdTe was obtained at annealing temperature of 450^{o}C. At 420 and 450^{o}C, the resistivity of CC-CdTe layers decreases by ~two orders of magnitude while for HT-CdTe layers, the resistivity reduced by ~one order of magnitude with respect to as-grown layers. In a similar experiment carried out by Ochoa-Landı´n et al. [25], the authors observed a very high resistivity in the order of 10^8 Ωcm for their as-grown CdTe layers and a decreased resistivity of 8.1×10^4 Ωcm after annealing p-CdTe layers with $CdCl_2$ treatment at 400^{o}C. The resistivities of n-CdTe illustrated in Figure 8.10 (b) still

indicate that the CC-CdTe layers have reduced resistivities when compared to HT-CdTe layers. However, it could be seen that the resistivity values within the explored temperature range are very close to each other. By comparing the resistivities of as-deposited p-CdTe with n-CdTe in Table 8.2, it was observed that the resistivity value of p-CdTe was ~41 times greater than that of n-CdTe.

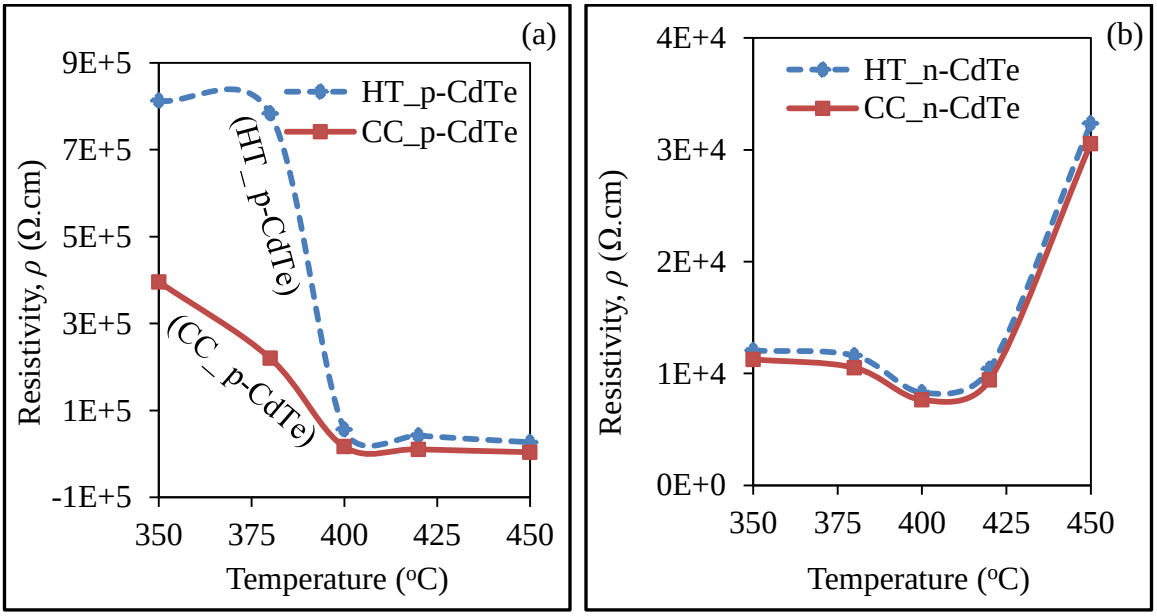


Figure 8.10. Typical resistivity of HT- and CC-treated CdTe thin films at different annealing temperatures of (350-450)^{o}C, CdTe thickness ~1000 nm for (a) p-CdTe thin films and (b) n-CdTe thin films.

8.4.2 Estimation of mobility values for p- and n-CdTe thin films

The mobility of charge carriers in p- (μ_p) and n-type (μ_n) semiconductors can be derived using Equations (8.6) and (8.7) respectively.

$$\boldsymbol{\sigma_n = nq\mu_n} \tag{8.6}$$

$$\boldsymbol{\sigma_p = pq\mu_p} \tag{8.7}$$

The two variables from Equations (8.6) and (8.7) required to estimate the mobility values are conductivity and doping density. The conductivity and doping density values were obtained from I-V and C-V measurement techniques respectively. *n* is the doping density of n-type semiconductor while *p* is the doping density of p-type semiconductor. The mobilities of n- and p- semiconductors are represented as μ_n *and* μ_p respectively. The constant *q* is the electronic charge.

Combining the electrical conductivity values measured from DC conductivity measurements and doping concentrations measured from C-V measurements, the value of mobilities were estimated for both n- and p-type CdTe layers. Results are summarised in Table 8.3.

Table 8.3. Mobility estimation of $CdCl_2$-treated n- and p-CdTe layers at different annealing temperatures of (350-450)^oC. The mobility values were obtained from I-V and C-V measurements.

	$CdCl_2$-treated n-CdTe			$CdCl_2$-treated p-CdTe		
Temperature (^oC)	σ_n $(\Omega.cm)^{-1}$	N_D-N_A (cm^{-3})	μ_n $(cm^2V^{-1}s^{-1})$	σ_p $(\Omega.cm)^{-1}$	N_A-N_D (cm^{-3})	μ_p $(cm^2V^{-1}s^{-1})$
0	4.75×10^{-5}	1.22×10^{16}	0.024	1.16×10^{-6}	4.69×10^{15}	0.002
350	8.88×10^{-5}	1.57×10^{15}	0.353	2.53×10^{-6}	3.06×10^{14}	0.052
380	9.51×10^{-5}	1.18×10^{15}	0.504	4.55×10^{-6}	1.81×10^{14}	0.157
400	1.31×10^{-4}	2.73×10^{13}	29.936	6.06×10^{-5}	3.00×10^{13}	12.630
420	1.06×10^{-4}	9.64×10^{13}	6.887	9.55×10^{-5}	1.75×10^{13}	34.114
450	3.27×10^{-5}	1.34×10^{16}	0.015	1.15×10^{-4}	1.71×10^{13}	97.835

Figure 8.11 illustrates the variation of mobility of n- and p-CdTe thin films at different annealing temperatures of (350-450)^oC. Up to the annealing temperature of 400^oC (Figure 8.11), n-CdTe shows higher mobility than p-CdTe. The higher mobility values observed in n-CdTe may be due to their lower resistivities. The more resistive a semiconductor material is, the less will be the speed at which the charge carrier moves. For this cause, the drift velocities of electrons are always higher than that of holes. The higher mobility values observed in n-CdTe may also be explained in terms of the effective mass of the charge carriers since the effective mass in hole is heavier than that of electrons in CdTe [26]. As explained by Sze and Ng, mobility increases with decrease in effective mass and increase in temperature. The increased temperature and minimal value of effective mass impact high thermal velocity to the charge carriers and this makes them to be less deflected by Coulomb scattering [27].

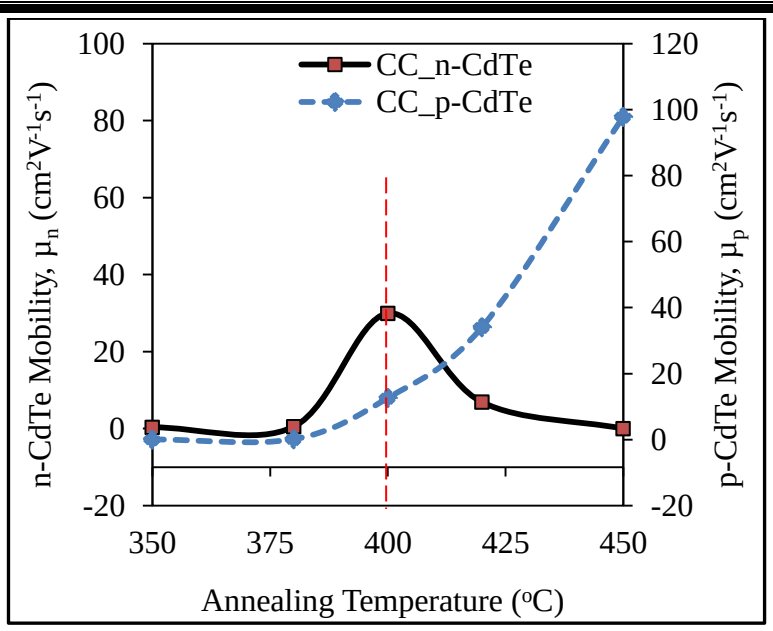


Figure 8.11. Mobility of n- and p-CdTe thin films at different annealing temperatures in the range (350-450)^{o}C.

A diminishing trend was however observed in the mobility of n-CdTe as the annealing temperature goes beyond 400^{o}C while for p-CdTe, mobility increases as the annealing temperature increases up to 450^{o}C as illustrated in Figure 8.11. Due to this discrepancy, the n-CdTe cannot be compared with p-CdTe beyond 400^{o}C. The decrease in the mobility of n-CdTe at higher annealing temperatures may be due to material sublimation since the CdTe layer used for this experiment is ~1.0 μm. Also, the vapour pressure of Cd and Te element can also be a contributing factor to the sublimation of n-CdTe layer. It should be recalled that n-type CdTe thin films are Cd-rich while p-type CdTe layers are Te-rich [10]. By considering the vapour pressure of the constituents which make up the CdTe thin films, the vapour pressure of Cd is higher than that of Te in the CdTe composition [28]. Due to this, there is the possibility of Cd in the n-CdTe which is Cd-rich to easily sublime during heat-treatment; this is because semiconductor materials with higher vapour pressure evaporates faster when compared with ones of lesser vapour pressure [16,28]. The loss of Cd from the CdTe thin films introduces Cd-vacancies and Te richness related defects into the thin films and this makes the layer to deviate from stoichiometry [28]. These experimental investigations revealed that the electronic behaviour of CdTe thin films is influenced by their electrical conductivity type. The result presented in Figure 8.11 further demonstrates that annealing temperatures of 400^{o}C and 450^{o}C may be ideal for heat-treating n-CdTe and p-CdTe thin films respectively.

It should be noted that the above mobility values are for electrical conduction normal to the FTO surface $(\mu_{\perp})$. Conventional Hall Effect measurements estimate the mobility parallel to FTO surface $(\mu_{//})$ and these two mobility values can be very different due to scattering from grain boundaries. The hole mobilities of CdTe layers reported by Miyake et al. [29] from Hall Effect are much smaller than the values estimated in this work.

8.5 Effect of chemical treatments on CdTe thin films

The possibility of Te precipitation in CdTe thin films exist due to easy electrodeposition of Te. The Te precipitation is usually detrimental to optoelectronic device performance [30,31]. It is therefore of paramount interest to eliminate these Te precipitates. One possible way of doing this is by applying chemical treatments to the top surface of the CdTe thin films [32]. This section discusses what happens to the material and opto-electronic properties of CdTe thin films after the application of chemical treatments to the CdTe top surface. The chemical treatments used in this section are $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$ solutions. The reason for the incorporation of $GaCl_3$ into $CdCl_2$ solution for surface treatment is due to the ability of Ga to remove Te precipitates [33]. Te precipitates contribute to the recombination and generation of photo-generated charge carriers in the CdTe-based device structures. The experimental work reported by Sochinskii et al. [34] showed that the dissolution of Te precipitates in CdTe single crystals can be achieved by annealing the crystals in Ga melt. Since the midgap defects known as killer centres in CdTe thin films originate from Te-richness [35], finding a possible means of reducing these defects to the barest minimum would cause the efficiency of the CdTe-based solar cell device structures to further improve.

The application of $CdCl_2$ as chemical treatment to the top surface of CdTe thin films before annealing have been known to offer numerous advantages such as: improvement in the material crystallinity, formation of larger grains and passivation of grain boundaries, lattice mismatch reduction between the CdS and CdTe hetero-partner, improvement of the alloying between CdS/CdTe interface, reduction of series resistance and removal of some unwanted sources of defects such as Te precipitates [24,36–38]. Therefore, since Ga which is a shallow donor in the Cd sites of CdTe thin films [33] has the potential of removing these Te precipitates and doping the material n-type; the incorporation of $GaCl_3$ into the universal $CdCl_2$ treatment has therefore been explored

in this work to be used as means of surface treatment to improve the efficiency of CdTe-based solar cells. This idea comes from the knowledge exhibited by researchers working on $X-$ and $\gamma-$ ray detector systems. It is expected that the complementary efforts of the three ions namely Ga^{3+}, Cd^{2+} and Cl^{-} in the $GaCl_3$+$CdCl_2$ solution would be more effective to combat Te precipitates and improve material quality.

8.5.1 Effect of chemical treatments on CdTe structural properties

To investigate the effect of chemical treatments on structural properties of CdTe thin films, X-ray diffraction (XRD) and Raman analytical techniques were used.

8.5.1.1 X-ray diffraction study

The XRD spectra of CdTe thin films grown for ~1.00 hour on glass/FTO substrates are shown in Figure 8.12. This study was carried out on as-deposited CdTe (AD-CdTe), CdTe annealed without any chemical treatments (HT-CdTe), CdTe treated with $CdCl_2$ solution only before annealing (CC-CdTe) and CdTe treated with mixture of $GaCl_3$+$CdCl_2$ solution before annealing (GC+CC-CdTe). The heat-treatment was carried out at 400^{o}C for duration of 10 minutes in air. The HT-CdTe serves as the baseline to identify the significant effects of chemically treating the top surface of the CdTe layers before annealing. As seen in Figure 8.12, the three CdTe spectra exhibit the prominent CdTe peak at 2θ within the range 23.75^{o} to 24.05^{o} along the (111) plane. The XRD peak along the (111) plane can therefore be referred to as the peak with most preferred orientation due to its highest intensity along this plane.

The XRD spectra shown in Figure 8.12 did not indicate the presence of any elemental hexagonal Te/Cd peaks or monoclinic Cd_xTeO_y peaks; however, the presence of hexagonal CdTe peak was observed in AD- and HT-CdTe layers. As explained by Dharmadasa [12], Te-related XRD peaks (such as E(Te) and Cd_xTeO_y) may be caused by Te precipitation which occurs as a result of local crystallisation. However, the presence of these excess Te may not be revealed by XRD if the excess Te is equally distributed in the CdTe thin film in amorphous phase [12]. Since elemental Te has hexagonal crystal phase and is mostly prominent in AD- and HT-CdTe thin films as seen in Raman spectra illustrated in Figure 8.14, the formation of hexagonal CdTe as observed in XRD spectra of AD- and HT-CdTe thin films (Figure 8.12) may likely be attributed to reaction between excess E(Te) and excess E(Cd) thereby producing hexagonal CdTe.

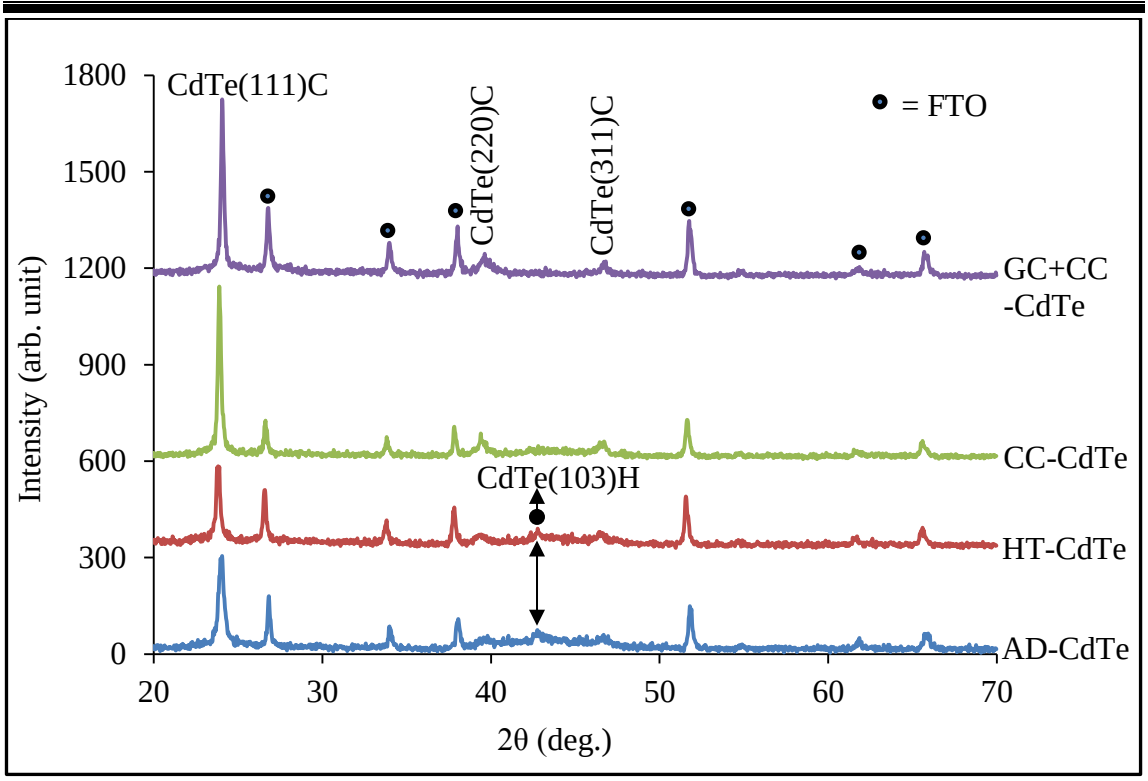


Figure 8.12. Typical XRD spectra of as-deposited CdTe thin films, CdTe thin films annealed without any chemical treatments and CdTe thin films chemically treated in the presence of $CdCl_2$ solution only and mixture of $GaCl_3$+$CdCl_2$ solution.

As illustrated in Figure 8.12, the XRD spectra of AD-CdTe and HT-CdTe thin films show the presence of both cubic and hexagonal crystal phase. The presence of mixed phases in CdTe may not be helpful when used in solar cells device fabrication. These mixed phases (cubic/hexagonal) depend on the substrate condition such as growth temperature, stirring rate and pH of the electrolyte. In a thin film layer where there are multi-phases, the material crystallinity suffers. This probably explains one of the reasons why as-deposited CdTe and annealed CdTe in the absence of appropriate chemical treatments show very poor performance in terms of device efficiency [16]. After heat-treatment using chemicals like $CdCl_2$, the unstable hexagonal phase disappears thereby leaving behind the only stable cubic phase(s). As seen from Figure 8.12, the $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$ treatments used in this work removed the low intensity peak corresponding to the unstable wurtzite phase.

Figure 8.12 also shows the presence of other two cubic peaks with low intensities along (220) and (311) planes. As illustrated in Figure 8.12, CdTe thin films treated with a mixture of $GaCl_3$ and $CdCl_2$ have the highest peak intensity along (111) plane when compared to the other three XRD spectra. A plot of the (111), (220) and (311) peak

intensities versus the sample treatment conditions is shown in Figure 8.13 to further demonstrate the significant contributions made by Ga addition into $CdCl_2$ solution. The high (111) peak intensity in GC+CC-CdTe is an indication of improved and higher crystallinity as compared to CC-CdTe and HT-CdTe thin films. It is a well-established fact in the literature that post deposition treatments using $CdCl_2$ solution improves the crystallinity of CdTe layers [10,39]. This present investigation shows that the crystallinity of CdTe thin films can further be enhanced via a mixture of $GaCl_3$+$CdCl_2$ treatment solution.

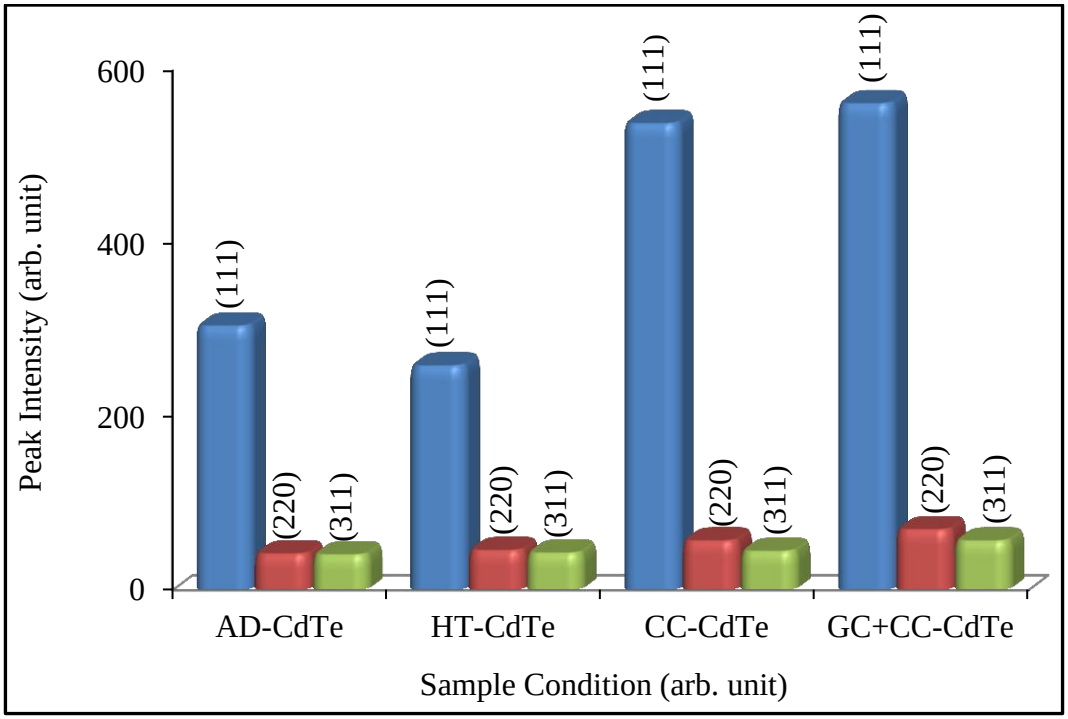


Figure 8.13. Variation of three main peaks intensities versus different post growth conditions for CdTe thin films.

A sudden orientation change in CdTe thin films has recently been identified [10]. When heat-treated at 385±5^{o}C, the grain boundaries melt and the randomisation of grains take place. At this point, intensity of (111) plane collapses and (220) and (311) peak intensities increase. However, further increase in temperature with $CdCl_2$ again increase (111) peak intensity; this trend has clearly been achieved in CC-CdTe samples. It is really interesting to observe further increase in (111) peaks for GC+CC-CdTe. This shows that CdTe layers improve much better in the presence of $GaCl_3$ and $CdCl_2$. Therefore, the device performance should improve with Ga addition. In this particular experiment, it is also possible that the grain boundary melting has not occurred due to

the narrow temperature difference between 385±5 and 400^{o}C. However, increase in (111) peak intensity is a good sign of material improvement.

The positions of angle 2θ and observed d-spacing values of the four CdTe spectra closely match the reported values in the JCPDS reference file stated in Table 8.4. Other parameters extracted from XRD measurements such as the FWHM, plane of orientation and CdTe phase are also included in Table 8.4. The crystallite sizes for each CdTe treatment conditions were estimated using Scherrer's equation given in Chapter 3. As summarised in Table 8.4, the smallest crystallites were seen in AD-CdTe thin films while the chemically treated CdTe thin films have the largest crystallites.

Table 8.4. Summary of XRD analyses of AD-, HT-, CC- and GC+CC-CdTe thin films along the various orientation planes.

Sample	Angle (2θ) (Deg.)	Counts (a.u.)	d-spacing (Å)	FWHM (Degrees)	Crystallite Size, D (nm)	Plane (hkl)	Formula/ Phase	Ref Code Matching
AD-CdTe	24.04	305	3.70	0.292	**29.1**	(111)	CdTe/Cubic	01-075-2086
	39.50	42	2.27	0.779	11.3	(220)	CdTe/Cubic	01-075-2086
	42.89	59	2.11	0.779	11.5	(103)	CdTe/Hex	00-019-0193
	46.58	41	1.95	0.779	11.6	(311)	CdTe/Cubic	00-015-0770
HT-CdTe	23.75	259	3.74	0.227	**37.3**	(111)	CdTe/Cubic	00-015-0770
	39.30	46	2.29	0.520	17.0	(220)	CdTe/Cubic	00-015-0770
	42.76	65	2.11	0.779	11.5	(103)	CdTe/Hex	00-019-0193
	46.50	43	1.95	0.390	23.2	(311)	CdTe/Cubic	00-015-0770
CC-CdTe	23.89	539	3.73	0.162	**52.3**	(111)	CdTe/Cubic	00-015-0770
	39.48	57	2.28	0.260	17.0	(220)	CdTe/Cubic	00-015-0770
	46.66	45	1.95	0.520	17.4	(311)	CdTe/Cubic	00-015-0770
GC+CC-CdTe	24.05	562	3.70	0.162	**52.3**	(111)	CdTe/Cubic	01-075-2086
	39.57	70	2.28	0.520	17.0	(220)	CdTe/Cubic	01-075-2086
	46.72	57	1.94	0.390	23.2	(311)	CdTe/Cubic	01-075-2086

8.5.1.2 Raman spectroscopy study

Apart from using XRD to identify given semiconductor phases, Raman spectroscopy is another quick technique that can equally be used to determine structural properties and identify phases present in a material. A Renishaw Raman microscope with 514 nm argon ion laser source was used in this work to obtain Raman spectra for CdTe thin films under different heat-treatment conditions. Extended spectrum for the CdTe thin films were collected at room temperature using a 100% laser power (~30 mW) and 50X

objective in the Raman microscope for 60 seconds. Overall, five Raman peaks which can be grouped into three different categories are identified in Figure 8.14.

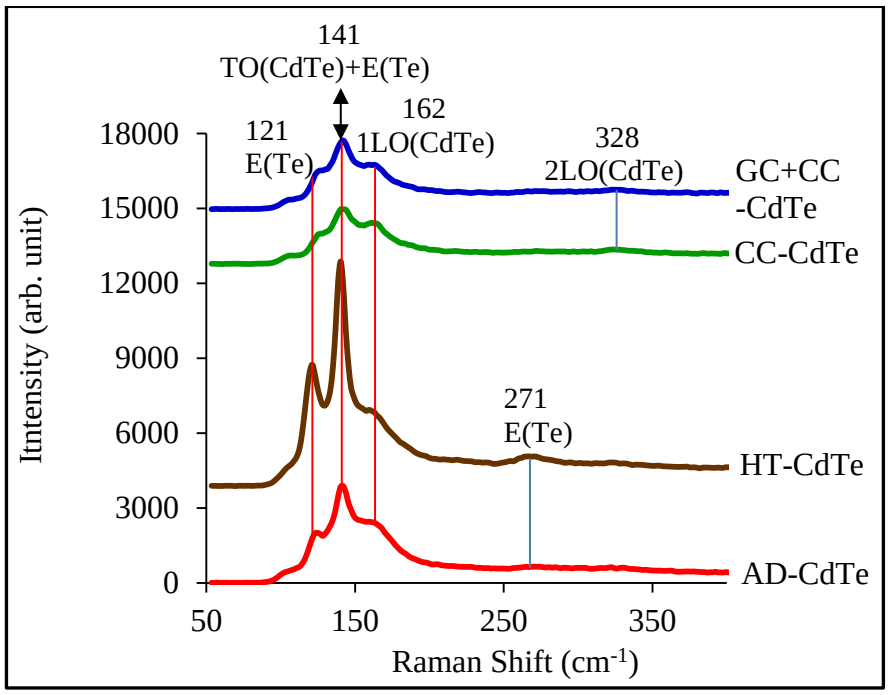


Figure 8.14. Raman spectra obtained for AD-, HT-, CC- and GC+CC-CdTe layers. Note the reduction of elemental Te peak at 121 cm^{-1} and enhancement of 1LO CdTe peak at 162 cm^{-1} after $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$ surface treatments.

The first category consists of two peaks occurring at 121 cm^{-1} and 271 cm^{-1} and they arise as a result of vibrations from elemental Te, {E(Te)}. The second category comprises of two phonon modes at 162 cm^{-1} and 328 cm^{-1} and they correspond to vibrations from CdTe thin films; these two Raman peaks are called the first order longitudinal optics (1LO) and second order longitudinal optics (2LO). These two different categories show the existence of two individual separate phases belonging to E(Te) and CdTe. The third category is a combined peak due to overlap of E(Te) and TO(CdTe). As illustrated in Figure 8.14, the first peak was obtained at wave numbers 121 cm^{-1}. This peak which corresponds to E(Te) is most prominent in the CdTe samples annealed ordinarily with no chemical treatments. The AD-CdTe also shows this E(Te) peak but with a reduced intensity. By looking at these two spectra, annealing in air with no adequate chemical treatments led to the crystallisation of this elemental Te at Raman position 121 cm^{-1}. It could also be observed that the elemental Te peak corresponding to 121 cm^{-1} has almost disappeared when chemically treated with $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$ aqueous solutions.

Another peak corresponding to E(Te) also arise at Raman shift 271 cm^{-1} in both AD- and HT-CdTe layers. Even though this peak has a very small intensity and not very obvious, its presence shows the un-suitability of these two types of materials for device fabrication because of the defects being introduced by Te precipitates [35]. This peak is however not seen in the CC- and GC+CC- treated CdTe films. Instead, another phonon mode of low peak intensity that corresponds to second longitudinal optics of CdTe appeared at wave numbers 328 cm^{-1}. The emergence of the 2LO CdTe phonon mode shows one of the improvements brought by CC- and GC+CC chemical treatments. Also, the Raman peak intensities of the 1LO(CdTe) improved via the $CdCl_2$ and $GaCl_3$+$CdCl_2$ treatment. The intensity of Raman peak at 141 cm^{-1} which corresponds to both E(Te) + TO(CdTe) is also more pronounced in AD- and HT- CdTe thin films. After applying CC- and GC+CC chemical treatments, the peak intensity of this mixed phase reduced drastically. This is another possible way through which the chemical treatments used in this experimental work minimise likely defects that can arise from Te precipitates.

8.5.2 Effect of chemical treatments on CdTe optical properties

The effect of different treatment conditions was also studied on the optical properties of CdTe thin films. For the optical study, the graph of absorbance square versus the photon energy is shown in Figure 8.15 while the diagram in the inset of Figure 8.15 shows the bar chart representation of how the bandgap changes with un-treated and treated CdTe thin films. Figure 8.15 shows the optical absorption curves for as-grown CdTe thin films, CdTe films annealed in air without and with different chemical treatments. It can be seen that heat treatment affects the energy bandgap of the material. As reported by Dharmadasa et al. [10], energy bandgap is useful to design and develop PV devices to harvest photons effectively and achieve better performance.

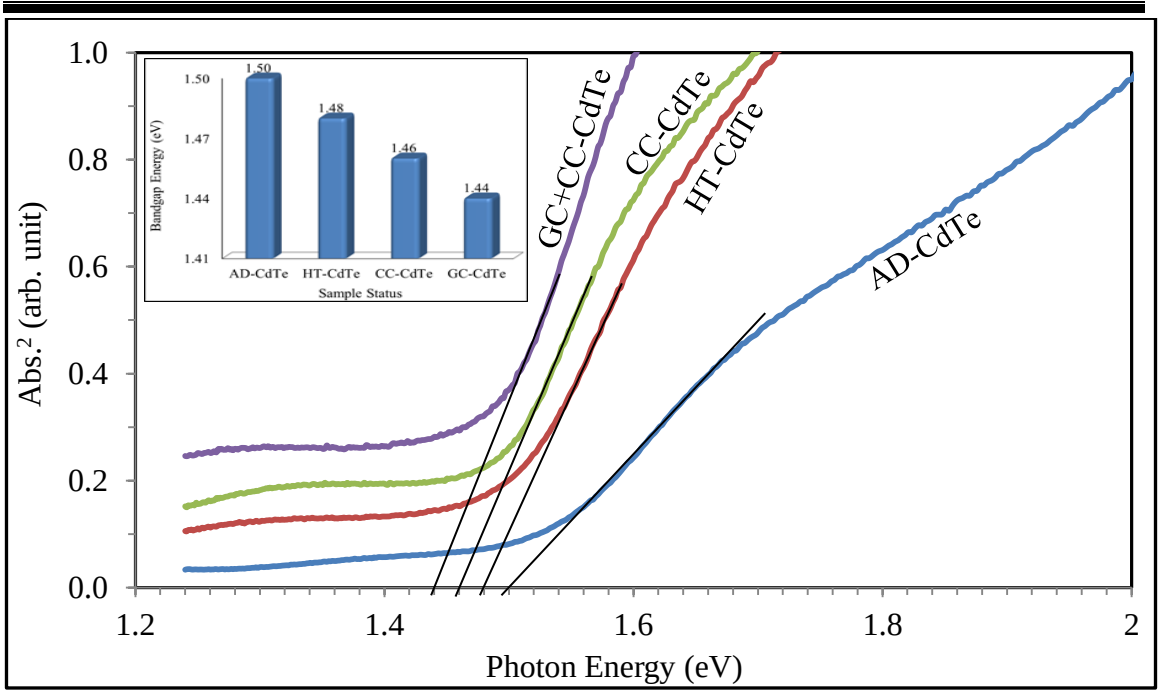


Figure 8.15. Optical absorption analysis of as-deposited CdTe (AD-CdTe) thin films, heat-treated CdTe (HT-CdTe) thin films, CdTe layers annealed in the presence of $CdCl_2$ (CC-CdTe) solution only and in the presence of mixture of $GaCl_3$ and $CdCl_2$ (GC+CC-CdTe) solution.

Researchers have reported the energy bandgap of CdTe thin films to be in the range 1.44-1.50 eV [40,41]. This range of values has also been obtained in this experimental work. The estimated energy bandgap of the as-deposited CdTe material was ~1.50 eV and this value decreases to ~1.48 eV after annealing ordinarily in air with no chemical treatments. Annealing in the presence of $CdCl_2$ (CC) and mixture of $GaCl_3$+$CdCl_2$ (GC+CC) further reduces the bandgap to 1.46 and 1.44 eV respectively. As stated by Redwan et al. [39], the reduction in energy bandgap after annealing with or without $CdCl_2$ treatment is an indication of improvement of crystallinity in the thin film. Thus, the energy bandgap reduction observed in this work after annealing CdTe thin films with and without chemical treatments reveal that the crystallinity of the materials was enhanced after heat-treatment in air. The energy bandgap obtained in this work for CdTe layers annealed with a mixture of $GaCl_3$+$CdCl_2$ corresponds to the bandgap of bulk CdTe layers. By visually observing the spectra in Figure 8.15, the optical absorption spectrum labelled GC+CC is the most absorbing spectrum and it has sharper absorption edges than the AD, HT and CC-CdTe thin films.

To further determine which of the CdTe post deposition treatment conditions give the highest absorption edge, the slope of each of the spectrum in Figure 8.15 was determined. The result obtained from the absorption edge slope was plotted as a function of the four different post deposition treatment conditions and the results are shown in Figure 8.16. In Figure 8.16, the plot of energy bandgap versus post deposition treatments was shown on the same graph with absorption edge slope for comparison purpose and to deduce the relationship between absorption edge and energy bandgap (E_g). The result in Figure 8.16 shows that GC+CC- treated CdTe thin films with the least E_g has the highest absorption edge slope while AD-CdTe thin films with the highest E_g has the least absorption edge slope. As seen from Figure 8.16, the relationship between E_g and absorption edge slope is therefore an inverse type. As explained by Han et al. [42], semiconductor materials with sharper absorption edge will have lesser impurity energy levels and defects in the thin film. The explanation given by Han et al. [42] demonstrates the possibility of GC+CC-treated CdTe layers to have lesser defects.

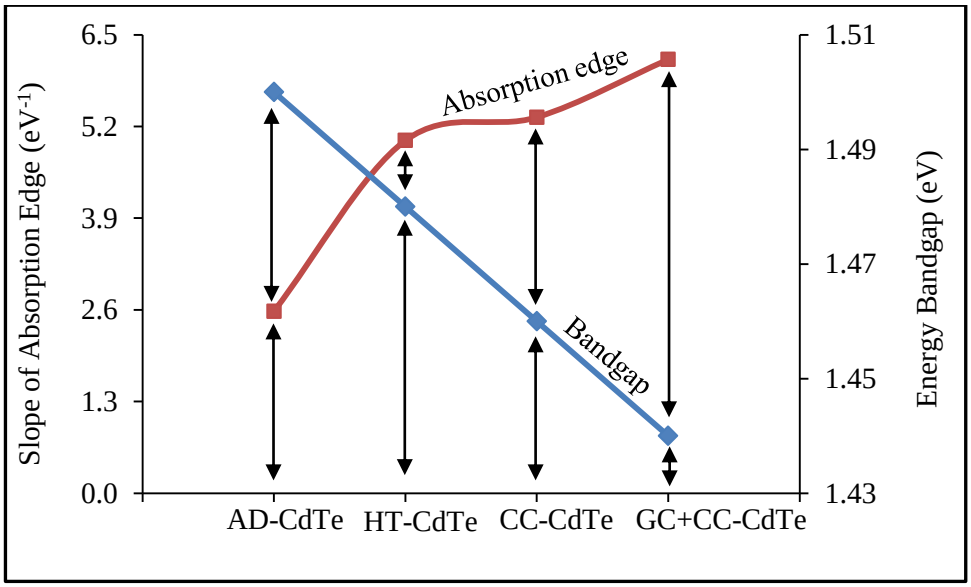


Figure 8.16. Typical diagram illustrating the relationship between absorption edge slope and energy bandgap for AD-, HT-, CC- and GC+CC-CdTe thin films.

Another advantage of having a sharp absorption edge is that it allows more photons to be absorbed even when the CdTe thickness is of few microns [43]. This optical result therefore shows the possibility of having better solar cell efficiency if mixtures of $GaCl_3$ and $CdCl_2$ solutions are used in treating solar cell device structures. The larger bandgaps recorded in AD-CdTe thin films could arise as a result of quantum effects

caused by presence of crystallites less than 10 nm in the material [44,45] while the small slope of absorption edge can be due to presence of large defects in the as-deposited materials thus making them unsuitable for solar cells fabrication in its present form [42]. Any gaps between grains also allow passage of all photons producing a larger bandgap value for AD-CdTe.

8.5.3 Effect on morphological properties

Apart from changing the structural and optical properties of the CdTe thin film materials, chemical solutions when applied to the CdTe top surface also cause a tremendous change in the morphological properties as observed in this work. SEM technique was used in studying how the material morphology changes with different chemical treatments. The CdTe SEM micrographs obtained for AD-CdTe, HT-CdTe, CC-CdTe and GC+CC-CdTe layers are shown in Figure 8.17 (a), 8.17 (b), 8.17 (c) and 8.17 (d) respectively. An increase in the grain sizes was observed after applying the different chemical treatments. The diverse effects of $CdCl_2$ treatment on grain sizes of CdTe thin films have been well researched and reported in the literature [36,46]. Small crystallites as seen in AD-CdTe (Figure 8.17 (a)) coalesce together to form larger crystals after applying $CdCl_2$ treatment (Figure 8.17 (c)); this shows that Cl when present in the material acts as fluxing agent and contributes to the process of grain growth [12].

The development of smaller grains into larger ones reduces the total number of grain boundaries and decreases the surface to volume ratio. Grain boundaries when present in large quantities within the material lead to scattering of charge carriers and these facilitate the R&G process within the bulk of the material [47]. The presence of R&G in the material leads to poor device performance. Apart from causing an improvement in the grain size, $CdCl_2$ treatment followed by annealing in an atmosphere that contains oxygen also helps in passivating the grain boundaries [47]. As reported by Dharmadasa [12], the presence of Cd in the $CdCl_2$ also converts excess Te into CdTe thereby improving the stoichiometry of the layers.

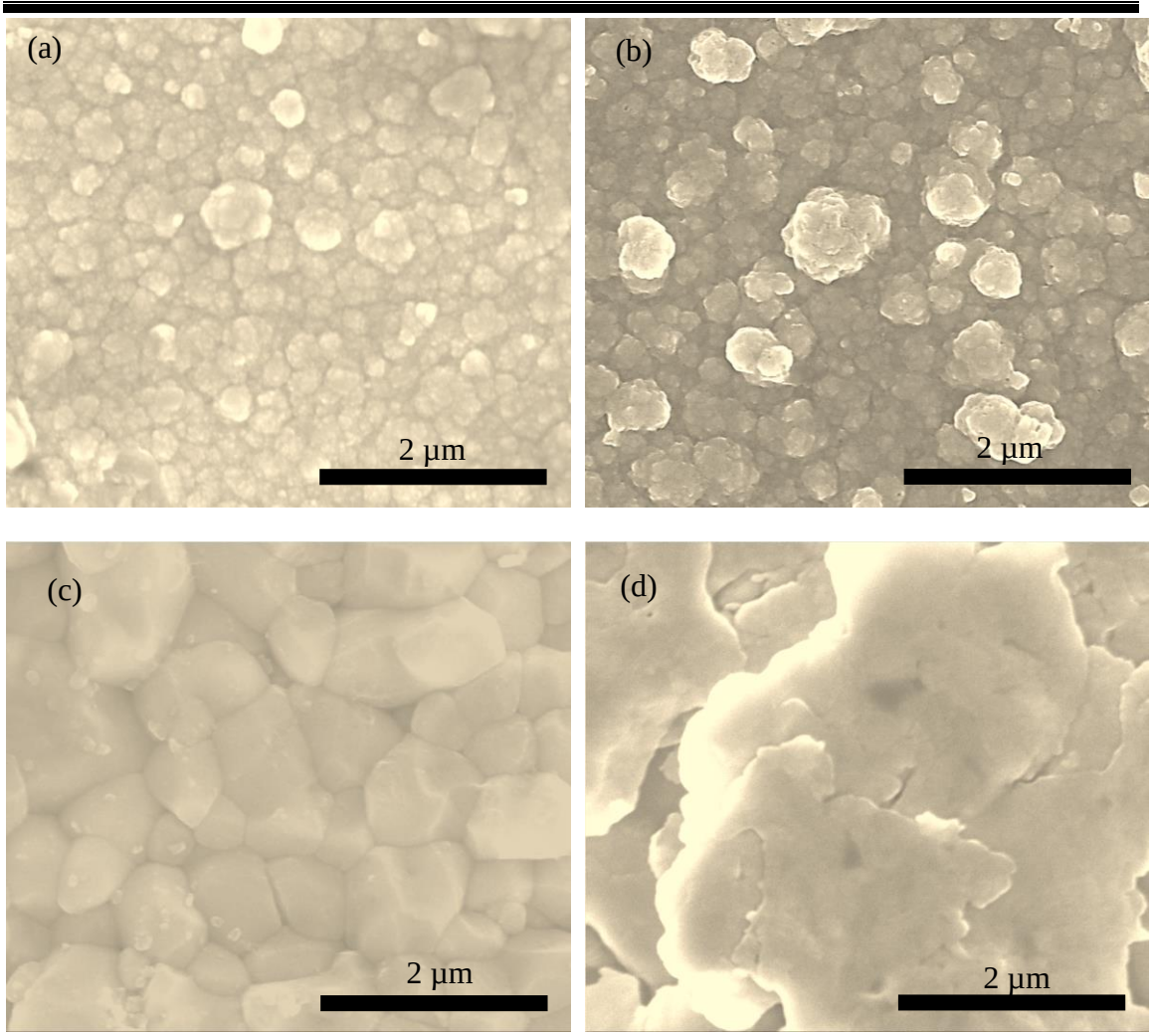


Figure 8.17. SEM micrographs of (a) AD-CdTe layers, (b) HT-CdTe layers, (c) CC-CdTe layers and (d) GC+CC-CdTe layers.

As seen in Figure 8.17 (d), the inclusion of $GaCl_3$ in the $CdCl_2$ chemical treatment further enhances the grain growth as compared to $CdCl_2$ treated layers only. Under these circumstances, three atoms namely Cd, Cl and Ga are involved. Therefore, apart from the useful contributions made by Cd and Cl to improve the material, Ga also has the ability to remove Te precipitates when used in CdTe or binary compound semiconductor materials containing Te atoms [34]. This therefore suggests the cause for having larger grains in the mixture of $GaCl_3$+$CdCl_2$ treated CdTe layers. It seems that wetting property or fluxing nature increase by adding Ga into this post treatment and annealing process. These experimental results further illustrate the possibility of having solar cell devices with improved efficiency when treated with $GaCl_3$+$CdCl_2$. The effect of this treatment is elaborated more in Chapter 9.

8.5.4 Effect on compositional properties

The atomic compositions of the chemically treated CdTe thin films were determined quantitatively using energy-dispersive X-ray analysis (EDX) technique. Figure 8.18 (a to d) show the EDX spectra obtained for the un-treated and chemically-treated CdTe layers while Table 8.5 shows the % atomic composition of elements present, and the corresponding conductivity type as observed from PEC cell measurements.

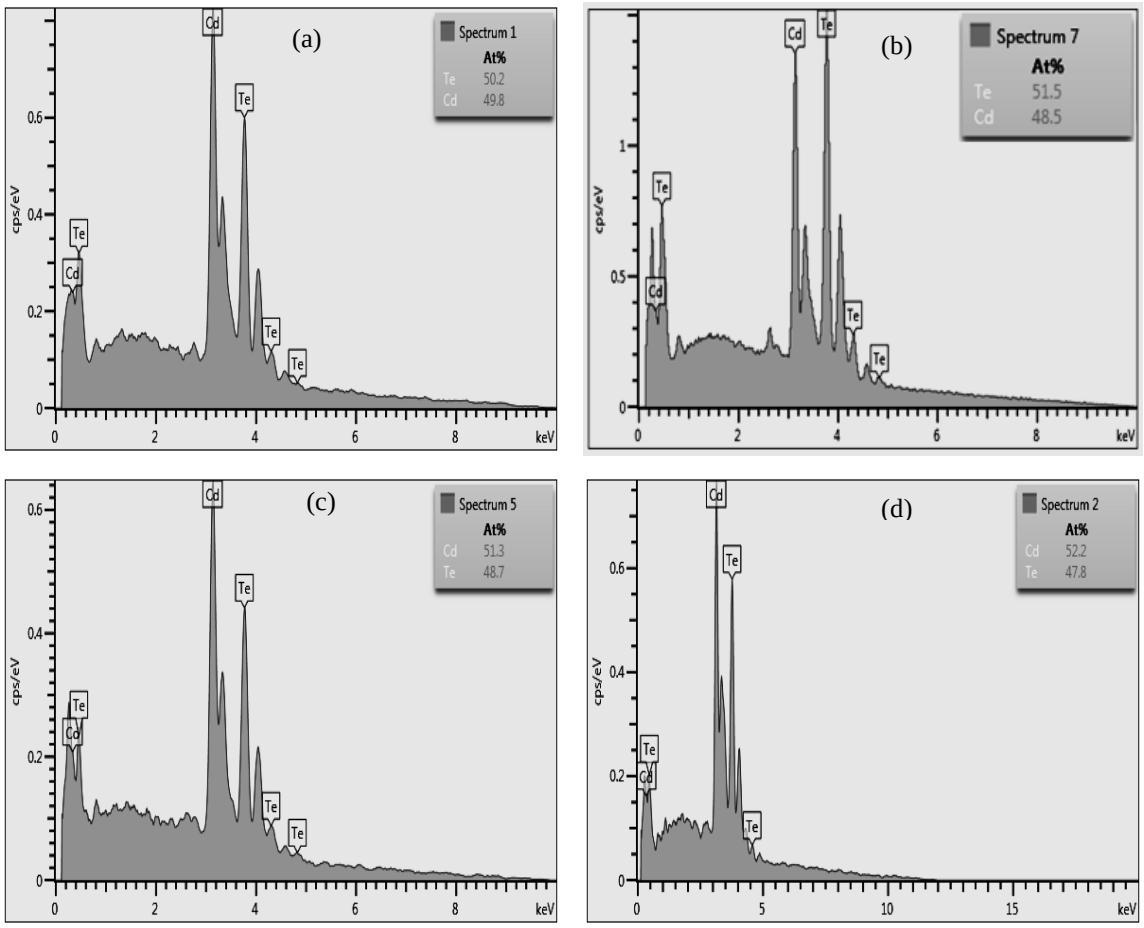


Figure 8.18. The EDX spectra of (a) As-deposited CdTe thin films, CdTe thin films annealed (b) without any chemical treatments, (c) with $CdCl_2$ and (d) with mixture of $GaCl_3$+$CdCl_2$.

The initial electrical conductivity type for the as-grown CdTe layer used in this investigation was found to be n-type using PEC cell measurement technique. After annealing ordinarily in air, the PEC signal converts to p-type but remains n-type for the chemically treated CdTe layers. Depending on the addition of external dopants and material atomic composition, CdTe as a semiconductor material can have p-, i- or n-electrical conductivity type [48–52]. The first p- and n- electrical conduction type for CdTe was achieved via the incorporation of external impurities by Jenny et al. [48]. The

experimental work carried out by Kruger et al. [49] showed that n- and p- type CdTe thin films can be achieved by changing the Cd/Te stoichiometry. Cd-rich CdTe layers give n-type while Te-rich CdTe layers produce p-type material.

Table 8.5. Comparison of the % atomic composition of Cd and Te in the un-treated and chemically-treated CdTe layers with their measured PEC cell signals.

	% Atomic Composition		Electrical Conductivity type (from PEC cell measurements)
Sample Condition	Cd	Te	
AD-CdTe	50.2	49.8	n
HT-CdTe	48.5	51.5	p
CC-CdTe	51.3	48.7	n
GC+CC-CdTe	52.2	47.8	n

From Table 8.5, the % atomic composition of Cd in as-deposited and chemically treated CdTe layers are higher than the % atomic composition of Te while for CdTe layers annealed ordinarily in air, the % of Te atom is higher than that of Cd. When this result is compared with the corresponding PEC cell measurements in Table 8.5, it was also observed that the CdTe layers with higher % of Cd atoms than Te are n-type in electrical conduction while CdTe layer with higher % of Te atom than Cd is p-type in electrical conduction. This experimental result is therefore in good agreement with the work published by Kruger et al. [49] that Cd- rich and Te- rich CdTe layers yield n- and p-type electrical conductivity respectively. The effect of Te precipitation removal can be seen in further reduction of % composition of Te atoms when mixture of $GaCl_3$+$CdCl_2$ solution was used as surface treatment for CdTe thin films. The $GaCl_3$+$CdCl_2$-treated CdTe layers show the highest % of Cd atoms as revealed in Table 8.5.

Other experiments were also carried out which demonstrate how Ga addition reduces the Te contents in the CdTe layer and bring the material into stoichiometry. A typical example of this is shown in Table 8.6. In this second scenerio, the initial starting material is Te-rich. It was noticed that after $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$ treatment, the % composition of Cd atoms increase while that of Te reduces. As seen in Table 8.6, Ga addition reduces the Te contents in the CdTe layer and bring the material into stoichiometry. In both cases, either the initial starting material is Cd-rich or Te-rich, the common trend is that after $GaCl_3$+$CdCl_2$ treatment, the atomic % of Te reduces. These experimental investigations further illusrate how Ga addition reduces Te

precipitates in the CdTe material. A typical EDX spectrum illustrating how mixture of $GaCl_3$+$CdCl_2$ bring the CdTe material close to stochiometry is shown in Figure 8.19.

Table 8.6. % atomic composition of Cd and Te in the un-treated and chemically-treated CdTe layers.

	% Atomic Composition	
Sample Condition	Cd	Te
AD-CdTe	43.9	56.1
CC-CdTe	49.3	50.7
GC+CC-CdTe	50.0	50.0

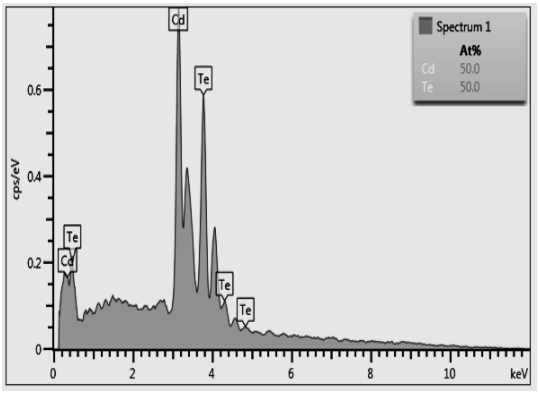


Figure 8.19. The EDX spectra of CdTe thin films treated with mixture of $GaCl_3$+$CdCl_2$ solution.

8.5.5 Effect on electrical properties

The experimental investigations carried out by Khallaf et al. [53] on undoped and Ga-doped CdS thin films showed that the resistivity of undoped-CdS thin films is higher than those of CdS layers doped with Ga. Their work showed that incorporation of Ga into the CdS bath is an effective way of lowering the thin film resistivity. In this work, CdTe bath was not doped with Ga; rather, Ga salt was applied in conjunction with $CdCl_2$ as chemicals to treat the surface of the CdTe thin films. This section describes the effect of different chemical treatments on the electrical properties of p-CdTe thin films with emphasis on $GaCl_3$ inclusion in $CdCl_2$. Both ohmic and Schottky behaviours were studied using glass/FTO/p-CdTe/Au and glass/FTO/p-CdTe/Al respectively. The resistivity values were estimated from the I-V characteristics of glass/FTO/p-CdTe/Au device structures while the doping densities were obtained from the C-V characteristics of Schottky diodes fabricated from glass/FTO/p-CdTe/Al.

Typical Mott-Schottky plots of AD-CdTe and GC+CC-treated CdTe layers used in estimating the doping density values are shown in Figure 8.20 (a) and 8.20 (b) respectively.

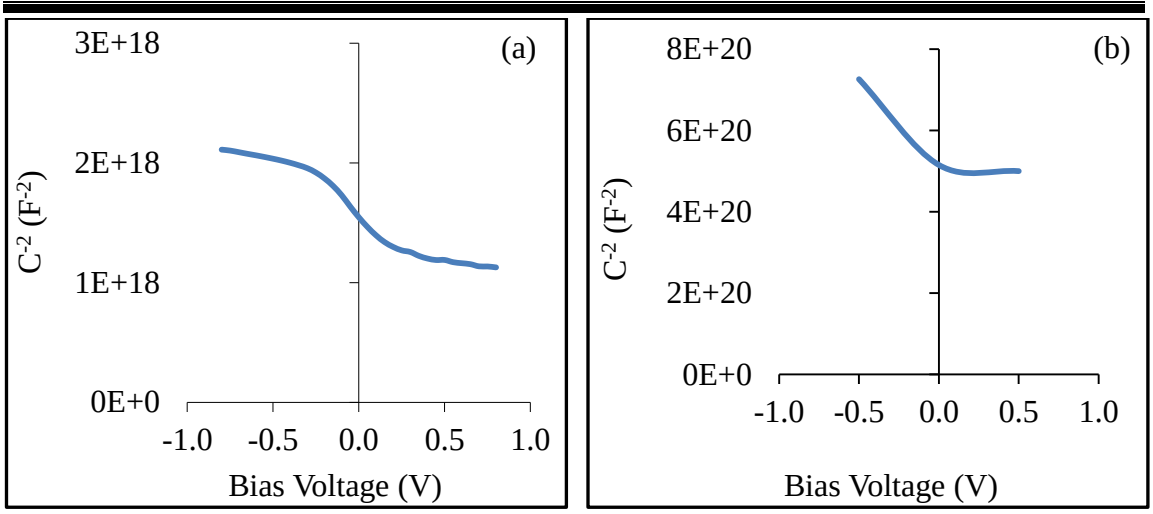


Figure 8.20. Typical Mott-Schottky plots of glass/FTO/p-CdTe/Al for (a) AD-CdTe and (b) GC+CC-treated CdTe thin films.

Figure 8.21 shows typical I-V characteristics for glass/FTO/p-CdTe/Au layers of ~1.5 µm thickness subjected to different surface treatments before Au metallisation. I-V curves show that the fabricated device structures exhibited a very good ohmic behaviour and these illustrate the high quality of the thin films. The formation of good ohmic contacts depict that there are little or no surface states at the interface which may affect the ohmic characteristics [54].

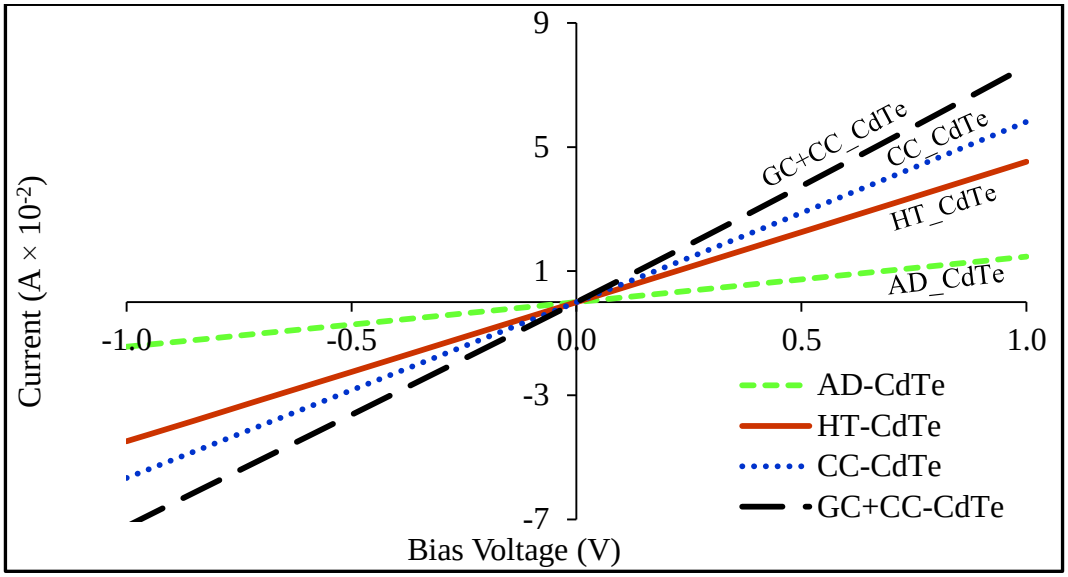


Figure 8.21. I-V characteristics of glass/FTO/p-CdTe/Au structures fabricated with different surface treatments on CdTe layer.

As seen in Figure 8.21, it was observed that the ohmic behaviours of the electroplated CdTe layers differ with varying chemical treatments. The resistance of the fabricated

resistors improved with surface chemical treatments. The minimum resistance value was observed in the CdTe layers treated with GC+CC while AD-CdTe layers possess the maximum resistance. The inclusion of GC into the usual CC treatment has been able to bring about improvement in the material by causing an increase in the material conductivity and reduction in the resistivity as seen in Table 8.7. The chemically-treated CdTe layers also show lower doping density of the order of 10^{13} cm^{-3} when compared to as-grown and ordinarily heat-treated CdTe layers with carrier concentrations of order 10^{15} cm^{-3}. The results obtained in this work are in line with the experimental results reported by Chu et al. [55] that $CdCl_2$ treatment lowers the carrier concentration of CdTe thin films. Therefore, for a high speed electronic device, the electrical conductivity should be large, charge carriers should have high mobility and optimised by an appropriate doping.

The results from I-V and C-V measurements were then used in calculating the mobility of the charge carriers as summarised in Table 8.7.

Table 8.7. Mobility estimation of p-CdTe thin films of ~1.5 µm thickness from I-V and C-V measurement techniques.

	I-V Measurement Results			C-V Measurement Results		Calculated Mobility Results from I-V/C-V
Sample Condition	R (Ω)	$\rho \times 10^{3}$ (Ωcm)	$\sigma \times 10^{-4}$ $(\Omega cm)^{-1}$	Slope $(F^{-2}V^{-1})$	N_A (cm^{-3})	µ $(cm^2V^{-1}s^{-1})$
AD	68.1	17.83	0.56	1.65×10^{18}	7.89×10^{15}	0.04
HT	22.1	5.78	1.73	2.13×10^{18}	6.09×10^{15}	0.18
CC	17.1	4.48	2.23	4.74×10^{20}	2.74×10^{13}	50.95
CC + GC	13.1	3.43	2.92	4.84×10^{20}	2.69×10^{13}	67.74

The mobility values have been calculated indirectly using the conductivity and doping density values obtained from I-V and C-V measurements respectively. This type of mobility is known as mobility perpendicular $(\mu_{\perp})$ because it is the electron mobility in perpendicular direction to the surface of the conducting substrate. The direct method of mobility estimation using the conventional Hall Effect method could not be used in this work due to the underlying conducting substrate on which the CdTe layer is

electroplated [9]. This type of mobility is known as mobility parallel $(\mu_{//})$ because it is the mobility of electrons in parallel direction to the surface of the conducting substrate.

As a result of the columnar growth and high crystallinity exhibited by these CdTe layers when electroplated [10,56], it is expected that their charge carriers should have the highest mobility within the device architecture and reduced recombination thereby leading to better solar cell performances. Due to very high crystallinity observed in rod-shaped semiconductor materials, the photo-generated charge carriers that flows in the direction perpendicular to the FTO substrate do not encounter grain boundary scattering [10]. The values of electron mobility measured in the parallel direction to the FTO surface $(\mu_{//})$ are always lower than the ones measured normal to the FTO surface $(\mu_{\perp})$. This is because when the charge carriers are moving parallel to the FTO substrate, they encounter large number of scattering from grain boundaries which inhibits their rate of flow. These scatterings, when present in large numbers slow down the rate of movement of the charge carriers.

The SEM images illustrated in Figure 8.17 showed that the as-deposited CdTe layers have the highest number of grain boundaries due to their smaller grains. On the other hand, the GC+CC CdTe which shows the highest mobility have the largest grains and least grain boundaries. Because of the very few grain boundaries present in GC+CC CdTe layers, there is less scattering of mobile charge carriers and reduced recombination of electrons and holes in the material. Apart from scattering of mobile charge carriers via the grain boundaries, other scattering sources for the charge carriers are scattering due to: ionised and neutral impurities, collisions between electrons and holes or between electron and electrons, lattice vibration and native defects [27]. The type of devices fabricated using the GC+CC surface treatments are therefore expected to show better solar cell device performances; the details of the devices fabricated from GC+CC surface treatments are discussed in Chapter 9.

8.6 Effect of pH variation of $GaCl_3$+$CdCl_2$ solution for device application

This section discusses the pH variation of $GaCl_3$+$CdCl_2$ solution and its effects on optoelectronic properties of CdTe thin films. The two pH values explored in this section are 2.40 and 0.60±0.02.

8.6.1 Effect on PEC cell measurements

The PEC signals observed for p- and n-CdTe layers as a function of AD-CdTe layer and CdTe layers treated with $GaCl_3$+$CdCl_2$ solution at different pH values (2.40 and 0.60±0.02) are shown in Figure 8.22. The AD-CdTe is used as the baseline for this experiment. For the p-CdTe layers, the PEC signal progressively increases as the pH of the solution decreases while for n-CdTe, the PEC signal decreases in magnitude thus tending towards p-material at a pH of 2.40. A decrease in the pH to 0.60 leads to further increase in the PEC signals as illustrated in Figure 8.22.

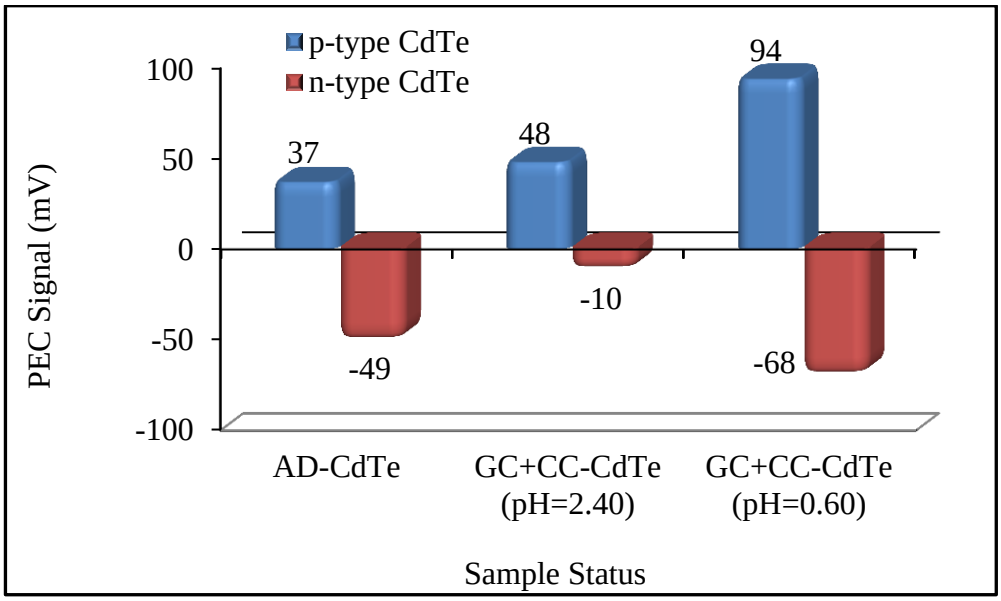


Figure 8.22. pH variation of $GaCl_3$+$CdCl_2$ solution and its effect on PEC signals.

8.6.2 Effect on morphological properties

In this experimental investigation, it was found out that pH of the chemical solutions used in treating the CdTe layers also influences the material morphology. Figure 8.23 (a) and Figure 8.23 (b) show the SEM images of CdTe thin films treated with $GaCl_3$+$CdCl_2$ solution at pH of 2.40 and 0.60±0.02 respectively. The annealing was carried out at temperature of 450^{o}C for 10 minutes in air. Both images show large grains; however, the largest grains were observed in the CdTe thin films chemically treated with solutions of pH 0.60 (Figure 8.23 (b)). A detailed experimental result on how pH influences the solar cell device performance is further discussed in Chapter 9.

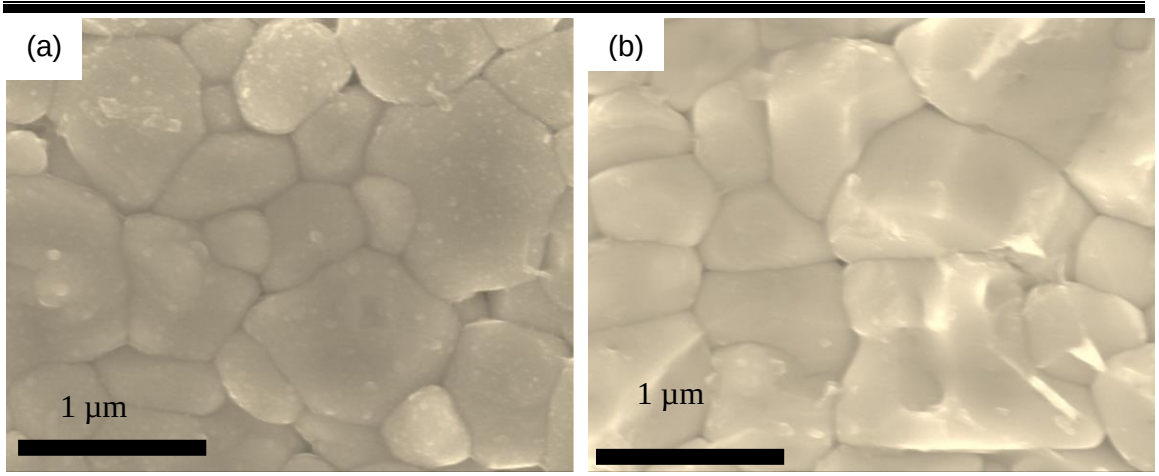


Figure 8.23. SEM images of CdTe layers treated with a mixture of $GaCl_3$+$CdCl_2$ solution at different pH values of (a) 2.40±0.02 and (b) 0.60±0.02.

8.7 Determination of Fermi level positions of electroplated AD- and CC-CdTe as observed from UPS measurement.

The PEC cell measurement is an indirect method of obtaining the approximate Fermi level position of the semiconductor materials. The PEC cell measurement is basically used to determine the type of electrical conduction of a semiconductor by considering sign of the PEC signal. The magnitude of the PEC signal gives a rough idea of where the Fermi level is positioned. Once the Fermi level position (*FLP*) is known, the doping concentration can then be determined. The limitation of PEC cell measurement is that it cannot be used to determine the exact position where the Fermi level lies. It only gives an approximate position for the Fermi level (E_F) based on the magnitude. The limitation in PEC cell measurement is however overcome by carrying out UPS measurement. With UPS measurement, the exact position of E_F can be determined. The UPS experiment was carried out on CdTe layers with an approximate thickness of ~1.5 µm and with the material structure glass/FTO/ED-CdTe. The CC-CdTe layer used for the UPS experiment was annealed at 400^{o}C for 15 minutes in air. The UPS measurements for AD- and CC-CdTe are summarised in Table 8.8. The high *KE* for the Au Fermi level cut-off represents the E_F while the high *KE* for the CdTe Fermi level cut-off represents the top of the valence band egde (E_{Vmax}). Due to the non-uniformity of CdTe layers, the E_{Vmax} measurements were obtained at various points and the average value taken as given in Table 8.8. The non-uniformity may happen as a result of lack of uniformity in the thickness of FTO substrate, thickness variation due to post growth

treatment and differences in the deposition potential along the surface of the FTO substrate as a result of voltage drop.

Table 8.8. Fermi level positions of electroplated AD- and CC-CdTe as observed from UPS measurement.

Sample Status	Gold Fermi level cut-off (E_F) (eV)	CdTe Fermi level cut-off (E_{Vmax}) (eV)		E_F-E_V (eV)		E_C-E_F (eV)		Type	Indicated as
AD-CdTe	25.60	24.18	24.34	1.42	1.26	0.02	0.18	*n*	J_1
				1.34		0.10			
CC-CdTe	25.60	25.31	25.37	0.29	0.23	1.15	1.21	*p*	J_2
				0.26		1.18			

The difference between the E_{Vmax} and E_F (E_F-E_V) as shown in Table 8.8 gives the position of Fermi level of the semiconductor material. A bandgap of 1.44 eV was used for the CdTe thin films so as to find the difference between the E_F and E_{Cmin} (E_C-E_F). As summarised in Table 8.8, the Fermi level of AD-CdTe was found to be at 0.10 eV below the conduction band minimum. This *FLP* shows that the AD-CdTe layer is n-type. For the $CdCl_2$ treated CdTe layers, the *FLP* was found to be at 0.26 eV above the valence band maximum. Since the E_F lies below the intrinsic Fermi level and above the $E_{Vmax,}$ it shows that the $CdCl_2$-treated CdTe layer has converted to p-type after annealing with $CdCl_2$. The pictorial representation of the conversion from n to p-type is illustrated in Figure 8.24.

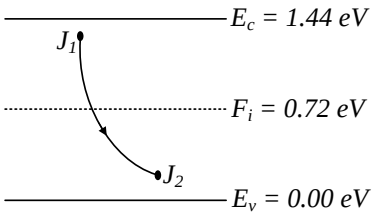


Figure 8.24. Pictorial representation of Fermi-level positions for as-deposited (J_1) and $CdCl_2$-treated (J_2) CdTe layers as observed from UPS measurements. (These measurements were carried out at Conn Centre for Renewable Energy Research at University of Louisville, USA).

The conversion from n- to p- type and vice versa have been well reported in the literature [15,57,58]. This conversion from n- to p- type does not happen always. It should be noted that there are many other parameters that can influence the changes in

the electrical conductivity type of CdTe from n to p and vice versa. Some of the factors are the concentration of Te and Cd ions in the electrolytic bath, the deposition potential used, pH of the electrolyte, different annealing conditions as used in this work, post deposition treatments such as the chemical treatment used in treating the top surface of the CdTe layer and the type of etchants used while processing the material for device fabrication. The previous work on PEC cell measurements discussed in section 8.3.4 describe the possibility of n-CdTe to move towards p-CdTe after annealing in the presence of $CdCl_2$; in this way, there is no total type conversion from n-type CdTe to p-type CdTe. For these particular CdTe layers used for the UPS experiment, the PEC cell measurements show negative signal for AD-CdTe layers and positive signal for CC-CdTe layers. The UPS results therefore show a good agreement with the PEC cell results for both AD- and CC-CdTe layers.

The knowledge of the *FLP* obtained from UPS measurement makes it easier to determine the electron and hole concentrations in the n- and p-type materials respectively. The electron and hole concentrations were determined from Equations (8.8) and (8.9) respectively. The estimated values are presented in Table 8.9. As reported by various researchers in the literature, doping density between ~10^{14} and ~10^{15} cm^{-3} have been obtained for CdS/CdTe solar cells device structures with efficiency greater than 10% [10,12,59,60]. As given in Table 8.9, annealing with $CdCl_2$ treatment brings the doping density to 2.75×10^{14} cm^{-3}; this value falls within the range of doping densities reported in the literature for CdTe-based solar cells >10%.

$$n = N_c \exp\left(\frac{-(E_C - E_F)}{kT}\right) \tag{8.8}$$

$$p = N_V \exp\left(\frac{-(E_F - E_V)}{kT}\right) \tag{8.9}$$

Where n is the electron concentration in cm^{-3}, p is the hole concentration in cm^{-3}, N_C (~7.9×10^{17} cm^{-3}) is the effective density of states in the conduction band edge, N_V (~6.3×10^{18} cm^{-3}) is the effective density of states in the valence band edge, k (1.38×10^{-23} $m^2kgs^{-2}K^{-1}$) is the Boltzmann constant, T is the room temperature measured in Kelvin. The CdTe effective electron mass (m_e^*) used for the estimation of N_C is m_e^* =~$0.1m_o$ while the CdTe effective hole mass (m_p^*) used for the estimation of N_V is m_p^* =~$0.4m_o$ [26].

Table 8.9. Electron and hole concentrations in CdTe layers calculated using the Fermi level positions obtained from UPS studies.

Sample Status	Electrical Conductivity Type	E_C-E_F (eV)	N_C (cm^{-3})	E_F-E_V (eV)	N_V (cm^{-3})	*Doping Density* (cm^{-3})
AD-CdTe (J_1)	n-type	0.10	$\sim 7.9\times10^{17}$	-	-	1.66×10^{16}
CC-CdTe (J_2)	p-type	-	-	0.26	$\sim 6.3\times10^{18}$	2.75×10^{14}

8.8 Summary

The electrodeposition of CdTe thin films have been successfully achieved using a two-electrode set-up in an aqueous solution that contains 1.0 M $CdSO_4$ and ~5 ml of dissolved TeO_2 solution. The electroplated CdTe thin films have cubic crystal structures and are polycrystalline in nature. According to the analysis performed using the XRD technique, CdTe thin films with the highest crystallinity was electroplated at a cathodic potential of 1400 mV. The crystallites sizes of as-deposited CdTe layers between cathodic potentials of 1350 and 1420 mV range between (10.9-32.7) nm. After $CdCl_2$ treatment, the crystallite sizes increased and fall in the range (26.2-52.3) nm within the explored potential range. PEC cell results show that both n- and p-type CdTe thin films can be obtained intrinsically using electroplating technique by varying the cathodic deposition potential. The initial results showed that at growth voltages less than 1370 mV, p-type CdTe thin films are obtained while at growth voltages greater than 1370 mV, n-type CdTe thin films are achieved. The n-type CdTe layers tend to move towards p-CdTe after $CdCl_2$ treatment based on the initial PEC cell results. The compositional analysis using EDX technique revealed that Cd-rich CdTe thin films are n-type while Te-rich CdTe thin films are p-type. The effect of annealing temperature on the electronic properties of n- and p-CdTe thin films was also investigated. The results showed that n-CdTe thin films of approximately same thickness with p-CdTe thin films have lesser electrical resistivity when compared with p-CdTe layers. The high resistivity of as-deposited CdTe layers and CdTe layers annealed ordinarily in air without any prior chemical treatments drastically reduced after treating with $CdCl_2$ solutions. The results obtained from the plot of mobility versus annealing temperatures suggest that

400^{o}C and 450^{o}C are appropriate for heat-treating electroplated n-CdTe and p-CdTe layers respectively.

The influence of different chemical treatments namely $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$ was also explored on the optoelectronic properties of CdTe thin films. The XRD results revealed that CdTe layers annealed in the presence of $GaCl_3$+$CdCl_2$ have improved crystallinity based on enhancements of the (111), (220) and (311) peaks intensities when compared to un-treated CdTe layers and $CdCl_2$-treated CdTe layers. The optical absorption results showed that CdTe layers treated with mixture of $GaCl_3$+$CdCl_2$ have the highest absorption edge and the energy bandgap of 1.44 eV, which is the bandgap for bulk CdTe. The largest grains were also seen in the CdTe layers treated with mixture of $GaCl_3$+$CdCl_2$ when compared to others. The compositional analysis also explained how the incorporation of $GaCl_3$ into the usual $CdCl_2$ treatment can bring Te-rich CdTe layers close to stoichiometry. CdTe layers treated with mixture of $GaCl_3$+$CdCl_2$ have the lowest electrical resistivity and highest mobility as observed from the I-V and C-V measurements. The effect of varying the pH of $GaCl_3$+$CdCl_2$ solution for surface treatment of CdTe layers was also studied. The overall results showed that CdTe layers treated with $GaCl_3$+$CdCl_2$ solution at pH of 0.60±0.02 demonstrate the best performance with respect to the analytical techniques used for the investigation. The results from UPS measurements revealed that $CdCl_2$ treatment changes the doping concentration which in turn influences the Fermi level position of the CdTe thin films.

References

[1] R. K. Pandey, S. N. Sahu, S. Chandra, Handbook of semiconductor electrodeposition, first ed., Marcel Dekker Inc., New York (1996).

[2] M. P. R. Panicker, M. Knaster, F. A. Kroger, J. Electrochem. Soc., **125** (1978) 566.

[3] O. I. Olusola, O. K. Echendu, I. M. Dharmadasa, J. Mater. Sci. Mater. Electron., **26** (2015) 1066–1076.

[4] P. Vanýsek, CRC Handbook of Chemistry and Physics, 91th ed., CRC Press, Boca Raton, Florida (2000).

[5] T. Mahalingam, V. S. John, S. Rajendran, P. J. Sebastian, Semicond. Sci. Technol., **17** (2002) 465–470.

[6] F. Fauzi, D. G. Diso, O. K. Echendu, V. Patel, Y. Purandare, R. Burton, I. M. Dharmadasa, Semicond. Sci. Technol., **28** (2013) 045005.

[7] A. Monshi, World J. Nano Sci. Eng., **02** (2012) 154–160.

[8] M. J. Peterson, F. H. Cocks, Mater. Sci. Eng., **41** (1979) 143–147.

[9] N. B. Chaure, S. Bordas, A. P. Samantilleke, S. N. Chaure, J. Haigh, I. M. Dharmadasa, Thin Solid Films, **437** (2003) 10–17.

[10] I. M. Dharmadasa, P. A. Bingham, O. K. Echendu, H. I. Salim, T. Druffel, R. Dharmadasa, G. U. Sumanasekera, R. R. Dharmasena, M. B. Dergacheva, K. A. Mit, K. A. Urazov, L. Bowen, M. Walls, A. Abbas, Coatings, **4** (2014) 380–415.

[11] M. Takahashi, K. Uosaki, H. Kita, S. Yamaguchi, J. Appl. Phys., **60** (1986) 2046–2049.

[12] I. M. Dharmadasa, Coatings, **4** (2014) 282–307.

[13] M. Berding, Phys. Rev. B, **60** (1999) 8943–8950.

[14] A. Carvalho, A. Tagantsev, S. Öberg, P. R. Briddon, N. Setter, Phys. B Condens. Matter, **404** (2009) 5019–5021.

[15] B. M. Basol, S. S. Ou, O. M. Stafsudd, J. Appl. Phys., **58** (1985) 3809–3813.

[16] N. A. Abdul-Manaf, PhD Thesis "Organic/Inorganic Hybrid Solar Cells Based on Electroplated CdTe," Sheffield Hallam University, Sheffield, 2015.

[17] A. Hossain, Y. Cui, A. E. Bolotnikov, G. S. Camarda, G. Yang, D. Kochanowska, M. Witkowska-Baran, A. Mycielski, R. B. James, J. Electron. Mater., **38** (2009) 1593–1599.

[18] I. S. Yahia, G. B. Sakr, T. Wojtowicz, G. Karczewski, Semicond. Sci. Technol., **25** (2010) 095001.

[19] I. S. Yahia, F. Yakuphanoglu, S. Chusnutdinow, T. Wojtowicz, G. Karczewski, Curr. Appl. Phys., **13** (2013) 537–543.

[20] M. G. Helander, M. T. Greiner, Z. B. Wang, W. M. Tang, Z. H. Lu, J. Vac. Sci. Technol. A Vacuum, Surfaces, Film., **29** (2011) 011019.

[21] S. K. Das, G. C. Morris, Sol. Energy Mater. Sol. Cells, **30** (1993) 107–118.

[22] Y. F. Lin, J. Song, Y. Ding, S. Y. Lu, Z. L. Wang, Adv. Mater., **20** (2008) 3127–3130.

[23] L. A. Kosyachenko, R. Yatskiv, N. S. Yurtsenyuk, O. L. Maslyanchuk, J. Grym, Semicond. Sci. Technol., **29** (2014) 015006.

[24] A. Rohatgi, R. Sudharsanan, S. A. Ringel, M. H. MacDougal, Sol. Cells, **30** (1991) 109–122.

[25] R. Ochoa Landin, O. Vigil Galan, Y. V. Vorobiev, R. Ramirez-Bon, Sol. Energy, **83** (2009) 134–138.

[26] L. L. Chang, Superlattices Microstruct., **6** (1989) 39–45.

[27] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New Jersey (2007).

[28] S. Pizzini, Physical Chemistry of Semiconductor Materials and Processes, first ed., John Wiley & Sons Ltd., Chichester, West Sussex, England (2015).

[29] M. Miyake, K. Murase, T. Hirato, Y. Awakura, J. Electroanal. Chem., **562** (2004) 247–253.

[30] S. H. Shin, J. Bajaj, L. a. Moudy, D. T. Cheung, Appl. Phys. Lett., **43** (1983) 68–70.

[31] S. Hu, C. H. Henager, J. Cryst. Growth, **311** (2009) 3184–3194.

[32] P. M. Amirtharaj, F. H. Pollak, Appl. Phys. Lett., **45** (1984) 789–791.

[33] P. Fernández, J. Optoelectron. Adv. Mater., **5** (2003) 369–388.

[34] N. V. Sochinskii, M. D. Serrano, E. Dieguez, F. Agullo-Rueda, U. Pal, J. Piqueras, P. Fernandez, J. Appl. Phys., **77** (1995) 2806–2808.

[35] I. M. Dharmadasa, O. K. Echendu, F. Fauzi, N. A. Abdul-Manaf, H. I. Salim, T. Druffel, R. Dharmadasa, B. Lavery, J. Mater. Sci. Mater. Electron., **26** (2015) 4571–4583.

[36] S. A. Ringel, A. W. Smith, M. H. MacDougal, A. Rohatgi, J. Appl. Phys., **70** (1991) 881–889.

[37] A. Romeo, S. Buecheler, M. Giarola, G. Mariotto, A. N. Tiwari, N. Romeo, A. Bosio, S. Mazzamuto, Thin Solid Films, **517** (2009) 2132–2135.

[38] X. Wu, Sol. Energy, **77** (2004) 803–814.

[39] M. A. Redwan, E. H. Aly, L. I. Soliman, A. A. El-Shazely, H. A. Zayed, Vacuum, **69** (2003) 545–555.

[40] C. Ferekides, J. Britt, Sol. Energy Mater. Sol. Cells, **35** (1994) 255–262.

[41] F. de Moure-Flores, J. G. Quiñones-Galván, A. Guillén-Cervantes, J. S. Arias-Cerón, A. Hernández-Hernández, J. Santoyo-Salazar, J. Santos-Cruz, S. A. Mayén-Hernández, M. de la L. Olvera, J. G. Mendoza-Álvarez, M. Meléndez-Lira, G. Contreras-Puente, J. Cryst. Growth, **386** (2014) 27–31.

[42] J. Han, C. Spanheimer, G. Haindl, G. Fu, V. Krishnakumar, J. Schaffner, C. Fan, K. Zhao, A. Klein, W. Jaegermann, Sol. Energy Mater. Sol. Cells, **95** (2011) 816–820.

[43] A. Bosio, N. Romeo, S. Mazzamuto, V. Canevari, Prog. Cryst. Growth Charact. Mater., **52** (2006) 247–279.

[44] T. R. Ravindran, A. K. Arora, B. Balamurugan, B. R. Mehta, Nanostructured

Mater., **11** (1999) 603–609.

[45] F. Bin Fauzi, PhD Thesis "Research and Development of CdS/CdTe Solar Cells Incorporating ZnTe Layers," Sheffield Hallam University, Sheffield, 2015.

[46] A. Romeo, S. Buecheler, M. Giarola, G. Mariotto, A. N. Tiwari, N. Romeo, A. Bosio, S. Mazzamuto, Thin Solid Films, **517** (2009) 2132–2135.

[47] T. L. Chu, S. S. Chu, Solid State Electron., **38** (1995) 533–549.

[48] D. Jenny, R. Bube, Phys. Rev., **96** (1954) 1190–1191.

[49] F. Kruger, D. de Nobel, J. Electron., **1** (1955) 190–202.

[50] K. Zanio, Semiconductors and Semimetals (Volume 13, Cadmium Telluride), Academic Press, New York, USA (1978).

[51] N. B. Chaure, A. P. Samantilleke, I. M. Dharmadasa, Sol. Energy Mater. Sol. Cells, **77** (2003) 303–317.

[52] B. E. Mccandless, J. R. Sites, Cadmium Telluride Solar Cells, in: Handb. Photovolt. Sci. Eng., first ed., John Wiley & Sons, Ltd, Chichester, West Sussex, England (2003): pp. 617–662.

[53] H. Khallaf, G. Chai, O. Lupan, L. Chow, S. Park, A. Schulte, Appl. Surf. Sci., **255** (2009) 4129–4134.

[54] D. A. Neamen, Semiconductor Physics and Devices: Basic Principles, third ed., McGraw-Hill, New York (2003).

[55] T. L. Chu, S. S. Chu, C. Ferekides, J. Britt, C. Q. Wu, J. Appl. Phys., **71** (1992) 3870–3876.

[56] B. M. Basol, J. Appl. Phys., **55** (1984) 601–603.

[57] V. Valdna, F. Buschmann, E. Mellikov, J. Cryst. Growth, **161** (1996) 164–167.

[58] E. Belas, J. Franc, R. Grill, A. L. Toth, P. Horodysky, P. Moravec, P. Hoschl, J. Electron. Mater., **34** (2005) 957–962.

[59] J. Britt, C. Ferekides, Appl. Phys. Lett., **62** (1993) 2851–2852.

[60] J. M. Woodcock, A. K. Turner, M. E. Ozsan, J. G. Summers, Thin film solar cells

based on electrodeposited CdTe, in: Conf. Rec. Twenty Second IEEE Photovolt. Spec. Conf., Las Vegas, NV, USA (1991): pp. 842–847.

Chapter 9 - Development of CdTe-based solar cells

9.1 Introduction

This chapter describes the fabrication of solar cells using different chemicals for surface treatments of the developed solar cell device structures. Studies were also carried out on solar cell device structures based on CdTe thin films that are treated with the mixture of $GaCl_3$ and saturated $CdCl_2$ at three different pH values. The three pHs explored are ~2.40±0.02, ~1.20±0.02 and ~0.60±0.02. Also, different solar cell device architectures have been carried out and their results are presented in this chapter. The knowledge of properties exhibited by the semiconductor materials discussed in the earlier chapters (Chapters 4-8) have been utilised in this chapter for solar cells fabrication. The fabricated solar cells are classified as two-layer and three-layer hetero-junction cells. The basic configuration of the two-layer hetero-junction solar cells discussed in this chapter is glass/FTO/n-CdS/n-CdTe/Au. The three-layer hetero-junction cells are referred to as multi-junction graded bandgap solar cells; most of the solar cell devices explored in this research and discussed in this chapter are from this category. They are: glass/FTO/n-CdS/n-CdTe/p-CdTe/Au, glass/FTO/n-CdS/n-CdTe/p-CdMnTe/Au, glass/FTO/n-CdS/n-CdTe/p-ZnTe/Au, glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe /Au.

9.2 Basic device processing steps

After developing the device structures, they were processed before making metal contacts on them. The fundamental device processing procedures used in this work are chemical treatments of the top surface of the CdTe absorber layers, post-deposition heat treatment and application of chemical etchants. The basic chemical used for treating the surface of the CdTe-based device is $CdCl_2$ saturated solution. This treatment has been in use since 1976 [1] and numerous reports in the literature show that $CdCl_2$ treatment drastically improves solar to electrical energy conversion efficiency [2–4] . However in the present research work, modifications of the surface treatments have been carried out by incorporating $GaCl_3$ into the universal $CdCl_2$ chemical treatment. This has been discussed in details in the preceding chapter. Also, post-deposition heat treatment which is an important processing step was carried out for the CdTe-based solar cell device

structures at annealing temperatures ranging from 400-450^{o}C within the duration of 10-20 minutes in air.

The chemical etchants used are acidic etchants and alkaline etchants. Etching is usually carried out to remove any form of surface impurities on the layer; by so doing, a cleaner surface with reduced defects is being ensured. Surface contaminations such as oxides formed on the CdTe top surface during heat-treatment in air can also be removed during etching process [5]. These two etchants can help in modifying the CdTe surface stoichiometry before back metal contact evaporation. For instance, acidic etchants attack Cd preferentially and leave the CdTe thin films with a Te-rich surface while the alkaline etchants attack Te preferentially and leave a Cd-rich surface [6]. The acidic etchant was prepared by dissolving 1 g of potassium di-chromate ($K_2Cr_2O_7$) in 20 ml of de-ionised water; this was followed by the addition of 1 ml of concentrated H_2SO_4 acid into the prepared solution. The alkaline etchant was prepared by dissolving 0.5 g of NaOH and 0.5 g of $Na_2S_2O_3$ in 50 ml of de-ionised water. The alkaline etchant solution was heated up to a temperature of ~60^{o}C before being used. The device structures were dipped inside the acidic etchant solution for ~5 seconds after which they were removed and rinsed in de-ionised water before being transferred to the alkaline solution for etching. The alkaline etchant duration was ~120 seconds.

After performing the alkaline etching, the device structures were rinsed again in de-ionised water, dried with nitrogen gas before being transferred to the vacuum coating system for back contact metallisation. It is essential to quickly transfer the etched layers into the vacuum coating system to prevent the surface from oxidising. Oxidation of the top surface can be at times useful since it creates an insulating (*I*) layer between the metal and semiconductor [7]. If the created *I* layer is very thin, it can act as a de-coupler between the metal and semiconductor and this tends to increase the band bending at the interface [8] as explained in Chapter two. However, if the created insulating layer is very thick, it introduces additional series resistance to the solar cell device structures, decreases the short-circuit current density and causes a deterioration of the solar cell conversion efficiency [9]. The final stage of the solar cell device fabrication before device assessment is the deposition of Au back contact. Au metal contacts have been mostly used in this work as back contact to CdTe-based solar cells. The metal coatings were done using Edwards Auto 306 vacuum metalliser at a chamber pressure of 10^{-7} mbar. The diameter and thickness of the Au contacts are 2 mm and ~100 nm respectively.

9.3 Motivation behind $GaCl_3$ incorporation

One of the main reasons of incorporating $GaCl_3$ treatment in this work is due to the ability of Ga to remove Te precipitates as reported by Sochinskii et al. [10] and Fernandez [11]. The experimental work carried out by Sochinskii et al. [10] demonstrated the possibility of removing Te precipitates in CdTe single crystals after annealing in Ga melt and Cd vapour media. In the work reported by Sochinskii et al. [10], as-grown p-CdTe wafers were annealed within the temperature range (500-600)^{o}C in Ga melt and Cd vapour for two different time durations. At a short annealing period of 2 hours, the authors observed that small Te precipitates disappeared leaving the larger ones behind. By further increasing the annealing time to 22 hours, the authors noticed a total disappearance of Te precipitates in the p-CdTe wafers volume. Thus, their work showed that treating a Te-rich CdTe layer in Ga melt or Cd vapour coupled with annealing time helps in the removal of Te precipitates. Te precipitates have been reported by researchers to be detrimental to optoelectronic devices [12,13]. The results from their works prompted the use of precursor containing Ga atoms to be applied as chemicals for surface treatment of CdTe-based device structures in this work.

9.4 Preparation of $GaCl_3$ and $CdCl_2$ solutions for surface treatment before annealing

The initial $GaCl_3$ aqueous solution was prepared by using gallium (III) sulphate as Ga precursor and concentrated hydrochloric acid (HCl) acid as Cl precursor. 0.18 M of $Ga_2(SO_4)_3$ was prepared by adding ~1.06 g of $Ga_2(SO_4)_3$ into 35 ml of de-ionised water to produce an aqueous solution. The initial pH of the $Ga_2(SO_4)_3$ solution was measured to be ~1.28±0.02 at room temperature. 2.5 ml of concentrated HCl acid was later added to the prepared $Ga_2(SO_4)_3$ solution to initiate a reaction leading to gallium chloride ($GaCl_3$). Ga has the unique feature of reacting slowly with HCl acid to produce gallium chloride required for this treatment [14]. The new pH of the solution was measured to be ~0.60±0.02 at room temperature after the HCl addition.

Saturated $CdCl_2$ aqueous solution was prepared by adding 0.15 M of $CdCl_2$ to 35 ml of de-ionised water. The $GaCl_3$ and $CdCl_2$ mixture were put together in 100 ml beaker and it was continuously stirred to obtain homogeneity before being used as surface treatment to CdTe thin films. Drops of the mixed solution were then applied to the top surface of the device structure with the aid of laboratory pipette and the solution was

uniformly spread on the CdTe thin film surface. The device structure was allowed to dry in air before annealing inside a temperature controlled furnace. The initial device structures were subjected to different annealing conditions. For the purpose of discussion in this work, treatment with $GaCl_3$ solution only is denoted as GC, treatment with $CdCl_2$ solution only is denoted as CC while treatment with mixture of $GaCl_3$ and $CdCl_2$ solution is denoted as GC+CC.

9.5 What happens when the top surface of CdTe layers are treated with Ga

As explained by Basol [15], the likely intrinsic defects in CdTe thin films are cadmium interstitials (Cd_i), cadmium vacancies (V_{Cd}), tellurium interstitials (Te_i) and tellurium vacancies (V_{Te}). Tellurium vacancies and cadmium interstitials act as donors while cadmium vacancies and tellurium interstitials act as acceptors. These donors and acceptors are all intrinsic in nature because they come mainly from the atoms that make up the semiconductor and not from external chemical elements introduced during growth, surface treatment or etching. Chu et al. [16] explained that triethylgallium (TEGa) can be used as an extrinsic dopant to change the electrical conductivity type of p-CdTe to n-type. The authors affirmed that one of the factors which determine the CdTe resistivity is the incorporation of Ga into Cd sites when TEGa is introduced as an extrinsic dopant into the MOCVD reaction chamber containing a mixture of dimethylcadmium and di-isopropyltellurium for CdTe formation. The explanation given by these authors showed the possibility of Ga occupying Cd sites. Similarly, Fernández [11] reiterated the possibility of Ga atoms to diffuse from Ga melt into the CdTe wafer during annealing of the wafers in Ga melt. Fernández [11] explained that when Ga diffuses into the CdTe wafer, the donor concentration is increased as a result of Ga atoms residing in Cd sites. Either Ga is used as a dopant or for treatment purpose to remove Te precipitates, Chu et al. [16] and Fernandez [11] both explained the possibility of Ga atoms being in Cd sites.

If the n-CdTe top surface is chemically treated with solutions containing trivalent atoms such as gallium (Ga), it is therefore possible for Ga being a trivalent atom to displace Cd in CdTe to form $Ga_{Cd}Te$. Two out of the three valence electrons in the Ga atoms are involved in forming covalent bonds with the six valence electrons of the neighbouring Te atoms. The remaining one negatively-charged electron which does not take part in bond formation becomes free and available for conduction; this conduction electron is

now donated to the crystal lattice in the conduction band. The Ga atom is therefore called a donor atom when it displaces Cd in its site due to its ability to give out a free electron for conduction. Figure 9.1 (a) shows the covalent bond formation that takes place between one Cd and Te valence atom while Figure 9.1 (b) illustrates the likely bond formation between the Ga and Te atoms after $GaCl_3$ surface treatment.

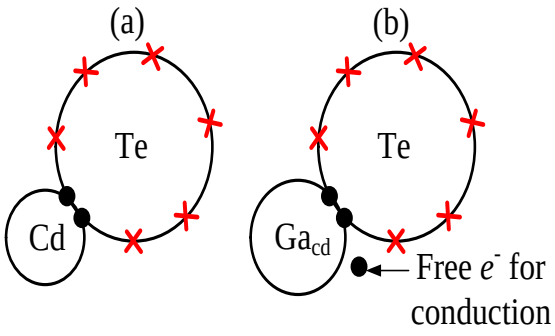


Figure 9.1. Covalent bond formation between (a) Cd and Te atoms and (b) Ga occupying Cd sites and bonding with Te as a result of surface treatment.

9.6 Fabrication of glass/FTO/n-CdS/n-CdTe/ device structures

The electroplated n-CdS layers used in this work were grown on glass/FTO substrates at a cathodic potential of 1200 mV with an approximate thickness of 150 nm. The CdS layers were annealed at 400^{o}C for 20 minutes in air. The CdS layers were first allowed to cool down after annealing before carrying out CdTe deposition. The CdTe layers were grown in the n-region at a cathodic potential of 1400 mV. Growing CdTe thin films at this cathodic potential ensures the deposition of n-type CdTe layers at most times provided the Te level in the bath is kept low. Most of the CdTe layers grown for device making and reported in this work were grown for ~3.0 to 5.5 hours with thickness ranging between ~1.2-2.0 µm. The thin film semiconductors obtained after depositing CdTe layers on CdS layers now become n-n heterojunction with the structure glass/FTO/n-CdS/n-CdTe. A schematic diagram of glass/FTO/CdS/CdTe/Au is illustrated in Figure 9.2 (a) while Figure 9.2 (b) and 9.2 (c) show the pictorial view of the fabricated glass/FTO/CdS/CdTe before and after gold (Au) coatings respectively.

Since annealing/annealing with chemical treatment is one of the basic processing steps required to obtain high efficiency solar cells [2,17], some of the device structures reported in this work were heat-treated without and with chemical treatments so as to observe the respective changes brought about by the introduction of chemicals used in

surface treatments. The device structures annealed ordinarily without chemical treatments were used as a reference sample to the chemically-treated ones. After annealing, the CdTe layers were allowed to cool down before rinsing the top surface with de-ionised water; this was done to remove the presence of any residues that might be left after chemical treatments. The rinsed surfaces are later dried with nitrogen gas before etching and metallisation.

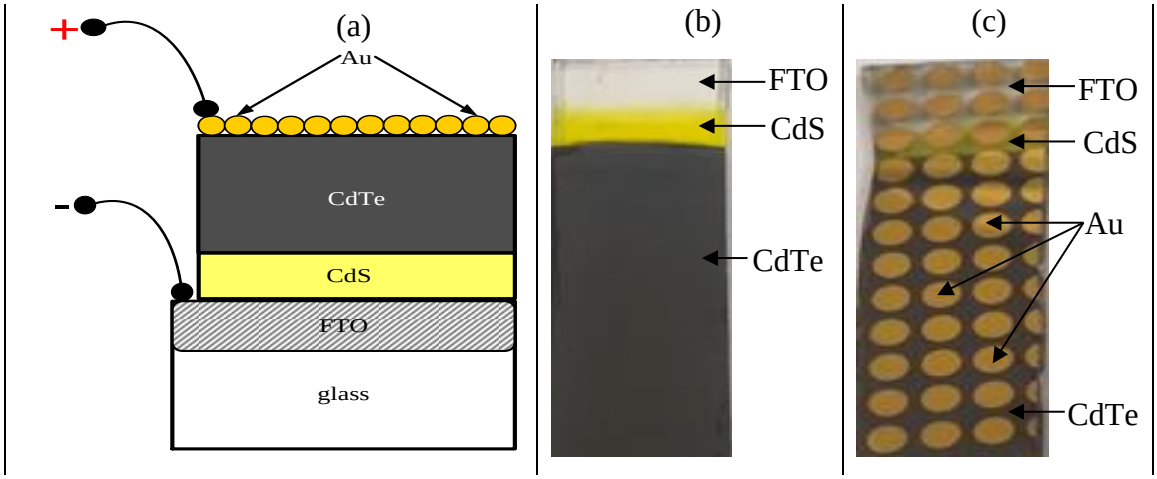


Figure 9.2. (a) Typical schematic diagram of glass/FTO/CdS/CdTe/Au, (b) glass/FTO/CdS/CdTe device structures fabricated before Au coating and (c) Solar cells fabricated from glass/FTO/CdS/CdTe/Au device structures.

9.7 Assessment of glass/FTO/n-CdS/n-CdTe/Au solar cells

The fabricated solar cells with the structure glass/FTO/n-CdS/n-CdTe/Au were characterised using I-V technique. Keithley 2401 with embedded power supply and solar simulators were used to assess the I-V characteristics of the developed solar cells under dark and illumination conditions. Table 9.1 shows the summary of I-V parameters obtained under AM1.5 illumination. The thicknesses of CdS and CdTe thin films used in this experiment were ~150 nm and 1500 nm respectively. The annealing temperature and time for samples in Table 9.1 were 450^{o}C and 10 minutes in air. These initial solar cells were fabricated under three different conditions. Solar cells labelled CP-19B were annealed ordinarily in air; CP-19C was annealed with $CdCl_2$ treatment only while CP-19G was annealed with $GaCl_3$ treatment only. The efficiencies obtained from this initial work are generally very poor; however, it could be seen that each of the treatment used played a key role in improving some of the solar cell parameters. For instance, it was observed that solar cells made from device structures treated with $GaCl_3$ only had the

highest FF while the highest J_{sc} was observed in the device structures treated with $CdCl_2$ only. Overall, the lowest efficiency was observed in the solar cells fabricated from samples that were not subjected to any chemical treatments before annealing. The highest cell efficiency for each of the three different conditions are boldened and highlighted as shown in Table 9.1 and their J-V curves are illustrated in Figure 9.3.

The series resistance and shunt resistance of the best cells represented in Figure 9.3 were also measured under AM1.5 illumination conditions. The HT-device structure was found to have the highest R_s. After $GaCl_3$ treatment, a reduction was observed in the R_s from 3185 Ω to 1911 Ω. The application of $CdCl_2$ reduces the R_s value from 3185 Ω to 732 Ω. The reduction of R_s value after $CdCl_2$ treatment as seen in this work agrees with the explanation given by Rohatgi et al. [18] that $CdCl_2$ treatment causes a reduction in R_s. The presence of low R_s in CC-device structure is one of the contributing factors which led to its J_{sc} improvement as compared to HT- and GC-device structures. The highest R_{sh} value was observed in GC-device structure; this value is more than four times and twelve times higher than the R_{sh} values observed in HT- and CC-device structures respectively. It is a well-known fact that low R_{sh} and high R_s values cause a significant reduction in FF. Therefore, the improvement in FF of CC-device structure as compared to the HT-device structure can be explained in terms of its lower R_s value while the better FF observed in GC-device structure with respect to other treatments can be attributed mainly to increased R_{sh} value. The results from this initial work led to the decision made in using a mixture of $GaCl_3$ and $CdCl_2$ solution for surface treatment in the subsequent experimental investigations carried out in this research programme. Based on the initial work, it is expected that the mixture of $GaCl_3$ and $CdCl_2$ solution would enhance all solar cell parameters.

Table 9.1. Solar cell parameters obtained from CdTe layers treated with different conditions. Note that the highlighted and boldened sample ID signifies cells with highest efficiency for each of the three different conditions.

Samples		Measured values per unit cell				Average measured values			
Sample status	Sample ID	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)
Annealed ordinarily in air (HT)	CP19-B_33	330	3.8	0.22	0.28	350	3.7	0.22	0.29
	CP19-B_32	420	3.4	0.20	0.29				
	CP19-B_23	300	4.0	0.24	0.29				
Annealed with $CdCl_2$ in air (CC)	CP19-C_13	270	9.8	0.27	0.71	273	12.9	0.27	0.95
	CP19-C_23	250	11.3	0.27	0.76				
	CP19-C_43	300	17.5	0.27	1.42				
Annealed with $GaCl_3$ in air (GC)	CP19-G_12	290	2.9	0.36	0.30	293	3.0	0.36	0.30
	CP19-G_22	290	3.0	0.36	0.31				
	CP19-G_33	300	3.1	0.35	0.33				

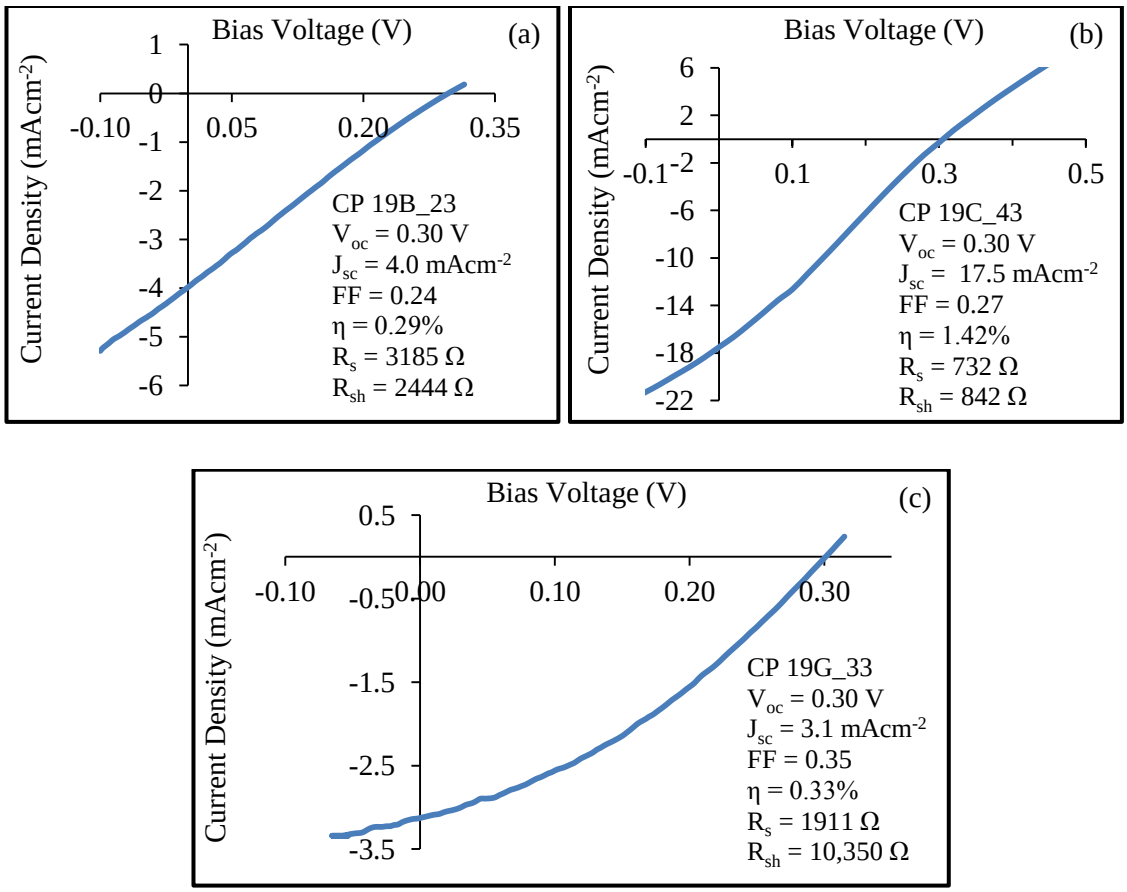


Figure 9.3. Typical J-V curves obtained for best solar cells fabricated from samples annealed (a) ordinarily in air, (b) with $CdCl_2$ treatment only and (c) with $GaCl_3$ treatment only.

9.8 Investigating the effect of $GaCl_3$ inclusion into the usual $CdCl_2$ treatment on glass/FTO/n-CdS/n-CdTe/Au device structures

The annealing temperature of 450^oC was discontinued for the n-n heterojunction device structure due to the reduced V_{oc} observed in the initial work. The experimental investigations carried out by Abdul [19] showed that 450^oC may not be suitable for device processing. The author's work showed that chemically treated device structures processed at high annealing temperature of 450^oC showed a huge reduction in V_{oc} and FF when compared to device structures processed at annealing temperature of 400^oC. The J_{sc} values obtained at 400^oC and 450^oC by the author for the different chemical treatments showed that the results are comparable with one another [19]. Table 9.2 shows the summary of I-V parameters obtained under AM1.5 illumination for CdS/CdTe device structures annealed under different chemical treatment conditions. The thicknesses of CdS and CdTe thin films used in this experiment were ~150 nm and 2.0 µm respectively. The chemical treatments employed here are: $CdCl_2$ only, mixture of $GaCl_3$+$CdCl_2$+CdF_2 and mixture of $GaCl_3$+$CdCl_2$. Samples treated with $CdCl_2$ are labelled CP 20C, CP 20M denotes samples treated with combination of $GaCl_3$+$CdCl_2$+CdF_2 while CP 20S refers to CdTe based device structures treated with mixture of $GaCl_3$+$CdCl_2$. The full details of the sample ID and status are illustrated in Table 9.2. The annealing temperature and time for samples in Table 9.2 are 400^oC and 15 minutes in air.

As expected, drastic improvements were seen in solar cells fabricated from device structures treated with Ga incorporation into $CdCl_2$ solution when compared to solar cells fabricated from device structures treated only with $CdCl_2$. These experimental results show that mixture of $GaCl_3$+$CdCl_2$ solution would be an effective means of treating CdTe top surface prior to metal evaporation. The reason for the improvement in device structures treated with chemical solutions containing Ga, Cd and Cl ions can be attributed to the ability of the trio to remove Te precipitates, reduce structural defects and doping effects [11]. Removal of Te precipitates can take place when CdTe thin films are deposited or when their surfaces are treated in a medium containing Cd or Cl ions [20,21]. As previously explained in section 9.3 and reported by Sochinskii et al. [10] and Fernandez [11], Te precipitates can also be successfully removed after annealing CdTe in Ga melt and Cd vapour media. Therefore, getting a solution containing Ga^{3+}, Cd^{2+} and Cl^- would be an effective means of removing Te precipitates.

Table 9.2. Summary of solar cell parameters fabricated from device structures annealed in the presence of $CdCl_2$, $GaCl_3$+$CdCl_2$+CdF_2 and $GaCl_3$+$CdCl_2$ solutions. The highlighted sample ID denotes cells with highest efficiency for each of the three different conditions.

Samples		Measured values per unit cell						Average measured values					
Sample status	Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	R_s (Ω)	R_{sh} (Ω)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	R_s (Ω)	R_{sh} (Ω)
Annealed with $CdCl_2$ in air	CP 20C_32	620	13.4	0.23	1.9	2195	2330	620	14.1	0.23	2.0	2551	2147
	CP 20C_14	620	14.3	0.23	2.0	3194	2077						
	CP 20C_33	620	14.5	0.24	2.2	2263	2033						
Annealed with $GaCl_3$ + $CdCl_2$ + CdF_2 in air	CP 20M_12	560	26.8	0.32	4.8	625	1737	570	30.6	0.32	5.6	569	1687
	CP 20M_13	570	31.4	0.31	5.6	588	1647						
	CP 20M_14	580	33.6	0.32	6.2	493	1676						
Annealed with $GaCl_3$ + $CdCl_2$ in air	CP 20S_24	620	37.4	0.29	6.7	508	1165	607	37.8	0.31	7.1	457	1386
	CP 20S_23	600	36.6	0.31	6.8	442	1566						
	CP 20S_22	600	39.4	0.32	7.6	420	1426						

An additional Cd precursor containing fluorine atoms (CdF_2) was also incorporated into the $GaCl_3$ treatment to observe its effect in sample CP-20M. This is due to the earlier reports given by Mazzamuto et al. [22] and Echendu et al. [23] that incorporation of fluorine atoms into the chlorine atmosphere during surface treatment rapidly promotes grain growth and increase device efficiency. Even though CP-20M showed better results than CP-20C in terms of improvement in J_{sc} and FF, better device efficiencies were obtained from samples CP-20S which had no fluorine incorporation as shown in Table 9.2. Due to this and subsequent results obtained from other experiments involving CdF_2 incorporation into the mixture of $GaCl_3$ and $CdCl_2$ solution which are not reported in this thesis; therefore, the incorporation of CdF_2 into GC+CC was discontinued.

As observed in the initial work discussed in section 9.7, a remarkable improvement was seen in the FF of device structures treated with $GaCl_3$ solution while $CdCl_2$ treatment drastically improves the J_{sc}. By combining the two chemical treatments together, a great improvement in all solar cell parameters was observed as shown in Table 9.2 when compared to the initial results stated in Table 9.1. As seen in Table 9.2, drastic improvements were observed in J_{sc} and FF of samples treated with chemical solutions containing Ga^{3+}, Cd^{2+} and Cl^{-}. This improvement can be mainly attributed to the complementary efforts of these three ions to effectively combat Te precipitates. As discussed in Chapter 8, CdTe thin films which were chemically treated with mixture of $GaCl_3$+$CdCl_2$ produced bandgap which corresponds to the energy bandgap of bulk CdTe thin films, sharpest absorption edge, highest crystallinity, least resistivity, highest conductivity, moderate doping density, higher mobility and larger grains when compared with CdTe thin films treated only with $CdCl_2$. The excellent collective features displayed by the $GaCl_3$+$CdCl_2$-treated CdTe layers thus enhance the transportation of mobile charge carriers across the device structure. This is therefore one of the likely reasons why solar cells fabricated from $GaCl_3$+$CdCl_2$-treated device structures with CdTe as an absorber layer showed improved solar cell parameters especially in the J_{sc} and FF. It could also be observed from Table 9.2 that the incorporation of Ga into $CdCl_2$ treatment solution has helped in further reducing the R_s as seen from samples CP-20M and CP-20S. The J-V curves of the best cells for each of the three treatments explained in Table 9.2 are diagrammatically shown in Figure 9.4.

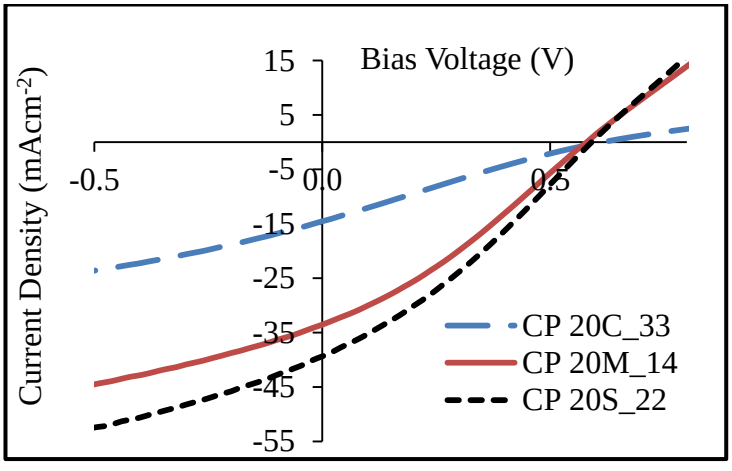


Figure 9.4. J-V curves obtained for best cells fabricated from samples annealed in air with: $CdCl_2$ treatment only (CP20C_33), $GaCl_3$+$CdCl_2$+CdF_2 treatment (CP 20M_14) and with $GaCl_3$+$CdCl_2$ treatment (CP 20S_22).

9.9 Effect of pH variation of $GaCl_3$+$CdCl_2$ treatment solution on efficiency of glass/FTO/n-CdS/n-CdTe/Au solar cells

In this section, the effect of variation in the pH of $GaCl_3$+$CdCl_2$ treatment solution was investigated on glass/FTO/n-CdS/n-CdTe/Au device structures. Three different pH values have been used namely 2.40±0.02, 1.20±0.02 and 0.60±0.02. Several cells were measured for each of the different pH treatments but to summarise, the best cell was selected from each set of pH values for easy comparison. Figure 9.5 shows typical J-V curves of the three different cells and their pH treatment values.

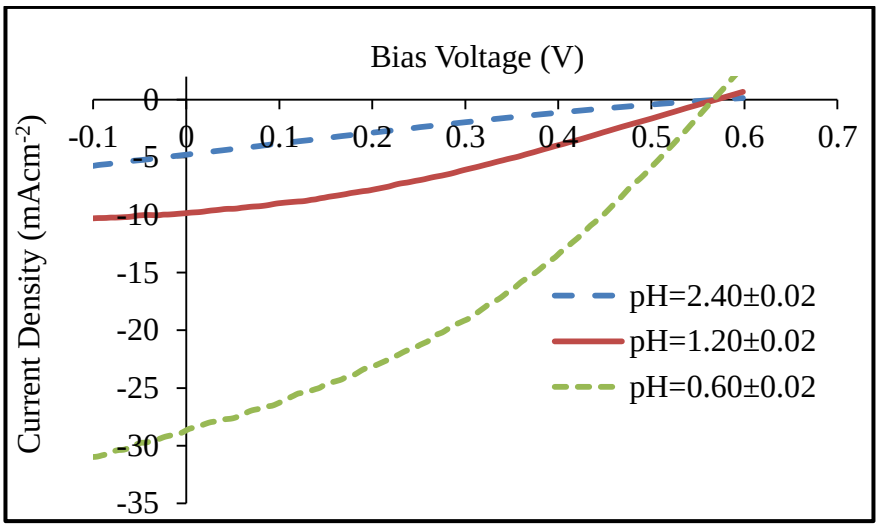


Figure 9.5. Typical J-V curves illustrating the effect of pH variation of $GaCl_3$+$CdCl_2$ solution on glass/FTO/n-CdS/n-CdTe/Au solar cell device structures.

As illustrated in Figure 9.5, the V_{oc} remains fairly the same with a slight variation. The comparable V_{oc} shows that the Fermi level is pinned at similar position thus making the ϕ_b to be almost the same value. These very results explain that the variation in pH treatments may not affect the defects which determine the position at which Fermi level pins. However, it can be seen that parameters such as the FF and J_{sc} were influenced by this variation. The mostly influenced solar cell parameter is the J_{sc}. The measured solar cell parameters at different pH of the chemical solutions used for surface treatments are given in Table 9.3. As seen in Table 9.3, a reduction in the pH causes an increase in the J_{sc}. This increase can be attributed mainly to the low R_s observed at very low pH value. At a low pH of 0.60±0.02, the R_s was minimal. This is because as the pH becomes acidic, more Cd is preferentially removed from the top surface of the CdTe absorber layer thereby leaving a thin Te-rich layer at the surface of the CdTe. The presence of thin Te-rich layer creates a p^+ material on the n-n+SB device structures and this changes

the device architecture. It is therefore possible for the device configuration to become n-n-p^+ at low pH of 0.60±0.02.

Table 9.3. Summary of solar cell parameters obtained from n-n+SB device structures treated with $GaCl_3$+$CdCl_2$ solution prior annealing and metallisation.

		Measured values under AM1.5 illumination condition				
Sample ID	pH±0.02	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	R_s (Ω)
Ol_1	2.40	561	4.8	0.22	0.6	5733
Ol_2	1.20	559	9.8	0.33	1.8	1274
Ol_3	0.60	567	28.7	0.36	5.8	319

As previously explained, the incorporation of thin layer of p^+ material on hetero-junction semiconductors before coating with metal helps in reducing the R_s [24]. These results therefore show that pH variation of the chemical treatment solutions is another effective way of modifying the surface of the CdTe layer. The highest efficiency obtained in this experimental set was ~5.8% using a low pH of 0.60±0.02 for surface treatment. This treatment condition was further applied to solar cells of other device configurations such as the n-n-p and n-n-n multi-junction graded bandgap solar cells and solar cell efficiencies in the range (8.0-12.8)% were obtained.

9.10 Characterisation of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au solar cells

The effect of having a p-CdTe layer on n-n+SB device structures have been investigated and this will form the basis of discussion in this section. After the deposition of the n-n hetero-structure, the layer was removed from the CdTe deposition bath, rinsed with de-ionised water and dried with nitrogen gas before dipping it again into the CdTe electrolytic bath to grow a p-CdTe layer at a cathodic potential of 1350 mV. The introduction of a p-CdTe layer to glass/FTO/n-CdS/n-CdTe changes the device structure from a two-layer to multi-junction graded bandgap structure. The new device structure now becomes glass/FTO/n-CdS/n-CdTe/p-CdTe. The fabricated graded bandgap solar cells have two interfaces namely n-n hetero-junction interface and n-p homo-junction interface. Since the semiconductors forming the n-p homo-junction were made from the same material, it is expected that the lattice mismatch between them is zero or kept to

the barest minimum. Despite the lattice mismatch between CdS and CdTe thin films which is ~10%, the CdS/CdTe hetero-structure has been a good combination for excellent photovoltaic activity [25]. Since the deposition of p-CdTe on n-CdTe does not introduce additional lattice mismatch to the device structure, the new n-n-p device structure is therefore expected to perform better.

The deliberate introduction of p-layer to the n-n hetero-structure is also another effective means of pinning the Fermi level of the absorber material close to the valence band. If this is successfully achieved, it will lead to the creation of excellent band bending. A good band bending is synonymous to strong internal electric field in the solar cell structure and it allows electrons and holes to be separated and effectively transported across the device structure to external circuit where they are collected for current generation [26]. By so doing, the amount of photo-generated charge carriers recombining within the bulk of the material is minimised and this will lead to J_{sc} enhancement.

Table 9.4 gives the summary of solar cell parameters obtained from glass/FTO/n-CdS/n-CdTe/p-CdTe/Au solar cells. The thicknesses of the thin films used were ~150 nm, 1500 nm and 120 nm for n-CdS, n-CdTe and p-CdTe layers respectively. CP19-2B represents n-n-p device structures annealed ordinarily in air, CP19-2C represents n-n-p device structures treated with $CdCl_2$ before being annealed in air while CP19-2S are samples treated with mixture of $GaCl_3$+$CdCl_2$ before annealing in air. The samples described in Table 9.4 were originally part of the n-n hetero-structure samples summarised in Table 9.1; the main difference is that the samples were divided into two. The first part was left as n-n device structures (the results are shown in Table 9.1) while for the second part, a p-type CdTe with thickness of ~120 nm was grown on it to form n-n-p multi-junction graded bandgap device structures (the results are shown in Table 9.4). To be able to compare both results together, it is essential to use the same annealing temperature and time used for samples in Table 9.1. For this reason, annealing temperature and time of 450^{o}C and 10 minutes in air were used for the processing of the n-n-p device structures.

Table 9.4. Summary of n-n-p solar cell parameters obtained from device structures (glass/FTO/n-CdS/n-CdTe/p-CdTe/Au) annealed: ordinarily in air, in the presence of $CdCl_2$ and mixture of $GaCl_3$+$CdCl_2$. The highlighted sample ID denotes best cells for each of the three different conditions.

Samples		Measured Values per Unit Cell						Average Measured Values					
Sample Status	Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	R_s (Ω)	R_{sh} (Ω)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	R_s (Ω)	R_{sh} (Ω)
Annealed ordinarily in air	CP19-2B_31	520	15.8	0.40	3.3	839	7373	520	19.5	0.40	4.1	699	5898
	CP19-2B_12	520	22.1	0.37	4.3	710	5161						
	CP19-2B_23	520	20.5	0.42	4.5	548	5161						
Annealed with $CdCl_2$ in air	CP19-2C_33	560	26.2	0.41	6.0	436	3441	573	27.6	0.39	6.2	455	3193
	CP19-2C_34	580	26.8	0.40	6.2	445	3128						
	CP19-2C_32	580	29.7	0.37	6.4	484	3011						
Annealed with $GaCl_3$ + $CdCl_2$ in air	CP19-2S_45	520	41.1	0.38	8.1	210	1129	533	41.1	0.38	8.3	231	1312
	CP19-2S_46	520	41.0	0.39	8.3	226	1087						
	CP19-2S_48	560	41.1	0.37	8.5	258	1720						

The results stated in Table 9.4 show that the highest solar cell efficiency comes from n-n-p device structures that were annealed in an atmosphere of $GaCl_3$+$CdCl_2$. The average measured FF obtained for the different heat-treatment conditions are comparable ranging in-between 0.38-0.40. In these set of devices, R_{sh} seems not to have a great influence on the solar cell parameters most especially the FF. Even though samples labelled CP19-2B have the highest R_{sh} and FF while samples labelled CP19-2S have the lowest R_{sh} and FF, the difference between the FF's are not so obvious. The main focus of this section would be on the contributions made by the mixture of $GaCl_3$+$CdCl_2$ in reducing R_s and enhancing the J_{sc} and overall solar efficiency. As shown in Table 9.4, the device structures with the lowest R_s have the highest J_{sc} and solar cell efficiency; these have also been diagrammatically represented in Figure 9.6 (a-c). The J-V curves

of the best cells for each of the treatment conditions as explained in Table 9.4 are shown in Figure 9.7.

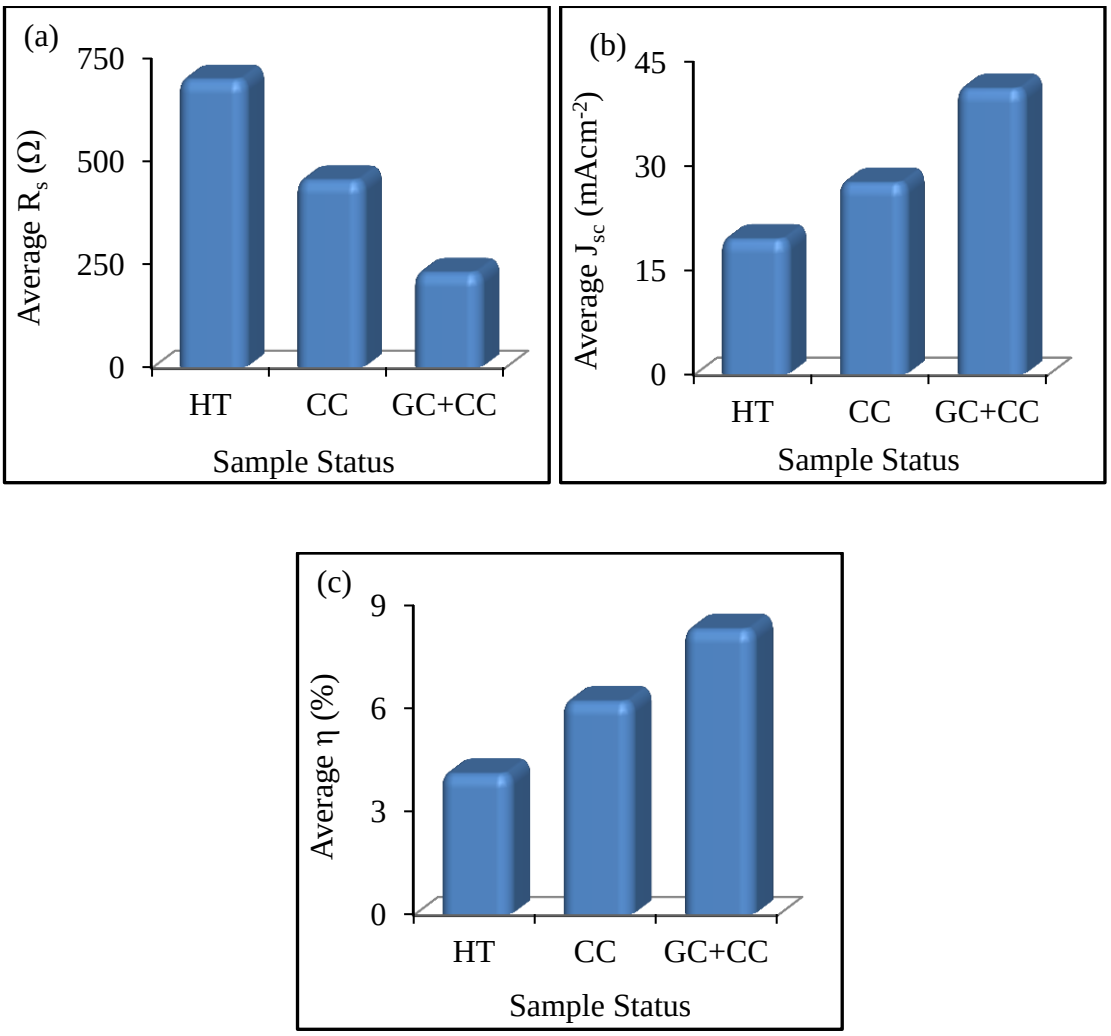


Figure 9.6. Typical diagrams explaining how the three different conditions affect (a) the series resistance, (b) the short-circuit current density and (c) the solar cell efficiency.

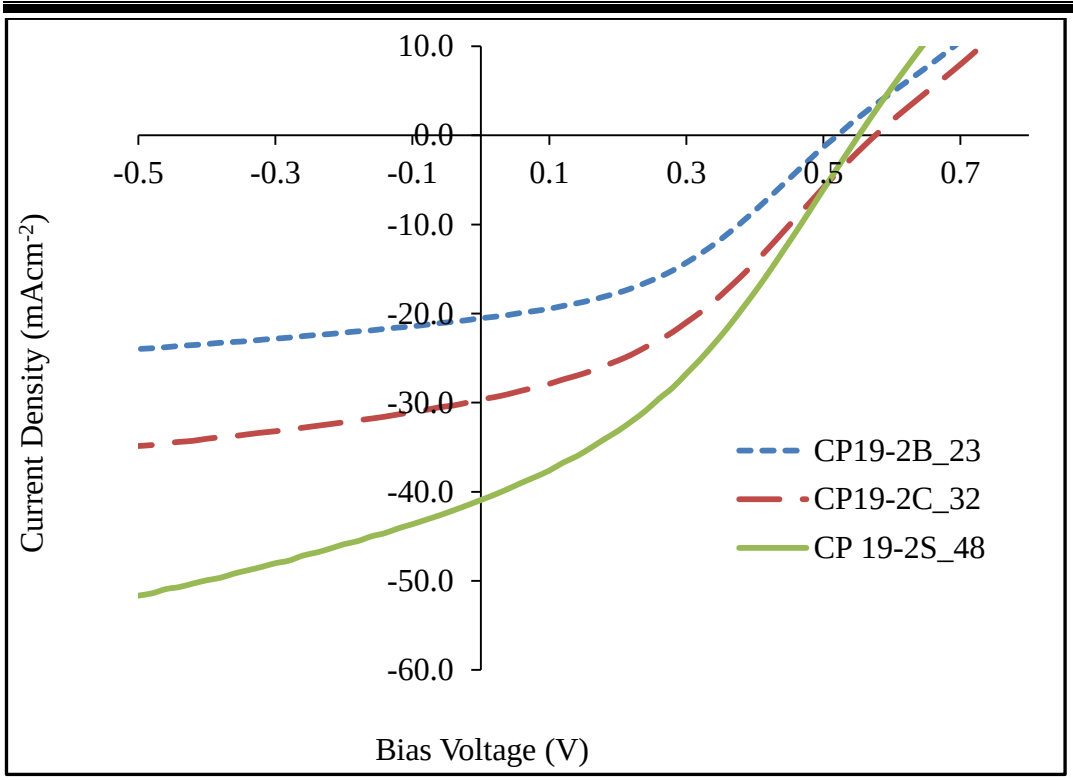


Figure 9.7. J-V characteristics of the best solar cells recorded in Table 9.4 for device structures annealed ordinarily in air (CP19-2B_23), with $CdCl_2$ treatment (CP19-2C_32) and with mixture of $GaCl_3$+ $CdCl_2$ treatment (CP19-2S_48).

9.11 Comparative study of n-n and n-n-p device structures annealed at 450^{o}C

Some of the average measured values of solar cell parameters for n-n and n-n-p were extracted from Table 9.1 and Table 9.4 and the results are tabulated in Table 9.5 for easy comparison. Under all treatment conditions, the n-n-p with p-CdTe of ~120 nm showed better electronic device quality than n-n device structures. The summarised results given in Table 9.5 are to show the trends and not necessarily the complete picture of the behaviour of n-n hetero-structure. The result however shows that 450^{o}C may not be suitable for n-n device structures while for device structures with p-CdTe layer (n-n-p), it might be appropriate to use higher annealing temperature. The results in Table 9.5 confirm the earlier investigations carried out in this research on the effect of annealing temperatures on electronic properties of CdTe thin films. The details of this investigation have been discussed in Chapter 8 and it simply reveals that n-CdTe have the least resistivity and highest mobility at 400^{o}C while at 450^{o}C, the least resistivity and highest mobility were observed in p-CdTe. Due to this, it is expected that the n-CdTe layers and p-CdTe layers would display optimum electronic performance at

annealing temperatures of 400^{o}C and 450^{o}C respectively when used in solar cells fabrication. It should be recalled that by lowering the annealing temperature of the n-n hetero-structure from 450^{o}C (see Table 9.1) to 400^{o}C (see Table 9.2), improvement was seen in the solar cell efficiency. Results from other experimental investigations that are not reported in this thesis also show that 400^{o}C is an appropriate annealing temperature for solar cell device structures having n-CdTe as an absorber layer.

Table 9.5. Summary of the average measured values of results from Table 9.1 and Table 9.4 demonstrating the adverse effect of higher annealing temperature (450^{o}C) on n-CdTe absorber layer.

Device structures with treatment conditions		Average measured values			
Device structure	Sample status	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF	η (%)
n-n	Annealed ordinarily in air	350	3.7	0.22	0.29
	Annealed with $CdCl_2$ in air	273	12.9	0.27	0.95
n-n-p	Annealed ordinarily in air	520	19.5	0.40	4.1
	Annealed with $CdCl_2$ in air	573	27.6	0.39	6.2

9.12 Effect of variation in thickness of p-CdTe layer on glass/FTO/n-CdS/n-CdTe/p-CdTe/Au solar cells efficiency

The incorporation of thin layer of p^{+} semiconductor material on hetero-junction semiconductors before coating with metal have been seen as means of reducing the R_s [24] and enhancing the barrier height [9]. The application of contact materials that can bring the Fermi level close to E_{Vmax} also helps to reduce the R_s. One of such materials is Cu metal; if a metal contact such as Au is alloyed with a small quantity of Cu and used as a back metal contact to CdTe, the Fermi level will be brought near E_{Vmax} due to the presence of Cu which is a p-type dopant of CdTe. This will then form a low resistance contact when the Fermi level is pinned close to E_{Vmax} [27]. Woodcock et al. [28] explained that if the CdTe top surface is modified in such a way that Te content is higher than Cd content before back contact deposition; the contact resistance will be reduced. A reduction in contact resistance will also help in minimising the series resistance since contact resistance is one of the factors that influence R_s [18]. As reported by Rohatgi et al. [18], etching the top surface with saturated dichromate etchant can assist in reducing the R_s which comes from Schottky contact. This is

because the acidic etchant attacks Cd preferentially and makes the CdTe top surface to be Te-rich [6]. If the R_s is successfully minimised, it will lead to enhancement in J_{sc}.

Another possible way of achieving the explanation given by Woodcock et al. [28] is to deposit a Te-rich p-type CdTe layer on the n-n+SB device structures. It is expected that this will reduce the resistance between the metal contact and CdTe thin films. Also, it is another possible way of deliberate positioning of the Fermi level close to the valence band. When the Fermi level is brought close to the E_{Vmax}, higher barrier height is expected to be formed under an ideal condition. However, the ideal situation may not always exist due to the defects introduced when the p-CdTe layer is grown in the Te-rich region. For this reason, it is of utmost importance to optimise the thickness of the p-CdTe layer that would be deposited on the n-CdTe so as to avoid Te-related defects [26]. As later seen in the reports presented in this work, it is important that the bulk of the material remains n-type while modifying the top surface to be p-type in electrical conduction. With the n-n+SB device structure, the Fermi level can also be pinned at any of the defect levels close to the valence band via post-growth treatments (see Figure 9.8 (a)) [6].

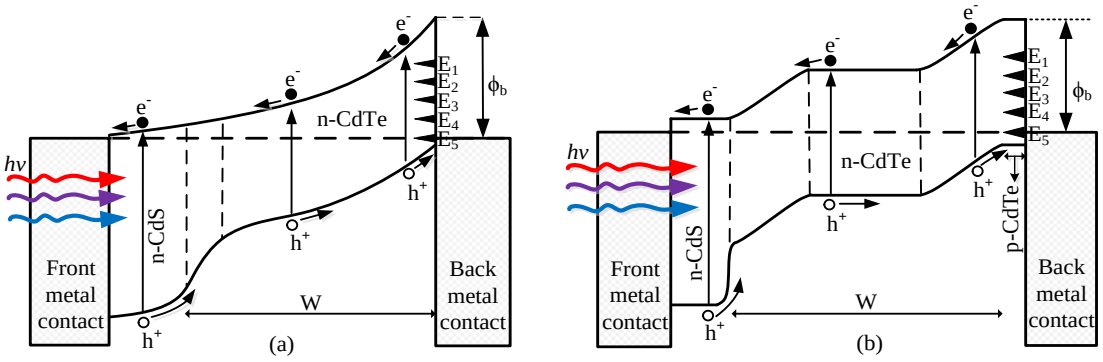


Figure 9.8. Energy band diagrams showing the different defect levels for (a) n-n+SB device structure and (b) n-n-p device structure.

The growth of p-layer on glass/FTO/n-CdS/n-CdTe/ device structures entirely changes the electronic properties of n+n+SB device structures. Apart from causing the Fermi level position to move towards the E_{Vmax}, the deposition of p-layer on glass/FTO/n-CdS/n-CdTe device structures also forms multi-junction graded bandgap solar cells which improve the slope of the energy band diagram as illustrated in Figure 9.8 (b). The main electrical contacts to n+n+SB are the front ohmic and back Schottky contacts. Due

to the Schottky diode formation between the metal and semiconductor interface, depletion region are formed at the M/S interface and extends into the bulk of the material as shown in Figure 9.8 (a). For the n-n-p device structure, ohmic contacts are formed at the front and back of the semiconductors. The depletion region formed therefore extends from the n-n to n-p interface as illustrated in Figure 9.8 (b).

9.12.1 Current-voltage (I-V) measurement technique

n-n+SB device structure indicated as D_4 in Table 9.6 was first developed and briefly studied using I-V measurement technique before the deposition of p-type CdTe layer. The summary of the results are presented in Table 9.6.

Table 9.6. Summary of I-V parameters obtained for n-n+SB (glass/FTO/n-CdS/n-CdTe/Au) and n-n-p (glass/FTO/n-CdS/n-CdTe/p-CdTe (different thicknesses)/Au device structures.

Thickness, L (nm)	0 (D_4)	35 (D_3)	150 (D_2)	1200 (D_1)
	I-V measured parameters under dark condition			
RF	$10^{2.1}$	$10^{4.0}$	$10^{0.3}$	$10^{0.0}$
n	2.21	1.58	4.10	6.91
I_s (A)	15.9×10^{-9}	7.9×10^{-9}	63.1×10^{-6}	158.5×10^{-6}
ϕ_b (eV)	>0.73	>0.75	>0.52	>0.49
R_s (Ω)	4082	414	478	798
R_{sh} (Ω)	0.79×10^{6}	8.81×10^{6}	1259	848
	I-V measured parameters under AM1.5 illumination condition			
V_{oc} (mV)	560	640	560	330
J_{sc} (mAcm^{-2})	26.6	37.0	38.0	28.1
FF	0.38	0.46	0.35	0.25
η (%)	5.7	10.9	7.5	2.3
R_s (Ω)	591	388	414	477
R_{sh} (Ω)	5955	6365	1697	382

The thicknesses of the n-CdS and n-CdTe layers used in the fabrication of n-n+SB device structures were ~150 nm and ~1200 nm respectively. The n-n+SB device structures possess rectifying ability with a rectification factor of $10^{2.1}$ when measured under dark condition. Under dark condition, the Schottky diode has high R_s of 4082 Ω and ideality factor in excess of 2.00. As explained by Li et al. [29], when metals are used as back contacts to CdTe, they form large Schottky barriers with high contact

resistance. The high contact resistance introduced between metal and semiconductor interface may be one of the reasons for the observed high R_s value in n-n+SB device structures [18] under dark condition. The large n value indicates the presence of large number of defects which act as electron traps in the device structure. Tunnelling through the device and presence of high R_s as seen in the fabricated Schottky diodes are other possible factors that can cause n value to exceed 2.00 [30]. Once electrons are trapped in the device structure, there will be loss of current; the leakage current is ~15.9 nA as stated in Table 9.6. The presence of large n value however underestimates the barrier heights of the n-n+SB device structures. Figure 9.9 (a) and 9.9 (b) illustrate the log-linear and linear-linear IV curves of the n-n+SB diodes respectively. Under illumination, a decrease was observed in the R_s value from ~4082 Ω to ~591 Ω. This behaviour further explains the photoconductivity of the fabricated Schottky diodes under illumination. The total efficiency obtained for this device structure as stated in Table 9.6 was ~5.7%.

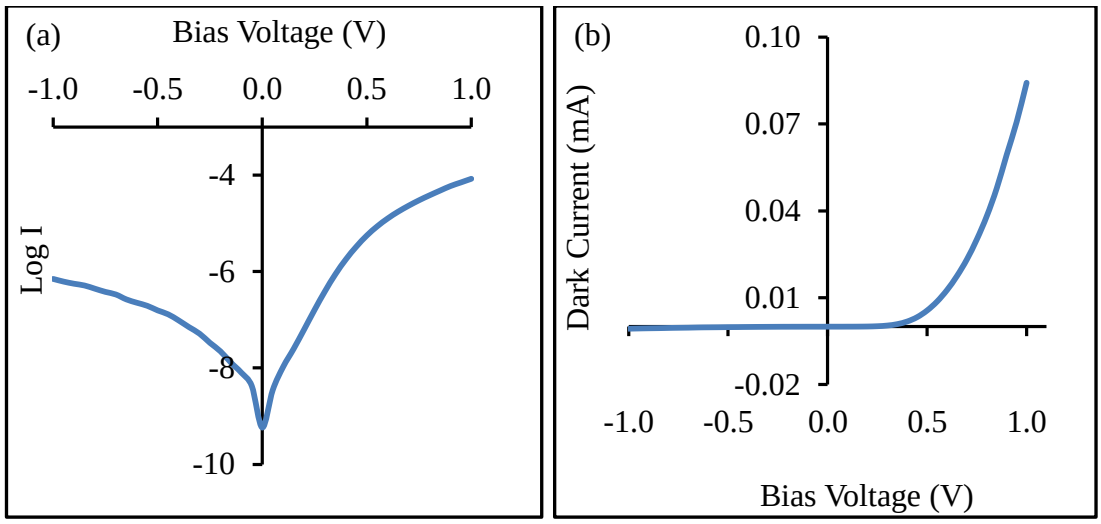


Figure 9.9. I-V characteristics of glass/FTO/n-CdS/n-CdTe/Au (n-n+SB) device structures under dark condition plotted in (a) Log-linear and (b) Linear-linear scales.

To study the effect of thickness of p-CdTe on n-n+SB device structures, three different thicknesses (~1.2 µm, 150 nm and 35 nm) of p-CdTe layers were used. The results obtained from the I-V characteristics have been summarised in Table 9.6. As seen in Table 9.6, under dark and illumination conditions, the incorporation of p-CdTe layer has helped in reducing series resistance of the n-n-p device structure as compared to the n-n+SB device structure. Under both measurement conditions, the n-n-p device structure with p-CdTe thickness of ~35 nm showed the least R_s. This is a good indication that the

incorporation of p-CdTe layer to the n-n+SB device structure helps in lowering the R_s of the initial n-n+SB device structure under both dark and illumination conditions. Table 9.6 further shows that as the thickness of the p-CdTe layers reduce, the R_s and R_{sh} measured under dark condition decreases and increases respectively. Since the sets of device structures discussed here are modified p-n junctions (that is, n-n-p), it is expected that the three structures possess rectifying ability when measured under dark. As illustrated in Figure 9.10, for the diode structure labelled 'p-CdTe (~1200 nm) or D_1', the p-CdTe has same thickness with n-CdTe (~1200 nm) and it showed an ohmic response under dark condition while for the diode labelled 'p-CdTe (~35 nm) or D_3', the p-CdTe thickness is ~35 nm and it exhibited a good diode response. Diode denoted as 'p-CdTe (~150 nm) or D_2' with p-CdTe thickness of ~150 nm showed a non-linear response and the I-V characteristic behaviour of D_2 lies in between D_1 and D_3.

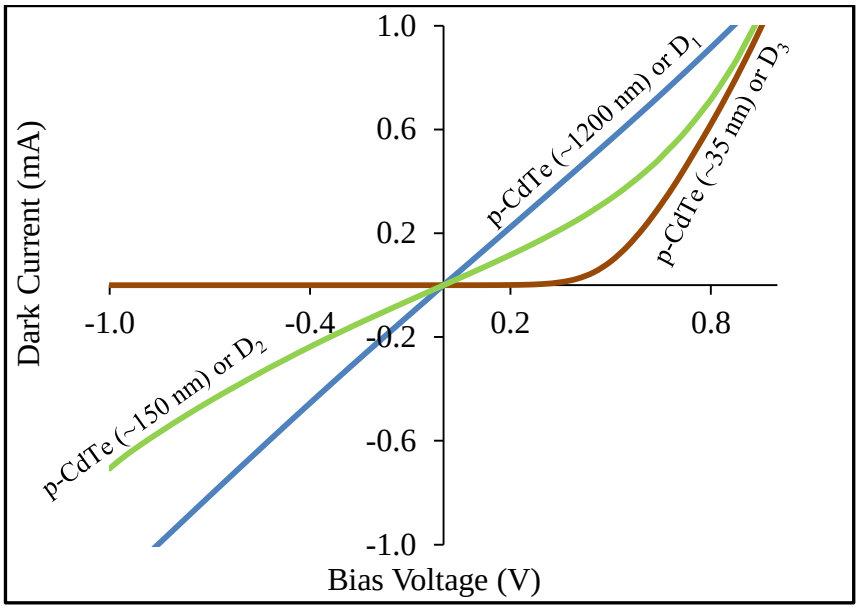


Figure 9.10. Linear-linear I-V characteristics of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p) device structures under dark condition with emphasis on variation of thickness of p-CdTe layers.

The log-linear I-V characteristics of diodes D_1, D_2 and D_3 are described in Figure 9.11 (a), 9.11 (b) and 9.11 (c) respectively. Diode D_1 has zero *RF* due to its ohmic behaviour. The *RF* of D_2 is very poor due to the non-ohmic or poor Schottky response observed while D_3 has the best *RF* as a result of its good Schottky behaviour. The perfect linear response of D_1 can be mainly attributed to the large thickness of the p-CdTe layer. The high thicknesses of p-CdTe layers promote the defects in the device structure; these defects come mainly from the excess Te in the p-CdTe layer. The effect of these defects

can be seen in the high value of ideality factor (n=6.9 for diode D_1 and 4.1 for diode D_2). Diode with large n value usually exhibit low R_{sh} and large leakage current. This is why Diode D_1 has the largest leakage current in order of microamperes while D_3 has the least leakage current in the order of nanoamperes. The low n value obtained in D_3 indicates that the level of recombination and generation centres in the n-n-p multi-junction solar cells have been minimised with reduced thickness of p-CdTe layer.

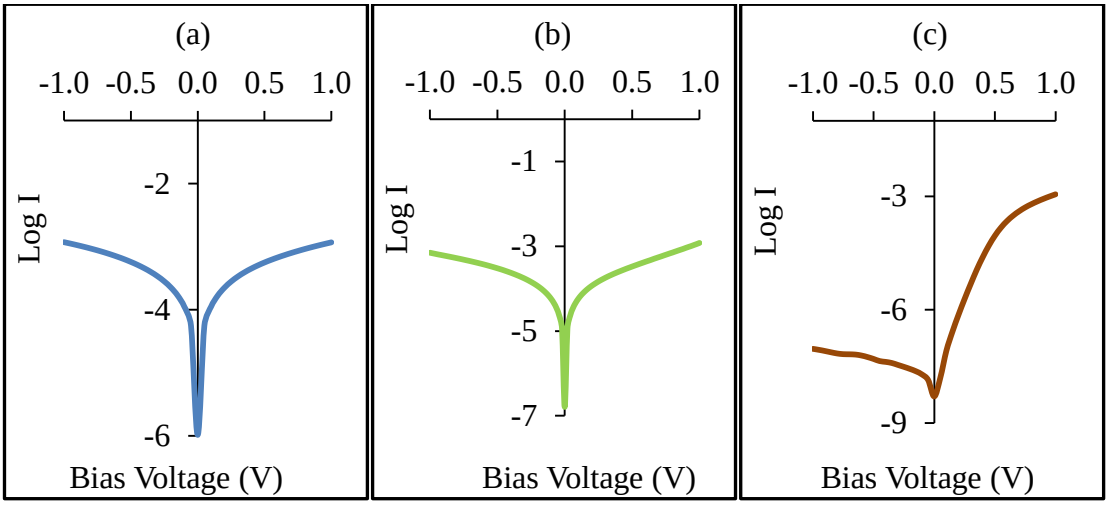


Figure 9.11. Log-linear I-V characteristics of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p) device structures under dark condition for (a) p-CdTe of ~1200 nm thickness (D_1), (b) p-CdTe of ~150 nm (D_2) and (c) p-CdTe of ~35 nm thickness (D_3).

The V_{oc} depends on the potential barrier height (ϕ_b). The ϕ_b is a function of the pinning position of the Fermi level and it can also depend on the I_s. Five defect levels have been identified to exist within the bandgap of CdTe below the conduction band minimum [26]. The positions of the 5 defect levels as reported by Dharmadasa et al. [6,26] are: E_1=0.40±0.04, E_2=0.65±0.02, E_3=0.73±0.02, E_4=0.96±0.04 and E_5=1.18±0.02 eV. Depending on the CdTe preparation and post growth treatment, the Fermi level can pin at any of these defect levels. As explained by Dharmadasa et al. [26], the band bending will be minimal if the condition under which the CdTe is prepared favours the pinning of Fermi level at E_1. From the results of V_{oc} and ϕ_b of D_1 given in Table 9.6, the band bending at the interface between the n-CdTe and p-CdTe will be minimal. This would lead to generation of weak electric field within the depletion region and production of solar cell with very poor efficiency as seen in diode D_1 under illumination (efficiency of D_1 is ~2.3% as stated in Table 9.6). The comparable J_{sc} values between D_2 and D_3 is possibly due to the fact that the band bending for these two diodes is sufficient to collect

the photo-generated charge carriers on both sides of the external circuits [31]. As explained by Dharmadasa et al. [31], pinning the Fermi level at E_2 (just below E_3 defect level) can result to low V_{oc} and high J_{sc}. The high J_{sc} comes when the E_3 defect level is filled and once this happens; there would be a drastic reduction of R&G activities which is dominant at E_3 defect level. Researchers have shown that defect levels E_1, E_2 and E_3 are common for CdTe layers that are Te-rich while E_4 and E_5 defect levels are dominant for CdTe thin films that are rich in Cd [6,26,32]. Using the results of the ϕ_b obtained in this work, it can be inferred that the Fermi level pinning of the three diodes were determined by defect levels E_1-E_3. These are defect levels associated with Te-rich CdTe layer. The Te-richness is likely to arise from the topmost p-CdTe grown on n-CdTe layer. The band diagram showing the defect levels and the likely pinning position of the Fermi level for diode D_3 is illustrated in Figure 9.12.

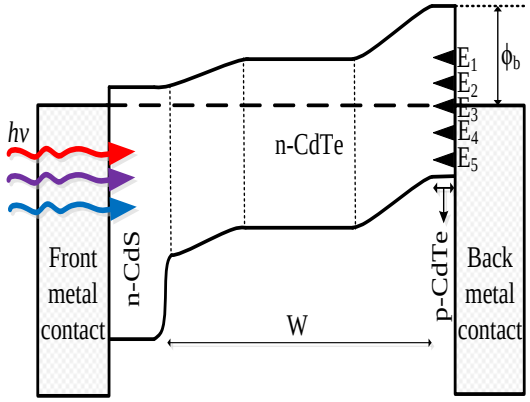


Figure 9.12. Energy band diagram showing the different defect levels and the likely pinning position of the Fermi level for n-n-p device structure with p-CdTe of ~35 nm thicknesses (D_3).

The J-V characteristic curves of the n-n+SB and n-n-p device structures are shown in Figure 9.13. The n-n+SB J-V curve is included in Figure 9.13 since it serves as the reference for comparison with the n-n-p J-V curves. As seen in Figure 9.13, the J-V characteristics of D_1 under illumination exhibited a very poor FF when compared to the others. The poor FF comes mainly from low R_{sh} observed in D_1 while the improved FF observed in D_3 arises from low R_s and large R_{sh} values. The solar cells efficiencies obtained for D_1, D_2 and D_3 are ~2.3, 7.5 and 10.9% respectively while the cell efficiency for the n-n+SB is ~5.7%. These results show that the thickness of the p-CdTe

layer deposited on the n-CdTe layer greatly influences the electronic properties of the n-n-p multi-junction solar cells.

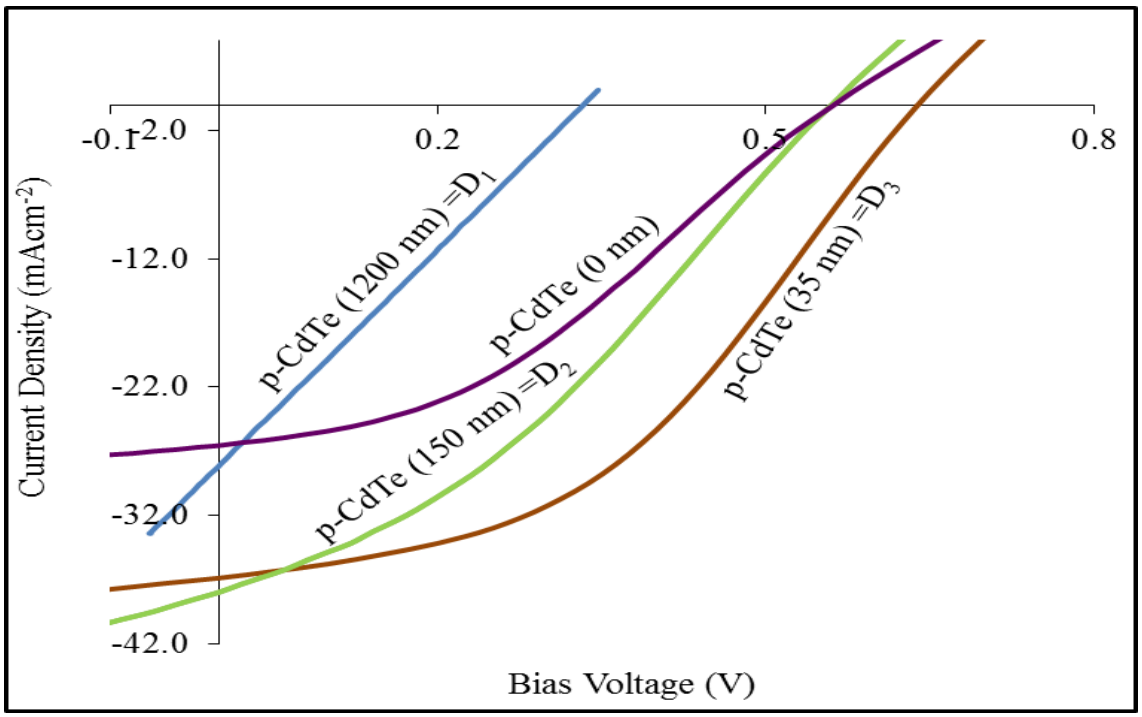


Figure 9.13. J-V characteristics of glass/FTO/n-CdS/n-CdTe/Au {n-n+SB or p-CdTe (0 nm)} and glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p) device structures under illumination condition with emphasis on different thicknesses of p-CdTe layers.

Based on the experimental results obtained in this work, the thickness of the p-CdTe thin films should be kept to the barest minimum so as to achieve highest solar-to-electric conversion efficiency. It should also be noted that the Fermi level pinning position of these diodes differ from one another due to the differences in the thickness of the p-CdTe layer. Therefore, when employing the n-n-p multi-junction device structure for solar cells fabrication, there is need to further optimise the thickness of the p-CdTe so as to obtain optimum efficiency.

9.12.2 Capacitance-voltage (C-V) measurement technique

The C-V technique was used to find the doping density of the fabricated device structures. The C-V and Mott-Schottky plots of the n-n+SB device structures are shown in Figure 9.14 (a) and 9.14 (b) respectively. The depletion capacitance (C_o) was estimated from Figure 9.14 (a) as 366 pF; using Equation (3.38), the depletion width, *W* was estimated to be 836 nm. The doping density of the n-n+SB hetero-structure was

estimated as 2.08×10^{16} by substituting the slope of the Mott-Schottky plot in Figure 9.14 (b) into Equation (3.35). The ratio of the depletion width to the thickness of the absorber layer (W:L) was estimated as ~0.70. The details of parameters obtained from C-V and Mott-Schottky plots are tabulated in Table 9.7.

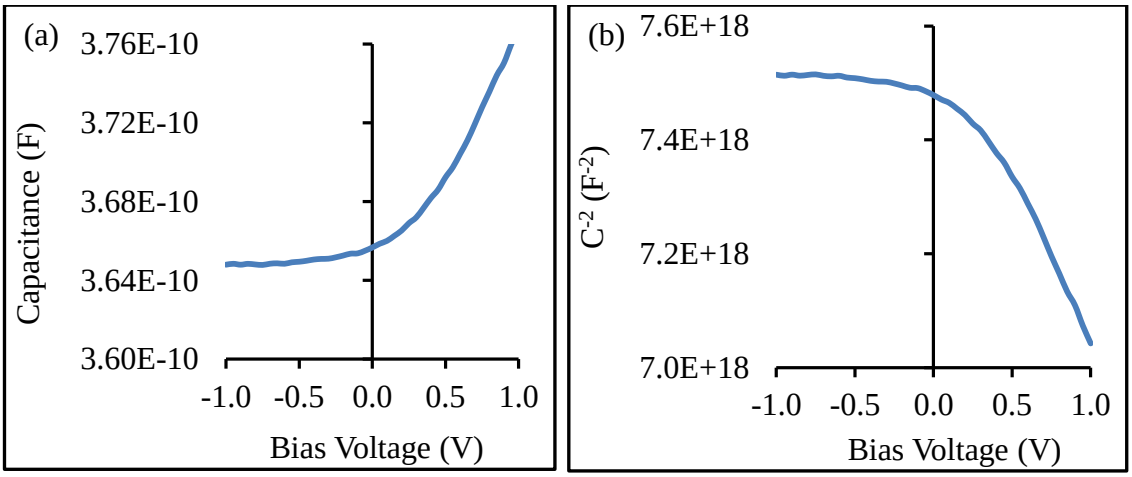


Figure 9.14. (a) Capacitance-voltage plot and (b) Mott-Schottky plot of n-n+SB device structure under dark condition.

Table 9.7. Summary of C-V parameters obtained for n-n+SB (glass/FTO/n-CdS/n-CdTe/Au) and n-n-p (glass/FTO/n-CdS/n-CdTe/p-CdTe (different thicknesses)/Au device structures.

Thickness, L (nm)	0 (D_4)	35 (D_3)	150 (D_2)	1200 (D_1)
	C-V measured parameters under dark condition			
C_o (pF)	366	491	487	354
W (nm)	836	623	628	864
W:L_e	0.70	0.50	0.47	0.36
Doping density (cm^{-3})	1.73×10^{16}	4.71×10^{15}	8.85×10^{15}	2.47×10^{16}
E_F-E_V (eV)	1.34	0.15	0.14	0.11
E_C-E_F (eV)	0.10	1.29	1.30	1.33

The C-V plots of the n-n-p device structures denoted as D_1, D_2 and D_3 are described using Figure 9.15 (a), 9.15 (b) and 9.15 (c) respectively. The C_o values obtained from these C-V plots are stated in Table 9.7. The corresponding widths were calculated by substituting the C_o values into Equation (3.38). Comparing the three widths of D_1 to D_3 together, n-n-p device structure labelled D_1 has the largest width while D_3 has the lowest depletion width. As earlier discussed, a wider depletion width is required for

solar cell to be efficient. However, it is also important to stress here that the depletion width must be healthy and not full of defects. If the depletion region is wide and full of defects as seen in D_1, the solar cell efficiency would be low because the electrons and holes generated within the depletion region will recombine again within the device structure and this will lead to loss of photo-generated currents. Since different thicknesses of p-CdTe layers are used in this investigation, it would be more appropriate and accurate to relate the width to the total thickness of the absorber layers. The effective absorber layer thickness (L_e) is the summation of the thickness of n-CdTe and p-CdTe used in this work. D_3 has the highest $W:L_e$ ratio and best efficiency when compared to D_1 and D_2. Comparing D_3 with n-n+SB device structures, n-n+SB has a larger $W:L_e$ ratio than D_3. The solar cell efficiency obtained in n-n+SB is however smaller than that of D_3; this is because there are more defects and leakage currents in n-n+SB as seen from the values of n, I_o and R_{sh} in Table 9.7.

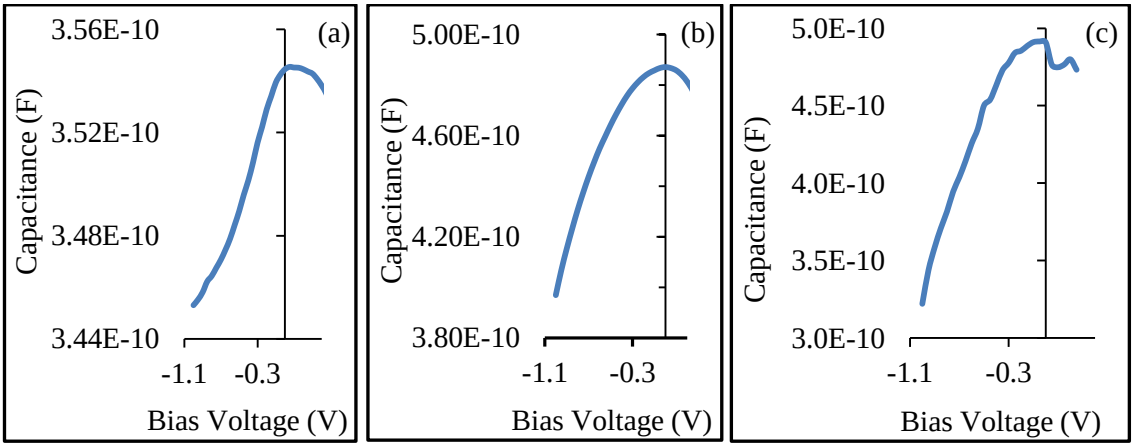


Figure 9.15. C-V plots of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p) device structures under dark condition at room temperature for (a) p-CdTe of ~1200 nm thickness (D_1), (b) p-CdTe of ~150 nm (D_2) and (c) p-CdTe of ~35 nm thickness (D_3).

Mott-Schottky plots used for the estimation of doping densities for D_1, D_2 and D_3 are shown in Figure 9.16 (a), 9.16 (b) and 9.16 (c) respectively. Other parameters such as the doping density and Fermi level positions obtained from C-V measurements for D_1, D_2 and D_3 are summarised in Table 9.7. The results from Table 9.7 explain that as the doping density increases from the order of 10^{15} to 10^{16} cm^{-3}, the solar cell efficiency reduces. This illustrates that there is an optimum doping density for solar cells to perform more efficiently.

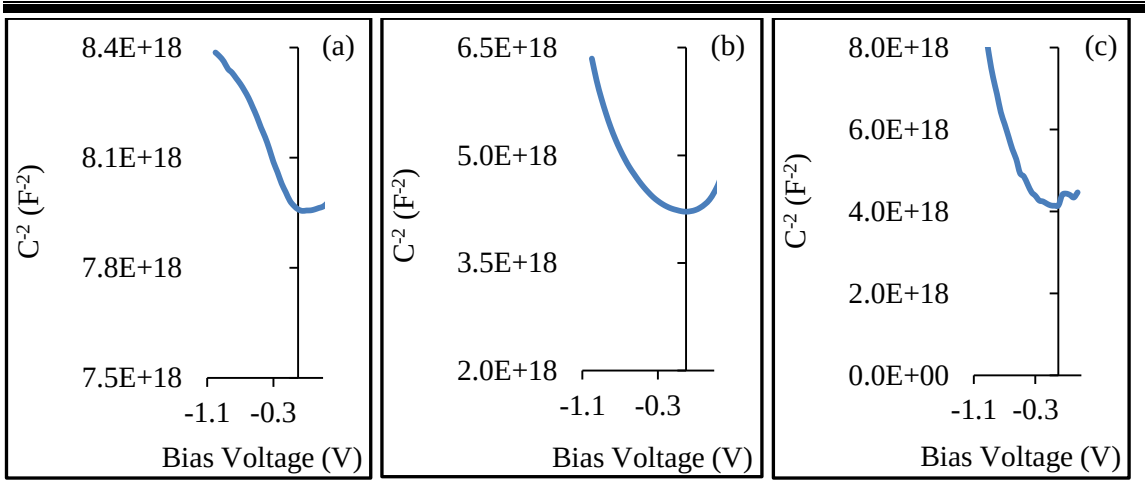


Figure 9.16. Mott-Schottky plots of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p) device structures under dark condition at room temperature for (a) p-CdTe of ~1200 nm thickness (D_1), (b) p-CdTe of ~150 nm (D_2) and (c) p-CdTe of ~35 nm thickness (D_3).

9.13 Characterisation of n-n-p solar cell device structures with other p-type semiconductors

Other p-type semiconductors such as p-ZnTe and p-CdMnTe were also used as back layers to n-CdS/n-CdTe device structures; the obtained results for some of the measured cells are summarised in Table 9.8. As seen in Table 9.8, the n-n-p device configurations with p-ZnTe as back layer demonstrate higher V_{oc} and FF than when using n-n-p device configurations with p-CdMnTe as back layer. The main shortcoming of the glass/FTO/n-CdS/n-CdTe/p-ZnTe/Au solar cell device structure is the low J_{sc} as seen in the solar cell parameters of Table 9.8. On the other hand, n-n-p device configurations with p-CdMnTe as back layer possess poor FF and low V_{oc} while the J_{sc} is exceptionally high when compared to the n-n-p device configurations with p-ZnTe as back layer.

Table 9.8. Solar cell parameters obtained from n-n-p device configurations with ZnTe and CdMnTe as p-layers.

glass/FTO/n-CdS/n-CdTe/p-ZnTe/Au					**glass/FTO/n-CdS/n-CdTe/p-CdMnTe/Au**				
Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
Olu_P9_13	520	6.6	0.42	~1.4	Olu_P10_35	350	30.3	0.27	~2.8
Olu_P9_22	590	10.0	0.40	~2.4	Olu_P10_25	402	26.0	0.27	~2.9
Olu_P9_24	590	10.4	0.40	~2.5	Olu_P10_36	393	29.4	0.27	~3.1

Even though it may not be right to conclude at this stage with these preliminary results; the results in Table 9.8 however point to the fact that if another ternary compound semiconductor which is CdZnTe is being made used of as a back layer to n-CdTe thin films, there is the chance of all solar cell parameters to be enhanced. The J-V characteristic curves of the best solar cells for glass/FTO/n-CdS/n-CdTe/p-ZnTe/Au and glass/FTO/n-CdS/n-CdTe/p-CdMnTe/Au given in Table 9.8 are illustrated in Figure 9.17 (a) and 9.17 (b) respectively.

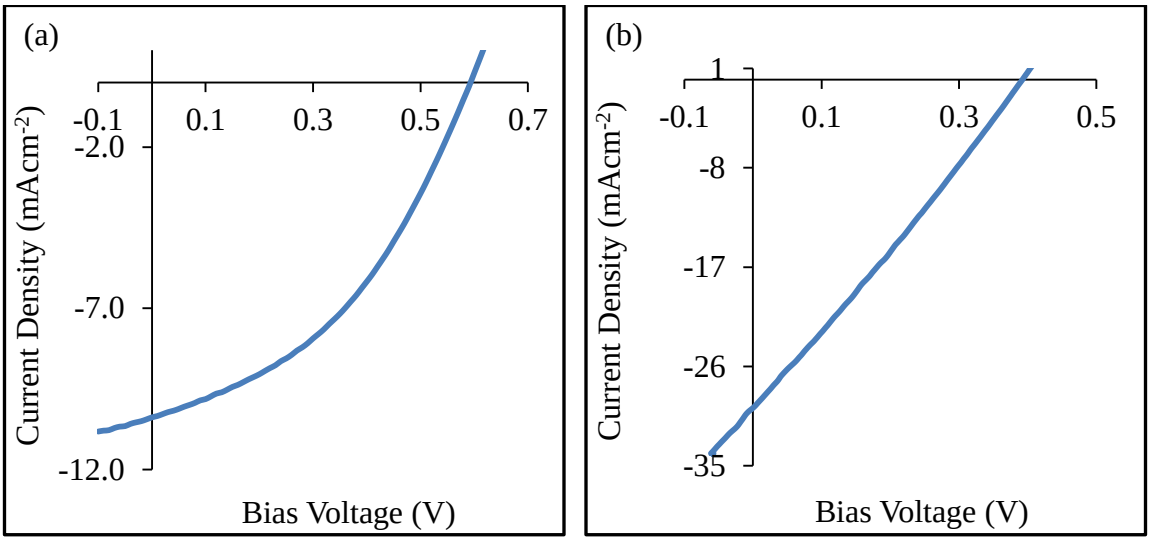


Figure 9.17. Typical J-V curves obtained for solar cells fabricated from (a) glass/FTO/n-CdS/n-CdTe/p-ZnTe/Au device structures and (b) glass/FTO/n-CdS/n-CdTe/p-CdMnTe/Au device configurations.

9.14 Characterisation of n-n-n+Schottky barrier solar cell device structures

CdS has been a suitable window layer to CdTe-based solar cells [33] and researchers working on photovoltaic (PV) materials have identified some factors which cause a reduction in the CdS/CdTe solar cell efficiency. One of the identified factors which cause a reduction in the efficiency of CdS/CdTe based solar cell is the formation of pinholes [34]. Non-uniformity of the CdS window layer can lead to the formation of pinholes after annealing. This non-uniformity is mostly experienced when the CdS layer is very thin ~(40-80) nm. Thus, the presence of pinholes will create shunting paths within the device structure. These unwanted shunting paths cause a reduction in all three solar cell parameters and the overall solar cell efficiency. Therefore, to prevent the formation of pinholes on CdS layers after annealing, thicker CdS thin films (>200 nm) is needed. One major disadvantage of using thick CdS is that it causes the short circuit

current density (J_{sc}) to reduce under illumination [34,35]. To prevent further degradation of solar cell parameters such as the J_{sc}, V_{oc} and *FF* through the use of very thin CdS layer, a buffer layer with higher bandgap than that of CdS is needed as an intermediate layer between the conducting substrate and CdS window layer [36]. With the incorporation of buffer layer, the CdS thickness can still be maintained at thickness <200 nm without necessarily causing a loss in the V_{oc} and *FF*.

Semiconductor materials containing Zn element such as ZnO [37], ZnS [30], ZnSnO [36], are generally being preferred as buffer layers to CdS/CdTe solar cells due to their large bandgap and resistive nature; these two features are the main characteristic features of buffer layers. This therefore means that buffer layers must not have high conductivity; if they do, they will become extension of the conducting glass substrates [36,38]. As explained by Jonathan et al. [36], the V_{oc} can be lowered by high conductivity. A resistive layer will therefore be needed on FTO substrates to be able to increase V_{oc}. These resistive layers are called buffer layers and they allow the growth of CdS layers on them without resulting to any losses in solar cell performance [36].

In this section, two Zn-related binary compound semiconductors namely ZnTe and ZnS thin films have been used as buffer layers to CdS/CdTe solar cells. ZnTe has been used in this work due to its resistive nature. The actual bandgap of bulk ZnTe thin film is ~2.26 eV. For it to be useful as a buffer layer to CdS/CdTe based solar cells, there is need to tune the bandgap of ZnTe material to be higher than that of CdS. As earlier explained in section 5.4.3, the ZnTe E_g was tuned by controlling the growth time. Therefore, a growth time of ~15 minutes was used in this experiment to deposit ZnTe layers so as to achieve a suitable E_g of ~2.6 eV. Thus this higher E_g obtained makes the n-ZnTe layers suitable as buffer layers to CdS window layers. The n-ZnTe layers used for this investigation were grown at a cathodic potential of 1650 mV in the Zn-rich region [39]. This is in line with the experimental report given by Jonathan et al. [36] that high FF was observed with Zn-rich buffer layers. The ZnS layers used in this work were provided by a fellow researcher in the group and it has a thickness of ~100 nm and bandgap of ~3.70 eV. Full details of the ZnS material characterisation can be found in the work published by Madugu et al. [40].

9.14.1 Characterisation of glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au solar cells

The thicknesses of n-ZnTe, n-CdS and n-CdTe used in the glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au solar cell device structures were ~100 nm, 150 nm and 1200 nm respectively. Table 9.9 shows parameters of 4 measured cells in the glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au device configurations. The solar cells efficiencies range between (6.8 to 8.1)% as seen in Table 9.9.

Table 9.9. Solar cell parameters obtained from n-n-n+SB device structures fabricated from glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au solar cells.

	Measured values per unit cell				Average measured values			
Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
JZ69-1_21	600	22.8	0.50	6.8	610	26.1	0.48	7.6
JZ69-1_12	600	28.0	0.45	7.6				
JZ69-1_11	620	25.7	0.49	7.8				
JZ69-1_23	620	27.7	0.47	8.1				

For further analysis under dark condition, the best cell from Table 9.9 (JZ69-1_23) was selected. The log-linear and linear I-V characteristics of JZ69-1_23 are described in Figure 9.18 (a) and 9.18 (b) respectively while the J-V curve under AM1.5 illumination is shown in Figure 9.19. The obtained electronic parameters of JZ69-1_23 under dark and AM1.5 illumination conditions are summarised in Table 9.10. When the parameters of glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au stated in Table 9.10 are compared with the n-n+Schottky barrier in Table 9.6, it was observed that the n-n-n+SB fabricated from n-ZnTe/n-CdS/n-CdTe exhibited better diode and solar cell performance than n-n+SB device structures.

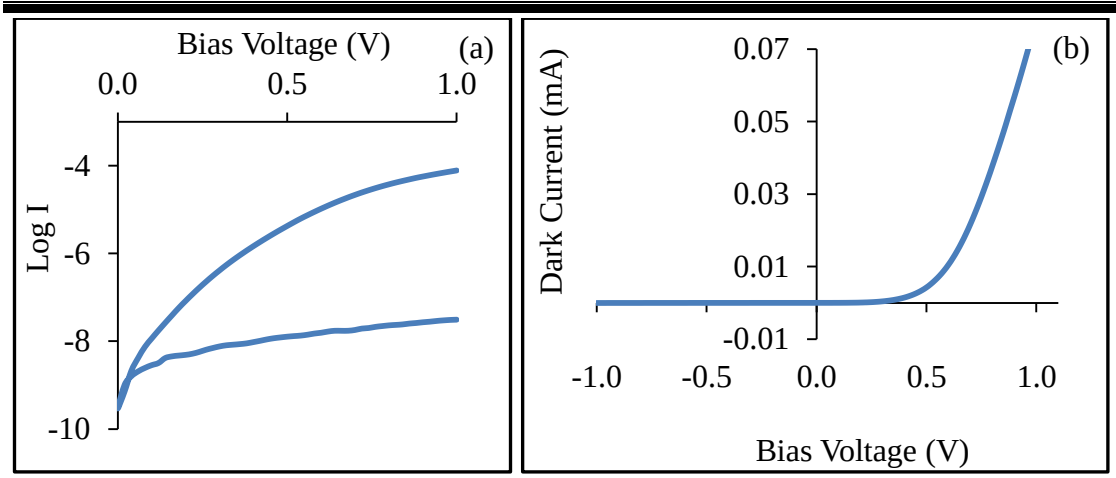


Figure 9.18. I-V characteristics of glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au (n-n-n+SB) device structures under dark condition plotted in (a) Log-linear and (b) Linear-linear scales.

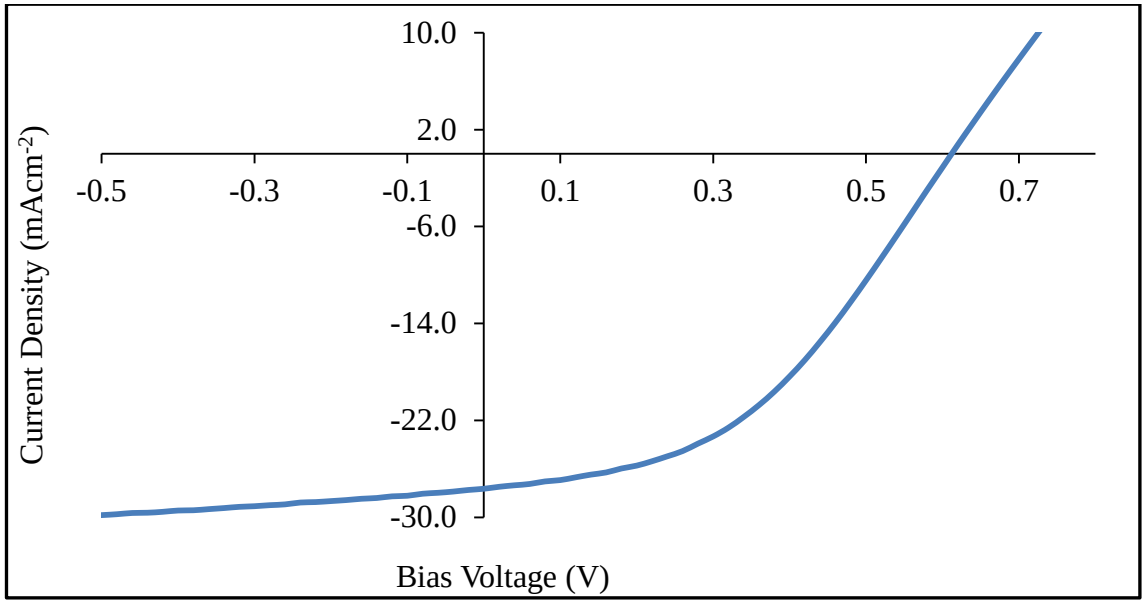


Figure 9.19. Typical J-V curve obtained for best solar cells fabricated from glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au device structures.

Table 9.10. Best solar cell parameters obtained from glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au device structures under dark and illumination conditions.

Under dark condition (JZ 69-1_23)						Under illumination (JZ 69-1_23)					
RF	*n*	ϕ_b (eV)	I_s (nA)	R_s (Ω)	R_{sh} (MΩ)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	*FF*	η (%)	R_s (Ω)	R_{sh} (Ω)
3.4	1.98	>0.78	2.51	4494	24.1	620	27.7	0.47	8.1	339	8871

9.14.2 Fabrication of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells

Three-layer device structures fabricated from n-n-n+Schottky barrier device structures are known to be more efficient in terms of solar-to-electric conversion efficiency than two-layer device structures fabricated from n-n+Schottky barrier [30]. The three-layer device structures discussed in this section were fabricated from glass/FTO/n-ZnS/n-CdS/n-CdTe solar cell device structure. The device structure is a combination of two n-n heterojunctions (HJ's) and a large Schottky barrier at the interface between the n-CdTe absorber layer and Au metal contact [27]. The results obtained from characterisation techniques such as PEC cell and optical absorption measurements discussed in the previous chapters are useful to obtain the actual energy band diagram of the device structure. The higher energy bandgap of ZnS thin films obtained from optical absorption measurements [40] makes the ZnS thin films suitable for use as a buffer layer to CdS/CdTe solar cells. With the higher bandgap of ZnS layer, pinholes can be minimised while bandgap grading is introduced to the device structure during heat treatments. The energy band diagram for n-n-n+SB device structure is shown in Figure 9.20.

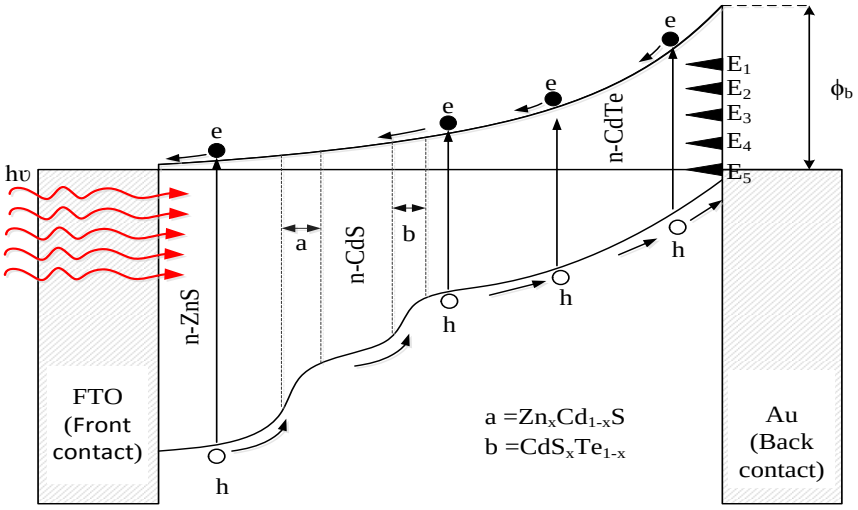


Figure 9.20. Energy band diagram of n-n-n+SB device structure showing the formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} as a result of interdiffusion of atoms at two different interfaces during annealing.

The formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} ternary compound semiconductors are illustrated in Figure 9.20. As explained by Echendu et al. [30], the formation of $Zn_xCd_{1-x}S$ at the interface between the ZnS/CdS HJ is due to the interdiffusion of Zn and Cd during annealing process. The same explanation applies to the formation of CdS_xTe_{1-x} at

the CdS/CdTe interface. Due to heat-treatment, S and Te interdiffuse to form CdS_xTe_{1-x}. Chu et al. [41] explained that treating the CdTe surface with $CdCl_2$ solution causes a reaction to take place at the interface between CdS and CdTe thin films thus producing a thin layer of CdS_xTe_{1-x}. According to Potter et al. [42], the formation of CdS_xTe_{1-x} alloy near the CdS/CdTe interface is being promoted through the $CdCl_2$ annealing process. Apart from ZnS functioning as a buffer layer, the incorporation of ZnS into the CdS/CdTe HJ likewise leads to the formation of graded bandgap device structure as described in Figure 9.20. Also, the formation of $Zn_xCd_{1-x}S$ and CdS_xTe_{1-x} tend to contribute to the bandgap grading of the device structure. Due to the graded bandgap structure, there is therefore a high tendency for this device structure to start absorbing high energy photons from the blue-end and low energy photons from the infrared region of the solar spectrum. This therefore maximises optical absorption from the solar spectrum, minimises thermalisation and improve collection of photo-generated charge carriers [43]. Since there is no p-layer in this device structure, the depletion region is therefore formed at the band bending created at the metal/semiconductor (n-CdTe/Au) interface. The depletion region provides a strong electric field to separate the photo-generated charge carriers created within the device structure. The fast separation of the photo-generated electrons and holes to the external circuit reduces the recombination of these charge carriers within the device structure. This therefore leads to generation of higher short circuit current density.

Due to the difference in the energy bandgap of these materials, the slope of the energy band diagram which represents the built-in electric field can be improved upon. Therefore, the formations of n-n HJ at the ZnS/CdS and CdS/CdTe interface also complement the creation of the built-in electric field within the device. The fabrication of rectifying n-n and p-p semiconductors have been well demonstrated by researchers in the field [44]. Due to the presence of defect states, it is difficult to have an ideal interface at the n-CdTe/Au contact. The existence of these states (shown as E_1 to E_5 in Figure 9.20) in the bandgap introduce strong pinning of the Fermi level and with an adequate surface processing of the absorber layer, the Fermi level can be pinned at E_5 which is close to the valence band (VB). Due to this Fermi level pinning effect, the potential barrier height is not always a dependant of the metal work function [6]. Existence of experimentally observed defect levels (E_1-E_5) is a real cause for reproducibility; and for high efficiency devices, Fermi level should be pinned at E_5 level closer to the valence band.

9.14.2.1 Characterisation of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells using current-voltage (I-V) technique

In solar cells fabrication, the thickness of the semiconductor material is of utmost importance. The thicknesses of n-ZnS, n-CdS and n-CdTe used in the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cell device structures were ~100 nm, 150 nm and 1200 nm respectively. Table 9.11 shows the parameters of 5 measured cells in the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device configuration under AM1.5 illumination condition. The efficiencies of the solar cells with an active area of ~0.031 cm^2 range from ~(9.1 to 12.8)% as seen in Table 9.11. For further analysis under dark condition, the best cell (MO1_5) was selected. The log-linear and linear-linear I-V characteristics of MO1_5 obtained under dark condition are shown in Figure 9.21.

Table 9.11. Measured solar cell parameters fabricated from glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures

	Measured values per unit cell				Average measured values			
Sample ID	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	FF	η (%)
MO1_1	640	35.7	0.40	~9.1	630	35.9	0.47	10.6
MO1_2	620	34.4	0.48	~10.2				
MO1_3	620	34.1	0.49	~10.4				
MO1_4	600	34.0	0.51	~10.4				
MO1_5	670	41.5	0.46	~12.8				

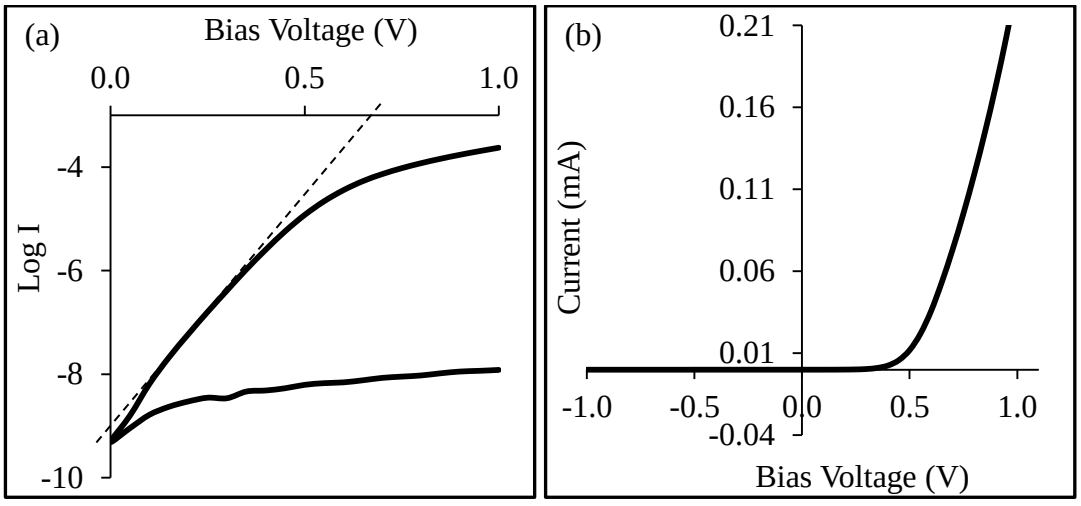


Figure 9.21. I-V characteristics of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au (n-n-n+SB) device structure under dark condition plotted in (a) Log-linear and (b) Linear-linear scales.

The parameters obtained from Log I vs V curve were: rectification factor (*RF*), ideality factor (*n*), reverse saturation current (I_s), potential barrier height (ϕ_b); from the linear-linear I-V curve, the series resistance (R_s) and shunt resistance (R_{sh}) were obtained from the high forward and reverse regions of the curve respectively. The J-V curve of MO1_5 under AM1.5 illumination is shown in Figure 9.22. The measured solar cell parameters of MO1_5 under dark and AM1.5 illumination conditions are summarised in Table 9.12.

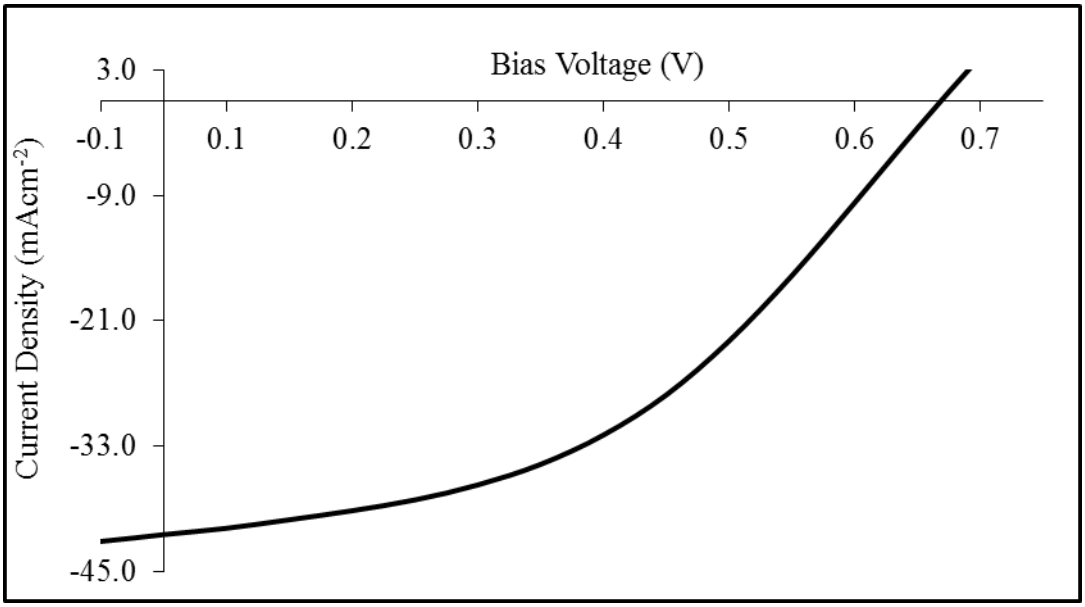


Figure 9.22. J-V characteristics of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells (n-n-n+SB device structure) under AM1.5 illumination condition.

Table 9.12. Parameters for best device measured from glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells under dark and illumination conditions.

Under dark condition (MO1_5)							Under illumination (MO1_5)					
RF	*Slope*	*n*	ϕ_b (eV)	I_s (nA)	R_s (Ω)	R_{sh} (MΩ)	V_{oc} (mV)	J_{sc} ($mAcm^{-2}$)	*FF*	η (%)	R_s (Ω)	R_{sh} (Ω)
$10^{4.3}$	11.03	1.52	>0.81	0.76	1250	81	670	41.5	0.46	12.8	134	3819

The *RF* obtained for diodes fabricated from n-n-n+SB device structure under dark condition is $10^{4.3}$. As reported by Dharmadasa [8], *RF* of $10^{3.0}$ is sufficient to obtain over 12% efficiency from the CdTe-based solar cells. For the CdTe-based solar cells with lower efficiency, it is therefore possible to have *RF* of lesser orders of magnitude as observed in a previous work [45]. The value of the ideality factor helps to determine

the type of current transport mechanism which takes place within the device structure. For the solar cells fabricated and reported in this work, the ideality factor of 1.52 was obtained. This shows that two current transport mechanisms (thermionic emission and recombination and generation (R&G) process) take place in parallel [8]. As reported by Rhoderick, n>1.00 due to carrier recombination [46]. When n>1.00, the ϕ_b is always being underestimated.

The I_s is obtained from the intercept of the straight line section of best tangent of the forward current curve on the Log I axis (Figure 9.21 (a)). The obtained I_s value is ~0.79 nA. This I_s value was used in estimating the barrier heights. The estimated ϕ_b for n-n-n+SB diode is >0.81 eV. The n value <2.00, high RF and larger ϕ_b obtained for n-n-n+SB diode illustrate how healthy the depletion width of the device structure is. It also shows the strength of the electric field produced in the depletion region. The healthy depletion region and strong electric fields work together to effectively separate and transfer the photo-generated electrons and holes to the external circuit. This explains the reason for the high J_{sc} observed in the n-n-n+SB device structures.

The R_s and R_{sh} values estimated from linear-linear dark I-V curve (see Figure 9.21 (b)) of n-n-n+SB device structure are ~1250 Ω and 81 MΩ respectively. The shape of the reverse curve of diode in Figure 9.21 (b) showed infinite R_{sh}. The incorporation of ZnS as a buffer layer in to the n-CdS/n-CdTe device structure leads to a great improvement in the R_{sh} when compared to the R_{sh} obtained for glass/FTO/n-CdS/n-CdTe/Au device structures without ZnS buffer layer (see n-n+SB device structure in Table 9.6). The presence of large R_{sh} indicates that the leakage paths for the photo-generated charge carriers are minimised; therefore, the amount of current loss through the leakage path is reduced and the current that flows through the external circuit will increase and this eventually leads to an improvement in the cell performance. With reduced leakage current paths, an improvement in the J_{sc} is expected. This improvement was observed in the experimental work with n-n-n+SB device structures.

The solar cell parameters of MO1_5 (n-n-n+SB solar cells) carried out at room temperature under AM1.5 illumination condition as stated in Table 9.12 comprises of the following parameters: V_{oc} = 670 mV, J_{sc} = 41.5 mAcm^{-2}, FF = 0.46 and η = ~12.8%. The estimated R_s and R_{sh} under light are ~134 Ω and ~3819 Ω respectively. The reduction of the R_s from ~1250 Ω under dark condition to ~134 Ω under AM1.5 illumination condition shows that the fabricated solar cell has a good photo conductivity

effect. The low R_s value also helps in enhancing the J_{sc} value. Some of the other possible reasons for high J_{sc} value are given in the next section. Also the larger bandgap of ZnS (~3.70 eV) in the front of the device structure has assisted in creating a steep slope to ease the transportation of electrons to the front contact. In this device structure, all three layers are active in PV conversion and the thermalisation effects are minimised. Other n-n-n+SB device structures such as glass/FTO/n-CdS/n-CdSe/n-CdTe/Au solar cells were also studied but the results yielded poor efficiency. These results are not reported in this thesis for brevity.

9.14.2.2 Discussion/reasons for observed high J_{sc}

The strength of electric field in the depletion region depends on the quality of the solar cell parameters obtained under dark and illumination conditions. Since the charge carriers are generated within the depletion region, there is the need to quickly separate them to external circuits before they recombine in the material. The drift velocity of the charge carriers are increased when the electric field is very strong. By so doing, the photo-generated charge carriers are prevented from recombining within the bulk of the material and this leads to J_{sc} enhancement. The presence of high *RF* of ~$10^{4.3}$, ϕ_b >0.81 eV and low *n* value of ~1.5 in MO1_5 all contribute to the formation of healthy depletion region and strength of the electric field. This is one of the basic reasons why the electronic parameters of n-n-n+SB under dark and illumination conditions improved when compared to n-n+SB device structures.

The J_{sc} obtained from the five measured cells of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells given in Table 9.11 are higher than the reported J_{sc} limit [47] for single p-n junction CdTe solar cell. This increase can be attributed to the graded bandgap structures used in this work [48]. To ensure the authenticity of the J_{sc} observed in this work, the surroundings CdTe layers were carefully removed to ensure that current is not being collected from the immediate CdTe surrounding layers. It was observed that after carefully removing the surrounding CdTe layers around the gold contact, the J_{sc} still remains. This shows that there was no lateral current collection around the measured solar cell contact in these devices. As suggested by Basol [49], the absence of current collection from the surroundings can be mainly due to the high resistivity and ultra-thin CdTe layers being used as an absorber. Due to the grading of the device structure, it is also possible to have the presence of impurity PV effect and impact ionisation. When either or both phenomena are present in a device structure, there is high tendency for the

J_{sc} to rise. Multi-junction graded bandgap solar cells such as the n-n-n+SB or n-n-p provide effective means of harvesting photons from various regions (UV, Vis, and IR regions) of the solar spectrum.

Due to the presence of IR radiations in the environment, photons with energy smaller than the CdTe energy bandgap can be absorbed from the surroundings to create electron-hole (e-h) pairs that can add to the previously generated charge carriers. The created electrons can be promoted from the valence band to any of the 5 defect levels earlier mentioned. Due to the strong electric field in the depletion region, the holes being created acquire sufficient kinetic energy and quickly move to the ohmic contact at the back. The quick drifting of the holes towards the back Au metal contact does not therefore permit the electrons to fall back into the valence band to recombine with holes [50]. The absorption of other low-energy infrared photons into the device structure can also create useful e-h pairs which can now promote the initial electron at the defect level to the conduction band where they are being finally drifted towards the front FTO contact for current generation. This phenomenon is known as impurity PV effect. On the other way round, another electron accelerating from the back contact towards the front contact can give energy to the electron at the defect level and re-promote them to the conduction band where they are eventually drifted towards the front contact. The collection of all these photo-generated currents via impurity PV effect and impact ionisation give rise to high short circuit current density at the output. This same explanation can be applied to the high J_{sc} observed in glass/FTO/n-CdS/n-CdTe/p-CdTe device structures.

9.14.2.3 Characterisation of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells using capacitance-voltage (C-V) technique

The depletion capacitance and the doping density of the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structure were determined using the C-V characterisation technique. The C-V measurements were carried out under dark condition at room temperature using AC frequency of 1 MHz. Figure 9.23 (a) and 9.23 (b) show the C-V characteristics and Mott-Schottky plots of the n-n-n+SB device structures respectively. The depletion capacitance of the n-n-n+SB multi-junction solar cell at zero bias is 264 pF as shown in Figure 9.23 (a). This value remains fairly constant with applied bias from the reverse region to the forward bias at V=~0.2 V. As the forward bias voltage increases beyond 0.2 V, increase of the depletion capacitance with applied forward bias

voltage was observed. The constant depletion capacitance from the reverse bias region is an indication that the solar cell device structure is fully depleted even at bias voltage of ~0.2 V [51]. For an almost or fully depleted device structure, the width of the depletion region is almost equal to the thickness of the electroplated layer. The theoretical thickness obtained for the absorber layer in the device structure is ~1200 nm while the depletion width obtained for the n-n-n+SB using Equation (3.38) is ~1160 nm. The correlation between the estimated theoretical thickness and measured depletion width further attest to the fully depleted nature of the n-n-n+SB device structure.

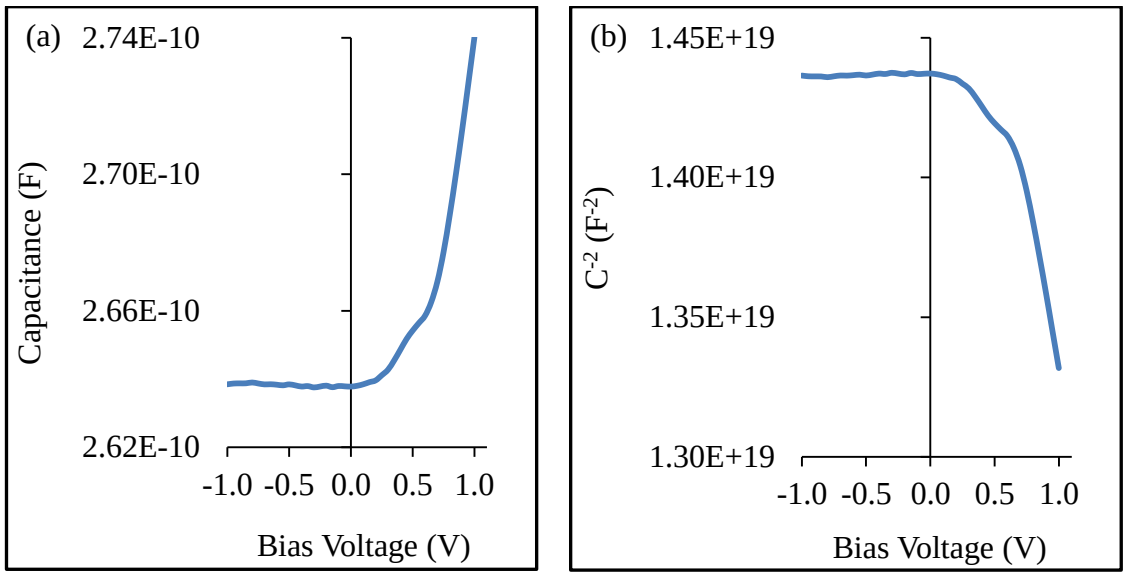


Figure 9.23. (a) Capacitance-voltage plot and (b) Mott-Schottky plot of n-n-n+SB device structures under dark condition.

One other electronic parameter which is also important in obtaining a good solar cell with optimum performance is the doping density. For solar cells to have higher efficiency, it must have a moderate doping. The doping density for glass/FTO/n-ZnS/n-CdS/n-CdTe/Au was estimated to be 5.20×10^{15} cm^{-3} and this value falls within the range of doping densities reported in the literature for solar cells having efficiency greater than 10% [21,28,52,53]. It should be noted that the straight line segment of Mott-Schottky plot is obtained after ~0.5 V forward bias and the depletion region is mainly within the CdTe layer. Therefore, the value obtained (5.20×10^{15} cm^{-3}) represents the doping concentration of n-type CdTe layers. Since the majority carriers are electrons in n-n-n+SB device structure, the obtained doping density (N_D-N_A) from the C^{-2} vs V plot (Mott-Schottky plot) is synonymous to the electron donor density in the solar cell device structures.

By substituting the estimated values of N_D-N_A into Equation (9.1), the position of Fermi level (E_c-E_F) for the n-CdTe used was estimated. The E_c-E_F was found to be at ~0.13 eV below the conduction band minimum.

$$\Delta E = E_C - E_F = kT \ln\left(\frac{N_C}{n}\right) \tag{9.1}$$

Where E_C is the lowest energy of the conduction band, E_F is the Fermi level, k is the Boltzmann constant, T is the room temperature measured in Kelvin and N_C is the effective density of states in the conduction band edge of CdTe semiconductors.

To compare the C-V results of n-n+SB discussed in section 9.12.2 with n-n-n+SB, the C-V parameters of the two device structures are tabulated together. The C-V plots of n-n+SB fabricated from glass/FTO/n-CdS/n-CdTe/Au solar cells have already been described in Figure 9.14. As seen in Table 9.13, the doping density of glass/FTO/n-CdS/n-CdTe/Au heterojunction solar cell is 2.08×10^{16} cm^{-3} while the doping density of glass/FTO/n-ZnS/n-CdS/n-CdTe/Au multi-junction solar cell is 5.20×10^{15} cm^{-3}. The decrease in the doping density can be attributed to the use of ZnS semiconductor as a buffer layer to CdS/CdTe solar cell. Since the doping density of the n-n-n+SB multi-junction device structure is lower than the n-n+SB device structure, it is therefore expected that the mobility of electrons and holes (majority and minority carriers respectively) in the n-n-n+SB multi-junction solar cells be higher than those of the n-n+SB solar cells. The probability of electrons and holes (charge carriers) recombining within the depletion region will be low since the rate at which they move to external circuit after being generated is higher in n-n-n+SB multi-junction than n-n+SB device structures. Since the level of R&G process is greatly reduced in n-n-n+SB multi-junction cells due to the high mobility of electrons and holes and wider/healthier depletion width, the solar cell device parameters will be greatly improved as seen in this experimental work.

Table 9.13. Summary of C-V parameters obtained for glass/FTO/n-CdS/n-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cell structures.

	C-V Measurement under Dark Condition at 1 MHz					
Device Structure	C_o (pF)	W (nm)	Slope ($F^{-2}V^{-1}$)	N_D-N_A (cm^{-3})	E_C-E_F (eV)	E_F-E_V (eV)
n-n + SB	366	836	7.5×10^{17}	1.73×10^{16}	0.10	1.34
n-n-n +SB	264	1160	2.5×10^{18}	5.20×10^{15}	0.13	1.31

9.15 Summary

Solar cells of different device configurations have been successfully fabricated and assessed using I-V and C-V techniques. The positive effects of Ga incorporation into the usual $CdCl_2$ treatments have been demonstrated on the optoelectronic properties of CdTe-based device structures. The initial experiments carried out on device structures comprising of n-CdS, n-CdTe and Au metal contacts showed that the device structures (glass/FTO/n-CdS/n-CdTe/Au) treated with mixture of $GaCl_3$+$CdCl_2$ solution produced better solar cell efficiencies than the ones treated only with $CdCl_2$. The inclusion of Ga into $CdCl_2$ solution has been seen to aid the reduction of series resistance thus leading to enhancement in short circuit current density and fill-factor. This improvement in solar cell parameters demonstrate the ability of Ga^{3+}, Cd^{2+} and Cl^- in the $GaCl_3$+$CdCl_2$ solution to effectively reduce Te precipitates which contribute to the recombination and generation of photo-generated charge carriers in the device structure. The highest solar cell efficiency obtained for glass/FTO/n-CdS/n-CdTe/Au device structures was ~7.6% and this was achieved with the mixture of $GaCl_3$+$CdCl_2$ surface treatment. The experimental studies carried out to examine the effect of variation in pH of $GaCl_3$+$CdCl_2$ solution on the device efficiency showed that the glass/FTO/n-CdS/n-CdTe device structures treated at a pH of 0.60±0.02 prior annealing and metallisation produced better solar cell efficiency than the ones treated at pH of 1.20 and 2.40±0.02. It was observed that acidic pH of 0.60 used for chemical treatments of glass/FTO/n-CdS/n-CdTe produced the least series resistance under illumination. The experimental results revealed the tendency of more acidic pH of 0.60±0.02 to modify the top surface of n-CdTe absorber layers and create a thin layer of p^+ material on the n-n+SB device structure to make it n-n-p^+ graded bandgap solar cell.

Experimental investigations involving the incorporation of p-CdTe layer of different thicknesses on n-n+SB device structures to form multi-junction graded bandgap solar cells were also explored. The results showed that when a larger thickness of p-CdTe is deposited on glass/FTO/n-CdS/n-CdTe, the efficiency of the device suffers. Likewise, the positions of Fermi levels of diodes fabricated from glass/FTO/n-CdS/n-CdTe/p-CdTe/Au (n-n-p) device configuration differ from one another due to the differences in the thicknesses of the p-CdTe layers. The highest efficiency of ~10.9% was observed with p-CdTe thickness of ~35 nm in the n-n-p device configuration. Overall, the fabrication of graded bandgap solar cells with the structure glass/FTO/n-CdS/n-CdTe/p-CdTe/Au showed better results than solar cells fabricated from glass/FTO/n-CdS/n-CdTe/Au. Other p-type semiconductor layers such as p-CdMnTe and p-ZnTe used as back layers to glass/FTO/n-CdS/n-CdTe yielded solar cell efficiency less than 4%.

Other multi-junction graded bandgap solar cells involving n-n-n+SB device configurations were also studied. Solar cells with glass/FTO/n-ZnTe/n-CdS/n-CdTe/Au device architecture yielded highest efficiency of ~8.1% while solar cells fabricated from glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures yielded highest solar-to-electric conversion efficiency of ~12.8%. The summary of the electronic parameters obtained from I-V and C-V measurement techniques for glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells showed that the n-n-n+SB device structure is a potential device architecture that can be further developed for high efficiency solar cell fabrication. The large bandgap in the front of the n-n-n+SB device structure has assisted in creating a steep slope to ease the transportation of electrons to the front contact and the production of strong electric field within the depletion region has helped in separating the holes and electrons to the back and front contacts respectively where they are collected for effective current generation. The overall effect of this process was seen in the improved short-circuit current density of the n-n-n+SB device structures. Future work on the graded bandgap device structures should be focused on improving the efficiency of glass/FTO/n-CdS/n-CdTe/p-CdTe/Au and glass/FTO/n-ZnS/n-CdS/n-CdTe/Au solar cells using optimised electroplated semiconductor materials.

References

[1] N. Nakayama, H. Matsumoto, K. Yamaguchi, S. Ikegami, Y. Hioki, Jpn. J. Appl. Phys., **15** (1976) 2281–2282.

[2] S. A. Ringel, A. W. Smith, M. H. MacDougal, A. Rohatgi, J. Appl. Phys., **70** (1991) 881–889.

[3] S. K. Das, Sol. Energy Mater. Sol. Cells, **29** (1993) 277–287.

[4] T. Schulmeyer, J. Fritsche, A. Thißen, A. Klein, W. Jaegermann, M. Campo, J. Beier, Thin Solid Films, **431-432** (2003) 84–89.

[5] A. Bosio, N. Romeo, S. Mazzamuto, V. Canevari, Prog. Cryst. Growth Charact. Mater., **52** (2006) 247–279.

[6] I. M. Dharmadasa, Prog. Cryst. Growth Charact. Mater., **36** (1998) 249–290.

[7] J. R. Pugh, D. Mao, J. G. Zhang, M. J. Heben, A. J. Nelson, A. J. Frank, J. Appl. Phys., **74** (1993) 2619–2625.

[8] I. M. Dharmadasa, Advances in Thin-Film Solar Cells, first ed., Pan Stanford Publishing Pte. Ltd., Boulevard, Singapore (2013).

[9] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New Jersey (2007).

[10] N. V. Sochinskii, M. D. Serrano, E. Dieguez, F. Agullo-Rueda, U. Pal, J. Piqueras, P. Fernandez, J. Appl. Phys., **77** (1995) 2806–2808.

[11] P. Fernández, J. Optoelectron. Adv. Mater., **5** (2003) 369–388.

[12] S. H. Shin, J. Bajaj, L. a. Moudy, D. T. Cheung, Appl. Phys. Lett., **43** (1983) 68–70.

[13] S. Hu, C. H. Henager, J. Cryst. Growth, **311** (2009) 3184–3194.

[14] Encyclopædia Britannica, http://www.britannica.com/science/gallium (accessed May 23, 2016).

[15] B. M. Basol, Sol. Cells, **23** (1988) 69–88.

[16] T. L. Chu, S. S. Chu, C. Ferekides, J. Britt, C. Q. Wu, J. Appl. Phys., **71** (1992) 3870–3876.

[17] X. Wu, Sol. Energy, **77** (2004) 803–814.

[18] A. Rohatgi, R. Sudharsanan, S. A. Ringel, M. H. MacDougal, Sol. Cells, **30** (1991) 109–122.

[19] N. A. Abdul-Manaf, PhD Thesis "Organic/Inorganic Hybrid Solar Cells Based on Electroplated CdTe," Sheffield Hallam University, Sheffield, 2015.

[20] M. Bugár, E. Belas, R. Grill, J. Procházka, Š. Uxa, P. Hlídek, J. Franc, R. Fesh, P. Höschl, IEEE Trans. Nucl. Sci., **58** (2011) 1942–1948.

[21] I. M. Dharmadasa, Coatings, **4** (2014) 282–307.

[22] S. Mazzamuto, L. Vaillant, A. Bosio, N. Romeo, N. Armani, G. Salviati, Thin Solid Films, **516** (2008) 7079–7083.

[23] O. K. Echendu, I. M. Dharmadasa, Mater. Chem. Phys., **157** (2015) 39–44.

[24] E. W. Jones, V. Barrioz, S. J. C. Irvine, D. Lamb, Thin Solid Films, **517** (2009) 2226–2230.

[25] T. Toyama, K. Matsune, H. Oda, M. Ohta, H. Okamoto, J. Phys. D. Appl. Phys., **39** (2006) 1537–1542.

[26] I. M. Dharmadasa, J. D. Bunning, A. P. Samantilleke, T. Shen, Sol. Energy Mater. Sol. Cells, **86** (2005) 373–384.

[27] I. M. Dharmadasa, A. P. Samantilleke, N. B. Chaure, J. Young, Semicond. Sci. Technol., **17** (2002) 1238–1248. http://iopscience.iop.org/0268-1242/17/12/306.

[28] J. M. Woodcock, A. K. Turner, M. E. Ozsan, J. G. Summers, Thin film solar cells based on electrodeposited CdTe, in: Conf. Rec. Twenty Second IEEE Photovolt. Spec. Conf., Las Vegas, NV, USA (1991): pp. 842–847.

[29] W. Li, L. Feng, J. Zhang, L. Wu, Y. Cai, J. Zheng, W. Cai, B. Li, Z. Lei, Sci. China, Ser. E Technol. Sci., **51** (2008) 33–39.

[30] O. K. Echendu, I. M. Dharmadasa, Energies, **8** (2015) 4416–4435.

[31] I. M. Dharmadasa, G. J. Tolan, M. Cazaux, Semicond. Sci. Technol., **23** (2008) 035023 (10pp).

[32] W. I. Lee, N. R. Taskar, I. B. Bhat, J. M. Borrego, S. K. Ghandhi, DLTS studies of n-type CdTe grown by organometallic vapor phase epitaxy, in: 19th IEEE Photovolt. Spec. Conf., New Orleans, LA, New York (1987): pp. 785–790.

[33] C. Ferekides, J. Britt, Sol. Energy Mater. Sol. Cells, **35** (1994) 255–262.

[34] C. S. Ferekides, R. Mamazza, U. Balasubramanian, D. L. Morel, Thin Solid Films, **480-481** (2005) 224–229.

[35] C. S. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D. L. Morel, Sol. Energy, **77** (2004) 823–830.

[36] J. D. Major, K. Durose, 2013 IEEE 39th Photovolt. Spec. Conf., (2013) 1146–1149.

[37] A. D. Compaan, A. Gupta, S. Lee, S. Wang, J. Drayton, Sol. Energy, **77** (2004) 815–822.

[38] N. Romeo, a. Bosio, V. Canevari, M. Terheggen, L. Vaillant Roca, Thin Solid Films, **431-432** (2003) 364–368.

[39] O. I. Olusola, M. L. Madugu, N. A. Abdul-Manaf, I. M. Dharmadasa, Curr. Appl. Phys., **16** (2016) 120–130.

[40] M. L. Madugu, O. I. Olusola, O. K. Echendu, B. Kadem, I. M. Dharmadasa, J. Electron. Mater., **45** (2016) 2710–2717.

[41] T. L. Chu, S. S. Chu, Solid State Electron., **38** (1995) 533–549.

[42] M. D. G. Potter, D. P. Halliday, M. Cousins, K. Durose, Thin Solid Films, **361-362** (2000) 248–252.

[43] I. M. Dharmadasa, O. Elsherif, G. J. Tolan, J. Phys. Conf. Ser., **286** (2011) 012041.

[44] W. G. Oldham, A. G. Milnes, Solid. State. Electron., **7** (1964) 153–165.

[45] O. I. Olusola, M. L. Madugu, I. M. Dharmadasa, Improvement of CdS/CdTe Solar Cell Parameters using ZnS Buffer Layer, in: Proc. of PVSAT-12, Liverpool

(2016): pp. 107–110. http://www.pvsat.org.uk/proceedings/.

[46] E. H. Rhoderick, IEE Proc. I Solid State Electron Devices, **129** (1982) 1–14.

[47] A. Morales-Acevedo, Sol. Energy Mater. Sol. Cells, **90** (2006) 2213–2220.

[48] N. B. Chaure, A. P. Samantilleke, I. M. Dharmadasa, Sol. Energy Mater. Sol. Cells, **77** (2003) 303–317.

[49] B. M. Basol, J. Appl. Phys., **55** (1984) 601–603.

[50] I. M. Dharmadasa, N. D. P. S. R. Kalyanaratne, R. Dharmadasa, J. Natl. Sci. Found. Sri Lanka, **41** (2013) 73–80.

[51] O. K. Echendu, PhD Thesis "Thin film solar cells using all-electrodeposited ZnS, CdS and CdTe materials," Sheffield Hallam University, Sheffield, 2014.

[52] J. Britt, C. Ferekides, Appl. Phys. Lett., **62** (1993) 2851–2852.

[53] I. M. Dharmadasa, P. A. Bingham, O. K. Echendu, H. I. Salim, T. Druffel, R. Dharmadasa, G. U. Sumanasekera, R. R. Dharmasena, M. B. Dergacheva, K. A. Mit, K. A. Urazov, L. Bowen, M. Walls, A. Abbas, Coatings, **4** (2014) 380–415.

Chapter 10 - Conclusions, challenges and suggestions for future work

10.1 Conclusions

The knowledge of subjects from chemistry, physics, material science and electronics have been utilised in this work to investigate the properties of electrodeposited semiconductor materials. The semiconductor materials studied in this work are CdSe, ZnTe, CdS, CdMnTe and CdTe thin films. ZnS thin films grown by one of our PhD researchers at the Solar Energy Research Group in Sheffield Hallam University was also made use of as a buffer layer in developing multi-junction graded bandgap solar cells.

The main experimental findings carried out during this research work are presented in Chapters 4 to 9. The main focus of Chapters 4 and 5 are on the development of CdSe and ZnTe thin films for electronic device applications. CdSe thin films as reported in this thesis have been successfully used in fabricating Schottky diodes while ZnTe thin films have been employed in fabricating homo-junction diodes with the device structures glass/FTO/n-ZnTe/p-ZnTe/Au. The electroplating of n-ZnTe thin films was achieved in this work by intrinsic doping. Chapter 6 discusses the growth and optimisation of n-CdS thin films for application as hetero-partner to other II-VI binary compound semiconductors such as ZnTe and CdTe. The optimised cathodic deposition potential to grow nearly stoichiometric CdS thin films was established at 1200 mV. Chapter 7 focuses on the application of n-CdS/p-ZnTe hetero-structures for applications in electronic devices. The main application areas investigated under this section include the fabrication of one-sided rectifying p-n junction diodes and solar cells from n-CdS/p-ZnTe hetero-structures layer.

Chapter 8 describes the growth and characterisation of CdTe thin films as the main solar cell absorber material while Chapter 9 is focused on solar cells development using CdTe-based device structures. The effects of $GaCl_3$ inclusion in the usual $CdCl_2$ treatments have been explored in relation to the material and opto-electronic properties of CdTe thin films and associated devices. It was observed that CdTe thin films and CdTe-based device structures treated with mixture of $GaCl_3$+$CdCl_2$ showed improved crystallinity and better solar cell performance than un-treated CdTe layers and CdTe layers treated only with $CdCl_2$ solution. Likewise, the effects of varying the pH of $GaCl_3$+$CdCl_2$ solution for surface treatment of CdTe thin films have been studied.

Results of this investigation revealed that CdTe based devices treated with mixture of $GaCl_3$+$CdCl_2$ at low pH of 0.60 ± 0.02 exhibited larger grains and enhanced solar cell efficiencies.

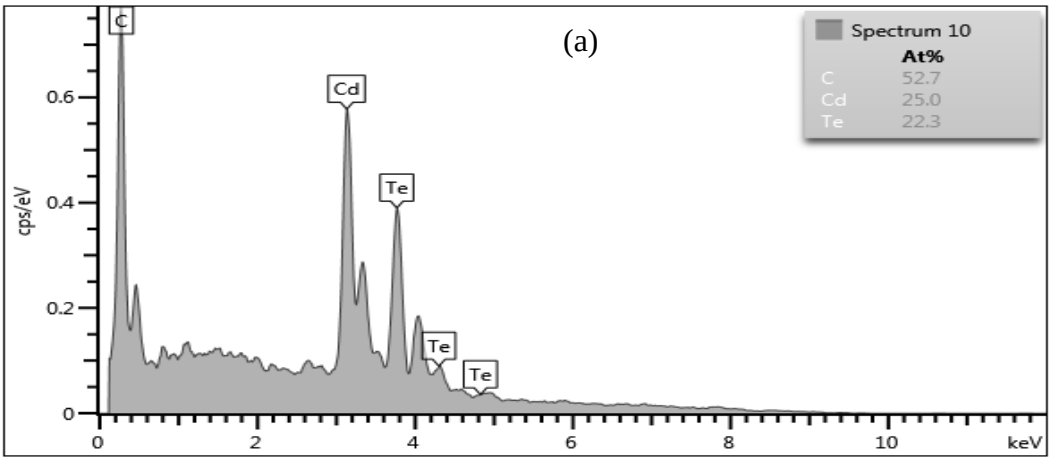
Different device structures have been reported in this thesis but the most important ones are the multi-junction graded bandgap solar cells based on glass/FTO/n-ZnS/n-CdS/n-CdTe/Au and glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device structures. While keeping the thickness of n-CdTe layers fixed at ~1200 nm, the effects of varying the thickness of p-CdTe layer used in glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device structures were also investigated. A p-CdTe layer of ~1200 nm thickness in the above device structures showed a pure ohmic behaviour under dark and a poor solar cell with poor fill factor and efficiency under illumination conditions. When a p-CdTe layer of ~35 nm thickness was used, good rectifying behaviours under dark and better solar cells with efficiency >10.0% were achieved under illumination conditions. These experimental investigations revealed that the thinner the p-CdTe layer in the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device structures, the better the solar cell performance. The highest efficiency reported in this thesis is ~12.8% and this was achieved using the glass/FTO/n-ZnS/n-CdS/n-CdTe/Au device structures. However, the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device structures seem to be a better candidate for high efficiency solar cells if the thicknesses of the semiconductor layers used in the multi-layer graded bandgap solar cells are well optimised.

10.2 Challenges encountered during the current investigations and proposed solution

Achieving solar cells with high efficiencies and maintaining the efficiency consistence is one of the main challenge faced in this work. Some of the factors responsible for this are non-uniformity of electroplated layers and achieving materials with same electronic quality at every deposition stage. With ED technique, it is difficult to maintain the pH and concentration of cations and anions salts in the bath during growth. Even though these parameters are regulated at the start of deposition, they however change as soon as the deposition commences. In this technique, the amounts of ions which make up the electrolytic bath is gradually being used up and they become unknown after carrying out the first deposition. This leads to problem of reproducibility of the thin films and for these reasons, the opto-electronic properties of these layers differ from batch to batch. Therefore to overcome these challenges, it is imperative to use a computerised

concentration analyser that can detect the amount of ions present in the electrolyte at each given period and a programmable automated pumping system that can constantly feed the electrolytic bath with the ions being used up.

Another basic challenges encountered in this work is the deterioration of carbon rod (anode electrode) with time. Continuous usage of the carbon rod without replacement kills the electrolytic bath. When it becomes obvious that the carbon rod is deteriorating visually, it can quickly and easily be replaced with new ones. In a situation where there is a gradual leakage of carbon into the bath from the anode, then this becomes a problem. This occurrence was observed after carrying out EDX analysis on one of the electroplated CdTe samples. The observed results are shown in Figure 10.1. As seen in Figure 10.1 (a), in a CdTe bath that is supposed to have mainly Cd and Te constituents, it was found out that the atomic % of carbon is much higher than Cd and Te combined together. The introduction of carbon into the atomic composition comes mainly from the leakage of carbon into the bath during deposition. The source of this leakage is the carbon rod being used as the anode. With the atomic % of C, the material being formed is no longer CdTe but $Cd_{1-x}C_xTe$. As seen in Figure 10.1 (a), the ternary compound formed is $Cd_{0.32}C_{0.68}Te$ while in Figure 10.1 (b), the ternary compound formed is $Cd_{0.37}C_{0.63}Te$. Carbon being a group IV element when bonded with CdTe introduces a dangling bond into the CdTe lattice. As explained in Chapter 2, dangling bond is one of the main causes of surface defects in a semiconductor material. To prevent this problem, it is proper to replace carbon rod from time to time or to completely seek for an alternative anode to carbon electrode.



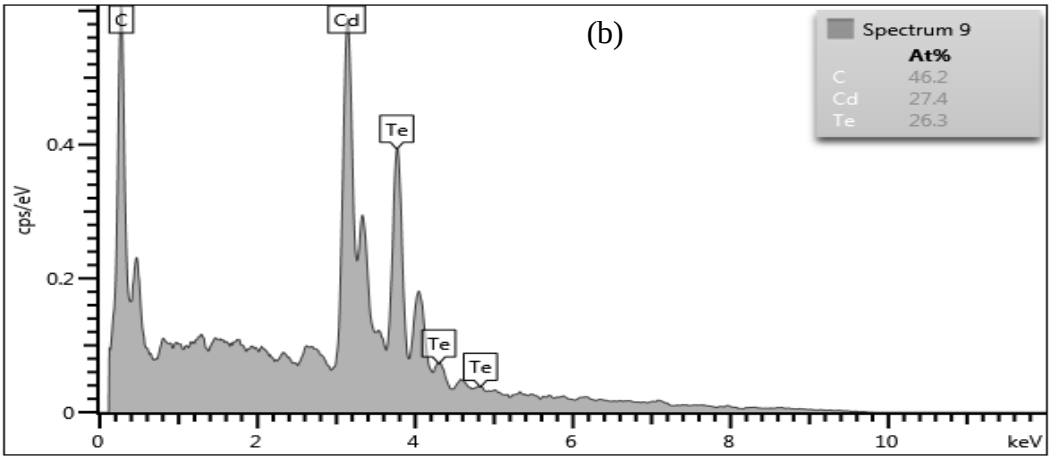


Figure 10.1. (a,b) Typical EDX spectra obtained at different times for CdTe thin films with emphasis on carbon anode degradation.

10.3 Suggestions for future work

The following are some of the suggestions for future work:

(i) To further develop the multi-junction graded bandgap solar cells based on glass/FTO/n-CdS/n-CdSe/n-CdTe/Au device structures for efficiency enhancement.

(ii) To explore the thickness of p-CdTe layers used in glass/FTO/n-CdS/n-CdTe/p-CdTe/Au device structures in-between 0-35 nm. It is anticipated that if the investigation of p-CdTe thin films as a back contact layer to n-CdTe thin films is successfully carried out between 0 and 35 nm, there is a high tendency to achieve solar cell efficiencies greater than 20%.

(iii) To investigate the effect of Ga as an extrinsic dopant in CdTe thin films. Since the effects of $GaCl_3$+$CdCl_2$ have been explored in this research work as surface treatments to CdTe thin films, it is vital to further study what happens when Ga is introduced into the CdTe electrolyte as an external dopant. Therefore, part of the future work would be focused on this study.