Waveform acquisition with resolutions exceeding those of the ADCs employed

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Waveform acquisition with resolutions exceeding those of the ADCs employed

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Abstract

This chapter discusses various software/firmware and hardware methods and architectures to improve the fidelity of the acquired waveforms beyond the vertical and horizontal resolutions that are possible with the ADC employed. The applicability of these approaches, and the limits on the enhancements that are achievable, depend upon the nature of the acquired waveform, and they are presented separately for one-shot, repeatable and repetitive waveforms. The possibilities of combining applicable methods in order to simultaneously increase both resolutions are also discussed. The consideration is illustrated by the simulation results and the acquired experimental waveforms relevant to the ultrasonic non-destructive evaluation.

Keywords: *waveform acquisition, vertical resolution, horizontal resolution, analog-to-digital converter (ADC), time-interleaved ADC, averaging, boxcar averaging, synchronous digital averaging, on-the-fly averaging architecture, oversampling, equivalent time sampling, random interleaved sampling, accurate interleaved sampling (AIS), one shot waveform, repetitive waveform, repeatable waveform, dither, two clock AIS architecture, time delayed AIS architecture*

2.1 Introduction

Waveform acquisition involves digitizing equidistant samples of a signal of interest which high spectral boundary is not negligible compared to the sampling frequency. The collection of the consecutive samples acquired during a particular time interval (time window) is referred to as an acquisition frame. The frame may be displayed for visual inspection, analysis, and measurements, which is common for digital storage oscilloscopes (DSOs); stored or used for subsequent digital processing, feature extraction, and/or parameter estimation in various electronic devices or purpose-built digitizers.

Waveform acquisition can be seen as substituting for the continuous graph of input variable versus time with a collection of associated dots located in the nodes of a graph paper of some scale. Better representation of the continuous waveform of interest can be achieved by increasing the horizontal and/or vertical resolution of the graph paper used. However, any realizable analog-to-digital converter (ADC) imposes particular limitations on both resolutions due to its limited number of bits (more precisely, effective number of bits—ENOB) which determines the vertical resolution and maximum sampling frequency which determines the horizontal resolution commonly referred to as the time base in DSO literature. (These resolutions defined by the ADC itself should not be confused with the horizontal and vertical screen resolutions of DSOs featuring displays.)

The data converter market represents approximately 17% of the world's analogue semiconductor market, which was estimated to be around \$20B in 2013 [1]. Additionally, ADCs are built into most microcontrollers, many systems-on-chip and even some field programmable gate arrays (FPGAs) [2]. The costs of the top-of-the-range DSOs can reach six figures (e.g. [3,4]). Every established electronic components distributor offers several hundred types of ADCs and quite a few DSOs that can meet the needs for diverse performance and power and/or cost requirements. Nevertheless, there are several instances when improvement of the ADC/DSO resolutions is highly desirable, for example:

- Most modern low-cost microcontrollers are equipped with built-in ADCs with a resolution ranging from 8 to12 bits and maximum sampling frequencies ranging from 100 kHz to 3 MHz, or more. Whilst these sampling frequencies are more than sufficient for the acquisition of various slowly changing waveforms, the vertical resolutions might not be high enough for achieving the required temperature resolution when converting the output voltage of many analogue sensors, such as temperature [5], force, pressure or humidity [6]. Using an additional higher resolution ADC (or a premium microcontroller with a built-in higher resolution ADC) would increase the cost of the device; however, that could be avoided if the resolution of the built-in ADC was enhanced;

- There are several applications where any increase in the ADC resolutions would be gratefully utilised, most notably DSOs, software-defined radios (SDRs) and high-speed communication links that use some modulation. For example, contemporary DSOs exhibit much higher resolutions compared to the very top-of-the-range ADCs that are achieved by using many lower specs ADCs that are simultaneously integrated into a proprietary integrated circuit as discussed in Section 2.3.2;
- Achieving flexible resolutions by modifying the programmable parts of an existing DSO or relevant software plugins without the need for an expensive hardware re-design or upgrade; and
- Overcoming the limitations imposed by a particular ADC architecture while retaining the benefits (e.g. flash ADCs provide the best horizontal resolutions, but achieving high vertical resolutions is impractical; the opposite applies to sigma-delta ADCs [7,8]).

This chapter discusses various software/firmware and hardware methods and architectures to improve the fidelity of the acquired waveforms beyond the capabilities of the ADC that is employed. It is organised as follows. Section 2.2 discusses how the ADC resolutions affect the fidelity of the acquired waveforms regardless of their nature. Section 2.3 outlines the methods that are available for enhancing the resolutions for one shot waveforms. The enhancements methods applicable to repetitive waveforms are considered in Section 2.4. Section 2.5 describes the methods for resolution enhancement related to repeatable waveforms. Section 2.6 presents the summary and conclusions.

2.2 What resolutions are sufficient for the task at hand?

2.2.1. Horizontal resolution

Waveform acquisition is founded on the Nyquist sampling theorem (some people prefer to reference Shannon, Whittaker, and Kotelnikov [9]). The theorem states that a band limited signal could potentially be accurately reconstructed if it is sampled with infinite vertical resolution at sampling frequency f_s exceeding the highest frequency of the signal spectrum F_h at least twice. This selection of the sampling frequency will completely prevent spectrum aliasing that distorts the signal otherwise. Strictly, band limited signals started in the Stone Age and must be digitized from this point until the collapse of the Sun. As ADCs came into existence less than 100 years ago and have a limited lifespan, this type of signal cannot be digitized perfectly backwards and forwards nowhere near this scale. Using any time-limited acquisition window in theory extends the spectral content of the signal of interest to infinity, resulting in spectrum distortions through spectrum aliasing. As the full power analog bandwidth of most commercially available ADCs is commonly engineered to be higher than their maximum sampling rate, this aliasing should be reduced by appropriate low pass filtering in the ADC analogue front end (AFE). One of the leading DSOs vendors recommends selecting the AFE bandwidth depending either on the reciprocity of the rise time of pulsate signals of interest [10, p.37] or at up to 5*F_h [11, p.13].

DSO manufacturers recommend digitizing a most basic sine wave with a sampling frequency at least 3–5 times its frequency [12], and apply built-in *sin(x)/x* interpolation to present the digitized waveform with extra clarity [13]. (Although linear interpolation can be used in principle for the acquired waveform reconstruction, it would require 4 times higher sampling frequency to achieve compatible reconstruction results [10, p.38; 11, p.15].) It is not uncommon to see a recommendation of selecting a sampling rate of 10x F_h for embedded designs (e.g., [14]).

Despite sine waves are widely used for testing purposes and quantification of the ADC performance, most electronic devices use digital signals that can be considered as rectangular waveforms. It has been shown that high accuracy measurement of the rise time of a periodic rectangular waveform required a DSO analogue bandwidth that exceeded the fundamental frequency of the waveform by a factor of 20 [15, Fig. 3–6]. Following another recommendation from the same DSO vendor (to keep the DSO’s sampling frequency four times higher than its analogue bandwidth [12]), the required sampling frequency eventually exceeded the fundamental frequency (or F_h if applicable) of the signal of interest by a factor of 80. This factor likely presents the upper estimate for the multiplier of the fundamental frequency of the signal because signals with faster transients occupy wider spectra.

Most waveforms of interest can fit between the extreme examples of sine and rectangular waves considered above. There is a viewpoint that increases in the sampling frequency may be unnecessary if the waveform samples acquired at lower frequency are appropriately interpolated (for example, using the *sin(x)/x* function, as mentioned above). We simulated acquisition of a pulse smoothed by a low pass RC-network, as shown in Fig.2.1, where an ideal switch was in the up position in samples numbered from 20 to 40 only. After processing by a high-order ideal Butterworth filter, the resultant pulse was digitized by several ideal ADCs operating at different sampling frequencies, and interpolated to a virtually continuous waveform using the **resample** function in MATLAB. The interpolation errors calculated relative to the waveform reconstructed from the highest sampling frequency available were found of the magnitude of up to a few percentage points (Fig.2.2, bottom) that translates to the ENOB after reconstruction of 6 bits only. Although ENOB is referred to the vertical resolution discussed in section 2.2.2, the obtained value would be unsatisfactory for all but very crude measurements.

Therefore the sampling frequency calculated from the sampling theorem using some reasonable assumption for F_h should be considered as a bare minimum, and must be increased further by a factor ranging from 2 to 40 giving the required sampling frequency f_s of 4..80 F_h depending on the nature of the waveform of interest. It might be overoptimistic to expect the *sin(x)/x* interpolation procedure to compensate for an insufficient sampling rate.

2.2.2 Vertical resolution

Most ADCs produce an output code that is proportional to the input voltage. In the latter, the smallest change that can be resolved depends upon the ADC’s reference voltage and the number of bits. As the reference voltage can vary for the majority of the commercially available off-the-shelf ADCs, the ADC resolution is commonly referred to simply as the number of bits in the output code that is fixed by the ADC design.

As an ADC produces a discrete fixed width digital code for the continuous input signal amplitude, there is a difference between the two values that is referred to as a quantization error for a single sample and quantization noise for a waveform. The required ADC resolution (bits) is commonly calculated using the following ubiquitous formula (e.g. [16,Section 5]):

$$N_b \geq \frac{SNR(dB)-1.76}{6.02}, \tag{2.1}$$

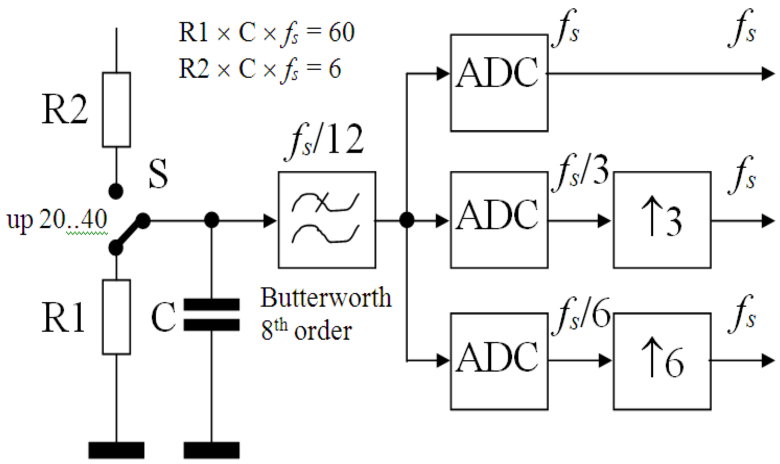


Figure 2.1. Block diagram of the smoothing low pass RC-network and digitizers used for simulating the sin(x)/x reconstruction accuracy versus sampling frequency [49]

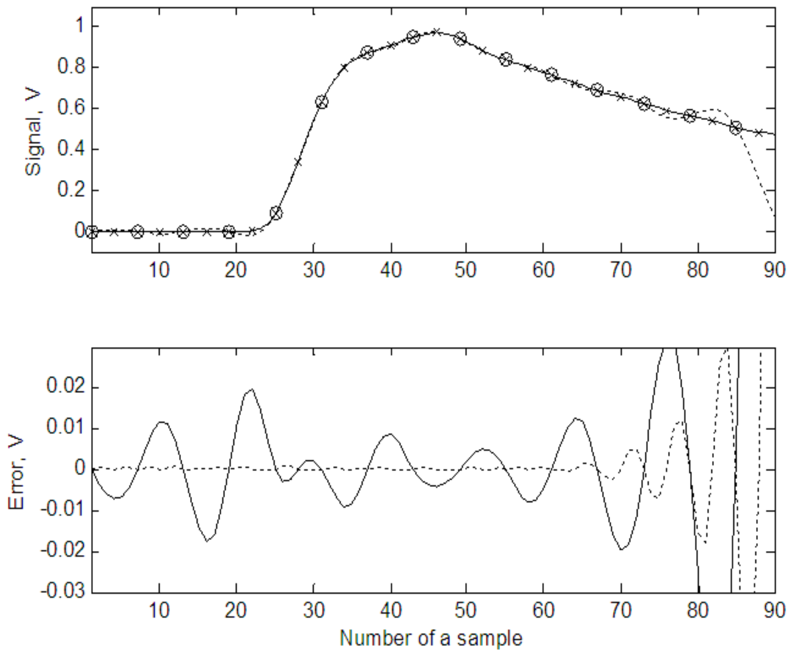


Figure 2.2. Waveforms simulated at different sampling frequencies (top) and reconstruction errors for the fs/6 (solid line) and fs/3 (dashed line) [49]

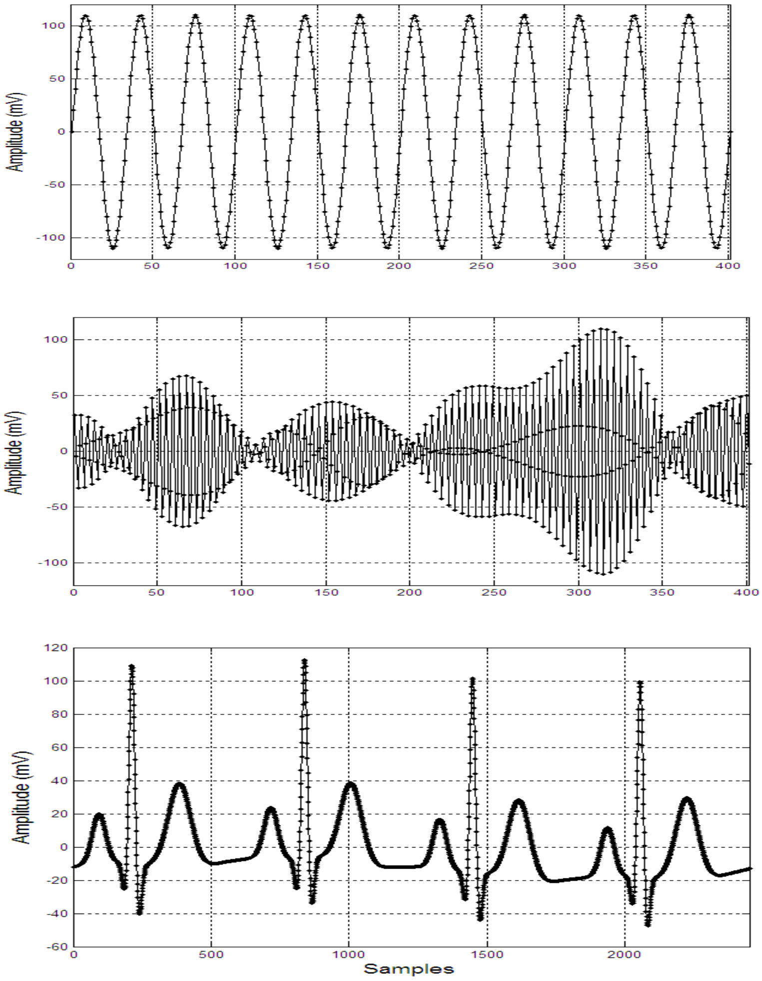
where the signal-to-noise ratio (SNR) refers to either the input SNR (in this case the calculated N_b ensures that the ADC's quantization noise is lower than the input noise), or to the signal-to-quantization noise ratio (SQNR) alone if the input noise can be considered negligible. (The derivation of a more comprehensive equation that includes some additional factors is presented in [17, eq. 10].)

It is important to remember that (2.1) was derived under some particular assumptions that should be met in order for it to be valid, namely:

- A rounding ADC was considered (truncating ADCs produce more quantization noise because of the offset of half of the ADC least significant bit (LSB); some commercially available ADCs do truncate rather than round their input signals);
- The ADC input is a sine wave (for any other input waveforms it is necessary to consider the ratio between their root mean square (RMS) and the amplitude voltages, known as the loading factor [18], or its reciprocal value, known as the crest factor [19]);
- The amplitude range of the sine wave perfectly matches the ADC input range (in practice, the required gain/attenuation and the offset to the input signal should be provided by the AFE);
- The frequency of the sine wave is not too low to be considered as a nearly direct current for the time window used for the acquisition (otherwise the ADC will produce nearly the same offset for every sample, resulting in a higher RMS overall); and
- The frequency of the sine wave is not too high, as demonstrated below.

Let us consider the importance of the loading factor for several typical waveforms in comparison to the sine wave (Fig.2.3, top graph), namely an orthogonal frequency division modulated (OFDM) waveform common for telecommunications [20] (Fig.2.3, middle graph) and an electrocardiogram (ECG) waveform common for biological signal processing [21] (Fig.2.3, bottom graph). The peak-to-peak amplitude of these waveforms related to their standard deviations is different from that of a sine wave; thus, the realized SQNR should account for the loading factor. By changing the offset voltage of the DSO, one can fit these waveforms into the full operating range of the ADC, and estimate the RMS value of the digitized waveform. The results show substantial deterioration compared to what was expected (Fig.2.3, the table, best case).

An arbitrary input signal, in addition to offsetting, often requires extra amplification or attenuation to fit the operating range of the ADC.



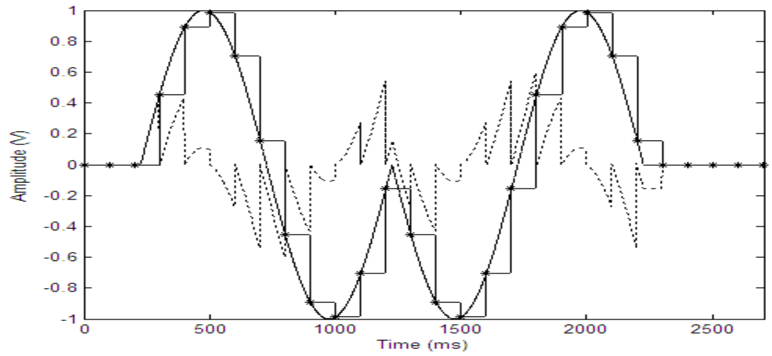
SQNRs CALCULATED FOR THE WAVEFORMS ABOVE

Waveform	**SQNR, dB Best case**	**SQNR, dB Worst case**
Sine wave	49.91	41.95
OFDM	44.18	36.22
ECG	42.23	34.27

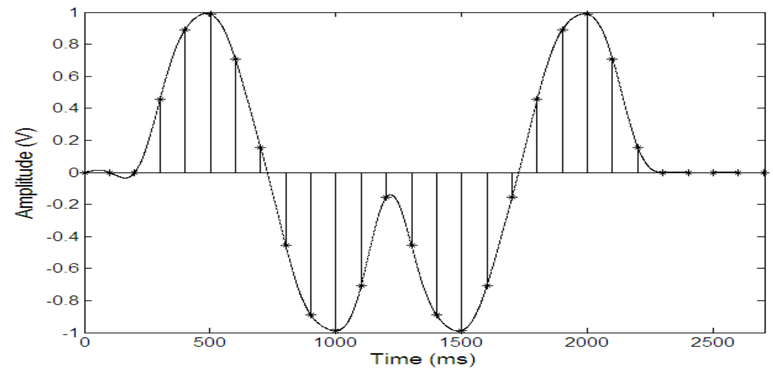
Figure 2.3. Waveforms used for simulation of the SQNRs and the results obtained (from top to bottom: sine wave, OFDM, ECG)

Most commonly, the gain can be adjusted according to the following set: 1x, 2x, 5x, 10x, etc if applicable. This means that if the 5x setting is used but the signal even slightly saturates, a lower setting of 2x will have to be used instead. This setting will lead to the reduction of the RMS value of the digitized signal by a factor of up to 5/2=2.5, or 7.96 dB, lowering the worst case QSNR down to 34–42 dBs only, as shown in Fig.2.3, the table. If the adjustment of the offset was not available, the realized QSNR would even be worse for the ECG case. Therefore it is quite possible to lose around 12 dB QSNR (or 2 bits of ENOB) due to the low loading factor of the input signal and suboptimal gain of the AFE.

To illustrate the importance of the adequate sampling frequency, let us consider sampling a 2-bit binary phase shift coded message with the fundamental frequency of 1 Hz and an amplitude of 1V, presented in Fig. 4a as a solid continuous line, by an ideal sampler with infinite resolution; thus, QSNR=∞ (in MATLAB simulations the actual resolution was 64 bits of the default double precision). In this case, using the sampling frequency of 10 Hz seems appropriate, and the obtained samples are shown in Fig.2.4a as the stepped solid line that can be used to reconstruct the input signal with the aid of a conventional digital-to-analog converter (DAC) that ideally holds its output voltage intact until the following sample. However, this reconstruction exhibits substantial errors, shown in Fig.2.4a as the dotted line. The difference between the original waveform and its reconstruction can be significantly reduced if the *sin(x)/x* interpolation is used instead (in Fig.2.4b, the solid line shows the reconstructed signal, the vertical lines point to the samples taken from the input waveform). The reconstruction error peaks at the bit change instant at about 14% (Fig.2.4c). The signal-to-reconstruction error ratio (SRER) is 29 dB giving an ENOB of 4.7 bits only according to (2.1). This primarily happens due to the presence of three discontinuities in the waveform that led to profound spectrum aliasing. Nevertheless, even when the input waveform was filtered by an FIR digital filter with the bandwidth of 3 Hz, with a stop band starting from 5 Hz and a side lobe level below -40 dB, the reconstruction error still peaked at about 5% with the overall SRER of 45 dB, which was equivalent to only 7.2 bits according to (2.1). Therefore, the required number of bits calculated from (2.1) should be considered to be a lower estimate for the required number of bits in the general case. If (2.1) is solved for the SQNR, and the latter is calculated for the actual number of bits of the selected ADC, this figure will be achievable in practice if all the conditions mentioned above are valid.



a



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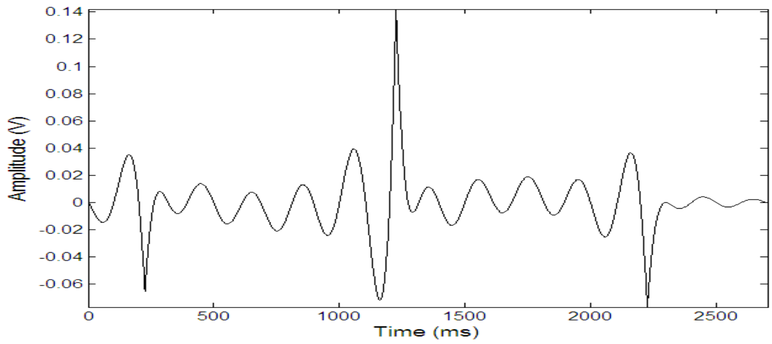


c

Figure 2.4. Simulation of the reconstruction errors of a 2-bit binary phase shift keying modulated signal sampled at 10x its fundamental frequency by an ADCwith infinite vertical resolution ((a) interpolation by bars provided by common DACs and reconstruction error (dashed line); (b)interpolation by *sin(x)/x*; (c) reconstruction error for *sin(x)/x* (note the scale))

2.2.3 Interrelation between the resolutions

For the successive approximation and for sigma-delta ADC architectures, the output code is produced by iterative processes that generally achieve better vertical resolution given more time. However, increasing the sampling interval decreases the maximum sampling frequency that is available. For these types of architectures, both resolutions need to be considered simultaneously. Some commercial so-called "flexible resolution" DSOs allow trading off one resolution for another (e.g. [22]).

2.3 One shot waveforms

These waveforms relate to one off processes that occur sporadically without repeating or ones that should be acquired for immediate processing or streaming.

2.3.1 Enhancing the vertical resolution

This enhancement is based on the fact that the width required for maintaining the sum of several binary variables without overflow exceeds their width. For example, adding two 8-bit variables requires having a total of 9 bits. If the result of such additions is divided by the number of constituents (the constituents are averaged), in the above example half a bit of resolution can be potentially gained. (This procedure would not work if all the constituents are exactly the same, as the average would equate to the value of the constant samples.) The additional values that are required for enhancement can be obtained by sampling the input signal at a sampling frequency f_{os} that is higher than that required to achieve the desired horizontal resolution by an integer factor k ($f_{os}=k\times F_s$), which is referred to as oversampling. If the oversampled waveforms are processed using moving average whilst keeping f_{os} for the output data, the procedure is known as boxcar averaging [23]. If the processing procedure (that performs either averaging or low pass filtering of the extra samples) eventually reverts the sampling frequency to f_s by decimating the output, vertical resolution enhancement can be achieved. Manufacturers of microcontrollers and DSOs refer to this procedure as oversampling [5, 6], oversampling and decimation [16] or simply resolution enhancement [24]. We will refer to this procedure as oversampling throughout this chapter even though this term can be confused with the procedure applied to reconstruction of analog audio signals using DACs [25]. Additional benefits of oversampling that are useful on their own include easing of the requirements for the AFE anti-aliasing filter and the possibility of filtering out some of the quantization noise [25].

The above consideration can only lead to resolution enhancement if the extra samples are not the same as those mentioned above. In many cases, the input signal features enough noise thereby allowing the oversampling to achieve the desired resolution enhancement without taking any extra measures. However, there are cases when some additional noise should be injected deliberately in order to make the procedure work. (Four methods for implementing injections are mentioned in [5, p.9]). The amount of noise should be high enough to allow for vertical resolution enhancement by oversampling, but low enough so as not to distort the signal of interest very much. The value of at least 1 LSB was suggested in [5, p.13]. We simulated the operation of a rounding digitizer when a random Gaussian noise was added to the input signal. Our study consisted of 1000 samples all kept at zero, and we calculated the RMS value at the output for various oversampling factors (number of averages) (Fig.2.5). The simulation confirmed that, if the RMS value of the injected noise was below 0.5 LSB, the output RMS value tended to saturate at higher oversampling factors, which meant that the vertical resolution enhancement would not be achieved. For values of 0.5 LSB or higher, the output RMS value followed the theoretical prediction (the output RMS to be proportional to the square root of the number of averages N_A). On this basis, we suggest using the RMS value of 0.5 LSB for the injected noise, if it is required.

To conclude the discussion of oversampling, we need to consider dither (or dithering), which was successfully applied to the low resolution ADCs available for digital audio during the early days of its development. Indeed, dither involved adding noise to the signal of interest before the conversion, but no oversampling was used due to the lack of fast ADCs at that time. This was done in order to smooth out the quantization noise spectrum that otherwise peaked at the harmonics of the fundamental frequency [26]. Despite the increased overall noise level [26], due to the human peculiarities of sound perception, the digitized sine waves sounded much less distorted than these recorded without dither (example records can be downloaded from [27]). Therefore, noise injection for the enhancement of the vertical resolution during oversampling can be called dither, but this should not be confused with the dither that is used for digital audio.

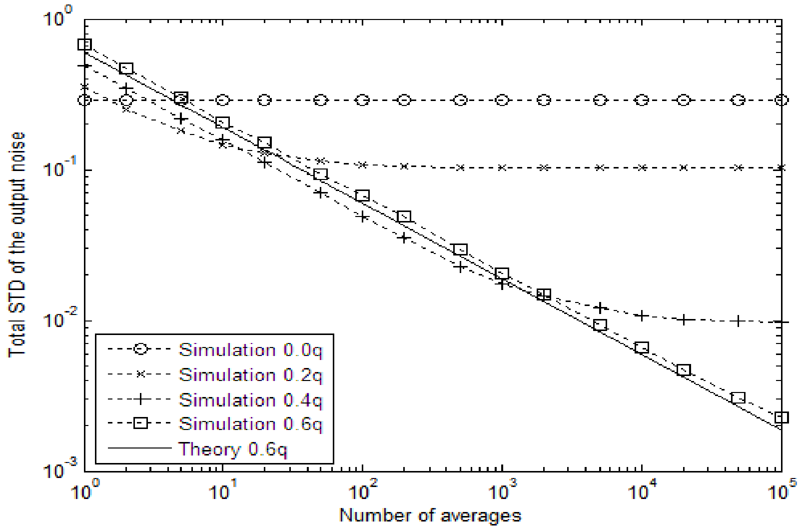


Figure 2.5. Simulated standard deviations of the output noise of a digitizer; the figure shows different levels of standard deviation of the input additive noise related to the quantization step (*q*) of 1 LSB [49]

2.3.2 Enhancing the horizontal resolution

Some ADCs could be overclocked beyond the manufacturer's specification to increase their sampling frequency, but doing this would invalidate their other specified parameters and, nevertheless, it would only marginally extend the maximum sampling rate. A better approach involves getting several identical ADCs to convert the signal of interest in parallel, and then clocking each of them individually to take samples after equidistant delays that cover a nominal minimal sampling interval of an individual ADC. The collected samples are then interleaved to present a final waveform with the sampling frequency increased by the interleaving factor N_I equal to the number of the ADCs used [28]. This hardware architecture is mostly referred to as time-interleaved ADCs (TIADC) [29]. In addition to the increase of the sampling frequency, counter-intuitively this architecture can lead to lower power consumption in comparison to a single high-speed ADC [30]. The most serious drawback of this architecture is the need to compensate for unavoidable mismatches of individual ADC parameters (like offset, gain, time skew [31], AFE and sample-and-hold errors [29]) that are usually software corrected. These mismatches can be reduced to a certain extent if all of the ADCs are implemented on the same semiconductor die. A selection of recently reported research prototypes features TIADCs with N_I ranging from 2 to 128, resolutions ranging from 6-14 bits and sampling at up to 16 Gsps, as shown in [29, Table 2]. Proprietary TIADC designs were successfully employed by various DSO manufacturers; [32] outlines the designs of flagship DSOs for one of the leading DSO vendors spanning from 1987 until 2007, with all the DSOs featuring TIADCs. The DSO built in 2007 contained 80 interleaved ADCs to achieve the overall sampling frequency of 20 Gsps.

It should be noted that ensuring precise timing for individual TI ADCs might be more important for acquisition fidelity than just increasing N_I; some examples of acquired waveforms with poorly time aligned TI ADCs are discussed in [33].

Whilst many DSOs provide multiple input channels by sharing a single high-speed ADC, some DSOs utilise multiple ADCs for different channels. In the latter case, the ADCs can be interleaved when only one channel input waveform is of interest.

2.3.3 Enhancing horizontal and vertical resolutions simultaneously

As TIADCs represent a hardware solution for increasing the horizontal resolution, and oversampling allows for enhancing the vertical resolution in software, they seem to be compatible and can be potentially combined, for example, in order to increase the vertical resolution of a given high-speed ADC.

2.4 Repetitive waveforms

In a strict mathematical sense, a periodic function should perfectly repeat itself after expiration of its time period. Acquired waveforms usually feature some period jitter and additive noise that results in any waveform not being fully compliant to the above definition. For example, a communication bit stream contains level changes happening at the fundamental bit rate but at unpredictable (non-periodic) instants. In electronics, a waveform can be generally considered repetitive if it can be observed on an analog oscilloscope screen, and a bit stream will form an eye pattern (diagram) widely used to establish the appropriate bit rate [34].

The acquired waveform may contain a fraction of a repetition or several repetitions (periods if applicable). Because of the repetitive nature of such a waveform, it is possible to collect several acquisition frames over time and process them to increase the resolutions.

2.3.4 Enhancing the vertical resolution

When several acquisition frames are collected and aligned in the time domain, it is possible to average them sample-by-sample, which is referred to as ensemble averaging [23]. This procedure is commonly used to reduce the additive noise dispersion times the number of averages N_A. In comparison to the resolution enhancement for the one shot waveforms using the oversampling discussed in Section 2.3.1, the samples are collected, not consecutively, but with a substantial delay equal to or exceeding the duration of the acquisition frame which should completely de-correlate any additive noise. Nevertheless, all the considerations of Section 3.1 are applicable here. In particular, increasing N_A leads to $sqrt(N_A)$ reduction of the noise RMS value only if the latter exceeds 0.5 LSB.

The potential of accurate waveform acquisition in the presence of additive noise was demonstrated in the custom digitizer that was capable of acquiring waveforms with amplitudes around 100 nVp-p against a noise background of 335μV RMS using an ADC with the LSB of 488 μV [35]. As noted by one study: "The physical basis of this performance is that the low amplitude input signal is added to electronic noise at the system input and 'rides' on this noise as it passes through the system" [36].

There is one notable distinction that relates to waveform averaging. Perfect aligning of the acquired frames in the time domain is not possible if the ADC and the source of the waveform are not clocked from the same source. This misalignment results in a particular frame jitter noise [34] that needs to be taken into account when assessing the averaged waveform's fidelity.

Most DSOs feature an averaging mode with the maximum number of averages up to 1,000 or more, depending on the DSO model. Sometimes the acquired waveforms with the increased vertical resolution cannot be displayed on the DSO's screen with the full resolution of the former due to the limited number of the pixels of the latter, but it can be stored for future use.

2.3.5 Enhancing the horizontal resolution

If the unpredictable time differences from the trigger event to the sampling edge of the ADC clock are measured with high accuracy, and a number of frames are collected, they can be interleaved in the time domain to reconstruct the waveform. For this procedure to work, the waveform repetitions should be strictly asynchronous to the ADC clock [38]; otherwise, only a limited range of the time differences can be obtained. The reconstruction could consist of analysing the recorded delays and selecting the waveforms that arrived most closely to the equidistant N_I time instants that cover the ADC sampling period [38]. Because the differences are random, the number of the collected acquisition frames is expected to be sufficiently large; achieving N_I=20 requires the collection of 104 frames, on average, but sometimes many more are needed [39]. Additionally, *sin(x)/x* interpolation over the selected set may be used in order to improve the quality of the acquired waveform [40]. This procedure is referred to as random interleaved sampling (RIS) [38] or random equivalent time sampling (ETS) [40]. If the time differences are not measured accurately, interleaving the acquired frames may lead to numerous glitches due to errors in the time alignment (e.g. [41, Fig. 11b]).

Another approach is to progressively delay the sampling edge of the ADC clock relative to the trigger event for every subsequent repetition of the waveform of interest by a specific and precise amount. A single sample may only be acquired during the entire repetition if the repetition frequency is commensurate with the ADC clock frequency and the generated internally synchronous trigger is used to clock the ADC directly [42, 43]. Alternatively, the precise inter-repetition delays may be applied to the continuing ADC clock pulses in order to acquire many samples over every repetition [44]. In this case, the number of acquired waveforms does not need to exceed N_I, which reduces the required acquisition time in comparison to the RIS. Confusingly, this procedure may also be referred to as ETS [43].

Regardless of whether or not the asynchronous or synchronous trigger is used for ETS, all the referenced studies stress that it must be stable; thus, it must occur at the same time instance for every repetition. Trigger stability was simulated using the first order triggering model [44, Section 5]; the simulation showed that the additive noise introduces jitter to the otherwise stable trigger event and the jitter RMS value increased with the decrease in the gradient of the trigger signal for the same RMS value of the additive noise. Therefore, noisy waveforms with slow transients may not be suitable for the ETS waveform acquisition.

2.3.6 Enhancing horizontal and vertical resolutions simultaneously

In general, combining ensemble averaging with RIS for repetitive waveforms seems rather complicated and it will likely require that a massive number of frames be acquired with the stable trigger.

2.5 Repeatable waveforms

Repeatable waveforms can be started at any time by the excitation signal from the instrument. They are essential, for example for distance measurement, object classification and remote sensing using radars and sonars; and, for measurement of the parameters and fault testing of the electrical and electronic devices, for example time-domain reflectometry (TDR) and ultrasonic non-destructive evaluation (NDE).

2.3.7 Vertical resolution

Operating repeatable waveforms makes it possible to tightly synchronise the excitation pulses with the ADC clock, eliminating most of the frame jitter noise [45]. The remaining frame jitter relates to the long-term drift of the frequency of the master oscillator [45]. If necessary, this drift can be reduced by using an atomic oscillator or oscillators that are temperature compensated, oven controlled or GPS-disciplined instead of a more common crystal oscillator [46]. As discussed in the previous sections related to the vertical resolution enhancement (Sections 2.3.1 and 2.4.1), some additive noise should be present in the waveform at the ADC input to enable this enhancement.

Fully synchronous digital averaging (SDA) can be implemented by updating the running totals for every waveform sample by adding the newly acquired frame samples to the totals in the software. This procedure would increase the overall time required for the fast waveform acquisition because it takes a considerable amount of time to update the totals for the waveforms acquired from many samples. During this update, the acquisition of extra frames should be postponed so as not to overwrite the most recently acquired frame until it is fully processed. A better alternative for SDA implementation is to update the running totals as soon as every new waveform sample becomes available from the ADC by employing dedicated hardware (on-the-fly averaging architecture [45]). This architecture allows for reducing the waveform acquisition time to its theoretical minimum of:

$$t_{acq} = \frac{N_A}{F_R}, \tag{2.2}$$

where F_R is the excitation repetition frequency.

Because SDA allows for the elimination of most of the frame jitter noise, better acquisition of waveform fidelity can be achieved in comparison to the ensemble averaging method applied to repetitive waveforms, as discussed in Section 2.4.1.

2.3.8 Horizontal resolution

As the excitation and ADC clock pulses are derived from the same master clock for repeatable waveforms, and because they no longer need to be derived from the waveform of interest as was the case for RIS, the acquisition trigger becomes as stable as one can obtain from contemporary instrumentation that enables accurate interleaved sampling (AIS). AIS makes it possible to acquire only N_I subsequent waveforms with time delays that are precise to each other without the need for any additional frames to implement RIS. When compared to TI-ADCs, AIS eliminates any mismatches among individual ADCs as only the same ADC is used for the acquisition of all the frames that are interleaved.

The precise delays required to implement AIS can be obtained using either two separate free running oscillators derived from the master clock (two clock AIS architecture [41]) or a delay line formed by a particular quantity of cascaded logic gates (time-delayed AIS [47]).

2.5.3 Enhancing horizontal and vertical resolutions simultaneously

Unlike the case for the repetitive waveform acquisition, acquiring repeatable waveforms does allow for combining both resolution enhancements at the expense of the increased waveform acquisition time:

$$t_{acq} = \frac{N_A \times N_I}{F_R}. \tag{2.3}$$

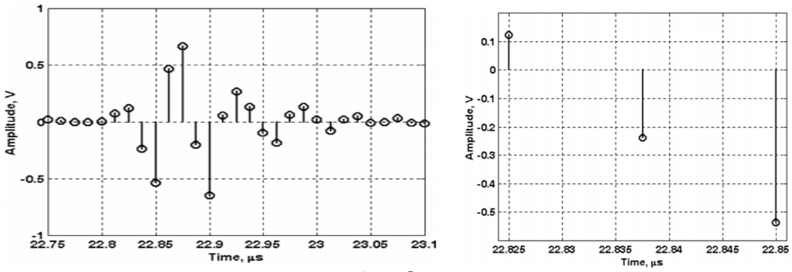
Even for excitation repetition frequencies in the low kHz range (the 1 to 10 kHz range is commonly used for ultrasonic NDE), the required waveform acquisition time may increase to a few seconds and even tens-of-seconds. Balancing N_A and N_I values within the available measurement time budget of the process of interest and the frequency of the master oscillator do not vary notably throughout the complete acquisition time.

A combination of on-the-fly averaging and AIS architectures can be implemented using an FPGA, as was done for several revisions of an ultrasonic NDE digitizer in our laboratory [49]. Fig.2.6 presents the ultrasonic waveforms acquired in the pulse echo mode from a 20 MHz transducer using an 80 MHz clocked ADC that illustrates increases in the acquired waveform fidelity for various combinations of N_A and N_I [50]. The right side of Fig.2.6 shows that the acquired waveform slightly drifted in the time domain from one acquisition to another due to changing ambient temperature. Such a high achieved horizontal resolution can be exploited to measure temperature ultrasonically [51].

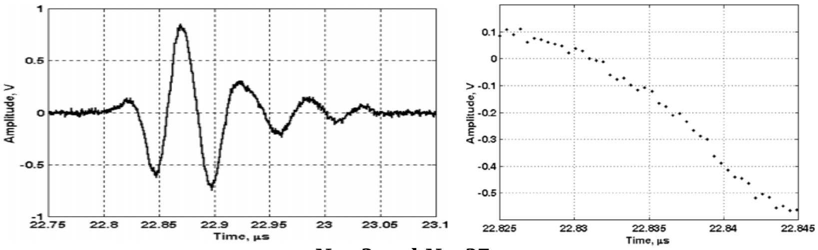
2.5.4 Application examples for ultrasonic NDE

Ultrasonic NDE is used to test the quality of finished products and to monitor the manufacturing processes and image structures of biological objects *in vivo*. These applications differ by the available measurement time budget: assessment of finished articles is very restricted, whilst observing evolving and live processes imposes particular limitations. These limitations are defined by the speed of evolution, as the repeatable signal must not vary much during the complete acquisition time, and by the need to extract the relevant information out of the acquired waveforms, which requires some processing time.

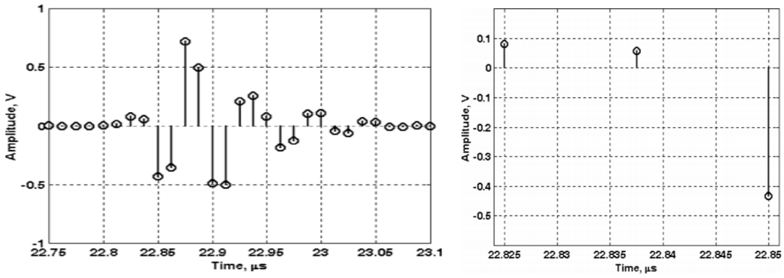
Examples of using acquired ultrasonic waveforms for quality control of hardened steel samples are presented in [52]. This application required substantial values for both N_A and N_I because high ultrasound attenuation in the steel samples lowered the input SNR, and the ultrasound velocity needed to be estimated with rather high resolution [52]. The TDR measurements discussed in [48, Section 4] were characterised by quite low additive noise and they required high time domain resolution, thus, resulting in lower N_A but higher N_I. In the case in which liquid foodstuffs are evaluated for consumption safety, both ultrasound attenuation and velocity were not that high, which allowed for the use of moderate N_A and N_I values [53].



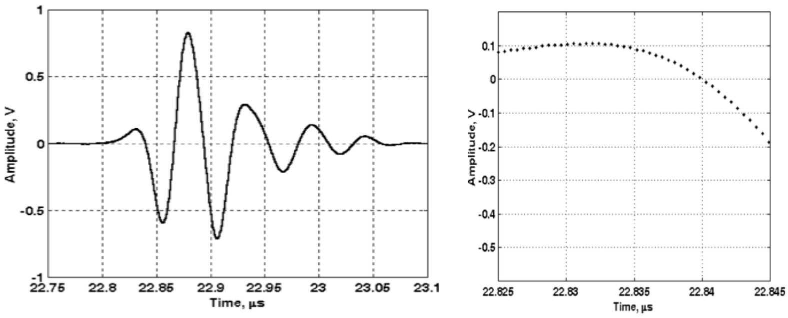
***N_A* =2 and *N_I* =1**



***N_A* =2 and *N_I* =27**



***N_A* =512 and *N_I* =1**



***N_A* =512 and *N_I* =27**

Figure 2.6.Ultrasonic waveforms acquired in the pulse echo mode from a 20 MHz transducer using an 80 MHz clocked ADC for various combinations of N_A and N_I [50, fig.9,10]

The measurement time budget was not found to be very restrictive when the formation of bio-compatible scaffolds in a stainless steel reactor was monitored because the manufacturing process took a substantial amount of time [54]. However, the monitoring of chemical reactions required faster waveform acquisition and processing [55] that was achieved by utilising a processor embedded into the FPGA fabric [56].

Finally, ultrasonic measurements of the intima-media thickness (IMT) of the common carotid artery *in vivo* were found to be the most restrictive. Despite the low input SNR that resulted from weak ultrasound reflections from tissue interfaces in the human body, it was possible to use only very few averages because providing higher N_I became more important for estimating the thickness with high resolution [57].

2.6 Summary and conclusions

This chapter discussed various software/firmware and hardware methods and architectures to improve the fidelity of the acquired waveforms beyond the capabilities of the ADC that is employed by enhancing their vertical and horizontal resolutions, on their own and simultaneously.

Section 2.2 considered which of the horizontal and vertical resolutions are required to achieve high fidelity waveform acquisition. The literature survey indicated that the waveform sampling frequency might need to be as high at 40 times the Nyquist sampling frequency for accurate measurements of the transient times. It was shown by simulation that *sin(x)/x* interpolation widely used for waveform reconstruction could not appropriately compensate for insufficient sampling frequency in the generic case of communication waveform acquisition that was considered. Other simulations showed that eq. 1, which is commonly used for assessment of the required number of ADC bits, needs to be used with care as it was derived for specific operating conditions that are not valid in a general case.

Sections 2.3-2.5 discussed methods for the enhancement of horizontal resolutions, vertical resolutions and both resolutions, simultaneously, depending on the nature of the waveform of interest; namely one-shot, repetitive and repeatable waveforms, respectively. The findings are summarised in the Table 2.1 below. Counter-intuitively, enhancement of the vertical resolution might require injecting extra additive noise at the input of the ADC if that resolution is to occur. It was shown that the best resolution enhancements are achievable for repeatable waveforms at the expense of the increased waveform acquisition time.

TABLE 2.1

<table>
<tr><th></th><th>Vertical resolution</th><th>Horizontal resolution</th></tr>
<tr><td>General</td><td>Every bit of the ADC resolution increases SQNR by 6.02 dB. The exact SQNR value depends upon the parameters of the acquired waveform.</td><td>The sampling frequency should exceed the fundamental frequency of the acquired waveform (or its high spectrum boundary if applicable) by the factor of 4 to 80. Sin(x)/x interpolation might not compensate for the insufficient sampling frequency.</td></tr>
<tr><td rowspan="2">One-shot waveforms</td><td>Can be enhanced by oversampling, provided that enough additive noise is present at the input. If the noise is not present, it should be injected deliberately. We recommend using the noise RMS value slightly above 0.5 LSB.</td><td>Can be enhanced by using time-interleaved ADCs. Individual ADC mismatches should be reduced and/or compensated. Precise clocking of individual ADCs is required.</td></tr>
<tr><td colspan="2">Combining the enhancements is possible.</td></tr>
<tr><td rowspan="2">Repetitive waveforms</td><td>Can be enhanced by ensemble averaging if some additive noise is present, as stated in the entry above. Additionally reduces the additive noise RMS value.</td><td>Can be enhanced by random interleaved sampling (or equivalent time sampling) if the acquired waveform does not change much from one repetition to another during the entire acquisition time. Requires a substantial amount of measurement time and a stable trigger.</td></tr>
<tr><td colspan="2">Combining the enhancements seems very complicated.</td></tr>
<tr><td rowspan="2">Repeatable waveforms</td><td>Can be enhanced by using synchronous digital averaging.</td><td>Can be enhanced using accurate interleaved sampling.</td></tr>
<tr><td colspan="2">Combining the enhancements is straightforward at the expense of the increased acquisition time.</td></tr>
</table>

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