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15.3% efficient graded bandgap solar cells fabricated using electroplated CdS and CdTe thin films

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Abstract

Making use of previously designed and experimentally tested results of graded bandgap devices, and the comprehensive electrodeposition of semiconducting materials knowledge, a three layer n-n-p device structure was fabricated and tested for their electronic properties and solar cell performance. Glass/FTO/n-CdS/n-CdTe/p-CdTe/Au devices were fabricated and studied as a first step towards development of graded bandgap devices using electroplated materials. Efficiencies up to 15.3% were observed for lab-scale small devices.

Keywords: CdS, CdTe, Electroplating of Semiconductors, Graded Bandgap Solar Cells,

Introduction

Photovoltaic (PV) devices are designed and fabricated mainly to harvest all possible photons, and create a useful electrical power output. One of the promising methods for this is a graded bandgap device as summarised and reviewed in a recent publication [1]. At the initial stage, this device architecture was designed to absorb all photons from ultra-violet (UV), Visible and Infra-Red (IR) regions [2] of the solar spectrum. In addition, the impact ionisation and impurity PV (IPV) effect were also built into the device structure in order to increase the photogenerated charge carriers. After experimentally testing these new designs using one of the most researched semiconductor systems, MOVPE grown GaAs/AlGaAs, devices with some excellent solar cell parameters (V_{oc}=1175 mV, FF~0.85) have been observed. These parameters were cross checked by independent measurements in six different reputed solar energy groups [3]. As expected from the new design, the existence of IPV effect was demonstrated in these devices by measuring large V_{oc} values in excess of 750 mV, in complete darkness [4]. Measured IPCE values of 140% for these devices confirmed the active impact ionisation occurring in these devices [1]. Since then other independent groups have also reported over 100% EQE values for their new photovoltaic devices [5,6].

Since the new designs have been experimentally tested with excellent results comparatively within a short period of time, our current efforts are devoted to focus on graded bandgap device architectures fabricated using low-cost materials. In addition to the proven scalability and manufacturability [7], electroplated CdS and CdTe materials offer an additional unique

property of rod-type or columnar-type grains spreading across the layer thickness [8,9]. As explained in a recent review [10], columnar shape grains provide grain boundary enhanced charge carrier separation and collection in thin film solar cells by producing weak internal electric fields around each grain surface and with a perpendicular electric field component to the main internal electric field of the device. This is one of the main features taking place during post-growth annealing in the presence of $CdCl_2$. This situation seems to work for many poly-crystalline thin film solar cells based on CdTe, CIGS or Perovskites when the columnar-type grains of right sizes are produced during the growth and post-growth processing steps. This short communication presents a summary of our preliminary work on entering into multi-layer graded bandgap solar cells development using electroplated CdS and CdTe materials.

Experimental

All materials used in these device fabrications were grown using electroplating. Out of over fifteen semiconductors explored and established in our laboratories, CdS electroplated using $(NH_4)_2S_2O_3$ and $CdCl_2$ precursors [11] and CdTe grown using $Cd(NO_3)_2$ precursor and TeO_2 solution [12] were used to fabricate the devices reported in this letter. Full details of materials growth and characterisation were published before and can be found in references [11] and [12]. In these two material papers structural, morphological, optical and electrical properties have been presented after comprehensive studies for both CdS and CdTe layers. The purpose of this short communication is to present the device results of multi-layer graded bandgap structures fabricated using these layers.

In order to grow n- and p-type CdTe layers required for these devices, previously established knowledge was used in this work [12]. Photoelectrochemical (PEC) cell experiments were carried out to test the electrical conduction of electroplated CdTe layers. In these tests, glass/FTO/CdTe layer was immersed in a suitable electrolyte ($Na_2S_2O_3$ aqueous solution) in order to form a solid/liquid junction. Its open circuit voltage was measured against a counter electrode (graphite rod) immersed in the same electrolyte, by measuring voltages under dark and illuminated conditions. The sign of the open circuit voltage or the PEC signal provides the information on electrical conductivity type, and the system is usually calibrated with a known material like n-CdS layer.

With the known electrical conductivity of CdTe, two types of device structures were fabricated in this work. The p-CdTe grown was used to fabricate conventional glass/FTO/n-CdS/p-CdTe/Au, p-n junction type devices, and n-CdTe grown was used to fabricate novel glass/FTO/n-CdS/n-CdTe/p-CdTe/Au, n-n-p two junction devices. Both these structures were assessed under AM1.5 illuminated conditions for solar cell performance comparison, and the new devices were further analysed by measuring I-V and C-V properties in dark conditions. All these devices were measured using a commercially available fully automated I-V system purchased from Oriel. Solar cell performance measurements were carried out under AM1.5 illumination, and the system was calibrated using a standard reference cell RR267MON provided with this commercial system. C-V measurements were carried out using a fully automated HP system at a detector signal frequency of 1 MHz.

Results and discussion

Figure 1 summarises the most needed information relevant to this material growth and device fabrication. This Figure shows the open circuit voltage of a CdTe/electrolyte junction or the PEC signal against the CdTe growth voltage, V_g. The V_g value in this figure is the cathodic voltage with respect to a graphite anode used in a 2-electrode electrodeposition system. Figure 1 shows the stoichiometric and intrinsic CdTe layers are deposited at a voltage V_i. CdTe layers grown at cathodic voltages below V_i are rich in Te and therefore electrical conduction is p-type (see Figure 1 (a) and (b)).

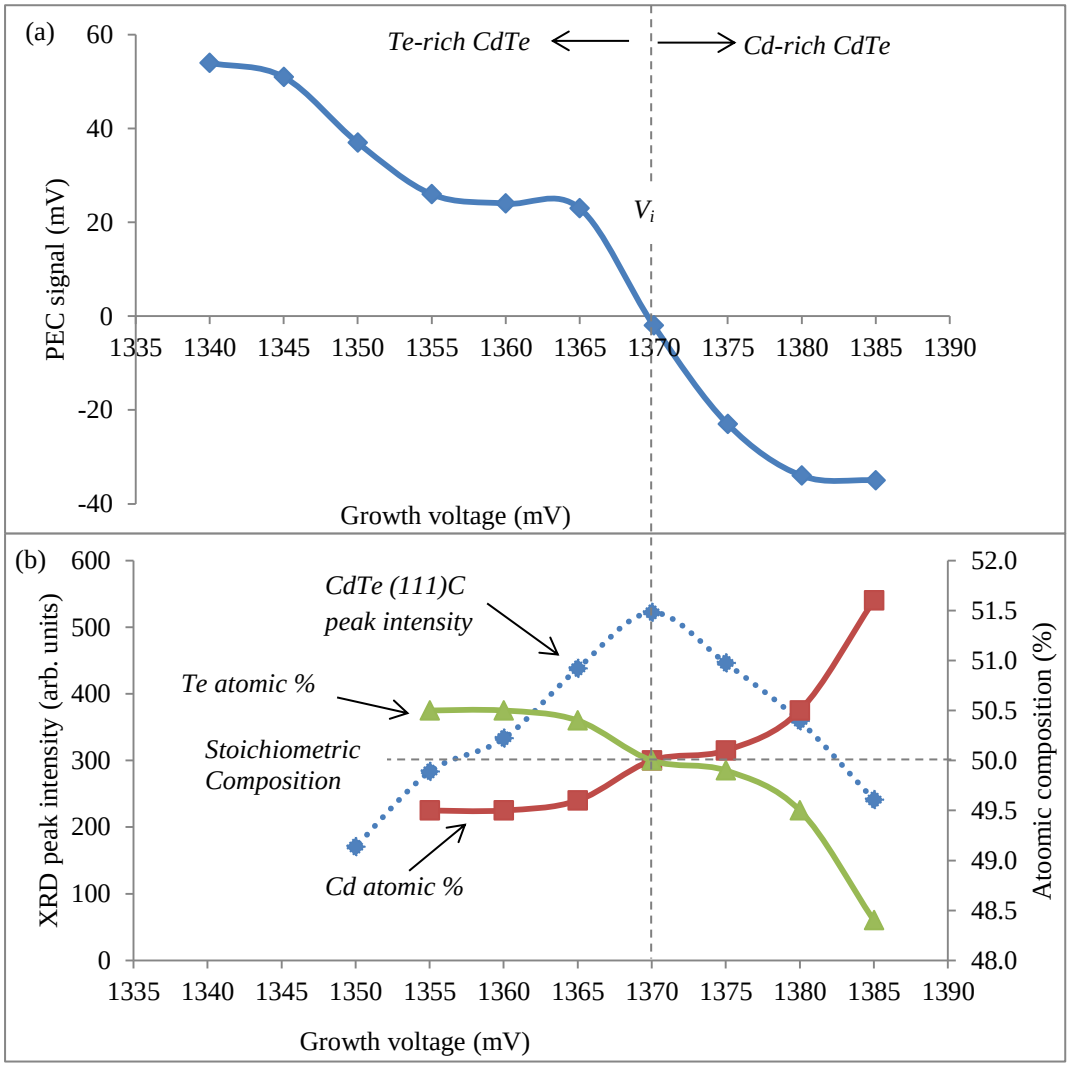

Figure 1: (a) PEC signals and (b) (111) XRD peak intensity for cubic CdTe and atomic composition of CdTe layers grown at different cathodic potentials between 1340 mV and 1385 mV, from electrolyte containing $Cd(NO_3)_2$ and TeO_2 solution [12]. The p- to n- transition and the highest crystallinity of CdTe occurs at the growth voltage of V_i when the composition change from Te-richness to Cd-richness.

Layers grown at voltages greater than V_i, are rich in Cd and electrical conduction becomes n-type. At V_i, the layer has only one phase, CdTe and is stoichiometric and therefore the crystallinity is maximum. The dotted curve shown in Figure 1(b) with a maximum at V_i, shows the summary of a large number of our XRD results indicating the variation of the highest intense peak of (111) CdTe. In order to produce material layers with minimum defects, the growth voltage should be very close to the V_i, to keep the crystalline nature high in CdTe layers. In this work, p-CdTe and n-CdTe required for device fabrication were grown at voltages, a few mV below and above the V_i respectively.

Figure 2(a) shows the schematic diagram of the novel device structure fabricated and tested in this work. The full device consisted of three semiconducting layers as in; glass/FTO/n-CdS (~150 nm)/n-CdTe (~1144 nm)/p-CdTe (~35 nm)/Au. The thickness used for different layers are also indicated, and a thick n-CdTe layer was used mainly due to our previous experimental observations reported in reference [13]. This work indicated that superior solar cells arise from device configurations with Cd-rich n-type CdTe rather than Te-rich p-type CdTe as the main absorbing layer. The energy band diagram of this device structure is shown in Figure 2(b) and a thin p-CdTe (~35 nm) layer was used only to fix the Fermi level closer to the valence band maximum, so that a healthy band bending occurs throughout the device structure. It should be noted that the n- and p-CdTe layers were grown very close to V_i using the same bath in order to keep the crystallinity high, remove additional interface states and therefore to minimise native defects. After growing n-type CdTe at a $V_g>V_i$, the growth voltage was simply changed to $V_g<V_i$, in order to grow a thin p-type CdTe layer. This doping is simply achieved by changing the stoichiometry of the layers rather than using any external doping agent.

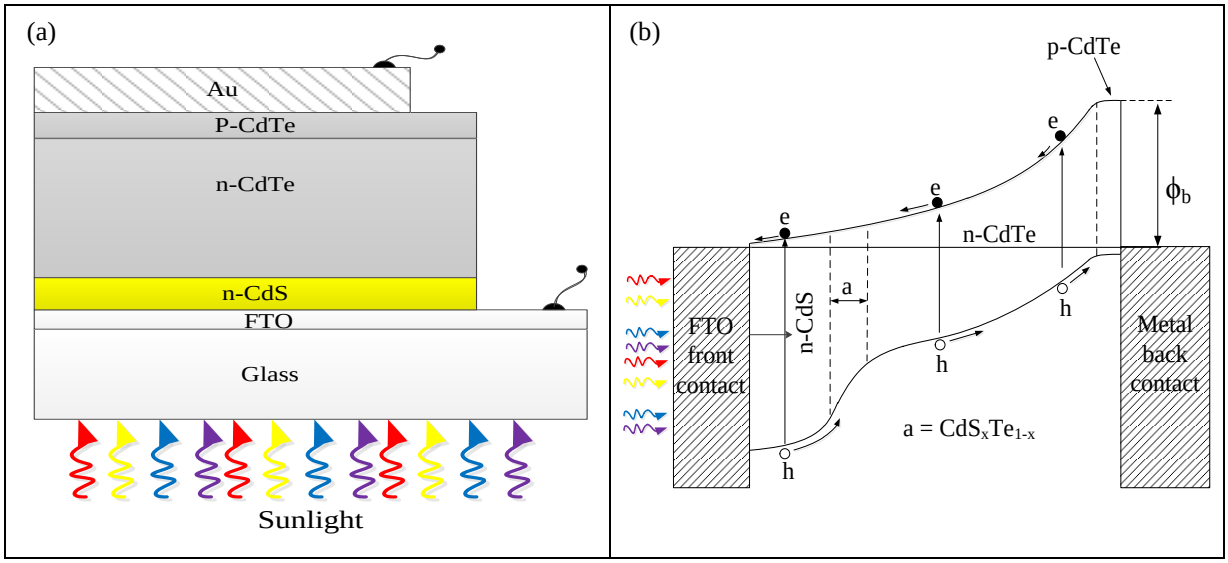

Figure 2: (a) Schematic diagram and (b) energy band diagram of the glass/FTO/n-CdS/n-CdTe/p-CdTe/Au thin film solar cell.

Conventional p-n junction type devices were also fabricated using glass/FTO/n-CdS/p-CdTe/Au structures. The p-CdTe required was grown at $V_g<V_i$ value and the thickness was kept at ~1144 nm for device comparison. The CdS layer thickness was also kept at ~150 nm

and all other processing steps were similar for both device structures. The schematic diagram and the energy band diagram of this device are not shown due to the familiarity of this well-known simple device structure.

Both device structures underwent similar processing steps during fabrication. The CdS layers used were heat treated at 420°C for 20 minutes in air, and the CdTe layers grown were $CdCl_2$ treated using usual manner (dipped in $CdCl_2$ solution, dried and heat treated at 450°C for 10 minutes in air). Circular Au contacts of 2 mm diameter, were evaporated on to chemically etched CdTe surfaces using acidic (dilute chromic acid) etch followed by alkaline ($Na_2S_2O_3$ and NaOH aqueous solution) etch.

All n-p and n-n-p devices were measured using the same system under identical conditions. Table 1 shows the solar cell parameters measured for the best devices for two types of device structures for comparison.

Table 1: Summary of cell parameters measured under AM1.5 illumination conditions, for n-p and n-n-p device structures.

Device	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF	Efficiency (%)
n-p	620	22.0	0.47	6.4
n-n-p	730	33.8	0.62	15.3

Since our aim is to explore the properties of novel devices with higher efficiencies, detailed measurements were carried out only on n-n-p device structures. In a typical experimental sample, about 36, 2 mm diameter Au contacts can be made. The statistics of efficiency values are plotted in Figure 3 and the scatter of efficiency is wide for this preliminary work. This non-uniform behaviour could arise due to several factors such as non-uniform FTO layer, materials growth and processing steps. While the work is progressing to improve reproducibility, consistency and uniformity, the device parameters of the best device observed with efficiency of 15.3% is studied in details and presented in this communication.

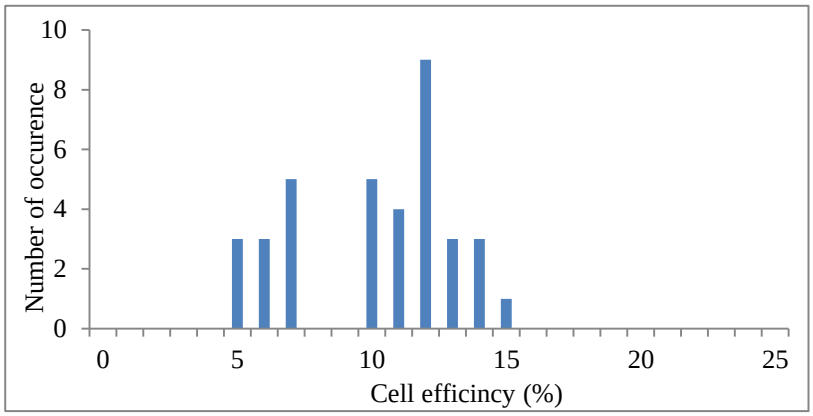

Figure 3: Statistics showing the cell efficiency distribution of n-n-p devices investigated in this preliminary work.

Figure 4 shows the I-V characteristics of the best device measured under dark condition. These were plotted in both linear-linear and log-linear scales, in order to extract important device parameters, and these are summarised in Table 2. Rectification factor (RF) at 1.00 V exceeds 4 orders of magnitude, indicating excellent rectifying quality of this device. Potential barrier height available in this structure for electron transport is greater than 0.80 eV, but the real value is under estimated due to a large ideality factor of 1.86.

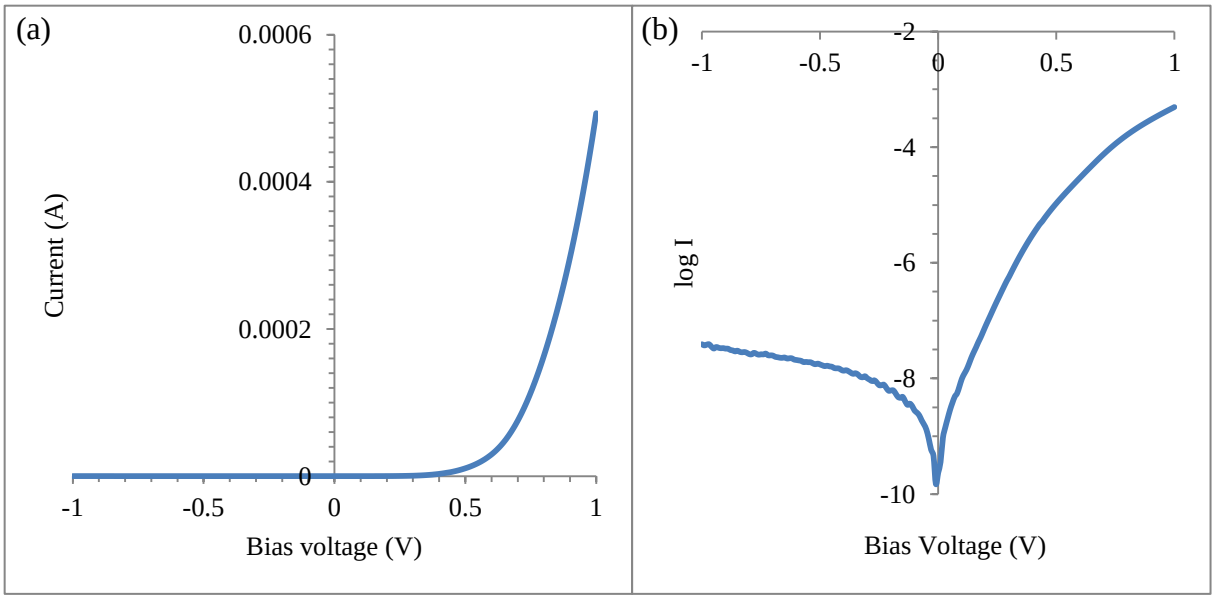

Figure 4: Current-Voltage curves plotted using (a) linear – linear and (b) log – linear scales for the best solar cell measured in the batch.

Table 2: Summary of the device parameters measured under dark condition for the highest efficiency solar cell.

RF	n	I_0(A)	φ_b(eV)	R_s(Ω)	R_{sh}(Ω)
$10^{4.1}$	1.86	10^{-9}	>0.80	500	7.2×10^{5}

In order to further investigate the properties of the depletion region and the doping concentration of the material, dark C-V measurements were carried out at a signal frequency of 1.0 MHz. Figure 5 shows the variation of capacitance as a function of bias voltage and corresponding Mott-Schottky plot for highest performing device. It is clear from the shape of the C-V curve that the device is fully depleted at reverse biased and close to zero biased voltages. As the device is forward biased, and voltage is increased, the depletion width, W becomes equals to the thickness of the device which is ~1.2 µm, around forward bias voltage of ~0.5 V. After this voltage, the capacitance increase with the increasing forward bias voltage, gradually reducing the depletion region. This variation behaves according to Mott-Schottky theory and provides estimates for diffusion voltage of the device (V_{bi}) and the

excess donor concentration (N_D-N_A) for n-CdTe layer. The data estimated are given in Table 3, and the V_{bi} of ~1.0 eV and (N_D-N_A) ~6.7×10^{14} $cm^{-3}$are most acceptable for this device. V_{bi} ~1.0 eV corresponds to a potential barrier height of ~1.10 eV and the doping concentration comes in the region corresponds to the high efficiency CdTe devices (~1.0×10^{14} - 5×10^{15} cm^{-3}) reported in the past [14-16].

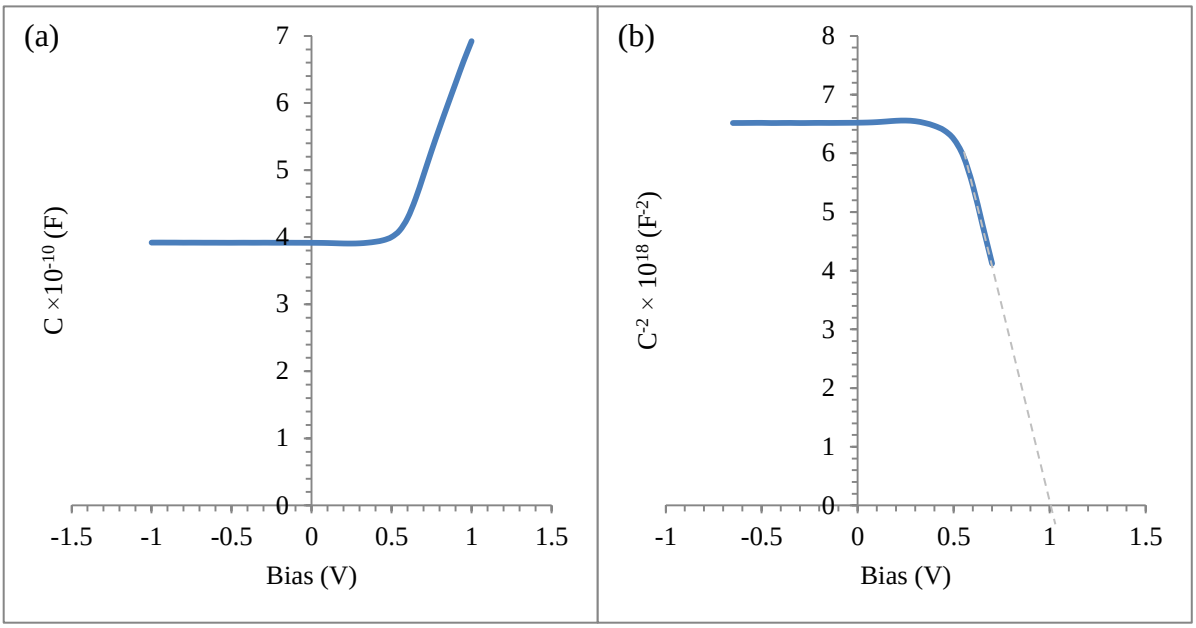

Figure 5: (a) Capacitance-voltage plot and (b) Schottky–Mott plot under dark conditions for the cell with highest conversion efficiency of 15.3%.

Table 3: Summary of device and material parameters obtained for 15.3% efficiency solar cell.

Zero bias Capacitance (pF)	Geometrical Capacitance (pF)	Built in Potential (V_{bi}) eV	Doping density (N_D-N_A) cm^{-3}
395	238	1.00	6.67×10^{14}

Figure 6(a) shows the J-V curve recorded under AM1.5 condition for the best solar cell measured, giving V_{oc}=730 mV, J_{sc}=33.8 $mAcm^{-2}$, FF=0.62 and conversion efficiency of 15.3%. Figure 6(b) shows an IPCE curve for a device with efficiency ~10% from the same batch. This shows the PV active nature of these n-n-p devices in the wavelength range between 300 nm and 880 nm, with a peak ~500 nm.

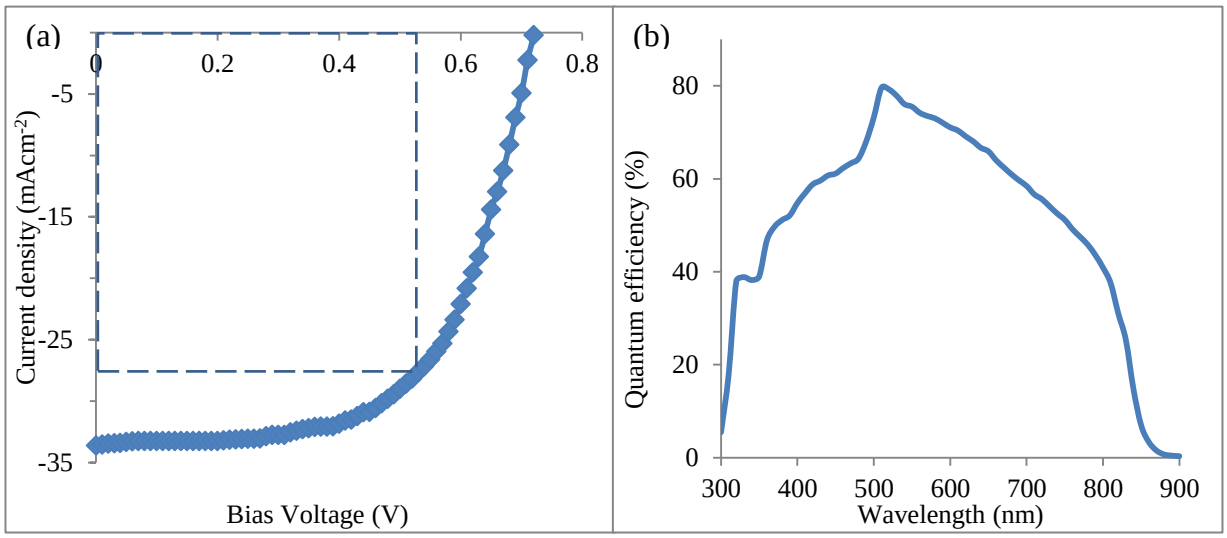

Figure 6: (a) J-V plot of the cell with highest efficiency under AM1.5 condition and (b) A typical IPCE curve for cells with efficiency of ~10%.

As indicated by the statistics shown in Figure 3, for these preliminary devices, it is clear that the uniformity of device parameters and consistency need improving. However, the best devices showing 15.3% efficiency for this three layer n-n-p device shows the high potential of achieving further improvements with materials and processing optimisation. The series resistance of 500 Ω measured for the best device is high and reduction of this should further improve the FF and the short circuit current density. This work is only the first step towards development of graded bandgap solar cells using only three layers. Bandgap grading takes place only in the CdS/CdTe interface during $CdCl_2$ treatment, in this device structure, and the work on multi-layer devices are in progress.

Conclusions

The work presented in this short communication successfully combined the knowledge acquired from two different research fronts; electrodeposition of semiconductors and the graded bandgap device structures. Without making any ambiguous assumptions, n-p and n-n-p device structures were fabricated using well studied electroplated n-CdS, n-CdTe and p-CdTe layers. As expected, these preliminary studies on n-n-p structures produced PV active devices showing best efficiencies of 15.3%, and perform much better than simple n-p junction type devices. Both I-V, C-V and IPCE measurements confirm promising devices capable of developing into multi-layer graded bandgap solar cells in order to harvest most of the photons available to achieve highest possible conversion efficiency. Work is progressing along these lines.

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