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This paper presents the architectures, theoretical analyses and testing results of modified time delay digital tanlock loops (TDTLs) systems. The modifications to the original TDTL architecture were introduced to overcome some of the limitations of the original TDTL and to enhance the overall performance of the particular systems. The limitations addressed in this paper include the nonlinearity of the phase detector, the restricted width of the locking range, and the overall system acquisition speed. Each of the modified architectures was tested through subjecting the system to sudden positive and negative frequency steps and comparing its response with that of the original TDTL. In addition, the performance of all the architectures was evaluated under noise-free as well as noisy environments. The extensive simulation results using MATLAB/SIMULINK demonstrate that the new architectures overcome the limitations they addressed and the overall results confirmed significant improvements in performance compared to the conventional TDTL system.

Keywords: Acquisition speed, DPLL, jitter, lock range, noise, TDTL.

1. Introduction

Synchronization between two electrical signals is fundamental to the proper operation of many electronic systems such as communications, signal processing and control systems (Chyun and Hung, 1996; Lindsey and Chak,1981; Gardner, 2005). Achieving this kind of synchronization has been achieved using phase-locked loops (PLL) (Terng-Yin, Bai-Jue, and Chen-Yi,1999; Best,2007;Crawford,2007). More recently, in the area of renewable energy and localized power generation (Pearce, Al Zahawi, and Shuttleworth, 2001;Pearce,Al Zahawi, Auckland,and Starr, 1996), PLLs are primarily used for the synchronization of local generators with the low voltage utility grid (Anani, Al-Kharji Al-Ali, Ponnapalli, Al-Araji, and Al-Qutayri,2012a, 2012b).

Fundamentally, a PLL is an electronic system which operates by detecting the difference in phase between an incoming signal and the output signal of a local voltage controlled oscillator (VCO) (Gardner, 2005). The result of this detection is subsequently employed to minimize or eliminate the phase difference between the said signals so as to achieve locking.

Advances in digital and integrated circuit technologies, led to the development of digital PLLs (DPLLs), which are typically classified as either uniform or a non-uniform based on the sampling technique they use to sample analogue signals. Non-uniform DPPLs are more attractive due to the ease of their modelling and circuit implementation (Lindsey, 1981). The zero-crossing Digital phase-locked loop (ZCDPLL) and the DTL (Jae, and Chong, 1982; Hussain, Boashash, Hassan-Ali, and Al-Araji, 2001; Al-Araji, Al-Qutayri, and Al-Moosa, 2004; Al-Kharji Al-Ali et al., 2012a) are examples of the non-uniform DPLLs. The advantages of the DTL include good linearity and reduced sensitivity to variations in the power of the input signal. However, the DTL uses a Hilbert Transformer (HT), which is clearly a disadvantage due to its implementation complexity (Guan-Chyun, and Hung, 1996). Later, this implementation issue was alleviated by the introduction of the time delay digital tanlock loop (TDTL) (Hussain et al., 2001; Al-Kharji Al-Ali et al., 2012b) in which the HT was replaced by a fixed time delay unit, Figure 1.

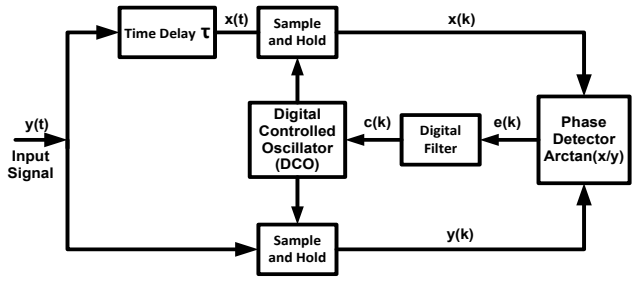


Figure 1. Block diagram of the first-order TDTL architecture.

However, the conventional TDTL has few shortcomings that limit its performance. These include the nonlinearity of the phase detector and the finite non-zero phase error in the locked state of the first-order TDTL system. Additionally, the second-order loop has a limited locking range and acquisition speed that can be improved. In this paper, new TDTL architectures are presented so as to mitigate these

limitations. Comparison between the performances of the original TDTL and the proposed architectures are also presented. Tests were performed using a variety of input signals under noisy and noise-free conditions.

Section 2, of this article, gives the mathematical analysis of the original TDTL and its MATLAB/Simulink simulation results are given in Section 3. The fundamental limitations of the basic TDTL are analysed in details in Section 4. New improved TDTL architectures are also presented in this section. The performance of these new architectures in noisy environment is presented in Section 5. Finally, the paper is concluded in Section 6.

2. TDTL Mathematical Analysis

In this section, the TDTL is mathematically modelled and analyzed under noise-free environment. The analysis is based on the model presented in (Jae, and Chong,1982; Al-Kharji Al-Ali et al., 2012). The TDTL loop takes an input sinusoidal signal $y(t)$ with a frequency offset $\Delta\omega = (\omega - \omega_o)$, which is converted to a phase shift. This phase shift is measured with respect to the free-running frequency ω_o of the DCO (digital controlled oscillator) as described below

$$y(t) = A\sin\left[\omega_o t + \theta(t)\right] \tag{1}$$

where A is the amplitude of the signal and $\theta(t) = \Delta\omega t + \theta_o$ is its phase process, whilst θ_o is a constant. The input signal is passed through a time delay unit τ, as indicated in Figure 1, which produces a variable phase shift 'lag' $\psi = \omega\tau$ whose value depends on the frequency of the input signal. As a result, a phase shifted signal $x(t)$ of the incoming signal is produced as

$$x(t) = A\sin\left[\omega_o t + \theta(t) - \psi\right] \tag{2}$$

The input and the phase shifted signals are passed through their corresponding sample

and hold blocks as depicted Figure 1. As a result, sampled versions of the signals are generated as

$$y(k) = A\sin\left[\omega_o t(k) + \theta(k)\right] \tag{3}$$

and

$$x(k) = A\sin\left[\omega_o t(k) + \theta(k) - \psi\right] \tag{4}$$

where $\theta(k) = \theta\left[t(k)\right]$

The sampling period between the sampling instants $t(k)$ and $t(k-1)$ is

$$T(k) = T_o - c(k-1) \tag{5}$$

where $T_o = 2\pi/\omega_o$ is the nominal period of the DCO whilst $c(i)$ is the output of the digital loop filter at the i[th] sampling instant. Assuming $t(0) = 0$, the required time to the k[th] sampling instant may be written as

$$t(k) = \sum_{i=1}^{k} T(i) = kT_o - \sum_{i=0}^{k-1} c(i) \tag{6}$$

Consequently, both $y(k)$ and $x(k)$ may be expressed as

$$y(k) = A\sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)\right] \tag{7}$$

and

$$x(k) = A\sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi\right] \tag{8}$$

As a result, the phase error, or difference, between the input signal and output signal of the Digital Controlled Oscillator can be expressed as

$$\phi(k) = \theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi \tag{9}$$

Hence, the above two equations can be given in terms of the phase error as

$$y(k) = A\sin\left[\phi(k) + \psi\right] \tag{10}$$

and

$$x(k) = A\sin[\phi(k)] \tag{11}$$

The arctan phase detector generates the loop error signal $e(k)$ as

$$e(k) = f\left[\tan^{-1}\left(\frac{sin[\phi(k)]}{sin[\phi(k)+\psi]}\right)\right] \tag{12}$$

where $f(\gamma) = -\pi + [(\gamma + \pi) mod\, 2\pi$. This error signal $e(k)$has a nonlinearity which deteriorates as the phase shift ψ departs further from the value of $\pi/2$ (rad). The digital loop filter whose a transfer function $D(z)$ accepts the error $e(k)$ and generates the signal $c(k)$ that forces the DCO to the required frequency. Subsequently, the difference equation of the system can be derived from equations (6) and (9) as

$$\phi(k+1) = \phi(k) - \omega c(k) + \Lambda_o \tag{13}$$

where $\Lambda_o = 2\pi(\Delta\omega/\omega_o)$. Because of the nonlinearity caused by variations in the phase shift ψ due to changes in the amplitude of the input signal, it is not possible to solve the system difference equation using the Z transform, which is necessary to obtain the locking range as has been done for the DTL(Hussain, Boashash, Hassan-Ali, and Al-Araji, 2001). Therefore, a numerical solution using the fixed-point theorem (Best 2007;Hussain et al., 2001) can be used to solve the difference equation similar to the case of the ZC-DPLLs (Osborne,1980a,1980b). The analyses for first-order and second-order TDTL systems are presented below.

The system difference equation of first-order TDTL loop is given by equation (14) with the digital filter transfer function $D(z)$ is simply a gain block G_1,

$$\phi(k+1) = \phi(k) - K_1' h[c(k)] + \Lambda_o \tag{14}$$

where $K_1' = \omega G_1$, if K_1 defined as $\omega_o G_1$,then $K_1' = K_1/W$ where $W = \omega_o/\omega$. Therefore, the locking range can be given as

$$2|1-W| < K_1 < 2W\,\frac{sin^2(\alpha) + sin^2(\alpha+\psi)}{\sin(\psi)} \tag{15}$$

$$2|1-W| < K_1 < 2W \frac{sin^2(\alpha)+sin^2(\alpha+\psi_o/W)}{\sin(\psi_o/W)} \tag{16}$$

where ψ_o is the nominal phase lag introduced on the incoming signal by the time delay unit, $\alpha = tan^{-1}(\beta)$, $\eta = \Lambda_o / K_1'$ and

$$\beta = \frac{[\sin(\psi)tan(\eta)]}{[1-cos(\psi)tan(\eta)]} = \frac{[\sin(\psi)]}{[cot(\eta)-cos(\psi)]}$$

The locking range of the first-order TDTL with a nominal phase shift $\pi/2$ is shown in Figure 2.

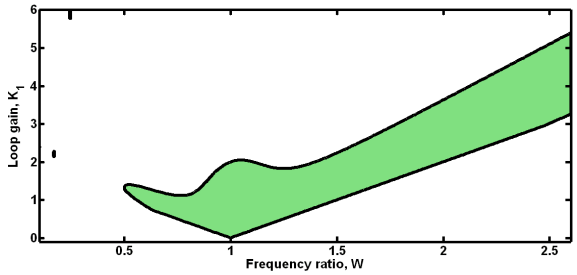


Figure 2 The locking range of first-order TDTL. $K_1 = G_1\omega_o$ and $W = \omega_o/\omega$.

The second-order TDTL, shown in Figure 3, uses a proportional accumulation digital filter whose transfer function $D(z)$ is

$$D(z) = G_1 + G_2/(1-z^{-1}) \tag{17}$$

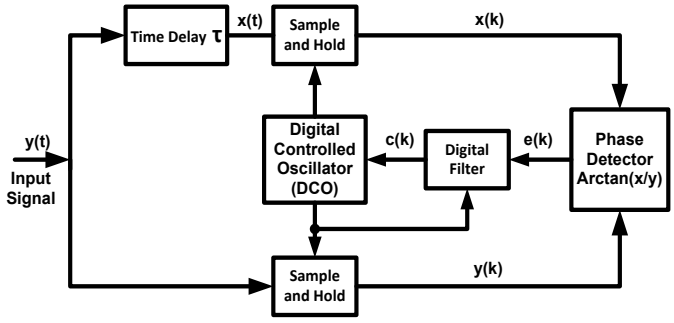


Figure 3 Block diagram of the second-order TDTL architecture.

where G_1 and G_2 are positive constants. Using equations (13) and (17), the difference equation of the system of the TDTL system can be expressed as

$$\phi(k+2) = 2\phi(k+1) - \phi(k) - rK_1'e(k+1) + K_1'e(k) \quad (18)$$

where $r = 1 + G_2 / G_1$ and $K_1' = K_1'\omega$.

Following similar approach to that in (Hussain et al., 2001) with a fixed-point analysis as in (Al-Araji et al., 2004) the locking range of the second-order TDTL, Figure 4, may be written as

$$0 < K_1 < \frac{4}{1+\mathrm{r}} \; W \; sin\left(\frac{\psi_o}{W}\right) \quad (19)$$

3. First- and Second-order TDTL Simulation Results

The performance of the first-order loop, presented in Figure 1, was extensively tested using input signals with sudden frequency changes relative to the free running frequency of the DCO. When the change in the input frequency makes it higher than that of the DCO, the change will be represented as a positive step, otherwise it is indicated as a negative step. For testing purposes, the time delay and the DCO free running frequency values have been chosen so that the initial phase lag parameter $\psi_o = \omega_o \tau = \pi / 2$ and the gain $\mathrm{K_1} = \mathrm{G_1}\omega_o = 1$.

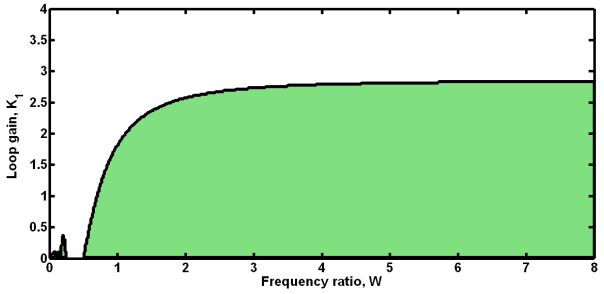
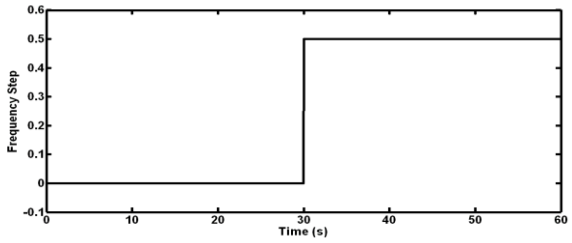


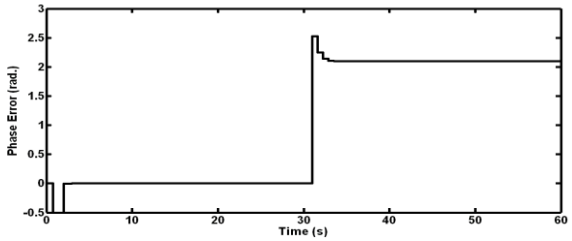
Figure 4 The second-order TDTL locking range (r =1.2 $K_1 = G_1\omega_o$ and $W = \omega_o / \omega$).

Figure 5 shows the effect of applying a positive input frequency step of 0.5 V ($\mathrm{W} = \omega_o / \omega_{in} = 0.667$) to the loop, whilst, Figure 6 shows the results of applying a negative input step of -0.3 V that corresponds to $\mathrm{W} = \omega_o / \omega_{in} = 1.428$. As can be seen from both figures, the phase response of the first-order TDTL converged to steady-

state within the time of few samples. However, this time may not be acceptable for some applications requiring fast acquisition speeds. Hence, increasing the acquisition speed is an important goal for a PLL engineer. An additional goal is to minimise/eliminate the finite phase error of the first-order TDTL loop. Albeit, this goal can be achieved using a second-order loop, this will be at the cost of degradation in the acquisition performance and the locking range as will be demonstrated below.



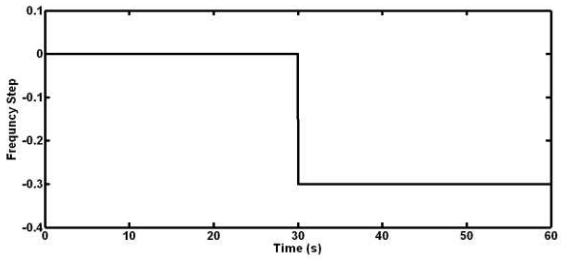
(a)



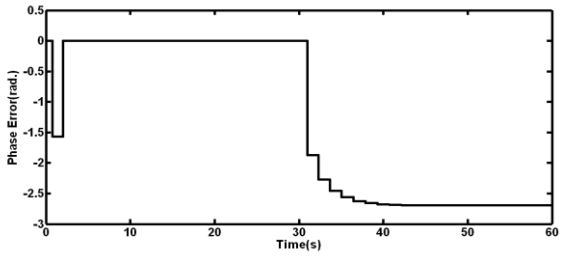
(b)

Figure 5 (a) A 0.5 V input step and (b) first-order TDTL phase-error response.

Similar tests were also carried out to evaluate the performance of the second-order TDTL system of Figure 3. The results of the phase error tests are shown in Figure 7 and 8, which show that the steady-state error of the second-order loop converges to zero. Clearly, improving the loop locking speed is desirable as some applications require fast synchronization.



(a)



(b)

Figure 6 (a) Negative input step of -0.3 V and (b) phase error response of the first-order TDTL.

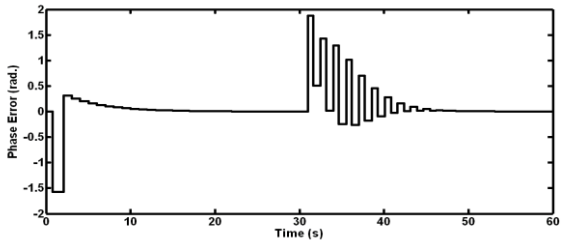


Figure 7 Phase error response of the second-order TDTL for a positive input frequency step of 0.3 V.

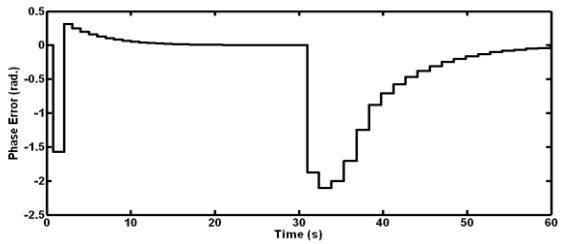


Figure 8 Phase error response of the second order TDTL for a negative input frequency step of -0.3 V.

4. Improvements to the Original TDTL

The analytical system models and the simulation results given earlier for the first- and second-order TDTLs show that the system has some constraints, which when overcome, the performance of both loops will be enhanced. The main system limitations that need to be addressed are:

- The nonlinearity in the first- and second-order TDTLs. This is attributed to having a fixed-time delay unit that results in different phase shifts for different input frequency signals.

- The second-order TDTL has a rather restricted locking range which can be extended.
- The first-order TDTL has relatively low acquisition speed, which can be improved.
- Phase-error convergence to zero of the second-order TDTL phase error tends to take a relatively long time.
- The non-zero steady-state phase error of the first-order TDTL is an obvious disadvantage.

The subsections below propose new TDTL system architectures that overcome the above limitations of the original TDTL.

4.1 TDTL with new linear phase detector

The fixed-time delay is the primary source of nonlinearity and it severely influences the locking range of the TDTL system. The idea of eliminating this nonlinearity problem by substituting the fixed-time delay block with a variable time delay unit has been proposed in the paper (Al-Qutayri, Al-Araji, Al-Kharji Al-Ali, and Anani, 2009). In this article, an improved TDTL equipped with a linearized phase detector (TDTL-LPD) is proposed as shown in Figure 9. It incorporates a controller for phase linearization as well as a variable 'adaptive' time delay block.

The phase linearization controller in the TDTL-LPD estimates the error caused by fluctuations in the frequency of the incoming signal during the time the loop is in locked condition. This estimate is then used to compensate for the non-linear changes in the phase by fine-tuning the adaptive time delay unit in order to preserve the quadrature relationship between the input signal $y(t)$ and its quadrature version $x(t)$.

The idea of the TDTL-LPD can be explained by examining the phase shift relationship with the incoming signal

$$\psi = \omega\tau \tag{20}$$

Where ψ (rad) is the phase shift, ω (rad/s) is the frequency and τ (s) is the time delay initiated by the variable time-delay unit.

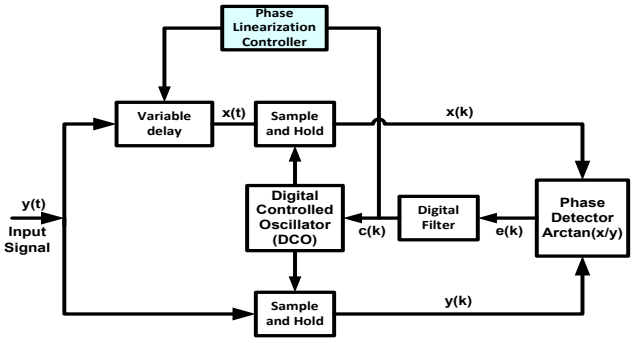


Figure 9 Architecture of the conventional first order TDTL-LPD.

The phase linearization controller in the TDTL-LPD compensates for changes in the input frequency to yield a fixed phase shift ψ (rad) while the system is working inside its nominal locking range. Consequently, variations in the input signal frequency will be counteracted by a suitable value of delay generated by the controller in order to uphold a $\pi/2$ (rad) phase shift. As shown in equation (21), for any rise in the incoming signal frequency, there will be a reduction in the time delay to keep the phase shift ψ fixed at $\pi/2$ (rad) as demonstrated in Figure 10.

$$\psi = \omega\tau = 2\times\pi\times f\times\tau = \frac{\pi}{2}\ rad \tag{21}$$

A comparison between the phase detector characteristics of the conventional TDTL and the TDTL-LPD is depicted in Figure 11. The TDTL has nonlinear parts while the TDTL-LPD follows a straight line, which indicates the nonlinearities have been eradicated.

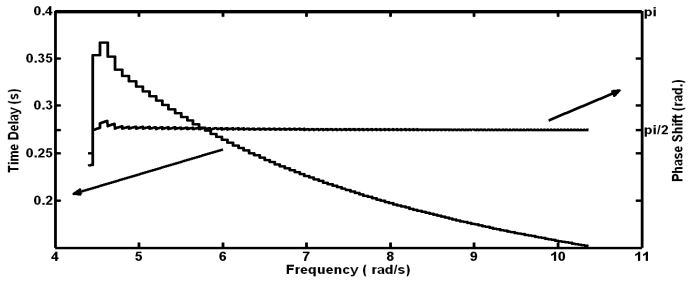


Figure 10 Variation in the required time delay with the input signal frequency to preserve a phase shift of $\pi/2$ (rad).

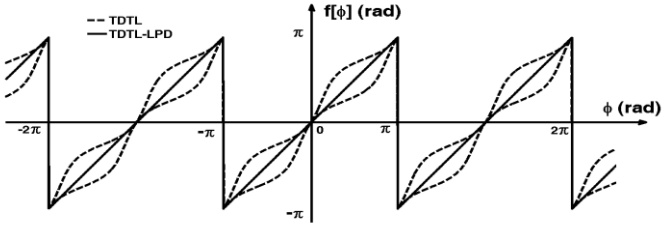


Figure 11 Characteristics the TDTL-LPD and TDTL phase detectors.

Preserving the phase shift at the value of $\pi/2$ (rad) , means that the phase shifted incoming signal $x(k)$, of equation (4), can be expressed as

$$x(k) = A\sin\left[\omega_o t(k) + \theta(k) - \frac{\pi}{2}\right] = A\cos\left[\omega_o t(k) + \theta(k)\right] \tag{22}$$

This is similar to the DTL in (Gloria, Grosso, Olivieri, and Restani,1999), therefore, the discretized signals generated by the samplers are

$$y(k) = A\sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)\right] \tag{23}$$

then

$$x(k) = A\cos\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)\right] \tag{24}$$

Consequently, both (23) and (24) can be re-written in terms of the phase error as

$$y(k) = A\sin\left[\phi(k)\right] \tag{25}$$

and

$$x(k) = A\cos\left[\phi(k)\right] \tag{26}$$

The loop error $e(k)$ at the output of the phase detector may be evaluated by (27).

$$e(k) = f\left[\tan^{-1}\left(\frac{sin[\phi(k)]}{cos[\phi(k)]}\right)\right] = f[\phi(k)] \tag{27}$$

where $f(\gamma) = -\pi + [(\gamma + \pi) mod\, 2\pi]$. Consequently, the first-order TDTL's locking range (Jae, and Chong,1982; Al-Qutayri et al., 2009), can be given as

$$2|1 - W| < K_1 < 2W \frac{sin^2(\alpha) + sin^2(\alpha + \frac{\pi}{2})}{\sin(\frac{\pi}{2})} \tag{28}$$

$$2|1 - W| < K_1 < 2W \frac{-2}{(-2 + \cos(2\alpha) + \cos(\pi + 2\alpha)} \tag{29}$$

which can be simplified as

$$2|1 - W| < K_1 < 2W \tag{30}$$

In case of the second-order TDTL-LPD, equation (19) may be expressed as

$$0 < K_1 < \frac{4}{1+\mathrm{r}}\ W\ sin\left(\frac{\pi}{2}\right) \tag{31}$$

$$0 < K_1 < \frac{4}{1+\mathrm{r}}\ W \tag{32}$$

Both first- and second-order TDTL-LPD locking range with a fixed phase shift of $\pi/2$ (rad) is shown in Figure 12 and 13. As demonstrated below, the TDTL-LPD response outperforms that of the conventional TDTL.

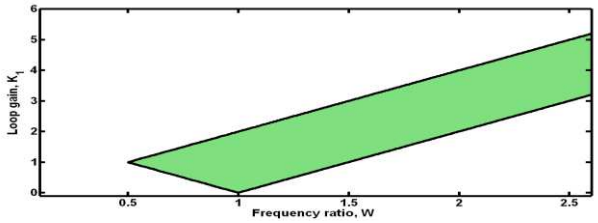


Figure12 First order TDTL-LPD locking rang, $K_1 = G_1\omega_o$, $W = \omega_o/\omega$ and $\psi = \pi/2$ (rad).

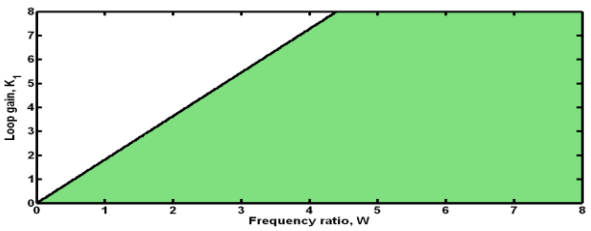
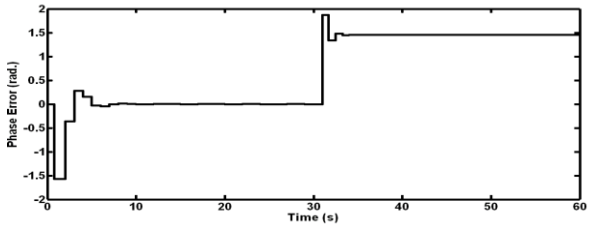
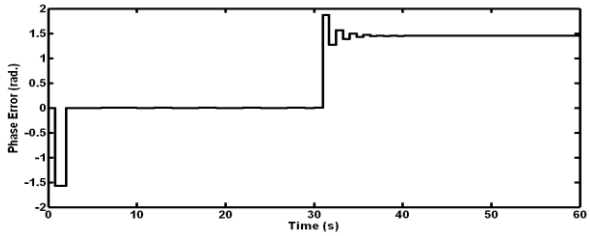


Figure13 Second-order TDTL-LPD locking range with (r=1.2), $K_1 = G_1\omega_o$, $W = \omega_o/\omega$ and $\psi = \pi/2$ (rad).

The responses of first-order TDTL-LPD and the TDTL to the injection of positive and negative frequency steps are shown in Figure 14 and 15 respectively. It can be seen from the figures that the TDTL-LPD requires less number of samples to achieve locking state compared to the TDTL.

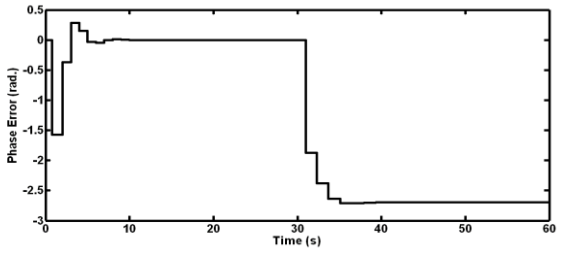


(a)

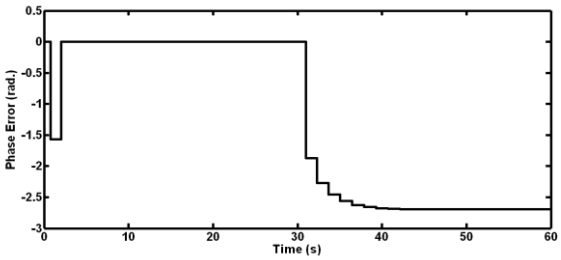


(b)

Figure14 Phase error responses for positive input frequency step of 0.3 V (a) first-order TDTL-LPD and (b) first-order TDTL, $K_1 = G_1\omega_o$, $W = \omega_o / \omega$ and $\psi = \pi/2$ (rad).



(a)

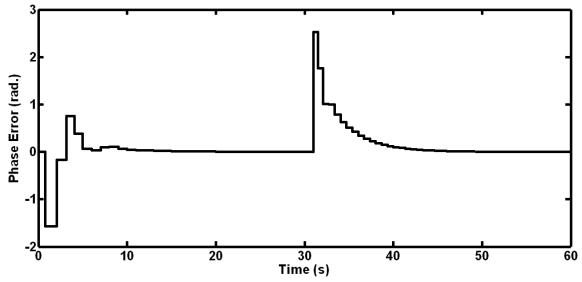


(b)

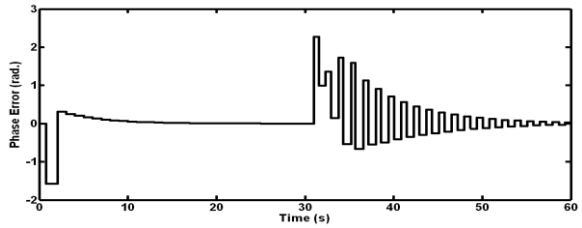
Figure15 Phase error response for negative input frequency step of -0.3 V (a) first-order TDTL-LPD and (b) first-order TDTL, $K_1 = G_1\omega_o$, $W = \omega_o / \omega$ and $\psi = \pi/2$ (rad).

Both Figures 14 and 15 demonstrate the enhancement in the acquisition time of the first-order TDTL-LPD architecture, which is obtained by using a fixed phase shift value for all incoming signal frequencies, which consequently linearizes the phase detector.

The evaluation of the response of the second-order TDTL-LPD followed a similar approach to that of the first-order. The responses of the TDTL-LPD and the TDTL to the application of positive and negative frequency steps are shown in Figure 16 and 17 respectively.

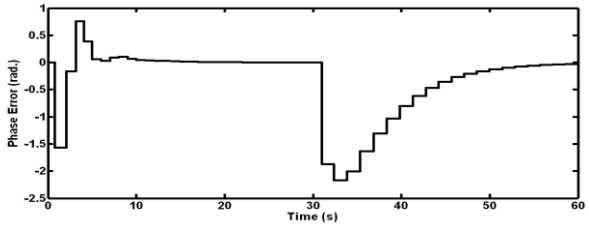


(a)

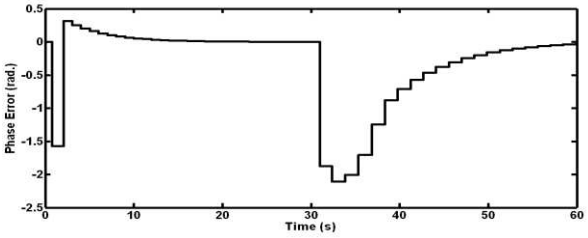


(b)

Figure16 Phase error response for positive input frequency step of 0.4 V (a) second-order TDTL-LPD and (b) second-order TDTL, $\psi = \pi / 2$ (rad), r =1.2 and $K_1 = 1$.



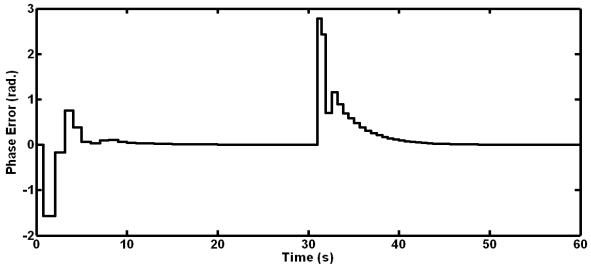
(a)



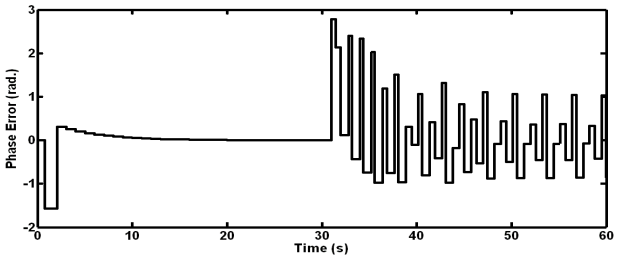
(b)

Figure 17 Phase error response for negative input frequency step of -0.3 V (a) second-order TDTL-LPD and (b) second-order TDTL, $\psi = \pi/2$ (rad), r =1.2 and $K_1 = 1$.

The locking range performance of the TDTL-LPD was tested and compared to that of the original TDTL. Figure 18 shows an example of such tests with a frequency step of 0.6 V. As can be seen, in Figure 18a, the original TDTL goes out of lock while in Figure 18b the TDTL-LPD attains the locking condition. A moderate improvement is achieved in the acquisition time of the second-order TDTL-LPD in comparison with the conventional TDTL. This will be investigated in detail in the following section.



(a)



(b)

Figure18 Second-order response for positive input frequency step of 0.6 V (a) TDTL-LPD and (b) TDTL, $\psi = \pi/2$ (rad), r =1.2 and $K_1 = 1$.

4.2 Second-order TDTL with Improved locking range and acquisition

As stated earlier and based on the responses in Figures 16 and 17, the acquisition speed of the second-order TDTL-LPD needs to be improved further. An improvement in the sampling will enhance the loop acquisition due to the accumulation path nature of the digital loop filter. This results in speeding up the time to reach the zero steady-state as proposed in the TDTL with wide locking range and fast acquisition (TDTL-WFA) architecture (Al-Araji, Al-Kharji Al-Ali, Al-Qutayri, Anani, and Ponnapalli 2010).

In order achieve faster acquisition the DCO unit is revised as illustrated in Figure 19. The idea is to boost the free running frequency of the DCO by a factor 'M', which is then used to accelerate the response of the loop digital filter. As shown in Figure 19, the free running frequency of the DCO is subsequently divided by the 'M' so as to preserve the loop sampling rate. The remaining blocks of Figure 19 are similar to the original TDTL-LPD. The performance of the second-order TDTL-LPD was compared with that of the improved second-order TDTL-WFA through an extensive set of tests. In those tests the oscillator's free running frequency was doubled by setting M=2.

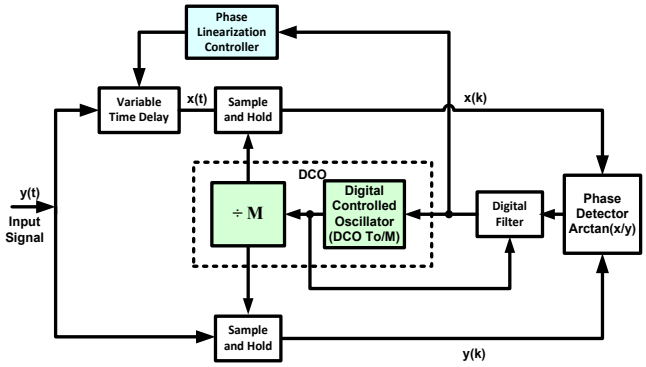
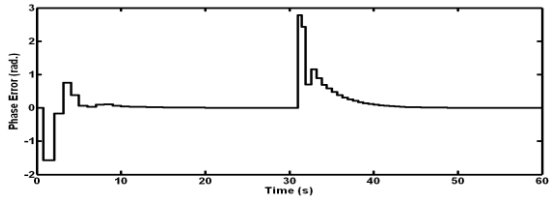


Figure19 Block diagram of the TDTL-WFA system.

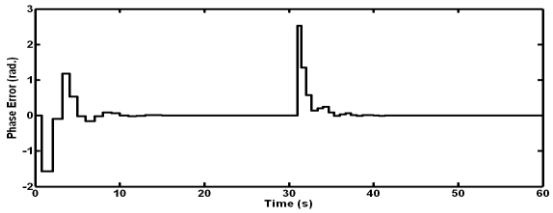
As in previous cases, the tests involved subjecting the loop to the same frequency steps that resemble sudden changes in the frequency of the incoming signal,

and comparing their responses. The results of the TDTL-WFA response show that it outperforms the TDTL-LPD. The responses of both loops to a positive frequency step of 0.4 V and a negative frequency step of -0.3 V, while the loops are inside their locking range, are shown in Figures 20 and 21 respectively. In both cases, the TDTL-WFA required considerable less number of sample times compared to the TDTL-LPD to converge to zero steady-state phase error and hence achieves full locking.

As can be expected, the acquisition speed of the TDTL-WFA can be improved by increasing the value of 'M'. This is demonstrated in Figure 22 by increasing M from 2 to 4 while applying a frequency modulated (FM) input signal, which shows that the peak of the error for M=4 is nearly half that for M=2.

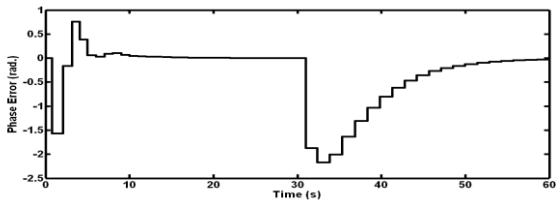


(a)

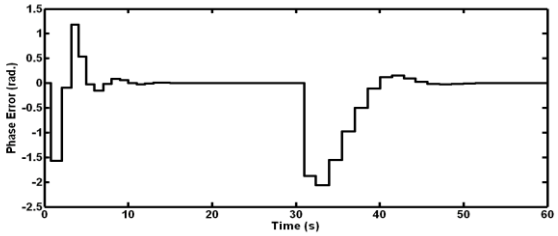


(b)

Figure 20 Phase error responses for positive input frequency step of 0.4 V (a) second-order TDTL-LPD and (b)second-order TDTL-WFA, $\psi = \pi / 2$ (rad), r =1.2 and $K_1 = 1$.



(a)



(b)

Figure 21 Phase error responses for negative input frequency step of -0.3 V (a) second-order TDTL-LPD and (b) second-order TDTL-WFA, $\psi = \pi/2$ (rad)., r =1.2 and $K_1 = 1$.

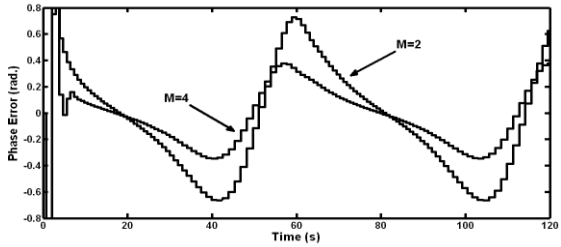


Figure 22 Phase error response of the TDTL-WFA as M is doubled with an FM input signal, $\psi = \pi/2$ (rad), r =1.2 and $K_1 = 1$.

4.3 An adaptive first-order TDTL with zero phase error (ATDTL-ZPE)

An adaptive TDTL with zero steady-state phase error (ATDTL-ZPE) (Al-Kharji Al-Ali, Al-Araji, Anani, Al-Qutayri, and Ponnapalli 2010) that overcomes the non-zero steady-state error of the first-order TDTL is examined in this section. In addition to eliminating the non-zero phase error, the architecture extends the loop locking range.

Compared to the original TDTL, the ATDTL-ZPE shown in Figure 23 incorporates a Frequency Estimator Controller (FEC) and an Adder block. The main concept behind this architecture is the use of these blocks to initialize the loop DCO to generate a frequency that matches that of the incoming signal. Hence, the new blocks in the ATDL-ZPE enable frequency tracking, as the DCO samples the input signal at its frequency and that frees the loop to work on tracking and correcting the phase error generated at the arctan phase detector output. This process enables the reduction of the first-order loop steady-state phase error to zero. An added advantage of this architecture is the widening of the loop locking range. This is achieved through a

transparent translation or shift process of the loop locking range to the anticipated frequency range. To linearize its phase, the ATDTL-ZPE shown in Figure 23 uses a variable delay block as the case in the TDTL-LPD (Al-Qutayri et al., 2009).

As can be seen in Figure 24, the FEC block of the ATDTL-ZPE consists of a derivative function, subtractor block, gain block, low-pass filter, multiplier, and a constant reference value of the DCO free running frequency (F0). The delayed signal is multiplied with the signal generated by the derivative block. The signal that results from this multiplication is fed to the low-pass filter which detects its envelope.

The DCO is initialized by the FEC, Figure 25, so that the incoming signal is sampled at a rate that equals its frequency but with a different phase. Subsequently the loops works at reducing this phase error, which manifests itself at the output of the arctan, phase detector.

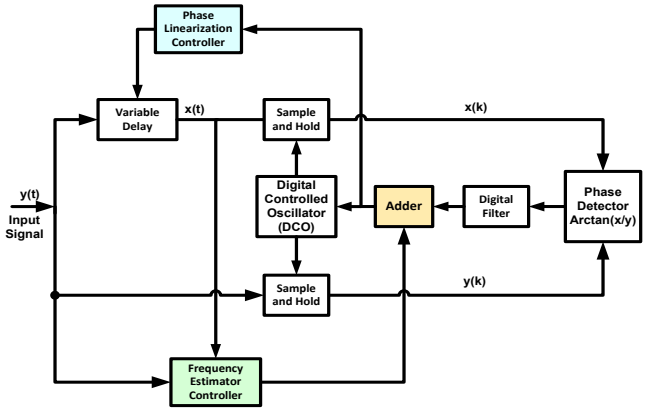


Figure23Architecture of the ATDTL-ZPE.

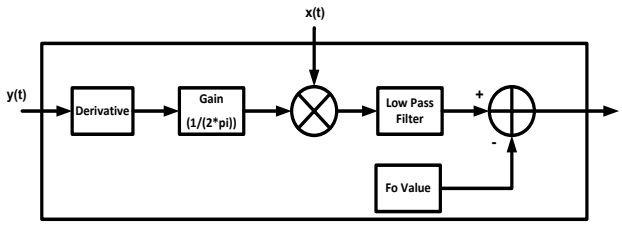
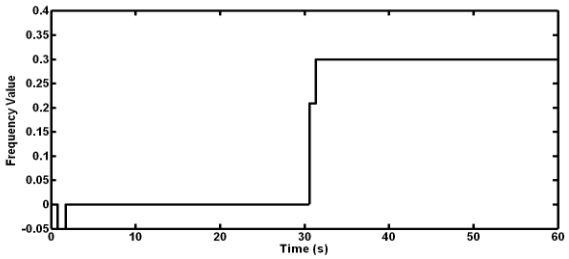


Figure24 block diagram of the Frequency estimator controller.

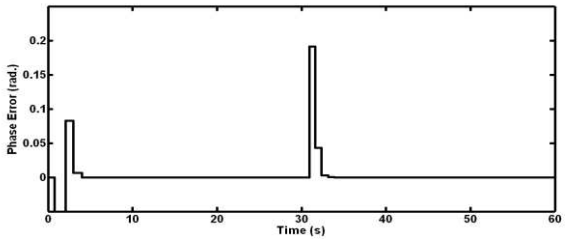
The locking range of the ATDTL-ZPE is similar to that of the first-order TDTL-LPD depicted in Figure 12. However, due to the initialization process of the DCO

frequency the ATDTL-ZPE has the ability to swiftly change the locking range to the exact frequency. As a result, it will constantly operate with W=1 keeping K_1 at the initial value of 1. However, K_1 must be maintained inside the interval $0 < K_1 < 2$ for the loop to remain locked.

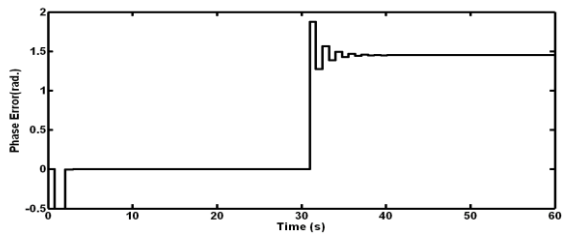
As in previous cases, the performance of the ATDTL-ZPE was compared to that of the original first-order TDTL by subjecting both loops to the same input frequency steps. The response of both loops to a positive frequency step of 0.3 V is illustrated in Figure 25. In addition to the input frequency step, Figure 25 shows the output of the carrier estimator controller, and the phase errors of both loops. It is evident from Figure 25 that the ATDTL-ZPE achieves the desired zero steady-state phase error. A similar test was performed using a negative step of -0.3 V and the results are shown in Figure 26. In both Figures 25 and 26, the ATDTL-ZPE achieves faster acquisition time compared to original TDTL. As indicated earlier this is due to the initialization process.



(a)

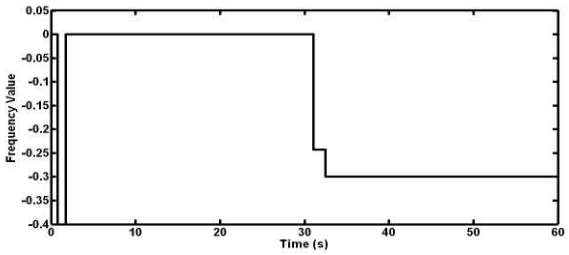


(b)

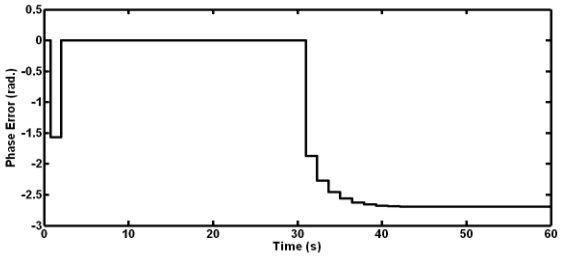


(c)

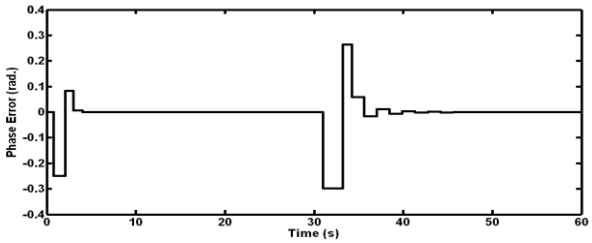
Figure 25 First order TDTL phase-error to positive frequency step input 0.3 V (a) FEC, (b) ATDTL-ZPE and (c) TDTL, $\psi = \pi/2$ (rad). and $K_1 = 1$.



(a)



(b)



(c)

Figure 26 First order TDTL response to negative frequency step input -0.3 V, (a) FEC, (b) ATDTL-ZPE and (c) TDTL, $\psi = \pi/2$ (rad).and $K_1 = 1$.

5. Noise, Jitter and BER Performance Tests

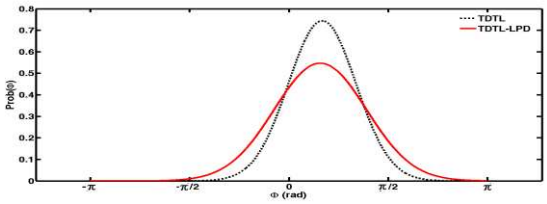
The effects of noise on the operation of the different TDTL architectures presented above are presented in this section. The noise performances are assessed using the probability density function (pdf). In the assessment, the input signal is assumed to have been corrupted by a zero mean additive white Gaussian noise (AWGN) which has two-sided power spectrum density of $G_{nw}(f) = n_o/2$ (Peyton, and Peeblesand, 1993; Haykin, and Moher, 2009; Skiller, and Huang, 2000). Therefore, autocorrelation may be obtained using the inverse Fourier Transform of $G_{nw}(f)\, G_{nw}(f)$as $R(\tau) = n_o\delta(\tau)/2$, where $\delta(\tau)$ represents the unit impulse function. Consequently,

$R(\tau) = 0$ for $\tau \neq 0$, hence any two samples of this form of noise are uncorrelated and therefore, they are statistically independent (Hussain, 2005; Pomalaza-Raez, 1988; Mehrotra, 2002; Ibrahim, and Hamadamin, 2006; Al-Kharji Al-Ali, Anani, Al-Araji, Al-Qutayri, and Ponnapalli, 2012).

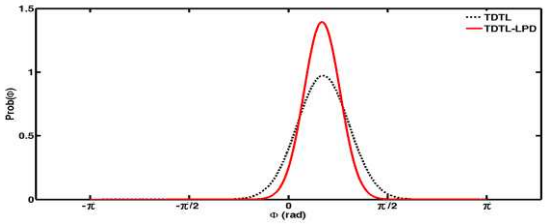
Figures 27 and 28 show some specimens of the extensive simulation results. In Figure 27, the TDTL-LPD outperforms the original TDTL for an SNR over 5 dBs. This is due to the fact that the use of the fixed delay block, in the TDTL, increases the phase-detector nonlinearity as the SNR increases.

The results in Figure 28 demonstrate that the performance of the ATDTL-ZPE surpasses that of the TDTL-WFA due to the fact that the ATDTL-ZPE is only used for phase synchronization as explained earlier. Furthermore, Figure 28 demonstrates that the ATDTL-ZPE and the TDTL-WFA outperform the second-order TDTL for SNR above 5 dBs. This is because when the TDTL-WFA is subjected to a fairly noisy environment, the fast acquisition characteristic will produce a reverse effect in delivering a fast settling time to the steady-state condition. However, since the ATDTL-ZPE makes use of the FEC to accomplish frequency tracking, the loop is only required to attain phase synchronizing.

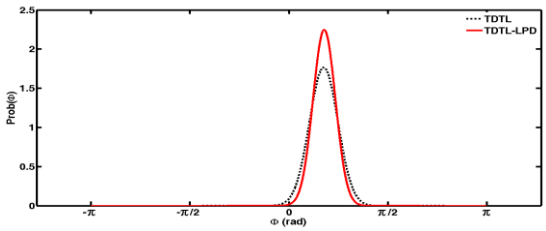
In very noisy environments i.e. when the SNR is less than 5 dBs, the FEC block cannot deliver the exact frequency value required by the TDTL loop and this results in degraded noise performance. Figure 29 illustrates the effect of noise on the jitter performance. From the figure, the ATDTL-ZPE gives the best performance while the original second-order TDTL gives the worse jitter. The reasons for these variations are the additional blocks that were introduced to the ATDTL-ZPE, TDTL-WFA and TDTL-LPD to improve various aspects of their individual performance.



(a)

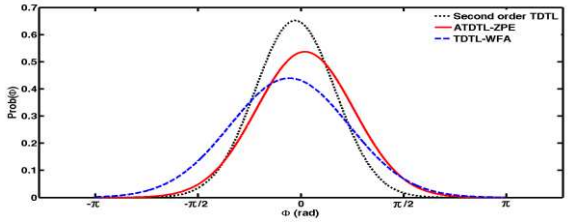


(b)

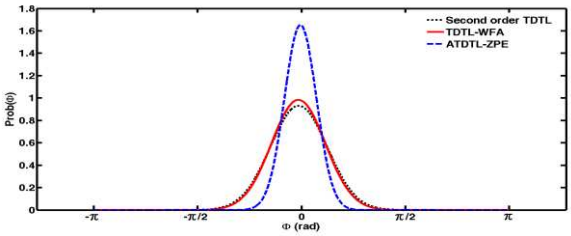


(c)

Figure 27 Noise performance od the first order architectures (a) SNR=5 dB (b) SNR=10 dB and (c) SNR=15 dB. $K_1 = 1$ and frequency step of 0.1 V.



(a)



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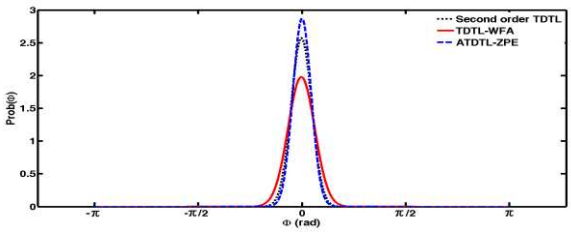
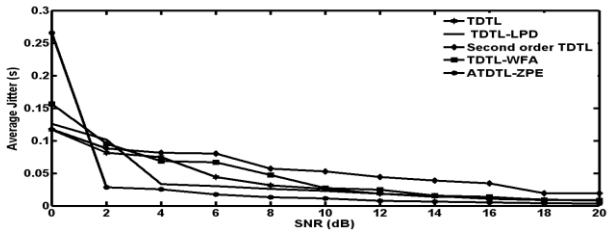
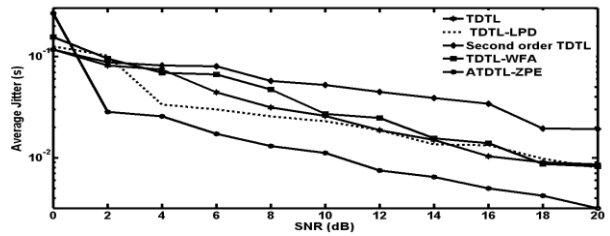


(c)

Figure 28 Noise performance of the second-order architectures with the SNR (a) SNR=5 dB (b) SNR=10 dB and (c) SNR=15 dB. $K_1 = 1$ and frequency step of 0.1 V.



(a)



(b)

Figure 29 Variation of the Jitter with SNR (a) linear scale and (b) Logarithmic scale, $K_1 = 1$ and step inputs of 0.1 V.

The performance of all the proposed TDTL based architectures, including the original TDTL, was evaluated under slow as well as fast fading channel conditions. In the case of slow fading channels, the performance of the various architectures was found to be almost similar. This is an expected result because under slow fading, the particular system loop will only need to deal with relatively small changes in the input signal. However, under fast fading conditions the performance of the improved TDTL architectures showed noticeable improvement compared to the original TDTL. This is due to the improved characteristics of the proposed architectures, such as wider locking range and higher acquisition speed, which enable them to cope with the relatively larger changes in the input signal. The improvement under fast fading conditions is demonstrated by the BER results in Figure 30. The BER performance was evaluated using a constant envelope orthogonal frequency division multiplexing (CEOFDM) with a phase shift keying (8-PSK) mapping at the transmitter.

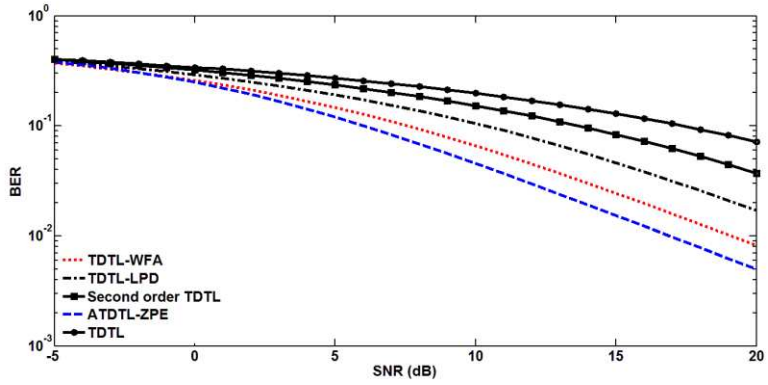


Figure 30 BER performance of different TDTL enhanced architectures for CEOFDM modulations under fast varying channel.

6. Conclusions

This paper presented a variety of system architectures to overcome some of the limitations of the original first- and second-order TDTL systems. The proposed TDTL-LPD overcame the nonlinearity associated with the original TDTLs by incorporating a phase linearization block. The TDTL-WFA system resolved the acquisition speed limitation of the second-order TDTL-LPD through the introduction of a modified DCO that over drives the digital loop filter. A widening of the lock range was achieved as an additional advantage of this process by seamlessly shifting the TDTL lock range to a specific frequency and hence preserving locking by maintaining the loop operating frequency at W=1. The non-zero phase error convergence of the first order TDTL was resolved by the ATDTL-ZPE, which has an adaptive mechanism targeted at solving this problem. The ATDTL-ZPE also achieved wider locking range than the original TDTL.

All the proposed systems architectures, TDTL-LPD, TDTL-WFA and TDTL-ZPE, achieved significantly better overall performance than the original TDTL when evaluated under noisy conditions. Each of the said architectures was targeted at improving a particular aspect of the system performance. Consequently, the choice of an individual system will vary according to a given set of requirements. For applications

that demand high acquisition speeds, the TDTL-WFA system can be employed. However, the ATDTL-ZPE delivers best noise performance. Finally, improved linearity was the objective of the TDTL-LPD. The performance of all TDTL architectures was assessed under fast fading channel conditions. The results demonstrated that the modified architectures provided improved BER performance over the original TDTL architecture.

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